Atmel SAM D10

SMART ARM-Based Microcontroller

DATASHEET SUMMARY

Description

The Atmel® | SMART™ SAM D10 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 14- to 24-pins with up to 16KB Flash and 4KB of SRAM. The SAM D10 devices operate at a maximum frequency of 48MHz and reach 2.46 Coremark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces. The SAM D10 series is compatible to the other product series in the SAM D family, enabling easy migration to larger device with added features.

The Atmel SAM D10 devices provide the following features: In-system programmable Flash, six-channel direct memory access (DMA) controller, 6 channel Event System, programmable interrupt controller, up to 22 programmable I/O pins, 32-bit real-time clock and calendar, two 16-bit Timer/Counters (TC) and one 24-bit Timer/Counter for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and one timer/counter has extended functions optimized for motor, lighting and other control applications. The series provide up to three Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I^2C up to 3.4MHz, SMBus, PMBus and LIN slave; up to 10-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, two analog comparators with window mode, Peripheral Touch Controller supporting up to 72 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM D10 devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug and trace of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The Atmel SAM D10 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

Features

- Processor
  - ARM Cortex-M0+ CPU running at up to 48MHz
    - Single-cycle hardware multiplier
    - Micro Trace Buffer
- Memories
  - 8/16KB in-system self-programmable Flash
  - 4KB SRAM Memory
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options with 48MHz Digital Frequency Locked Loop (DFLL48M) and 48MHz to 96MHz Fractional Digital Phase Locked Loop (FDPLL96M)
  - External Interrupt Controller (EIC)
  - 8 external interrupts
  - One non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
  - Idle and standby sleep modes
  - SleepWalking peripherals
- Peripherals
  - 6-channel Direct Memory Access Controller (DMAC)
  - 6-channel Event System
  - Two 16-bit Timer/Counters (TC), configurable as either:
    - One 16-bit TC with compare/capture channels
    - One 8-bit TC with compare/capture channels
    - One 32-bit TC with compare/capture channels, by using two TCs
  - One 24-bit Timer/Counters for Control (TCC), with extended functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - Up to three Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - I^2C Bus up to 3.4MHz
    - SMBUS/PMBUS
    - SPI
    - LIN slave
  - 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to 10 channels
    - Differential and single-ended input
    - 1/2x to 16x programmable gain stage
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - 10-bit, 350ksps Digital-to-Analog Converter (DAC)
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC)
    - Up to 72-channel capacitive touch and proximity sensing
- I/O
  - Up to 22 programmable I/O pins
- Packages
  - 24-pin QFN
  - 20-pin SOIC
  - 20-ball WLCSP
  - 14-pin SOIC
- Operating Voltage
  - 1.62V – 3.63V

1. Configuration Summary

Table 1-1. Configuration Summary

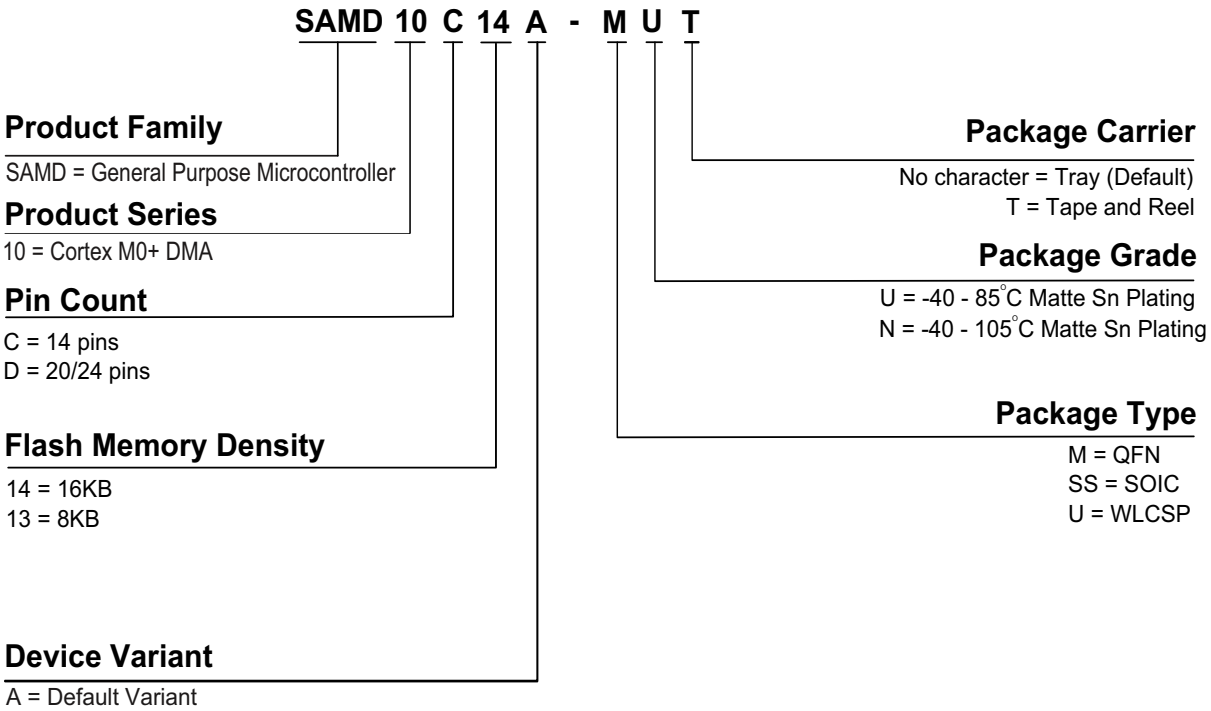
	SAM D10D – 24-pin QFN	SAM D10D – 20-pin SOIC / WLCSP	SAM D10C – 14-pin SOIC
Pins	24	20	14
General Purpose I/O-pins (GPIOs)	22	18	12
Flash	16/8KB	16/8KB	16/8KB
SRAM	4KB	4KB	4KB
Timer Counter (TC)	2	2	2[3]
Waveform output channels for TC	2	2	2
Timer Counter for Control (TCC)	1	1	1
Waveform output channels per TCC	8	8	8
DMA channels	6	6	6
Serial Communication Interface (SERCOM)	3	3	2
Analog-to-Digital Converter (ADC) channels	10	8	5
Analog Comparators (AC)	2	2	2
Digital-to-Analog Converter (DAC) channels	1	1	1
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1

Table 1-1. Configuration Summary (Continued)

	SAM D10D – 24-pin QFN	SAM D10D – 20-pin SOIC / WLCSP	SAM D10C – 14-pin SOIC
RTC compare values	1 32-bit value or 2 16-bit values	1 32-bit value or 2 16-bit values	1 32-bit value or 2 16-bit values
External Interrupt lines	8	8	8
Peripheral Touch Controller (PTC) channels (X- x Y-lines) for mutual capacitance(1)	72 (9x8)	42 (7x6)	12 (4x3)
Peripheral Touch Controller (PTC) channels for self capacitance (Y-lines only)(2)	16	13	7
Maximum CPU frequency	48MHz	48MHz	48MHz
Packages	QFN	SOIC / WLCSP	SOIC
Oscillators	32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHzinternal oscillator (OSC32K) 32kHz ultra-low-power internal oscillator (OSCULP32K) 8MHz high-accuracy internal oscillator (OSC8M) 48MHz Digital Frequency Locked Loop (DFLL48M) 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)		
Event System channels	6	6	6
SW Debug Interface	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes

Notes:
1. The number of X- and Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. The number in the "Configuration Summary" on page 3 is the maximum number of channels that can be obtained.
2. The number of Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. The number given here is the maximum number of Y-lines that can be obtained.
3. The signals for TC2 are not routed out on the 14-pin package.

2. Ordering Information



2.1 SAM D10C – 14-pin SOIC

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD10C13A-SSUT	8K	4K	SOIC14	Tape & Reel
ATSAMD10C13A-SSNT	8K	4K	SOIC14	Tape & Reel
ATSAMD10C14A-SSUT	16K	4K	SOIC14	Tape & Reel
ATSAMD10C14A-SSNT	16K	4K	SOIC14	Tape & Reel

2.2 SAM D10D – 20-pin SOIC

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD10D13A-SSUT	8K	4K	SOIC20	Tape & Reel
ATSAMD10D13A-SSNT	8K	4K	SOIC20	Tape & Reel
ATSAMD10D14A-SSUT	16K	4K	SOIC20	Tape & Reel
ATSAMD10D14A-SSNT	16K	4K	SOIC20	Tape & Reel

2.3 SAM D10D – 20-ball WLCSP

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD10D14A-UUT	16K	4K	WLCSP20	Tape & Reel

2.4 SAM D10D – 24-pin QFN

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD10D13A-MUT	8K	4K	QFN24	Tape & Reel
ATSAMD10D13A-MNT	8K	4K	QFN24	Tape & Reel
ATSAMD10D14A-MUT	16K	4K	QFN24	Tape & Reel
ATSAMD10D14A-MNT	16K	4K	QFN24	Tape & Reel

2.5 Device Identification

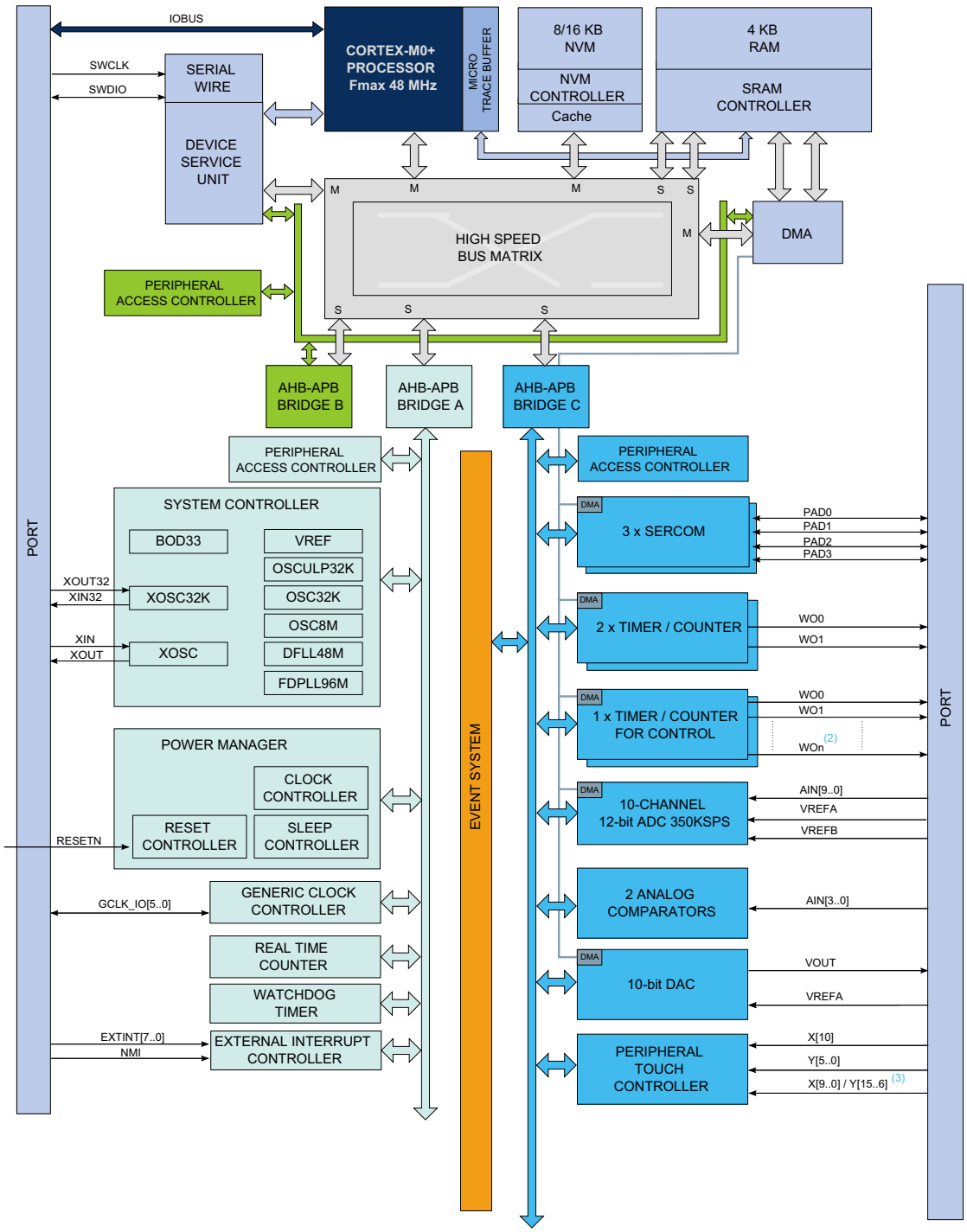
The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The device variants have a reset value of DID=0x1001drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

Table 2-1. Device Identification Values

Device Variant	DID.DEVSEL	Device ID (DID)
SAMD10D14AM	0x00	0x10020r00
SAMD10D13AM	0x01	0x10020r01
Reserved	0x02	
SAMD10D14ASS	0x03	0x10020r03
SAMD10D13ASS	0x04	0x10020r04
Reserved	0x05	
SAMD10C14A	0x06	0x10020r06
SAMD10C13A	0x07	0x10020r07
Reserved	0x08	
SAMD10D14AU	0x09	0x10020r09

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die. The device variant denotes functional differences, whereas the die revision marks evolution of the die

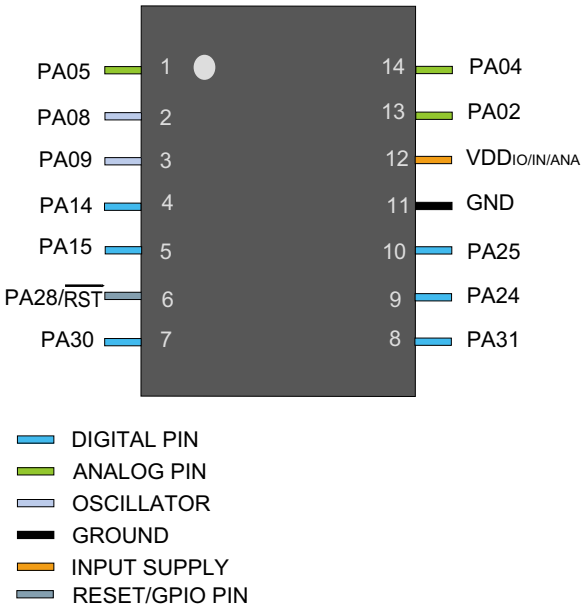
3. Block Diagram



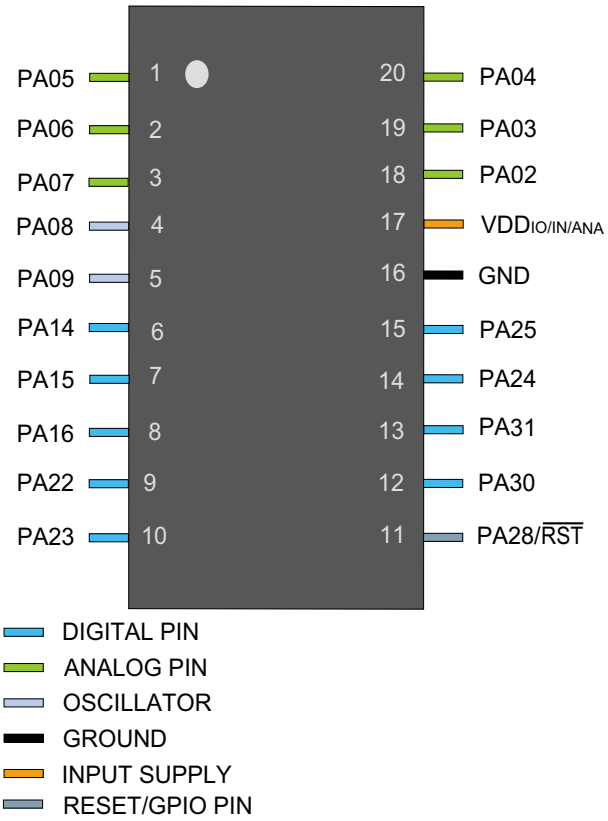
Notes:
1. Some products have different number of SERCOM instances, PTC signals and ADC signals.
2. The number of PTC X- and Y-lines depend on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines.

4. Pinout

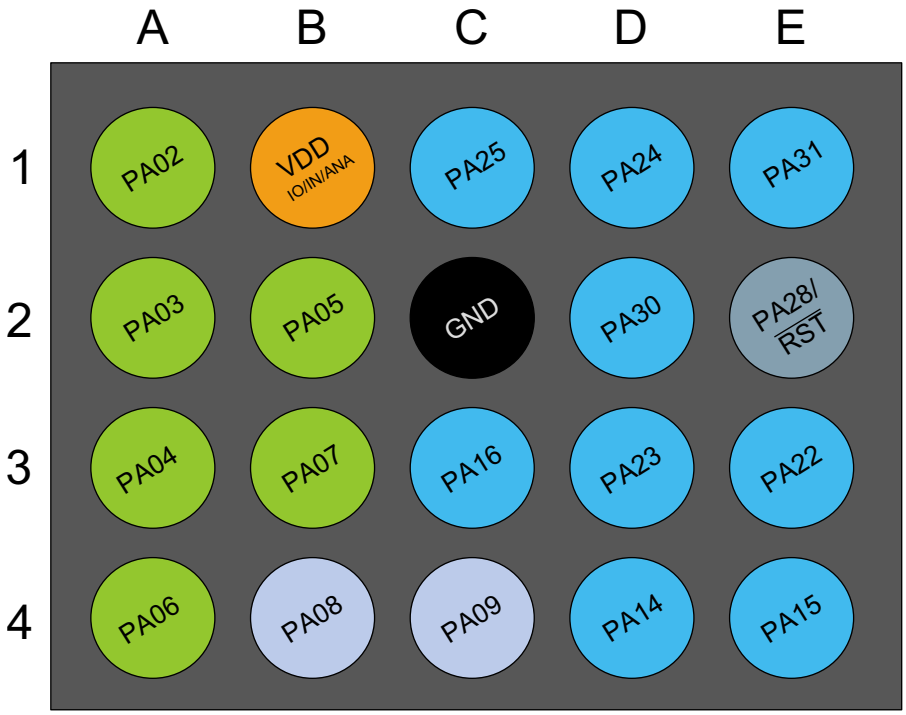
4.1 SAM D10C 14-pin SOIC



4.2 SAM D10D 20-pin SOIC

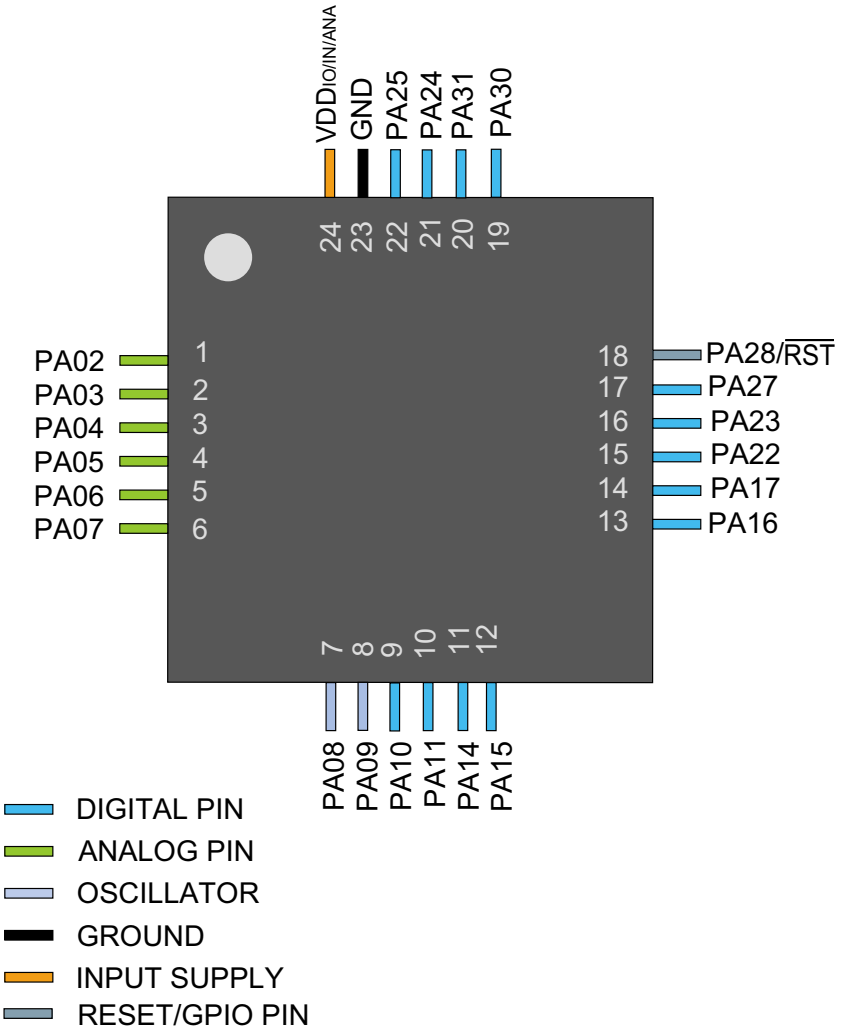


4.3 SAM D10D 20-ball WLCSP



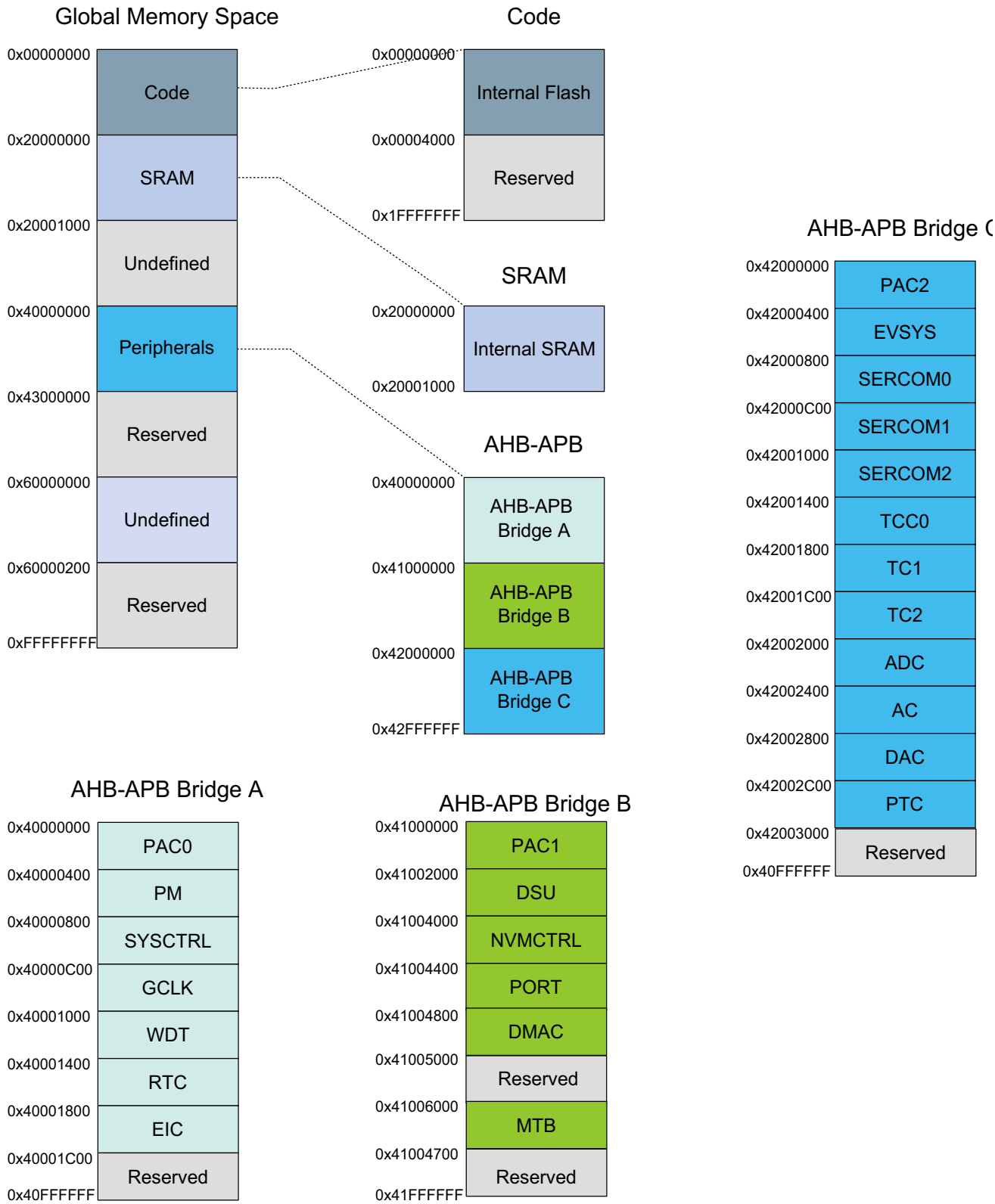
- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- GROUND
- INPUT SUPPLY
- REGULATED OUTPUT SUPPLY
- RESET PIN

4.4 SAM D10D 24-pin QFN



5. Product Mapping

Figure 5-1. Atmel SAM D10 Product Mapping



6. Processor And Architecture

6.1 Cortex M0+ Processor

The Atmel SAM D10 implements the ARM® Cortex™-M0+ processor, which is based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 processor, and upward compatible to Cortex-M3 and M4 processors.

For more information refer to www.arm.com.

6.1.1 Cortex M0+ Configuration

Features	Configuration option	Atmel SAM D10 configuration
Interrupts	External interrupts 0-32	32
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Absent(1)
Memory Protection Unit	Not present or 8-region	Not present
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

Note: 1. All software run in privileged mode only

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA®-3 AHB-Lite™ system interface that provides connections to peripherals and all system memory, including flash and RAM
- Single 32-bit I/O port bus interfacing to the PORT with one-cycle loads and stores

7. Packaging Information

7.1 Thermal Considerations

7.1.1 Thermal Resistance Data

Table 6-1 on page 13 summarizes the thermal resistance data depending on the package.

Table 7-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}	Units
24-pin QFN	61.7	25.4	°C/W
20-pin SOIC	44.0	21.0	°C/W
20-ball WLCSP	37.4	6.6	°C/W
14-pin SOIC	58.5	26.3	°C/W

7.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

Equation 1

$$T_J = T_A + (P_D \times \theta_{JA})$$

Equation 2

$$T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$$

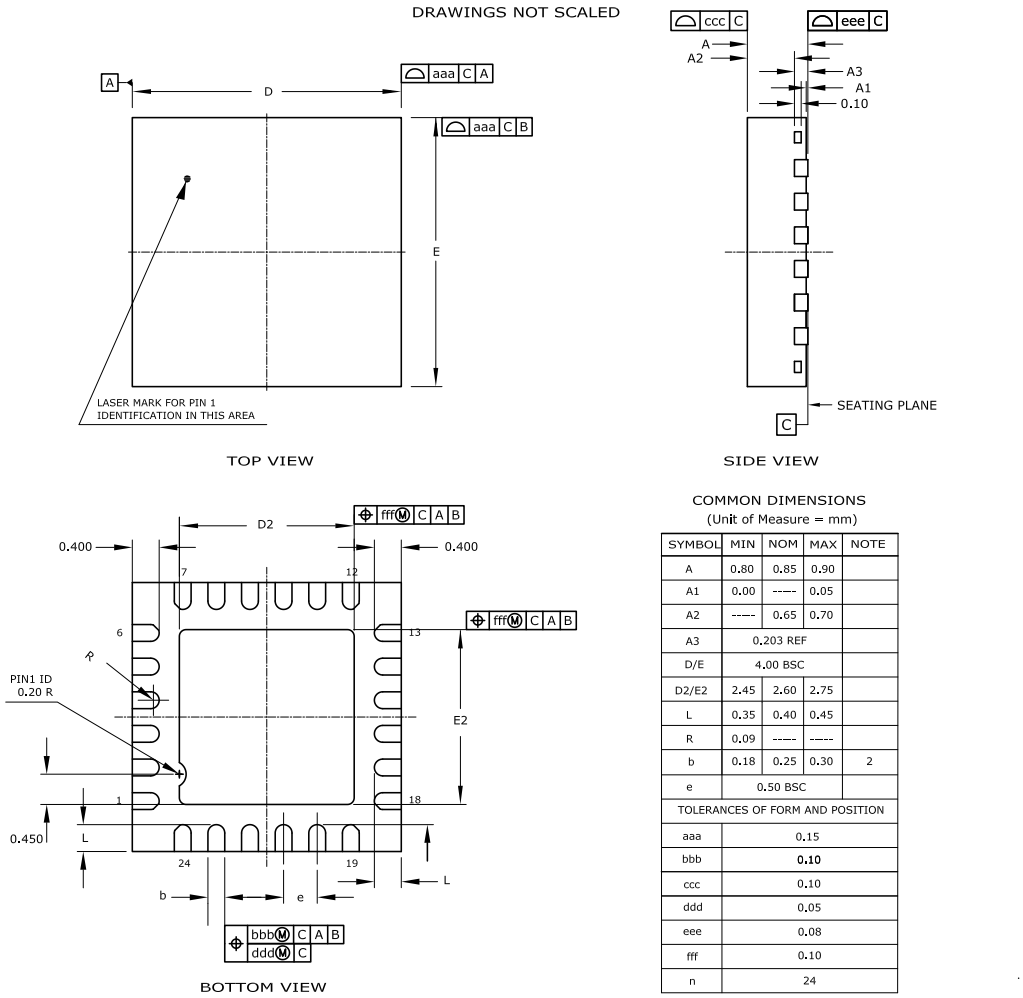
where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 6-1 on page 13.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 6-1 on page 13.
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W).
- T_A = ambient temperature (°C).

From the *Equation 1*, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

7.2 Package Drawings

7.2.1 24-pin QFN



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
A1	0.00	-----	0.05	
A2	-----	0.65	0.70	
A3		0.203 REF		
D/E		4.00 BSC		
D2/E2	2.45	2.60	2.75	
L	0.35	0.40	0.45	
R	0.09	-----	-----	
b	0.18	0.25	0.30	2
e		0.50 BSC		
TOLERANCES OF FORM AND POSITION				
aaa		0.15		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
fff		0.10		
n		24		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VGGD-6 for proper dimensions, tolerances, datums, etc. (excepted D2/E2 Min et Nom).
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

02/18/2014

Table 7-2. Device and Package Maximum Weight

44	mg

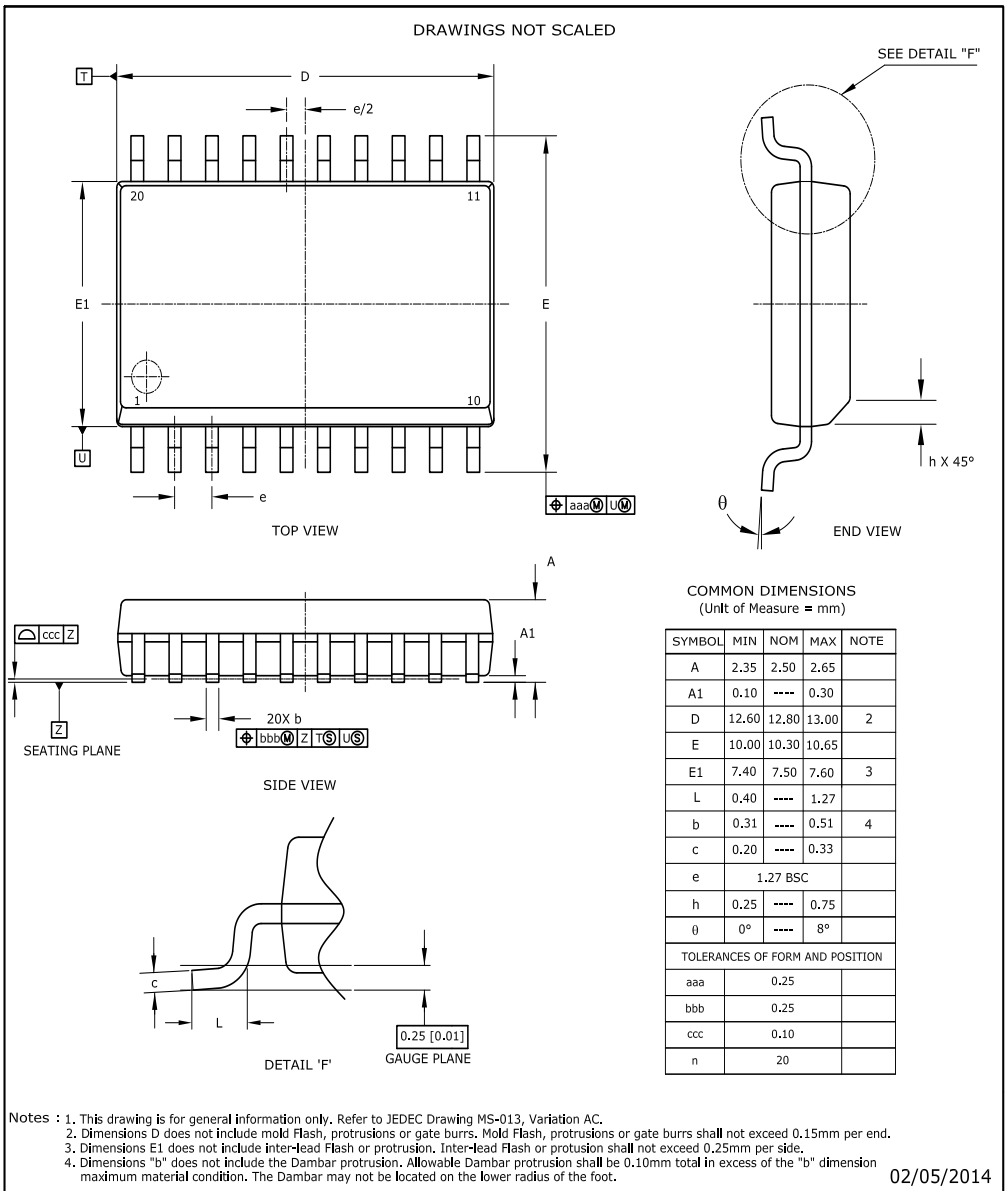
Table 7-3. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 7-4. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

7.2.2 20-pin SOIC



SYMBOL	MIN	NOM	MAX	NOTE
A	2.35	2.50	2.65	
A1	0.10	----	0.30	
D	12.60	12.80	13.00	2
E	10.00	10.30	10.65	
E1	7.40	7.50	7.60	3
L	0.40	----	1.27	
b	0.31	----	0.51	4
c	0.20	----	0.33	
e	1.27 BSC			
h	0.25	----	0.75	
θ	0°	----	8°	
TOLERANCES OF FORM AND POSITION				
aaa	0.25			
bbb	0.25			
ccc	0.10			
n	20			

Table 7-5. Device and Package Maximum Weight

530	mg

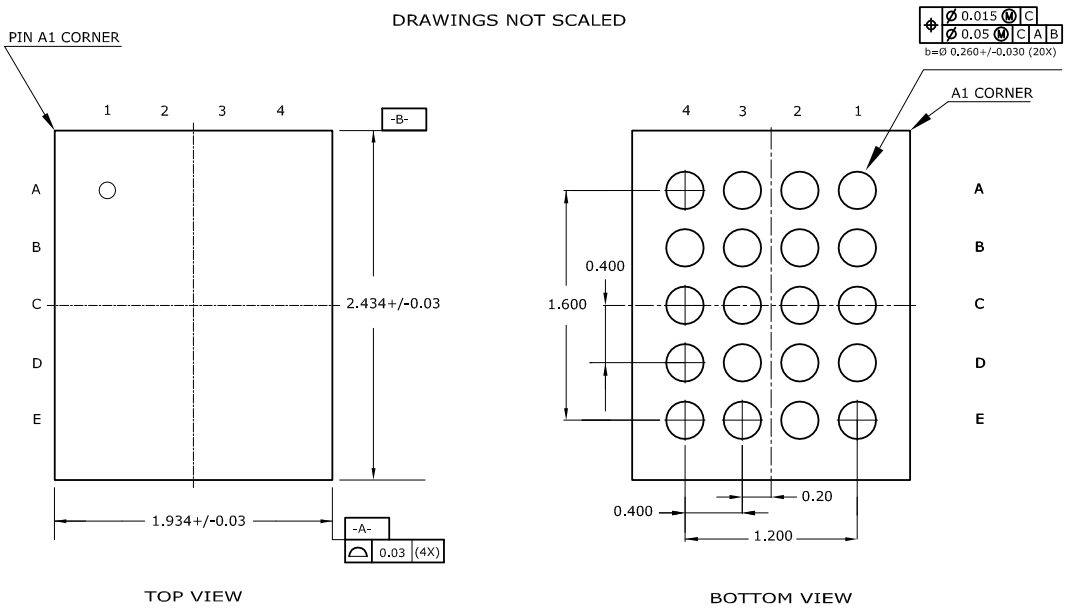
Table 7-6. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 7-7. Package Reference

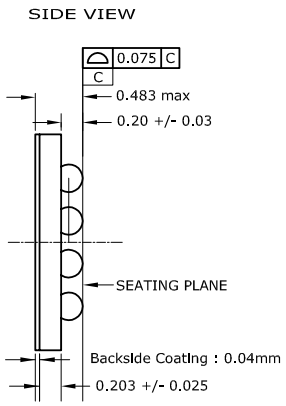
JEDEC Drawing Reference	MS-013
JESD97 Classification	E3

7.2.3 20-ball WLCSP



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PA02	0.6	0.8
A2	PA03	0.2	0.8
A3	PA04	-0.2	0.8
A4	PA06	-0.6	0.8
B1	VDD	0.6	0.4
B2	PA05	0.2	0.4
B3	PA07	-0.2	0.4
B4	PA08	-0.6	0.4
C1	PA25	0.6	0
C2	GND	0.2	0
C3	PA16	-0.2	0
C4	PA09	-0.6	0
D1	PA24	0.6	-0.4
D2	PA30	0.2	-0.4
D3	PA23	-0.2	-0.4
D4	PA14	-0.6	-0.4
E1	PA31	0.6	-0.8
E2	PA28	0.2	-0.8
E3	PA22	-0.2	-0.8
E4	PA15	-0.6	-0.8



Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

Table 7-8. Device and Package Maximum Weight

7	mg

Table 7-9. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 7-10. Package Reference

JEDEC Drawing Reference	MS-220
JESD97 Classification	E8

7.2.4 14-pin SOIC

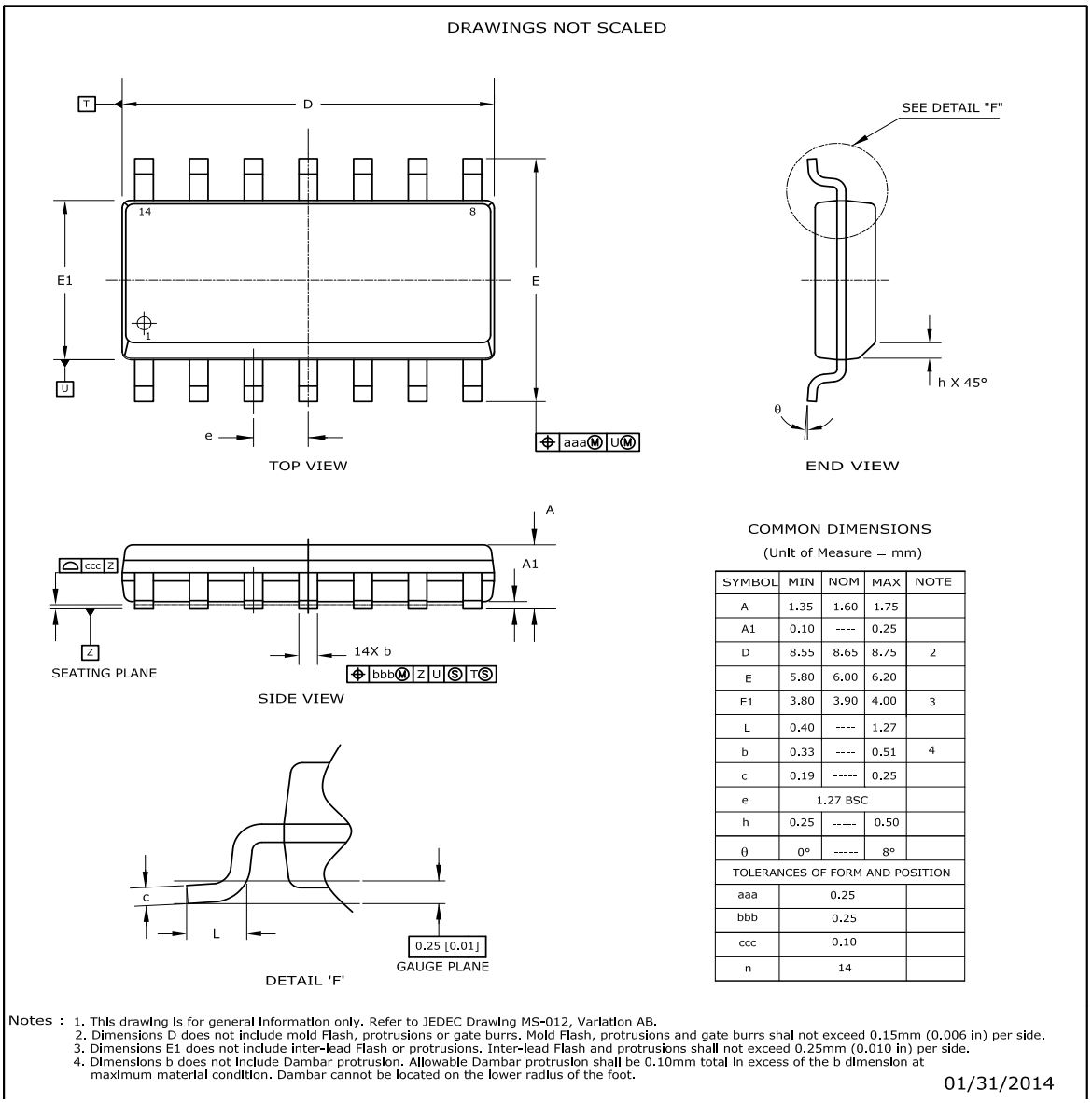


Table 7-11. Device and Package Maximum Weight

230	mg

Table 7-12. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 7-13. Package Reference

JEDEC Drawing Reference	MS-012
JESD97 Classification	E3

7.3 Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max
Preheat Temperature 175°C +/-25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

A maximum of three reflow passes is allowed per component.

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