AVR600: STK600 Expansion, routing and socket boards

AMEL®

8-bit **AVR**® Microcontrollers

Application Note

1 Introduction

This application note describes the process of developing new routing, socket and expansion cards for the STK[®]600. It also describes the physical parameters for creating such cards.

The STK600 starter kit from Atmel has a sandwich design to match a specific part package and pin out to the generic pin headers. It also features an expansion area where most part pins are available.

While the variety of IC packages is relatively limited, the number of possible pin outs increases rapidly with the number of pins. i.e. a 6 pin IC can have 720 (6!) different pin outs!

The routing / socket card design provides a low cost solution to support upcoming devices as the socket is the cost driving factor.

STK600 users might also want to create their own routing cards to include specialized hardware to prototype their design.

Figure 1-1. STK600 router and socket card



Rev. 8170B-AVR-12/10





2 Routing cards

The routing cards sit between the generic socket card and the STK600. It has one pair of electric pads underneath to mate with the STK600 spring loaded connector, and one pair of pads on top where the socket card connector connects. A part specific card with the target IC soldered on can be viewed as a routing card without the top pads.

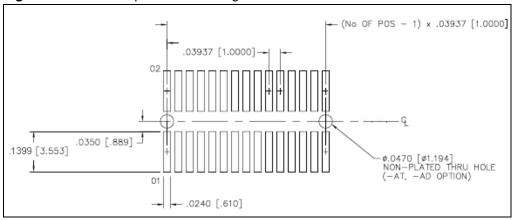
2.1 Connector footprints

A Routing card should have pads to mate with the following spring loaded connectors:

Table 2-1. Router card connectors

| Manufacturer and MPN | Quantity | Comment |
|---------------------------|----------|------------------------------|
| SAMTEC, FSI-140-03-G-D-AD | 2 | 80 pins To socket card (top) |
| SAMTEC, FSI-150-03-G-D-AD | 2 | 100 pins To STK600 (bottom) |

Figure 2-1. PCB land pattern for mating to FSI connectors



2.2 Physical dimensions and component placement

82mm

69mm

69mm

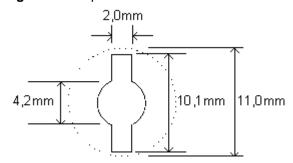
69mm

60mm

90 deg angle on routing card

Figure 2-2. Routing card connector pad placement and dimensions

Figure 2-3. Clip hole dimensions



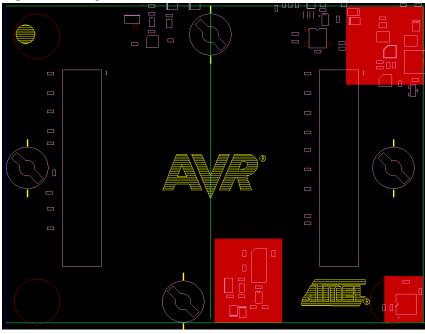
The board thickness should be 1.6mm to be compatible with the clips.

Note that components on the main board might conflict with through hole mounted or secondary side mounted components. Areas with such components are highlighted in the next figure





Figure 2-4. Height restricted areas due to main board components



2.3 STK600 socket connectors pinout

The following figure shows the pinout for the STK600 headers. This correspond to the routing card connectors J1 and J2 $\,$

PA[7.0] 🔇 PJ[7.0] 🕸 9 111 131 151 177 29 21 23 33 35 37 39 41 43 33 46 49 51 56 67 77 73 78 88 89 91 92 98 99 99 99 99 VTGC GND VTGC GND 141
16
18
20
24
28
30
32
34
36
38
40
42
44
46
56
56
67
68
87
77
78
88
88
89
99
99
96
96 VTG GND PC[7.0] (\$\) PC[7.0] VTG GND GND PM1 VTGC VTG PD[7.0] ((>) ⟨⟨⟨>PDI7.01< PM[7.0] <<>> GND VTGO PE[7..0] ((>) (C) PE[7..0] PN[7.0] <<>> VTG GND PF[7.0] (\$\infty\$) VTGC PP[7.0] (\(\right)) VTG PG[7..0] ((>) 62 64 66 70 72 74 76 80 82 84 86 88 90 92 94 PQ[7..0] (\(\sigma\) VTG GND PH[7.0] (\$\infty) VBUST UVCON GND -IGND TGT_PDATA[7.0] <<> ♦ TGT_PDATA[7..0] GND TGT_PCTRL[7.0] FSI-150-03-G-D-AD DARD_ID[7.0] < >BOARD_ID[7..0]

Figure 2-5. STK600 Socket connectors pin out

Table 2-2. STK600 J201 left, routing card J1 connector pin out

| Signal name | Pin ı | number | Signal name |
|-------------|-------|--------|-------------|
| VTG | 2 | 1 | GND |
| PA1 | 4 | 3 | PA0 |
| PA3 | 6 | 5 | PA2 |
| PA5 | 8 | 7 | PA4 |
| PA7 | 10 | 9 | PA6 |
| VTG | 12 | 11 | GND |
| PB1 | 14 | 13 | PB0 |
| PB3 | 16 | 15 | PB2 |
| PB5 | 18 | 17 | PB4 |
| PB7 | 20 | 19 | PB6 |
| VTG | 22 | 21 | GND |
| PC1 | 24 | 23 | PC0 |
| PC3 | 26 | 25 | PC2 |
| PC5 | 28 | 27 | PC4 |
| PC7 | 30 | 29 | PC6 |
| VTG | 32 | 31 | GND |
| PD1 | 34 | 33 | PD0 |
| PD3 | 36 | 35 | PD2 |
| PD5 | 38 | 37 | PD4 |
| PD7 | 40 | 39 | PD6 |
| VTG | 42 | 41 | GND |
| PE1 | 44 | 43 | PE0 |
| PE3 | 46 | 45 | PE2 |
| PE5 | 48 | 47 | PE4 |
| PE7 | 50 | 49 | PE6 |
| VTG | 52 | 51 | GND |
| PF1 | 54 | 53 | PF0 |
| PF3 | 56 | 55 | PF2 |
| PF5 | 58 | 57 | PF4 |
| PF7 | 60 | 59 | PF6 |
| VTG | 62 | 61 | GND |
| PG1 | 64 | 63 | PG0 |
| PG3 | 66 | 65 | PG2 |
| PG5 | 68 | 67 | PG4 |
| PG7 | 70 | 69 | PG6 |
| VTG | 72 | 71 | GND |
| PH1 | 74 | 73 | PH0 |
| PH3 | 76 | 75 | PH2 |





| Signal name | Pin | number | Signal name |
|-------------|-----|--------|-------------|
| PH5 | 78 | 77 | PH4 |
| PH7 | 80 | 79 | PH6 |
| VTG | 82 | 81 | GND |
| AREF0 | 84 | 83 | XTAL1 |
| AREF1 | 86 | 85 | XTAL2 |
| TGT_MOSI | 88 | 87 | GND |
| TGT_MISO | 90 | 89 | TOSC1 |
| TGT_SCK | 92 | 91 | TOSC2 |
| TDI | 94 | 93 | TGT_RESET |
| TDO | 96 | 95 | GND |
| TMS | 98 | 97 | Vext |
| TCK | 100 | 99 | Vcc |

Table 2-3. STK600 J202 right, routing card connector J2 pin out

| Signal name | P | in number | Signal name |
|-------------|----|-----------|-------------|
| VTG | 2 | 1 | GND |
| PJ1 | 4 | 3 | PJ0 |
| PJ3 | 6 | 5 | PJ2 |
| PJ5 | 8 | 7 | PJ4 |
| PJ7 | 10 | 9 | PJ6 |
| VTG | 12 | 11 | GND |
| PK1 | 14 | 13 | PK0 |
| PK3 | 16 | 15 | PK2 |
| PK5 | 18 | 17 | PK4 |
| PK7 | 20 | 19 | PK6 |
| VTG | 22 | 21 | GND |
| PL1 | 24 | 23 | PL0 |
| PL3 | 26 | 25 | PL2 |
| PL5 | 28 | 27 | PL4 |
| PL7 | 30 | 29 | PL6 |
| VTG | 32 | 31 | GND |
| PM1 | 34 | 33 | PM0 |
| PM3 | 36 | 35 | PM2 |
| PM5 | 38 | 37 | PM4 |
| PM7 | 40 | 39 | PM6 |
| VTG | 42 | 41 | GND |
| PN1 | 44 | 43 | PN0 |
| PN3 | 46 | 45 | PN2 |
| PN5 | 48 | 47 | PN4 |

| Signal name | Pin | number | Signal name |
|-------------|-----|--------|-------------|
| PN7 | 50 | 49 | PN6 |
| VTG | 52 | 51 | GND |
| PP1 | 54 | 53 | PP0 |
| PP3 | 56 | 55 | PP2 |
| PP5 | 58 | 57 | PP4 |
| PP7 | 60 | 59 | PP6 |
| VTG | 62 | 61 | GND |
| PQ1 | 64 | 63 | PQ0 |
| PQ3 | 66 | 65 | PQ2 |
| PQ5 | 68 | 67 | PQ4 |
| PQ7 | 70 | 69 | PQ6 |
| VBUST | 72 | 71 | DP |
| UVCON | 74 | 73 | DN |
| Vcc | 76 | 75 | UID |
| Vext | 78 | 77 | GND |
| TGT_PDATA1 | 80 | 79 | TGT_PDATA0 |
| TGT_PDATA3 | 82 | 81 | TGT_PDATA2 |
| TGT_PDATA5 | 84 | 83 | TGT_PDATA4 |
| TGT_PDATA7 | 86 | 85 | TGT_PDATA6 |
| TGT_PCTRL1 | 88 | 87 | TGT_PCTRL0 |
| TGT_PCTRL3 | 90 | 89 | TGT_PCTRL2 |
| TGT_PCTRL5 | 92 | 91 | TGT_PCTRL4 |
| TGT_PCTRL7 | 94 | 93 | TGT_PCTRL6 |
| BOARD_ID1 | 96 | 95 | BOARD_ID0 |
| BOARD_ID3 | 98 | 97 | BOARD_ID2 |
| BOARD_ID5 | 100 | 99 | BOARD_ID4 |

2.3.1 Signal descriptions

 Table 2-4. Socket card connector pin description

| STK600 Signal name | MCU | Comment |
|--------------------|--------------|---|
| PAx, PBx etc | PAx, PBx etc | 1-to-1 mcu pin mapping |
| VTG | Vcc | Target supply rail controlled by AVR Studio [®] / STK600 |
| GND | GND | |
| AREFx | AREF | Analog reference voltage, controlled by AVR Studio / STK600 |
| XTALx | XTALx | Clock pins connected to oscillator on STK600. |





| STK600 Signal name | MCU | Comment |
|---------------------------------------|-----------------|--|
| TGT_SCK, TGT_MISO, TGT_MOSI | ISP pins | ISP programming interface |
| TGT_TDI, TGT_TDO, TGT_TMS, TGT_TCK | JTAG pins | JTAG programming interface |
| VBUST | VBUS | VBUS (sense) for USB |
| UID | UID | ID pin for USB OTG |
| UVCON | UVCON | USB VBUS generation control for USB OTG. A low level on this signal enables VBUS generation. |
| DP, DN | DP, DN | USB differential pair |
| TGT_PDATA(0-7) | (HV) data pins | Data pins for high voltage (PP/HVSP) programming. |
| TGT_CTRL0 | (HV) BS2 | |
| TGT_CTRL1 | (HV) Ready/Busy | Control signals for High voltage |
| TGT_CTRL2 | (HV) /OE | Parallell Programming / Serial |
| TGT_CTRL3 | (HV) /WR | Programming. Please refer to AVR datasheet for further |
| TGT_CTRL4 | (HV) BS1 | information. |
| TGT_CTRL5 | (HV) XA0 | On AVRs with common |
| TGT_CTRL6 | (HV) XA1 | XA1/BS2, XA1 is used. On AVRs with common |
| TGT_CTRL7 | (HV) PAGEL | BS1/PAGEL, BS1 is used. |
| BOARD_IDn | none | ID system for router / socket / expansion cards, see section 5 - ID System |

- Notes: 1. Not all AVR will have every pin (ex. two aref pins, tosc or usb)
 - 2. A MCU pin will fan-out to both Pnx pin and to the programming interface(s) located at that pin.

3 Socket cards

Socket cards route each pin from the IC socket to separate pins on the spring loaded connectors on the bottom side, facing the routing card.

3.1 Power design issues

Since all routing is handled by the routing card, even power lines and power decoupling is ignored at the socket card. This produces less than ideal power design which may lead to unwanted noise, ground bounce and other effects. It should therefore be expected that heavily loaded designs can not run at full speed on STK600. Likewise, such power design is not recommended for custom designs.

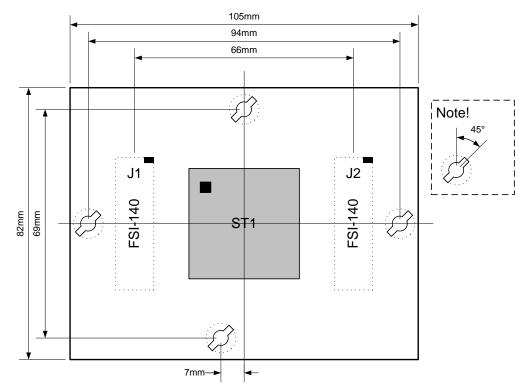
3.2 Connector MPN

Table 3-1. Socket card connector

| Manufacturer and MPN | Quantity | Comment |
|---------------------------|----------|--------------------------------|
| SAMTEC, FSI-140-03-G-D-AD | 2 | Spring loaded 80-pin connector |

3.3 Physical dimensions and component placement

Figure 3-1. Socket card connector placement and dimensions



The board thickness should be 1.6mm to be compatible with the clips.

4 Expansion cards

The STK600 features an expansion area where cards for custom peripherals like memory expansion, LCD etc can be placed. STK600 routes all part pins and power to the expansion card connectors.

4.1 Connector MPN

Table 4-1. Expansion card connector

| Manufacturer and MPN | Quantity | Comment |
|----------------------|----------|---------|
| FCI, 61082-101402LF | 2 | |





4.2 Physical dimensions and component placement

Pin 1 EXPANDO T□■Z 유 모 Ь (**III**)+ TERM Ц ✐ \$PLIT Ц SLOPECTRL RS232 1(000) Ц USB mini-AB EXPAND1 Pin 1 Max Width: 55mm

Figure 4-1. Expansion card connector placement and dimensions

There is no requirement to board thickness.

4.3 STK600 Expansion connectors pin out

(C).PJ[7.0] PA[7..0] (()) 8 10 12 14 16 18 20 24 26 33 32 34 36 38 34 46 48 50 52 54 46 66 66 66 66 68 88 88 90 92 94 98 98 VTGo -GND VTG₀ GND PK[7.0] <<>>) <<>> PK[7..0] 17 19 21 23 25 27 29 31 33 35 35 37 39 41 43 46 47 49 51 53 56 57 67 69 71 73 79 81 GND PC[7..0] <<>> VTG GND РЦ7..0] (🔷) VTG <>> РЦ7..0] VTG0 GND PD[7..0] <<>> PM[7..0] (\$> (0.7]MP< 34 36 38 40 42 44 46 48 50 52 54 56 68 70 72 74 76 78 80 82 84 86 88 90 92 94 96 PE[7..0] ((>) <>> PE7.01</> PN[7..0] (>> <<>>PN[7.0] VTG0 GND VTGo GND <>> PP[7..0] PP[7.0] (\$\infty VEGO GND GND PG[7..0] <<>> PQ[7.0] (\$\infty) <<>>PQ7..0J PH[7..0] <<>> VTG GND GND ⟨⟩TGT_PDATA[7.0] TGT_PDATA[7..0] << TGT_RESET VC08GNDVC08 61083-101402LF 61083-101402LF BOARD_ID[7.0] < >BOARD_ID[7..0]

Figure 4-2. Pinout for expansion connectors

Table 4-2. STK600 J301 "expand0" connector pin out

| Signal name | Pin number | | Signal name |
|-------------|------------|----|-------------|
| VTG | 2 | 1 | GND |
| PA1 | 4 | 3 | PA0 |
| PA3 | 6 | 5 | PA2 |
| PA5 | 8 | 7 | PA4 |
| PA7 | 10 | 9 | PA6 |
| VTG | 12 | 11 | GND |
| PB1 | 14 | 13 | PB0 |
| PB3 | 16 | 15 | PB2 |
| PB5 | 18 | 17 | PB4 |
| PB7 | 20 | 19 | PB6 |
| VTG | 22 | 21 | GND |
| PC1 | 24 | 23 | PC0 |
| PC3 | 26 | 25 | PC2 |
| PC5 | 28 | 27 | PC4 |
| PC7 | 30 | 29 | PC6 |
| VTG | 32 | 31 | GND |





| Signal name | Pin | number | Signal name |
|-------------|-----|--------|-------------|
| PD1 | 34 | 33 | PD0 |
| PD3 | 36 | 35 | PD2 |
| PD5 | 38 | 37 | PD4 |
| PD7 | 40 | 39 | PD6 |
| VTG | 42 | 41 | GND |
| PE1 | 44 | 43 | PE0 |
| PE3 | 46 | 45 | PE2 |
| PE5 | 48 | 47 | PE4 |
| PE7 | 50 | 49 | PE6 |
| VTG | 52 | 51 | GND |
| PF1 | 54 | 53 | PF0 |
| PF3 | 56 | 55 | PF2 |
| PF5 | 58 | 57 | PF4 |
| PF7 | 60 | 59 | PF6 |
| VTG | 62 | 61 | GND |
| PG1 | 64 | 63 | PG0 |
| PG3 | 66 | 65 | PG2 |
| PG5 | 68 | 67 | PG4 |
| PG7 | 70 | 69 | PG6 |
| VTG | 72 | 71 | GND |
| PH1 | 74 | 73 | PH0 |
| PH3 | 76 | 75 | PH2 |
| PH5 | 78 | 77 | PH4 |
| PH7 | 80 | 79 | PH6 |
| VTG | 82 | 81 | GND |
| AREF0 | 84 | 83 | XTAL1 |
| AREF1 | 86 | 85 | XTAL2 |
| TGT_MOSI | 88 | 87 | GND |
| TGT_MISO | 90 | 89 | TOSC1 |
| TGT_SCK | 92 | 91 | TOSC2 |
| TDI | 94 | 93 | TGT_RESET |
| TDO | 96 | 95 | Vcc6 |
| TMS | 98 | 97 | GND |
| TCK | 100 | 99 | Vcc6 |

Table 4-2. STK600 J302 "expand1" connector pinout

| Signal name | Pin ı | number | Signal name |
|-------------|-------|--------|-------------|
| VTG | 2 | 1 | GND |
| PJ1 | 4 | 3 | PJ0 |

AVR600

| Signal name | Pin ı | number | Signal name | | | |
|-------------|-------|--------|-------------|--|--|--|
| PJ3 | 6 | 5 | PJ2 | | | |
| PJ5 | 8 | 7 | PJ4 | | | |
| PJ7 | 10 | 9 | PJ6 | | | |
| VTG | 12 | 11 | GND | | | |
| PK1 | 14 | 13 | PK0 | | | |
| PK3 | 16 | 15 | PK2 | | | |
| PK5 | 18 | 17 | PK4 | | | |
| PK7 | 20 | 19 | PK6 | | | |
| VTG | 22 | 21 | GND | | | |
| PL1 | 24 | 23 | PL0 | | | |
| PL3 | 26 | 25 | PL2 | | | |
| PL5 | 28 | 27 | PL4 | | | |
| PL7 | 30 | 29 | PL6 | | | |
| VTG | 32 | 31 | GND | | | |
| PM1 | 34 | 33 | PM0 | | | |
| PM3 | 36 | 35 | PM2 | | | |
| PM5 | 38 | 37 | PM4 | | | |
| PM7 | 40 | 39 | PM6 | | | |
| VTG | 42 | 41 | GND | | | |
| PN1 | 44 | 43 | PN0 | | | |
| PN3 | 46 | 45 | PN2 | | | |
| PN5 | 48 | 47 | PN4 | | | |
| PN7 | 50 | 49 | PN6 | | | |
| VTG | 52 | 51 | GND | | | |
| PP1 | 54 | 53 | PP0 | | | |
| PP3 | 56 | 55 | PP2 | | | |
| PP5 | 58 | 57 | PP4 | | | |
| PP7 | 60 | 59 | PP6 | | | |
| VTG | 62 | 61 | GND | | | |
| PQ1 | 64 | 63 | PQ0 | | | |
| PQ3 | 66 | 65 | PQ2 | | | |
| PQ5 | 68 | 67 | PQ4 | | | |
| PQ7 | 70 | 69 | PQ6 | | | |
| Vext | 72 | 71 | GND | | | |
| Vext | 74 | 73 | GND | | | |
| GND | 76 | 75 | Vcc | | | |
| GND | 78 | 77 | Vcc | | | |
| TGT_PDATA1 | 80 | 79 | TGT_PDATA0 | | | |
| TGT_PDATA3 | 82 | 81 | TGT_PDATA2 | | | |





| Signal name | Pin | number | Signal name |
|-------------|-----|--------|-------------|
| TGT_PDATA5 | 84 | 83 | TGT_PDATA4 |
| TGT_PDATA7 | 86 | 85 | TGT_PDATA6 |
| TGT_PCTRL1 | 88 | 87 | TGT_PCTRL0 |
| TGT_PCTRL3 | 90 | 89 | TGT_PCTRL2 |
| TGT_PCTRL5 | 92 | 91 | TGT_PCTRL4 |
| TGT_PCTRL7 | 94 | 93 | TGT_PCTRL6 |
| Vcc3 | 96 | 95 | GND |
| BOARD_ID1 | 98 | 97 | BOARD_ID0 |
| BOARD_ID7 | 100 | 99 | BOARD_ID6 |

5 ID System

The STK600 features an id system to identify which routing, socket and expansion card is attached. The STK600 can impose voltage limitations based on the IDs, and AVR Studio will notify the user if the combination is incorrect.

The ID system consists of two common output and two board unique input signals. Each input is one of sixteen possible values based in the input signals – giving a total id space of 256.

Three IDs are reserved for custom use and can be implemented without use of ICs.

Table 5-1. IDs reserved for custom use

| Туре | ID | |
|------------------------|------|--|
| Board limited to 1.8 V | 0xCA | |
| Board limited to 3.3 V | 0xCC | |
| No limit on voltage | 0xCF | |

The id 0xff indicates no board present.

5.1 Signal usage

Table 5-2. ID system signal usage

| name | Direction | Function |
|-----------|------------|----------------------------|
| BOARD_ID0 | Output (A) | Common output to functions |
| BOARD_ID1 | Output (B) | Common output to functions |
| BOARD_ID2 | Input | Input from routing card |
| BOARD_ID3 | Input | Input from routing card |
| BOARD_ID4 | Input | Input from socket card |
| BOARD_ID5 | Input | Input from socket card |
| BOARD_ID6 | Input | Input from expansion card |
| BOARD_ID7 | Input | Input from expansion card |

5.2 ID functions

The functions and their output according to input A and B

| В | Α | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Functions as logic expressions

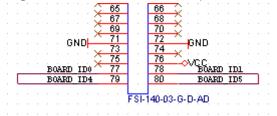
| Function | Expression | ID |
|----------|---------------------------------------|-----|
| 0 | 0 | 0x0 |
| 1 | $\overline{A+B}$ | 0x1 |
| 2 | $A\overline{B}$ | 0x2 |
| 3 | \overline{B} | 0x3 |
| 4 | $\overline{A}B$ | 0x4 |
| 5 | \overline{A} | 0x5 |
| 6 | $A \oplus B$ | 0x6 |
| 7 | \overline{AB} | 0x7 |
| 8 | AB | 0x8 |
| 9 | $\overline{A \oplus B}$ | 0x9 |
| 10 | A | 0xA |
| 11 | $\overline{B} + AB$ | 0xB |
| 12 | В | 0xC |
| 13 | $B + \overline{A} \cdot \overline{B}$ | 0xD |
| 14 | A + B | 0xE |
| 15 | 1 | 0xF |

5.3 Examples

For a socket card to report the ID 0xAC:

Route BOARD_ID0 to BOARD_ID4 and BOARD_ID1 to BOARD_ID5

Figure 5-1. Socket card id example



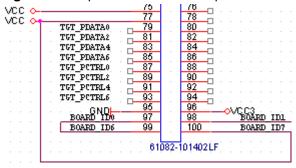




For an expansion card to report the ID 0xCF:

Route BOARD_ID0 to BOARD_ID6 and VCC to BOARD_ID7

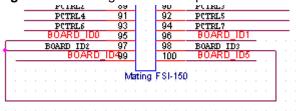
Figure 5-2. Expansion card id example



For a router card to report the ID 0xCC:

Route BOARD_ID0 to both BOARD_ID2 and BOARD_ID3.

Figure 5-3. Routing card id example



6 Design example

To support a new package type one would typically start with designing the socket card. The pinout between the socket card and routing card is not defined and left to the designer. An example is given in figure 6-1

Next is the design of the routing card (figure 6-3). The routing cards role is to connect each pin from the socket card to the corresponding pin on STK600. In addition to decoupling etc, the routing card should also fan-out the correct signals to programming headers.

Each card in the stack has its own board_id pins, the routing card is responsible for passing on the signal to the socket card.

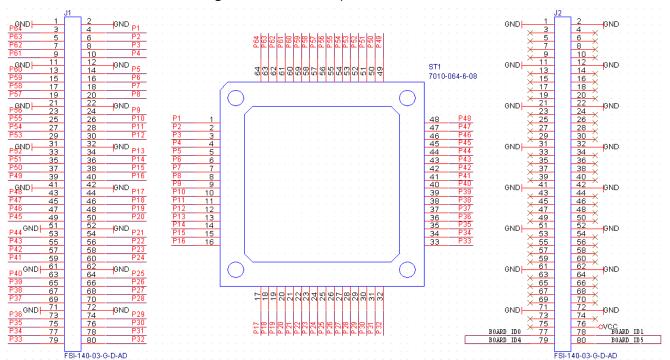


Figure 6-1. Schema capture of socket card

Both the socket and routing card must also include the clip holes:

PCB Clip Hole PCB Clip Hole

E4

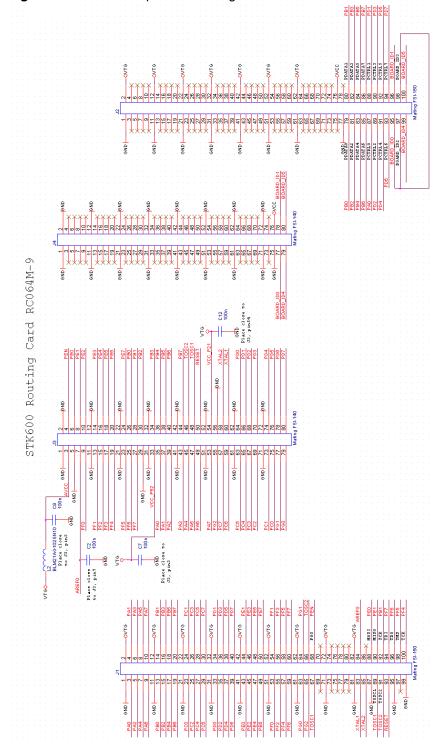
GND
PCB Clip Hole
GND
PCB Clip Hole
GND

Figure 6-2. Clip holes included in schematic.





Figure 6-3. Schema capture of routing card



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