



ATtiny1624/1626/1627

Product Brief

Introduction

The ATtiny1624/1626/1627 microcontrollers of the tinyAVR® 2 family are using the AVR® CPU with hardware multiplier, running at up to 20 MHz, with 16 KB Flash, 2 KB of SRAM, and 256B of EEPROM available in a 14-, 20-, and 24-pin package. The family uses the latest technologies from Microchip with a flexible and low-power architecture, including Event System and SleepWalking, advanced digital peripherals, and accurate analog features such as a 12-bit differential ADC with Programmable Gain Amplifier (PGA).

Features

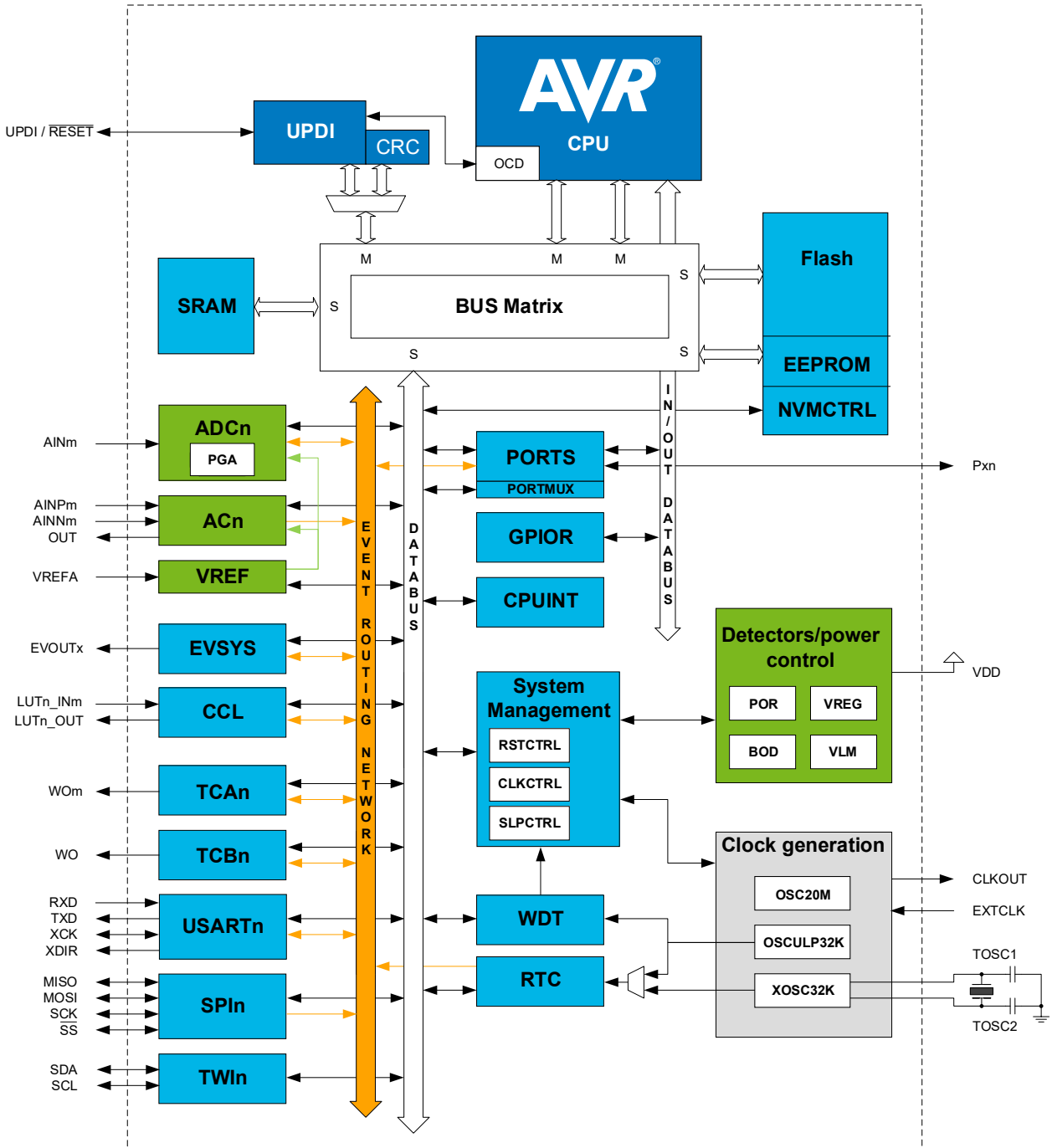
- High-Performance Low-Power AVR® CPU
 - Running at up to 20 MHz
 - Single-cycle I/O access
 - Two-level interrupt controller with vectored interrupts
 - Two-cycle hardware multiplier
 - Supply voltage range: 1.8V to 5.5V
- Memories
 - 16 KB In-System self-programmable Flash memory
 - 2 KB SRAM
 - 256B EEPROM
 - 32B of user row in nonvolatile memory that can keep data during chip-erase and be programmed while the device is locked
 - Write/erase endurance
 - Flash 10,000 cycles
 - EEPROM 100,000 cycles
 - Data retention: 40 years at 55°C
- System
 - Power-on Reset (POR)
 - Brown-out Detection (BOD)
 - Clock options
 - Lockable 20 MHz Low-Power internal oscillator
 - 32.768 kHz Ultra Low-Power (ULP) internal oscillator
 - 32.768 kHz external crystal oscillator
 - External clock input
 - Single-pin Unified Program and Debug Interface (UPDI)
 - Three sleep modes
 - Idle with all peripherals running and immediate wake-up time
 - Standby
 - Configurable operation of selected peripherals
 - SleepWalking peripherals
 - Power-Down with full data retention

- Peripherals
 - One 16-bit Timer/Counter type A (TCA) with a dedicated period register and three PWM channels
 - Two 16-bit Timer/Counter type B (TCB) with input capture and simple PWM functionality
 - One 16-bit Real-Time Counter (RTC) running from external 32.768 kHz crystal or internal 32.768 kHz ULP oscillator
 - Two Universal Synchronous Asynchronous Receiver Transmitter (USART) with fractional baud rate generator, auto-baud, and start-of-frame detection
 - Master/Slave Serial Peripheral Interface (SPI)
 - Master/Slave Two-Wire Interface (TWI) with dual address match
 - Standard mode (Sm, 100 kHz)
 - Fast mode (Fm, 400 kHz)
 - Fast mode plus (Fm+, 1 MHz)
 - Event System for CPU independent and predictable inter-peripheral signaling
 - Configurable Custom Logic (CCL) with four programmable Look-Up Tables (LUT)
 - One Analog Comparator (AC) with scalable reference input
 - One 12-bit differential 375 ksps Analog-to-Digital Converter (ADC) with Programmable Gain Amplifier (PGA) and up to 15 input channels
 - Multiple internal voltage references
 - 1.024V
 - 2.048V
 - 2.500V
 - 4.096V
 - VDD
 - Automated Cyclic Redundancy Check (CRC) flash memory scan
 - Watchdog Timer (WDT) with Window Mode, with a separate on-chip oscillator
 - External interrupt on all general purpose pins
- I/O and Packages
 - Up to 22 programmable I/O pins
 - 14-pin
 - SOIC150
 - TSSOP
 - 20-pin
 - SOIC300
 - SSOP
 - VQFN 3x3 mm
 - 24-pin
 - VQFN 4x4 mm
- Temperature Ranges
 - -40°C to 85°C (standard)
 - -40°C to 125°C (extended)
- Speed Grades (-40°C to 85°C)
 - 0-5 MHz @ 1.8V – 5.5V
 - 0-10 MHz @ 2.7V – 5.5V
 - 0-20 MHz @ 4.5V – 5.5V
- Speed Grades (-40°C to 125°C)
 - 0-8 MHz @ 2.7V - 5.5V
 - 0-16 MHz @ 4.5V - 5.5V

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1. Block Diagram



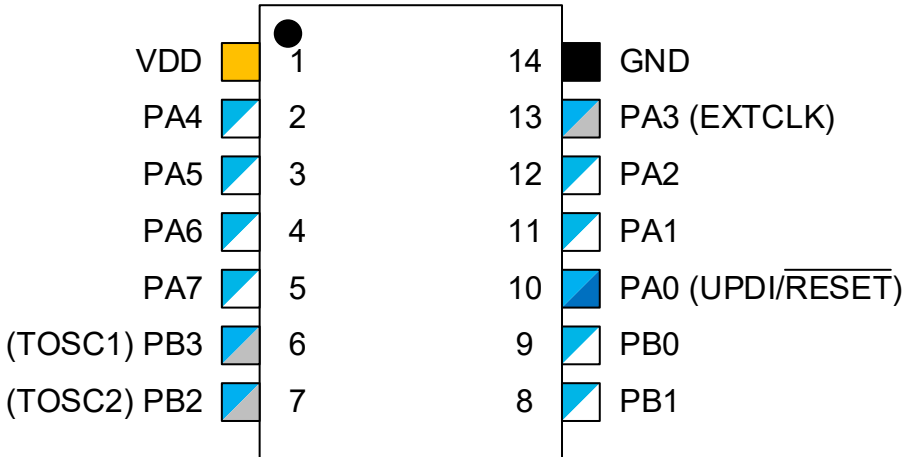
2. Peripheral Overview

Table 2-1. Peripheral Overview

Device	ATtiny1624	ATtiny1626	ATtiny1627
Pins	14	20	24
Package	SOIC	SOIC,VQFN	VQFN
Maximum frequency (MHz)	20	20	20
General purpose I/O	12	18	22
PORT	PA[7:0], PB[3:0]	PA[7:0], PB[5:0], PC[3:0]	PA[7:0], PB[7:0], PC[5:0]
External interrupts	12	18	22
Event system channels	6	6	6
CCL LUTs	4	4	4
Real-Time Counter (RTC)	1	1	1
16-bit Timer/Counter type A (TCA)	1	1	1
16-bit Timer/Counter type B (TCB)	2	2	2
12-bit Timer/Counter type D (TCD)	-	-	-
USART/SPI master	2	2	2
SPI	1	1	1
TWI (I ² C)	1	1	1
ADC (channels)	1 (9)	1 (15)	1 (15)
DAC	-	-	-
Analog Comparators (inputs)	1 (4p/3n)	1 (4p/3n)	1 (4p/3n)
Peripheral Touch Controller (PTC) (self cap/mutual cap channels)	-	-	-
Unified Program and Debug Interface (UPDI) activated by shared pin using high-voltage signal or fuse override	1	1	1

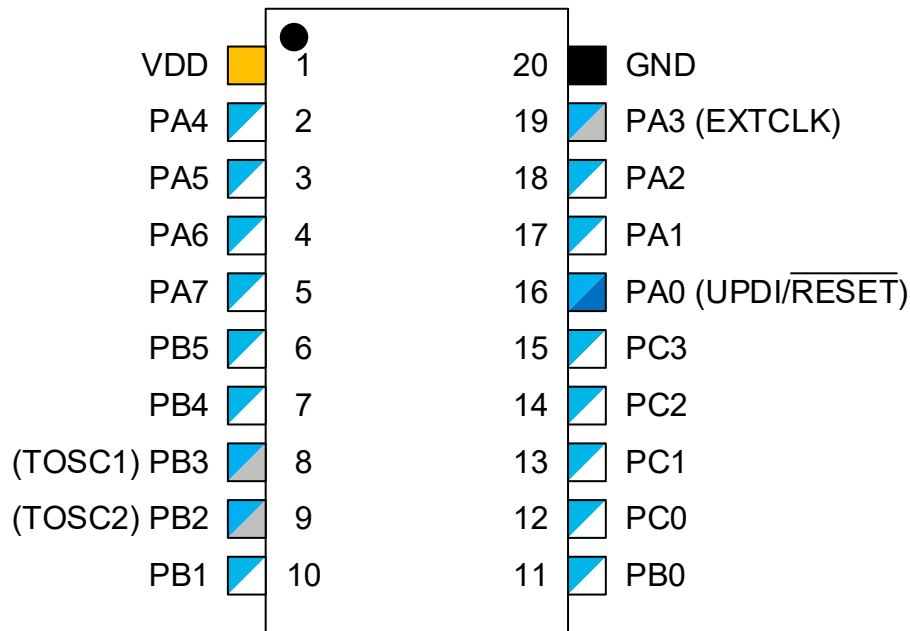
3. Pinout

3.1 14-Pin SOIC, TSSOP



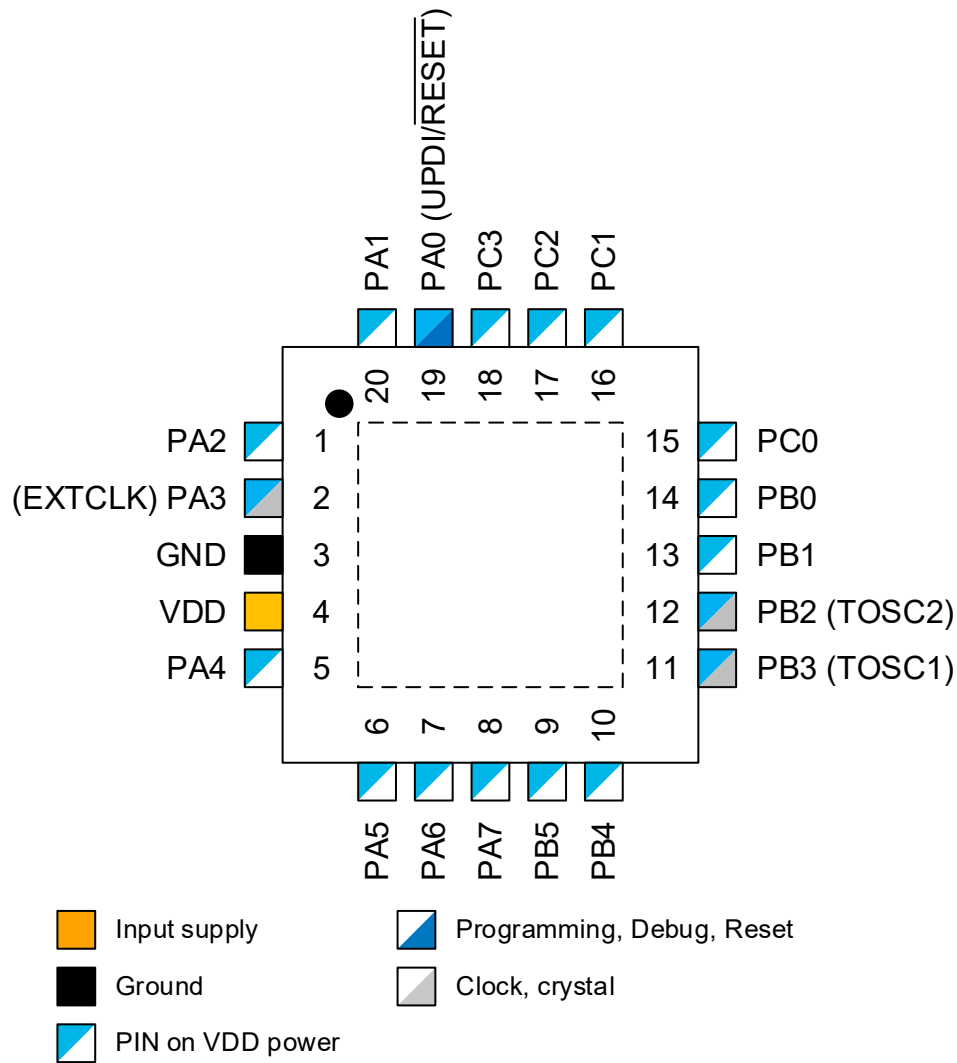
- Input supply
- Ground
- PIN on VDD power
- Programming, Debug, Reset
- Clock, crystal

3.2 20-Pin SOIC, SSOP

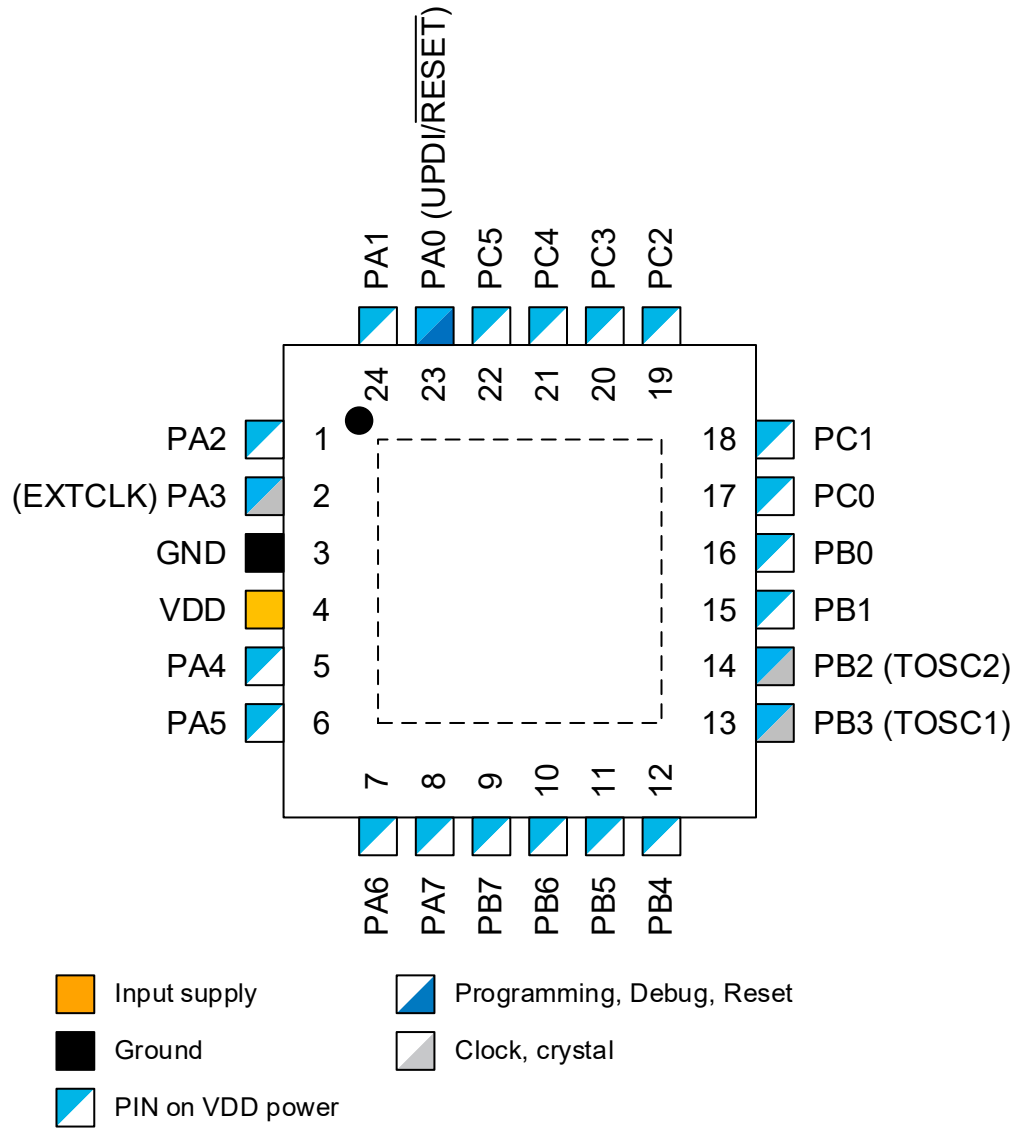


- Input supply
- Ground
- PIN on VDD power
- Programming, Debug, Reset
- Clock, crystal

3.3 20-Pin VQFN



3.4 24-Pin VQFN



4. I/O Multiplexing and Considerations

4.1 I/O Multiplexing

Table 4-1. PORT Function Multiplexing

VQFN 24-pin	VQFN 20-pin	SSOP/SOIC 20-pin	TSSOP/SOIC 14-pin	Pin Name (1,2)	Other/Special	ADC0 ⁽³⁾	AC0	USART0	USART1	SPI0	TWI0	TCA0	TCBn	CCL
23	19	16	10	PA0	RESET UPDI									LUT0-IN0
24	20	17	11	PA1		AIN1		TXD ⁽⁴⁾	TXD	MOSI				LUT0-IN1
1	1	18	12	PA2	EVOUTA	AIN2		RxD ⁽⁴⁾	RXD	MISO				LUT0-IN2
2	2	19	13	PA3	EXTCLK	AIN3		XCK ⁽⁴⁾	XCK	SCK		WO3	1,WO	
3	3	20	14	GND										
4	4	1	1	VDD										
5	5	2	2	PA4		AIN4		XDIR ⁽⁴⁾	XDIR	SS		WO4		LUT0-OUT
6	6	3	3	PA5	VREFA	AIN5	OUT					WO5	0,WO	LUT3-OUT ⁽⁴⁾
7	7	4	4	PA6		AIN6	AINN0							
8	8	5	5	PA7	EVOUTA ⁽⁴⁾	AIN7	AINP0							LUT1-OUT
9				PB7	EVOUTA ⁽⁴⁾									
10				PB6			AINP3							LUT2-OUT ⁽⁴⁾
11	9	6		PB5	CLKOUT	AIN8	AINP1					WO2 ⁽⁴⁾		
12	10	7		PB4	RESET ⁽⁴⁾	AIN9	AINN1					WO1 ⁽⁴⁾		LUT0-OUT
13	11	8	6	PB3	TOSC1			RxD				WO0 ⁽⁴⁾		LUT2-OUT
14	12	9	7	PB2	TOSC2 EVOUTA			TxD				WO2		LUT2-IN2
15	13	10	8	PB1		AIN10	AINP2	XCK			SDA	WO1		LUT2-IN1
16	14	11	9	PB0		AIN11	AINN2	XDIR			SCL	WO0		LUT2-IN0
17	15	12		PC0		AIN12			XCK ⁽⁴⁾	SCK ⁽⁴⁾			0,WO ⁽⁴⁾	LUT3-IN0
18	16	13		PC1		AIN13			RxD ⁽⁴⁾	MISO ⁽⁴⁾				LUT1-OUT ⁽⁴⁾ LUT3-IN1
19	17	14		PC2	EVOUTC	AIN14			TxD ⁽⁴⁾	MOSI ⁽⁴⁾				LUT3-IN2
20	18	15		PC3		AIN15			XDIR ⁽⁴⁾	SS ⁽⁴⁾		WO3 ⁽⁴⁾		LUT1-IN0
21				PC4								WO4 ⁽⁴⁾	1,WO ⁽⁴⁾	LUT1-IN1 LUT3-OUT
22				PC5								WO5 ⁽⁴⁾		LUT1-IN2

Note:

1. Pin names are of type Pxn, with x being the PORT instance (A, B) and n the pin number. Notation for signals is PORTx_PINn.
2. All pins can be used for external interrupt, where pins Px2 and Px6 of each port have full asynchronous detection. All pins can be used as event input.
3. AIN[15:8] can not be used as negative ADC input for differential measurements.
4. Alternative pin location. For selecting alternative pin location refer to PORTMUX section.

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