

## Two Output PCIe Gen1/2/3/4 Clock Generator

### Features

- Complies with PCIe Gen1/2/3/4 Common Clock Spec
- Integrated MEMS Resonator Eliminates the Need for External 25 MHz Crystal
- 100 MHz HCSL/LVDS/LVCMOS Options Available
- Wide Temperature Range:
  - Ext. Industrial: -40°C to +105°C
  - Industrial: -40°C to +85°C
  - Commercial: -20°C to +70°C
- Supply Range of 2.25V to 3.6V
- Low Power Consumption
  - 30% Lower than Competing Devices
- Excellent Shock & Vibration Immunity
  - Qualified to MIL-STD-883
- Space Saving 14-Lead QFN Package
- Lead-Free and RoHS-Compliant

### Applications

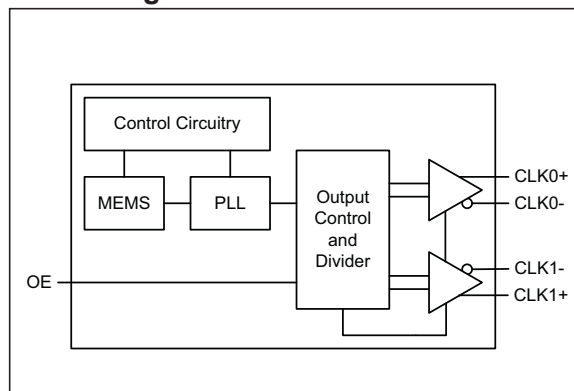
- Communications/Networking
  - Ethernet
  - 1G, 10GBASE-T/KR/LR/SR, and FcoE
  - Routers and Switches
  - Gateways, VoIP, Wireless AP's
  - Passive Optical Networks
- Storage
  - SAN, NAS, SSD, JBOD
- Embedded Applications
  - Industrial, Medical, and Avionics
  - Security Systems and Office Automation
  - Digital Signage, POS and others
- Consumer Electronics
  - Smart TV, Bluray, STB

### General Description

The DSC557-03 is a two output PCI express clock generator meeting Gen1, Gen2, Gen3 and Gen 4 specifications. The clock generator uses proven silicon MEMS technology to provide 100 MHz\* differential output clocks with excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the external quartz crystal, the DSC557-03 significantly enhances reliability and accelerates product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

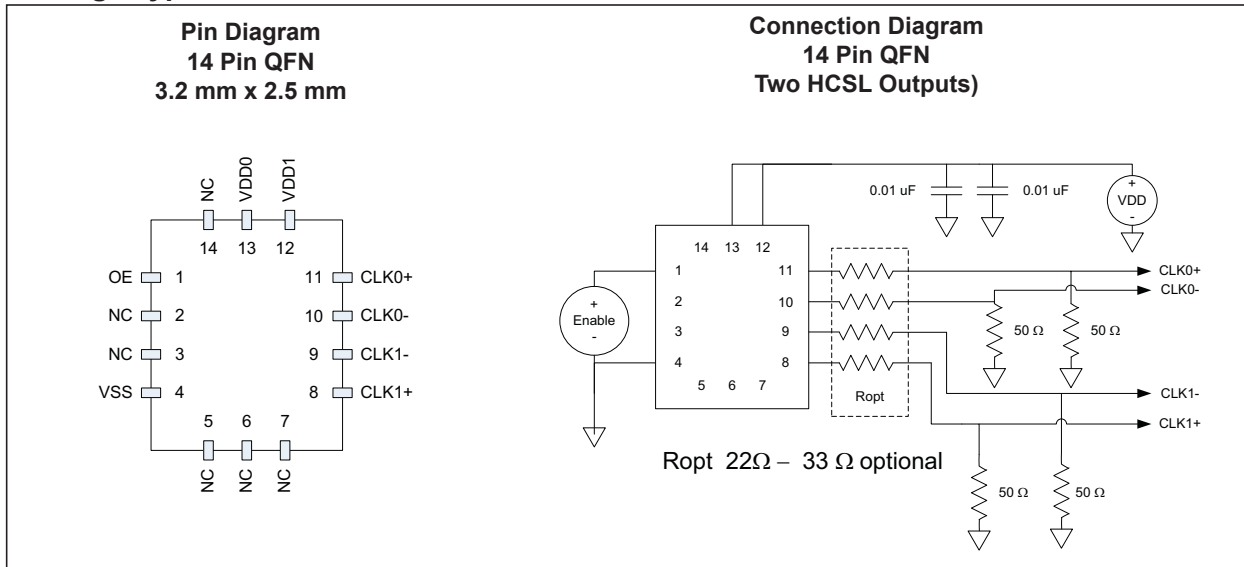
DSC557-03 has an Output Enable / Disable feature allowing it to disable the outputs when OE is low. The device is available in a space saving 14 pin QFN. Additional output formats are also available in any combination of LVCMOS, LVDS, and HCSL.

### Block Diagram



# DSC557-03

## Package Type



**TABLE 0-1: PIN DESCRIPTION (14 QFN)**

Pin Number	Pin Name	Pin Type	Description
1	OE	I	Output Enable; Active-high.
2	NC	N/A	Ground recommended or leave as a NC.
3	NC	N/A	Ground recommended or leave as a NC.
4	VSS	Power	Ground.
5	NC	N/A	Ground recommended or leave as a NC.
6	NC	N/A	Ground recommended or leave as a NC.
7	NC	N/A	Ground recommended or leave as a NC.
8	CLK1+	O	True output of differential pair.
9	CLK1-	O	Complement output of differential pair.
10	CLK0-	O	Complement output of differential pair.
11	CLK0+	O	True output of differential pair.
12	VDD1	Power	Power Supply for Output 1 (CLK1+/-).
13	VDD0	Power	Power Supply for Core and Output 0 (CLK0+/-).
14	NC	N/A	Ground recommended or leave as a NC.
ePAD	ePAD	N/A	Thermal pad, floating, not DC connected to substrate ground.

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage .....	-0.3V to +4.0V
Input Voltage .....	-0.3V to $V_{DD} + 0.3V$
ESD Protection (HBM) .....	.4 kV
ESD Protection (MM) .....	400V
ESD Protection (CDM) .....	1.5 kV

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:**  $V_{DD} = 3.3V$ ;  $T = 25^{\circ}C$ , unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	$V_{DD}$	2.25	—	3.6	V	Note 1
Supply Current	$I_{DD}$	—	—	—	—	EN pin low - outputs are disabled
Supply Current (Two HCSL Outputs), Note 2	$I_{DD}$	—	60	—	mA	EN pin high - outputs are enabled $R_L = 50\Omega$ , $F_{O1} = F_{O2} = 100$ MHz
Frequency Stability	$\Delta f$	—	—	$\pm 100$	ppm	Includes frequency variations due to initial tolerance, temp. and power supply voltage
		—	—	$\pm 50$		
Startup Time	$t_{SU}$	—	—	5	ms	Note 3
Input Logic Levels,	$V_{IH}$	$0.7 \times V_{DD}$	—	—	V	Input logic high
	$V_{IL}$	—	—	$0.3 \times V_{DD}$		Input logic low
Output Disable Time	$t_{DA}$	—	—	5	ns	Note 4
Output Enable Time	$t_{EN}$	—	—	20	ns	—
Pull-Up Resistor	—	—	40	—	k $\Omega$	Pull-up on OE pin
<b>HCSL Outputs</b>						
Output Logic Levels						
Output Logic High	$V_{OH}$	0.725	—	—	V	$R_L = 50\Omega$
Output Logic Low	$V_{OL}$	—	—	0.1	V	
Peak to Peak Output Swing	—	—	750	—	mV	Single-ended
Output Transition Time						
Rise Time	$t_R$	200	—	400	ps	20% to 80%, $R_L = 50\Omega$ , $C_L = 2$ pF
Fall Time	$t_F$	200	—	400		
Frequency	$f_0$	—	100	—	MHz	Single frequency
Output Duty Cycle	SYM	48	—	52	%	Differential
Period Jitter Note 5	$J_{PER}$	—	2.5	—	pSRMS	$F_{O1} = F_{O2} = 100$ MHz

# DSC557-03

## ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics:  $V_{DD} = 3.3V$ ;  $T = 25^{\circ}C$ , unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Jitter, Phase (Common Clock Architecture) Note 6	$T_J$	—	17	86	$ps_{PP}$	PCIe Gen 1.1 $T_J = D_J + 14.069 \times R_J$ (BER $10^{-12}$ )
	$J_{RMS-CCHF}$	—	1.46	3.1	$ps_{RMS}$	PCIe Gen 2.1, 1.5 MHz to Nyquist
	$J_{RMS-CCLF}$	—	0.08	3.0	$ps_{RMS}$	PCIe Gen 2.1, 10 kHz to 1.5 MHz
	$J_{RMS-CC}$	—	0.313	1.0	$ps_{RMS}$	PCIe Gen 3.0
—		0.313	0.5	$ps_{RMS}$	PCIe Gen 4.0	
Integrated Phase Noise (Data Clock Architecture) Note 6	$J_{RMS-DCHF}$	—	2.15	—	$ps_{RMS}$	PCIe Gen 2.1, 1.5 MHz to Nyquist
	$J_{RMS-CCLF}$	—	0.06	—	$ps_{RMS}$	PCIe Gen 2.1, 10 kHz to 1.5 MHz
	$J_{RMS-DC}$	—	0.32	—	$ps_{RMS}$	PCIe Gen 3.0
<b>LVDS Output</b>						
Offset Voltage	$V_{OS}$	1.125	1.25	1.40	V	$V_{DD} = 2.5V/3.3V$
$V_{OS}$ Magnitude Change	$\Delta V_{OS}$	—	—	50	mV	—
Output High Voltage	$V_{OH}$	$0.9 \times V_{DD}$	—	—	V	—
Output Low Voltage	$V_{OL}$	—	—	$0.1 \times V_{DD}$	V	—
Output Frequency	$f_{OUT}$	—	100	—	MHz	—
Differential Output Voltage	$V_{OD}$	275	350	475	$mV_{PP}$	—
$V_{OD}$ Magnitude Change	$\Delta V_{OD}$	—	—	40	mV	—
LVDS Output Rise/Fall Time	$t_r/t_f$	—	200	—	ps	20% – 80%
Output Duty Cycle	ODC	48	50	52	%	20% – 80%, $R_L = 50\Omega$ , $C_L = 2$ pF
Period Jitter, Peak to Peak	$J_{PTP}$	—	2.5	—	ps	$f_{OUT} = 100$ MHz, Standard Drive
Integrated Phase Noise	$J_{PH}$	—	0.28	—	$ps_{RMS}$	200 kHz to 20 MHz @ 100 MHz, $T_A = +105^{\circ}C$
		—	0.4	—		100 kHz to 80 MHz @ 100 MHz
		—	1.7	2.0		12 kHz to 10 MHz @ 100 MHz
<b>LVC MOS Output</b>						
Output High Voltage	$V_{OH}$	$0.8 \times V_{DD}$	—	—	V	$\pm 10$ mA drive current
Output Low Voltage	$V_{OL}$	—	—	$0.2 \times V_{DD}$	V	$\pm 10$ mA drive current
Output Frequency	$f_{OUT}$	—	100	—	MHz	—
Output Rise/Fall Time	$t_r/t_f$	—	1.2	—	ns	20% – 80%, $C_L = 15$ pF
Output Duty Cycle	ODC	48	50	52	%	$f_{OUT} = 100$ MHz, Standard Drive
Period Jitter	$J_{PTP}$	—	3	—	$ps_{RMS}$	$f_{OUT} = 100$ MHz, Standard Drive
Integrated Phase Noise	$J_{PH}$	—	0.3	—	$ps_{RMS}$	200 kHz to 20 MHz @ 100 MHz
		—	0.38	—		100 kHz to 20 MHz @ 100 MHz
		—	1.7	2.0		12 kHz to 20 MHz @ 100 MHz

- Note 1:**  $V_{DD}$  pin should be filtered with a 0.1  $\mu F$  capacitor.  
**Note 2:** Output is enabled if OE pin is floated or not connected.  
**Note 3:**  $t_{su}$  is time to 100 PPM stable output frequency after  $V_{DD}$  is applied and outputs are enabled.  
**Note 4:** Output Waveform and Connection Diagram define the parameters.  
**Note 5:** Period Jitter includes crosstalk from adjacent output.  
**Note 6:** Jitter limits established by Gen 1.1, Gen 2.1, Gen 3.0 and Gen 4.0 PCIe standards.

## TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Junction Operating Temperature	$T_J$	—	—	+150	°C	—
Storage Temperature Range	$T_S$	-55	—	+150	°C	—
Lead Temperature	—	—	+260	—	°C	Soldering, 40s

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e.,  $T_A$ ,  $T_J$ ,  $\theta_{JA}$ ). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

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## 2.0 OE FUNCTION AND OUTPUT WAVEFORM: HCSSL

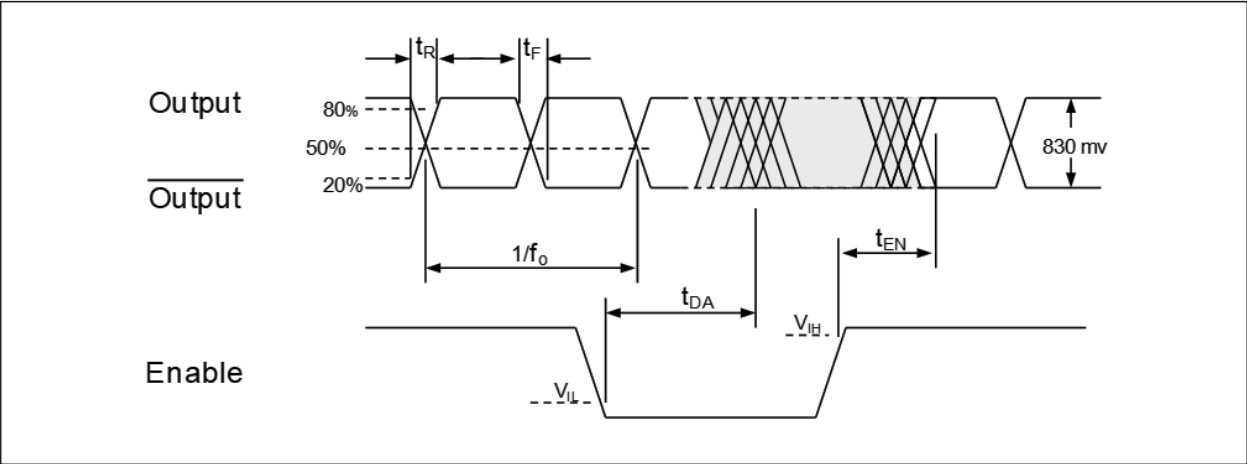


FIGURE 2-1: OE Function and Output Waveform.

3.0 SOLDER REFLOW PROFILE

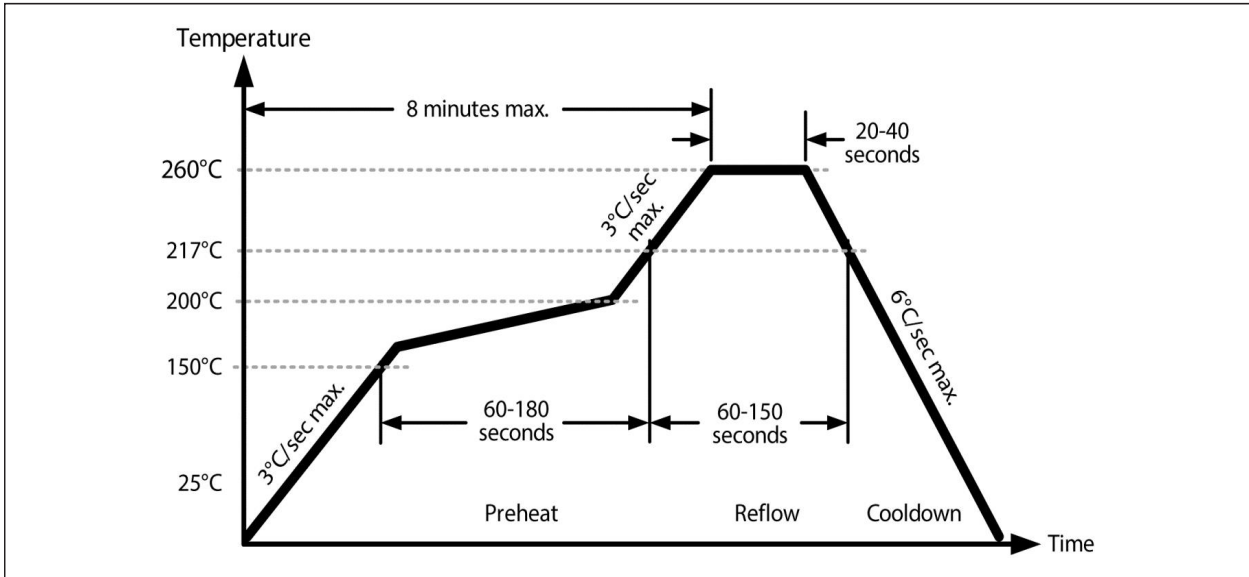


FIGURE 3-1: Solder Reflow Profile.

TABLE 3-1: SOLDER REFLOW

14 QFN MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp.)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time Maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20 to 40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

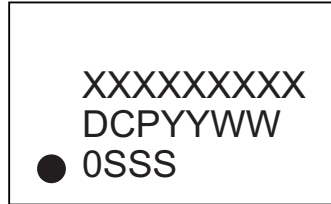
# DSC557-03

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## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

14-Lead QFN\*  
(2.5 mm x 3.2 mm)



Example



<b>Legend:</b>	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar ( ) and/or Overbar ( ) symbol may not be to scale.	

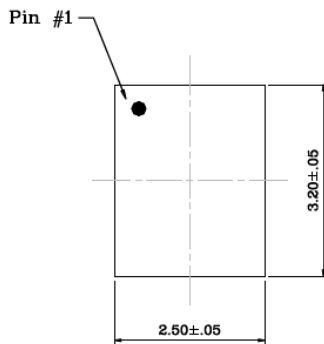


## 14-Lead QFN Package Outline and Recommended Land Pattern

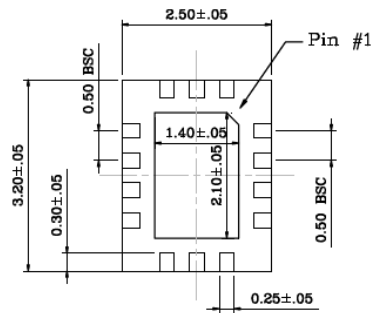
**TITLE**

14 LEAD QFN 2.5x3.2mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

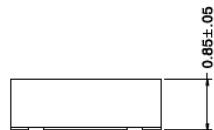
<b>DRAWING #</b>	QFN2532-14LD-PL-1	<b>UNIT</b>	MM
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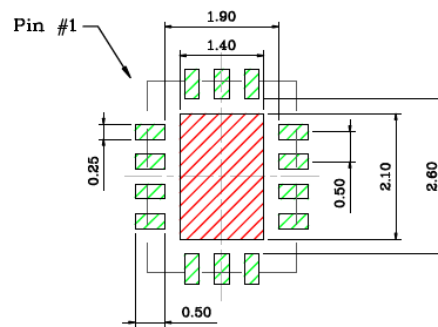
Top View



Bottom View



Side View



Recommended Land Pattern

**NOTE:**

1. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
2. Red shaded rectangle in Recommended Land Pattern is keep out area.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

# DSC557-03

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision A (June 2020)

- Conversion of Discera Data Sheet DSC557-03 as Microchip data sheet DS20006318A.
- Added LVDS section to the **Section 1.0 “Electrical Characteristics”** table.
- Added LVCMOS section to the **Section 1.0 “Electrical Characteristics”** table.

# DSC557-03

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	X	X	X	X	X	X
Device	CLK1 Output Format	CLK0 Output Format	Package	Temperature	Frequency Stability	Media Type
<b>Device:</b>	DSC557-03: Two Output PCIe Gen1/2/3/4 Clock Generator					
<b>CLK1 Output Format</b>	1 = LVCMOS					
	3 = LVDS					
	4 = HCSL					
<b>CLK0 Output Format</b>	1 = LVCMOS					
	3 = LVDS					
	4 = HCSL					
<b>Package:</b>	F = 14-Lead 2.5 mm x 3.2 mm QFN					
<b>Temperature:</b>	E = -20°C to +70°C (Commercial)					
	I = -40°C to +85°C (Industrial)					
	L = -40°C to +105°C (Extended Industrial)					
<b>Frequency Stability:</b>	0 = ±100 ppm					
	1 = ±50 ppm					
<b>Media Type:</b>	<blank> = 110/Tube					
	T = 1,000/Reel					
<b>Examples:</b>						
a) DSC557-0313FL0: CLK1 Output LVCMOS, CLK0 Output LVDS, 14-Lead QFN, -40°C to +105°C, ±100 ppm, 110/Tube						
b) DSC557-0344FI0: CLK1 Output HCSL, CLK0 Output HCSL, 14-Lead QFN, -40°C to +85°C, ±100 ppm, 110/Tube						
d) DSC557-0343F: CLK1 Output HCSL, CLK0 Output LVDS, 14-Lead QFN, -20°C to +70°C, ±50 ppm, 1,000Tape/Reel						
e) DSC557-0343FL1T: CLK1 Output HCSL, CLK0 Output LVDS, 14-Lead QFN, 40°C to +105°C, ±50 ppm, 1,000Tape/Reel						
<b>Note 1:</b> Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.						

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NOTES:

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