

# DSC60XX

# **Ultra-Small, Ultra-Low Power MEMS Oscillator**

#### **Features**

- Wide Frequency Range: 2 kHz to 80 MHz
- Ultra-Low Power Consumption: 1.3 mA/12 μA (Active/Standby)
- · Ultra-Small Footprints
  - $1.6 \text{ mm} \times 1.2 \text{ mm}$
  - $2.0 \text{ mm} \times 1.6 \text{ mm}$
  - $2.5 \text{ mm} \times 2.0 \text{ mm}$
  - $-3.2 \text{ mm} \times 2.5 \text{ mm}$
- Frequency Select Input Supports Two Pre-Defined Frequencies
- · High Stability: ±25 ppm, ±50 ppm
- · Wide Temperature Range
  - Industrial: -40°C to 85°C
  - Ext. Commercial: -20° to 70°C
- · Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- · High Reliability
  - 20x Better MTF Than Quartz Oscillators
- Supply Range of 1.71V to 3.63V
- · Short Sample Lead Time: <2 weeks
- · Lead Free & RoHS Compliant

#### **Applications**

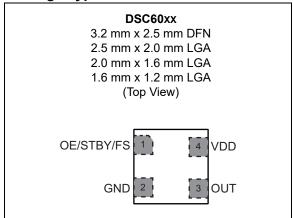
- Low Power/Portable Applications: IoT, Embedded/Smart Devices
- Consumer: Home Healthcare, Fitness Devices, Home Automation
- Automotive: Rear View/Surround View Cameras, Infotainment System
- Industrial: Building/Factory Automation, Surveillance Camera

#### **General Description**

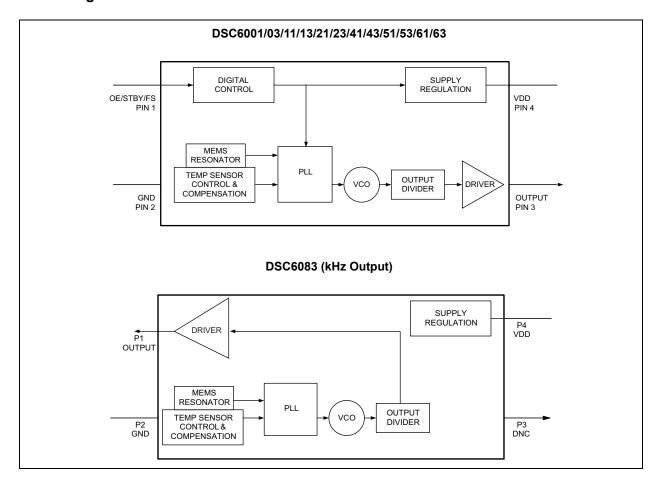
The DSC60xx family of MEMS oscillators combines industry-leading low-power consumption, ultra-small packages with exceptional frequency stability, and jitter performance over temperature. The single-output DSC60xx MEMS oscillators are excellent choices for use as clock references in small, battery-powered devices such as wearable and Internet of Things (IoT) devices in which small size, low power consumption, and long-term reliability are paramount. They also meet the stringent mechanical durability and reliability requirements within Automotive Electronics Council standard Q100 (AEC-Q100), so they are well suited for under-hood applications as well.

The DSC60xx family is available in ultra-small  $1.6~\text{mm} \times 1.2~\text{mm}$  and  $2.0~\text{mm} \times 1.6~\text{mm}$  packages. Other package sizes include:  $2.5~\text{mm} \times 2.0~\text{mm}$  and  $3.2~\text{mm} \times 2.5~\text{mm}$ . These packages are "drop-in" replacements for standard 4-pin CMOS quartz crystal oscillators.

#### **Package Types**



# **Block Diagrams**



#### 1.0 ELECTRICAL CHARACTERISTICS

#### **Absolute Maximum Ratings**

Supply Voltage	
Input Voltage (V <sub>IN</sub> )	
ESD Protection	

#### **ELECTRICAL CHARACTERISTICS**

<b>Electrical Characteristics:</b> Unless otherwise indicated, $V_{DD} = 1.8V - 5\%$ to 3.3V +10%, $T_A = -40$ °C to 85°C.								
Parameters	Symbol	Min.	Тур.	Max.	Units	Conditions		
Supply Voltage Note 1	$V_{DD}$	1.71		3.63	V	_		
		_	1.3			F <sub>OUT</sub> = 24 MHz, V <sub>DD</sub> = 1.8V, No Load		
Active Supply Current	I <sub>DD</sub>	_	1.19		mA	$F_{OUT}$ = 32.768 kHz (DSC6083), $V_{DD}$ = 1.8V, No Load		
Power Supply Ramp	t <sub>PU</sub>	0.1	1	100	ms	Note 9		
Standby Supply Current	I <sub>STBY</sub>	_	12			V <sub>DD</sub> = 1.8/2.5V		
Note 2	SIBY	_	80		μA	V <sub>DD</sub> = 3.3V		
Frequency Stability Note 3	Δf	_	1	±25 ±50	ppm	All temp ranges		
Aging	Δf	_	1	±5	ppm	1st year @25°C		
Aging		_	1	±1		Per year after first year		
Startup Time	t <sub>SU</sub>	_	_	1.3	ms	From 90% V <sub>DD</sub> to valid clock output, T = 25°C		
Input Logic Lovele Note 4	$V_{IH}$	0.7 x V <sub>DD</sub>		_	٧	Input Logic High		
Input Logic Levels Note 4	$V_{IL}$	_	1	0.3 x V <sub>DD</sub>	٧	Input Logic Low		
Output Disable Time Note 5	t <sub>DA</sub>	_	l	200+Period	μs	_		
Output Enable Time Note 6	t <sub>EN</sub>		_	1	μs	_		
Enable Pull-Up Resistor Note 7		_	300	_	kΩ	If configured		
Output Logic Levels,	V <sub>OH</sub>	0.8 x V <sub>DD</sub>		_	V	Output Logic High, I = 1 mA		
Low Drive	$V_{OL}$	_	_	0.2 x V <sub>DD</sub>	V	Output Logic Low, I = -1 mA		

- **Note 1:** Pin 4  $V_{DD}$  should be filtered with 0.1  $\mu F$  capacitor.
  - 2: Not including current through pull-up resistor on EN pin (if configured). Higher standby current seen at >3.3V V<sub>DD</sub>.
  - 3: Includes frequency variations due to initial tolerance, temp. and power supply voltage.
  - 4: Input waveform must be monotonic with rise/fall time < 10 ms
  - **5:** Output Disable time takes up to one period of the output waveform + 200 ns.
  - 6: For parts configured with OE, not Standby.
  - 7: Output is enabled if pad is floated or not connected.
  - 8: Output Duty Cycle will be 40% to 60% when output frequency is between 40 MHz to 60 MHz.
  - 9: Time to reach 90% of target  $V_{\mbox{\scriptsize DD}}.$  Power ramp rise must be monotonic.

# DSC60XX

# **ELECTRICAL CHARACTERISTICS (CONTINUED)**

<b>Electrical Characteristics:</b> Unless otherwise indicated, $V_{DD} = 1.8V - 5\%$ to $3.3V + 10\%$ , $T_A = -40$ °C to $85$ °C.									
Parameters	Symbol	Min.	Тур.	Max.	Units	Conditions	Conditions		
		_	2.5	3.5		DSC60x3 Low Drive, 20% to 80% $C_L = 5 pF$	V <sub>DD</sub> = 1.8V		
Output Transition Time	t <sub>RX</sub> /t <sub>FX</sub>	_	1.5	2.2	ns		V <sub>DD</sub> = 2.5V/3.3V		
Rise Time/Fall Time	. /.	_	1.2	2.0		DSC60x1 Std. Drive,	V <sub>DD</sub> = 1.8V		
	t <sub>RY</sub> /t <sub>FY</sub>	_	0.6	1.2	ns	20% to 80% C <sub>L</sub> = 10 pF	V <sub>DD</sub> = 2.5V/3.3V		
Frequency	$f_0$	0.002	_	80	MHz	Output on Pin	1 for < 1 MHz		
Output Duty Cycle, Note 8	SYM	45	_	55	%	_			
	J <sub>PER</sub>	_	32	40		DSC60x3 Low Drive,	V <sub>DD</sub> = 1.8V		
Period Jitter, RMS		_	25	32		F <sub>OUT</sub> = 27 MHz	V <sub>DD</sub> = 2.5V/3.3V		
Period Jiller, Rivio		_	23	30	ps <sub>RMS</sub>	DSC60x1 Std. Drive, F <sub>OUT</sub> = 27 MHz	V <sub>DD</sub> = 1.8V		
		_	20	28			V <sub>DD</sub> = 2.5V/3.3V		
		_	180	240		DSC60x3 Low Drive, F <sub>OUT</sub> = 27 MHz	V <sub>DD</sub> = 1.8V		
Cycle-to-Cycle Jitter (peak)	1	_	120	170			V <sub>DD</sub> = 2.5V/3.3V		
	J <sub>Cy</sub> -cy	_	115	190	ps ps	DSC60x1, Std. Drive,	V <sub>DD</sub> = 1.8V		
		_	90	150		F <sub>OUT</sub> = 27 MHz	V <sub>DD</sub> = 2.5V/3.3V		

- **Note 1:** Pin 4  $V_{DD}$  should be filtered with 0.1  $\mu$ F capacitor.
  - 2: Not including current through pull-up resistor on EN pin (if configured). Higher standby current seen at >3.3V V<sub>DD</sub>.
  - 3: Includes frequency variations due to initial tolerance, temp. and power supply voltage.
  - 4: Input waveform must be monotonic with rise/fall time < 10 ms
  - 5: Output Disable time takes up to one period of the output waveform + 200 ns.
  - **6:** For parts configured with OE, not Standby.
  - 7: Output is enabled if pad is floated or not connected.
  - 8: Output Duty Cycle will be 40% to 60% when output frequency is between 40 MHz to 60 MHz.
  - **9:** Time to reach 90% of target V<sub>DD</sub>. Power ramp rise must be monotonic.

# **TEMPERATURE SPECIFICATIONS (Note 1)**

Parameters	Sym.	Min.	Тур.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature	TJ	_	_	+150	°C	_
Ambient Operating Temperature	T <sub>A</sub>	-40	_	+85	°C	Industrial
Ambient Operating Temperature	T <sub>A</sub>	-20	_	+70	°C	Extended Commercial
Storage Ambient Temperature Range	T <sub>A</sub>	-55	_	+150	°C	_
Soldering Temperature	T <sub>S</sub>	_	+260	_	°C	40 sec. max.

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T<sub>A</sub>, T<sub>J</sub>, θ<sub>JA</sub>). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

#### 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1 and Table 2-2.

TABLE 2-1: DSC6001/03/11/13/21/23/41/43/51/53/61/63 PIN FUNCTION TABLE (OUTPUT ≥1 MHZ)

Pin Number	Pin Name	Pin Type	Description
	OE		Output Enable: H = Specified Frequency Output, Note 1 L = Output is high impedance
1	STBY	I	Standby: H = Specified Frequency Output, Note 1 L = Output is high impedance, Device is in low power mode, Supply current is at I <sub>STBY</sub>
	FS		Frequency Select: H = Output Frequency 1, Note 2 L = Output Frequency 2
2	GND	Power	Power supply ground
3	Output	0	Oscillator clock output
4	VDD	Power	Power supply, Note 3

- Note 1: DSC600x/1x/2x has 300 kΩ internal pull-up resistor on pin1. DSC604x/5x/6x has no internal pull-up resistor on pin1 and needs an external pull-up or to be driven by another chip.
  - 2: Two pre-programmed frequencies can be configured at http://clockworks.microchip.com/timing/.
  - 3: Bypass with 0.1  $\mu$ F capacitor placed as close to the  $V_{DD}$  pin as possible.

TABLE 2-2: DSC6083 PIN FUNCTION TABLE (OUTPUT FREQUENCY <1 MHZ)

Pin Number	Pin Name	Pin Type	Description
1	Output	0	Oscillator clock output
2	GND	Power	Power supply ground
3	DNC	DNC	Do Not Connect
4	VDD	Power	Power supply, Note 1

**Note 1:** Bypass with 0.1 μF capacitor placed as close to V<sub>DD</sub> pin as possible.

#### 2.1 Output Buffer Options

The DSC60xx family is available in multiple output driver configurations.

The low-drive DSC60x3 is configured with a low-power driver that minimizes current consumption and EMI while delivering greater than 1 mA output current at 20%/80% of the supply voltage. The standard-drive DSC60x1 delivers greater than 3 mA output current at 20%/80% of the supply voltage.

# 3.0 DIAGRAMS

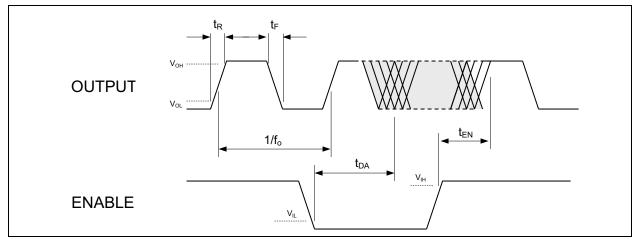


FIGURE 3-1: Output Waveform.

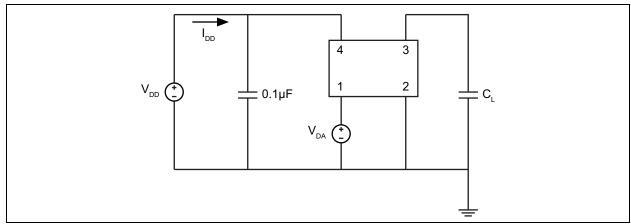


FIGURE 3-2: Test Circuit.

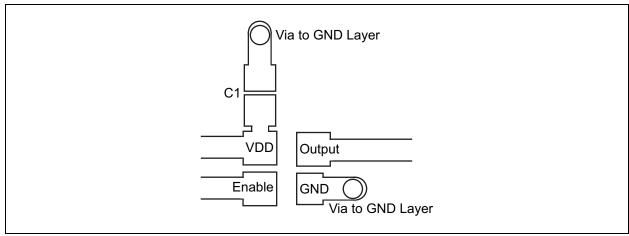


FIGURE 3-3: Recommended Board Layout.

# 4.0 SOLDER REFLOW PROFILE

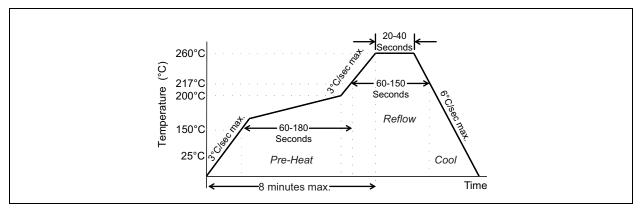


FIGURE 4-1: Solder Reflow Profile.

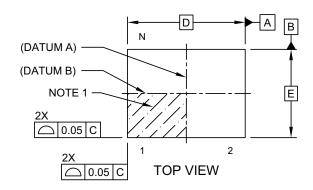
MSL 1 @ 260°C refer to JSTD-020C					
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec. max.				
Preheat Time 150°C to 200°C	60 to 180 sec.				
Time maintained above 217°C	60 to 150 sec.				
Peak Temperature	255°C to 260°C				
Time within 5°C of actual Peak	20 to 40 sec.				
Ramp-Down Rate	6°C/sec. max.				
Time 25°C to Peak Temperature	8 minutes max.				

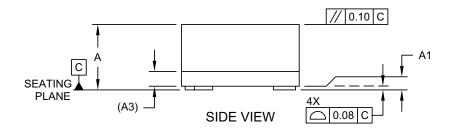
# 5.0 PACKAGING INFORMATION

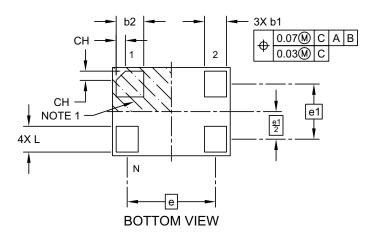
# 4-Lead VFLGA 1.6 mm x 1.2 mm Package Outline

# 4-Lead Very Thin Fine Pitch Land Grid Array (ARA) - 1.6x1.2 mm Body [VFLGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





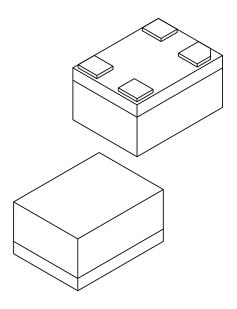


Microchip Technology Drawing C04-1199A Sheet 1 of 2

# 4-Lead VFLGA 1.6 mm x 1.2 mm Package Outline

# 4-Lead Very Thin Fine Pitch Land Grid Array (ARA) - 1.6x1.2 mm Body [VFLGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	Dimension Limits		NOM	MAX
Number of Terminals	N		4	
Terminal Pitch	е		1.20 BSC	
Terminal Pitch	e1		0.75 BSC	
Overall Height	Α	0.79 0.84 0.89		
Standoff	A1	0.00	0.02	0.05
Substrate Thickness (with Terminals)	A3	0.20 REF		
Overall Length	D		1.60 BSC	
Overall Width	Е		1.20 BSC	
Terminal Width	b1	0.25	0.30	0.35
Terminal Width	b2	0.325	0.375	0.425
Terminal Length	L	0.30	0.35	0.40
Terminal 1 Index Chamfer	CH	-	0.125	-

#### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

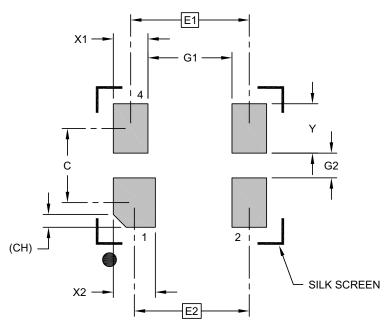
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1199A Sheet 2 of 2

# 4-Lead VFLGA 1.6 mm x 1.2 mm Recommended Land Pattern

# 4-Lead Very Thin Fine Pitch Land Grid Array (ARA) - 1.6x1.2 mm Body [VFLGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX	
Contact Pitch	E1		1.20 BSC		
Contact Pitch	E2		1.16 BSC		
Contact Spacing	С		0.75		
Contact Width (X3)	X1			0.35	
Contact Width	X2			0.43	
Contact Pad Length (X6)	Υ			0.50	
Space Between Contacts (X4)	G1	0.85			
Space Between Contacts (X3)	G2	0.25		·	
Contact 1 Index Chamfer	СН	0	0.13 X 45° REF		

#### Notes:

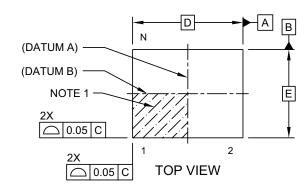
Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.

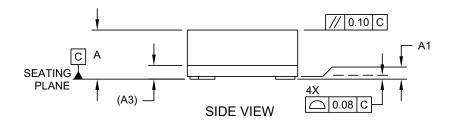
Microchip Technology Drawing C04-3199A

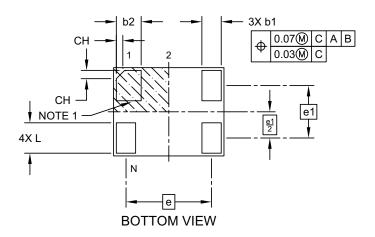
# 4-Lead VFLGA 2.0 mm x 1.6 mm Package Outline

#### 4-Lead Very Thin Fine Pitch Land Grid Array (ASA) - 2.0x1.6 mm Body [VFLGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





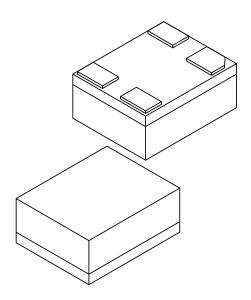


Microchip Technology Drawing C04-1200A Sheet 1 of 2

# 4-Lead VFLGA 2.0 mm x 1.6 mm Package Outline (Continued)

# 4-Lead Very Thin Fine Pitch Land Grid Array (ASA) - 2.0x1.6 mm Body [VFLGA]

: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Number of Terminals	Ν		6	
Terminal Pitch	е		1.55 BSC	
Terminal Pitch	e1		0.95 BSC	
Overall Height	Α	0.79	0.84	0.89
Standoff	A1	0.00	0.02	0.05
Substrate Thickness (with Terminals)	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	Е		1.60 BSC	
Terminal Width	b1	0.30	0.35	0.40
Terminal Width	b2	0.40	0.45	0.50
Terminal Length	L	0.50	0.55	0.60
Terminal 1 Index Chamfer	CH	-	0.15	-

#### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

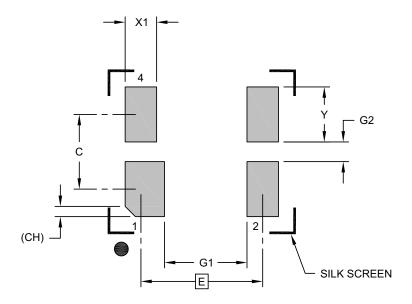
 $\label{lem:REF:Reference Dimension, usually without tolerance, for information purposes only. \\$ 

Microchip Technology Drawing  $\,$  C04-1200A Sheet 2 of 2  $\,$ 

# 4-Lead VFLGA 2.0 mm x 1.6 mm Package Outline

# 4-Lead Very Thin Fine Pitch Land Grid Array (ASA) - 2.0x1.6 mm Body [VFLGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



#### RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	Е	1.55 BSC		
Contact Spacing	С		0.95	
Contact Width (X4)	X1			0.50
Contact Width (X2)	X2			0.40
Contact Pad Length (X6)	Υ			0.70
Space Between Contacts (X4)	G1	1.05		
Space Between Contacts (X3)	G2	0.25		
Contact 1 Index Chamfer	CH	CH 0.13 X 45° REF		

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

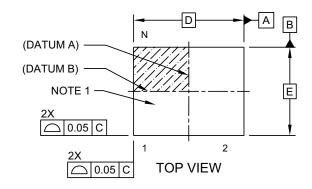
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

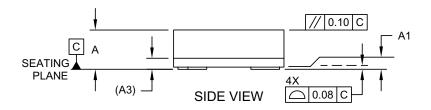
Microchip Technology Drawing C04-3200A

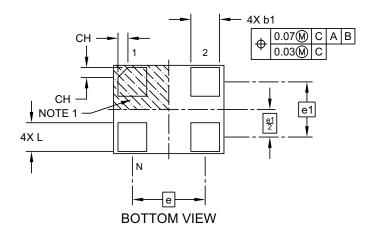
# 4-Lead VLGA 2.5 mm x 2.0 mm Package Outline

#### 4-Lead Very Thin Land Grid Array (AUA) - 2.5x2.0 mm Body [VLGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





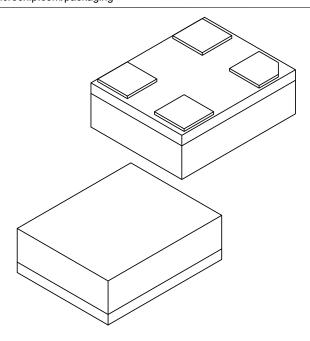


Microchip Technology Drawing C04-1202A Sheet 1 of 2

# 4-Lead VLGA 2.5 mm x 2.0 mm Package Outline (Continued)

# 4-Lead Very Thin Land Grid Array (AUA) - 2.5x2.0 mm Body [VLGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Number of Terminals	Ν		4	
Terminal Pitch	е		1.65 BSC	
Terminal Pitch	e1	1.25 BSC		
Overall Height	Α	0.79	0.84	0.89
Standoff	A1	0.00	0.02	0.05
Substrate Thickness (with Terminals)	A3		0.20 REF	
Overall Length	D		2.50 BSC	
Overall Width	Е		2.00 BSC	
Terminal Width	b1	0.60	0.65	0.70
Terminal Length	L	0.60	0.65	0.70
Terminal 1 Index Chamfer	CH	-	0.225	-

#### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

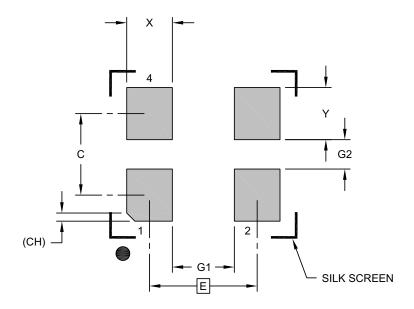
 $\label{eq:REF:Reference Dimension, usually without tolerance, for information purposes only. \\$ 

Microchip Technology Drawing C04-1202A Sheet 2 of 2

# 4-Lead VLGA 2.5 mm x 2.0 mm Recommended Land Pattern

# 4-Lead Very Thin Land Grid Array (AUA) - 2.5x2.0 mm Body [VLGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



#### RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.65 BSC		
Contact Spacing	С		1.25	
Contact Width (X4)	Х			0.70
Contact Pad Length (X6)	Υ			0.80
Space Between Contacts (X4)	G1	0.95		
Space Between Contacts (X3)	G2	0.45		
Contact 1 Index Chamfer	CH	0.13 X 45° REF		

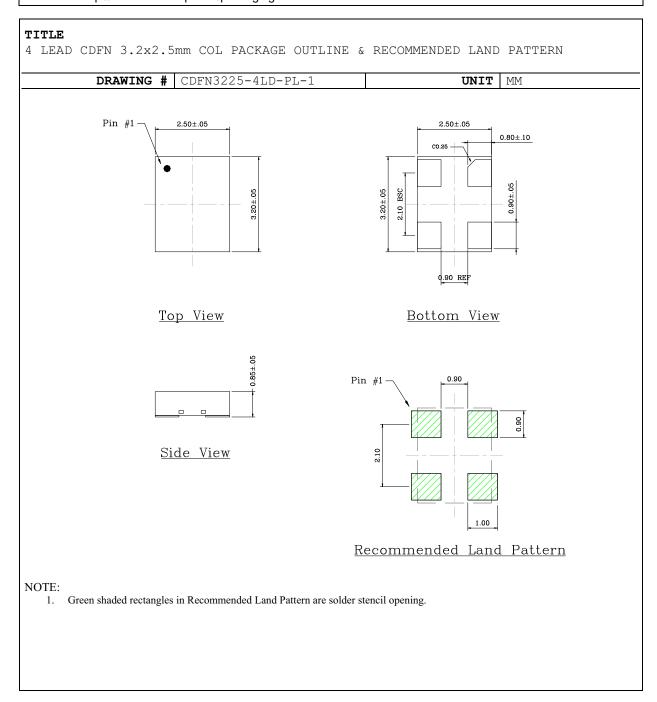
#### Notes:

Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3202A

# 4-Lead CDFN 3.2 mm x 2.5 mm Package Outline and Recommended Land Pattern

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



# **APPENDIX A: REVISION HISTORY**

# **Revision A (September 2016)**

 Initial creation of DSC60xx Microchip data sheet DS20005625A.

# **Revision B (September 2017)**

- Added Power Supply Ramp value in Electrical Characteristics table.
- Redrew diagrams for clarity. No technical content affected.

# **Revision C (November 2018)**

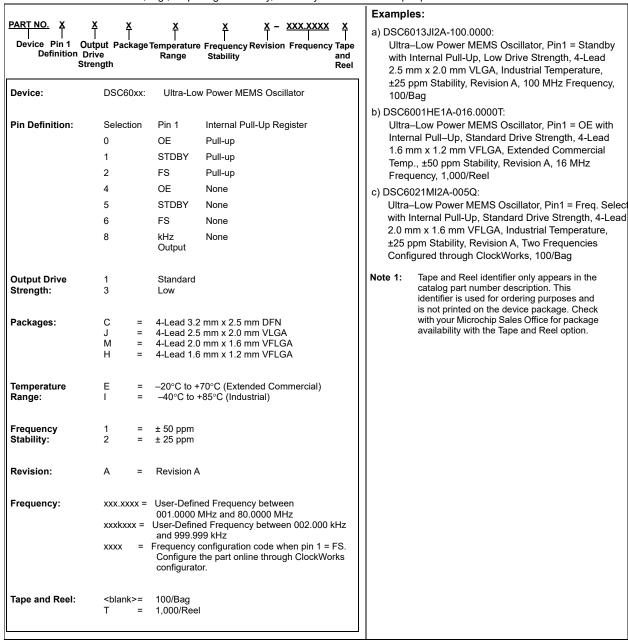
 Added a new condition to the Active Supply Current parameter with a new typical value in the Electrical Characteristics table.



NOTES:

#### PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.



**Note 1:** Please visit Microchip ClockWorks<sup>®</sup> Configurator Website to configure the part number for customized frequency. http://clockworks.microchip.com/timing/.



NOTES:

#### Note the following details of the code protection feature on Microchip devices:

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