DSC60XXB

Ultra-Small, Ultra-Low Power MEMS Oscillator

Features

- Wide Frequency Range: 2 kHz to 80 MHz
- Ultra-Low Power Consumption: 1.3 mA/1 µA (Active/Standby)
- Ultra-Small Footprints
  - 1.6 mm x 1.2 mm
  - 2.0 mm x 1.6 mm
  - 2.5 mm x 2.0 mm
- Frequency Select Input Supports Two Pre-Defined Frequencies
- High Stability: ±20 ppm, ±25 ppm, ±50 ppm
- Wide Temperature Range
  - Automotive: –40°C to +125°C
  - Ext. Industrial: –40°C to +105°C
  - Industrial: –40°C to +85°C
  - Ext. Commercial: –20° to +70°C
- Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - 20x Better MTF Than Quartz Oscillators
- Supply Range of 1.71V to 3.63V
- Short Sample Lead Time: <2 weeks
- Lead Free & RoHS Compliant

Applications

- Low Power/Portable Applications: IoT, Embedded/Smart Devices
- Consumer: Home Healthcare, Fitness Devices, Home Automation
- Automotive: Rear View/Surround View Cameras, Infotainment System (Please refer to DSA60xx Family)
- Industrial: Building/Factory Automation, Surveillance Camera

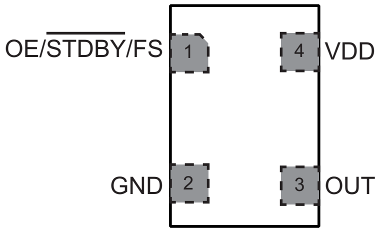
General Description

The DSC60xxB family of MEMS oscillators combines industry-leading low-power consumption, ultra-small packages with exceptional frequency stability, and jitter performance over temperature. The single-output DSC60xxB MEMS oscillators are excellent choices for use as clock references in small, battery-powered devices such as wearable and Internet of Things (IoT) devices in which small size, low power consumption, and long-term reliability are paramount. The Automotive Grade AEC-Q100 qualified option is available for this device.

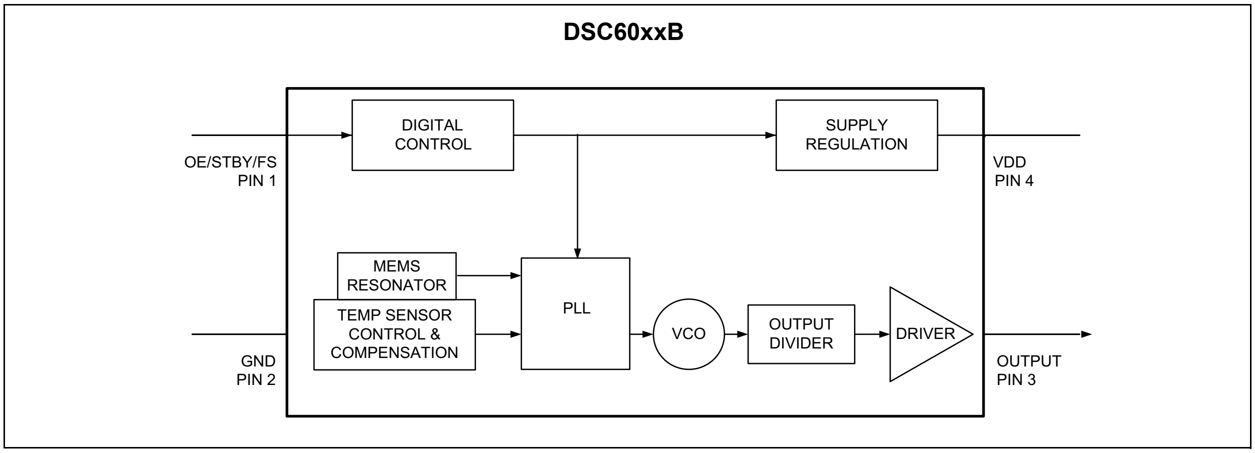
The DSC60xxB family is available in ultra-small 1.6 mm x 1.2 mm, 2.0 mm x 1.6 mm and 2.5 mm x 2.0 mm packages. These packages are "drop-in" replacements for standard 4-pin CMOS quartz crystal oscillators.

Package Types

DSC60xxB
2.5 mm x 2.0 mm LGA
2.0 mm x 1.6 mm LGA
1.6 mm x 1.2 mm LGA
(Top View)



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Supply Voltage .... –0.3V to +4.0V
Input Voltage (V_{IN}) .... –0.3V to V_{DD}+0.3V
ESD Protection .... 4 kV HBM, 400V MM, 2 kV CDM

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 1.8V –5% to 3.3V +10%, T_A = –40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage Note 1	V_{DD}	1.71	—	3.63	V	—
Active Supply Current	I_{DD}	—	1.3	—	mA	F_{OUT} = 24 MHz, V_{DD} = 1.8V, No Load
Power Supply Ramp	t_{PU}	0.1	—	100	ms	Note 9
Standby Supply Current Note 2	I_{STBY}	—	1.0	—	µA	V_{DD} = 1.8/2.5V
		—	1.5	—		V_{DD} = 3.3V
Frequency	f_0	0.002	—	80	MHz	—
Frequency Stability Note 3	Δf	—	—	±20 ±25 ±50	ppm	All temp ranges
Aging	Δf	—	—	±5	ppm	1st year @25°C
		—	—	±1		Per year after first year
Startup Time	t_{SU}	—	—	1.5	ms	From 90% V_{DD} to valid clock output, T = 25°C
Input Logic Levels Note 4	V_{IH}	0.7 x V_{DD}	—	—	V	Input Logic High
	V_{IL}	—	—	0.3 x V_{DD}	V	Input Logic Low
Output Disable Time Note 5	t_{DA}	—	—	200 + 2 Periods	ns	—
Output Enable Time Note 6	t_{EN}	—	—	1	µs	—
Enable Pull-Up Resistor Note 7	—	—	300	—	kΩ	If configured
Output Logic Levels, Low Drive	V_{OH}	0.8 x V_{DD}	—	—	V	Output Logic High, I = 1 mA
	V_{OL}	—	—	0.2 x V_{DD}	V	Output Logic Low, I = –1 mA

Note 1: Pin 4 V_{DD} should be filtered with 0.1 µF capacitor.
2: Not including current through pull-up resistor on EN pin (if configured).
3: Includes frequency variations due to initial tolerance, temp. and power supply voltage.
4: Input waveform must be monotonic with rise/fall time < 10 ms
5: Output Disable time takes up to two periods of the output waveform + 200 ns.
6: For parts configured with OE, not Standby.
7: Output is enabled if pad is floated or not connected.
8: Output Duty Cycle will be 40% to 60% when output frequency is between 40 MHz to 60 MHz.
9: Time to reach 90% of target V_{DD}. Power ramp rise must be monotonic.
10: Peak-to-peak period jitter is measured over 10,000 cycles.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 1.8V –5% to 3.3V +10%, T_A = –40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Output Transition Time Rise Time/Fall Time	t_{RX}/t_{FX}	—	2.5	3.5	ns	DSC60x3B Low Drive, 20% to 80% C_L = 5 pF	V_{DD} = 1.8V
		—	1.5	2.2			V_{DD} = 2.5V/3.3V
	t_{RY}/t_{FY}	—	1.2	2.0	ns	DSC60x1B Std. Drive, 20% to 80% C_L = 10 pF	V_{DD} = 1.8V
		—	0.6	1.2			V_{DD} = 2.5V/3.3V
Output Duty Cycle Note 8	SYM	45	—	55	%	—	
Period Jitter, RMS	J_{PER}	—	28	—	ps	DSC60x3B Low Drive, F_{OUT} = 27 MHz C_L = 5 pF	V_{DD} = 1.8V
		—	23	—			V_{DD} = 2.5V/3.3V
		—	20	—		DSC60x1B Std. Drive, F_{OUT} = 27 MHz C_L = 10 pF	V_{DD} = 1.8V
		—	18	—			V_{DD} = 2.5V/3.3V
Cycle-to-Cycle Jitter, Peak	$J_{Cy–Cy}$	—	120	—	ps	DSC60x3B Low Drive, F_{OUT} = 27 MHz C_L = 5 pF	V_{DD} = 1.8V
		—	90	—			V_{DD} = 2.5V/3.3V
		—	115	—		DSC60x1B Std. Drive, F_{OUT} = 27 MHz C_L = 10 pF	V_{DD} = 1.8V
		—	90	—			V_{DD} = 2.5V/3.3V

Note 1: Pin 4 V_{DD} should be filtered with 0.1 µF capacitor.
2: Not including current through pull-up resistor on EN pin (if configured).
3: Includes frequency variations due to initial tolerance, temp. and power supply voltage.
4: Input waveform must be monotonic with rise/fall time < 10 ms
5: Output Disable time takes up to two periods of the output waveform + 200 ns.
6: For parts configured with OE, not Standby.
7: Output is enabled if pad is floated or not connected.
8: Output Duty Cycle will be 40% to 60% when output frequency is between 40 MHz to 60 MHz.
9: Time to reach 90% of target V_{DD}. Power ramp rise must be monotonic.
10: Peak-to-peak period jitter is measured over 10,000 cycles.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 1.8V –5% to 3.3V +10%, T_A = –40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Period Jitter, Peak-to-Peak, Note 10	$J_{PERPK-PK}$	—	210	—	ps	DSC60x3B Low Drive, F_{OUT} = 27 MHz C_L = 5 pF	V_{DD} = 1.8V
		—	190	—			V_{DD} = 2.5V/3.3V
		—	160	—		DSC60x1B Std. Drive, F_{OUT} = 27 MHz C_L = 10 pF	V_{DD} = 1.8V
		—	144	—			V_{DD} = 2.5V/3.3V

Note 1: Pin 4 V_{DD} should be filtered with 0.1 µF capacitor.

2: Not including current through pull-up resistor on EN pin (if configured).

3: Includes frequency variations due to initial tolerance, temp. and power supply voltage.

4: Input waveform must be monotonic with rise/fall time < 10 ms

5: Output Disable time takes up to two periods of the output waveform + 200 ns.

6: For parts configured with OE, not Standby.

7: Output is enabled if pad is floated or not connected.

8: Output Duty Cycle will be 40% to 60% when output frequency is between 40 MHz to 60 MHz.

9: Time to reach 90% of target V_{DD}. Power ramp rise must be monotonic.

10: Peak-to-peak period jitter is measured over 10,000 cycles.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature	T_J	—	—	+150	°C	—
Storage Ambient Temperature Range	T_S	–55	—	+150	°C	—
Soldering Temperature	—	—	+260	—	°C	40 sec. max.

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

The DSC60xxB is a highly configurable device and can be factory programmed in many different ways to meet the customer's needs. Microchip's ClockWorks® Configurator http://clockworks.microchip.com/Timing/ must be used to choose the necessary options, create the final part number, data sheet, and order samples. The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: DSC60XXB PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	OE	Output Enable: H = Active, L = Disabled (High Impedance).
	$\overline{\text{STDBY}}$	Standby: H = Device is active, L = Device is in standby (Low Power Mode).
	FS	Frequency Select: H = Output Frequency 1, L = Output Frequency 2.
2	GND	Ground.
3	OUTPUT	Oscillator clock output
4	VDD	Power Supply: 1.71V to 3.63V.

An explanation of the different options listed in Table 2-1 follows.

2.1 Pin 1

This is a control pin and may be configured to fulfill one of six different functions. If not actively driven, a 10 kΩ pull-up resistor is recommended.

2.1.1 OUTPUT ENABLE (OE)

Pin 1 may be configured as OE. Oscillator output may be turned on and off according to the state of this pin.

2.1.2 $\overline{\text{STDBY}}$

Pin 1 may be configured as Standby. When the pin is low, both output buffer and PLL will be off and the device will enter a low power mode.

2.1.3 FREQUENCY SELECT (FS)

Pin 1 may be configured as FS. The output may be set to one of two pre-programmed frequencies. The output clock frequencies can only be set to either kHz or MHz. A combination of kHz and MHz cannot be set.

2.2 Pins 2 through 4

Pins 2 and 4 are the supply terminals, GND and VDD respectively. Pin 3 is the clock output, programmable to Standard and Low Drive strength settings. Visit ClockWorks® Configurator to customize your device.

3.0 DIAGRAMS

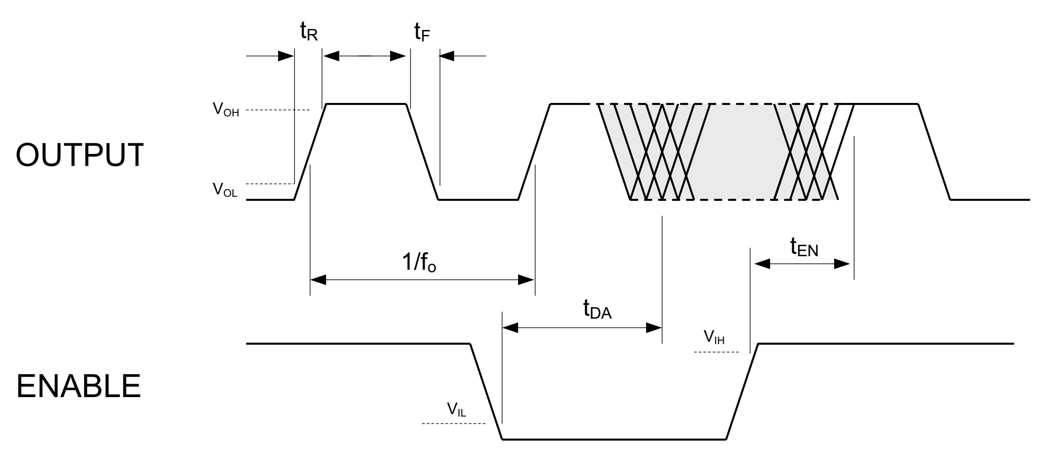


FIGURE 3-1: *Output Waveform.*

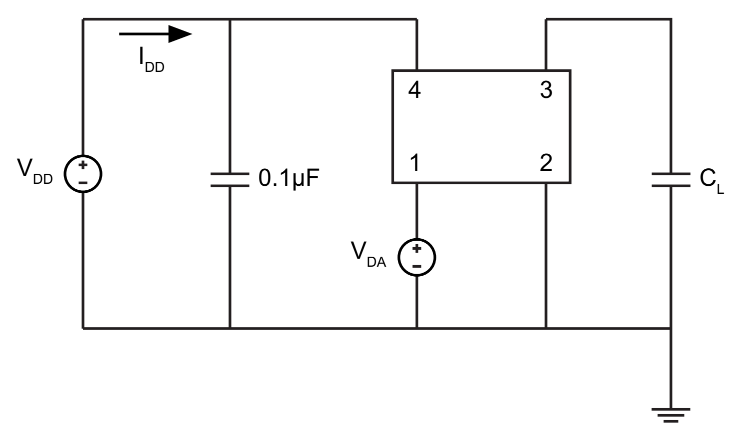


FIGURE 3-2: *Test Circuit.*

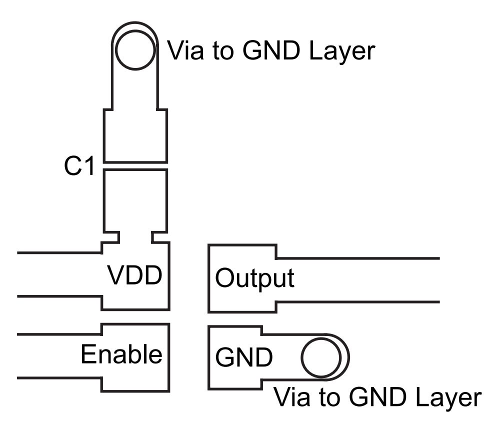


FIGURE 3-3: *Recommended Board Layout.*

4.0 SOLDER REFLOW PROFILE

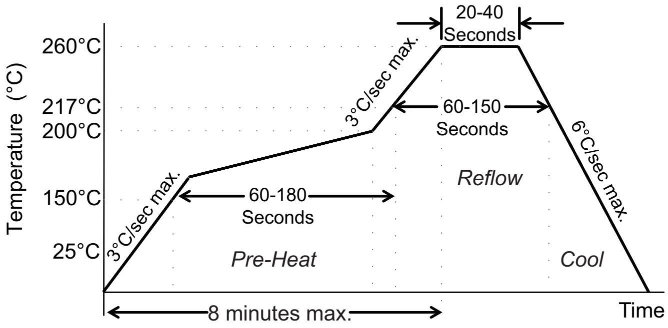


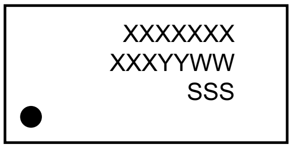
FIGURE 4-1: *Solder Reflow Profile.*

MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of actual Peak	20 to 40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

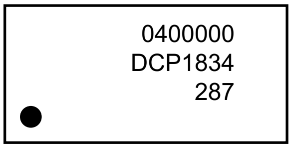
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

4-Lead VFLGA*
2.5 x 2.0

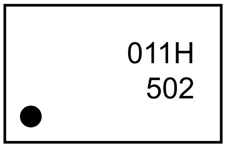


Example



4-Lead VFLGA*
2.0 x 1.6/1.6 x 1.2

Example



Legend:		
	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	SSS	Alphanumeric traceability code
	ⓔ3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

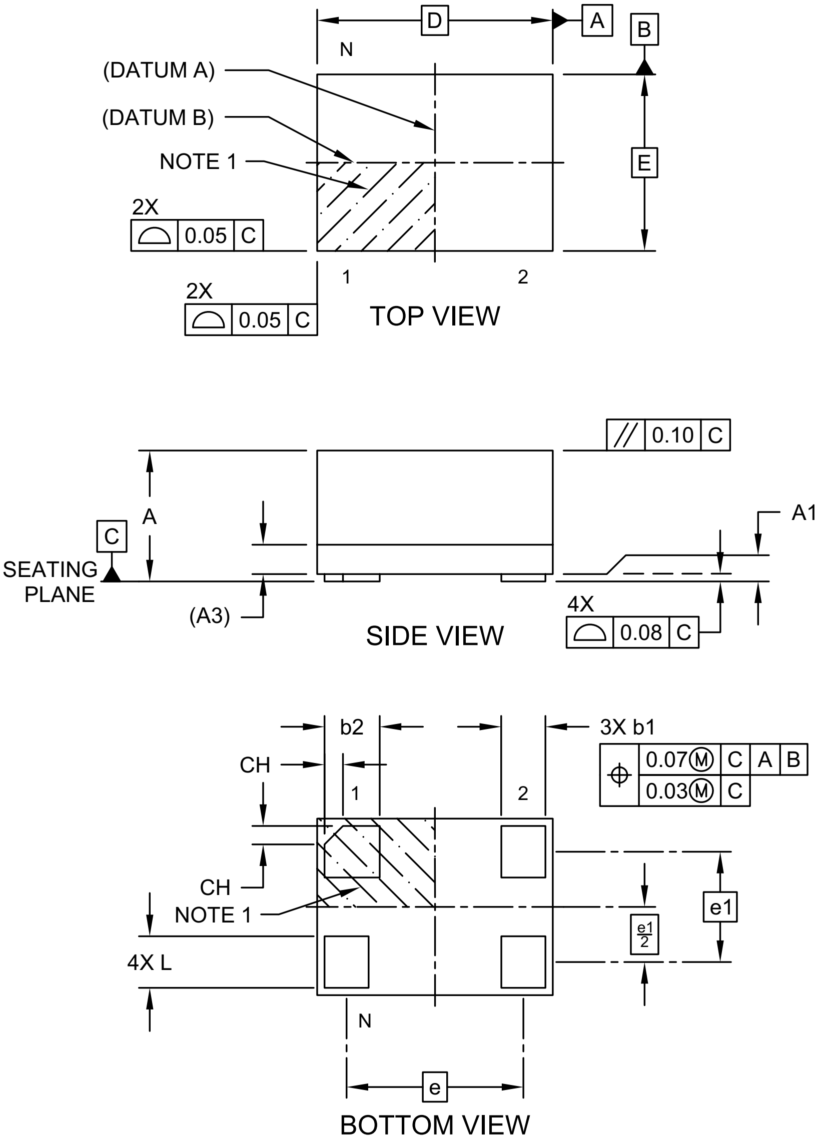
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

4-Lead VFLGA 1.6 mm x 1.2 mm Package Outline

4-Lead Very Thin Fine Pitch Land Grid Array (ARA) - 1.6x1.2 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

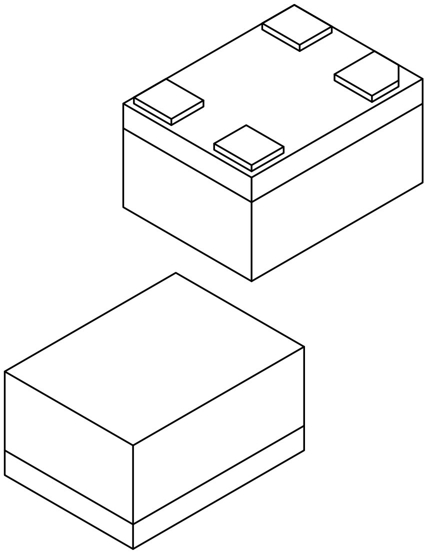


Microchip Technology Drawing C04-1199A Sheet 1 of 2

4-Lead VFLGA 1.6 mm x 1.2 mm Package Outline

4-Lead Very Thin Fine Pitch Land Grid Array (ARA) - 1.6x1.2 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		4	
Terminal Pitch	e		1.20 BSC	
Terminal Pitch	e1		0.75 BSC	
Overall Height	A	0.79	0.84	0.89
Standoff	A1	0.00	0.02	0.05
Substrate Thickness (with Terminals)	A3		0.20 REF	
Overall Length	D		1.60 BSC	
Overall Width	E		1.20 BSC	
Terminal Width	b1	0.25	0.30	0.35
Terminal Width	b2	0.325	0.375	0.425
Terminal Length	L	0.30	0.35	0.40
Terminal 1 Index Chamfer	CH	-	0.125	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

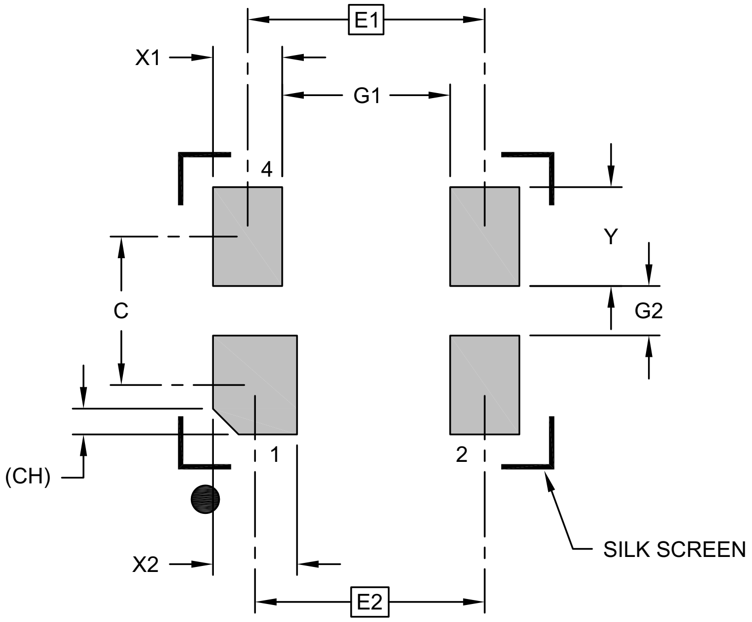
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1199A Sheet 2 of 2

4-Lead VFLGA 1.6 mm x 1.2 mm Recommended Land Pattern

4-Lead Very Thin Fine Pitch Land Grid Array (ARA) - 1.6x1.2 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E1		1.20 BSC	
Contact Pitch	E2		1.16 BSC	
Contact Spacing	C		0.75	
Contact Width (X3)	X1			0.35
Contact Width	X2			0.43
Contact Pad Length (X6)	Y			0.50
Space Between Contacts (X4)	G1	0.85		
Space Between Contacts (X3)	G2	0.25		
Contact 1 Index Chamfer	CH		0.13 X 45° REF	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

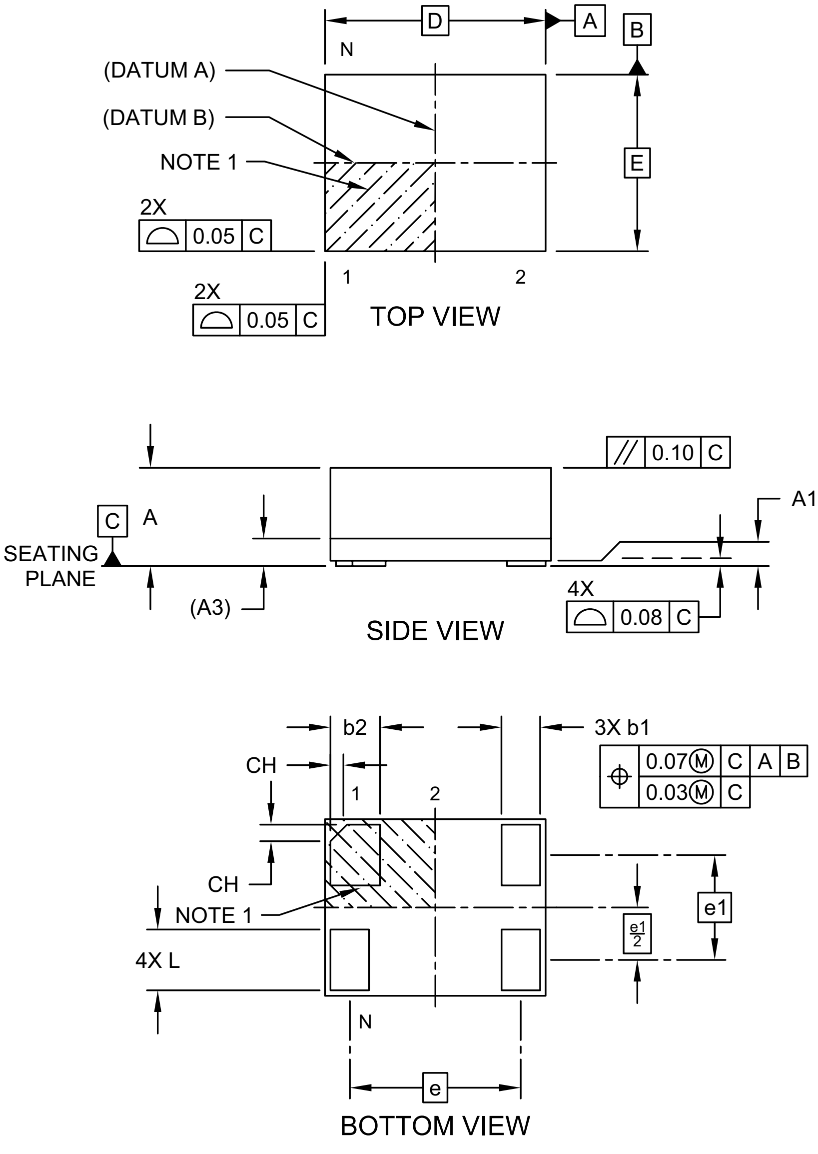
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3199A

4-Lead VFLGA 2.0 mm x 1.6 mm Package Outline

4-Lead Very Thin Fine Pitch Land Grid Array (ASA) - 2.0x1.6 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

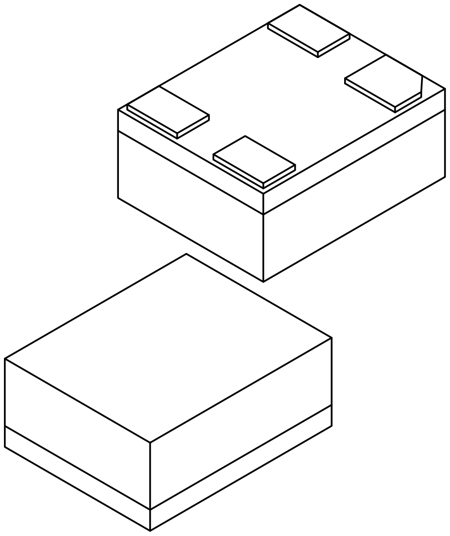


Microchip Technology Drawing C04-1200A Sheet 1 of 2

4-Lead VFLGA 2.0 mm x 1.6 mm Package Outline (Continued)

4-Lead Very Thin Fine Pitch Land Grid Array (ASA) - 2.0x1.6 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		6	
Terminal Pitch	e		1.55 BSC	
Terminal Pitch	e1		0.95 BSC	
Overall Height	A	0.79	0.84	0.89
Standoff	A1	0.00	0.02	0.05
Substrate Thickness (with Terminals)	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		1.60 BSC	
Terminal Width	b1	0.30	0.35	0.40
Terminal Width	b2	0.40	0.45	0.50
Terminal Length	L	0.50	0.55	0.60
Terminal 1 Index Chamfer	CH	-	0.15	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

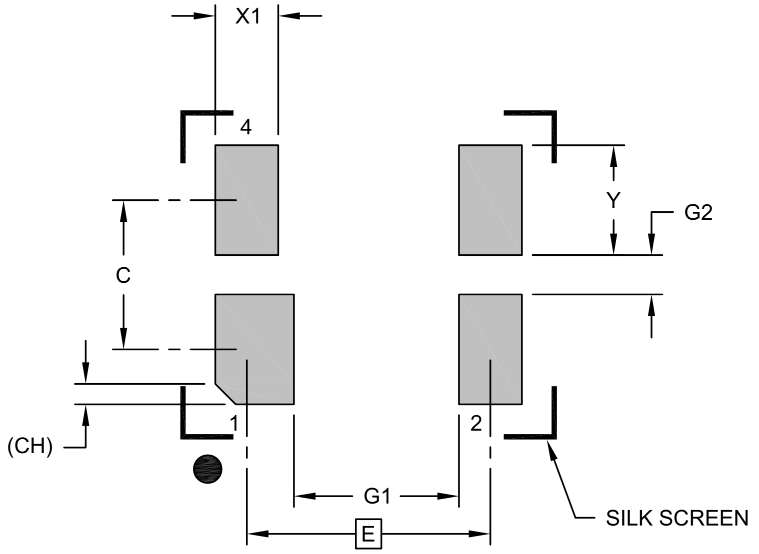
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1200A Sheet 2 of 2

4-Lead VFLGA 2.0 mm x 1.6 mm Package Outline

4-Lead Very Thin Fine Pitch Land Grid Array (ASA) - 2.0x1.6 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	1.55 BSC		
Contact Spacing	C		0.95	
Contact Width (X4)	X1			0.50
Contact Width (X2)	X2			0.40
Contact Pad Length (X6)	Y			0.70
Space Between Contacts (X4)	G1	1.05		
Space Between Contacts (X3)	G2	0.25		
Contact 1 Index Chamfer	CH	0.13 X 45° REF		

Notes:

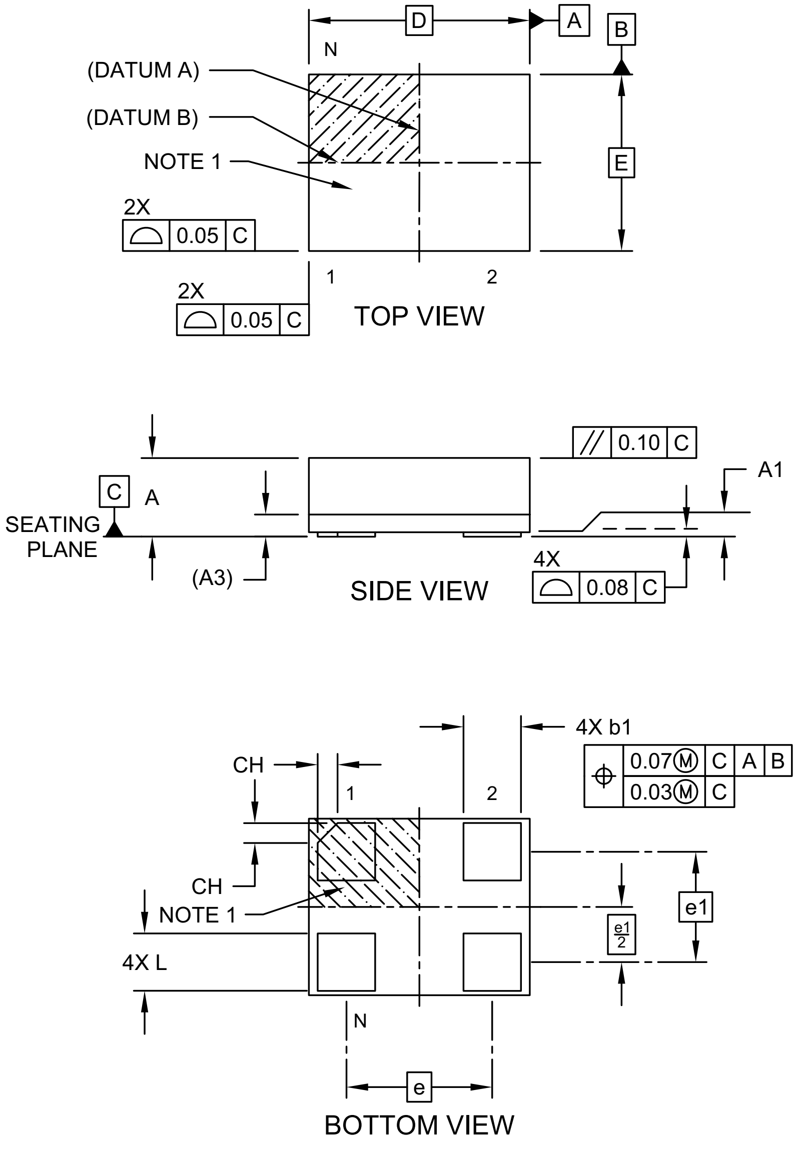
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3200A

4-Lead VLGA 2.5 mm x 2.0 mm Package Outline

4-Lead Very Thin Land Grid Array (AUA) - 2.5x2.0 mm Body [VLGA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

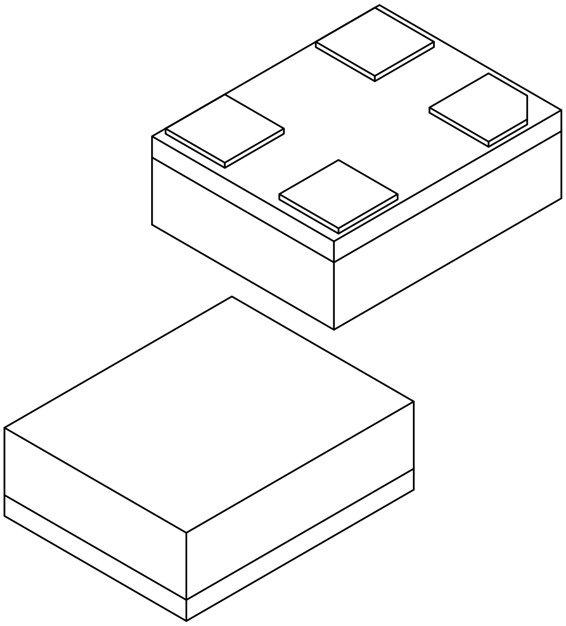


Microchip Technology Drawing C04-1202A Sheet 1 of 2

4-Lead VLGA 2.5 mm x 2.0 mm Package Outline (Continued)

4-Lead Very Thin Land Grid Array (AUA) - 2.5x2.0 mm Body [VLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		4	
Terminal Pitch	e		1.65 BSC	
Terminal Pitch	e1		1.25 BSC	
Overall Height	A	0.79	0.84	0.89
Standoff	A1	0.00	0.02	0.05
Substrate Thickness (with Terminals)	A3		0.20 REF	
Overall Length	D		2.50 BSC	
Overall Width	E		2.00 BSC	
Terminal Width	b1	0.60	0.65	0.70
Terminal Length	L	0.60	0.65	0.70
Terminal 1 Index Chamfer	CH	-	0.225	-

Notes:

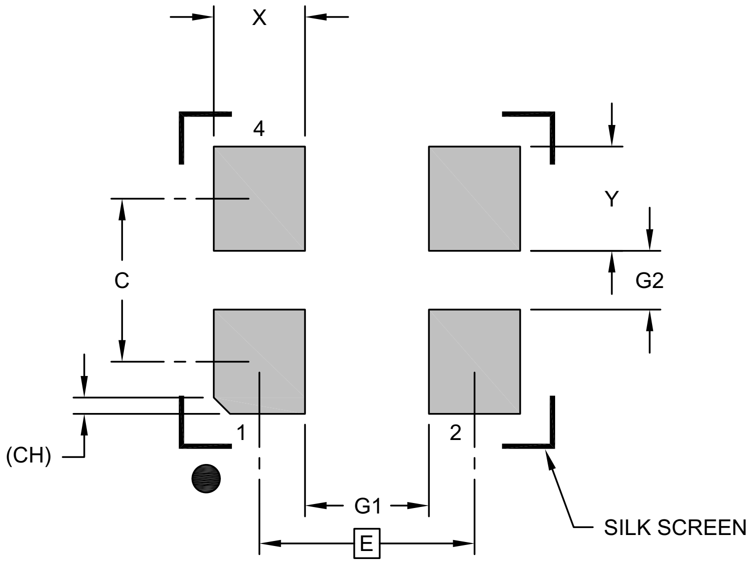
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1202A Sheet 2 of 2

4-Lead VLGA 2.5 mm x 2.0 mm Recommended Land Pattern

4-Lead Very Thin Land Grid Array (AUA) - 2.5x2.0 mm Body [VLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.65 BSC		
Contact Spacing	C		1.25	
Contact Width (X4)	X			0.70
Contact Pad Length (X6)	Y			0.80
Space Between Contacts (X4)	G1	0.95		
Space Between Contacts (X3)	G2	0.45		
Contact 1 Index Chamfer	CH	0.13 X 45° REF		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3202A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (January 2019)

- Initial creation of DSC60xxB Microchip data sheet DS20006133A.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	X	X	X –	XXX.XXXX	X
Device	Pin 1 Definition	Output Drive Strength	Package	Temperature Range	Frequency Stability	Revision	Frequency	Tape and Reel

Device: DSC60: Ultra-Low Power MEMS Oscillator

Pin 1 Definition:

Selection	Pin 1	Internal Pull-Up Register
0	OE	Pull-up
1	$\overline{\text{STDBY}}$	Pull-up
2	FS	Pull-up
4	OE	None
5	$\overline{\text{STDBY}}$	None
6	FS	None

Output Drive Strength:

1	Standard
3	Low

Package:
J = 4-Lead 2.5 mm x 2.0 mm VLGA
M = 4-Lead 2.0 mm x 1.6 mm VFLGA
H = 4-Lead 1.6 mm x 1.2 mm VFLGA

Temperature Range:
A = –40°C to +125°C (Automotive)
L = –40°C to +105°C (Extended Industrial)
I = –40°C to +85°C (Industrial)
E = –20°C to +70°C (Extended Commercial)

Frequency Stability:
1 = ± 50 ppm
2 = ± 25 ppm
3 = ± 20 ppm

Revision:
B = Revision B

Frequency:
xxx.xxxx = User-Defined Frequency between 001.0000 MHz and 80.0000 MHz
xxxkxxx = User-Defined Frequency between 002.000 kHz and 999.999 kHz
xxxx = Frequency configuration code when pin 1 = FS. Configure the part online through ClockWorks® configurator.

Tape and Reel:
<blank>= 140/Tube (J Package Option)
<blank>= 100/Bag (M & H Package Options)
T = 1,000/Reel
B = 3,000/Reel

Examples:

a) DSC6013JI3B-80.0000:
Ultra–Low Power MEMS Oscillator, Pin1 = $\overline{\text{STDBY}}$ with Internal Pull-Up, Low Drive Strength, 4-Lead 2.5 mm x 2.0 mm VLGA, Industrial Temperature, ±20 ppm Stability, Revision B, 80 MHz Frequency, 140/Tube

b) DSC6001HE1B-016.0000T:
Ultra–Low Power MEMS Oscillator, Pin1 = OE with Internal Pull–Up, Standard Drive Strength, 4-Lead 1.6 mm x 1.2 mm VFLGA, Extended Commercial Temp., ±50 ppm Stability, Revision B, 16 MHz Frequency, 1,000/Reel

c) DSC6021MI2B-005Q:
Ultra–Low Power MEMS Oscillator, Pin1 = Freq. Select with Internal Pull-Up, Standard Drive Strength, 4-Lead 2.0 mm x 1.6 mm VFLGA, Industrial Temperature, ±25 ppm Stability, Revision B, Two Frequencies Configured through ClockWorks, 100/Bag

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note 1: Please visit Microchip ClockWorks® Configurator Website to configure the part number for customized frequency. http://clockworks.microchip.com/timing/.

NOTES:

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