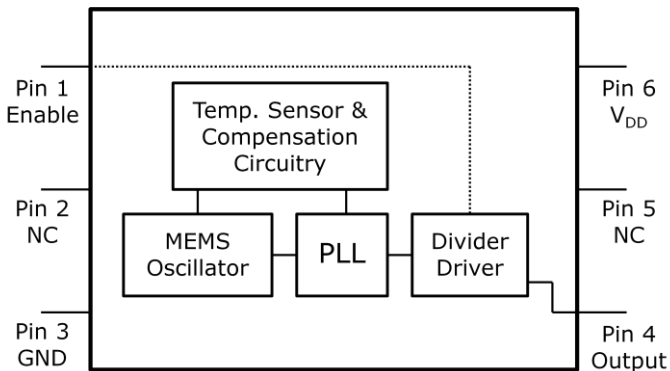# DSC8101 | DSC8121

**MICREL** ®

## Programmable Low-Jitter Precision CMOS Oscillator

## General Description

The DSC8101 & DSC8121 series of high performance field-programmable oscillators utilizes a proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. Using the TIMEFLASH programmer, the end user can easily program the oscillators' frequency in the field for immediate testing or use in advance prototype development or production.

DSC8101 has a standby feature allowing it to completely power-down when EN pin is pulled low; whereas for DSC8121, only the outputs are disabled when EN is low. Both oscillators are available in industry standard packages, including the small 3.2x2.5 mm$^2$, and are "drop-in" replacement for standard 4-pin CMOS quartz oscillators.

## Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±10, ±25, ±50 ppm**
- **Wide Temperature Range**
  - o Automotive: -55° to 125° C
  - o Ext. Industrial: -40° to 105° C
  - o Industrial: -40° to 85° C
  - o Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **Wide Freq. Range: 10 to 170 MHz**
- **Small Industry Standard Footprints**
  - o 2.5x2.0, 3.2x2.5, 5.0x3.2, & 7.0x5.0 mm
- **Excellent Shock & Vibration Immunity**
  - o Qualified to MIL-STD-883
- **High Reliability**
  - o 20x better MTF than quartz oscillators
- **Low Current Consumption**
- **Supply Range of 2.25 to 3.6 V**
- **Standby & Output Enable Function**
- **Lead Free & RoHS Compliant**

## Block Diagram



## Output Enable Modes

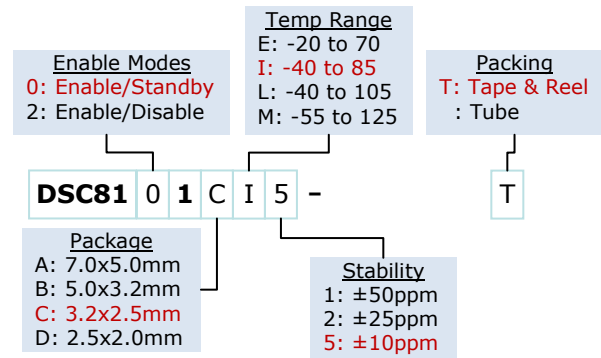| EN Pin | DSC8101 | DSC8121 |
|--------|---------|---------|
| High | Output Active | Output Active |
| NC | Output Active | Output Active |
| Low | Standby | Output Disabled |

## Applications

- **Storage Area Networks**
  - o SATA, SAS, Fibre Channel
- **Passive Optical Networks**
  - o EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
  - o 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express**
- **DisplayPort**

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## Absolute Maximum Ratings

| Item | Min | Max | Unit | Condition |
|------|-----|-----|------|-----------|
| Supply Voltage | -0.3 | +4.0 | V | |
| Input Voltage | -0.3 | $V_{DD}$+0.3 | V | |
| Junction Temp | - | +150 | °C | |
| Storage Temp | -55 | +150 | °C | |
| Soldering Temp | - | +260 | °C | 40sec max. |
| ESD | - | | V | |
| HBM | | 4000 | | |
| MM | | 400 | | |
| CDM | | 1500 | | |

Note: 1000+ years of data retention on internal memory

## Ordering Code

Enable Modes
0: Enable/Standby
2: Enable/Disable

Temp Range
E: -20 to 70
I: -40 to 85
L: -40 to 105
M: -55 to 125

Packing
T: Tape & Reel
: Tube

**DSC81** 0 1 C I 5 – T

Package
A: 7.0x5.0mm
B: 5.0x3.2mm
C: 3.2x2.5mm
D: 2.5x2.0mm

Stability
1: ±50ppm
2: ±25ppm
5: ±10ppm

## Specifications

| Parameter | | Condition | Min. | Typ. | Max. | Unit |
|-----------|--|-----------|------|------|------|------|
| Supply Voltage[1] | $V_{DD}$ | | 2.25 | | 3.6 | V |
| Supply Current | $I_{DD}$ | EN pin low – output is disabled<br>DSC8101<br>DSC8121 | | 20 | 0.095<br>22 | mA |
| Frequency Stability<br>    Ext Comm. & Ind. only<br>    All temp ranges<br>    All temp ranges | Δf | Includes frequency variations due to initial tolerance, temp. and power supply voltage | | | ±10<br>±25<br>±50 | ppm |
| Aging | Δf | 1 year @25°C | | | ±5 | ppm |
| Startup Time[2] | $t_{SU}$ | T=25°C | | | 5 | ms |
| Input Logic Levels<br>    Input logic high<br>    Input logic low | $V_{IH}$<br>$V_{IL}$ | | 0.75x$V_{DD}$<br>- | | -<br>0.25x$V_{DD}$ | V |
| Output Disable Time[3] | $t_{DA}$ | | | | 5 | ns |
| Output Enable Time | $t_{EN}$ | DSC8101<br>DSC8121 | | | 5<br>20 | ms<br>ns |
| Enable Pull-Up Resistor[4] | | Pull-up resistor exist | | 40 | | kΩ |
| **CMOS Output** | | | | | | |
| Supply Current[4] | $I_{DD}$ | output is enabled<br>$C_L$=15pF, $F_0$=125 MHz | | 31 | 35 | mA |
| Output Logic Levels<br>    Output logic high<br>    Output logic low | $V_{OH}$<br>$V_{OL}$ | I=±6mA | 0.9x$V_{DD}$<br>- | | -<br>0.1x$V_{DD}$ | V |
| Output Transition time[3]<br>    Rise Time<br>    Fall Time | $t_R$<br>$t_F$ | 20% to 80%<br>$C_L$=15pF | | 1.1<br>1.3 | 2<br>2 | ns |
| Frequency | $f_0$ | All temp range except Auto<br>Auto temp range | 10 | | 170<br>100 | MHz |
| Output Duty Cycle | SYM | | 45 | | 55 | % |
| Period Jitter | $J_{PER}$ | Fout=125MHz | | 3 | | $ps_{RMS}$ |
| Integrated Phase Noise | $J_{PH}$ | 200kHz to 20MHz @ 125MHz<br>100kHz to 20MHz @ 125MHz<br>12kHz to 20MHz @ 125MHz | | 0.3<br>0.38<br>1.7 | <br><br>2 | $ps_{RMS}$ |

1.  Pin 6 $V_{DD}$ should be filtered with 0.1uf capacitor.
2.  $t_{su}$ is time to 100PPM of output frequency after $V_{DD}$ is applied and outputs are enabled.
3.  Output Waveform and Test Circuit figures below define the parameters.
4.  Output is enabled if pad is floated or not connected.

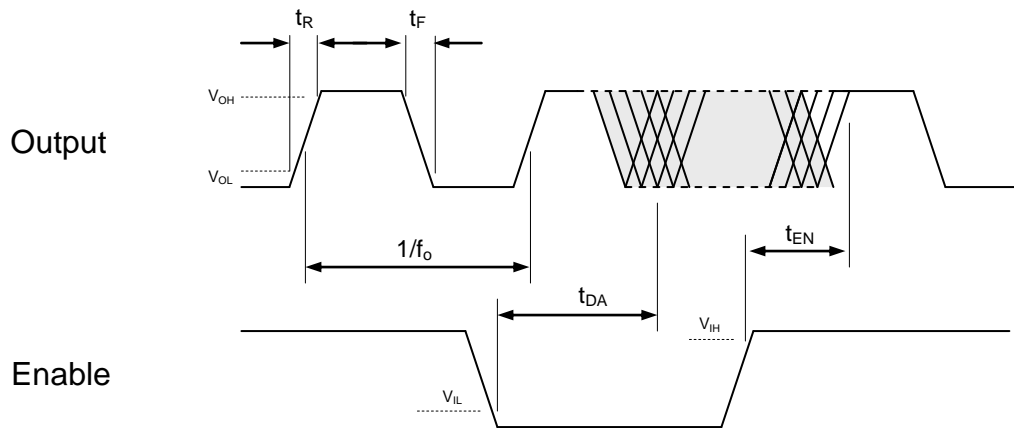## Nominal Performance Parameters (Unless specified otherwise: T=25° C, $V_{DD}$=3.3 V)
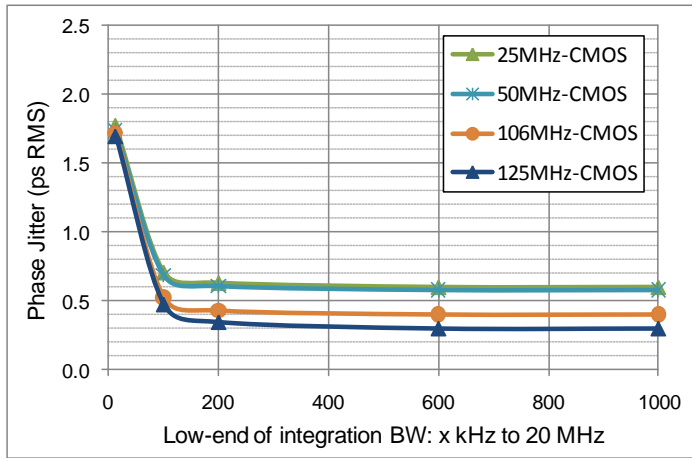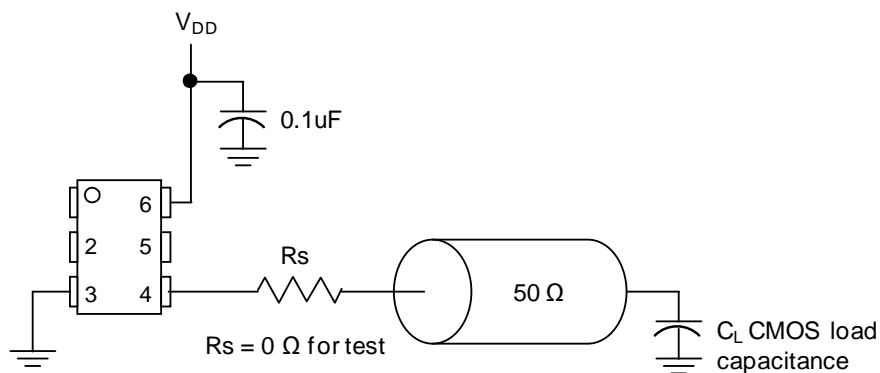
Phase jitter (integrated phase noise)
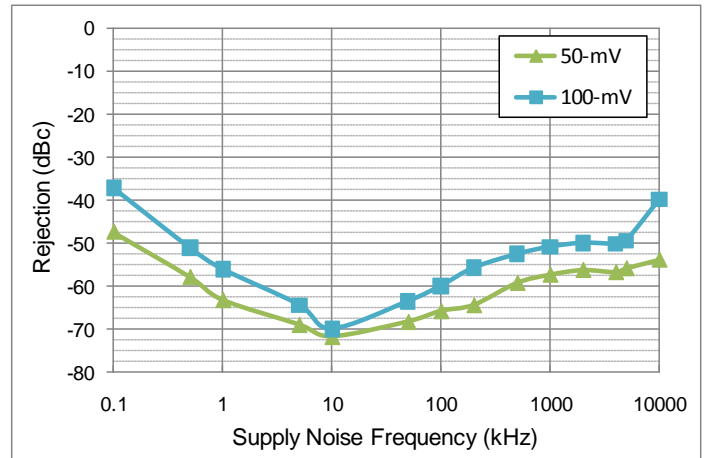
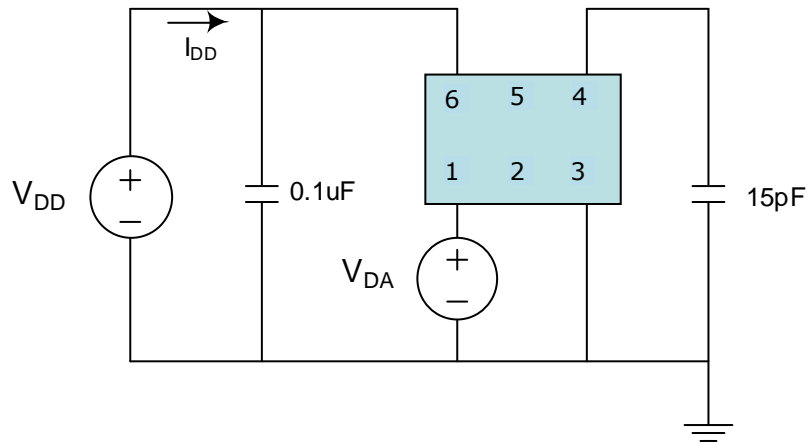Power supply rejection ratio

## Output Waveform

## Typical Termination Scheme

$V_{DD}$

0.1uF

Rs

Rs = 0 Ω for test

50 Ω

$C_L$ CMOS load capacitance

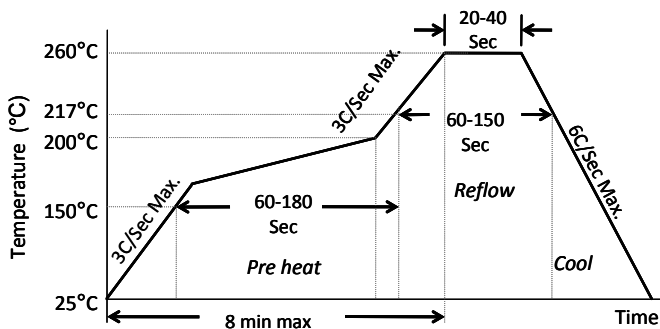Rs serves to match the trace impedances. Depending on board layout, the value may range from 0 to 30 ohms.

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## Test Circuit



## Board Layout (recommended)
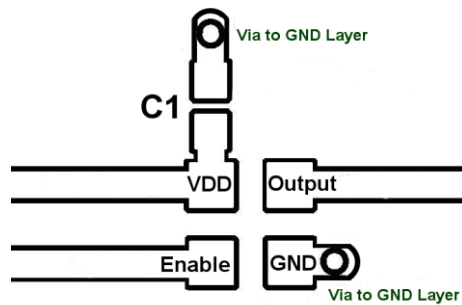


## Solder Reflow Profile



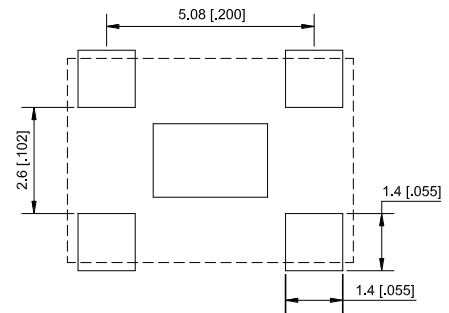| MSL 1 @ 260°C refer to JSTD-020C | |
| --- | --- |
| Ramp-Up Rate (200°C to Peak Temp) | 3°C/Sec Max. |
| Preheat  Time 150°C to 200°C | 60-180  Sec |
| Time maintained above 217°C | 60-150 Sec |
| Peak Temperature | 255-260°C |
| Time within 5°C of actual Peak | 20-40 Sec |
| Ramp-Down Rate | 6°C/Sec Max. |
| Time 25°C to Peak Temperature | 8 min Max. |

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# Package Dimensions
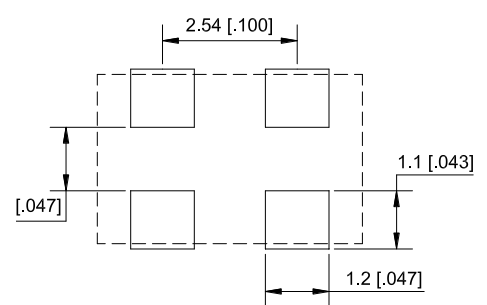
## 7.0 x 5.0 mm Plastic Package
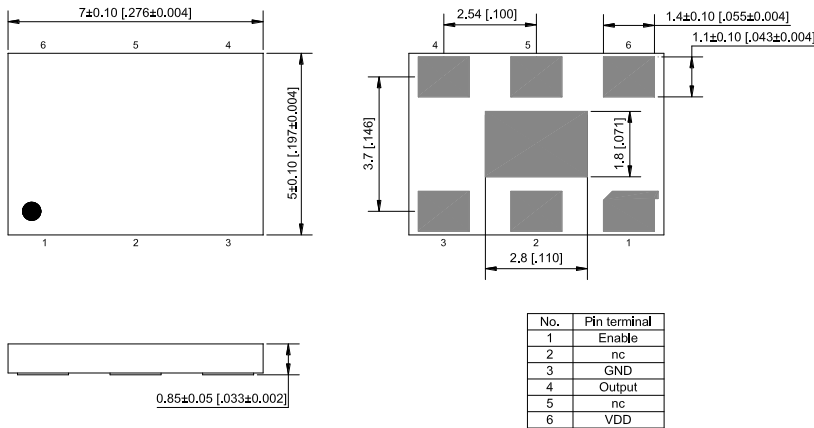
External Dimensions
units: mm[inch]

7±0.10 [.276±0.004]
5±0.10 [.197±0.004]

0.85±0.05 [.033±0.002]

2.54 [.100]
3.7 [.146]
2.8 [.110]
1.4±0.10 [.055±0.004]
1.1±0.10 [.043±0.004]
1.8 [.071]

Recommended
Solder Pad Layout
units: mm[inch]

5.08 [.200]
2.6 [.102]
1.4 [.055]
1.4 [.055]

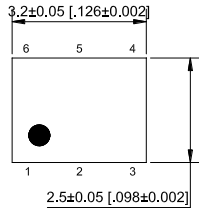| No. | Pin terminal |
|-----|--------------|
| 1 | Enable |
| 2 | nc |
| 3 | GND |
| 4 | Output |
| 5 | nc |
| 6 | VDD |

## 5.0 x 3.2 mm Plastic Package

External Dimensions
units: mm[inch]

5±0.05 [.197±0.002]
3.2±0.05 [.126±0.002]

0.85±0.05 [.033±0.002]

1.27 [.050]
1.2 [.047] REF
0.64±0.05 [.025±0.002]
1±0.05 [.039±0.002]

Recommended
Solder Pad Layout
units: mm[inch]

2.54 [.100]
[.047]
1.1 [.043]
1.2 [.047]

| No. | Pin terminal |
|-----|--------------|
| 1 | Enable |
| 2 | nc |
| 3 | GND |
| 4 | Output |
| 5 | nc |
| 6 | VDD |

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## 3.2 x 2.5 mm Plastic Package

External Dimensions
units: mm[inch]
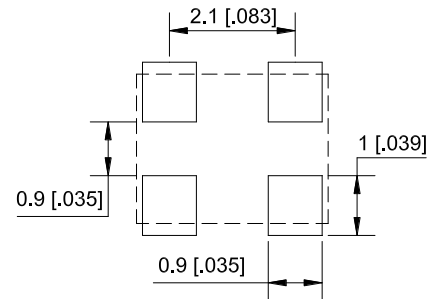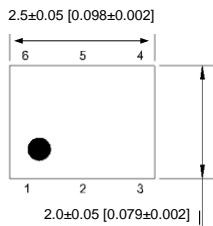
Recommended
Solder Pad Layout
units: mm[inch]

3.2±0.05 [.126±0.002]
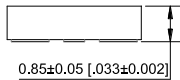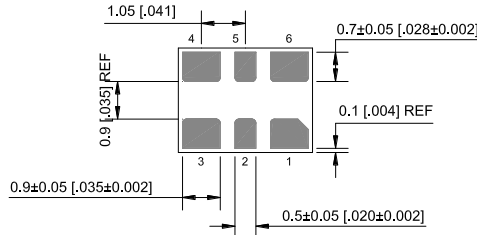
6  5  4

1  2  3

2.5±0.05 [.098±0.002]

0.85±0.05 [.033±0.002]

1.05 [.041]

4  5  6

3  2  1

0.9 [.035] REF

0.7±0.05 [.028±0.002]

0.1 [.004] REF

0.9±0.05 [.035±0.002]

0.5±0.05 [.020±0.002]

2.1 [.083]

0.9 [.035]

0.9 [.035]

1 [.039]

| No. | Pin terminal |
|-----|--------------|
| 1 | Enable |
| 2 | nc |
| 3 | GND |
| 4 | Output |
| 5 | nc |
| 6 | VDD |

## 2.5 x 2.0 mm Plastic Package

2.5±0.05 [0.098±0.002]

6  5  4

1  2  3

2.0±0.05 [0.079±0.002]

0.85±0.05 [.033±0.002]

0.825 [.032]

4  5  6

3  2  1

0.9 [.035] REF

0.7±0.10 [0.028±0.004]

0.1 [.004] REF

0.65±0.05 [0.026±0.002]

0.25±0.05 [0.099±0.002]

Recommended
Solder Pad Layout
units: mm[inch]

* Power Supply Decoupling
Capacitor is Required

* Via to Power Layer

Via to GND Layer

6   4

1   3

0.85 [0.033]

0.70 [0.028]

0.65 [0.026]
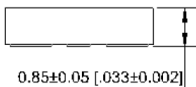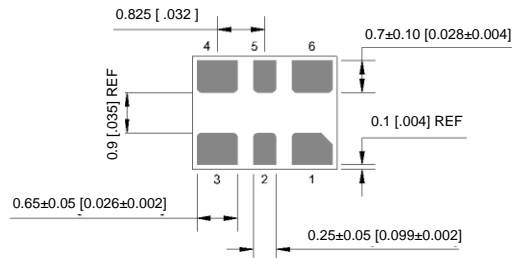
| No. | Pin terminal |
|-----|--------------|
| 1 | Enable |
| 2 | nc |
| 3 | GND |
| 4 | Output |
| 5 | Output̄ |
| 6 | VDD |

**Disclaimer:**

**MICREL, Inc.** ● **2180 Fortune Drive,** **San Jose, California** **95131** ● **USA**
**Phone: +1 (408) 944-0800** ● **Fax: +1 (408) 474-1000** ● **Email: hbwhelp@micrel.com** ● **www.micrel.com**

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