
16-Bit Digital Signal Controllers for Digital Power Applications with Interconnected High-Speed PWM, ADC, PGA and Comparators

Operating Conditions

- 3.0V to 3.6V, -40°C to +85°C, DC to 70 MIPS
- 3.0V to 3.6V, -40°C to +125°C, DC to 60 MIPS

Flash Architecture

- 16 Kbytes-32 Kbytes of Program Flash

Core: 16-Bit dsPIC33E CPU

- Code-Efficient (C and Assembly) Architecture
- Two 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle Mixed-Sign MUL Plus Hardware Divide
- 32-Bit Multiply Support
- Two Additional Working Register Sets (reduces context switching)

Clock Management

- ±0.9% Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer (WDT)
- Fast Wake-up and Start-up

Power Management

- Low-Power Management modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset
- 0.5 mA/MHz Dynamic Current (typical)
- 10 µA IPD Current (typical)

High-Speed PWM

- Three PWM Generators (two outputs per generator)
- Individual Time Base and Duty Cycle for each PWM
- 1.04 ns PWM Resolution (frequency, duty cycle, dead time and phase)
- Supports Center-Aligned, Redundant, Complementary and True Independent Output modes
- Independent Fault and Current-Limit Inputs
- Output Override Control
- PWM Support for:
 - AC/DC, DC/DC, inverters, PFC, lighting

Advanced Analog Features

- High-Speed ADC module:
 - 12-bit with 2 dedicated SAR ADC cores and one shared SAR ADC core
 - Up to 3.25 Msps conversion rate per ADC core @ 12-bit resolution
 - Dedicated result buffer for each analog channel
 - Flexible and independent ADC trigger sources
 - Two digital comparators
 - One oversampling filter
- Two Rail-to-Rail Comparators with Hysteresis:
 - Dedicated 12-bit Digital-to-Analog Converter (DAC) for each analog comparator
- Two Programmable Gain Amplifiers:
 - Single-ended or independent ground reference
 - Five selectable gains (4x, 8x, 16x, 32x and 64x)
 - 40 MHz gain bandwidth

Interconnected SMPS Peripherals

- Reduces CPU Interaction to Improve Performance
- Flexible PWM Trigger Options for ADC Conversions
- High-Speed Comparator Truncates PWM (15 ns typical):
 - Supports Cycle-by-Cycle Current mode control
 - Current Reset mode (variable frequency)

Timers/Output Compare/Input Capture

- Three 16-Bit and One 32-Bit Timers/Counters
- One Output Compare (OC) module, Configurable as Timers/Counters
- One Input Capture (IC) module

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Communication Interfaces

- One UART module (15 Mbps):
 - Supports LIN/J2602 protocols and IrDA®
- One 4-Wire SPI module (15 Mbps)
- One I²C module (up to 1 Mbaud) with SMBus Support

Input/Output

- Sink/Source up to 12mA/15mA, respectively; Pin-Specific for Standard VOH/VOL
- 5V Tolerant Pins
- Selectable Open-Drain, Pull-ups and Pull-Downs
- External Interrupts on All I/O Pins
- Peripheral Pin Select (PPS) to allow Function Remap with Six Virtual I/Os

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1, -40°C to +125°C)
- Class B Safety Library, IEC 60730
- 4x4x0.6 mm and 6x6x0.5 mm UQFN Packages are Designed and Optimized to ease IPC9592B 2nd Level Temperature Cycle Qualification

Debugger Development Support

- In-Circuit and In-Application Programming
- Three Program and One Complex Data Breakpoint
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

TABLE 1: dsPIC33EPXXGS202 FAMILY DEVICES

| Device | Pins | Program Memory Bytes | RAM Bytes | Timers ⁽¹⁾ | Remappable Peripherals | | | | | PWM | ADC Inputs | I ² C | ADC Cores | PGA | Analog Comparator | General Purpose I/O (GPIO) | Packages |
|------------------|------|----------------------|-----------|-----------------------|------------------------|----------------|------|-----|------------------------------------|-----|------------|------------------|-----------|-----|-------------------|----------------------------|---|
| | | | | | Input Capture | Output Compare | UART | SPI | External Interrupts ⁽²⁾ | | | | | | | | |
| dsPIC33EP16GS202 | 28 | 16K | 2K | 3 | 1 | 1 | 1 | 1 | 3 | 3x2 | 12 | 1 | 3 | 2 | 2 | 21 | SSOP, SOIC, QFN-S, UQFN (4x4 mm), UQFN (6x6 mm) |
| dsPIC33EP32GS202 | 28 | 32K | 2K | 3 | 1 | 1 | 1 | 1 | 3 | 3x2 | 12 | 1 | 3 | 2 | 2 | 21 | |

Note 1: The external clock for Timer1, Timer2 and Timer3 is remappable.

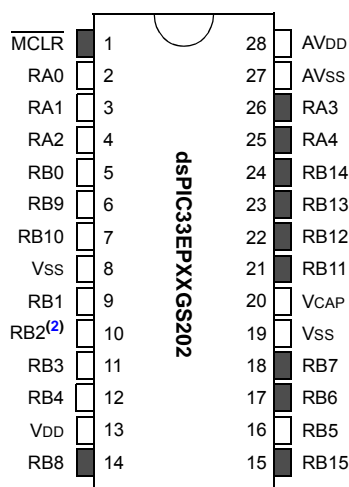
Note 2: INT0 is not remappable; INT1 and INT2 are remappable.

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Pin Diagrams

28-Pin SOIC,
28-Pin SSOP

■ = Pins are up to 5V tolerant



PIN FUNCTION DESCRIPTIONS

| Pin | Pin Function | Pin | Pin Function |
|-----|--|-----|------------------------------|
| 1 | MCLR | 15 | PGEC3/RP47/RB15 |
| 2 | AN0/PGA1P1/CMP1A/RA0 | 16 | TDO/AN9/PGA2N2/RP37/RB5 |
| 3 | AN1/PGA1P2/PGA2P1/CMP1B/RA1 | 17 | PGED1/TDI/AN10/SCL1/RP38/RB6 |
| 4 | AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2 | 18 | PGEC1/AN11/SDA1/RP39/RB7 |
| 5 | AN3/PGA2P3/CMP1D/CMP2B/RP32/RB0 | 19 | Vss |
| 6 | AN4/CMP2C/RP41/RB9 | 20 | VCAP |
| 7 | AN5/CMP2D/RP42/RB10 | 21 | TMS/PWM3H/RP43/RB11 |
| 8 | Vss | 22 | TCK/PWM3L/RP44/RB12 |
| 9 | OSC1/CLKI/AN6/RP33/RB1 | 23 | PWM2H/RP45/RB13 |
| 10 | OSC2/CLKO/AN7/PGA1N2/RP34/RB2 ⁽²⁾ | 24 | PWM2L/RP46/RB14 |
| 11 | PGED2/AN8/INT0/RP35/RB3 | 25 | PWM1H/RA4 |
| 12 | PGEC2/ADTRG31/RP36/RB4 | 26 | PWM1L/RA3 |
| 13 | VDD | 27 | AVSS |
| 14 | PGED3/FLT31/RP40/RB8 | 28 | AVDD |

Legend: Shaded pins are up to 5 VDC tolerant.

Note 1: RPn represents remappable peripheral functions. See [Table 10-1](#) and [Table 10-2](#) for the complete list of remappable sources.

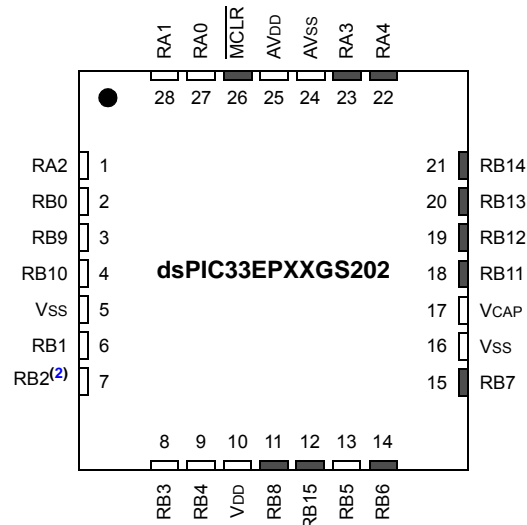
2: At device power-up, a pulse with an amplitude around 2V and a duration greater than 500 μ s, may be observed on this device pin, independent of pull-down resistors. It is recommended not to use this pin as an output driver unless the circuit being driven can endure this active duration.

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Pin Diagrams (Continued)

28-Pin UQFN, 28-Pin UQFN,
28-Pin QFN-S

■ = Pins are up to 5V tolerant



PIN FUNCTION DESCRIPTIONS

| Pin | Pin Function | Pin | Pin Function |
|-----|--|-----|-----------------------------|
| 1 | AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2 | 15 | PGEC1/AN11/SDA1/RP39/RB7 |
| 2 | AN3/PGA2P3/CMP1D/ CMP28/RP32/RB0 | 16 | Vss |
| 3 | AN4/CMP2C/RP41/RB9 | 17 | VCAP |
| 4 | AN5/CMP2D/RP42/RB10 | 18 | TMS/PWM3H/RP43/RB11 |
| 5 | Vss | 19 | TCK/PWM3L/RP44/RB12 |
| 6 | OSC1/CLKI/AN6/RP33/RB1 | 20 | PWM2H/RP45/RB13 |
| 7 | OSC2/CLKO/AN7/PGA1N2/RP34/RB2 ⁽²⁾ | 21 | PWM2L/RP46/RB14 |
| 8 | PGED2/AN8/INT0/RP35/RB3 | 22 | PWM1H/RA4 |
| 9 | PGEC2/ADTRG31/RP36/RB4 | 23 | PWM1L/RA3 |
| 10 | VDD | 24 | AVss |
| 11 | PGED3/FLT31/RP40/RB8 | 25 | AVDD |
| 12 | PGEC3/RP47/RB15 | 26 | MCLR |
| 13 | TDO/AN9/PGA2N2/RP37/RB5 | 27 | AN0/PGA1P1/CMP1A/RA0 |
| 14 | PGED1/TDI/AN10/SCL1/RP38/RB6 | 28 | AN1/PGA1P2/PGA2P1/CMP1B/RA1 |

Legend: Shaded pins are up to 5 VDC tolerant.

Note 1: RPn represents remappable peripheral functions. See [Table 10-1](#) and [Table 10-2](#) for the complete list of remappable sources.

2: At device power-up, a pulse with an amplitude around 2V and a duration greater than 500 μ s, may be observed on this device pin, independent of pull-down resistors. It is recommended not to use this pin as an output driver unless the circuit being driven can endure this active duration.

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

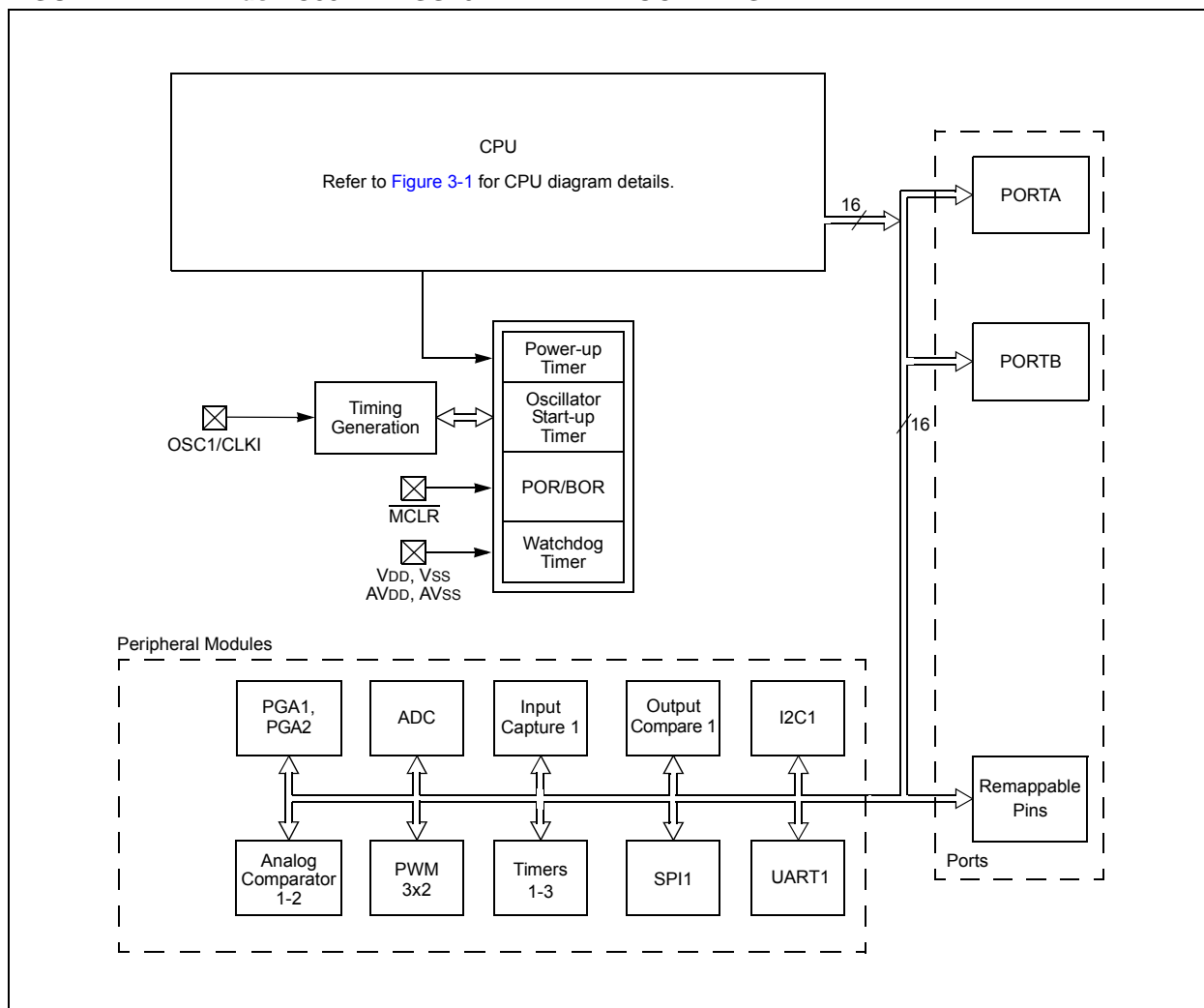
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXGS202 Digital Signal Controller (DSC) devices.

The dsPIC33EPXXGS202 devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EPXXGS202 FAMILY BLOCK DIAGRAM



dsPIC33EPXXGS202 FAMILY

TABLE 1-1: PINOUT I/O DESCRIPTIONS

| Pin Name | Pin Type | Buffer Type | PPS | Description |
|----------------|----------|-------------|-----|--|
| AN0-AN11 | I | Analog | No | Analog input channels. |
| CLKI | I | ST/ CMOS | No | External clock source input. Always associated with OSC1 pin function. |
| CLKO | O | — | No | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function. |
| OSC1 | I | ST/ CMOS | No | Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. |
| OSC2 | I/O | — | No | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. |
| IC1 | I | ST | Yes | Capture Input 1. |
| OCFA | I | ST | Yes | Compare Fault A input (for compare channels). |
| OC1 | O | — | Yes | Compare Output 1. |
| INT0 | I | ST | No | External Interrupt 0. |
| INT1 | I | ST | Yes | External Interrupt 1. |
| INT2 | I | ST | Yes | External Interrupt 2. |
| RA0-RA4 | I/O | ST | No | PORTA is a bidirectional I/O port. |
| RB0-RB15 | I/O | ST | No | PORTB is a bidirectional I/O port. |
| T1CK | I | ST | Yes | Timer1 external clock input. |
| T2CK | I | ST | Yes | Timer2 external clock input. |
| T3CK | I | ST | Yes | Timer3 external clock input. |
| U1CTS | I | ST | Yes | UART1 Clear-to-Send. |
| U1RTS | O | — | Yes | UART1 Request-to-Send. |
| U1RX | I | ST | Yes | UART1 receive. |
| U1TX | O | — | Yes | UART1 transmit. |
| BCLK1 | O | ST | Yes | UART1 IrDA® baud clock output. |
| SCK1 | I/O | ST | Yes | Synchronous serial clock input/output for SPI1. |
| SDI1 | I | ST | Yes | SPI1 data in. |
| SDO1 | O | — | Yes | SPI1 data out. |
| SS1 | I/O | ST | Yes | SPI1 slave synchronization or frame pulse I/O. |
| SCL1 | I/O | ST | No | Synchronous serial clock input/output for I2C1. |
| SDA1 | I/O | ST | No | Synchronous serial data input/output for I2C1. |
| TMS | I | ST | No | JTAG Test mode select pin. |
| TCK | I | ST | No | JTAG test clock input pin. |
| TDI | I | ST | No | JTAG test data input pin. |
| TDO | O | — | No | JTAG test data output pin. |
| FLT1-FLT8 | I | ST | Yes | PWM Fault Inputs 1 through 8. |
| FLT31 | I | ST | No | PWM Fault Input 31. |
| PWM1L-PWM3L | O | — | No | PWM Low Outputs 1 through 3. |
| PWM1H-PWM3H | O | — | No | PWM High Outputs 1 through 3. |
| SYNCI1, SYNCI2 | I | ST | Yes | PWM Synchronization Inputs 1 and 2. |
| SYNCO1, SYNCO2 | O | — | Yes | PWM Synchronization Outputs 1 and 2. |
| CMP1A-CMP2A | I | Analog | No | Comparator Channels 1A through 2A inputs. |
| CMP1B-CMP2B | I | Analog | No | Comparator Channels 1B through 2B inputs. |
| CMP1C-CMP2C | I | Analog | No | Comparator Channels 1C through 2C inputs. |
| CMP1D-CMP2D | I | Analog | No | Comparator Channels 1D through 2D inputs. |

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
 ST = Schmitt Trigger input with CMOS levels O = Output I = Input
 PPS = Peripheral Pin Select TTL = TTL input buffer

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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

| Pin Name | Pin Type | Buffer Type | PPS | Description |
|---------------|----------|-------------|-----|---|
| PGA1P1-PGA1P3 | I | Analog | No | PGA1 Positive Inputs 1 through 3. |
| PGA1N2 | I | Analog | No | PGA1 Negative Input 2. |
| PGA2P1-PGA2P3 | I | Analog | No | PGA2 Positive Inputs 1 through 3. |
| PGA2N2 | I | Analog | No | PGA2 Negative Input 2. |
| ADTRG31 | I | ST | No | External ADC trigger source. |
| PGED1 | I/O | ST | No | Data I/O pin for Programming/Debugging Communication Channel 1. |
| PGEC1 | I | ST | No | Clock input pin for Programming/Debugging Communication Channel 1. |
| PGED2 | I/O | ST | No | Data I/O pin for Programming/Debugging Communication Channel 2. |
| PGEC2 | I | ST | No | Clock input pin for Programming/Debugging Communication Channel 2. |
| PGED3 | I/O | ST | No | Data I/O pin for Programming/Debugging Communication Channel 3. |
| PGEC3 | I | ST | No | Clock input pin for Programming/Debugging Communication Channel 3. |
| MCLR | I/P | ST | No | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| AVDD | P | P | No | Positive supply for analog modules. This pin must be connected at all times. |
| AVSS | P | P | No | Ground reference for analog modules. This pin must be connected at all times. |
| VDD | P | — | No | Positive supply for peripheral logic and I/O pins. |
| VCAP | P | — | No | CPU logic filter capacitor connection. |
| VSS | P | — | No | Ground reference for logic and I/O pins. |

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
 ST = Schmitt Trigger input with CMOS levels O = Output I = Input
 PPS = Peripheral Pin Select TTL = TTL input buffer

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NOTES:

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXGS202 family requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names which must always be connected:

- All VDD and VSS pins (see [Section 2.2 “Decoupling Capacitors”](#))
- All AVDD and AVSS pins regardless if ADC module is not used (see [Section 2.2 “Decoupling Capacitors”](#))
- VCAP (see [Section 2.3 “CPU Logic Filter Capacitor Connection \(VCAP\)”](#))
- MCLR pin (see [Section 2.4 “Master Clear \(MCLR\) Pin”](#))
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see [Section 2.5 “ICSP Pins”](#))
- OSC1 and OSC2 pins when external oscillator source is used (see [Section 2.6 “External Oscillator Pins”](#))

2.2 Decoupling Capacitors

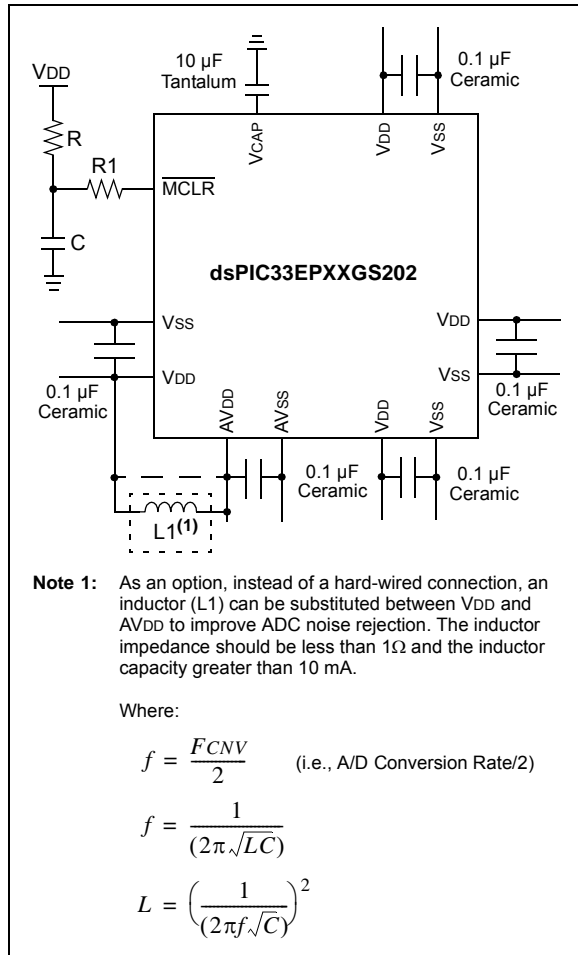
The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 μF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

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FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (<1 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor greater than 4.7 µF (10 µF is recommended), 16V connected to ground. The type can be ceramic or tantalum. See [Section 25.0 “Electrical Characteristics”](#) for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See [Section 22.4 “On-Chip Voltage Regulator”](#) for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

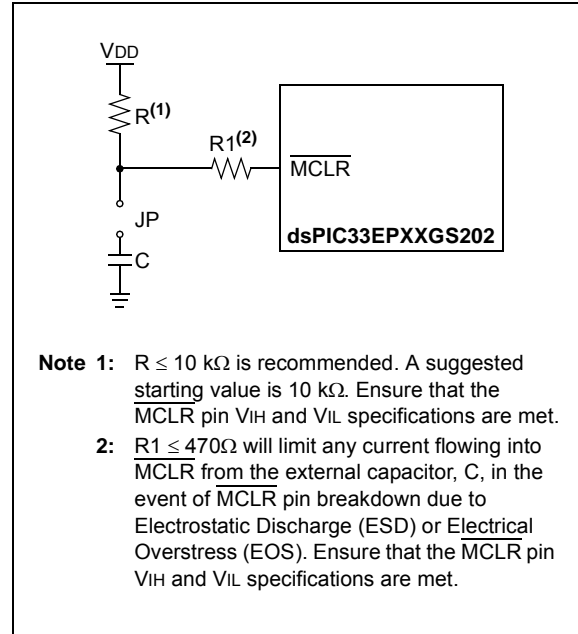
- Device Reset
- Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in [Figure 2-2](#), it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in [Figure 2-2](#) within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



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2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (VIH) and Voltage Input Low (VIL) requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICKit™ 3, MPLAB ICD 3 or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, MPLAB ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

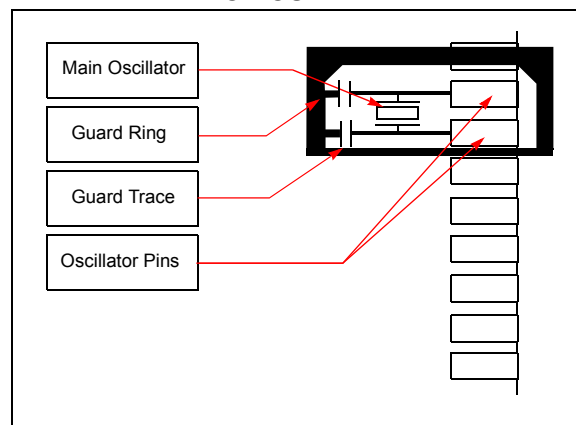
- “Using MPLAB® ICD 3” (poster) DS51765
- “Multi-Tool Design Advisory” DS51764
- “MPLAB® REAL ICE™ In-Circuit Emulator User’s Guide” DS51616
- “Using MPLAB® REAL ICE™ In-Circuit Emulator” (poster) DS51749

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For details, see **Section 8.0 “Oscillator Configuration”** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in [Figure 2-3](#).

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



dsPIC33EPXXGS202 FAMILY

2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to $3 \text{ MHz} < F_{IN} < 5.5 \text{ MHz}$ to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLDBF to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic-low state.

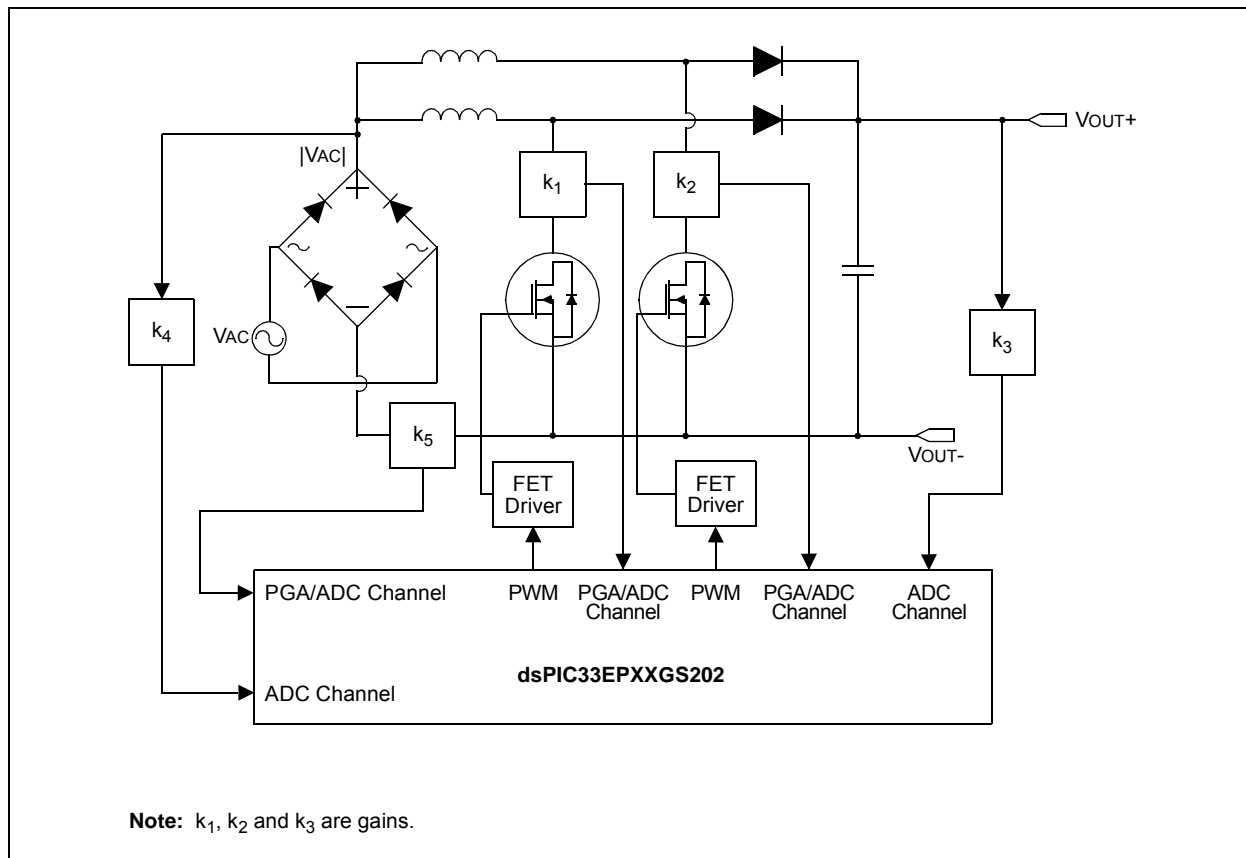
Alternatively, connect a 1k to 10k resistor between V_{SS} and unused pins and drive the output to logic low.

2.9 Targeted Applications

- Power Factor Correction (PFC):
 - Interleaved PFC
 - Critical Conduction PFC
 - Bridgeless PFC
- DC/DC Converters:
 - Buck, Boost, Forward, Flyback, Push-Pull
 - Half/Full-Bridge
 - Phase-Shift Full-Bridge
 - Resonant Converters
- DC/AC:
 - Half/Full-Bridge Inverter
 - Resonant Inverter

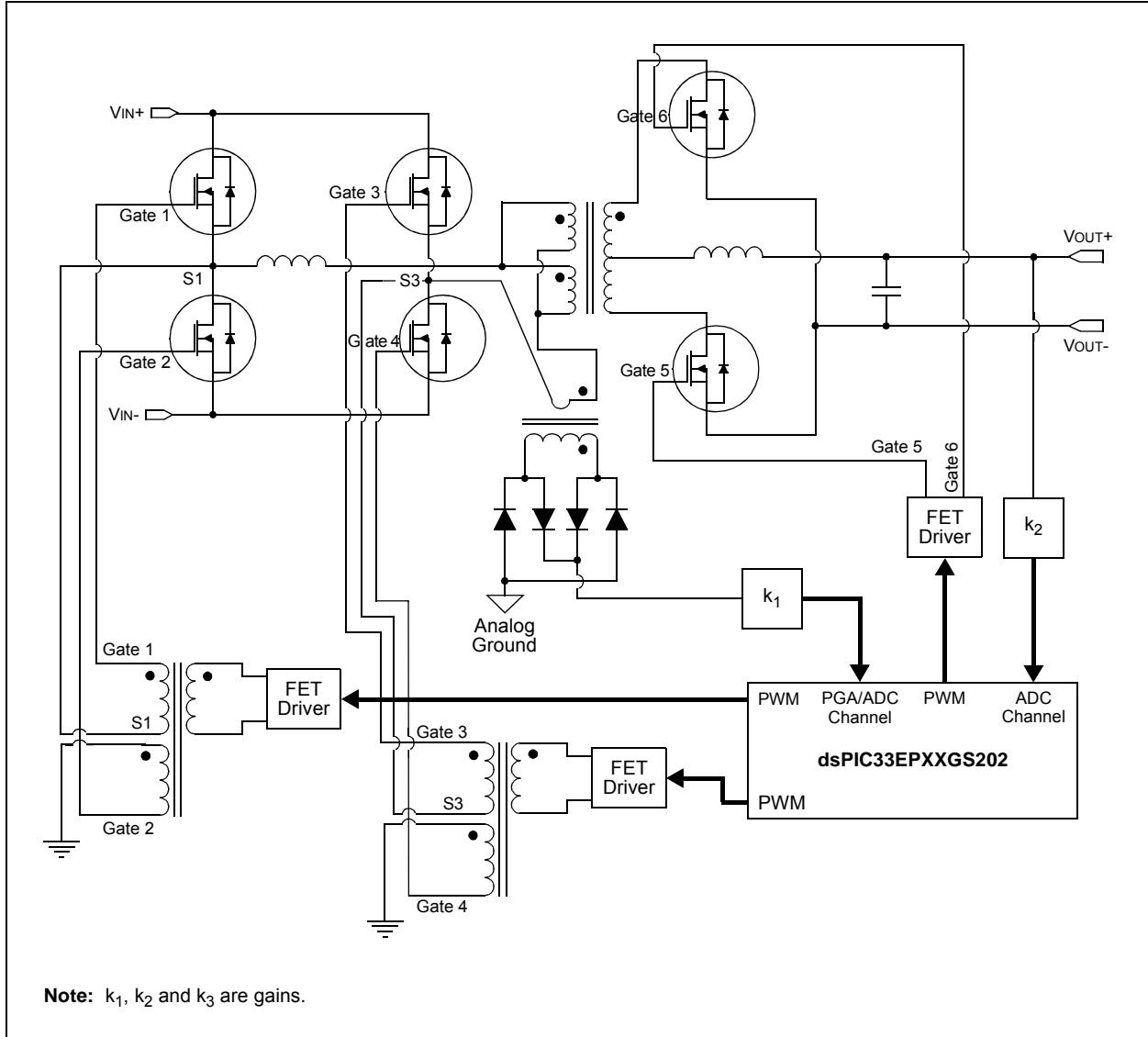
Examples of typical application connections are shown in [Figure 2-4](#) through [Figure 2-6](#).

FIGURE 2-4: INTERLEAVED PFC



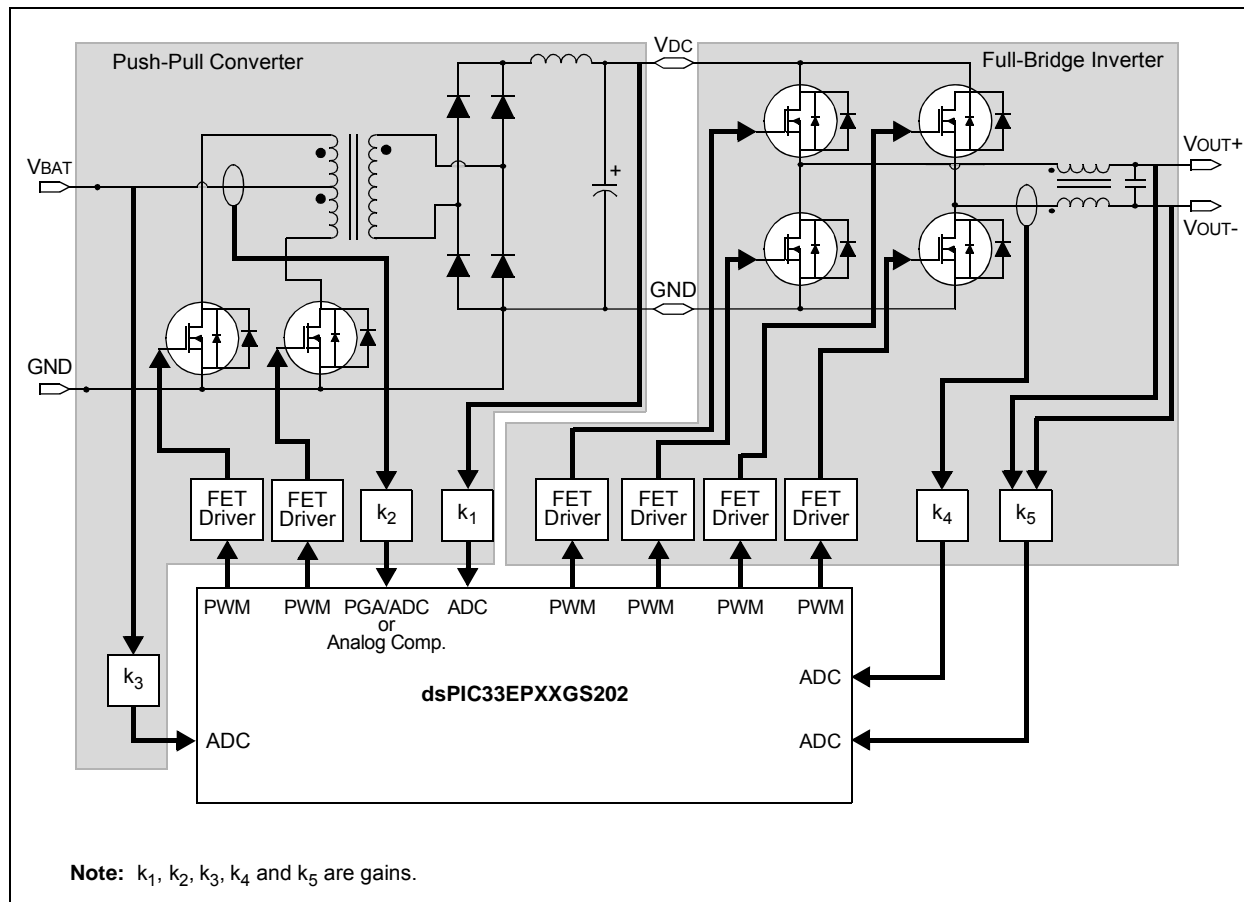
dsPIC33EPXXGS202 FAMILY

FIGURE 2-5: PHASE-SHIFTED FULL-BRIDGE CONVERTER



dsPIC33EPXXGS202 FAMILY

FIGURE 2-6: OFF-LINE UPS



3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**CPU**” (DS70359) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for Digital Signal Processing (DSP). The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EPXXGS202 devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a data, address or address offset register. The 16th Working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

In addition, the dsPIC33EPXXGS202 devices include two Alternate Working register sets which consist of W0 through W14. The Alternate registers can be made persistent to help reduce the saving and restoring of register content during Interrupt Service Routines (ISRs). The Alternate Working registers can be assigned to a specific Interrupt Priority Level (IPL1 through IPL6) by configuring the CTXTx<2:0> bits in the FALTREG Configuration register. The Alternate Working registers can also be accessed manually by using the CTXTSWP instruction. The CCTXI<2:0> and MCTXI<2:0> bits in the CTXTSTAT register can be used to identify the current and most recent, manually selected Working register sets.

3.2 Instruction Set

The instruction set for dsPIC33EPXXGS202 devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The base Data Space (DS) can be addressed as 1K word or 2 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Space boundary is device-specific.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 16K program word boundary. The program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Refer to “**Data Memory**” (DS70595) in the “*dsPIC33/PIC24 Family Reference Manual*” for more details on PSV and table accesses.

On dsPIC33EPXXGS202 devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms.

3.4 Addressing Modes

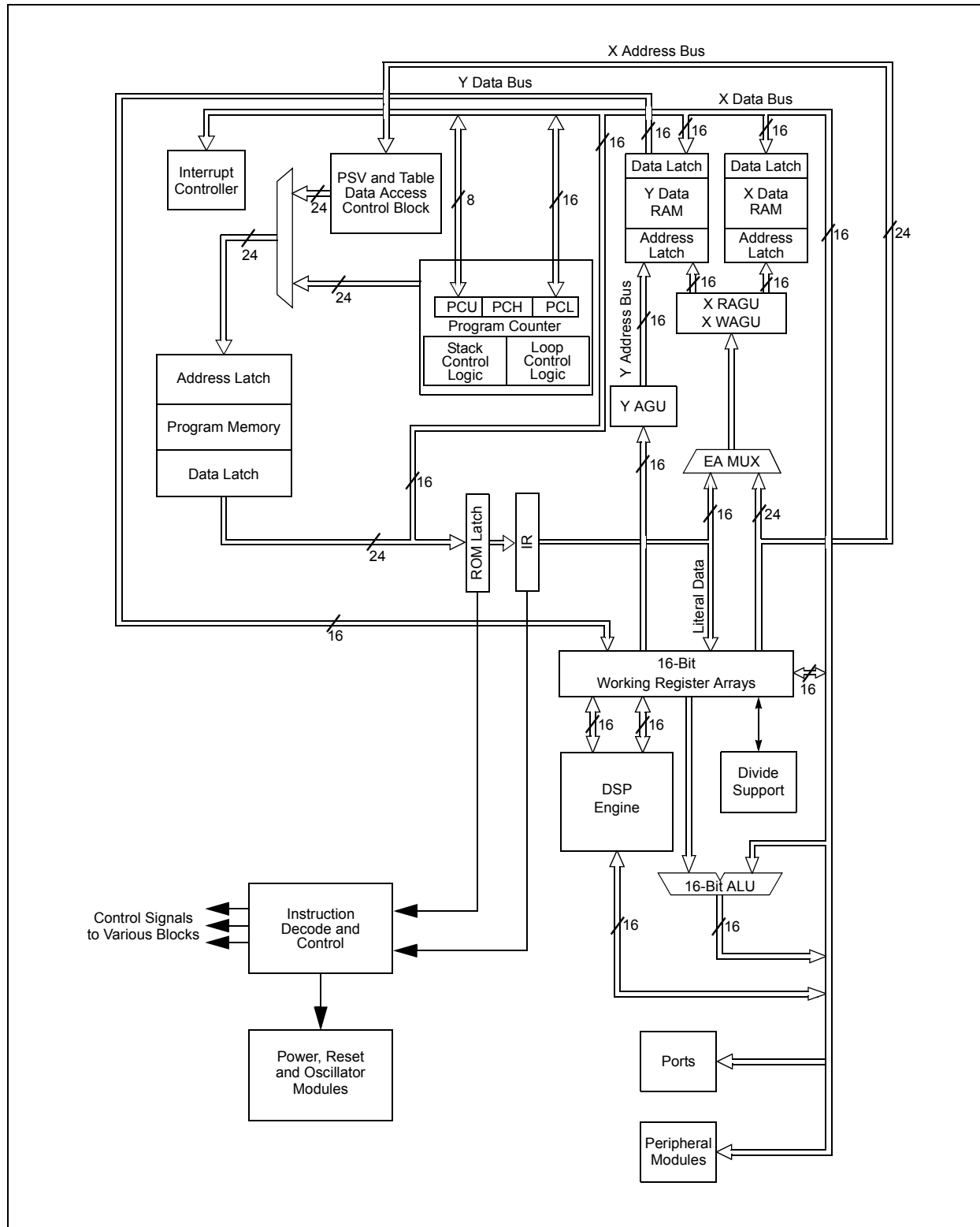
The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

dsPIC33EPXXGS202 FAMILY

FIGURE 3-1: dsPIC33EPXXGS202 CPU BLOCK DIAGRAM



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3.5 Programmer's Model

The programmer's model for the dsPIC33EPXXGS202 family is shown in [Figure 3-2](#). All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. [Table 3-1](#) lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXGS202 devices contain control registers for Modulo Addressing, Bit-Reversed Addressing and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in [Table 3-1](#).

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

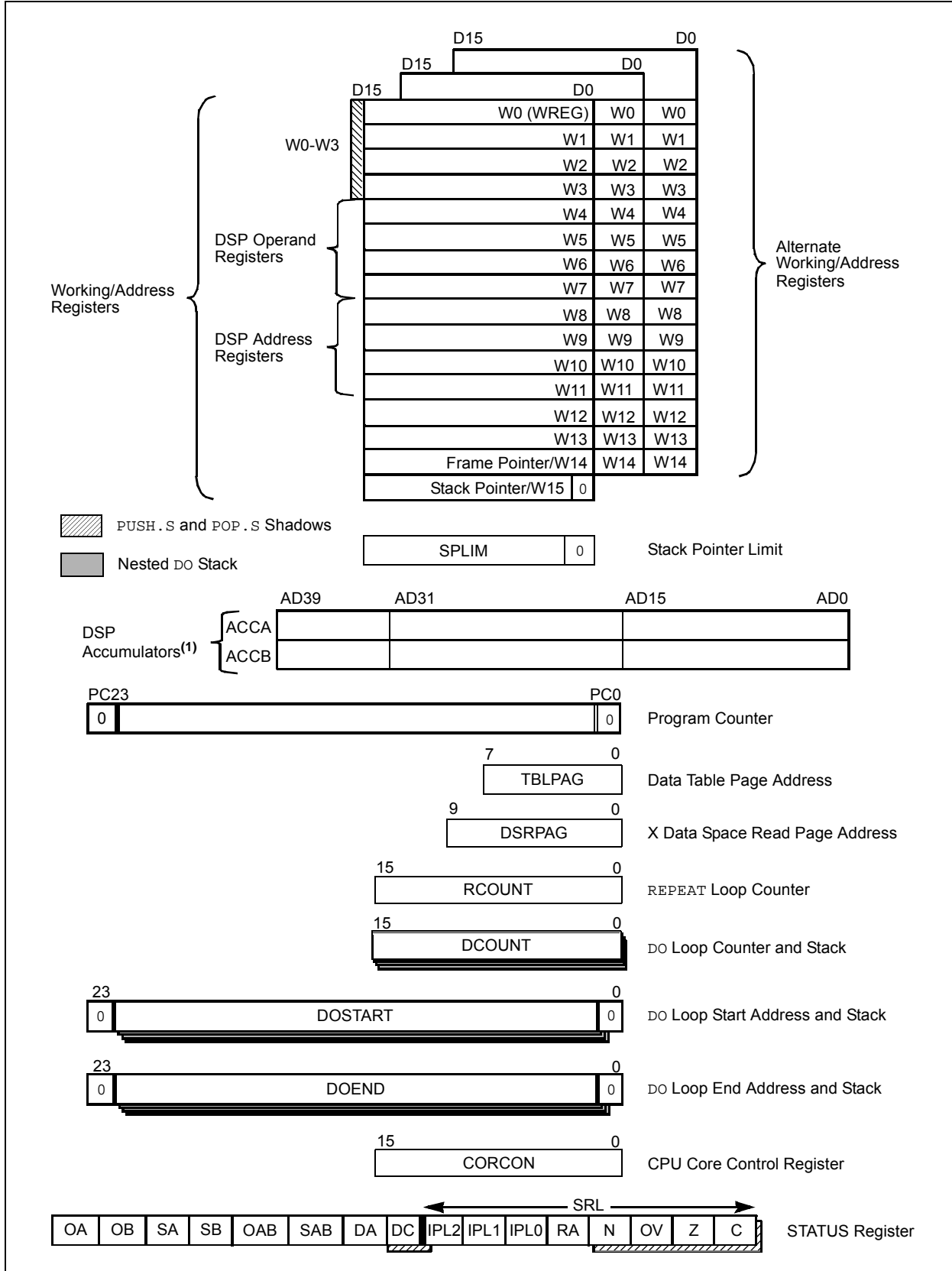
| Register(s) Name | Description |
|---|---|
| W0 through W15 ⁽¹⁾ | Working Register Array |
| W0 through W14 ⁽¹⁾ | Alternate Working Register Array 1 |
| W0 through W14 ⁽¹⁾ | Alternate Working Register Array 2 |
| ACCA, ACCB | 40-Bit DSP Accumulators |
| PC | 23-Bit Program Counter |
| SR | ALU and DSP Engine STATUS Register |
| SPLIM | Stack Pointer Limit Value Register |
| TBLPAG | Table Memory Page Address Register |
| DSRPAG | Extended Data Space (EDS) Read Page Register |
| RCOUNT | REPEAT Loop Counter Register |
| DCOUNT | DO Loop Counter Register |
| DOSTARTH ⁽²⁾ , DOSTARTL ⁽²⁾ | DO Loop Start Address Register (High and Low) |
| DOENDH, DOENDL | DO Loop End Address Register (High and Low) |
| CORCON | Contains DSP Engine, DO Loop Control and Trap Status bits |

Note 1: Memory-mapped W0 through W14 represent the value of the register in the currently active CPU context.

2: The DOSTARTH and DOSTARTL registers are read-only.

dsPIC33EPXXGS202 FAMILY

FIGURE 3-2: PROGRAMMER'S MODEL



3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

3.6.1 KEY RESOURCES

- “**CPU**” (DS70359) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

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3.7 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

| | | | | | | | |
|--------|-------|-------------------|-------------------|-------|-------|-----|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/C-0 | R/C-0 | R-0 | R/W-0 |
| OA | OB | SA ⁽³⁾ | SB ⁽³⁾ | OAB | SAB | DA | DC |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|----------------------|----------------------|----------------------|-----|-------|-------|-------|-------|
| R/W-0 ⁽²⁾ | R/W-0 ⁽²⁾ | R/W-0 ⁽²⁾ | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| IPL2 ⁽¹⁾ | IPL1 ⁽¹⁾ | IPL0 ⁽¹⁾ | RA | N | OV | Z | C |
| bit 7 | | | | | | | bit 0 |

| | | |
|-------------------|-------------------|------------------------------------|
| Legend: | C = Clearable bit | U = Unimplemented bit, read as '0' |
| R = Readable bit | W = Writable bit | '0' = Bit is cleared |
| -n = Value at POR | '1' = Bit is set | x = Bit is unknown |

- bit 15 **OA:** Accumulator A Overflow Status bit
 1 = Accumulator A has overflowed
 0 = Accumulator A has not overflowed
- bit 14 **OB:** Accumulator B Overflow Status bit
 1 = Accumulator B has overflowed
 0 = Accumulator B has not overflowed
- bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit⁽³⁾
 1 = Accumulator A is saturated or has been saturated at some time
 0 = Accumulator A is not saturated
- bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit⁽³⁾
 1 = Accumulator B is saturated or has been saturated at some time
 0 = Accumulator B is not saturated
- bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit
 1 = Accumulators A or B have overflowed
 0 = Neither Accumulators A or B have overflowed
- bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit
 1 = Accumulators A or B are saturated, or have been saturated at some time
 0 = Neither Accumulator A or B are saturated
- bit 9 **DA:** DO Loop Active bit
 1 = DO loop in progress
 0 = DO loop not in progress
- bit 8 **DC:** MCU ALU Half Carry/Borrow bit
 1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
 0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

- Note 1:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- 2:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- 3:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

dsPIC33EPXXGS202 FAMILY

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

| | |
|---------|---|
| bit 7-5 | IPL<2:0> : CPU Interrupt Priority Level Status bits ^(1,2) 111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8) |
| bit 4 | RA : REPEAT Loop Active bit 1 = REPEAT loop is in progress 0 = REPEAT loop is not in progress |
| bit 3 | N : MCU ALU Negative bit 1 = Result was negative 0 = Result was non-negative (zero or positive) |
| bit 2 | OV : MCU ALU Overflow bit This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred |
| bit 1 | Z : MCU ALU Zero bit 1 = An operation that affects the Z bit has set it at some time in the past 0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result) |
| bit 0 | C : MCU ALU Carry/Borrow bit 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred |

- Note 1:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- 2:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- 3:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

dsPIC33EPXXGS202 FAMILY

REGISTER 3-2: CORCON: CORE CONTROL REGISTER

| | | | | | | | |
|--------|-----|-------|-------|--------------------|-----|-----|-------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
| VAR | — | US1 | US0 | EDT ⁽¹⁾ | DL2 | DL1 | DL0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-------|-------|--------|---------------------|-----|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R-0 | R/W-0 | R/W-0 |
| SATA | SATB | SATDW | ACCSAT | IPL3 ⁽²⁾ | SFA | RND | IF |
| bit 7 | | | | | | | bit 0 |

| | |
|-------------------|------------------------------------|
| Legend: | C = Clearable bit |
| R = Readable bit | W = Writable bit |
| -n = Value at POR | '1' = Bit is set |
| | U = Unimplemented bit, read as '0' |
| | '0' = Bit is cleared |
| | x = Bit is unknown |

- bit 15 **VAR:** Variable Exception Processing Latency Control bit
 1 = Variable exception processing latency
 0 = Fixed exception processing latency
- bit 14 **Unimplemented:** Read as '0'
- bit 13-12 **US<1:0>:** DSP Multiply Unsigned/Signed Control bits
 11 = Reserved
 10 = DSP engine multiplies are mixed-sign
 01 = DSP engine multiplies are unsigned
 00 = DSP engine multiplies are signed
- bit 11 **EDT:** Early DO Loop Termination Control bit⁽¹⁾
 1 = Terminates executing DO loop at the end of current loop iteration
 0 = No effect
- bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits
 111 = 7 DO loops are active
 •
 •
 •
 001 = 1 DO loop is active
 000 = 0 DO loops are active
- bit 7 **SATA:** ACCA Saturation Enable bit
 1 = Accumulator A saturation is enabled
 0 = Accumulator A saturation is disabled
- bit 6 **SATB:** ACCB Saturation Enable bit
 1 = Accumulator B saturation is enabled
 0 = Accumulator B saturation is disabled
- bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit
 1 = Data Space write saturation is enabled
 0 = Data Space write saturation is disabled
- bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit
 1 = 9.31 saturation (super saturation)
 0 = 1.31 saturation (normal saturation)
- bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3⁽²⁾
 1 = CPU Interrupt Priority Level is greater than 7
 0 = CPU Interrupt Priority Level is 7 or less

- Note 1:** This bit is always read as '0'.
- Note 2:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

dsPIC33EPXXGS202 FAMILY

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

- bit 2 **SFA:** Stack Frame Active Status bit
 1 = Stack frame is active; W14 and W15 address of 0x0000 to 0xFFFF, regardless of DSRPAG
 0 = Stack frame is not active; W14 and W15 address of Base Data Space
- bit 1 **RND:** Rounding Mode Select bit
 1 = Biased (conventional) rounding is enabled
 0 = Unbiased (convergent) rounding is enabled
- bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit
 1 = Integer mode is enabled for DSP multiply
 0 = Fractional mode is enabled for DSP multiply

Note 1: This bit is always read as '0'.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 3-3: CTXTSTAT: CPU W REGISTER CONTEXT STATUS REGISTER

| | | | | | | | |
|--------|-----|-----|-----|-----|--------|--------|--------|
| U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| — | — | — | — | — | CCTXI2 | CCTXI1 | CCTXI0 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-----|-----|-----|-----|--------|--------|--------|
| U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| — | — | — | — | — | MCTXI2 | MCTXI1 | MCTXI0 |
| bit 7 | | | | | | bit 0 | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **CCTXI<2:0>:** Current (W Register) Context Identifier bits

111 = Reserved

-
-
-

011 = Reserved

010 = Alternate Working Register Set 2 is currently in use

001 = Alternate Working Register Set 1 is currently in use

000 = Default register set is currently in use

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **MCTXI<2:0>:** Manual (W Register) Context Identifier bits

111 = Reserved

-
-
-

011 = Reserved

010 = Alternate Working Register Set 2 was most recently manually selected

001 = Alternate Working Register Set 1 was most recently manually selected

000 = Default register set was most recently manually selected

dsPIC33EPXXGS202 FAMILY

3.8 Arithmetic Logic Unit (ALU)

The dsPIC33EPXXGS202 family ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the “16-Bit MCU and DSC Programmer's Reference Manual” (DS70000157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.8.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed, or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.8.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. Sixteen-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.9 DSP Engine

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtractor (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or Integer DSP Multiply (IF)
- Signed, unsigned or mixed-sign DSP multiply (USx)
- Conventional or Convergent Rounding (RND)
- Automatic Saturation On/Off for ACCA (SATA)
- Automatic Saturation On/Off for ACCB (SATB)
- Automatic Saturation On/Off for Writes to Data Memory (SATDW)
- Accumulator Saturation mode Selection (ACCSAT)

TABLE 3-2: DSP INSTRUCTIONS SUMMARY

| Instruction | Algebraic Operation | ACC Write Back |
|-------------|-----------------------|----------------|
| CLR | $A = 0$ | Yes |
| ED | $A = (x - y)^2$ | No |
| EDAC | $A = A + (x - y)^2$ | No |
| MAC | $A = A + (x \cdot y)$ | Yes |
| MAC | $A = A + x^2$ | No |
| MOVSAC | No change in A | Yes |
| MPY | $A = x \cdot y$ | No |
| MPY | $A = x^2$ | No |
| MPY.N | $A = -x \cdot y$ | No |
| MSC | $A = A - x \cdot y$ | Yes |

dsPIC33EPXXGS202 FAMILY

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**dsPIC33E/PIC24E Program Memory**” (DS70000613) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXGS202 family architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

4.1 Program Address Space

The program address memory space of the dsPIC33EPXXGS202 family devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in [Section 4.9 “Interfacing Program and Data Memory Spaces”](#).

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFFFF). The exception is the use of TBLRD operations, which use TBLPAG to permit access to calibration data and Device ID sections of the configuration memory space.

The program memory maps for the dsPIC33EP16/32GS202 devices are shown in [Figure 4-1](#) and [Figure 4-2](#).

4.2 Unique Device Identifier (UDID)

All dsPIC33EPXXGS202 family devices are individually encoded during final manufacturing with a Unique Device Identifier or UDID. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a requirement. It may also be used by the application manufacturer for any number of things that may require unique identification, such as:

- Tracking the device
- Unique serial number
- Unique security key

The UDID comprises five 24-bit program words. When taken together, these fields form a unique 120-bit identifier.

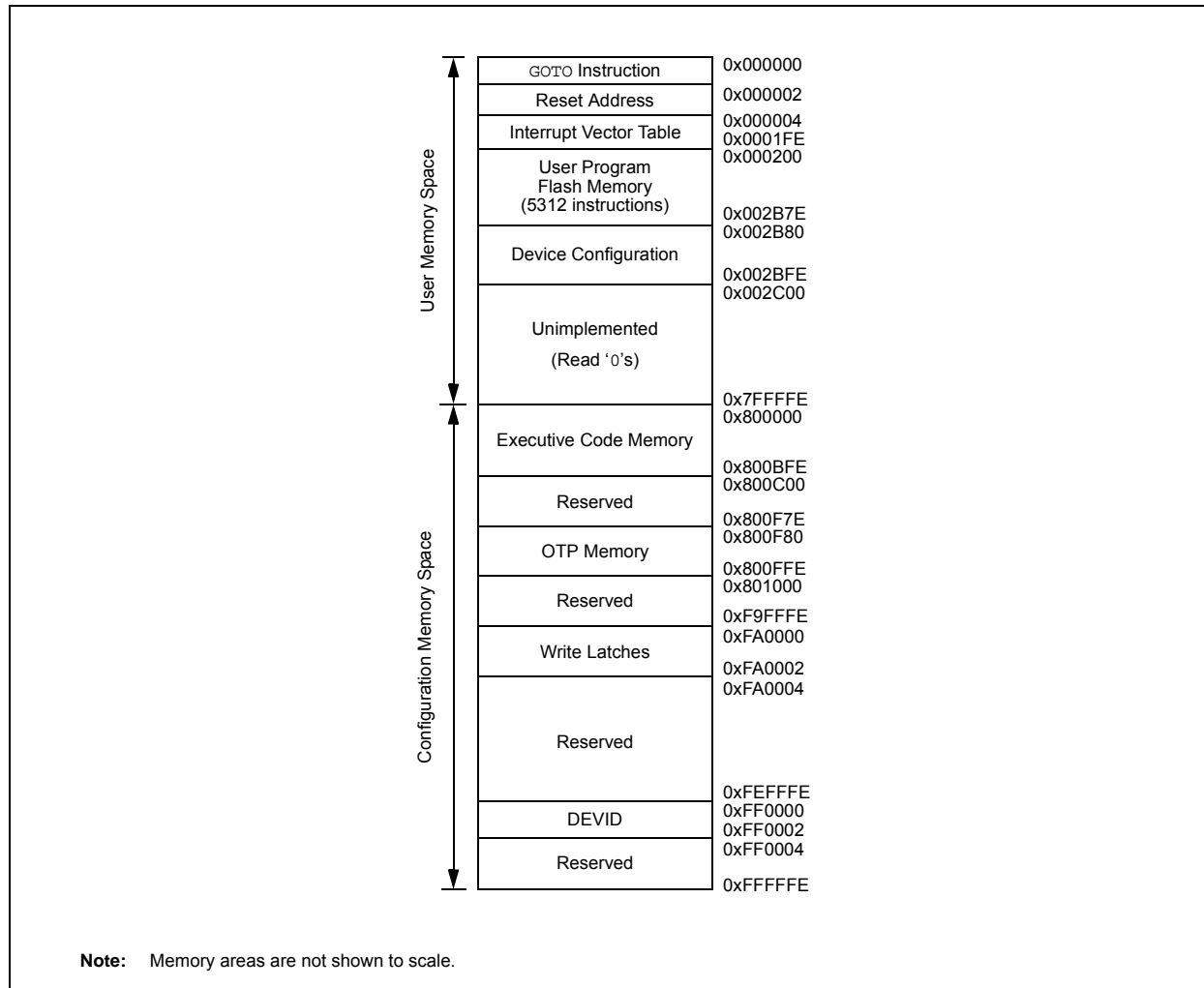
The UDID is stored in five read-only locations, located between 800F00h and 800F08h in the device configuration space. [Table 4-1](#) lists the addresses of the Identifier Words and shows their contents.

TABLE 4-1: UDID ADDRESSES

| Name | Address | Bits 23:16 | Bits 15:8 | Bits 7:0 |
|-------|---------|-------------|-----------|----------|
| UDID1 | 800F00 | UDID Word 1 | | |
| UDID2 | 800F02 | UDID Word 2 | | |
| UDID3 | 800F04 | UDID Word 3 | | |
| UDID4 | 800F06 | UDID Word 4 | | |
| UDID5 | 800F08 | UDID Word 5 | | |

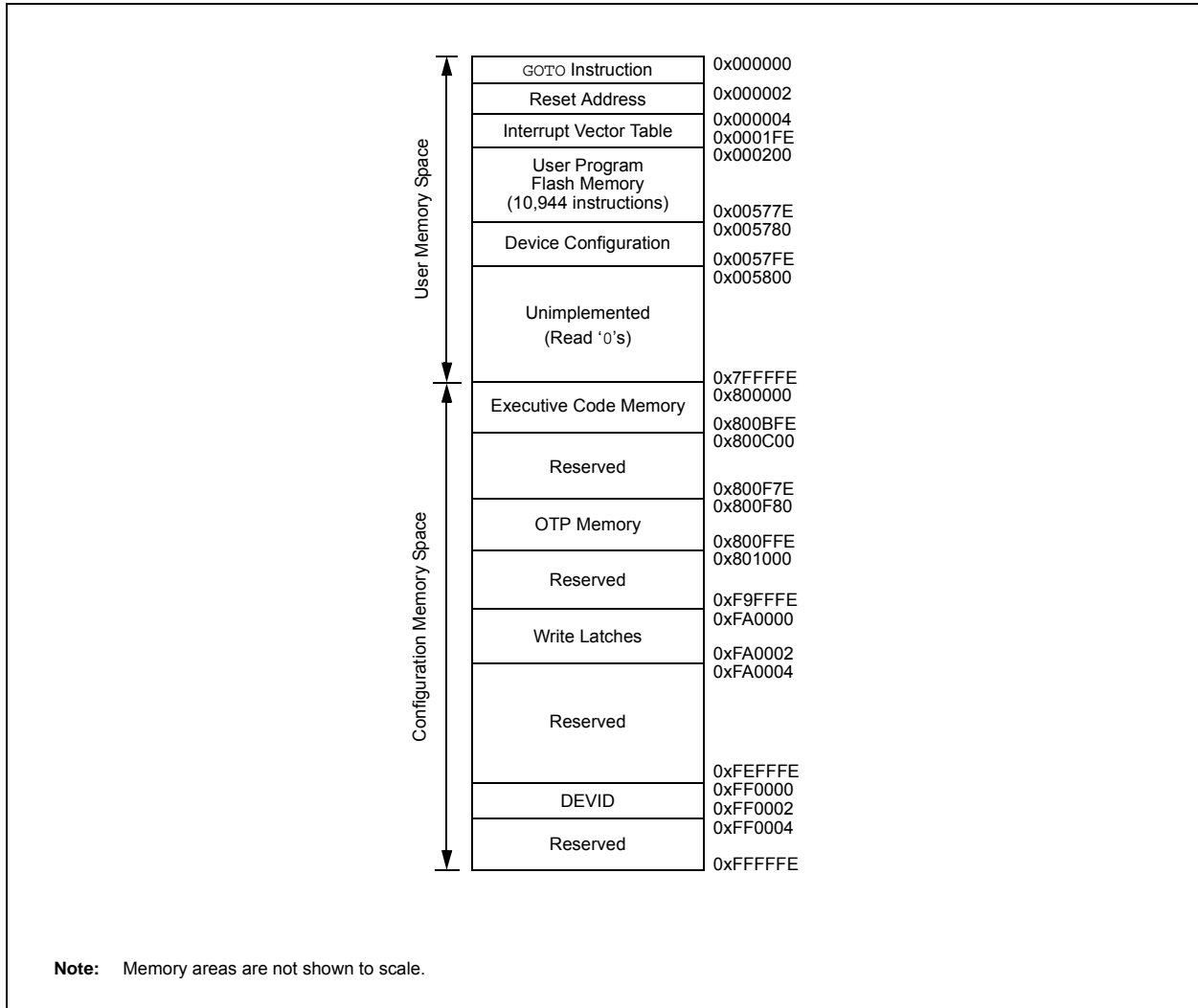
dsPIC33EPXXGS202 FAMILY

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP16GS202 DEVICES



dsPIC33EPXXGS202 FAMILY

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP32GS202 DEVICES



dsPIC33EPXXGS202 FAMILY

4.2.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-3).

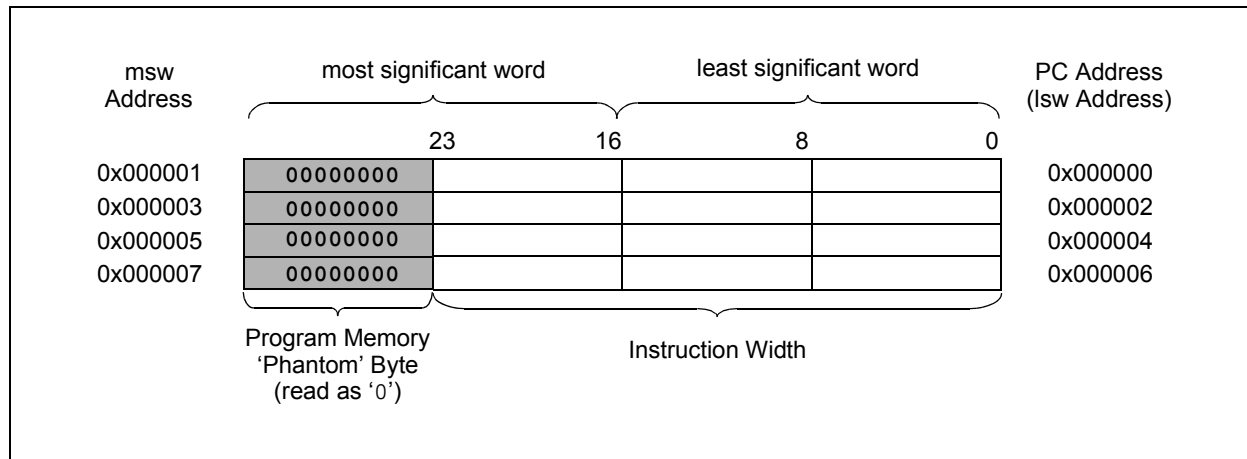
Program memory addresses are always word-aligned on the lower word, and addresses are incremented, or decremented, by two during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

4.2.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXGS202 family devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in Section 7.1 “Interrupt Vector Table”.

FIGURE 4-3: PROGRAM MEMORY ORGANIZATION



4.3 Data Address Space

The dsPIC33EPXXGS202 family CPU has a separate 16-bit wide data memory space. The Data Space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory map is shown in [Figure 4-4](#).

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This arrangement gives a base Data Space address range of 64 Kbytes or 32K words.

The lower half of the data memory space (i.e., when $EA<15> = 0$) is used for implemented memory addresses, while the upper half ($EA<15> = 1$) is reserved for the Program Space Visibility (PSV).

dsPIC33EPXXGS202 family devices implement up to 12 Kbytes of data memory. If an EA points to a location outside of this area, an all-zero word or byte is returned.

4.3.1 DATA SPACE WIDTH

The data memory space is organized in byte-addressable, 16-bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

4.3.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC[®] MCU devices and improve Data Space memory usage efficiency, the dsPIC33EPXXGS202 family instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB; the MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

4.3.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, are primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EPXXGS202 family core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control, and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

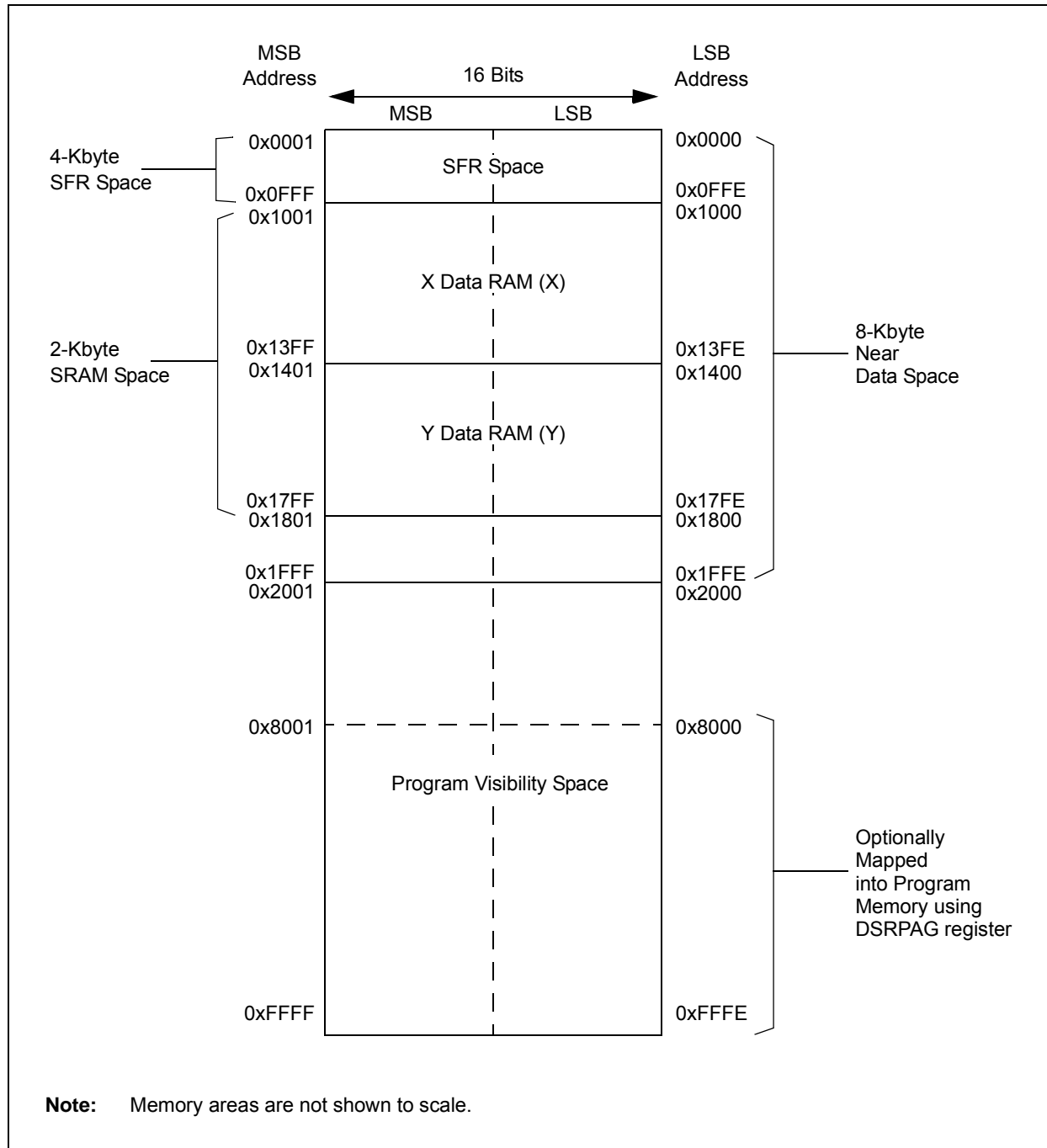
| |
|---|
| Note: The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information. |
|---|

4.3.4 NEAR DATA SPACE

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a Working register as an Address Pointer.

dsPIC33EPXXGS202 FAMILY

FIGURE 4-4: DATA MEMORY MAP FOR dsPIC33EP16/32GS202 DEVICES



dsPIC33EPXXGS202 FAMILY

4.3.5 X AND Y DATA SPACES

The dsPIC33EPXXGS202 core has two Data Spaces, X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X Data Space is used by all instructions and supports all addressing modes. X Data Space has separate read and write data buses. The X read data bus is the read data path for all instructions that view Data Space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y Data Space is used in concert with the X Data Space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSA, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X Data Space.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

4.4 Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

4.4.1 KEY RESOURCES

- “**dsPIC33E/PIC24E Program Memory**” (DS70000613) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

4.5 Special Function Register Maps

TABLE 4-2: CPU CORE REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets | |
|-----------------------|-------|---|--------|--------|--------|--------|--------|---|-------|-------|----------|---|-------|-------|-------|-------|-------|------------|------|
| W0 | 0000 | W0 (WREG) | | | | | | | | | | | | | | | | xxxx | |
| W1 | 0002 | W1 | | | | | | | | | | | | | | | | xxxx | |
| W2 | 0004 | W2 | | | | | | | | | | | | | | | | xxxx | |
| W3 | 0006 | W3 | | | | | | | | | | | | | | | | xxxx | |
| W4 | 0008 | W4 | | | | | | | | | | | | | | | | xxxx | |
| W5 | 000A | W5 | | | | | | | | | | | | | | | | xxxx | |
| W6 | 000C | W6 | | | | | | | | | | | | | | | | xxxx | |
| W7 | 000E | W7 | | | | | | | | | | | | | | | | xxxx | |
| W8 | 0010 | W8 | | | | | | | | | | | | | | | | xxxx | |
| W9 | 0012 | W9 | | | | | | | | | | | | | | | | xxxx | |
| W10 | 0014 | W10 | | | | | | | | | | | | | | | | xxxx | |
| W11 | 0016 | W11 | | | | | | | | | | | | | | | | xxxx | |
| W12 | 0018 | W12 | | | | | | | | | | | | | | | | xxxx | |
| W13 | 001A | W13 | | | | | | | | | | | | | | | | xxxx | |
| W14 | 001C | W14 | | | | | | | | | | | | | | | | xxxx | |
| W15 | 001E | W15 | | | | | | | | | | | | | | | | xxxx | |
| SPLIM | 0020 | SPLIM | | | | | | | | | | | | | | | | 0000 | |
| ACCAL | 0022 | ACCAL | | | | | | | | | | | | | | | | 0000 | |
| ACCAH | 0024 | ACCAH | | | | | | | | | | | | | | | | 0000 | |
| ACCAU | 0026 | Sign Extension of ACCA<39> | | | | | | | | ACCAU | | | | | | | | 0000 | |
| ACCBL | 0028 | ACCBL | | | | | | | | | | | | | | | | 0000 | |
| ACCBH | 002A | ACCBH | | | | | | | | | | | | | | | | 0000 | |
| ACCBU | 002C | Sign Extension of ACCB<39> | | | | | | | | ACCBU | | | | | | | | 0000 | |
| PCL | 002E | PCL<15:1> | | | | | | | | | | | | | | | | — | 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | — | PCH<6:0> | | | | | | | | 0000 |
| DSRPAG | 0032 | — | — | — | — | — | — | Extended Data Space (EDS) Read Page Register (DSRPAG<9:0>) | | | | | | | | | | 0001 | |
| DSWPAG ⁽¹⁾ | 0034 | — | — | — | — | — | — | Extended Data Space (EDS) Write Page Register (DSWPAG8:0>) ⁽¹⁾ | | | | | | | | | | 0001 | |
| RCOUNT | 0036 | RCOUNT<15:0> | | | | | | | | | | | | | | | | 0000 | |
| DCOUNT | 0038 | DO Loop Counter Register (DCOUNT<15:0>) | | | | | | | | | | | | | | | | 0000 | |
| DOSTARTL | 003A | DO Loop Start Address Register Low (DOSTARTL<15:1>) | | | | | | | | | | | | | | | | — | 0000 |
| DOSTARTH | 003C | — | — | — | — | — | — | — | — | — | — | DO Loop Start Address Register High (DOSTARTH<5:0>) | | | | | 0000 | | |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The contents of this register should never be modified. The DSWPAG must always point to the first page.

TABLE 4-2: CPU CORE REGISTER MAP (CONTINUED)

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|---|-------------|---------------|--------|--------|--------|--------|--------|-------------|-------|---|--------|-------|--------|--------|--------|------------|
| DOENDL | 003E | D0 Loop End Address Register Low (DOENDL<15:1>) | | | | | | | | | | | | | | | — | 0000 |
| DOENDH | 0040 | — | — | — | — | — | — | — | — | — | — | D0 Loop End Address Register High (DOENDH<5:0>) | | | | | 0000 | |
| SR | 0042 | OA | OB | SA | SB | OAB | SAB | DA | DC | IPL2 | IPL1 | IPL0 | RA | N | OV | Z | C | 0000 |
| CORCON | 0044 | VAR | — | US1 | US0 | EDT | DL2 | DL1 | DL0 | SATA | SATB | SATDW | ACCSAT | IPL3 | SFA | RND | IF | 0020 |
| MODCON | 0046 | XMODEN | YMODEN | — | — | BWM3 | BWM2 | BWM1 | BWM0 | YWM3 | YWM2 | YWM1 | YWM0 | XWM3 | XWM2 | XWM1 | XWM0 | 0000 |
| XMODSRT | 0048 | X Mode Start Address Register (XMODSRT<15:1>) | | | | | | | | | | | | | | | — | 0000 |
| XMODEND | 004A | X Mode End Address Register (XMODEND<15:1>) | | | | | | | | | | | | | | | — | 0001 |
| YMODSRT | 004C | Y Mode Start Address Register (YMODSRT<15:1>) | | | | | | | | | | | | | | | — | 0000 |
| YMODEND | 004E | Y Mode End Address Register (YMODEND<15:1>) | | | | | | | | | | | | | | | — | 0001 |
| XBREV | 0050 | BREN | XBREV<14:0> | | | | | | | | | | | | | | 0000 | |
| DISICNT | 0052 | — | — | DISICNT<13:0> | | | | | | | | | | | | | 0000 | |
| TBLPAG | 0054 | — | — | — | — | — | — | — | — | TBLPAG<7:0> | | | | | | | | 0000 |
| CTXTSTAT | 005A | — | — | — | — | — | CCTXI2 | CCTXI1 | CCTXI0 | — | — | — | — | — | MCTXI2 | MCTXI1 | MCTXI0 | 0000 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The contents of this register should never be modified. The DSWPAG must always point to the first page.

TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|----------|----------|-----------|-----------|-----------|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------------|
| IFS0 | 0800 | NVMIF | — | ADCIF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | — | — | — | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | — | — | INT2IF | — | — | — | — | — | — | — | — | INT1IF | CNIF | AC1IF | M2C1IF | SI2C1IF | 0000 |
| IFS3 | 0806 | — | — | — | — | — | — | PSEMIF | — | — | — | — | — | — | — | — | — | 0000 |
| IFS4 | 0808 | — | — | — | — | — | — | PSESIF | — | — | — | — | — | — | — | U1EIF | — | 0000 |
| IFS5 | 080A | PWM2IF | PWM1IF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS6 | 080C | ADCAN1IF | ADCAN0IF | — | — | — | — | — | — | AC2IF | — | — | — | — | — | — | PWM3IF | 0000 |
| IFS7 | 080E | — | — | — | — | — | — | — | — | — | — | ADCAN7IF | ADCAN6IF | ADCAN5IF | ADCAN4IF | ADCAN3IF | ADCAN2IF | 0000 |
| IFS9 | 0812 | — | — | ADCAN14IF | ADCAN13IF | ADCAN12IF | ADCAN11IF | ADCAN10IF | ADCAN9IF | ADCAN8IF | — | — | — | — | — | — | — | 0000 |
| IFS10 | 0814 | — | — | I2C1BCIF | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS11 | 0816 | — | — | — | — | — | — | — | — | — | — | — | — | ADFL0IF | ADCMP1IF | ADCMP0IF | — | 0000 |
| IEC0 | 0820 | NVMIE | — | ADCIE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | — | — | — | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | — | — | INT2IE | — | — | — | — | — | — | — | — | INT1IE | CNIE | AC1IF | M2C1IE | SI2C1IE | 0000 |
| IEC3 | 0826 | — | — | — | — | — | — | PSEMIE | — | — | — | — | — | — | — | — | — | 0000 |
| IEC4 | 0828 | — | — | — | — | — | — | PSESIE | — | — | — | — | — | — | — | U1EIE | — | 0000 |
| IEC5 | 082A | PWM2IE | PWM1IE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC6 | 082C | ADCAN1IE | ADCAN0IE | — | — | — | — | — | AC3IE | AC2IE | — | — | — | — | — | — | PWM3IE | 0000 |
| IEC7 | 082E | — | — | — | — | — | — | — | — | — | — | ADCAN7IE | ADCAN6IE | ADCAN5IE | ADCAN4IE | ADCAN3IE | ADCAN2IE | 0000 |
| IEC9 | 0832 | — | — | ADCAN14IE | ADCAN13IE | ADCAN12IE | ADCAN11IE | ADCAN10IE | ADCAN9IE | ADCAN8IE | — | — | — | — | — | — | — | 0000 |
| IEC10 | 0834 | — | — | I2C1BCIE | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC11 | 0836 | — | — | — | — | — | — | — | — | — | — | — | — | ADFL0IE | ADCMP1IE | ADCMP0IE | — | 0000 |
| IPC0 | 0840 | — | T1IP2 | T1IP1 | T1IP0 | — | OC1IP2 | OC1IP1 | OC1IP0 | — | IC1IP2 | IC1IP1 | IC1IP0 | — | INT0IP2 | INT0IP1 | INT0IP0 | 4444 |
| IPC1 | 0842 | — | T2IP2 | T2IP1 | T2IP0 | — | — | — | — | — | — | — | — | — | — | — | — | 4000 |
| IPC2 | 0844 | — | U1RXIP2 | U1RXIP1 | U1RXIP0 | — | SPI1IP2 | SPI1IP1 | SPI1IP0 | — | SPI1EIP2 | SPI1EIP1 | SPI1EIP0 | — | T3IP2 | T3IP1 | T3IP0 | 4444 |
| IPC3 | 0846 | — | NVMIP2 | NVMIP1 | NVMIP0 | — | — | — | — | — | ADCIP2 | ADCIP1 | ADCIP0 | — | U1TXIP2 | U1TXIP1 | U1TXIP0 | 4044 |
| IPC4 | 0848 | — | CNIP2 | CNIP1 | CNIP0 | — | AC1IP2 | AC1IP1 | AC1IP0 | — | M2C1IP2 | M2C1IP1 | M2C1IP0 | — | SI2C1IP2 | SI2C1IP1 | SI2C1IP0 | 4444 |
| IPC5 | 084A | — | — | — | — | — | — | — | — | — | — | — | — | — | INT1IP2 | INT1IP1 | INT1IP0 | 0004 |
| IPC7 | 084E | — | — | — | — | — | — | — | — | — | — | INT2IP2 | INT2IP1 | INT2IP0 | — | — | — | 0040 |
| IPC14 | 085C | — | — | — | — | — | — | — | — | — | PSEMIP2 | PSEMIP1 | PSEMIP0 | — | — | — | — | 0040 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP (CONTINUED)

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--------|------------|------------|------------|---------|------------|------------|------------|----------|------------|------------|------------|---------|------------|------------|------------|------------|
| IPC16 | 0860 | — | — | — | — | — | — | — | — | — | U1EIP2 | U1EIP1 | U1EIP0 | — | — | — | — | 0040 |
| IPC18 | 0864 | — | — | — | — | — | — | — | — | — | PSESIP2 | PSESIP1 | PSESIP0 | — | — | — | — | 0040 |
| IPC23 | 086E | — | PWM2IP2 | PWM2IP1 | PWM2IP0 | — | PWM1IP2 | PWM1IP1 | PWM1IP0 | — | — | — | — | — | — | — | — | 4400 |
| IPC24 | 0870 | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IP2 | PWM3IP1 | PWM3IP0 | 0004 |
| IPC25 | 0872 | — | AC2IP2 | AC2IP1 | AC2IP0 | — | — | — | — | — | — | — | — | — | — | — | — | 4000 |
| IPC27 | 0876 | — | ADCAN1IP2 | ADCAN1IP1 | ADCAN1IP0 | — | ADCAN0IP2 | ADCAN0IP1 | ADCAN0IP0 | — | — | — | — | — | — | — | — | 4400 |
| IPC28 | 0878 | — | ADCAN5IP2 | ADCAN5IP1 | ADCAN5IP0 | — | ADCAN4IP2 | ADCAN4IP1 | ADCAN4IP0 | — | ADCAN3IP2 | ADCAN3IP1 | ADCAN3IP0 | — | ADCAN2IP2 | ADCAN2IP1 | ADCAN2IP0 | 4444 |
| IPC29 | 087A | — | — | — | — | — | — | — | — | — | ADCAN7IP2 | ADCAN7IP1 | ADCAN7IP0 | — | ADCAN6IP2 | ADCAN6IP1 | ADCAN6IP0 | 0044 |
| IPC35 | 0886 | — | — | — | — | — | ICDIP2 | ICDIP1 | ICDIP0 | — | — | — | — | — | — | — | — | 0400 |
| IPC37 | 088A | — | ADCAN8IP2 | ADCAN8IP1 | ADCAN8IP0 | — | — | — | — | — | — | — | — | — | — | — | — | 4000 |
| IPC38 | 088C | — | ADCAN12IP2 | ADCAN12IP1 | ADCAN12IP0 | — | ADCAN11IP2 | ADCAN11IP1 | ADCAN11IP0 | — | ADCAN10IP2 | ADCAN10IP1 | ADCAN10IP0 | — | ADCAN9IP2 | ADCAN9IP1 | ADCAN9IP0 | 0444 |
| IPC39 | 088E | — | — | — | — | — | — | — | — | — | ADCAN14IP2 | ADCAN14IP1 | ADCAN14IP0 | — | ADCAN13IP2 | ADCAN13IP1 | ADCAN13IP0 | 0040 |
| IPC43 | 0896 | — | — | — | — | — | — | — | — | — | I2C1BCIP2 | I2C1BCIP1 | I2C1BCIP0 | — | — | — | — | 0040 |
| IPC44 | 0898 | — | ADFL0IP2 | ADFL0IP1 | ADFL0IP0 | — | ADCMP1IP2 | ADCMP1IP1 | ADCMP1IP0 | — | ADCMP1IP2 | ADCMP1IP1 | ADCMP1IP0 | — | — | — | — | 4440 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE | SFTACERR | DIV0ERR | — | MATHERR | ADDRERR | STKERR | OSCFail | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | AIVTEN | — | — | — | — | — | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | NAE | — | — | — | DOOVR | — | — | — | APLL | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | ILR3 | ILR2 | ILR1 | ILR0 | VECNUM7 | VECNUM6 | VECNUM5 | VECNUM4 | VECNUM3 | VECNUM2 | VECNUM1 | VECNUM0 | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-4: TIMER1 THROUGH TIMER3 REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--|--------|--------|--------|--------|--------|-------|-------|-------|-------|--------|--------|-------|-------|-------|-------|------------|
| TMR1 | 0100 | Timer1 Register | | | | | | | | | | | | | | | | xxxx |
| PR1 | 0102 | Period Register 1 | | | | | | | | | | | | | | | | FFFF |
| T1CON | 0104 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS1 | TCKPS0 | — | TSYNC | TCS | — | 0000 |
| TMR2 | 0106 | Timer2 Register | | | | | | | | | | | | | | | | xxxx |
| TMR3HLD | 0108 | Timer3 Holding Register (for 32-bit timer operations only) | | | | | | | | | | | | | | | | xxxx |
| TMR3 | 010A | Timer3 Register | | | | | | | | | | | | | | | | xxxx |
| PR2 | 010C | Period Register 2 | | | | | | | | | | | | | | | | FFFF |
| PR3 | 010E | Period Register 3 | | | | | | | | | | | | | | | | FFFF |
| T2CON | 0110 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS1 | TCKPS0 | T32 | — | TCS | — | 0000 |
| T3CON | 0112 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS1 | TCKPS0 | — | — | TCS | — | 0000 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-5: INPUT CAPTURE 1 REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|---------------------------------|--------|--------|---------|---------|---------|-------|-------|--------|----------|-------|----------|----------|----------|----------|----------|------------|
| IC1CON1 | 0140 | — | — | ICSIDL | ICTSEL2 | ICTSEL1 | ICTSEL0 | — | — | — | IC1 | IC10 | ICOV | ICBNE | ICM2 | ICM1 | ICM0 | 0000 |
| IC1CON2 | 0142 | — | — | — | — | — | — | — | — | ICTRIG | TRIGSTAT | — | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000D |
| IC1BUF | 0144 | Input Capture 1 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC1TMR | 0146 | Input Capture 1 Timer Register | | | | | | | | | | | | | | | | 0000 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-6: OUTPUT COMPARE 1 REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|-------------------------------------|--------|----------|---------|---------|---------|-------|-------|--------|----------|--------|----------|----------|----------|----------|----------|------------|
| OC1CON1 | 0900 | — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | — | ENFLTA | — | — | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 | 0000 |
| OC1CON2 | 0902 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | — | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000C |
| OC1RS | 0904 | Output Compare 1 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC1R | 0906 | Output Compare 1 Register | | | | | | | | | | | | | | | | xxxx |
| OC1TMR | 0908 | Timer Value 1 Register | | | | | | | | | | | | | | | | xxxx |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-7: PWM REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|---|--------|--------|--------|--------|--------|----------|----------|----------|----------|----------|----------|----------|--------------|---------|---------|------------|
| PTCON | 0C00 | PTEN | — | PTSIDL | SESTAT | SEIEN | EIPU | SYNCPOL | SYNCOEN | SYNCEN | SYNCSRC2 | SYNCSRC1 | SYNCSRC0 | SEVTPS3 | SEVTPS2 | SEVTPS1 | SEVTPS0 | 0000 |
| PTCON2 | 0C02 | — | — | — | — | — | — | — | — | — | — | — | — | — | PCLKDIV<2:0> | | | 0000 |
| PTPER | 0C04 | PWM Primary Master Time Base Period Register (PTPER<15:0>) | | | | | | | | | | | | | | | | FFF8 |
| SEVTCMP | 0C06 | PWM Special Event Compare Register (SEVTCMP<12:0>) | | | | | | | | | | | | | | | | 0000 |
| MDC | 0C0A | MDC<15:0> | | | | | | | | | | | | | | | | 0000 |
| STCON | 0C0E | — | — | — | SESTAT | SEIEN | EIPU | SYNCPOL | SYNCOEN | SYNCEN | SYNCSRC2 | SYNCSRC1 | SYNCSRC0 | SEVTPS3 | SEVTPS2 | SEVTPS1 | SEVTPS0 | 0000 |
| STCON2 | 0C10 | — | — | — | — | — | — | — | — | — | — | — | — | — | PCLKDIV<2:0> | | | 0000 |
| STPER | 0C12 | PWM Secondary Master Time Base Period Register (STPER<15:0>) | | | | | | | | | | | | | | | | FFF8 |
| SSEVTCMP | 0C14 | PWM Secondary Special Event Compare Register (SSEVTCMP<12:0>) | | | | | | | | | | | | | | | | 0000 |
| CHOP | 0C1A | CHPCLKEN | — | — | — | — | — | CHOPCLK6 | CHOPCLK5 | CHOPCLK4 | CHOPCLK3 | CHOPCLK2 | CHOPCLK1 | CHOPCLK0 | — | — | — | 0000 |
| PWMKEY | 0C1E | PWM Protection Lock/Unlock Key Value Register (PWMKEY<15:0>) | | | | | | | | | | | | | | | | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-8: PWM GENERATOR 1 REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|---|---------|---------------|---------|-----------|-----------|-----------|-----------|---------|---------|----------|----------|----------|----------|---------|---------|------------|
| PWMCON1 | 0C20 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC1 | DTC0 | — | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON1 | 0C22 | PENH | PENL | POLH | POLL | PMOD1 | PMOD0 | OVRENH | OVRENL | OVRDAT1 | OVRDAT0 | FLTDAT1 | FLTDAT0 | CLDAT1 | CLDAT0 | SWAP | OSYNC | C000 |
| FCLCON1 | 0C24 | IFLTMOD | CLSRC4 | CLSRC3 | CLSRC2 | CLSRC1 | CLSRC0 | CLPOL | CLMOD | FLTSRC4 | FLTSRC3 | FLTSRC2 | FLTSRC1 | FLTSRC0 | FLTPOL | FLTMOD1 | FLTMOD0 | 00F8 |
| PDC1 | 0C26 | PWM Generator 1 Duty Cycle Register (PDC1<15:0>) | | | | | | | | | | | | | | | | 0000 |
| PHASE1 | 0C28 | PWM Phase-Shift Value or Independent Time Base Period for the PWM Generator 1 Register (PHASE1<15:0>) | | | | | | | | | | | | | | | | 0000 |
| DTR1 | 0C2A | — | — | DTR1<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR1 | 0C2C | — | — | ALTDTR1<13:0> | | | | | | | | | | | | | | 0000 |
| SDC1 | 0C2E | SDC1<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE1 | 0C30 | SPHASE1<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG1 | 0C32 | TRGCMP<12:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON1 | 0C34 | TRGDIV3 | TRGDIV2 | TRGDIV1 | TRGDIV0 | — | — | — | — | DTM | — | TRGSTR5 | TRGSTR4 | TRGSTR3 | TRGSTR2 | TRGSTR1 | TRGSTR0 | 0000 |
| STRIG1 | 0C36 | STRGCMP<12:0> | | | | | | | | | | | | | | | | 0000 |
| PWMCAP1 | 0C38 | PWMCAP<12:0> | | | | | | | | | | | | | | | | 0000 |
| LEBCON1 | 0C3A | PHR | PHF | PLR | PLF | FLTEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY1 | 0C3C | — | — | — | — | LEB<8:0> | | | | | | | | | | | 0000 | |
| AUXCON1 | 0C3E | HRPDIS | HRDDIS | — | — | BLANKSEL3 | BLANKSEL2 | BLANKSEL1 | BLANKSEL0 | — | — | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSEL0 | CHOPHEN | CHOPLEN | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-9: PWM GENERATOR 2 REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets | |
|-----------|-------|---|---------|---------------|---------|-----------|-----------|-----------|-----------|---------|---------|----------|----------|----------|----------|----------|----------|------------|------|
| PWMCON2 | 0C40 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEEN | TRGIEN | ITB | MDCS | DTC1 | DTC0 | — | — | MTBS | CAM | XPRES | IUE | 0000 | |
| IOCON2 | 0C42 | PENH | PENL | POLH | POLL | PMOD1 | PMOD0 | OVRENH | OVRENL | OVRDAT1 | OVRDAT0 | FLTDAT1 | FLTDAT0 | CLDAT1 | CLDAT0 | SWAP | OSYNC | C000 | |
| FCLCON2 | 0C44 | IFLTMOD | CLSRC4 | CLSRC3 | CLSRC2 | CLSRC1 | CLSRC0 | CLPOL | CLMOD | FLTSRC4 | FLTSRC3 | FLTSRC2 | FLTSRC1 | FLTSRC0 | FLTPOL | FLTMOD1 | FLTMOD0 | 00F8 | |
| PDC2 | 0C46 | PWM Generator 2 Duty Cycle Register (PDC2<15:0>) | | | | | | | | | | | | | | | | 0000 | |
| PHASE2 | 0C48 | PWM Phase-Shift Value or Independent Time Base Period for the PWM Generator 2 Register (PHASE2<15:0>) | | | | | | | | | | | | | | | | 0000 | |
| DTR2 | 0C4A | — | — | DTR2<13:0> | | | | | | | | | | | | | | 0000 | |
| ALTDTR2 | 0C4C | — | — | ALTDTR2<13:0> | | | | | | | | | | | | | | 0000 | |
| SDC2 | 0C4E | SDC2<15:0> | | | | | | | | | | | | | | | | 0000 | |
| SPHASE2 | 0C50 | SPHASE2<15:0> | | | | | | | | | | | | | | | | 0000 | |
| TRIG2 | 0C52 | TRGCMP<12:0> | | | | | | | | | | | | — | — | — | 0000 | | |
| TRGCON2 | 0C54 | TRGDIV3 | TRGDIV2 | TRGDIV1 | TRGDIV0 | — | — | — | — | DTM | — | TRGSTRT5 | TRGSTRT4 | TRGSTRT3 | TRGSTRT2 | TRGSTRT1 | TRGSTRT0 | 0000 | |
| STRIG2 | 0C56 | STRGCMP<12:0> | | | | | | | | | | | | — | — | — | 0000 | | |
| PWMCAP2 | 0C58 | PWMCAP<12:0> | | | | | | | | | | | | — | — | — | 0000 | | |
| LEBCON2 | 0C5A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 | |
| LEBDLY2 | 0C5C | — | — | — | — | LEB<8:0> | | | | | | | | | | — | — | — | 0000 |
| AUXCON2 | 0C5E | HRPDIS | HRDDIS | — | — | BLANKSEL3 | BLANKSEL2 | BLANKSEL1 | BLANKSEL0 | — | — | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSEL0 | CHOPHEN | CHOPLEN | 0000 | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-10: PWM GENERATOR 3 REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets | | | |
|-----------|-------|---|---------|---------------|---------|-----------|-----------|-----------|-----------|---------|---------|----------|----------|----------|----------|----------|----------|------------|---|---|------|
| PWMCON3 | 0C60 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC1 | DTC0 | — | — | MTBS | CAM | XPRES | IUE | 0000 | | | |
| IOCON3 | 0C62 | PENH | PENL | POLH | POLL | PMOD1 | PMOD0 | OVRENH | OVRENL | OVRDAT1 | OVRDAT0 | FLTDAT1 | FLTDAT0 | CLDAT1 | CLDAT0 | SWAP | OSYNC | C000 | | | |
| FCLCON3 | 0C64 | IFLTMOD | CLSRC4 | CLSRC3 | CLSRC2 | CLSRC1 | CLSRC0 | CLPOL | CLMOD | FLTSRC4 | FLTSRC3 | FLTSRC2 | FLTSRC1 | FLTSRC0 | FLTPOL | FLTMOD1 | FLTMOD0 | 00F8 | | | |
| PDC3 | 0C66 | PWM Generator 3 Duty Cycle Value Register (PDC3<15:0>) | | | | | | | | | | | | | | | | 0000 | | | |
| PHASE3 | 0C68 | Phase-Shift Value or Independent Time Base Period for the PWM Generator 3 Register (PHASE3<15:0>) | | | | | | | | | | | | | | | | 0000 | | | |
| DTR3 | 0C6A | — | — | DTR3<13:0> | | | | | | | | | | | | | | 0000 | | | |
| ALTDTR3 | 0C6C | — | — | ALTDTR3<13:0> | | | | | | | | | | | | | | 0000 | | | |
| SDC3 | 0C6E | SDC3<15:0> | | | | | | | | | | | | | | | | 0000 | | | |
| SPHASE3 | 0C70 | SPHASE3<15:0> | | | | | | | | | | | | | | | | 0000 | | | |
| TRIG3 | 0C72 | TRGCMP<12:0> | | | | | | | | | | | | — | — | — | 0000 | | | | |
| TRGCON3 | 0C74 | TRGDIV3 | TRGDIV2 | TRGDIV1 | TRGDIV0 | — | — | — | — | DTM | — | TRGSTRT5 | TRGSTRT4 | TRGSTRT3 | TRGSTRT2 | TRGSTRT1 | TRGSTRT0 | 0000 | | | |
| STRIG3 | 0C76 | STRGCMP<12:0> | | | | | | | | | | | | — | — | — | 0000 | | | | |
| PWMCAP3 | 0C78 | PWMCAP<12:0> | | | | | | | | | | | | | | | | 0000 | | | |
| LEBCON3 | 0C7A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 | | | |
| LEBDLY3 | 0C7C | — | — | — | — | LEB<8:0> | | | | | | | | | | | | — | — | — | 0000 |
| AUXCON3 | 0C7E | HRPDIS | HRDDIS | — | — | BLANKSEL3 | BLANKSEL2 | BLANKSEL1 | BLANKSEL0 | — | — | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSEL0 | CHOPHEN | CHOPLEN | 0000 | | | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-11: I2C1 REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets | |
|-----------|-------|------------------------------|--------|---------|--------|--------|--------|----------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------------------------|------|
| I2C1CONL | 0200 | I2CEN | — | I2CSIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 | |
| I2C1CONH | 0202 | — | — | — | — | — | — | — | — | — | PCIE | SCIE | BOEN | SDAHT | SBCDE | AHEN | DHEN | 0000 | |
| I2C1STAT | 0204 | ACKSTAT | TRSTAT | ACKTIM | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 | |
| I2C1ADD | 0206 | — | — | — | — | — | — | I2C1 Address Register | | | | | | | | | | 0000 | |
| I2C1MSK | 0208 | — | — | — | — | — | — | I2C1 Address Mask Register | | | | | | | | | | 0000 | |
| I2C1BRG | 020A | Baud Rate Generator Register | | | | | | | | | | | | | | | | 0000 | |
| I2C1TRN | 020C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | I2C1 Transmit Register | 00FF |
| I2C1RCV | 020E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | I2C1 Receive Register | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: UART1 REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--|--------|----------|--------|--------|--------|-------|-------------------------|----------|----------|-------|--------|-------|--------|--------|-------|------------|
| U1MODE | 0220 | UARTEN | — | USIDL | IREN | RTSMD | — | UEN1 | UEN0 | WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL1 | PDSEL0 | STSEL | 0000 |
| U1STA | 0222 | UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL1 | URXISEL0 | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| U1TXREG | 0224 | — | — | — | — | — | — | — | UART1 Transmit Register | | | | | | | | | xxxx |
| U1RXREG | 0226 | — | — | — | — | — | — | — | UART1 Receive Register | | | | | | | | | 0000 |
| U1BRG | 0228 | Baud Rate Generator Prescaler Register | | | | | | | | | | | | | | | | 0000 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-13: SPI1 REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|---|--------|---------|--------|--------|---------|---------|---------|-------|--------|--------|--------|--------|--------|--------|--------|------------|
| SPI1STAT | 0240 | SPIEN | — | SPISIDL | — | — | SPIBEC2 | SPIBEC1 | SPIBEC0 | SRMPT | SPIROV | SRXMPT | SISEL2 | SISEL1 | SISEL0 | SPITBF | SPIRBF | 0000 |
| SPI1CON1 | 0242 | — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | SPRE2 | SPRE1 | SPRE0 | PPRE1 | PPRE0 | 0000 |
| SPI1CON2 | 0244 | FRMEN | SPIFSD | FRMPOL | — | — | — | — | — | — | — | — | — | — | — | FRMDLY | SPIBEN | 0000 |
| SPI1BUF | 0248 | SPI1 Transmit and Receive Buffer Register | | | | | | | | | | | | | | | | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-14: ADC REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets | |
|-----------|-------|---------------------|--------------|---------|---------------|-------------|-----------|-----------|-----------|----------|----------|---------------|-----------|---------------|-----------|-----------|-----------|------------|------|
| ADCON1L | 0300 | ADON | — | ADSIDL | — | — | — | — | — | NRE | — | — | — | — | — | — | — | 1000 | |
| ADCON1H | 0302 | — | — | — | — | — | — | — | — | FORM | SHRRES1 | SHRRES0 | — | — | — | — | — | 0060 | |
| ADCON2L | 0304 | REFCIE | REFERCIE | — | EIEN | — | SHREISEL2 | SHREISEL1 | SHREISEL0 | — | SHRADCS6 | SHRADCS5 | SHRADCS4 | SHRADCS3 | SHRADCS2 | SHRADCS1 | SHRADCS0 | 0000 | |
| ADCON2H | 0306 | REFRDY | REFERR | — | — | — | — | SHRSAMC9 | SHRSAMC8 | SHRSAMC7 | SHRSAMC6 | SHRSAMC5 | SHRSAMC4 | SHRSAMC3 | SHRSAMC2 | SHRSAMC1 | SHRSAMC0 | 0000 | |
| ADCON3L | 0308 | REFSEL2 | REFSEL1 | REFSEL0 | SUSPEND | SUSPCIE | SUSPRDY | SHRSAMP | CNVRTCH | SWLCTRG | SWCTRG | CNVCHSEL5 | CNVCHSEL4 | CNVCHSEL3 | CNVCHSEL2 | CNVCHSEL1 | CNVCHSEL0 | 0000 | |
| ADCON3H | 030A | CLKSEL1 | CLKSEL0 | CLKDIV5 | CLKDIV4 | CLKDIV3 | CLKDIV2 | CLKDIV1 | CLKDIV0 | SHREN | — | — | — | — | — | C1EN | COEN | 0000 | |
| ADCON4L | 030C | — | — | — | — | — | — | r | r | — | — | — | — | — | — | SAMC1EN | SAMC0EN | 0000 | |
| ADCON4H | 030E | — | — | — | — | — | — | — | — | — | — | — | — | C1CHS1 | C1CHS0 | C0CHS1 | C0CHS0 | 0000 | |
| ADMOD0L | 0310 | — | SIGN7 | — | SIGN6 | — | SIGN5 | — | SIGN4 | — | SIGN3 | — | SIGN2 | DIFF1 | SIGN1 | DIFF0 | SIGN0 | 0000 | |
| ADMOD0H | 0312 | — | — | DIFF14 | SIGN14 | — | SIGN13 | — | SIGN12 | — | SIGN11 | — | SIGN10 | — | SIGN9 | — | SIGN8 | 0000 | |
| ADIEL | 0320 | — | IE<14:0> | | | | | | | | | | | | | | | 0000 | |
| ADSTATL | 0330 | — | AN14RDY | AN13RDY | AN12RDY | AN11RDY | AN10RDY | AN9RDY | AN8RDY | AN7RDY | AN6RDY | AN5RDY | AN4RDY | AN3RDY | AN2RDY | AN1RDY | AN0RDY | 0000 | |
| ADCMPOENL | 0338 | — | CMPEN<14:0> | | | | | | | | | | | | | | | 0000 | |
| ADCMPOLO | 033C | ADC CMPLO Register | | | | | | | | | | | | | | | | 0000 | |
| ADCMPOHI | 033E | ADC CMPHI Register | | | | | | | | | | | | | | | | 0000 | |
| ADCMP1ENL | 0340 | — | CMPEN14 | — | — | CMPEN<11:0> | | | | | | | | | | | | 0000 | |
| ADCMP1LO | 0344 | ADC CMPLO Register | | | | | | | | | | | | | | | | 0000 | |
| ADCMP1HI | 0346 | ADC CMPHI Register | | | | | | | | | | | | | | | | 0000 | |
| ADFL0DAT | 0368 | ADC FLDATA Register | | | | | | | | | | | | | | | | 0000 | |
| ADFL0CON | 036A | FLEN | MODE1 | MODE0 | OVRSAM2 | OVRSAM1 | OVRSAM0 | IE | RDY | — | — | — | — | FLCHSEL4 | FLCHSEL3 | FLCHSEL2 | FLCHSEL1 | FLCHSEL0 | 0000 |
| ADTRIG0L | 0380 | — | — | — | TRGSRC1<4:0> | | | | — | — | — | TRGSRC0<4:0> | | | | | | | 0000 |
| ADTRIG0H | 0382 | — | — | — | TRGSRC3<4:0> | | | | — | — | — | TRGSRC2<4:0> | | | | | | | 0000 |
| ADTRIG1L | 0384 | — | — | — | TRGSRC5<4:0> | | | | — | — | — | TRGSRC4<4:0> | | | | | | | 0000 |
| ADTRIG1H | 0386 | — | — | — | TRGSRC7<4:0> | | | | — | — | — | TRGSRC6<4:0> | | | | | | | 0000 |
| ADTRIG2L | 0388 | — | — | — | TRGSRC9<4:0> | | | | — | — | — | TRGSRC8<4:0> | | | | | | | 0000 |
| ADTRIG2H | 038A | — | — | — | TRGSRC11<4:0> | | | | — | — | — | TRGSRC10<4:0> | | | | | | | 0000 |
| ADTRIG3L | 038C | — | — | — | TRGSRC13<4:0> | | | | — | — | — | TRGSRC12<4:0> | | | | | | | 0000 |
| ADTRIG3H | 038E | — | — | — | — | — | — | — | — | — | — | — | — | TRGSRC14<4:0> | | | | 0000 | |
| ADCMPOCON | 03A0 | — | — | — | CHNL4 | CHNL3 | CHNL2 | CHNL1 | CHNL0 | CMPEN | IE | STAT | BTWN | HIHI | HILO | LOHI | LOLO | 0000 | |
| ADCMPICON | 03A4 | — | — | — | CHNL4 | CHNL3 | CHNL2 | CHNL1 | CHNL0 | CMPEN | IE | STAT | BTWN | HIHI | HILO | LOHI | LOLO | 0000 | |
| ADLVLTRGL | 03D0 | — | LVLEN<14:0> | | | | | | | | | | | | | | | 0000 | |
| ADCORE0L | 03D4 | — | — | — | — | — | — | SAMC<9:0> | | | | SAMC<9:0> | | | | | | 0000 | |
| ADCORE0H | 03D6 | — | — | — | EISEL2 | EISEL1 | EISEL0 | RES1 | RES0 | — | ADCS6 | ADCS5 | ADCS4 | ADCS3 | ADCS2 | ADCS1 | ADCS0 | 0000 | |
| ADCORE1L | 03D8 | — | — | — | — | — | — | SAMC<9:0> | | | | SAMC<9:0> | | | | | | 0000 | |
| ADCORE1H | 03DA | — | — | — | EISEL2 | EISEL1 | EISEL0 | RES1 | RES0 | — | ADCS6 | ADCS5 | ADCS4 | ADCS3 | ADCS2 | ADCS1 | ADCS0 | 0000 | |
| ADEIEL | 03F0 | — | EIEN<14:0> | | | | | | | | | | | | | | | 0000 | |
| ADEISTATL | 03F8 | — | EISTAT<14:0> | | | | | | | | | | | | | | | 0000 | |

Legend: — = unimplemented, read as '0'; r - reserved bit. Reset values are shown in hexadecimal.

TABLE 4-14: ADC REGISTER MAP (CONTINUED)

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--------------------|--------|--------|--------|-----------|-----------|-----------|-----------|---------|-------|-------|-------|-------|----------|--------|---------|------------|
| ADCON5L | 0400 | SHRRDY | — | — | — | — | — | C1RDY | C0RDY | SHRPWR | — | — | — | — | — | C1PWR | C0PWR | 0000 |
| ADCON5H | 0402 | — | — | — | — | WARMTIME3 | WARMTIME2 | WARMTIME1 | WARMTIME0 | SHRCIE | — | — | — | — | — | C1CIE | C0CIE | 0000 |
| ADCAL0L | 0404 | CAL1RDY | — | — | — | r | CAL1DIFF | CAL1EN | CAL1RUN | CAL0RDY | — | — | — | r | CAL0DIFF | CAL0EN | CAL0RUN | 0000 |
| ADCAL1H | 040A | CSHRRDY | — | — | — | r | — | CSHREN | CSHRRUN | — | — | — | — | — | — | — | — | 0000 |
| ADCBUF0 | 040C | ADC Data Buffer 0 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF1 | 040E | ADC Data Buffer 1 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF2 | 0410 | ADC Data Buffer 2 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF3 | 0412 | ADC Data Buffer 3 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF4 | 0414 | ADC Data Buffer 4 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF5 | 0416 | ADC Data Buffer 5 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF6 | 0418 | ADC Data Buffer 6 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF7 | 041A | ADC Data Buffer 7 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF8 | 041C | ADC Data Buffer 8 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF9 | 041E | ADC Data Buffer 9 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF10 | 0420 | ADC Data Buffer 10 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF11 | 0422 | ADC Data Buffer 11 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF12 | 0424 | ADC Data Buffer 12 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF13 | 0426 | ADC Data Buffer 13 | | | | | | | | | | | | | | | | 0000 |
| ADCBUF14 | 0428 | ADC Data Buffer 14 | | | | | | | | | | | | | | | | 0000 |

Legend: — = unimplemented, read as '0'; r - reserved bit. Reset values are shown in hexadecimal.

TABLE 4-15: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--------|--------|---------|---------|---------|---------|---------|---------|-------|-------|---------|---------|---------|---------|---------|---------|------------|
| RPOR0 | 0670 | — | — | RP33R5 | RP33R4 | RP33R3 | RP33R2 | RP33R1 | RP33R0 | — | — | RP32R5 | RP32R4 | RP32R3 | RP32R2 | RP32R1 | RP32R0 | 0000 |
| RPOR1 | 0672 | — | — | RP35R5 | RP35R4 | RP35R3 | RP35R2 | RP35R1 | RP35R0 | — | — | RP34R5 | RP34R4 | RP34R3 | RP34R2 | RP34R1 | RP34R0 | 0000 |
| RPOR2 | 0674 | — | — | RP37R5 | RP37R4 | RP37R3 | RP37R2 | RP37R1 | RP37R0 | — | — | RP36R5 | RP36R4 | RP36R3 | RP36R2 | RP36R1 | RP36R0 | 0000 |
| RPOR3 | 0676 | — | — | RP39R5 | RP39R4 | RP39R3 | RP39R2 | RP39R1 | RP39R0 | — | — | RP38R5 | RP38R4 | RP38R3 | RP38R2 | RP38R1 | RP38R0 | 0000 |
| RPOR4 | 0678 | — | — | RP41R5 | RP41R4 | RP41R3 | RP41R2 | RP41R1 | RP41R0 | — | — | RP40R5 | RP40R4 | RP40R3 | RP40R2 | RP40R1 | RP40R0 | 0000 |
| RPOR5 | 067A | — | — | RP43R5 | RP43R4 | RP43R3 | RP43R2 | RP43R1 | RP43R0 | — | — | RP42R5 | RP42R4 | RP42R3 | RP42R2 | RP42R1 | RP42R0 | 0000 |
| RPOR6 | 067C | — | — | RP45R5 | RP45R4 | RP45R3 | RP45R2 | RP45R1 | RP45R0 | — | — | RP44R5 | RP44R4 | RP44R3 | RP44R2 | RP44R1 | RP44R0 | 0000 |
| RPOR7 | 067E | — | — | RP47R5 | RP47R4 | RP47R3 | RP47R2 | RP47R1 | RP47R0 | — | — | RP46R5 | RP46R4 | RP46R3 | RP46R2 | RP46R1 | RP46R0 | 0000 |
| RPOR8 | 0680 | — | — | RP177R5 | RP177R4 | RP177R3 | RP177R2 | RP177R1 | RP177R0 | — | — | RP176R5 | RP176R4 | RP176R3 | RP176R2 | RP176R1 | RP176R0 | 0000 |
| RPOR9 | 0682 | — | — | RP179R5 | RP179R4 | RP179R3 | RP179R2 | RP179R1 | RP179R0 | — | — | RP178R5 | RP178R4 | RP178R3 | RP178R2 | RP178R1 | RP178R0 | 0000 |
| RPOR10 | 0684 | — | — | RP181R5 | RP181R4 | RP181R3 | RP181R2 | RP181R1 | RP181R0 | — | — | RP180R5 | RP180R4 | RP180R3 | RP180R2 | RP180R1 | RP180R0 | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-16: PERIPHERAL PIN SELECT INPUT REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets | |
|-----------|-------|--------------|----------|----------|----------|----------|----------|----------|----------|--------------|--------|--------|--------|--------|--------|--------|--------|------------|------|
| RPINR0 | 06A0 | INT1R<7:0> | | | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | INT2R<7:0> | | | | | | | | | 0000 |
| RPINR2 | 06A4 | T1CKR<7:0> | | | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR3 | 06A6 | T3CKR7 | T3CKR6 | T3CKR5 | T3CKR4 | T3CKR3 | T3CKR2 | T3CKR1 | T3CKR0 | T2CKR7 | T2CKR6 | T2CKR5 | T2CKR4 | T2CKR3 | T2CKR2 | T2CKR1 | T2CKR0 | 0000 | |
| RPINR7 | 06AE | — | — | — | — | — | — | — | — | IC1R<7:0> | | | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | OCFAR<7:0> | | | | | | | | | 0000 |
| RPINR12 | 06B8 | FLT2R7 | FLT2R6 | FLT2R5 | FLT2R4 | FLT2R3 | FLT2R2 | FLT2R1 | FLT2R0 | FLT1R7 | FLT1R6 | FLT1R5 | FLT1R4 | FLT1R3 | FLT1R2 | FLT1R1 | FLT1R0 | 0000 | |
| RPINR13 | 06BA | FLT4R7 | FLT4R6 | FLT4R5 | FLT4R4 | FLT4R3 | FLT4R2 | FLT4R1 | FLT4R0 | FLT3R7 | FLT3R6 | FLT3R5 | FLT3R4 | FLT3R3 | FLT3R2 | FLT3R1 | FLT3R0 | 0000 | |
| RPINR18 | 06C4 | U1CTSR7 | U1CTSR6 | U1CTSR5 | U1CTSR4 | U1CTSR3 | U1CTSR2 | U1CTSR1 | U1CTS0 | U1RXR7 | U1RXR6 | U1RXR5 | U1RXR4 | U1RXR3 | U1RXR2 | U1RXR1 | U1RXR0 | 0000 | |
| RPINR20 | 06C8 | SCK1INR7 | SCK1INR6 | SCK1INR5 | SCK1INR4 | SCK1INR3 | SCK1INR2 | SCK1INR1 | SCK1INR0 | SDI1R7 | SDI1R6 | SDI1R5 | SDI1R4 | SDI1R3 | SDI1R2 | SDI1R1 | SDI1R0 | 0000 | |
| RPINR21 | 06CA | — | — | — | — | — | — | — | — | SS1R<7:0> | | | | | | | | | 0000 |
| RPINR37 | 06EA | SYNCl1R<7:0> | | | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR38 | 06EC | — | — | — | — | — | — | — | — | SYNCl2R<7:0> | | | | | | | | | 0000 |
| RPINR42 | 06F4 | FLT6R7 | FLT6R6 | FLT6R5 | FLT6R4 | FLT6R3 | FLT6R2 | FLT6R1 | FLT6R0 | FLT5R7 | FLT5R6 | FLT5R5 | FLT5R4 | FLT5R3 | FLT5R2 | FLT5R1 | FLT5R0 | 0000 | |
| RPINR43 | 06F6 | FLT8R7 | FLT8R6 | FLT8R5 | FLT8R4 | FLT8R3 | FLT8R2 | FLT8R1 | FLT8R0 | FLT7R7 | FLT7R6 | FLT7R5 | FLT7R4 | FLT7R3 | FLT7R2 | FLT7R1 | FLT7R0 | 0000 | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-17: NVM REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|------------|-------|-----------------|--------|--------|---------|--------|--------|-------|-------|-------|-------|-------|------------------|---------------|--------|--------|--------|------------|
| NVMCON | 0728 | WR | WREN | WRERR | NVMSIDL | — | — | RPDF | URERR | — | — | — | — | NVMOP3 | NVMOP2 | NVMOP1 | NVMOP0 | 0000 |
| NVMADR | 072A | NVMADR<15:0> | | | | | | | | | | | | | | | | 0000 |
| NVMADRU | 072C | — | — | — | — | — | — | — | — | — | — | — | — | NVMADR<23:16> | | | | 0000 |
| NVMKEY | 072E | — | — | — | — | — | — | — | — | — | — | — | NVMKEY<7:0> | | | | | 0000 |
| NVMSRCADRL | 0730 | NVMSRCADR<15:0> | | | | | | | | | | | | | | | | 0000 |
| NVMSRCADRH | 0732 | — | — | — | — | — | — | — | — | — | — | — | NVMSRCADR<23:16> | | | | | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-18: SYSTEM CONTROL REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets | |
|-----------|-------|--------|------------|---------|--------|--------|-----------|-----------|-------------|----------|----------|----------|---------|---------|---------|---------|---------|------------|------|
| RCON | 0740 | TRAPR | IOPUWR | — | — | VREGSF | — | CM | VREGS | EXTR | SWR | SWDTEN | WDTO | SLEEP | IDLE | BOR | POR | Note 1 | |
| OSCCON | 0742 | — | COSC2 | COSC1 | COSC0 | — | NOSC2 | NOSC1 | NOSC0 | CLKLOCK | IOLOCK | LOCK | — | CF | — | — | OSWEN | Note 2 | |
| CLKDIV | 0744 | ROI | DOZE2 | DOZE1 | DOZE0 | DOZEN | FRCDIV2 | FRCDIV1 | FRCDIV0 | PLLPOST1 | PLLPOST0 | — | PLLPRE4 | PLLPRE3 | PLLPRE2 | PLLPRE1 | PLLPRE0 | 3040 | |
| PLLFBD | 0746 | — | — | — | — | — | — | — | PLLDIV<8:0> | | | | | | | | | 0030 | |
| OSCTUN | 0748 | — | — | — | — | — | — | — | — | — | — | TUN<5:0> | | | | | | 0000 | |
| LFSR | 074C | — | LFSR<14:0> | | | | | | | | | | | | | | | | 0000 |
| ACLKCON | 0750 | ENAPLL | APLLCK | SELACLK | — | — | APSTSCLR2 | APSTSCLR1 | APSTSCLR0 | ASRCSEL | FRCSEL | — | — | — | — | — | — | 2740 | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: RCON register Reset values are dependent on the type of Reset.

2: OSCCON register Reset values are dependent on the Configuration fuses.

TABLE 4-19: PMD REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--------|--------|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|--------|-------|--------|-------|------------|
| PMD1 | 0760 | — | — | T3MD | T2MD | T1MD | — | PWMMD | — | I2C1MD | — | U1MD | — | SPI1MD | — | — | ADCMD | 0000 |
| PMD2 | 0762 | — | — | — | — | — | — | — | IC1MD | — | — | — | — | — | — | — | OC1MD | 0000 |
| PMD3 | 0764 | — | — | — | — | — | CMPMD | — | — | — | — | — | — | — | — | — | — | 0000 |
| PMD6 | 076A | — | — | — | — | — | PWM3MD | PWM2MD | PWM1MD | — | — | — | — | — | — | — | — | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | CMP2MD | CMP1MD | — | — | — | — | — | — | PGA1MD | — | 0000 |
| PMD8 | 076E | — | — | — | — | — | PGA2MD | — | — | — | — | — | — | — | — | — | — | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-20: PROGRAMMABLE GAIN AMPLIFIER REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--------|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------------|-------|-------|-------|-------|-------|------------|
| PGA1CON | 0504 | PGAEN | — | SELPI2 | SELPI1 | SELPI0 | SELNI2 | SELNI1 | SELNI0 | — | — | — | — | — | GAIN2 | GAIN1 | GAIN0 | 0000 |
| PGA1CAL | 0506 | — | — | — | — | — | — | — | — | — | — | PGACAL<5:0> | | | | | | 0000 |
| PGA2CON | 0508 | PGAEN | — | SELPI2 | SELPI1 | SELPI0 | SELNI2 | SELNI1 | SELNI0 | — | — | — | — | — | GAIN2 | GAIN1 | GAIN0 | 0000 |
| PGA2CAL | 050A | — | — | — | — | — | — | — | — | — | — | PGACAL<5:0> | | | | | | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-21: ANALOG COMPARATOR REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--------|--------|---------|---------|-------------|--------|---------|-------|--------|--------|-------|-------|---------|--------|--------|-------|------------|
| CMP1CON | 0540 | CMPON | — | CMPSIDL | HYSSEL1 | HYSSEL0 | FLTREN | FCLKSEL | — | INSEL1 | INSEL0 | — | HYPOL | CMPSTAT | ALTINP | CMPPOL | — | 0000 |
| CMP1DAC | 0542 | — | — | — | — | CMREF<11:0> | | | | | | | | | | | | 0000 |
| CMP2CON | 0544 | CMPON | — | CMPSIDL | HYSSEL1 | HYSSEL0 | FLTREN | FCLKSEL | — | INSEL1 | INSEL0 | — | HYPOL | CMPSTAT | ALTINP | CMPPOL | — | 0000 |
| CMP2DAC | 0546 | — | — | — | — | CMREF<11:0> | | | | | | | | | | | | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: PORTA REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|------------|-------|-----------|-------|-------|------------|
| TRISA | 0E00 | — | — | — | — | — | — | — | — | — | — | — | TRISA<4:0> | | | | 001F | |
| PORTA | 0E02 | — | — | — | — | — | — | — | — | — | — | — | RA<4:0> | | | | 0000 | |
| LATA | 0E04 | — | — | — | — | — | — | — | — | — | — | — | LATA<4:0> | | | | 0000 | |
| ODCA | 0E06 | — | — | — | — | — | — | — | — | — | — | — | ODCA<4:0> | | | | 0000 | |
| CNENA | 0E08 | — | — | — | — | — | — | — | — | — | — | — | CNIEA<4:0> | | | | 0000 | |
| CNPUA | 0E0A | — | — | — | — | — | — | — | — | — | — | — | CNPUA<4:0> | | | | 0000 | |
| CNPDA | 0E0C | — | — | — | — | — | — | — | — | — | — | — | CNPDA<4:0> | | | | 0000 | |
| ANSELA | 0E0E | — | — | — | — | — | — | — | — | — | — | — | — | — | ANSA<2:0> | | 0007 | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-23: PORTB REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|-------------|--------|--------|--------|--------|------------|-------|-------|-----------|-------|-------|-------|-------|-------|-------|-------|------------|
| TRISB | 0E10 | TRISB<15:0> | | | | | | | | | | | | | | | | FFFF |
| PORTB | 0E12 | RB<15:0> | | | | | | | | | | | | | | | | xxxx |
| LATB | 0E14 | LATB<15:0> | | | | | | | | | | | | | | | | xxxx |
| ODCB | 0E16 | ODCB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNENB | 0E18 | CNIEB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNPUB | 0E1A | CNPUB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNPDB | 0E1C | CNPDB<15:0> | | | | | | | | | | | | | | | | 0000 |
| ANSELB | 0E1E | — | — | — | — | — | ANSB<10:9> | | — | ANSB<7:0> | | | | | | | 06FF | |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXGS202 FAMILY

4.5.1 PAGED MEMORY SCHEME

The dsPIC33EPXXGS202 architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre- and post-modified Effective Addresses (EAs). The upper half of the base Data Space address is used in conjunction with the Data Space Read Page (DSRPAG) register to form the Program Space Visibility (PSV) address.

The Data Space Read Page (DSRPAG) register is located in the SFR space. Construction of the PSV address is shown in Figure 4-5. When $DSRPAG\langle 9 \rangle = 1$ and the base address bit, $EA\langle 15 \rangle = 1$, the $DSRPAG\langle 8:0 \rangle$ bits are concatenated onto $EA\langle 14:0 \rangle$ to form the 24-bit PSV read address.

The paged memory scheme provides access to multiple 32-Kbyte windows in the PSV memory. The Data Space Read Page register (DSRPAG), in combination with the upper half of the Data Space address, can provide up to 8 Mbytes of PSV address space. The paged data memory space is shown in Figure 4-6.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG.

FIGURE 4-5: PROGRAM SPACE VISIBILITY (PSV) READ ADDRESS GENERATION

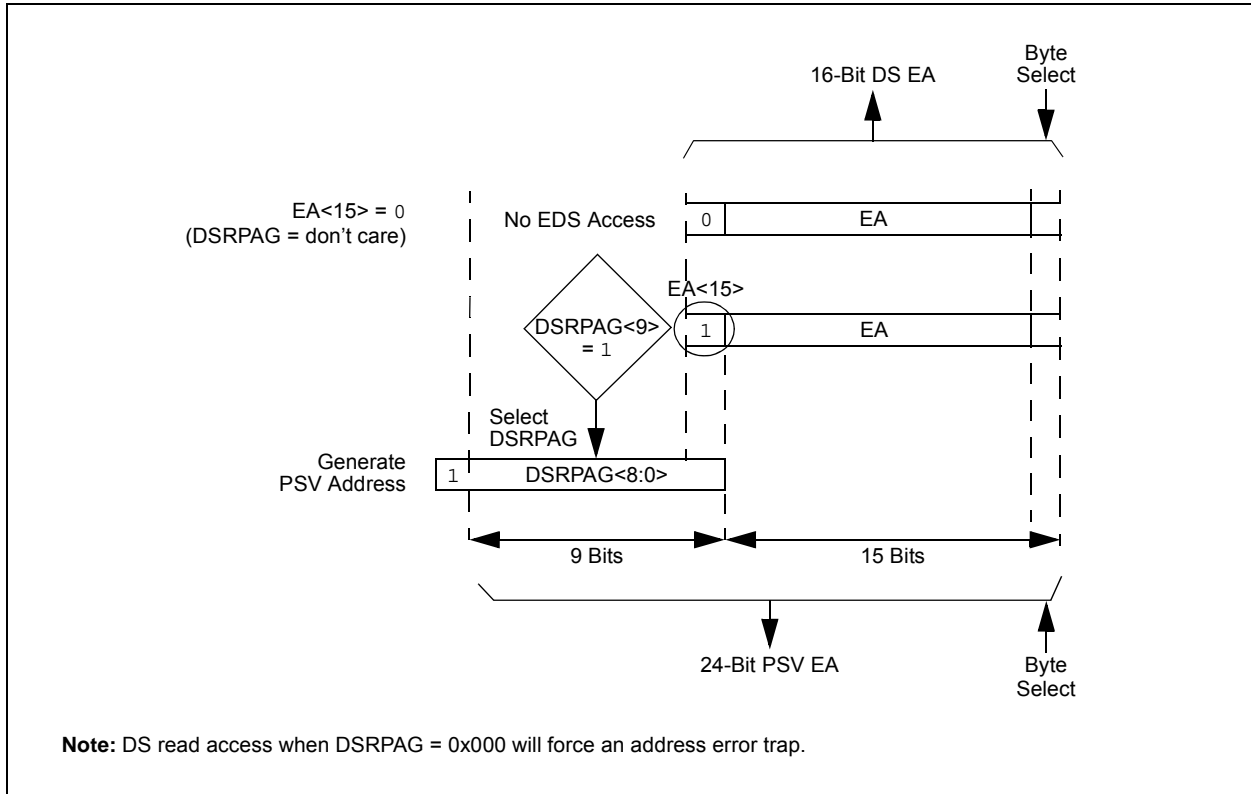
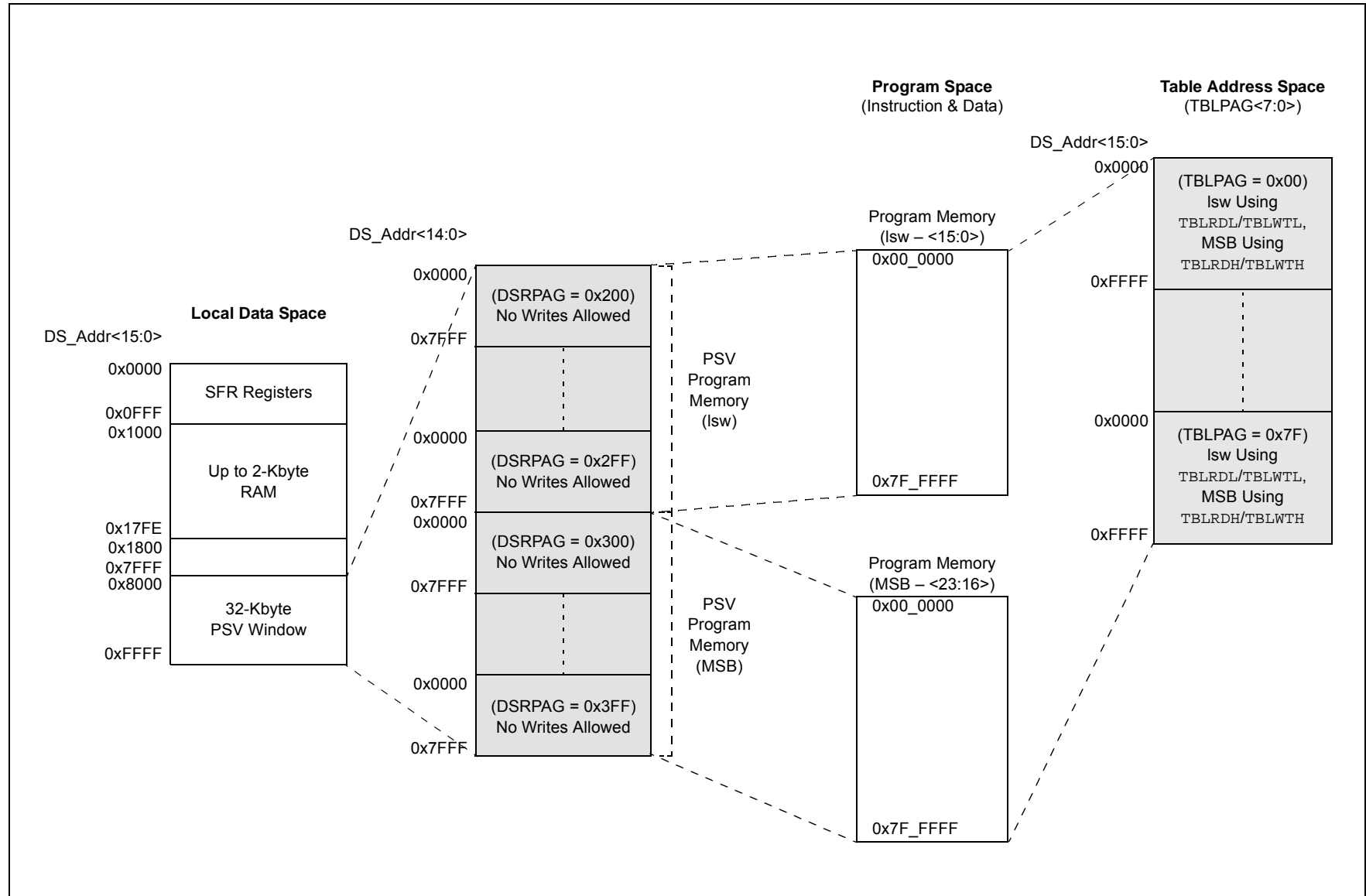


FIGURE 4-6: PAGED DATA MEMORY SPACE



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When a PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the PSV pages can occur at the page boundaries when:

- The initial address, prior to modification, addresses the PSV page
- The EA calculation uses Pre- or Post-Modified Register Indirect Addressing; however, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSRPAG register is incremented and the EA<15> bit is set to keep the base address within the PSV window. When an underflow is detected, the DSRPAG register is decremented and the EA<15> bit is set to keep the

base address within the PSV window. This creates a linear PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0 and PSV spaces. Table 4-24 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSRPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

TABLE 4-24: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0 AND PSV SPACE BOUNDARIES^(2,3,4)

| O/U, R/W | Operation | Before | | | After | | |
|-------------|----------------------------|----------------|--------------|------------------------|----------------|--------------|----------------------------|
| | | DSxPAG | DS EA<15> | Page Description | DSxPAG | DS EA<15> | Page Description |
| O, Read | [++Wn] or | DSRPAG = 0x2FF | 1 | PSV: Last lsw page | DSRPAG = 0x300 | 1 | PSV: First MSB page |
| O, Read | [Wn++] | DSRPAG = 0x3FF | 1 | PSV: Last MSB page | DSRPAG = 0x3FF | 0 | See Note 1 |
| U, Read | [--Wn] or [Wn--] | DSRPAG = 0x001 | 1 | PSV page | DSRPAG = 0x001 | 0 | See Note 1 |
| U, Read | | DSRPAG = 0x200 | 1 | PSV: First lsw page | DSRPAG = 0x200 | 0 | See Note 1 |
| U, Read | | DSRPAG = 0x300 | 1 | PSV: First MSB page | DSRPAG = 0x2FF | 1 | PSV: Last lsw page |

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: The Register Indirect Addressing now addresses a location in the base Data Space (0x0000-0x7FFF).

2: An EDS access, when DSRPAG = 0x000, will generate an address error trap.

3: Only reads from PS are supported using DSRPAG.

4: Pseudolinear Addressing is not supported for large offsets.

dsPIC33EPXXGS202 FAMILY

4.5.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible regardless of the contents of the Data Space Read Page register. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of base Data Space in combination with DSRPAG = 0x000. Consequently, DSRPAG is initialized to 0x001 at Reset.

Note: DSRPAG should not be used to access Page 0. An EDS access with DSRPAG set to 0x000 will generate an address error trap.

The remaining PSV pages are only accessible using the DSRPAG register in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA<15> = 1.

4.5.3 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating the Stack Pointer (for example, creating stack frames).

Note: To protect against misaligned stack accesses, W15<0> is fixed to '0' by the hardware.

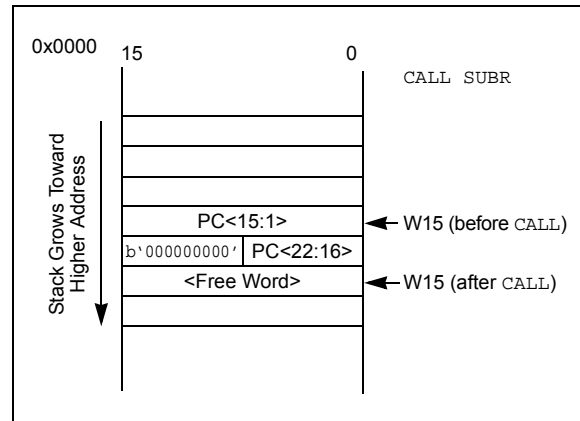
W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EPXXGS202 devices and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

The Software Stack Pointer always points to the first available free word and fills the software stack, working from lower toward higher addresses. Figure 4-7 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-7. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

- Note 1:** To maintain the Software Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore, restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).
- 2:** As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment

FIGURE 4-7: CALL STACK FRAME



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4.6 Instruction Addressing Modes

The addressing modes shown in Table 4-25 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.6.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.6.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a Working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-25: FUNDAMENTAL ADDRESSING MODES SUPPORTED

| Addressing Mode | Description |
|---|---|
| File Register Direct | The address of the file register is specified explicitly. |
| Register Direct | The contents of a register are accessed directly. |
| Register Indirect | The contents of Wn form the Effective Address (EA). |
| Register Indirect Post-Modified | The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value. |
| Register Indirect Pre-Modified | Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA. |
| Register Indirect with Register Offset (Register Indexed) | The sum of Wn and Wb forms the EA. |
| Register Indirect with Literal Offset | The sum of Wn and a literal forms the EA. |

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4.6.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions, and the DSP accumulator class of instructions, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the `MOV` instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit `Wb` (Register Offset) field is shared by both source and destination (but typically, only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.6.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MPY`, `MPY.N`, `MOVSAC` and `MSC`), also referred to as `MAC` instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {`W8`, `W9`, `W10`, `W11`}. For data reads, `W8` and `W9` are always directed to the X RAGU, and `W10` and `W11` are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for `W8` and `W9`, and Y Data Space for `W10` and `W11`.

Note: Register Indirect with Register Offset Addressing mode is available only for `W9` (in X space) and `W11` (in Y space).

In summary, the following addressing modes are supported by the `MAC` class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.6.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, `BRA` (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the `DISI` instruction uses a 14-bit unsigned literal field. In some instructions, such as `ULNK`, the source of an operand or result is implied by the opcode itself. Certain operations, such as a `NOB`, do not have any operands.

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4.7 Modulo Addressing

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a Bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.7.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-2).

Note: Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.7.2 W ADDRESS REGISTER SELECTION

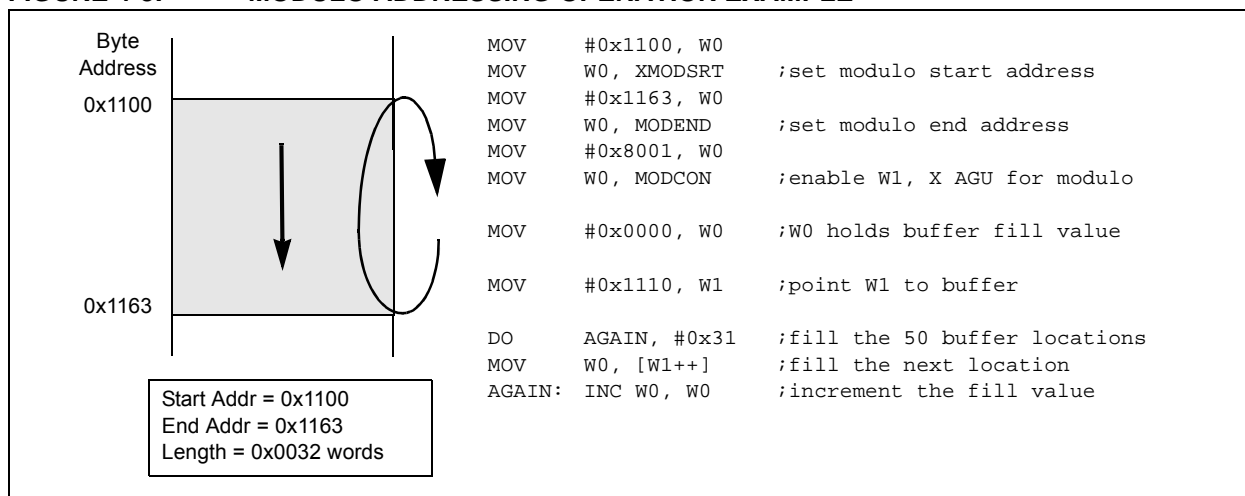
The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags, as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-2). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '1111' and the XMODEN bit is set (MODCON<15>).

The Y Address Space Pointer W register (YWM), to which Modulo Addressing is to be applied, is stored in MODCON<7:4>. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '1111' and the YMODEN bit is set at MODCON<14>.

FIGURE 4-8: MODULO ADDRESSING OPERATION EXAMPLE



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4.7.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note: The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as $[W7 + W2]$) is used, Modulo Addressing correction is performed, but the contents of the register remain unchanged.

4.8 Bit-Reversed Addressing

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.8.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled when all of these conditions are met:

- BWMx bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is $M = 2^N$ bytes, the last 'N' bits of the data buffer start address must be zeros.

$XB<14:0>$ is the Bit-Reversed Addressing modifier, or 'pivot point', which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note: All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note: Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

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FIGURE 4-9: BIT-REVERSED ADDRESSING EXAMPLE

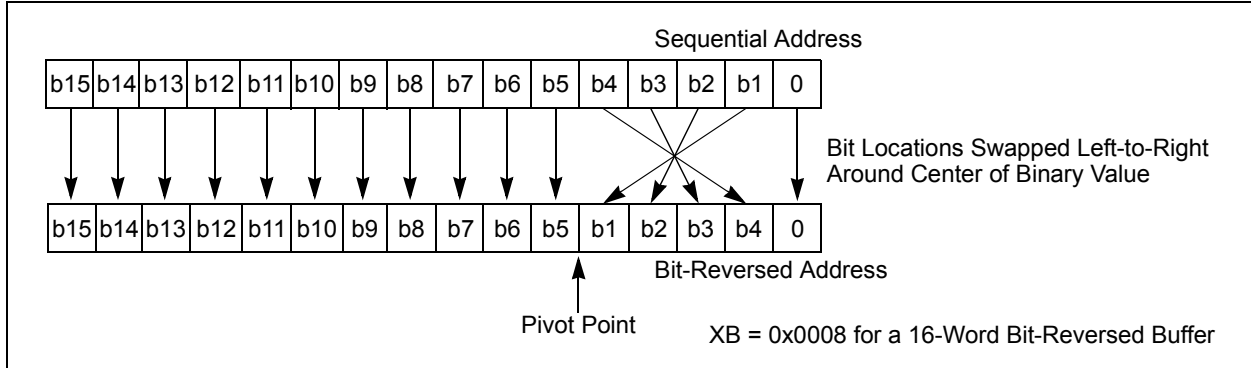


TABLE 4-26: BIT-REVERSED ADDRESSING SEQUENCE (16-ENTRY)

| Normal Address | | | | | Bit-Reversed Address | | | | |
|----------------|----|----|----|---------|----------------------|----|----|----|---------|
| A3 | A2 | A1 | A0 | Decimal | A3 | A2 | A1 | A0 | Decimal |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 8 |
| 0 | 0 | 1 | 0 | 2 | 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 1 | 1 | 3 | 1 | 1 | 0 | 0 | 12 |
| 0 | 1 | 0 | 0 | 4 | 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | 0 | 10 |
| 0 | 1 | 1 | 0 | 6 | 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 | 1 | 1 | 1 | 0 | 14 |
| 1 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 9 | 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 | 0 | 1 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 11 | 1 | 1 | 0 | 1 | 13 |
| 1 | 1 | 0 | 0 | 12 | 0 | 0 | 1 | 1 | 3 |
| 1 | 1 | 0 | 1 | 13 | 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 1 | 0 | 14 | 0 | 1 | 1 | 1 | 7 |
| 1 | 1 | 1 | 1 | 15 | 1 | 1 | 1 | 1 | 15 |

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4.9 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXGS202 family architecture uses a 24-bit wide Program Space (PS) and a 16-bit wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33EPXXGS202 family devices provides two methods by which Program Space can be accessed during operation:

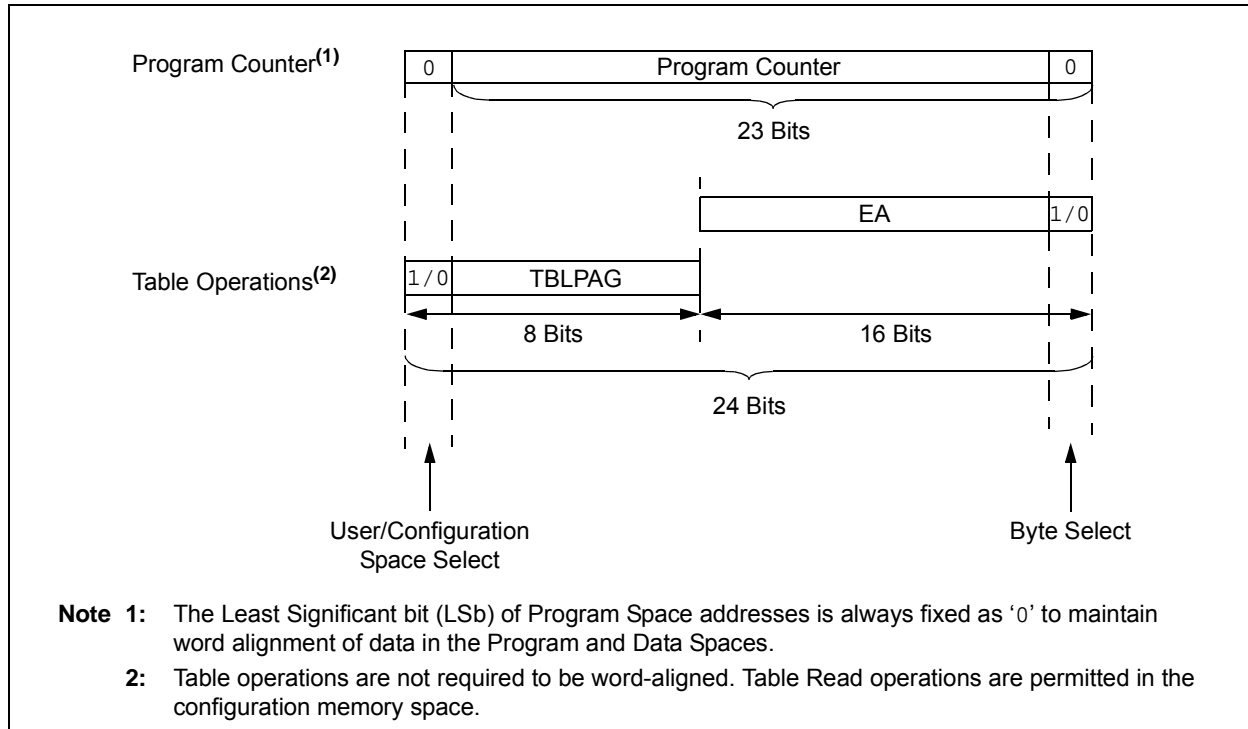
- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

TABLE 4-27: PROGRAM SPACE ADDRESS CONSTRUCTION

| Access Type | Access Space | Program Space Address | | | | |
|--|---------------|-----------------------------------|----------|------------------------|--------|-----|
| | | <23> | <22:16> | <15> | <14:1> | <0> |
| Instruction Access (Code Execution) | User | 0 | PC<22:1> | | | 0 |
| | | 0xxx xxxxx xxxxx xxxxx xxxxx xxx0 | | | | |
| TBLRD/TBLWT (Byte/Word Read/Write) | User | TBLPAG<7:0> | | Data EA<15:0> | | |
| | | 0xxx xxxxx | | xxxx xxxxx xxxxx xxxxx | | |
| | Configuration | TBLPAG<7:0> | | Data EA<15:0> | | |
| | | 1xxx xxxxx | | xxxx xxxxx xxxxx xxxxx | | |

FIGURE 4-10: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



4.9.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The `TBLRDL` and `TBLWTL` instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The `TBLRDH` and `TBLWTH` instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. `TBLRDL` and `TBLWTL` access the space that contains the least significant data word. `TBLRDH` and `TBLWTH` access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

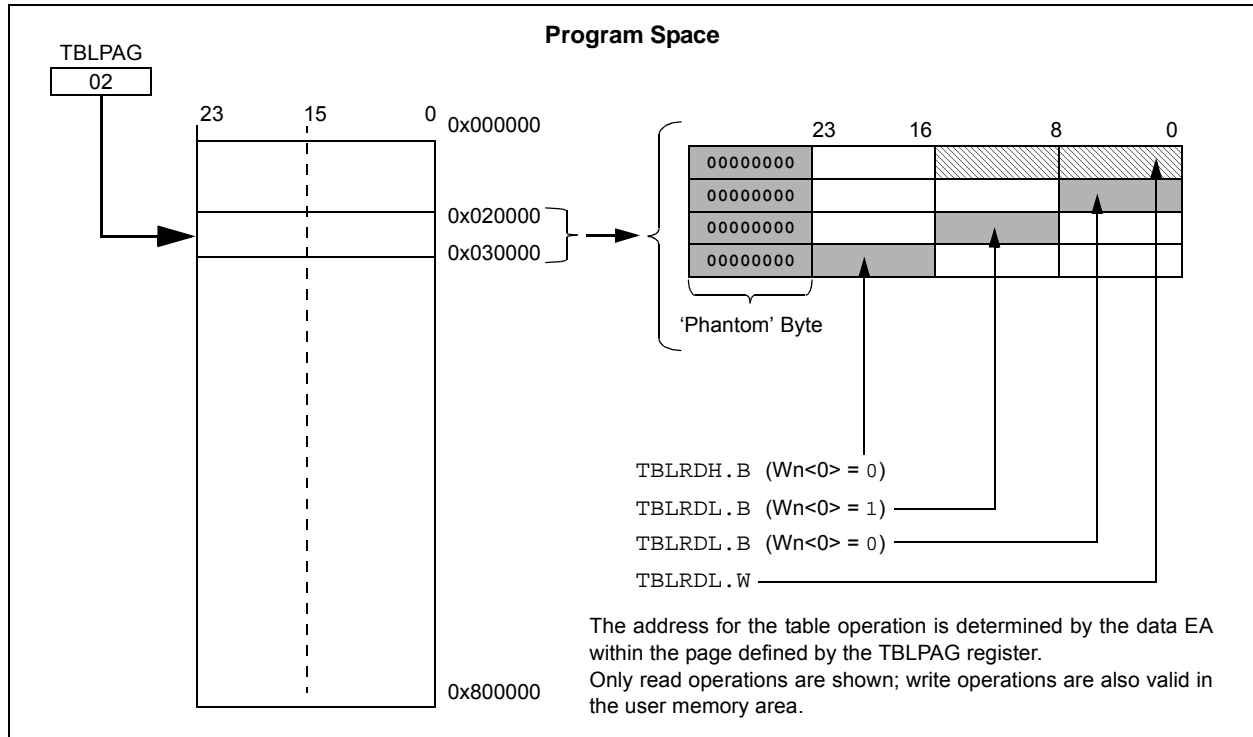
- `TBLRDL` (Table Read Low):
 - In Word mode, this instruction maps the lower word of the Program Space location ($P<15:0>$) to a data address ($D<15:0>$)
 - In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

- `TBLRDH` (Table Read High):
 - In Word mode, this instruction maps the entire upper word of a program address ($P<23:16>$) to a data address. The 'phantom' byte ($D<15:8>$) is always '0'.
 - In Byte mode, this instruction maps the upper or lower byte of the program word to $D<7:0>$ of the data address in the `TBLRDL` instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, `TBLWTH` and `TBLWTL`, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in [Section 5.0 "Flash Program Memory"](#).

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (`TBLPAG`). `TBLPAG` covers the entire program memory space of the device, including user application and configuration spaces. When $TBLPAG<7> = 0$, the table page is located in the user memory space. When $TBLPAG<7> = 1$, the page is located in configuration space.

FIGURE 4-11: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



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NOTES:

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5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Flash Programming” (DS70609) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 family devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in three ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)
- Run-Time Self-Programming (RTSP)

ICSP allows for a dsPIC33EPXXGS202 family device to be serially programmed while in the end application circuit. This is done with a programming clock and programming data (PGECx/PGEDx) line, and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the

device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

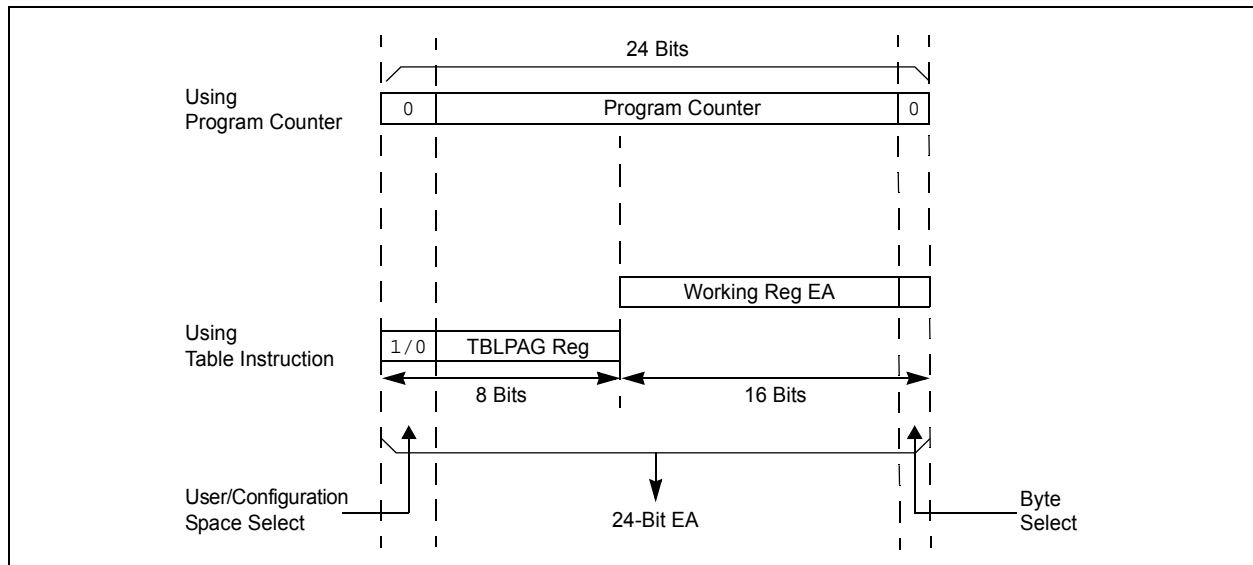
Enhanced In-Circuit Serial Programming uses an on-board bootloader, known as the Program Executive, to manage the programming process. Using an SPI data frame format, the Program Executive can erase, program and verify program memory. For more information on Enhanced ICSP, see the device programming specification.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data with a single program memory word and erase program memory in blocks or ‘pages’ of 512 instructions (1536 bytes) at a time.

5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in **Figure 5-1**. The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes. The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



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5.2 RTSP Operation

The dsPIC33EPXXGS202 family Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a single page (8 rows or 512 instructions) of memory at a time and to program one row at a time. It is possible to program two instructions at a time as well.

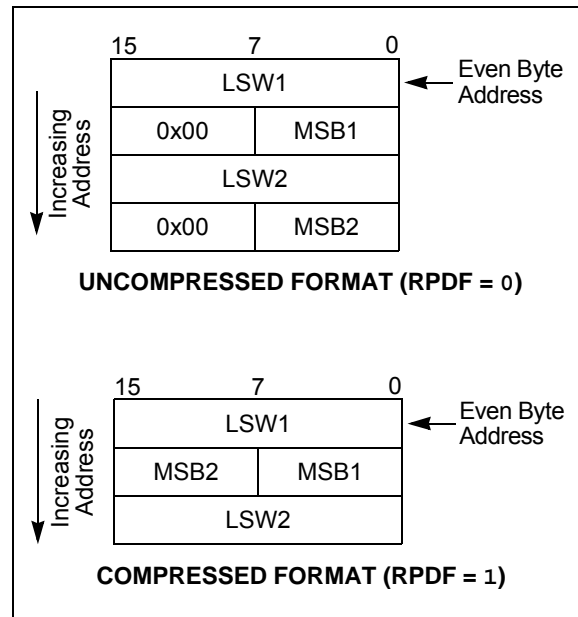
The page erase and single row write blocks are edge-aligned, from the beginning of program memory on boundaries of 1536 bytes and 192 bytes, respectively. Figure 25-14 in Section 25.0 “Electrical Characteristics” lists the typical erase and programming times.

Row programming is performed by loading 192 bytes into data memory and then loading the address of the first byte in that row into the NVMSRCADR register. Once the write has been initiated, the device will automatically load the write latches and increment the NVMSRCADR and the NVMADR(U) registers until all bytes have been programmed. The RPDF bit (NVMCON<9>) selects the format of the stored data in RAM to be either compressed or uncompressed. See Figure 5-2 for data formatting. Compressed data helps to reduce the amount of required RAM by using the upper byte of the second word for the MSB of the second instruction.

The basic sequence for RTSP word programming is to use the TBLWTL and TBLWTH instructions to load two of the 24-bit instructions into the write latches found in configuration memory space. Refer to Figure 4-1 through Figure 4-3 for write latch addresses. Programming is performed by unlocking and setting the control bits in the NVMCON register.

All erase and program operations may optionally use the NVM interrupt to signal the successful completion of the operation.

FIGURE 5-2: UNCOMPRESSED/COMPRESSED FORMAT



5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished. Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of Program Flash Memory (PFM) at a time on every other word address boundary (0x000000, 0x000004, 0x000008, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change. For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS.

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5.4 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

5.4.1 KEY RESOURCES

- **“Flash Programming”** (DS70609) in the *“dsPIC33/PIC24 Family Reference Manual”*,
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

5.5 Control Registers

Five SFRs are used to write and erase the Program Flash Memory: NVMCON, NVMKEY, NVMADR, NVMADRU and NVMSRCADR.

The NVMCON register ([Register 5-1](#)) selects the operation to be performed (page erase, word/row program) and initiates the program/erase cycle.

NVMKEY ([Register 5-4](#)) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word/row for programming operations, or the selected page for erase operations. The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

For row programming operation, data to be written to Program Flash Memory is written into data memory space (RAM) at an address defined by the NVMSRCADR register (location of first element in row programming data).

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REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

| | | | | | | | |
|-----------------------|----------------------|----------------------|------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| R/SO-0 ⁽¹⁾ | R/W-0 ⁽¹⁾ | R/W-0 ⁽¹⁾ | R/W-0 | U-0 | U-0 | R/W-0 | R/C-0 |
| WR | WREN | WRERR | NVMSIDL ⁽²⁾ | — | — | RPDF | URERR |
| bit 15 | | | | | | | bit 8 |
| U-0 | U-0 | U-0 | U-0 | R/W-0 ⁽¹⁾ | R/W-0 ⁽¹⁾ | R/W-0 ⁽¹⁾ | R/W-0 ⁽¹⁾ |
| — | — | — | — | NVMOP3 ^(3,4) | NVMOP2 ^(3,4) | NVMOP1 ^(3,4) | NVMOP0 ^(3,4) |
| bit 7 | | | | | | | bit 0 |

| | | |
|-------------------|-------------------|--|
| Legend: | C = Clearable bit | SO = Settable Only bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15 **WR:** Write Control bit⁽¹⁾
 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete
 0 = Program or erase operation is complete and inactive
- bit 14 **WREN:** Write Enable bit⁽¹⁾
 1 = Enables Flash program/erase operations
 0 = Inhibits Flash program/erase operations
- bit 13 **WRERR:** Write Sequence Error Flag bit⁽¹⁾
 1 = An improper program or erase sequence attempt, or termination has occurred (bit is set automatically on any set attempt of the WR bit)
 0 = The program or erase operation completed normally
- bit 12 **NVMSIDL:** NVM Stop in Idle Control bit⁽²⁾
 1 = Flash voltage regulator goes into Standby mode during Idle mode
 0 = Flash voltage regulator is active during Idle mode
- bit 11-10 **Unimplemented:** Read as '0'
- bit 9 **RPDF:** Row Programming Data Format
 1 = Row data to be stored in RAM in compressed format
 0 = Row data to be stored in RAM in uncompressed format
- bit 8 **URERR:** Row Programming Data Underrun Error bit
 1 = Indicates row programming operation has been terminated
 0 = No data underrun error is detected
- bit 7-4 **Unimplemented:** Read as '0'

- Note 1:** These bits can only be reset on a POR.
- 2:** If this bit is set, power consumption will be further reduced (IDLE), and upon exiting Idle mode, there is a delay (TVREG) before Flash memory becomes operational.
- 3:** All other combinations of NVMOP<3:0> are unimplemented.
- 4:** Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.
- 5:** Two adjacent words on a 4-word boundary are programmed during execution of this operation.

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REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER (CONTINUED)

bit 3-0 **NVMOP<3:0>**: NVM Operation Select bits^(1,3,4)

- 1111 = Reserved
-
-
- 0101 = Reserved
- 0100 = Reserved
- 0011 = Memory page erase operation
- 0010 = Memory row program operation
- 0001 = Memory double-word program operation⁽⁵⁾
- 0000 = Reserved

- Note 1:** These bits can only be reset on a POR.
- 2:** If this bit is set, power consumption will be further reduced (IDLE), and upon exiting Idle mode, there is a delay (TVREG) before Flash memory becomes operational.
- 3:** All other combinations of NVMOP<3:0> are unimplemented.
- 4:** Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.
- 5:** Two adjacent words on a 4-word boundary are programmed during execution of this operation.

REGISTER 5-2: NVMADR: NONVOLATILE MEMORY LOWER ADDRESS REGISTER

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| NVMADR<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| NVMADR<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-0 **NVMADR<15:0>**: Nonvolatile Memory Lower Write Address bits
 Selects the lower 16 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

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REGISTER 5-3: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| NVMADRU<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'
 bit 7-0 **NVMADRU<23:16>:** Nonvolatile Memory Upper Write Address bits
 Selects the upper 8 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY REGISTER

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------------|-----|-----|-----|-----|-----|-----|-------|
| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| NVMKEY<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'
 bit 7-0 **NVMKEY<7:0>:** Key Register bits (write-only)

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REGISTER 5-5: NVMSRCADRL: NVM SOURCE DATA ADDRESS LOW REGISTER

| | | | | | | | |
|-----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMSRCADR<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMSRCADR<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-0 **NVMSRCADR<15:0>**: Source Data Address bits
 The RAM address of the data to be programmed into Flash when the NVMOP<3:0> bits are set to row programming.

REGISTER 5-6: NVMSRCADRH: NVM SOURCE DATA ADDRESS HIGH REGISTER

| | | | | | | | |
|------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMSRCADR<31:24> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMSRCADR<23:16> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-0 **NVMSRCADR<31:16>**: Source Data Address bits
 The RAM address of the data to be programmed into Flash when the NVMOP<3:0> bits are set to row programming. These bits must be always programmed to zero.

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NOTES:

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6.0 RESETS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Reset” (DS70602) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
 - Illegal Opcode Reset
 - Uninitialized W Register Reset
 - Security Reset

A simplified block diagram of the Reset module is shown in **Figure 6-1**.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state, and some are unaffected.

Note: Refer to the specific peripheral section or **Section 4.0 “Memory Organization”** of this manual for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see **Register 6-1**).

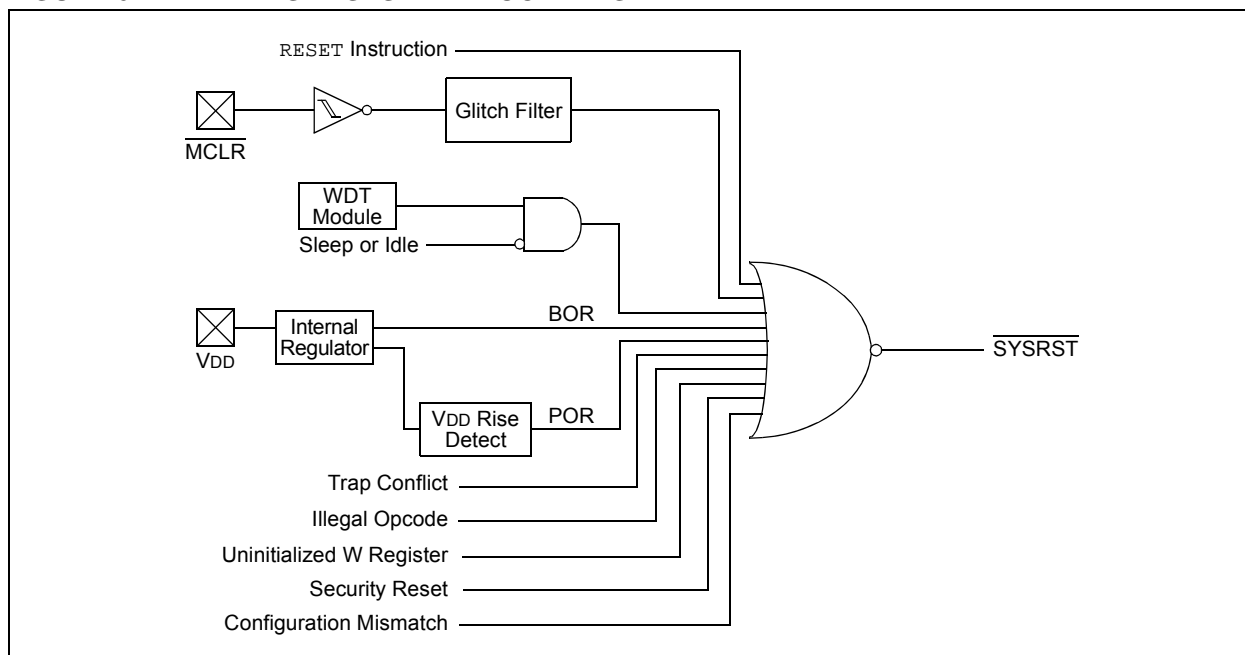
A POR clears all the bits, except for the BOR and POR bits (RCON<1:0>) that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

For all Resets, the default clock source is determined by the FNOSC<2:0> bits in the FOSCSEL Configuration register. The value of the FNOSCx bits is loaded into the NOSC<2:0> (OSCCON<10:8>) bits on Reset, which in turn, initializes the system clock.

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM



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6.1 Reset Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

6.1.1 KEY RESOURCES

- **“Reset”** (DS70602) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

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REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

| | | | | | | | |
|--------|--------|-----|-----|--------|-----|-------|-------|
| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| TRAPR | IOPUWR | — | — | VREGSF | — | CM | VREGS |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-------|-----------------------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
| EXTR | SWR | SWDTEN ⁽²⁾ | WDTO | SLEEP | IDLE | BOR | POR |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **TRAPR:** Trap Reset Flag bit
 1 = A Trap Conflict Reset has occurred
 0 = A Trap Conflict Reset has not occurred
- bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Register Access Reset Flag bit
 1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
 0 = An illegal opcode or Uninitialized W register Reset has not occurred
- bit 13-12 **Unimplemented:** Read as '0'
- bit 11 **VREGSF:** Flash Voltage Regulator Standby During Sleep bit
 1 = Flash voltage regulator is active during Sleep
 0 = Flash voltage regulator goes into Standby mode during Sleep
- bit 10 **Unimplemented:** Read as '0'
- bit 9 **CM:** Configuration Mismatch Flag bit
 1 = A Configuration Mismatch Reset has occurred.
 0 = A Configuration Mismatch Reset has not occurred
- bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
 1 = Voltage regulator is active during Sleep
 0 = Voltage regulator goes into Standby mode during Sleep
- bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
 1 = A Master Clear (pin) Reset has occurred
 0 = A Master Clear (pin) Reset has not occurred
- bit 6 **SWR:** Software RESET (Instruction) Flag bit
 1 = A RESET instruction has been executed
 0 = A RESET instruction has not been executed
- bit 5 **SWDTEN:** Software Enable/Disable of WDT bit⁽²⁾
 1 = WDT is enabled
 0 = WDT is disabled
- bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
 1 = WDT time-out has occurred
 0 = WDT time-out has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the WDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

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REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

| | |
|-------|---|
| bit 3 | SLEEP: Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode 0 = Device has not been in Sleep mode |
| bit 2 | IDLE: Wake-up from Idle Flag bit 1 = Device has been in Idle mode 0 = Device has not been in Idle mode |
| bit 1 | BOR: Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred |
| bit 0 | POR: Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred |

- Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the WDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Interrupts**” (DS70000600) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXGS202 family CPU.

The interrupt controller has the following features:

- Six Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Fixed Interrupt Entry and Return Latencies
- Alternate Interrupt Vector Table (AIVT) for Debug Support

7.1 Interrupt Vector Table

The dsPIC33EPXXGS202 family Interrupt Vector Table (IVT), shown in [Figure 7-1](#), resides in program memory, starting at location, 000004h. The IVT contains six non-maskable trap vectors and up to fifty sources of interrupts. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT), shown in [Figure 7-2](#), is available only when the Boot Segment (BS) is defined and the AIVT has been enabled. To enable the Alternate Interrupt Vector Table, the Configuration bit, AIVTDIS in the FSEC register, must be programmed and the AIVTEN bit must be set (INTCON2<8> = 1). When the AIVT is enabled, all interrupt and exception processes use the alternate vectors instead of the default vectors. The AIVT begins at the start of the last page of the Boot Segment, defined by BSLIM<12:0>. The second half of the page is no longer usable space. The Boot Segment must be at least 2 pages to enable the AIVT.

Note: Although the Boot Segment must be enabled in order to enable the AIVT, application code does not need to be present inside of the Boot Segment. The AIVT (and IVT) will inherit the Boot Segment code protection.

The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXGS202 family devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

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FIGURE 7-1: dsPIC33EPXXGS202 FAMILY INTERRUPT VECTOR TABLE

| | | |
|----------------------|-----------------------------|----------|
| | Reset – GOTO Instruction | 0x000000 |
| | Reset – GOTO Address | 0x000002 |
| | Oscillator Fail Trap Vector | 0x000004 |
| | Address Error Trap Vector | 0x000006 |
| | Generic Hard Trap Vector | 0x000008 |
| | Stack Error Trap Vector | 0x00000A |
| | Math Error Trap Vector | 0x00000C |
| | Reserved | 0x00000E |
| | Generic Soft Trap Vector | 0x000010 |
| | Reserved | 0x000012 |
| | Interrupt Vector 0 | 0x000014 |
| | Interrupt Vector 1 | 0x000016 |
| | ⋮ | ⋮ |
| | ⋮ | ⋮ |
| | ⋮ | ⋮ |
| | Interrupt Vector 52 | 0x00007C |
| | Interrupt Vector 53 | 0x00007E |
| | Interrupt Vector 54 | 0x000080 |
| | ⋮ | ⋮ |
| | ⋮ | ⋮ |
| | ⋮ | ⋮ |
| | Interrupt Vector 116 | 0x0000FC |
| | Interrupt Vector 117 | 0x0000FE |
| | Interrupt Vector 118 | 0x000100 |
| | Interrupt Vector 119 | 0x000102 |
| | Interrupt Vector 120 | 0x000104 |
| | ⋮ | ⋮ |
| | ⋮ | ⋮ |
| | ⋮ | ⋮ |
| | Interrupt Vector 244 | 0x0001FC |
| Interrupt Vector 245 | 0x0001FE | |
| START OF CODE | 0x000200 | |

See [Table 7-1](#) for Interrupt Vector Details

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FIGURE 7-2: dsPIC33EPXXGS202 FAMILY ALTERNATE INTERRUPT VECTOR TABLE

| | | |
|---|---------------------------------------|---------------------------------------|
| ↓ Decreasing Natural Order Priority AINT ↑ | Reserved | BSLIM<12:0> ⁽¹⁾ + 0x000000 |
| | Reserved | BSLIM<12:0> ⁽¹⁾ + 0x000002 |
| | Oscillator Fail Trap Vector | BSLIM<12:0> ⁽¹⁾ + 0x000004 |
| | Address Error Trap Vector | BSLIM<12:0> ⁽¹⁾ + 0x000006 |
| | Generic Hard Trap Vector | BSLIM<12:0> ⁽¹⁾ + 0x000008 |
| | Stack Error Trap Vector | BSLIM<12:0> ⁽¹⁾ + 0x00000A |
| | Math Error Trap Vector | BSLIM<12:0> ⁽¹⁾ + 0x00000C |
| | Reserved | BSLIM<12:0> ⁽¹⁾ + 0x00000E |
| | Generic Soft Trap Vector | BSLIM<12:0> ⁽¹⁾ + 0x000010 |
| | Reserved | BSLIM<12:0> ⁽¹⁾ + 0x000012 |
| | Interrupt Vector 0 | BSLIM<12:0> ⁽¹⁾ + 0x000014 |
| | Interrupt Vector 1 | BSLIM<12:0> ⁽¹⁾ + 0x000016 |
| | : | : |
| | : | : |
| | : | : |
| | Interrupt Vector 52 | BSLIM<12:0> ⁽¹⁾ + 0x00007C |
| | Interrupt Vector 53 | BSLIM<12:0> ⁽¹⁾ + 0x00007E |
| | Interrupt Vector 54 | BSLIM<12:0> ⁽¹⁾ + 0x000080 |
| | : | : |
| | : | : |
| | : | : |
| | Interrupt Vector 116 | BSLIM<12:0> ⁽¹⁾ + 0x0000FC |
| | Interrupt Vector 117 | BSLIM<12:0> ⁽¹⁾ + 0x0000FE |
| | Interrupt Vector 118 | BSLIM<12:0> ⁽¹⁾ + 0x000100 |
| | Interrupt Vector 119 | BSLIM<12:0> ⁽¹⁾ + 0x000102 |
| Interrupt Vector 120 | BSLIM<12:0> ⁽¹⁾ + 0x000104 | |
| : | : | |
| : | : | |
| : | : | |
| Interrupt Vector 244 | BSLIM<12:0> ⁽¹⁾ + 0x0001FC | |
| Interrupt Vector 245 | BSLIM<12:0> ⁽¹⁾ + 0x0001FE | |

See [Table 7-1](#) for Interrupt Vector Details

Note 1: The address depends on the size of the Boot Segment defined by BSLIM<12:0>.
 $[(BSLIM<12:0> - 1) \times 0x400] + \text{Offset}$.

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TABLE 7-1: INTERRUPT VECTOR DETAILS

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|--------------------------------------|----------|---------|-------------------|------------------------|----------|--------------|
| | | | | Flag | Enable | Priority |
| Highest Natural Order Priority | | | | | | |
| INT0 – External Interrupt 0 | 8 | 0 | 0x000014 | IFS0<0> | IEC0<0> | IPC0<2:0> |
| IC1 – Input Capture 1 | 9 | 1 | 0x000016 | IFS0<1> | IEC0<1> | IPC0<6:4> |
| OC1 – Output Compare 1 | 10 | 2 | 0x000018 | IFS0<2> | IEC0<2> | IPC0<10:8> |
| T1 – Timer1 | 11 | 3 | 0x00001A | IFS0<3> | IEC0<3> | IPC0<14:12> |
| Reserved | 12–14 | 4–6 | 0x00001C–0x000020 | — | — | — |
| T2 – Timer2 | 15 | 7 | 0x000022 | IFS0<7> | IEC0<7> | IPC1<14:12> |
| T3 – Timer3 | 16 | 8 | 0x000024 | IFS0<8> | IEC0<8> | IPC2<2:0> |
| SPI1E – SPI1 Error | 17 | 9 | 0x000026 | IFS0<9> | IEC0<9> | IPC2<6:4> |
| SPI1 – SPI1 Transfer Done | 18 | 10 | 0x000028 | IFS0<10> | IEC0<10> | IPC2<10:8> |
| U1RX – UART1 Receiver | 19 | 11 | 0x00002A | IFS0<11> | IEC0<11> | IPC2<14:12> |
| U1TX – UART1 Transmitter | 20 | 12 | 0x00002C | IFS0<12> | IEC0<12> | IPC3<2:0> |
| ADC – ADC Global Convert Done | 21 | 13 | 0x00002E | IFS0<13> | IEC0<13> | IPC3<6:4> |
| Reserved | 22 | 14 | 0x000030 | — | — | — |
| NVM – NVM Write Complete | 23 | 15 | 0x000032 | IFS0<15> | IEC0<15> | IPC3<14:12> |
| SI2C1 – I2C1 Slave Event | 24 | 16 | 0x000034 | IFS1<0> | IEC1<0> | IPC4<2:0> |
| MI2C1 – I2C1 Master Event | 25 | 17 | 0x000036 | IFS1<1> | IEC1<1> | IPC4<6:4> |
| CMP1 – Analog Comparator 1 Interrupt | 26 | 18 | 0x000038 | IFS1<2> | IEC1<2> | IPC4<10:8> |
| CN – Input Change Interrupt | 27 | 19 | 0x00003A | IFS1<3> | IEC1<3> | IPC4<14:12> |
| INT1 – External Interrupt 1 | 28 | 20 | 0x00003C | IFS1<4> | IEC1<4> | IPC5<2:0> |
| Reserved | 29-36 | 21-28 | 0x00003E–0x00004C | — | — | — |
| INT2 – External Interrupt 2 | 37 | 29 | 0x00004E | IFS1<13> | IEC1<13> | IPC7<6:4> |
| Reserved | 38-64 | 30-56 | 0x000050–0x000084 | — | — | — |
| PSEM – PWM Special Event Match | 65 | 57 | 0x000086 | IFS3<9> | IEC3<9> | IPC14<6:4> |
| Reserved | 63-72 | 55-64 | 0x000088–0x000094 | — | — | — |
| U1E – UART1 Error Interrupt | 73 | 65 | 0x000096 | IFS4<1> | IEC4<1> | IPC16<6:4> |
| Reserved | 74-80 | 66-72 | 0x000098–0x0000A4 | — | — | — |
| PWM Secondary Special Event Match | 81 | 73 | 0x0000A6 | IFS4<9> | IEC4<9> | IPC18<6:4> |
| Reserved | 82-101 | 74-93 | 0x0000A8–0x0000CE | — | — | — |
| PWM1 – PWM1 Interrupt | 102 | 94 | 0x0000D0 | IFS5<14> | IEC5<14> | IPC23<10:8> |
| PWM2 – PWM2 Interrupt | 103 | 95 | 0x0000D2 | IFS5<15> | IEC5<15> | IPC23<14:12> |
| PWM3 – PWM3 Interrupt | 104 | 96 | 0x0000D4 | IFS6<0> | IEC6<0> | IPC24<2:0> |
| Reserved | 105-110 | 97-102 | 0x0000D6–0x0000E0 | — | — | — |
| CMP2 – Analog Comparator 2 Interrupt | 111 | 103 | 0x0000E2 | IFS6<7> | IEC6<7> | IPC25<14:12> |
| Reserved | 112-117 | 104-109 | 0x0000E4–0x0000EE | — | — | — |
| AN0 Conversion Done | 118 | 110 | 0x0000F0 | IFS6<14> | IEC6<14> | IPC27<10:8> |
| AN1 Conversion Done | 119 | 111 | 0x0000F2 | IFS6<15> | IEC6<15> | IPC27<14:12> |
| AN2 Conversion Done | 120 | 112 | 0x0000F4 | IFS7<0> | IEC7<0> | IPC28<2:0> |
| AN3 Conversion Done | 121 | 113 | 0x0000F6 | IFS7<1> | IEC7<1> | IPC28<6:4> |
| AN4 Conversion Done | 122 | 114 | 0x0000F8 | IFS7<2> | IEC7<2> | IPC28<10:8> |
| AN5 Conversion Done | 123 | 115 | 0x0000FA | IFS7<3> | IEC7<3> | IPC28<14:12> |
| AN6 Conversion Done | 124 | 116 | 0x0000FC | IFS7<4> | IEC7<4> | IPC29<2:0> |
| AN7 Conversion Done | 125 | 117 | 0x0000FE | IFS7<5> | IEC7<5> | IPC29<6:4> |

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TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|-----------------------------------|----------|---------|-------------------|------------------------|-----------|--------------|
| | | | | Flag | Enable | Priority |
| Reserved | 126-158 | 118-150 | 0x000100-0x000140 | — | — | — |
| AN8 Conversion Done | 159 | 151 | 0x000142 | IFS9<7> | IEC9<7> | IPC37<14:12> |
| AN9 Conversion Done | 160 | 152 | 0x000144 | IFS9<8> | IEC9<8> | IPC38<2:0> |
| AN10 Conversion Done | 161 | 153 | 0x000146 | IFS9<9> | IEC9<9> | IPC38<6:4> |
| AN11 Conversion Done | 162 | 154 | 0x000148 | IFS9<10> | IEC9<10> | IPC38<10:8> |
| AN12 Conversion Done | 163 | 155 | 0x00014A | IFS9<11> | IEC9<11> | IPC38<14:12> |
| AN13 Conversion Done | 164 | 156 | 0x00014C | IFS9<12> | IEC9<12> | IPC39<2:0> |
| AN14 Conversion Done | 165 | 157 | 0x00014E | IFS9<13> | IEC9<13> | IPC39<6:4> |
| Reserved | 166-180 | 158-172 | 0x000150-0x00016C | — | — | — |
| I2C1 – I2C1 Bus Collision | 181 | 173 | 0x00016E | IFS10<13> | IEC10<13> | IPC43<6:4> |
| Reserved | 182-184 | 174-176 | 0x000170-0x000174 | — | — | — |
| ADCMP0 – ADC Digital Comparator 0 | 185 | 177 | 0x000176 | IFS11<1> | IEC11<1> | IPC44<6:4> |
| ADCMP1 – ADC Digital Comparator 1 | 186 | 178 | 0x000178 | IFS11<2> | IEC11<2> | IPC44<10:8> |
| ADFL0 – ADC Filter 0 | 187 | 179 | 0x00017A | IFS11<3> | IEC11<3> | IPC44<14:12> |
| Reserved | 188-253 | 180-245 | 0x00017C-0x0001FE | — | — | — |

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7.3 Interrupt Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

7.3.1 KEY RESOURCES

- “**Interrupts**” (DS70000600) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

7.4 Interrupt Control and Status Registers

dsPIC33EPXXGS202 family devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- INTTREG

7.4.1 INTCON1 THROUGH INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS), as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior, contains the Global Interrupt Enable bit (GIE) and the Alternate Interrupt Vector Table Enable bit (AIVTEN).

INTCON3 contains the status flags for the Auxiliary PLL and DO stack overflow status trap sources.

The INTCON4 register contains the Software Generated Hard Trap Status bit (SGHT).

7.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

7.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt sources can be assigned to one of seven priority levels.

7.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number (VECNUM<7:0>) and Interrupt Level bits (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in [Table 7-1](#). For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INTOIF bit is found in IFS0<0>, the INTOIE bit in IEC0<0> and the INTOIP<2:0> bits in the first position of IPC0 (IPC0<2:0>).

7.4.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers refer to “**CPU**” (DS70359) in the “*dsPIC33/PIC24 Family Reference Manual*”.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in [Register 7-3](#) through [Register 7-7](#) in the following pages.

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REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

| | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/C-0 | R/C-0 | R-0 | R/W-0 |
| OA | OB | SA | SB | OAB | SAB | DA | DC |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|----------------------|----------------------|----------------------|-----|-------|-------|-------|-------|
| R/W-0 ⁽³⁾ | R/W-0 ⁽³⁾ | R/W-0 ⁽³⁾ | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| IPL2 ⁽²⁾ | IPL1 ⁽²⁾ | IPL0 ⁽²⁾ | RA | N | OV | Z | C |
| bit 7 | | | | | | bit 0 | |

| | |
|-------------------|------------------------------------|
| Legend: | C = Clearable bit |
| R = Readable bit | W = Writable bit |
| -n = Value at POR | '1' = Bit is set |
| | U = Unimplemented bit, read as '0' |
| | '0' = Bit is cleared |
| | x = Bit is unknown |

bit 7-5 **IPL<2:0>**: CPU Interrupt Priority Level Status bits^(2,3)

111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

- Note 1:** For complete register details, see [Register 3-1](#).
- 2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- 3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

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REGISTER 7-2: CORCON: CORE CONTROL REGISTER⁽¹⁾

| | | | | | | | |
|--------|-----|-------|-------|-------|-----|-----|-------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
| VAR | — | US1 | US0 | EDT | DL2 | DL1 | DL0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-------|-------|--------|---------------------|-----|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R-0 | R/W-0 | R/W-0 |
| SATA | SATB | SATDW | ACCSAT | IPL3 ⁽²⁾ | SFA | RND | IF |
| bit 7 | | | | | | | bit 0 |

| | |
|-------------------|------------------------------------|
| Legend: | C = Clearable bit |
| R = Readable bit | W = Writable bit |
| -n = Value at POR | '1' = Bit is set |
| | U = Unimplemented bit, read as '0' |
| | '0' = Bit is cleared |
| | x = Bit is unknown |

bit 15 **VAR:** Variable Exception Processing Latency Control bit
 1 = Variable exception processing latency
 0 = Fixed exception processing latency

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3⁽²⁾
 1 = CPU Interrupt Priority Level is greater than 7
 0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see [Register 3-2](#).

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

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REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

| | | | | | | | |
|--------|--------|--------|---------|---------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|----------|---------|-----|---------|---------|--------|---------|-------|
| R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
| SFTACERR | DIV0ERR | — | MATHERR | ADDRERR | STKERR | OSCFAIL | — |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled
- bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit
1 = Trap was caused by overflow of Accumulator A
0 = Trap was not caused by overflow of Accumulator A
- bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit
1 = Trap was caused by overflow of Accumulator B
0 = Trap was not caused by overflow of Accumulator B
- bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit
1 = Trap was caused by catastrophic overflow of Accumulator A
0 = Trap was not caused by catastrophic overflow of Accumulator A
- bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit
1 = Trap was caused by catastrophic overflow of Accumulator B
0 = Trap was not caused by catastrophic overflow of Accumulator B
- bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit
1 = Trap overflow of Accumulator A
0 = Trap is disabled
- bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit
1 = Trap overflow of Accumulator B
0 = Trap is disabled
- bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit
1 = Trap on catastrophic overflow of Accumulator A or B is enabled
0 = Trap is disabled
- bit 7 **SFTACERR:** Shift Accumulator Error Status bit
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift
- bit 6 **DIV0ERR:** Divide-by-Zero Error Status bit
1 = Math error trap was caused by a divide-by-zero
0 = Math error trap was not caused by a divide-by-zero
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **MATHERR:** Math Error Status bit
1 = Math error trap has occurred
0 = Math error trap has not occurred

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REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

- bit 3 **ADDRERR:** Address Error Trap Status bit
 1 = Address error trap has occurred
 0 = Address error trap has not occurred
- bit 2 **STKERR:** Stack Error Trap Status bit
 1 = Stack error trap has occurred
 0 = Stack error trap has not occurred
- bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
 1 = Oscillator failure trap has occurred
 0 = Oscillator failure trap has not occurred
- bit 0 **Unimplemented:** Read as '0'

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REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

| | | | | | | | |
|--------|-------|--------|-----|-----|-----|-----|--------|
| R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| GIE | DISI | SWTRAP | — | — | — | — | AIVTEN |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|--------|--------|--------|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | INT2EP | INT1EP | INT0EP |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **GIE:** Global Interrupt Enable bit
 1 = Interrupts and associated IE bits are enabled
 0 = Interrupts are disabled, but traps are still enabled
- bit 14 **DISI:** DISI Instruction Status bit
 1 = DISI instruction is active
 0 = DISI instruction is not active
- bit 13 **SWTRAP:** Software Trap Status bit
 1 = Software trap is enabled
 0 = Software trap is disabled
- bit 12-9 **Unimplemented:** Read as '0'
- bit 8 **AIVTEN:** Alternate Interrupt Vector Table Enable
 1 = Uses Alternate Interrupt Vector Table
 0 = Uses standard Interrupt Vector Table
- bit 7-3 **Unimplemented:** Read as '0'
- bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
 1 = Interrupt on negative edge
 0 = Interrupt on positive edge
- bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
 1 = Interrupt on negative edge
 0 = Interrupt on positive edge
- bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
 1 = Interrupt on negative edge
 0 = Interrupt on positive edge

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REGISTER 7-5: INTCON3: INTERRUPT CONTROL REGISTER 3

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| — | — | — | — | — | — | — | NAE |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-------|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 |
| — | — | — | DOOVR | — | — | — | APLL |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-9 **Unimplemented:** Read as '0'
- bit 8 **NAE:** NVM Address Error Soft Trap Status bit
 1 = NVM address error soft trap has occurred
 0 = NVM address error soft trap has not occurred
- bit 7-5 **Unimplemented:** Read as '0'
- bit 4 **DOOVR:** DO Stack Overflow Soft Trap Status bit
 1 = DO stack overflow soft trap has occurred
 0 = DO stack overflow soft trap has not occurred
- bit 3-1 **Unimplemented:** Read as '0'
- bit 0 **APLL:** Auxiliary PLL Loss of Lock Soft Trap Status bit
 1 = APLL lock soft trap has occurred
 0 = APLL lock soft trap has not occurred

REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| — | — | — | — | — | — | — | SGHT |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-1 **Unimplemented:** Read as '0'
- bit 0 **SGHT:** Software Generated Hard Trap Status bit
 1 = Software generated hard trap has occurred
 0 = Software generated hard trap has not occurred

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REGISTER 7-7: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

| | | | | | | | |
|--------|-----|-----|-----|-------|------|------|------|
| U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
| — | — | — | — | ILR3 | ILR2 | ILR1 | ILR0 |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| VECNUM7 | VECNUM6 | VECNUM5 | VECNUM4 | VECNUM3 | VECNUM2 | VECNUM1 | VECNUM0 |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **ILR<3:0>:** New CPU Interrupt Priority Level bits
 1111 = CPU Interrupt Priority Level is 15
 •
 •
 •
 0001 = CPU Interrupt Priority Level is 1
 0000 = CPU Interrupt Priority Level is 0

bit 7-0 **VECNUM<7:0>:** Vector Number of Pending Interrupt bits
 11111111 = 255, Reserved; do not use
 •
 •
 •
 00001001 = 9, IC1 – Input Capture 1
 00001000 = 8, INTO – External Interrupt 0
 00000111 = 7, Reserved; do not use
 00000110 = 6, Generic soft error trap
 00000101 = 5, Reserved; do not use
 00000100 = 4, Math error trap
 00000011 = 3, Stack error trap
 00000010 = 2, Generic hard trap
 00000001 = 1, Address error trap
 00000000 = 0, Oscillator fail trap

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NOTES:

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8.0 OSCILLATOR CONFIGURATION

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Oscillator Module**” (DS70005131) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com)

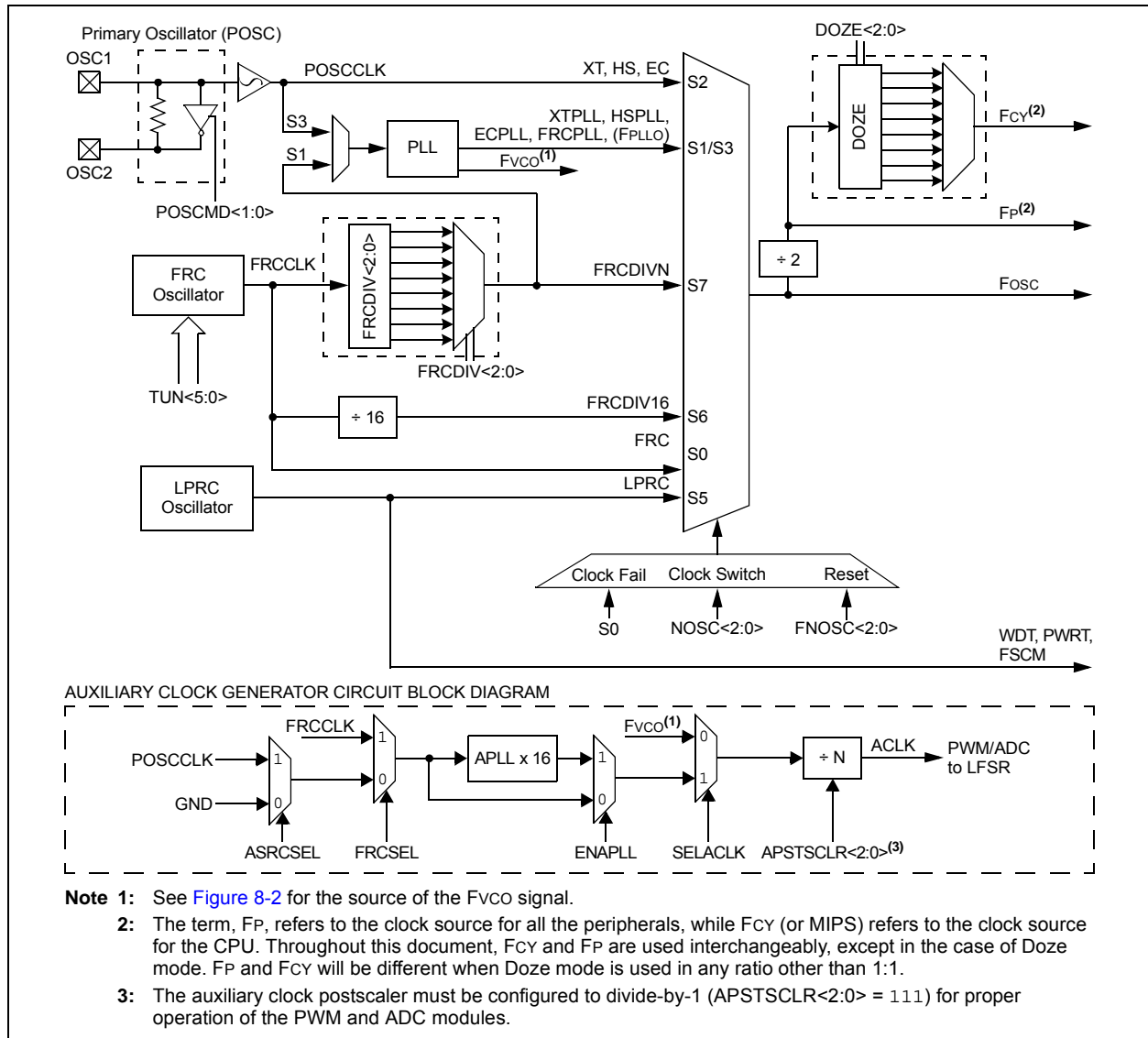
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 family oscillator system provides:

- On-Chip Phase-Locked Loop (PLL) to Boost Internal Operating Frequency on Select Internal and External Oscillator Sources
- On-the-Fly Clock Switching between Various Clock Sources
- Doze mode for System Power Savings
- Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown
- Configuration bits for Clock Source Selection
- Auxiliary PLL for ADC and PWM

A simplified diagram of the oscillator system is shown in **Figure 8-1**.

FIGURE 8-1: OSCILLATOR SYSTEM DIAGRAM



Note 1: See **Figure 8-2** for the source of the FVCO signal.

2: The term, FP, refers to the clock source for all the peripherals, while FCY (or MIPS) refers to the clock source for the CPU. Throughout this document, FCY and FP are used interchangeably, except in the case of Doze mode. FP and FCY will be different when Doze mode is used in any ratio other than 1:1.

3: The auxiliary clock postscaler must be configured to divide-by-1 (APSTSCCLR<2:0> = 111) for proper operation of the PWM and ADC modules.

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8.1 CPU Clocking System

The dsPIC33EPXXGS202 family of devices provides six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase-Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

Instruction execution speed or device operating frequency, F_{CY} , is given by [Equation 8-1](#).

EQUATION 8-1: DEVICE OPERATING FREQUENCY

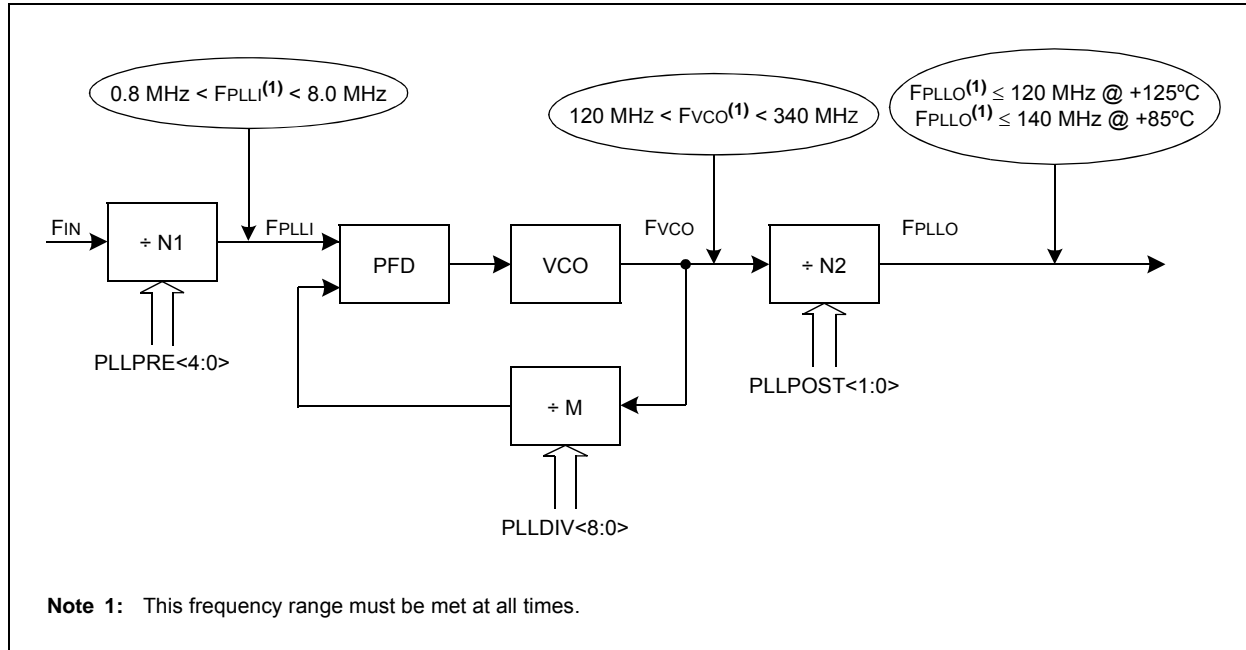
$$F_{CY} = F_{OSC}/2$$

[Figure 8-2](#) is a block diagram of the PLL module.

[Equation 8-2](#) provides the relationship between input frequency (F_{IN}) and output frequency (F_{PULO}).

[Equation 8-3](#) provides the relationship between input frequency (F_{IN}) and VCO frequency (F_{VCO}).

FIGURE 8-2: PLL BLOCK DIAGRAM



EQUATION 8-2: FPLLO CALCULATION

$$F_{PULO} = F_{IN} \times \left(\frac{M}{N1 \times N2} \right) = F_{IN} \times \left(\frac{(PLLDIV<8:0> + 2)}{(PLLPRE<4:0> + 2) \times 2(PLLPOST<1:0> + 1)} \right)$$

Where:

$$N1 = PLLPRE<4:0> + 2$$

$$N2 = 2 \times (PLLPOST<1:0> + 1)$$

$$M = PLLDIV<8:0> + 2$$

EQUATION 8-3: Fvco CALCULATION

$$F_{VCO} = F_{IN} \times \left(\frac{M}{N1} \right) = F_{IN} \times \left(\frac{(PLLDIV<8:0> + 2)}{(PLLPRE<4:0> + 2)} \right)$$

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TABLE 8-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

| Oscillator Mode | Oscillator Source | POSCMD<1:0> | FNOSC<2:0> | See Notes |
|--|-------------------|-------------|------------|-----------|
| Fast RC Oscillator with Divide-by-N (FRCDIVN) | Internal | xx | 111 | 1, 2 |
| Fast RC Oscillator with Divide-by-16 | Internal | xx | 110 | 1 |
| Low-Power RC Oscillator (LPRC) | Internal | xx | 101 | 1 |
| Primary Oscillator (HS) with PLL (HSPLL) | Primary | 10 | 011 | |
| Primary Oscillator (XT) with PLL (XTPLL) | Primary | 01 | 011 | |
| Primary Oscillator (EC) with PLL (ECPLL) | Primary | 00 | 011 | 1 |
| Primary Oscillator (HS) | Primary | 10 | 010 | |
| Primary Oscillator (XT) | Primary | 01 | 010 | |
| Primary Oscillator (EC) | Primary | 00 | 010 | 1 |
| Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL) | Internal | xx | 001 | 1 |
| Fast RC Oscillator (FRC) | Internal | xx | 000 | 1 |

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

8.2 Auxiliary Clock Generation

The auxiliary clock generation is used for peripherals that need to operate at a frequency unrelated to the system clock, such as PWM or ADC.

The primary oscillator and internal FRC oscillator sources can be used with an Auxiliary PLL (APLL) to obtain the auxiliary clock. The Auxiliary PLL has a fixed 16x multiplication factor.

The auxiliary clock has the following configuration restrictions:

- For proper PWM operation, auxiliary clock generation must be configured for 120 MHz (see Parameter OS56 in [Section 25.0 “Electrical Characteristics”](#)). If a slower frequency is desired, the PWM Input Clock Prescaler (Divider) Select bits (PCLKDIV<2:0>) should be used.
- To achieve 1.04 ns PWM resolution, the auxiliary clock must use the 16x Auxiliary PLL (APLL). All other clock sources will have a minimum PWM resolution of 8 ns.
- If the primary PLL is used as a source for the auxiliary clock, the primary PLL should be configured up to a maximum operation of 30 MIPS or less.

8.3 Oscillator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

8.3.1 KEY RESOURCES

- **“Oscillator Module”** (DS70005131) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

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8.4 Oscillator Control Registers

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾

| | | | | | | | |
|--------|-------|-------|-------|-------|----------------------|----------------------|----------------------|
| U-0 | R-0 | R-0 | R-0 | U-0 | R/W-y | R/W-y | R/W-y |
| — | COSC2 | COSC1 | COSC0 | — | NOSC2 ⁽²⁾ | NOSC1 ⁽²⁾ | NOSC0 ⁽²⁾ |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|---------|--------|------|-----|-------------------|-----|-----|-------|
| R/W-0 | R/W-0 | R-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 |
| CLKLOCK | IOLOCK | LOCK | — | CF ⁽³⁾ | — | — | OSWEN |
| bit 7 | | | | bit 0 | | | |

| | |
|-------------------|--|
| Legend: | y = Value set from Configuration bits on POR |
| R = Readable bit | W = Writable bit |
| -n = Value at POR | '1' = Bit is set |
| | U = Unimplemented bit, read as '0' |
| | '0' = Bit is cleared |
| | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)

- 111 = Fast RC Oscillator (FRC) with Divide-by-n
- 110 = Fast RC Oscillator (FRC) with Divide-by-16
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Reserved
- 011 = Primary Oscillator (XT, HS, EC) with PLL
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
- 000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits⁽²⁾

- 111 = Fast RC Oscillator (FRC) with Divide-by-n
- 110 = Fast RC Oscillator (FRC) with Divide-by-16
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Reserved
- 011 = Primary Oscillator (XT, HS, EC) with PLL
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
- 000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit

- 1 = If (FCKSM0 = 1), then clock and PLL configurations are locked; if (FCKSM0 = 0), then clock and PLL configurations may be modified
- 0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 **IOLOCK:** I/O Lock Enable bit

- 1 = I/O lock is active
- 0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit (read-only)

- 1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
- 0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

Note 1: Writes to this register require an unlock sequence.

Note 2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

Note 3: This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

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REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾ (CONTINUED)

| | |
|---------|--|
| bit 4 | Unimplemented: Read as '0' |
| bit 3 | CF: Clock Fail Detect bit ⁽³⁾ 1 = FSCM has detected a clock failure 0 = FSCM has not detected a clock failure |
| bit 2-1 | Unimplemented: Read as '0' |
| bit 0 | OSWEN: Oscillator Switch Enable bit 1 = Requests oscillator switch to selection specified by the NOSC<2:0> bits 0 = Oscillator switch is complete |

- Note 1:** Writes to this register require an unlock sequence.
- 2:** Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.
- 3:** This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

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REGISTER 8-2: CLKDIV: CLOCK DIVISOR REGISTER

| | | | | | | | |
|--------|----------------------|----------------------|----------------------|------------------------|---------|---------|---------|
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| ROI | DOZE2 ⁽¹⁾ | DOZE1 ⁽¹⁾ | DOZE0 ⁽¹⁾ | DOZEN ^(2,3) | FRCDIV2 | FRCDIV1 | FRCDIV0 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|----------|----------|-----|---------|---------|---------|---------|---------|
| R/W-0 | R/W-1 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PLLPOST1 | PLLPOST0 | — | PLLPRE4 | PLLPRE3 | PLLPRE2 | PLLPRE1 | PLLPRE0 |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **ROI:** Recover on Interrupt bit
 1 = Interrupts will clear the DOZEN bit and the processor clock, and the peripheral clock ratio is set to 1:1
 0 = Interrupts have no effect on the DOZEN bit
- bit 14-12 **DOZE<2:0>:** Processor Clock Reduction Select bits⁽¹⁾
 111 = Fcy divided by 128
 110 = Fcy divided by 64
 101 = Fcy divided by 32
 100 = Fcy divided by 16
 011 = Fcy divided by 8 (default)
 010 = Fcy divided by 4
 001 = Fcy divided by 2
 000 = Fcy divided by 1
- bit 11 **DOZEN:** Doze Mode Enable bit^(2,3)
 1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks
 0 = Processor clock and peripheral clock ratio is forced to 1:1
- bit 10-8 **FRCDIV<2:0>:** Internal Fast RC Oscillator Postscaler bits
 111 = FRC divided by 256
 110 = FRC divided by 64
 101 = FRC divided by 32
 100 = FRC divided by 16
 011 = FRC divided by 8
 010 = FRC divided by 4
 001 = FRC divided by 2
 000 = FRC divided by 1 (default)
- bit 7-6 **PLLPOST<1:0>:** PLL VCO Output Divider Select bits (also denoted as 'N2', PLL postscaler)
 11 = Output divided by 8
 10 = Reserved
 01 = Output divided by 4 (default)
 00 = Output divided by 2
- bit 5 **Unimplemented:** Read as '0'

- Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
- 2:** This bit is cleared when the ROI bit is set and an interrupt occurs.
- 3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

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REGISTER 8-2: CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)

bit 4-0 **PLLPRE<4:0>**: PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)
 11111 = Input divided by 33
 •
 •
 •
 00001 = Input divided by 3
 00000 = Input divided by 2 (default)

- Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
2: This bit is cleared when the ROI bit is set and an interrupt occurs.
3: The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

REGISTER 8-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|---------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| — | — | — | — | — | — | — | PLLDIV8 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PLLDIV<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV<8:0>**: PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)
 111111111 = 513
 •
 •
 •
 000110000 = 50 (default)
 •
 •
 •
 000000010 = 4
 000000001 = 3
 000000000 = 2

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REGISTER 8-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER⁽¹⁾

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-------|-----|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-----|----------|-------|-------|-------|-------|-------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | TUN<5:0> | | | | | |
| bit 7 | | | | | | bit 0 | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits

011111 = Maximum frequency deviation of 1.457% (7.477 MHz)

011110 = Center frequency + 1.41% (7.474 MHz)

•

•

•

000001 = Center frequency + 0.047% (7.373 MHz)

000000 = Center frequency (7.37 MHz nominal)

111111 = Center frequency – 0.047% (7.367 MHz)

•

•

•

100001 = Center frequency – 1.457% (7.263 MHz)

100000 = Minimum frequency deviation of -1.5% (7.259 MHz)

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step-size is an approximation and is neither characterized nor tested.

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REGISTER 8-5: ACLKCON: AUXILIARY CLOCK DIVISOR CONTROL REGISTER

| | | | | | | | |
|--------|--------|---------|-----|-----|-----------|-----------|-----------|
| R/W-0 | R-0 | R/W-1 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 |
| ENAPLL | APLLCK | SELACLK | — | — | APSTSCLR2 | APSTSCLR1 | APSTSCLR0 |
| bit 15 | | | | | | bit 0 | |

| | | | | | | | |
|---------|--------|-----|-----|-----|-----|-----|-----|
| R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| ASRCSEL | FRCSEL | — | — | — | — | — | — |
| bit 7 | | | | | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **ENAPLL:** Auxiliary PLL Enable bit
 1 = APLL is enabled
 0 = APLL is disabled
- bit 14 **APLLCK:** APLL Locked Status bit (read-only)
 1 = Indicates that the Auxiliary PLL is in lock
 0 = Indicates that the Auxiliary PLL is not in lock
- bit 13 **SELACLK:** Select Auxiliary Clock Source for Auxiliary Clock Divider bit
 1 = Auxiliary oscillators provide the source clock for the auxiliary clock divider
 0 = Primary PLL (Fvco) provides the source clock for the auxiliary clock divider
- bit 12-11 **Unimplemented:** Read as '0'
- bit 10-8 **APSTSCLR<2:0>:** Auxiliary Clock Output Divider bits
 111 = Divided by 1
 110 = Divided by 2
 101 = Divided by 4
 100 = Divided by 8
 011 = Divided by 16
 010 = Divided by 32
 001 = Divided by 64
 000 = Divided by 256
- bit 7 **ASRCSEL:** Select Reference Clock Source for Auxiliary Clock bit
 1 = Primary oscillator is the clock source
 0 = No clock input is selected
- bit 6 **FRCSEL:** Select Reference Clock Source for Auxiliary PLL bit
 1 = Selects FRC clock for Auxiliary PLL
 0 = Input clock source is determined by the ASRCSEL bit setting
- bit 5-0 **Unimplemented:** Read as '0'

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REGISTER 8-6: LFSR: LINEAR FEEDBACK SHIFT REGISTER

| | | | | | | | |
|--------|------------|-------|-------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | LFSR<14:8> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| LFSR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **LFSR<14:0>:** Pseudorandom Data bits

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9.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Watchdog Timer and Power-Saving Modes**” (DS70615) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com)

2: Some registers and associated bits described in this section may not be available on all devices. Refer to [Section 4.0 “Memory Organization”](#) in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 family devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXGS202 family devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application’s power consumption while still maintaining critical application features, such as timing-sensitive communications.

EXAMPLE 9-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV #SLEEP_MODE    ; Put the device into Sleep mode
PWRSAV #IDLE_MODE     ; Put the device into Idle mode
```

9.1 Clock Frequency and Clock Switching

The dsPIC33EPXXGS202 family devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC_x bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in [Section 8.0 “Oscillator Configuration”](#).

9.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXGS202 family devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in [Example 9-1](#).

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to “wake-up”.

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9.2.1 SLEEP MODE

The following occur in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification on the I/O ports, or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of the these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into stand-by when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

9.2.2 IDLE MODE

The following occur in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see [Section 9.4 “Peripheral Module Disable”](#)).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the `PWRSVAV` instruction or the first instruction in the ISR.

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral (for example, the `TSIDL` bit in the Timer1 Control register (T1CON<13>)).

9.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a `PWRSVAV` instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

9.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

9.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD_x control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have any effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD_x register is cleared and the peripheral is supported by the specific dsPIC[®] DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note: If a PMD_x bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD_x bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

9.5 Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

9.5.1 KEY RESOURCES

- “**Watchdog Timer and Power-Saving Modes**” (DS70615) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

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REGISTER 9-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1

| | | | | | | | |
|--------|-----|-------|-------|-------|-----|-------|-----|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 |
| — | — | T3MD | T2MD | T1MD | — | PWMMD | — |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|--------|-----|-------|-----|--------|-----|-------|-------|
| R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 |
| I2C1MD | — | U1MD | — | SPI1MD | — | — | ADCMD |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **T3MD:** Timer3 Module Disable bit
1 = Timer3 module is disabled
0 = Timer3 module is enabled
- bit 12 **T2MD:** Timer2 Module Disable bit
1 = Timer2 module is disabled
0 = Timer2 module is enabled
- bit 11 **T1MD:** Timer1 Module Disable bit
1 = Timer1 module is disabled
0 = Timer1 module is enabled
- bit 10 **Unimplemented:** Read as '0'
- bit 9 **PWMMD:** PWM Module Disable bit
1 = PWM module is disabled
0 = PWM module is enabled
- bit 8 **Unimplemented:** Read as '0'
- bit 7 **I2C1MD:** I2C1 Module Disable bit
1 = I2C1 module is disabled
0 = I2C1 module is enabled
- bit 6 **Unimplemented:** Read as '0'
- bit 5 **U1MD:** UART1 Module Disable bit
1 = UART1 module is disabled
0 = UART1 module is enabled
- bit 4 **Unimplemented:** Read as '0'
- bit 3 **SPI1MD:** SPI1 Module Disable bit
1 = SPI1 module is disabled
0 = SPI1 module is enabled
- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **ADCMD:** ADC Module Disable bit
1 = ADC module is disabled
0 = ADC module is enabled

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REGISTER 9-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| — | — | — | — | — | — | — | IC1MD |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| — | — | — | — | — | — | — | OC1MD |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **IC1MD:** Input Capture 1 Module Disable bit

1 = Input Capture 1 module is disabled

0 = Input Capture 1 module is enabled

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **OC1MD:** Output Compare 1 Module Disable bit

1 = Output Compare 1 module is disabled

0 = Output Compare 1 module is enabled

REGISTER 9-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

| | | | | | | | |
|--------|-----|-----|-----|-----|-------|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 |
| — | — | — | — | — | CMPMD | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **CMPMD:** Comparator Module Disable bit

1 = Comparator module is disabled

0 = Comparator module is enabled

bit 9-0 **Unimplemented:** Read as '0'

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REGISTER 9-4: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

| | | | | | | | |
|--------|-----|-----|-----|-----|--------|--------|--------|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | PWM3MD | PWM2MD | PWM1MD |
| bit 15 | | | | | bit 8 | | |

| | | | | | | | |
|-------|-----|-----|-----|-----|-------|-----|-----|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | bit 0 | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10 **PWM3MD:** PWM3 Module Disable bit
1 = PWM3 module is disabled
0 = PWM3 module is enabled
- bit 9 **PWM2MD:** PWM2 Module Disable bit
1 = PWM2 module is disabled
0 = PWM2 module is enabled
- bit 8 **PWM1MD:** PWM1 Module Disable bit
1 = PWM1 module is disabled
0 = PWM1 module is enabled
- bit 7-0 **Unimplemented:** Read as '0'

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REGISTER 9-5: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|--------|--------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | — | CMP2MD | CMP1MD |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|--------|-----|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 |
| — | — | — | — | — | — | PGA1MD | — |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-10 **Unimplemented:** Read as '0'
- bit 9 **CMP2MD:** Comparator Channel 2 (CMP2) Module Disable bit
 1 = CMP2 module is disabled
 0 = CMP2 module is enabled
- bit 8 **CMP1MD:** Comparator Channel 1 (CMP1) Module Disable bit
 1 = CMP1 module is disabled
 0 = CMP1 module is enabled
- bit 7-2 **Unimplemented:** Read as '0'
- bit 1 **PGA1MD:** PGA1 Module Disable bit
 1 = PGA1 module is disabled
 0 = PGA1 module is enabled
- bit 0 **Unimplemented:** Read as '0'

REGISTER 9-6: PMD8: PERIPHERAL MODULE DISABLE CONTROL REGISTER 8

| | | | | | | | |
|--------|-----|-----|-----|-----|--------|-------|-----|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 |
| — | — | — | — | — | PGA2MD | — | — |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-------|-----|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10 **PGA2MD:** PGA2 Module Disable bit
 1 = PGA2 module is disabled
 0 = PGA2 module is enabled
- bit 9-0 **Unimplemented:** Read as '0'

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NOTES:

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10.0 I/O PORTS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “I/O Ports” (DS70000598) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

Many of the device pins are shared among the peripherals and the Parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

10.1 Parallel I/O (PIO) Ports

Generally, a Parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral’s output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port

has ownership of the output data and control signals of the I/O pin. The logic also prevents “loop through”, in which a port’s digital output can drive the input of a peripheral that shares the same pin. **Figure 10-1** illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

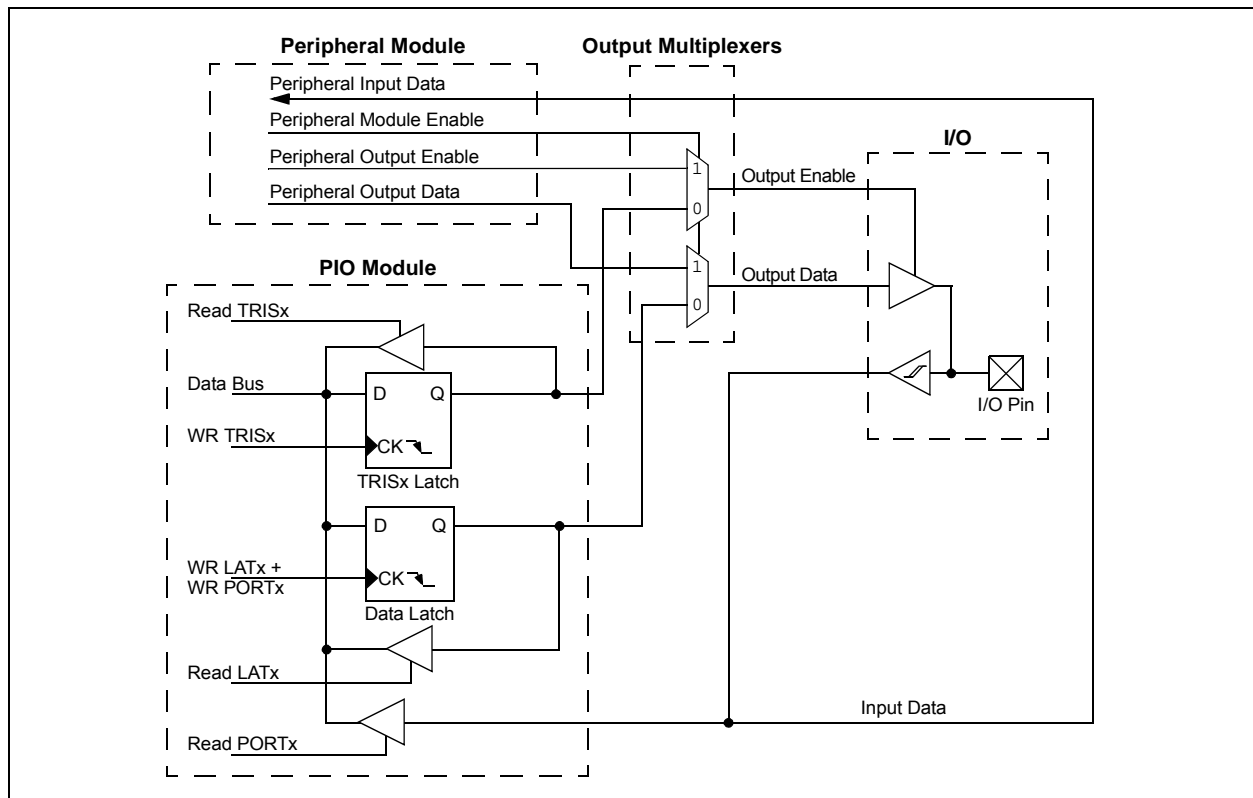
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have eight registers directly associated with their operation as digital I/Os. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a ‘1’, then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx), read the latch. Writes to the latch, write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device are disabled. This means the corresponding LATx and TRISx registers, and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

FIGURE 10-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



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10.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See the “Pin Diagrams” section for the available 5V tolerant pins and Table 25-11 for the maximum VIH specification for each pin.

10.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as timers, UART, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin, defined as a digital input (including the ANx pins), can cause the input buffer to consume current that exceeds the device specifications.

10.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP, as shown in Example 10-1.

10.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the ICN functionality of each I/O port. The CNENx registers contain the ICN interrupt enable control bits for each of the input pins. Setting any of these bits enables an ICN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pull-downs act as a current source, or sink source, connected to the pin, and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are enabled separately, using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note: Pull-ups and pull-downs on Input Change Notification pins should always be disabled when the port pin is configured as a digital output.

EXAMPLE 10-1: PORT WRITE/READ

```
MOV    0xFF00, W0    ; Configure PORTB<15:8>
                        ; as inputs
MOV    W0, TRISB    ; and PORTB<7:0>
                        ; as outputs
NOP                    ; Delay 1 cycle
BTSS   PORTB, #13   ; Next Instruction
```

10.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

10.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, “RPn”, in their full pin designation, where “n” is the remappable pin number. “RPn” is used to designate pins that support both remappable input and output functions.

10.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. One example includes I²C modules. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/Os and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

10.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

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10.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see [Register 10-1](#) through [Register 10-15](#)). Each register contains sets of 8-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 8-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

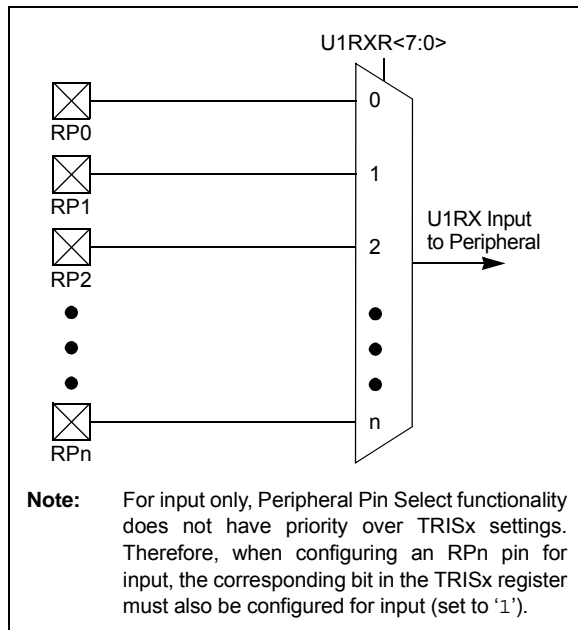
For example, [Figure 10-2](#) illustrates remappable pin selection for the U1RX input.

10.4.4.1 Virtual Connections

The dsPIC33EPXXGS202 devices support six virtual RPn pins (RP176-RP181), which are identical in functionality to all other RPn pins, with the exception of pinouts. These six pins are internal to the devices and are not connected to a physical device pin.

These pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example, the output of the analog comparator can be connected to RP176 and the PWM Fault input can be configured for RP176 as well. This configuration allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

FIGURE 10-2: REMAPPABLE INPUT FOR U1RX



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TABLE 10-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

| Input Name ⁽¹⁾ | Function Name | Register | Configuration Bits |
|---------------------------|--------------------|----------|--------------------|
| External Interrupt 1 | INT1 | RPINR0 | INT1R<7:0> |
| External Interrupt 2 | INT2 | RPINR1 | INT2R<7:0> |
| Timer1 External Clock | T1CK | RPINR2 | T1CKR<7:0> |
| Timer2 External Clock | T2CK | RPINR3 | T2CKR<7:0> |
| Timer3 External Clock | T3CK | RPINR3 | T3CKR<7:0> |
| Input Capture 1 | IC1 | RPINR7 | IC1R<7:0> |
| Output Compare Fault A | OCFA | RPINR11 | OCFAR<7:0> |
| PWM Fault 1 | FLT1 | RPINR12 | FLT1R<7:0> |
| PWM Fault 2 | FLT2 | RPINR12 | FLT2R<7:0> |
| PWM Fault 3 | FLT3 | RPINR13 | FLT3R<7:0> |
| PWM Fault 4 | FLT4 | RPINR13 | FLT4R<7:0> |
| UART1 Receive | U1RX | RPINR18 | U1RXR<7:0> |
| UART1 Clear-to-Send | $\overline{U1CTS}$ | RPINR18 | U1CTSR<7:0> |
| SPI1 Data Input | SDI1 | RPINR20 | SDI1R<7:0> |
| SPI1 Clock Input | SCK1 | RPINR20 | SCK1R<7:0> |
| SPI1 Slave Select | $\overline{SS1}$ | RPINR21 | SS1R<7:0> |
| PWM Synchronous Input 1 | SYNCI1 | RPINR37 | SYNCI1R<7:0> |
| PWM Synchronous Input 2 | SYNCI2 | RPINR38 | SYNCI2R<7:0> |
| PWM Fault 5 | FLT5 | RPINR42 | FLT5R<7:0> |
| PWM Fault 6 | FLT6 | RPINR42 | FLT6R<7:0> |
| PWM Fault 7 | FLT7 | RPINR43 | FLT7R<7:0> |
| PWM Fault 8 | FLT8 | RPINR43 | FLT8R<7:0> |

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

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10.4.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Each register contains sets of 6-bit fields, with each set associated with one RPn pin (see [Register 10-16](#) through [Register 10-26](#)). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see [Table 10-2](#) and [Figure 10-3](#)).

A null output is associated with the Output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

10.4.5.1 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs, and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

FIGURE 10-3: MULTIPLEXING REMAPPABLE OUTPUTS FOR RPn

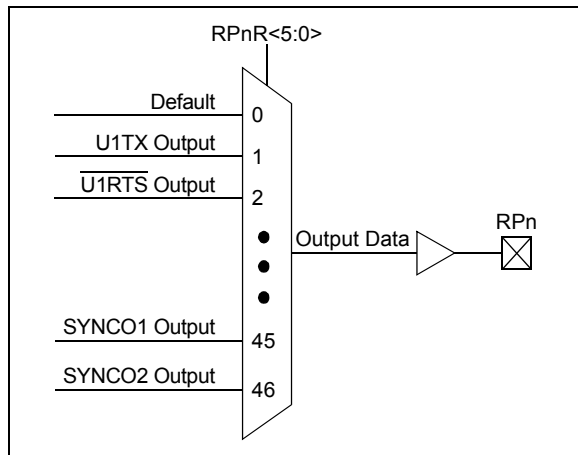


TABLE 10-2: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

| Function | RPNR<5:0> | Output Name |
|--------------|-----------|--|
| Default PORT | 000000 | RPn tied to Default Pin |
| U1TX | 000001 | RPn tied to UART1 Transmit |
| U1RTS/BCLK | 000010 | RPn tied to UART1 Request-to-Send |
| SDO1 | 000101 | RPn tied to SPI1 Data Output |
| SCK1 | 000110 | RPn tied to SPI1 Clock Output |
| SS1 | 000111 | RPn tied to SPI1 Slave Select |
| OC1 | 010000 | RPn tied to Output Compare 1 Output |
| ACMP1 | 011000 | RPn tied to Analog Comparator 1 Output |
| ACMP2 | 011001 | RPn tied to Analog Comparator 2 Output |
| SYNCO1 | 101101 | RPn tied to PWM Primary Master Time Base Sync Output |
| SYNCO2 | 101110 | RPn tied to PWM Secondary Master Time Base Sync Output |

10.5 I/O Helpful Tips

1. In some cases, certain pins, as defined in [Table 25-11](#) under “Injection Current”, have internal protection diodes to VDD and VSS. The term, “Injection Current”, is also referred to as “Clamp Current”. On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device, that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a ‘0’, regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a ‘0’.

Note: Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to $\sim(V_{DD} - 0.8)$, not VDD. This value is still above the minimum V_{IH} of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the V_{OH}/I_{OH} and V_{OL}/I_{OL} DC characteristics specification. The respective I_{OH} and I_{OL} current rating only applies to maintaining the corresponding output at or above the V_{OH} , and at or below the V_{OL} levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum V_{IH}/V_{IL} levels. An I/O pin output can safely sink or source any current less than that listed in the Absolute Maximum Ratings in [Section 25.0 “Electrical Characteristics”](#) of this data sheet. For example:

$$V_{OH} = 2.4V @ I_{OH} = -8 \text{ mA and } V_{DD} = 3.3V$$

The maximum output current sourced by any 8 mA I/O pin = 12 mA.

LED source current < 12 mA is technically permitted.

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6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
- Only one “output” function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
 - It is possible to assign a “remappable output” function to multiple pins and externally short or tie them together for increased current drive.
 - If any “dedicated output” function is enabled on a pin, it will take precedence over any remappable “output” function.
 - If any “dedicated digital” (input or output) function is enabled on a pin, any number of “input” remappable functions can be mapped to the same pin.
 - If any “dedicated analog” function(s) are enabled on a given pin, “digital input(s)” of any kind will all be disabled, although a single “digital output”, at the user’s cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input, provided there is no external analog input, such as for a built-in self-test.
 - Any number of “input” remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable “output”.
 - The TRISx registers control *only* the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRISx setting. The TRISx register *does not* control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRISx settings, which means that the TRISx bit must be set to input for pins with only remappable input function(s) assigned.
 - All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin has been disabled. Only the Analog Pin Select (ANSELx) registers control the digital input buffer, *not* the TRISx register. The user must disable the analog function on a pin using the Analog Pin Select registers in order to use any “digital input(s)” on a corresponding pin, no exceptions.

10.6 I/O Ports Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

10.6.1 KEY RESOURCES

- “**I/O Ports**” (DS70000598) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

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10.7 Peripheral Pin Select Registers

REGISTER 10-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| INT1R<7:0> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15-8 **INT1R<7:0>**: Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

bit 7-0 **Unimplemented**: Read as '0'

REGISTER 10-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| INT2R<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15-8 **Unimplemented**: Read as '0'

bit 7-0 **INT2R<7:0>**: Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

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REGISTER 10-3: RPINR2: PERIPHERAL PIN SELECT INPUT REGISTER 2

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| T1CKR<7:0> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-8 **T1CKR<7:0>**: Assign Timer1 External Clock (T1CK) to the Corresponding RPn Pin bits
 10110101 = Input tied to RP181
 10110100 = Input tied to RP180
 •
 •
 •
 00000001 = Input tied to RP1
 00000000 = Input tied to Vss

bit 7-0 **Unimplemented**: Read as '0'

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REGISTER 10-4: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| T3CKR7 | T3CKR6 | T3CKR5 | T3CKR4 | T3CKR3 | T3CKR2 | T3CKR1 | T3CKR0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| T2CKR7 | T2CKR6 | T2CKR5 | T2CKR4 | T2CKR3 | T2CKR2 | T2CKR1 | T2CKR0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **T3CKR<7:0>**: Assign Timer3 External Clock (T3CK) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180

•
•
•

0000001 = Input tied to RP1
0000000 = Input tied to Vss

bit 7-0 **T2CKR<7:0>**: Assign Timer2 External Clock (T2CK) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180

•
•
•

0000001 = Input tied to RP1
0000000 = Input tied to Vss

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REGISTER 10-5: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| IC1R<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'
 bit 7-0 **IC1R<7:0>:** Assign Input Capture 1 (IC1) to the Corresponding RPn Pin bits
 10110101 = Input tied to RP181
 10110100 = Input tied to RP180
 •
 •
 •
 00000001 = Input tied to RP1
 00000000 = Input tied to Vss

REGISTER 10-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| OCFAR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'
 bit 7-0 **OCFAR<7:0>:** Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits
 10110101 = Input tied to RP181
 10110100 = Input tied to RP180
 •
 •
 •
 00000001 = Input tied to RP1
 00000000 = Input tied to Vss

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REGISTER 10-7: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FLT2R7 | FLT2R6 | FLT2R5 | FLT2R4 | FLT2R3 | FLT2R2 | FLT2R1 | FLT2R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FLT1R7 | FLT1R6 | FLT1R5 | FLT1R4 | FLT1R3 | FLT1R2 | FLT1R1 | FLT1R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-8 **FLT2R<7:0>**: Assign PWM Fault 2 (FLT2) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

bit 7-0 **FLT1R<7:0>**: Assign PWM Fault 1 (FLT1) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

dsPIC33EPXXGS202 FAMILY

REGISTER 10-8: RPINR13: PERIPHERAL PIN SELECT INPUT REGISTER 13

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FLT4R7 | FLT4R6 | FLT4R5 | FLT4R4 | FLT4R3 | FLT4R2 | FLT4R1 | FLT4R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FLT3R7 | FLT3R6 | FLT3R5 | FLT3R4 | FLT3R3 | FLT3R2 | FLT3R1 | FLT3R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-8 **FLT4R<7:0>**: Assign PWM Fault 4 (FLT4) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

bit 7-0 **FLT3R<7:0>**: Assign PWM Fault 3 (FLT3) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

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REGISTER 10-9: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| U1CTSR7 | U1CTSR6 | U1CTSR5 | U1CTSR4 | U1CTSR3 | U1CTSR2 | U1CTSR1 | U1CTSR0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| U1RXR7 | U1RXR6 | U1RXR5 | U1RXR4 | U1RXR3 | U1RXR2 | U1RXR1 | U1RXR0 |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15-8 **U1CTSR<7:0>**: Assign UART1 Clear-to-Send ($\overline{U1CTS}$) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

bit 7-0 **U1RXR<7:0>**: Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

dsPIC33EPXXGS202 FAMILY

REGISTER 10-10: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SCK1INR7 | SCK1INR6 | SCK1INR5 | SCK1INR4 | SCK1INR3 | SCK1INR2 | SCK1INR1 | SCK1INR0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SDI1R7 | SDI1R6 | SDI1R5 | SDI1R4 | SDI1R3 | SDI1R2 | SDI1R1 | SDI1R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-8 **SCK1INR<7:0>**: Assign SPI1 Clock Input (SCK1) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

bit 7-0 **SDI1R<7:0>**: Assign SPI1 Data Input (SDI1) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

dsPIC33EPXXGS202 FAMILY

REGISTER 10-11: RPINR21: PERIPHERAL PIN SELECT INPUT REGISTER 21

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SS1R<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'
 bit 7-0 **SS1R<7:0>:** Assign SPI1 Slave Select ($\overline{SS1}$) to the Corresponding RPn Pin bits
 10110101 = Input tied to RP181
 10110100 = Input tied to RP180
 •
 •
 •
 00000001 = Input tied to RP1
 00000000 = Input tied to Vss

REGISTER 10-12: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SYNC11R<7:0> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **SYNC11R<7:0>:** Assign PWM Synchronization Input 1 (SYNC11) to the Corresponding RPn Pin bits
 10110101 = Input tied to RP181
 10110100 = Input tied to RP180
 •
 •
 •
 00000001 = Input tied to RP1
 00000000 = Input tied to Vss
 bit 7-0 **Unimplemented:** Read as '0'

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REGISTER 10-13: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-------|-----|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SYNCI2R<7:0> | | | | | | | |
| bit 7 | | | | | | bit 0 | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **SYNCI2R<7:0>:** Assign PWM Synchronization Input 2 (SYNCI2) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

dsPIC33EPXXGS202 FAMILY

REGISTER 10-14: RPINR42: PERIPHERAL PIN SELECT INPUT REGISTER 42

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FLT6R7 | FLT6R6 | FLT6R5 | FLT6R4 | FLT6R3 | FLT6R2 | FLT6R1 | FLT6R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FLT5R7 | FLT5R6 | FLT5R5 | FLT5R4 | FLT5R3 | FLT5R2 | FLT5R1 | FLT5R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15-8 **FLT6R<7:0>**: Assign PWM Fault 6 (FLT6) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

bit 7-0 **FLT5R<7:0>**: Assign PWM Fault 5 (FLT5) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

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REGISTER 10-15: RPINR43: PERIPHERAL PIN SELECT INPUT REGISTER 43

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FLT8R7 | FLT8R6 | FLT8R5 | FLT8R4 | FLT8R3 | FLT8R2 | FLT8R1 | FLT8R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FLT7R7 | FLT7R6 | FLT7R5 | FLT7R4 | FLT7R3 | FLT7R2 | FLT7R1 | FLT7R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-8 **FLT8R<7:0>**: Assign PWM Fault 8 (FLT8) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

bit 7-0 **FLT7R<7:0>**: Assign PWM Fault 7 (FLT7) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

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REGISTER 10-16: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

| | | | | | | | |
|--------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP33R5 | RP33R4 | RP33R3 | RP33R2 | RP33R1 | RP33R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP32R5 | RP32R4 | RP32R3 | RP32R2 | RP32R1 | RP32R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP33R<5:0>:** Peripheral Output Function is Assigned to RP33 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP32R<5:0>:** Peripheral Output Function is Assigned to RP32 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)

REGISTER 10-17: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

| | | | | | | | |
|--------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP35R5 | RP35R4 | RP35R3 | RP35R2 | RP35R1 | RP35R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP34R5 | RP34R4 | RP34R3 | RP34R2 | RP34R1 | RP34R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP35R<5:0>:** Peripheral Output Function is Assigned to RP35 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP34R<5:0>:** Peripheral Output Function is Assigned to RP34 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)

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REGISTER 10-18: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

| | | | | | | | |
|--------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP37R5 | RP37R4 | RP37R3 | RP37R2 | RP37R1 | RP37R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP36R5 | RP36R4 | RP36R3 | RP36R2 | RP36R1 | RP36R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP37R<5:0>:** Peripheral Output Function is Assigned to RP37 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP36R<5:0>:** Peripheral Output Function is Assigned to RP36 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)

REGISTER 10-19: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

| | | | | | | | |
|--------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP39R5 | RP39R4 | RP39R3 | RP39R2 | RP39R1 | RP39R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP38R5 | RP38R4 | RP38R3 | RP38R2 | RP38R1 | RP38R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP39R<5:0>:** Peripheral Output Function is Assigned to RP39 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP38R<5:0>:** Peripheral Output Function is Assigned to RP38 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)

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REGISTER 10-20: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

| | | | | | | | |
|--------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP41R5 | RP41R4 | RP41R3 | RP41R2 | RP41R1 | RP41R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP40R5 | RP40R4 | RP40R3 | RP40R2 | RP40R1 | RP40R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP41R<5:0>:** Peripheral Output Function is Assigned to RP41 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP40R<5:0>:** Peripheral Output Function is Assigned to RP40 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)

REGISTER 10-21: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

| | | | | | | | |
|--------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP43R5 | RP43R4 | RP43R3 | RP43R2 | RP43R1 | RP43R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP42R5 | RP42R4 | RP42R3 | RP42R2 | RP42R1 | RP42R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP43R<5:0>:** Peripheral Output Function is Assigned to RP43 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP42R<5:0>:** Peripheral Output Function is Assigned to RP42 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)

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REGISTER 10-22: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

| | | | | | | | |
|--------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP45R5 | RP45R4 | RP45R3 | RP45R2 | RP45R1 | RP45R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP44R5 | RP44R4 | RP44R3 | RP44R2 | RP44R1 | RP44R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP45R<5:0>:** Peripheral Output Function is Assigned to RP45 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP44R<5:0>:** Peripheral Output Function is Assigned to RP44 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)

REGISTER 10-23: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

| | | | | | | | |
|--------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP47R5 | RP47R4 | RP47R3 | RP47R2 | RP47R1 | RP47R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|--------|--------|--------|--------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP46R5 | RP46R4 | RP46R3 | RP46R2 | RP46R1 | RP46R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP47R<5:0>:** Peripheral Output Function is Assigned to RP47 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP46R<5:0>:** Peripheral Output Function is Assigned to RP46 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)

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REGISTER 10-24: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8

| | | | | | | | |
|--------|-----|---------|---------|---------|---------|---------|---------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP177R5 | RP177R4 | RP177R3 | RP177R2 | RP177R1 | RP177R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|---------|---------|---------|---------|---------|---------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP176R5 | RP176R4 | RP176R3 | RP176R2 | RP176R1 | RP176R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP177R<5:0>:** Peripheral Output Function is Assigned to RP177 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP176R<5:0>:** Peripheral Output Function is Assigned to RP176 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)

REGISTER 10-25: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9

| | | | | | | | |
|--------|-----|---------|---------|---------|---------|---------|---------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP179R5 | RP179R4 | RP179R3 | RP179R2 | RP179R1 | RP179R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|---------|---------|---------|---------|---------|---------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP178R5 | RP178R4 | RP178R3 | RP178R2 | RP178R1 | RP178R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP179R<5:0>:** Peripheral Output Function is Assigned to RP179 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP178R<5:0>:** Peripheral Output Function is Assigned to RP178 Output Pin bits
 (see [Table 10-2](#) for peripheral function numbers)

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REGISTER 10-26: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

| | | | | | | | |
|--------|-----|---------|---------|---------|---------|---------|---------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP181R5 | RP181R4 | RP181R3 | RP181R2 | RP181R1 | RP181R0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|---------|---------|---------|---------|---------|---------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | RP180R5 | RP180R4 | RP180R3 | RP180R2 | RP180R1 | RP180R0 |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP181R<5:0>:** Peripheral Output Function is Assigned to RP181 Output Pin bits
(see [Table 10-2](#) for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP180R<5:0>:** Peripheral Output Function is Assigned to RP180 Output Pin bits
(see [Table 10-2](#) for peripheral function numbers)

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11.0 TIMER1

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Timers” (DS70362) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to [Section 4.0 “Memory Organization”](#) in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be Operated in Asynchronous Counter mode from an External Clock Source
- The External Clock Input (T1CK) can Optionally be Synchronized to the Internal Device Clock and the Clock Synchronization is Performed after the Prescaler

A block diagram of Timer1 is shown in [Figure 11-1](#).

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

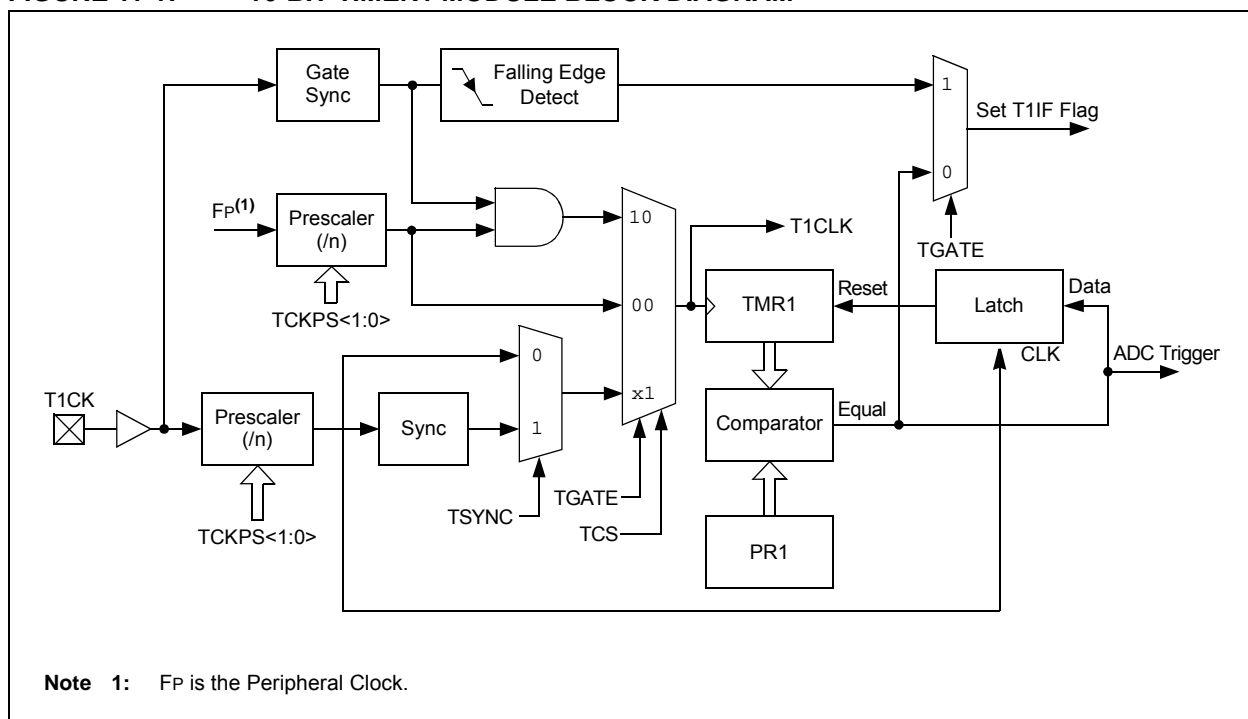
- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit settings for different operating modes are provided in [Table 11-1](#).

TABLE 11-1: TIMER MODE SETTINGS

| Mode | TCS | TGATE | TSYNC |
|----------------------|-----|-------|-------|
| Timer | 0 | 0 | x |
| Gated Timer | 0 | 1 | x |
| Synchronous Counter | 1 | x | 1 |
| Asynchronous Counter | 1 | x | 0 |

FIGURE 11-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



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11.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

11.1.1 KEY RESOURCES

- **“Timers”** (DS70362) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

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11.2 Timer1 Control Register

REGISTER 11-1: T1CON: TIMER1 CONTROL REGISTER

| | | | | | | | |
|--------------------|-----|-------|-----|-----|-----|-----|-------|
| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| TON ⁽¹⁾ | — | TSIDL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-------|--------|--------|-----|----------------------|--------------------|-------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 |
| — | TGATE | TCKPS1 | TCKPS0 | — | TSYNC ⁽¹⁾ | TCS ⁽¹⁾ | — |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **TON:** Timer1 On bit⁽¹⁾
 1 = Starts 16-bit Timer1
 0 = Stops 16-bit Timer1
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-7 **Unimplemented:** Read as '0'
- bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
 When TCS = 1:
 This bit is ignored.
 When TCS = 0:
 1 = Gated time accumulation is enabled
 0 = Gated time accumulation is disabled
- bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
 11 = 1:256
 10 = 1:64
 01 = 1:8
 00 = 1:1
- bit 3 **Unimplemented:** Read as '0'
- bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit⁽¹⁾
 When TCS = 1:
 1 = Synchronizes external clock input
 0 = Does not synchronize external clock input
 When TCS = 0:
 This bit is ignored.
- bit 1 **TCS:** Timer1 Clock Source Select bit⁽¹⁾
 1 = External clock is from pin, T1CK (on the rising edge)
 0 = Peripheral Clock (FP)
- bit 0 **Unimplemented:** Read as '0'

Note 1: When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.

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NOTES:

12.0 TIMER2/3

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Timers” (DS70362) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to [Section 4.0 “Memory Organization”](#) in this data sheet for device-specific register and bit information.

The Timer2/3 module is a 32-bit timer, which can also be configured as two independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2 and Timer3 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare modules (Timer2 and Timer3 only)

Individually, both of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON and T3CON registers. T2CON details are in [Register 12-1](#). T3CON details are in [Register 12-2](#).

For 32-bit timer/counter operation, Timer2 is the least significant word (lsw); Timer3 is the most significant word (msw) of the 32-bit timers.

Note: For 32-bit operation, T3CON control bits are ignored. Only T2CON control bits are used for setup and control. Timer2 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 interrupt flag.

A block diagram for an example 32-bit timer pair (Timer2/3) is shown in [Figure 12-2](#).

12.1 Timer Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

12.1.1 KEY RESOURCES

- “Timers” (DS70362) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

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FIGURE 12-1: TIMERx BLOCK DIAGRAM (x = 2,3)

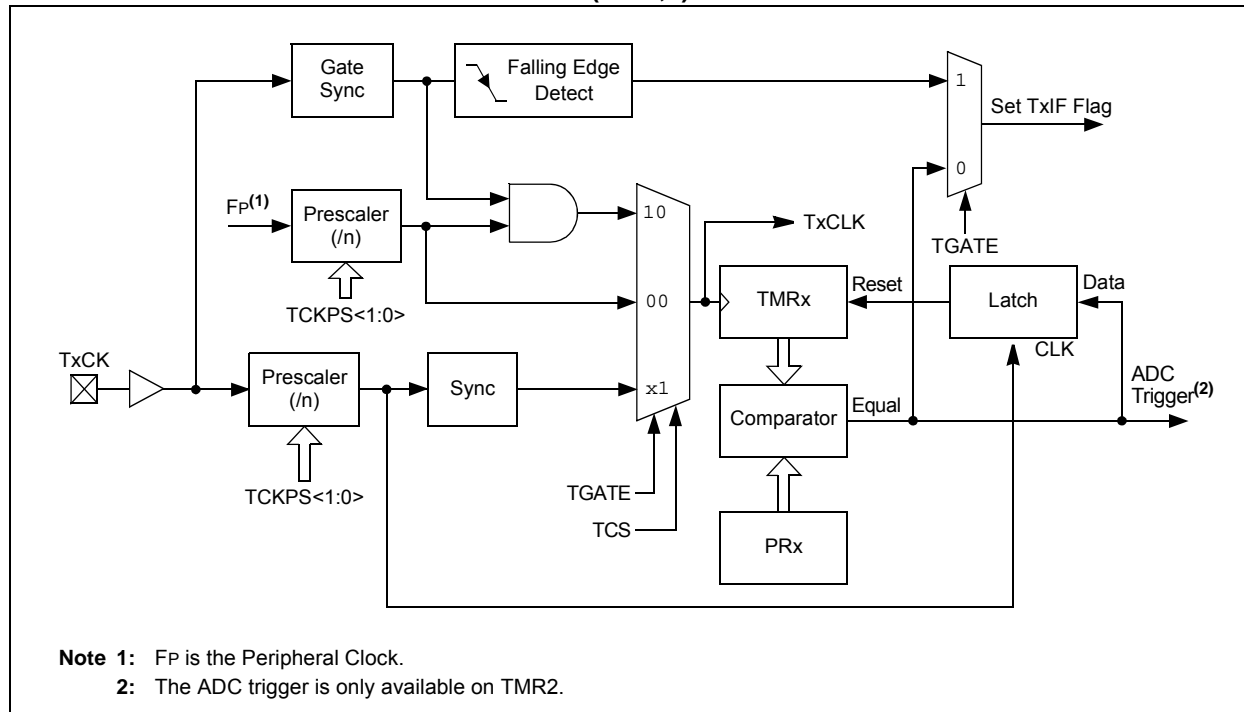
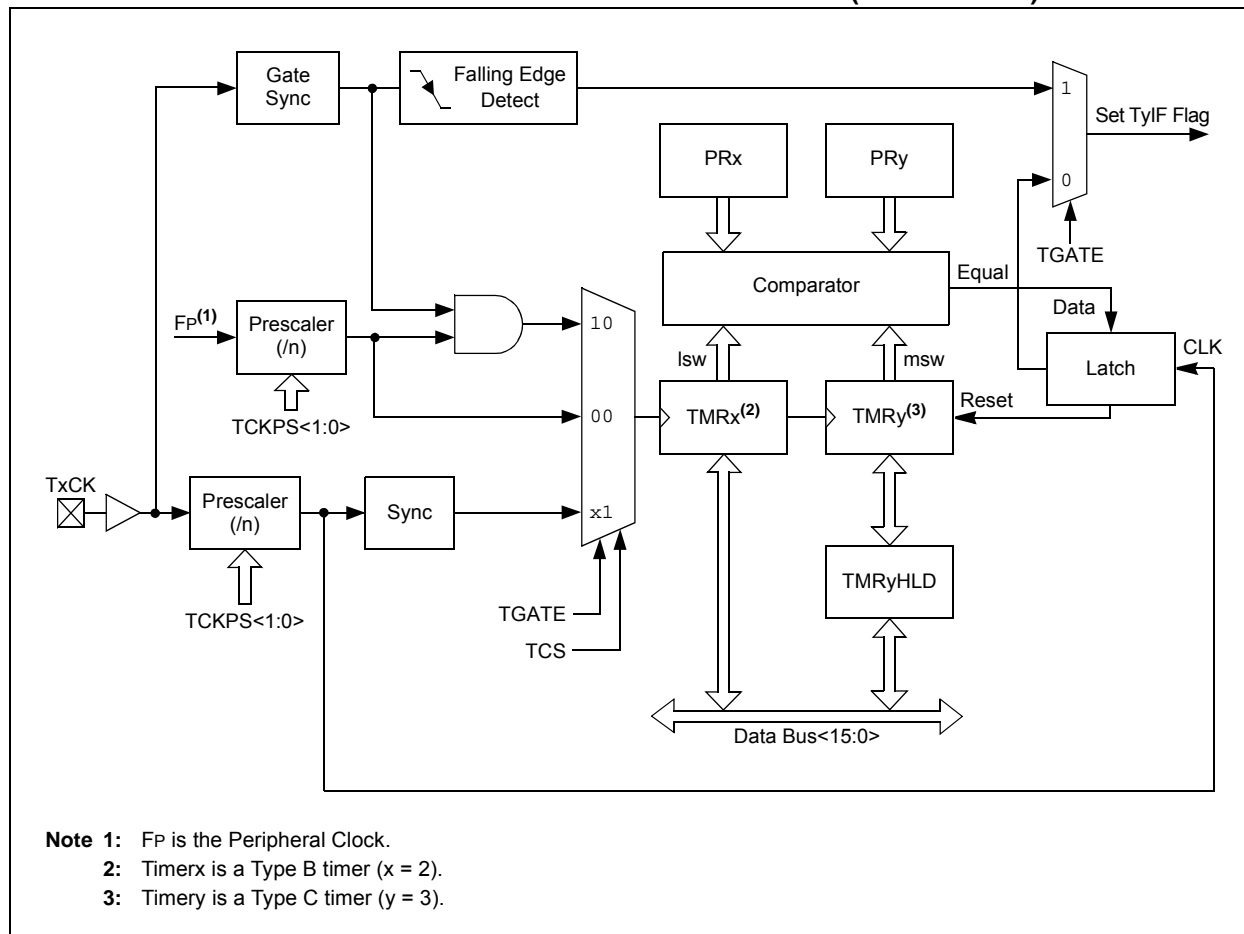


FIGURE 12-2: TYPE B/TIME C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)



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12.2 Timer2/3 Control Registers

REGISTER 12-1: T2CON: TIMER2 CONTROL REGISTER

| | | | | | | | |
|--------|-----|-------|-----|-----|-----|-------|-----|
| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| TON | — | TSIDL | — | — | — | — | — |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-------|--------|--------|-------|-----|-------|-----|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 |
| — | TGATE | TCKPS1 | TCKPS0 | T32 | — | TCS | — |
| bit 7 | | | | | | bit 0 | |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 15 **TON:** Timer2 On bit
 When T32 = 1:
 1 = Starts 32-bit Timer2/3
 0 = Stops 32-bit Timer2/3
 When T32 = 0:
 1 = Starts 16-bit Timer2
 0 = Stops 16-bit Timer2
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **TSIDL:** Timer2 Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-7 **Unimplemented:** Read as '0'
- bit 6 **TGATE:** Timer2 Gated Time Accumulation Enable bit
 When TCS = 1:
 This bit is ignored.
 When TCS = 0:
 1 = Gated time accumulation is enabled
 0 = Gated time accumulation is disabled
- bit 5-4 **TCKPS<1:0>:** Timer2 Input Clock Prescale Select bits
 11 = 1:256
 10 = 1:64
 01 = 1:8
 00 = 1:1
- bit 3 **T32:** 32-Bit Timer Mode Select bit
 1 = Timer2 and Timer3 form a single 32-bit timer
 0 = Timer2 and Timer3 act as two 16-bit timers
- bit 2 **Unimplemented:** Read as '0'
- bit 1 **TCS:** Timer2 Clock Source Select bit
 1 = External clock is from pin, T2CK (on the rising edge)
 0 = Peripheral Clock (FP)
- bit 0 **Unimplemented:** Read as '0'

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REGISTER 12-2: T3CON: TIMER3 CONTROL REGISTER

| | | | | | | | |
|--------------------|-----|----------------------|-----|-----|-----|-------|-----|
| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| TON ⁽¹⁾ | — | TSIDL ⁽²⁾ | — | — | — | — | — |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|----------------------|-----------------------|-----------------------|-----|-----|--------------------|-----|
| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 |
| — | TGATE ⁽¹⁾ | TCKPS1 ⁽¹⁾ | TCKPS0 ⁽¹⁾ | — | — | TCS ⁽¹⁾ | — |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **TON:** Timer3 On bit⁽¹⁾
 1 = Starts 16-bit Timer3
 0 = Stops 16-bit Timer3
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **TSIDL:** Timer3 Stop in Idle Mode bit⁽²⁾
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-7 **Unimplemented:** Read as '0'
- bit 6 **TGATE:** Timer3 Gated Time Accumulation Enable bit⁽¹⁾
 When TCS = 1:
 This bit is ignored.
 When TCS = 0:
 1 = Gated time accumulation is enabled
 0 = Gated time accumulation is disabled
- bit 5-4 **TCKPS<1:0>:** Timer3 Input Clock Prescale Select bits⁽¹⁾
 11 = 1:256
 10 = 1:64
 01 = 1:8
 00 = 1:1
- bit 3-2 **Unimplemented:** Read as '0'
- bit 1 **TCS:** Timer3 Clock Source Select bit⁽¹⁾
 1 = External clock is from pin, T3CK (on the rising edge)
 0 = Peripheral Clock (FP)
- bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timer3 operation; all timer functions are set through T2CON.

2: When 32-bit timer operation is enabled (T32 = 1) in the Timer2 Control register (T2CON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

13.0 INPUT CAPTURE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Input Capture with Dedicated Timer**” (DS70000352) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurements. The dsPIC33EPXXGS202 family devices support one input capture channel.

Key features of the input capture module include:

- Hardware-Configurable for 32-Bit Operation in all modes by Cascading Two Adjacent Modules

- Synchronous and Trigger modes of Output Compare Operation, with up to Six User-Selectable Trigger/Sync Sources Available
- A 4-Level FIFO Buffer for Capturing and Holding Timer Values for Several Events
- Configurable Interrupt Generation
- Up to Four Clock Sources Available, Driving a Separate Internal 16-Bit Counter

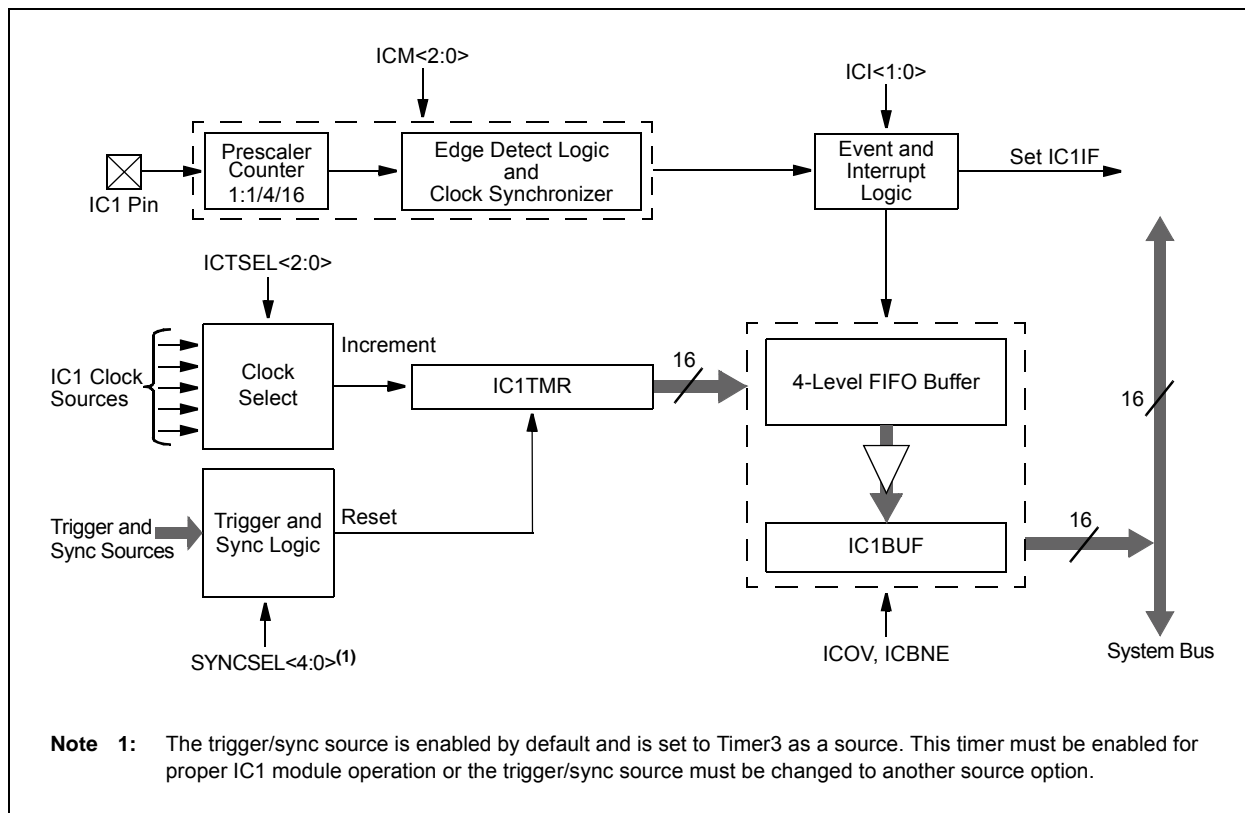
13.1 Input Capture Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

13.1.1 KEY RESOURCES

- “**Input Capture with Dedicated Timer**” (DS70000352) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections

FIGURE 13-1: INPUT CAPTURE MODULE BLOCK DIAGRAM



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13.2 Input Capture Control Registers

REGISTER 13-1: IC1CON1: INPUT CAPTURE CONTROL REGISTER 1

| | | | | | | | |
|--------|-----|--------|---------|---------|---------|-------|-----|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| — | — | ICSIDL | ICTSEL2 | ICTSEL1 | ICTSEL0 | — | — |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-------|-------|-------------|-------------|-------|-------|-------|
| U-0 | R/W-0 | R/W-0 | R-0, HC, HS | R-0, HC, HS | R/W-0 | R/W-0 | R/W-0 |
| — | IC11 | IC10 | ICOV | ICBNE | ICM2 | ICM1 | ICM0 |
| bit 7 | | | | | | | bit 0 |

| | | |
|-------------------|-----------------------------|------------------------------------|
| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **ICSIDL:** Input Capture Stop in Idle Control bit
 1 = Input capture will halt in CPU Idle mode
 0 = Input capture will continue to operate in CPU Idle mode
- bit 12-10 **ICTSEL<2:0>:** Input Capture Timer Select bits
 111 = Peripheral Clock (FP) is the clock source of the IC1
 110 = Reserved
 101 = Reserved
 100 = T1CLK is the clock source of the IC1 (only the synchronous clock is supported)
 011 = Reserved
 010 = Reserved
 001 = T2CLK is the clock source of the IC1
 000 = T3CLK is the clock source of the IC1
- bit 9-7 **Unimplemented:** Read as '0'
- bit 6-5 **ICI<1:0>:** Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
 11 = Interrupt on every fourth capture event
 10 = Interrupt on every third capture event
 01 = Interrupt on every second capture event
 00 = Interrupt on every capture event
- bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
 1 = Input capture buffer overflow has occurred
 0 = No input capture buffer overflow has occurred
- bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
 1 = Input capture buffer is not empty, at least one more capture value can be read
 0 = Input capture buffer is empty
- bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
 111 = Input capture functions as an interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
 110 = Unused (module is disabled)
 101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
 100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
 011 = Capture mode, every rising edge (Simple Capture mode)
 010 = Capture mode, every falling edge (Simple Capture mode)
 001 = Capture mode, every rising and falling edge (Edge Detect mode, (ICI<1:0>) is not used in this mode)
 000 = Input capture is turned off

dsPIC33EPXXGS202 FAMILY

REGISTER 13-2: IC1CON2: INPUT CAPTURE CONTROL REGISTER 2

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-----------------------|-------------------------|-----|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| R/W-0 | R/W-0, HS | U-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-1 |
| ICTRIG ⁽¹⁾ | TRIGSTAT ⁽²⁾ | — | SYNCSEL4 ⁽³⁾ | SYNCSEL3 ⁽³⁾ | SYNCSEL2 ⁽³⁾ | SYNCSEL1 ⁽³⁾ | SYNCSEL0 ⁽³⁾ |
| bit 7 | | | | | | | bit 0 |

| | | | |
|-------------------|----------------------------|------------------------------------|--------------------|
| Legend: | HS = Hardware Settable bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ICTRIG:** Input Capture Trigger Operation Select bit⁽¹⁾

1 = Input source used to trigger the input capture timer (Trigger mode)

0 = Input source used to synchronize the input capture timer to a timer of another module (Synchronization mode)

bit 6 **TRIGSTAT:** Timer Trigger Status bit⁽²⁾

1 = IC1TMR has been triggered and is running

0 = IC1TMR has not been triggered and is being held clear

bit 5 **Unimplemented:** Read as '0'

Note 1: The input source is selected by the SYNCSEL<4:0> bits of the IC1CON2 register.

2: This bit is set by the selected input source (selected by SYNCSEL<4:0> bits); it can be read, set and cleared in software.

3: Do not use the IC1 module as its own sync or trigger source.

4: This option should only be selected as a trigger source and not as a synchronization source.

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REGISTER 13-2: IC1CON2: INPUT CAPTURE CONTROL REGISTER 2 (CONTINUED)

| | |
|---------|---|
| bit 4-0 | SYNCSEL<4:0> : Input Source Select for Synchronization and Trigger Operation bits ⁽³⁾ |
| | 11111 = No sync or trigger source for IC1 |
| | 11110 = Reserved |
| | 11101 = Reserved |
| | 11100 = Reserved |
| | 11011 = Reserved |
| | 11010 = Reserved |
| | 11001 = CMP2 module synchronizes or triggers IC1 ⁽⁴⁾ |
| | 11000 = CMP1 module synchronizes or triggers IC1 ⁽⁴⁾ |
| | 10111 = Reserved |
| | 10110 = Reserved |
| | 10101 = Reserved |
| | 10100 = Reserved |
| | 10011 = Reserved |
| | 10010 = Reserved |
| | 10001 = Reserved |
| | 10000 = Reserved |
| | 01111 = Reserved |
| | 01110 = Reserved |
| | 01101 = Timer3 synchronizes or triggers IC1 (default) |
| | 01100 = Timer2 synchronizes or triggers IC1 |
| | 01011 = Timer1 synchronizes or triggers IC1 |
| | 01010 = Reserved |
| | 01001 = Reserved |
| | 01000 = Reserved |
| | 00111 = Reserved |
| | 00110 = Reserved |
| | 00101 = Reserved |
| | 00100 = Reserved |
| | 00011 = Reserved |
| | 00010 = Reserved |
| | 00001 = OC1 module synchronizes or triggers IC1 |
| | 00000 = No sync or trigger source for IC1 |

- Note 1:** The input source is selected by the SYNCSEL<4:0> bits of the IC1CON2 register.
- 2:** This bit is set by the selected input source (selected by SYNCSEL<4:0> bits); it can be read, set and cleared in software.
- 3:** Do not use the IC1 module as its own sync or trigger source.
- 4:** This option should only be selected as a trigger source and not as a synchronization source.

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14.0 OUTPUT COMPARE

Note 1: This data sheet summarizes the features of the dsPIC33EPXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Output Compare with Dedicated Timer**” (DS70005159) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The output compare module can select one of four available clock sources for its time base. The module compares the value of the timer with the value of one or two Compare registers, depending on the operating mode selected. The state of the output pin changes when the timer value matches the Compare register value. The output compare module generates either a

single output pulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events.

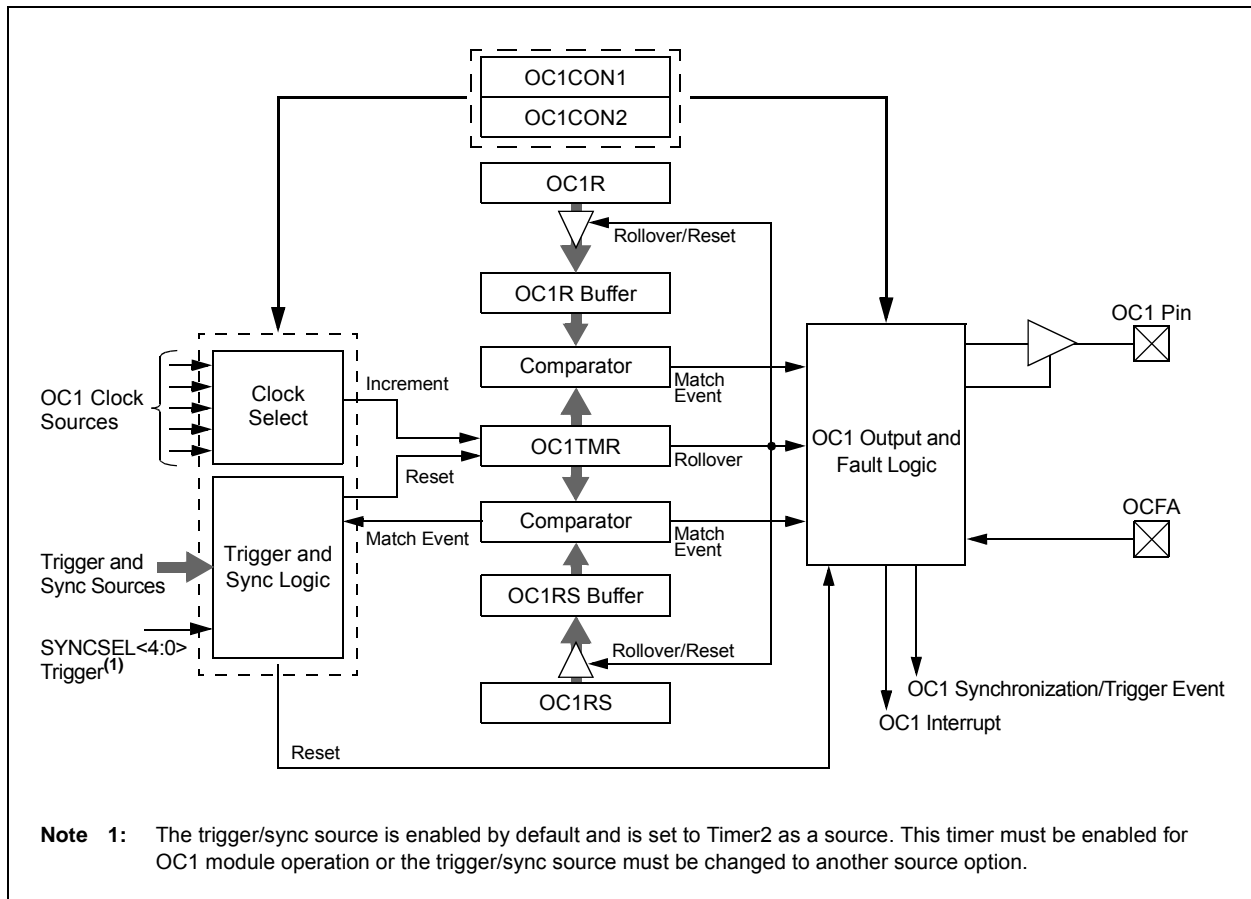
14.1 Output Compare Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

14.1.1 KEY RESOURCES

- “**Output Compare with Dedicated Timer**” (DS70005159) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

FIGURE 14-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



Note 1: The trigger/sync source is enabled by default and is set to Timer2 as a source. This timer must be enabled for OC1 module operation or the trigger/sync source must be changed to another source option.

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14.2 Output Compare Control Registers

REGISTER 14-1: OC1CON1: OUTPUT COMPARE CONTROL REGISTER 1

| | | | | | | | |
|--------|-----|--------|---------|---------|---------|-------|-----|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | — |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|--------|-----|-----|------------|----------|-------|-------|-------|
| R/W-0 | U-0 | U-0 | R/W-0, HSC | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| ENFLTA | — | — | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 |
| bit 7 | | | | | | bit 0 | |

| | | | |
|-------------------|---------------------------------------|------------------------------------|--------------------|
| Legend: | HSC = Hardware Settable/Clearable bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **OCSIDL:** Output Compare Stop in Idle Mode Control bit
 - 1 = Output compare halts in CPU Idle mode
 - 0 = Output compare continues to operate in CPU Idle mode
- bit 12-10 **OCTSEL<2:0>:** Output Compare Clock Select bits
 - 111 = Peripheral Clock (FP)
 - 110 = Reserved
 - 101 = Reserved
 - 100 = T1CLK is the clock source of the OC1 (only the synchronous clock is supported)
 - 011 = Reserved
 - 010 = Reserved
 - 001 = T3CLK is the clock source of the OC1
 - 000 = T2CLK is the clock source of the OC1
- bit 9-8 **Unimplemented:** Read as '0'
- bit 7 **ENFLTA:** Fault A Input Enable bit
 - 1 = Output Compare Fault A input (OCFA) is enabled
 - 0 = Output Compare Fault A input (OCFA) is disabled
- bit 6-5 **Unimplemented:** Read as '0'
- bit 4 **OCFLTA:** PWM Fault A Condition Status bit
 - 1 = PWM Fault A condition on the OCFA pin has occurred
 - 0 = No PWM Fault A condition on the OCFA pin has occurred
- bit 3 **TRIGMODE:** Trigger Status Mode Select bit
 - 1 = TRIGSTAT (OC1CON2<6>) is cleared when OC1RS = OC1TMR or in software
 - 0 = TRIGSTAT is cleared only by software

Note 1: OC1R and OC1RS are double-buffered in PWM mode only.

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REGISTER 14-1: OC1CON1: OUTPUT COMPARE CONTROL REGISTER 1 (CONTINUED)

- bit 2-0 **OCM<2:0>**: Output Compare Mode Select bits
- 111 = Center-Aligned PWM mode: Output is set high when OC1TMR = OC1R and set low when OC1TMR = OC1RS⁽¹⁾
 - 110 = Edge-Aligned PWM mode: Output is set high when OC1TMR = 0 and set low when OC1TMR = OC1R⁽¹⁾
 - 101 = Double Compare Continuous Pulse mode: Initializes OC1 pin low, toggles OC1 state continuously on alternate matches of OC1R and OC1RS
 - 100 = Double Compare Single-Shot mode: Initializes OC1 pin low, toggles OC1 state on matches of OC1R and OC1RS for one cycle
 - 011 = Single Compare mode: Compare event with OC1R, continuously toggles OC1 pin
 - 010 = Single Compare Single-Shot mode: Initializes OC1 pin high, compare event with OC1R, forces OC1 pin low
 - 001 = Single Compare Single-Shot mode: Initializes OC1 pin low, compare event with OC1R, forces OC1 pin high
 - 000 = Output compare channel is disabled

Note 1: OC1R and OC1RS are double-buffered in PWM mode only.

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REGISTER 14-2: OC1CON2: OUTPUT COMPARE CONTROL REGISTER 2

| | | | | | | | | |
|--------|--------|----------|-------|-----|-----|-----|-----|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | |
| FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | — | |
| bit 15 | | | | | | | | bit 8 |

| | | | | | | | | |
|--------|-----------|--------|----------|----------|----------|----------|----------|-------|
| R/W-0 | R/W-0, HS | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | |
| OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | |
| bit 7 | | | | | | | | bit 0 |

| | | | |
|-------------------|----------------------------|------------------------------------|--------------------|
| Legend: | HS = Hardware Settable bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

- bit 15 **FLTMD:** Fault Mode Select bit
 - 1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTA bit is cleared in software and a new PWM period starts
 - 0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts
- bit 14 **FLTOUT:** Fault Out bit
 - 1 = PWM output is driven high on a Fault
 - 0 = PWM output is driven low on a Fault
- bit 13 **FLTTRIEN:** Fault Output State Select bit
 - 1 = OC1 pin is tri-stated on a Fault condition
 - 0 = OC1 pin I/O state is defined by the FLTOUT bit on a Fault condition
- bit 12 **OCINV:** Output Compare Invert bit
 - 1 = OC1 output is inverted
 - 0 = OC1 output is not inverted
- bit 11-8 **Unimplemented:** Read as '0'
- bit 7 **OCTRIG:** Output Compare Trigger/Sync Select bit
 - 1 = Triggers OC1 from the source designated by the SYNCSEL<4:0> bits
 - 0 = Synchronizes OC1 with the source designated by the SYNCSEL<4:0> bits
- bit 6 **TRIGSTAT:** Timer Trigger Status bit
 - 1 = Timer source has been triggered and is running
 - 0 = Timer source has not been triggered and is being held clear
- bit 5 **OCTRIS:** Output Compare Output Pin Direction Select bit
 - 1 = Output compare is tri-stated
 - 0 = Output compare module drives the OCx pin

Note 1: This option should only be selected as a trigger source and not as a synchronization source.

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REGISTER 14-2: OC1CON2: OUTPUT COMPARE CONTROL REGISTER 2 (CONTINUED)

| | |
|---------|---|
| bit 4-0 | SYNCSEL<4:0> : Trigger/Synchronization Source Selection bits |
| 11111 | = OC1RS compare event is used for synchronization |
| 11110 | = INT2 pin synchronizes or triggers OC1 |
| 11101 | = INT1 pin synchronizes or triggers OC1 |
| 11100 | = Reserved |
| 11011 | = Reserved |
| 11010 | = Reserved |
| 11001 | = CMP2 module triggers OC1 ⁽¹⁾ |
| 11000 | = CMP1 module triggers OC1 ⁽¹⁾ |
| 10111 | = Reserved |
| 10110 | = Reserved |
| 10101 | = Reserved |
| 10100 | = Reserved |
| 10011 | = Reserved |
| 10010 | = Reserved |
| 10001 | = Reserved |
| 10000 | = IC1 input capture interrupt event synchronizes or triggers OC1 |
| 01111 | = Reserved |
| 01110 | = Reserved |
| 01101 | = Timer3 synchronizes or triggers OC1 |
| 01100 | = Timer2 synchronizes or triggers OC1 (default) |
| 01011 | = Timer1 synchronizes or triggers OC1 |
| 01010 | = Reserved |
| 01001 | = Reserved |
| 01000 | = Reserved |
| 00111 | = Reserved |
| 00110 | = Reserved |
| 00101 | = IC1 input capture event synchronizes or triggers OC1 |
| 00100 | = Reserved |
| 00011 | = Reserved |
| 00010 | = Reserved |
| 00001 | = Reserved |
| 00000 | = No sync or trigger source for OC1 |

Note 1: This option should only be selected as a trigger source and not as a synchronization source.

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NOTES:

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15.0 HIGH-SPEED PWM

Note: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**High-Speed PWM Module**” (DS70000323) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

The high-speed PWM module on dsPIC33EPXXGS202 devices supports a wide variety of PWM modes and output formats. This PWM module is ideal for power conversion applications, such as:

- AC/DC Converters
- DC/DC Converters
- Power Factor Correction
- Uninterruptible Power Supply (UPS)
- Inverters
- Battery Chargers
- Digital Lighting

15.1 Features Overview

The high-speed PWM module incorporates the following features:

- Three PWM Generators with Two Outputs per Generator
- Two Master Time Base Modules
- Individual Time Base and Duty Cycle for each PWM Output
- Duty Cycle, Dead Time, Phase Shift and a Frequency Resolution of 1.04 ns
- Independent Fault and Current-Limit Inputs
- Redundant Output
- True Independent Output
- Center-Aligned PWM mode
- Output Override Control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Dual Trigger from PWM to Analog-to-Digital Converter (ADC)
- PWMxL and PWMxH Output Pin Swapping
- Independent PWMx Frequency, Duty Cycle and Phase-Shift Changes
- Enhanced Leading-Edge Blanking (LEB) Functionality
- PWMx Capture Functionality

Note: Duty cycle, dead time, phase shift and frequency resolution is 8.32 ns in Center-Aligned PWM mode.

Figure 15-1 conceptualizes the PWM module in a simplified block diagram. Figure 15-2 illustrates how the module hardware is partitioned for each PWM output pair for the Complementary PWM mode.

The PWM module contains three PWM generators. The module has up to six PWM output pins: PWM1H/PWM1L through PWM3H/PWM3L. For complementary outputs, these six I/O pins are grouped into high/low pairs.

15.2 Feature Description

The PWM module is designed for applications that require:

- High resolution at high PWM frequencies
- The ability to drive Standard, Edge-Aligned, Center-Aligned Complementary and Push-Pull mode outputs
- The ability to create multiphase PWM outputs

Two common, medium power converter topologies are push-pull and half-bridge. These designs require the PWM output signal to be switched between alternate pins, as provided by the Push-Pull PWM mode.

Phase-shifted PWM describes the situation where each PWM generator provides outputs, but the phase relationship between the generator outputs is specifiable and changeable.

Multiphase PWM is often used to improve DC/DC Converter load transient response, and reduce the size of output filter capacitors and inductors. Multiple DC/DC Converters are often operated in parallel, but phase shifted in time. A single PWM output operating at 250 kHz has a period of 4 μ s, but an array of four PWM channels, staggered by 1 μ s each, yields an effective switching frequency of 1 MHz. Multiphase PWM applications typically use a fixed-phase relationship.

Variable phase PWM is useful in Zero Voltage Transition (ZVT) power converters. Here, the PWM duty cycle is always 50% and the power flow is controlled by varying the relative phase shift between the two PWM generators.

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15.2.1 WRITE-PROTECTED REGISTERS

On the dsPIC33EPXXGS202 family devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FDEVOPT<0>). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring PWMLOCK = 0.

To gain write access to these locked registers, the user application must write two consecutive values (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

The correct unlocking sequence is described in [Example 15-1](#).

EXAMPLE 15-1: PWM WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

```
; Writing to FCLCON1 register requires unlock sequence

mov #0xabcd, w10      ; Load first unlock key to w10 register
mov #0x4321, w11      ; Load second unlock key to w11 register
mov #0x0000, w0       ; Load desired value of FCLCON1 register in w0
mov w10, PWMKEY      ; Write first unlock key to PWMKEY register
mov w11, PWMKEY      ; Write second unlock key to PWMKEY register
mov w0, FCLCON1      ; Write desired value to FCLCON1 register

; Set PWM ownership and polarity using the IOCON1 register
; Writing to IOCON1 register requires unlock sequence

mov #0xabcd, w10      ; Load first unlock key to w10 register
mov #0x4321, w11      ; Load second unlock key to w11 register
mov #0xF000, w0       ; Load desired value of IOCON1 register in w0
mov w10, PWMKEY      ; Write first unlock key to PWMKEY register
mov w11, PWMKEY      ; Write second unlock key to PWMKEY register
mov w0, IOCON1       ; Write desired value to IOCON1 register
```

15.3 PWM Resources

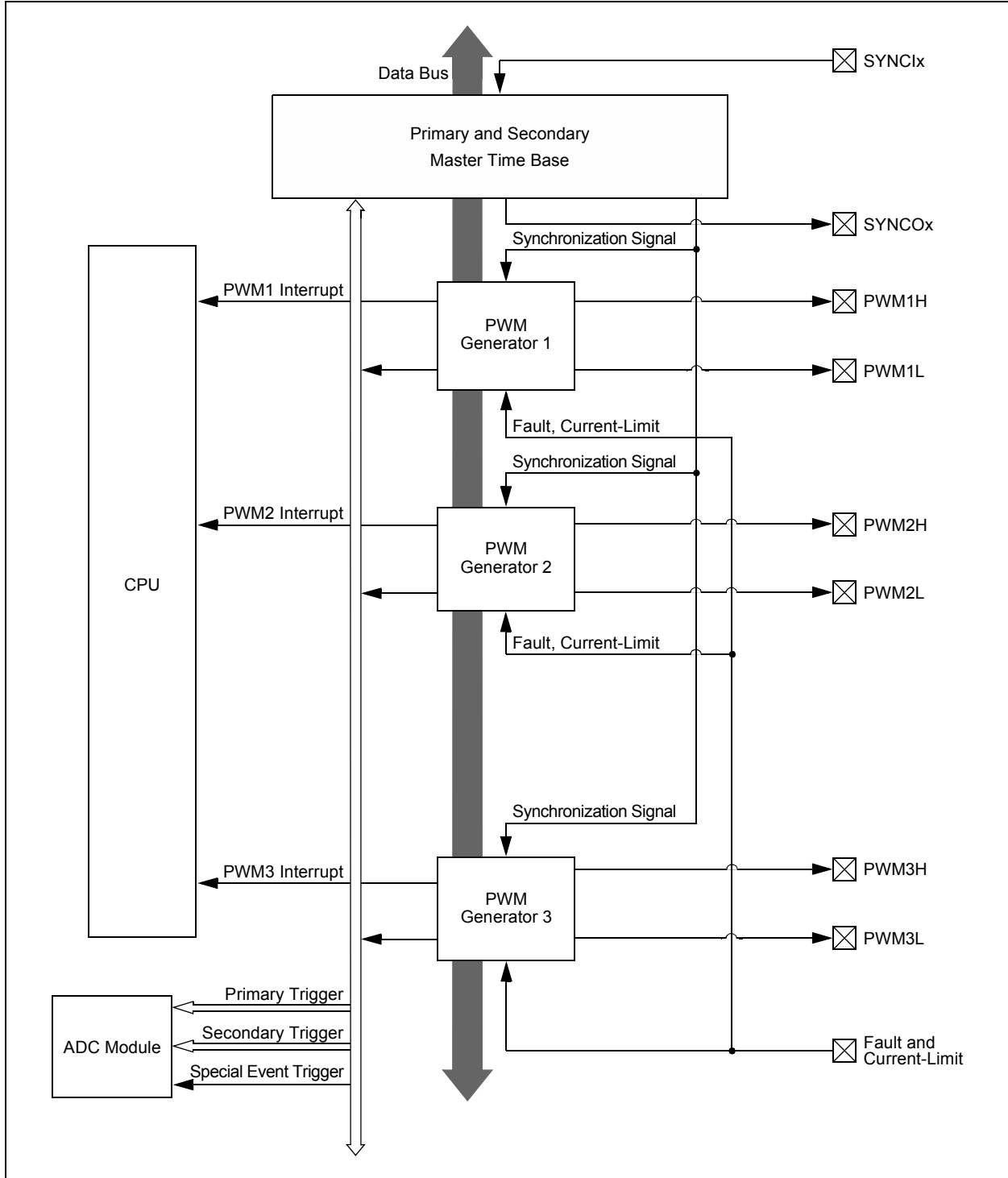
Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

15.3.1 KEY RESOURCES

- “**High-Speed PWM Module**” (DS70000323) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

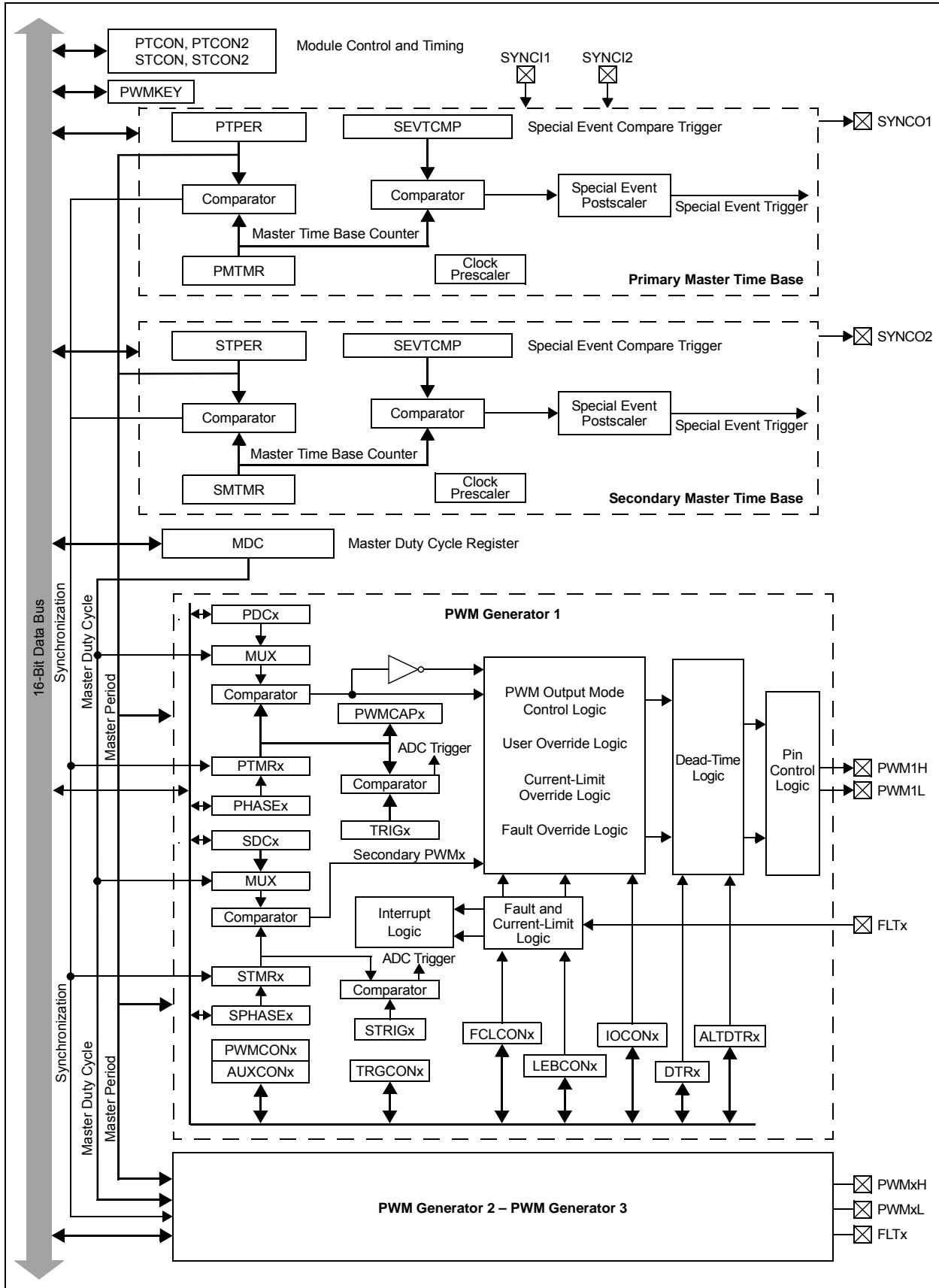
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FIGURE 15-1: HIGH-SPEED PWM MODULE ARCHITECTURAL DIAGRAM



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FIGURE 15-2: SIMPLIFIED CONCEPTUAL BLOCK DIAGRAM OF THE HIGH-SPEED PWM



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REGISTER 15-1: PTCON: PWM TIME BASE CONTROL REGISTER

| | | | | | | | |
|--------|-----|--------|---------|-------|---------------------|------------------------|------------------------|
| R/W-0 | U-0 | R/W-0 | HS/HC-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PTEN | — | PTSIDL | SESTAT | SEIEN | EIPU ⁽¹⁾ | SYNCPOL ⁽¹⁾ | SYNCOEN ⁽¹⁾ |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-----------------------|-------------------------|-------------------------|-------------------------|------------------------|------------------------|------------------------|------------------------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SYNCEN ⁽¹⁾ | SYNCSRC2 ⁽¹⁾ | SYNCSRC1 ⁽¹⁾ | SYNCSRC0 ⁽¹⁾ | SEVTPS3 ⁽¹⁾ | SEVTPS2 ⁽¹⁾ | SEVTPS1 ⁽¹⁾ | SEVTPS0 ⁽¹⁾ |
| bit 7 | | | | | | bit 0 | |

| | | |
|-------------------|-----------------------------|--|
| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15 **PTEN:** PWM Module Enable bit
1 = PWM module is enabled
0 = PWM module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **PTSIDL:** PWM Time Base Stop in Idle Mode bit
1 = PWM time base halts in CPU Idle mode
0 = PWM time base runs in CPU Idle mode
- bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending
- bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled
- bit 10 **EIPU:** Enable Immediate Period Updates bit⁽¹⁾
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWM cycle boundaries
- bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit⁽¹⁾
1 = SYNCIx/SYNCO1 polarity is inverted (active-low)
0 = SYNCIx/SYNCO1 is active-high
- bit 8 **SYNCOEN:** Primary Time Base Synchronization Enable bit⁽¹⁾
1 = SYNCO1 output is enabled
0 = SYNCO1 output is disabled
- bit 7 **SYNCEN:** External Time Base Synchronization Enable bit⁽¹⁾
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled
- bit 6-4 **SYNCSRC<2:0>:** Synchronous Source Selection bits⁽¹⁾
111 = Reserved
101 = Reserved
100 = Reserved
011 = Reserved
010 = Reserved
001 = SYNCI2
000 = SYNCI1

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCIx feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

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REGISTER 15-1: PTCON: PWM TIME BASE CONTROL REGISTER (CONTINUED)

bit 3-0 **SEVTPS<3:0>**: PWM Special Event Trigger Output Postscaler Select bits⁽¹⁾
 1111 = 1:16 Postscaler generates a Special Event Trigger on every sixteenth compare match event
 •
 •
 0001 = 1:2 Postscaler generates a Special Event Trigger on every second compare match event
 0000 = 1:1 Postscaler generates a Special Event Trigger on every compare match event

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCIx feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

REGISTER 15-2: PTCON2: PWM CLOCK DIVIDER SELECT REGISTER 2

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----------------------------|-------|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | PCLKDIV<2:0> ⁽¹⁾ | | |
| bit 7 | | | | | bit 0 | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-3 **Unimplemented:** Read as '0'
 bit 2-0 **PCLKDIV<2:0>**: PWM Input Clock Prescaler (Divider) Select bits⁽¹⁾
 111 = Reserved
 110 = Divide-by-64, maximum PWM timing resolution
 101 = Divide-by-32, maximum PWM timing resolution
 100 = Divide-by-16, maximum PWM timing resolution
 011 = Divide-by-8, maximum PWM timing resolution
 010 = Divide-by-4, maximum PWM timing resolution
 001 = Divide-by-2, maximum PWM timing resolution
 000 = Divide-by-1, maximum PWM timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

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REGISTER 15-3: PTPER: PWM PRIMARY MASTER TIME BASE PERIOD REGISTER^(1,2)

| | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| PTPER<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
| PTPER<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PTPER<15:0>**: Primary Master Time Base (PMTMR) Period Value bits

- Note 1:** The PWM time base has a minimum value of 0x0010 and a maximum value of 0xFFFF.
2: Any period value that is less than 0x0028 must have the Least Significant 3 bits set to '0', thus yielding a period resolution at 8.32 ns (at fastest auxiliary clock rate).

REGISTER 15-4: SEVTCMP: PWM SPECIAL EVENT COMPARE REGISTER⁽¹⁾

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SEVTCMP<12:5> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|--------------|-------|-------|-------|-------|-----|-----|-----|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| SEVTCMP<4:0> | | | | | — | — | — |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-3 **SEVTCMP<12:0>**: Special Event Compare Count Value bits

bit 2-0 **Unimplemented:** Read as '0'

- Note 1:** One LSB = 1.04 ns (at fastest auxiliary clock rate); therefore, the minimum SEVTCMP resolution is 8.32 ns.

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REGISTER 15-5: STCON: PWM SECONDARY MASTER TIME BASE CONTROL REGISTER

| | | | | | | | |
|--------|-----|-----|---------|-------|---------------------|---------|---------|
| U-0 | U-0 | U-0 | HS/HC-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | SESTAT | SEIEN | EIPU ⁽¹⁾ | SYNCPOL | SYNCOEN |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------|----------|----------|----------|---------|---------|---------|---------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SYNCEN | SYNCSRC2 | SYNCSRC1 | SYNCSRC0 | SEVTPS3 | SEVTPS2 | SEVTPS1 | SEVTPS0 |
| bit 7 | | | | | | | bit 0 |

| | | |
|-------------------|----------------------------|------------------------------------|
| Legend: | HS = Hardware Settable bit | HC = Hardware Clearable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **SESTAT:** Special Event Interrupt Status bit
 1 = Secondary special event interrupt is pending
 0 = Secondary special event interrupt is not pending
- bit 11 **SEIEN:** Special Event Interrupt Enable bit
 1 = Secondary special event interrupt is enabled
 0 = Secondary special event interrupt is disabled
- bit 10 **EIPU:** Enable Immediate Period Updates bit⁽¹⁾
 1 = Active Secondary Period register is updated immediately
 0 = Active Secondary Period register updates occur on PWM cycle boundaries
- bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit
 1 = SYNCIx/SYNCO2 polarity is inverted (active-low)
 0 = SYNCIx/SYNCO2 polarity is active-high
- bit 8 **SYNCOEN:** Secondary Master Time Base Synchronization Enable bit
 1 = SYNCO2 output is enabled.
 0 = SYNCO2 output is disabled
- bit 7 **SYNCEN:** External Secondary Master Time Base Synchronization Enable bit
 1 = External synchronization of secondary time base is enabled
 0 = External synchronization of secondary time base is disabled
- bit 6-4 **SYNCSRC<2:0>:** Secondary Time Base Sync Source Selection bits
 111 = Reserved
 101 = Reserved
 100 = Reserved
 011 = Reserved
 010 = Reserved
 001 = SYNCI2
 000 = SYNCI1
- bit 3-0 **SEVTPS<3:0>:** PWM Secondary Special Event Trigger Output Postscaler Select bits
 1111 = 1:16 Postscale
 0001 = 1:2 Postscale
 0000 = 1:1 Postscale

Note 1: This bit only applies to the secondary master time base period.

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REGISTER 15-6: STCON2: PWM SECONDARY CLOCK DIVIDER SELECT REGISTER 2

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----------------------------|-------|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | PCLKDIV<2:0> ⁽¹⁾ | | |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **PCLKDIV<2:0>:** PWM Input Clock Prescaler (Divider) Select bits⁽¹⁾

- 111 = Reserved
- 110 = Divide-by-64, maximum PWM timing resolution
- 101 = Divide-by-32, maximum PWM timing resolution
- 100 = Divide-by-16, maximum PWM timing resolution
- 011 = Divide-by-8, maximum PWM timing resolution
- 010 = Divide-by-4, maximum PWM timing resolution
- 001 = Divide-by-2, maximum PWM timing resolution
- 000 = Divide-by-1, maximum PWM timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 15-7: STPER: PWM SECONDARY MASTER TIME BASE PERIOD REGISTER^(1,2)

| | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| STPER<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| STPER<7:0> | | | | | | | |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **STPER<15:0>:** Secondary Master Time Base (SMTMR) Period Value bits

- Note 1:** The PWM time base has a minimum value of 0x0010 and a maximum value of 0xFFFF8.
Note 2: Any period value that is less than 0x0028 must have the Least Significant three bits set to '0', thus yielding a period resolution at 8.32 ns (at fastest auxiliary clock rate).

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REGISTER 15-8: SSEVTCMP: PWM SECONDARY SPECIAL EVENT COMPARE REGISTER⁽¹⁾

| | | | | | | | |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SSEVTCMP<12:5> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|---------------|-------|-------|-------|-------|-----|-----|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| SSEVTCMP<4:0> | | | | | — | — | — |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-3 **SSEVTCMP<12:0>**: Special Event Compare Count Value bits

bit 2-0 **Unimplemented**: Read as '0'

Note 1: One LSB = 1.04 ns (at fastest auxiliary clock rate); therefore, the minimum SEVTCMP resolution is 8.32 ns.

REGISTER 15-9: CHOP: PWM CHOP CLOCK GENERATOR REGISTER⁽¹⁾

| | | | | | | | |
|----------|-----|-----|-----|-----|-----|----------|----------|
| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| CHPCLKEN | — | — | — | — | — | CHOPCLK6 | CHOPCLK5 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|----------|----------|----------|----------|----------|-----|-----|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| CHOPCLK4 | CHOPCLK3 | CHOPCLK2 | CHOPCLK1 | CHOPCLK0 | — | — | — |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **CHPCLKEN**: Enable Chop Clock Generator bit

1 = Chop clock generator is enabled
 0 = Chop clock generator is disabled

bit 14-10 **Unimplemented**: Read as '0'

bit 9-3 **CHOPCLK<6:0>**: Chop Clock Divider bits

Value is in 8.32 ns increments. The frequency of the chop clock signal is given by the following expression:

$$\text{Chop Frequency} = 1 / (16.64 * (\text{CHOPCLK}<6:0> + 1) * \text{Primary Master PWM Input Clock Period})$$

bit 2-0 **Unimplemented**: Read as '0'

Note 1: The chop clock generator operates with the primary PWM clock prescaler (PCLKDIV<2:0>) in the PTCN2 register ([Register 15-2](#)).

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REGISTER 15-10: MDC: PWM MASTER DUTY CYCLE REGISTER^(1,2)

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| MDC<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| MDC<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-0 **MDC<15:0>**: Master PWM Duty Cycle Value bits

Note 1: The smallest pulse width that can be generated on the PWMx output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of Period – 0x0008.

2: As the duty cycle gets closer to 0% or 100% of the PWM period (0 to 40 ns, depending on the mode of operation), PWM duty cycle resolution will increase from one to three LSBs.

REGISTER 15-11: PWMKEY: PWM PROTECTION LOCK/UNLOCK KEY REGISTER

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PWMKEY<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PWMKEY<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-0 **PWMKEY<15:0>**: PWM Protection Lock/Unlock Key Value bits

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REGISTER 15-12: PWMCONx: PWMx CONTROL REGISTER

| | | | | | | | |
|------------------------|-----------------------|---------|--------|-------|--------|--------------------|---------------------|
| HS/HC-0 | HS/HC-0 | HS/HC-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FLTSTAT ⁽¹⁾ | CLSTAT ⁽¹⁾ | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB ⁽³⁾ | MDCS ⁽³⁾ |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-------|-----|-----|-------|------------------------|----------------------|-------|
| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DTC1 | DTC0 | — | — | MTBS | CAM ^(2,3,4) | XPRES ⁽⁵⁾ | IUE |
| bit 7 | | | | | | bit 0 | |

| | | |
|-------------------|-----------------------------|--|
| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15 **FLTSTAT:** Fault Interrupt Status bit⁽¹⁾
 1 = Fault interrupt is pending
 0 = No Fault interrupt is pending
 This bit is cleared by setting FLTIEN = 0.
- bit 14 **CLSTAT:** Current-Limit Interrupt Status bit⁽¹⁾
 1 = Current-limit interrupt is pending
 0 = No current-limit interrupt is pending
 This bit is cleared by setting CLIEN = 0.
- bit 13 **TRGSTAT:** Trigger Interrupt Status bit
 1 = Trigger interrupt is pending
 0 = No trigger interrupt is pending
 This bit is cleared by setting TRGIEN = 0.
- bit 12 **FLTIEN:** Fault Interrupt Enable bit
 1 = Fault interrupt is enabled
 0 = Fault interrupt is disabled and the FLTSTAT bit is cleared
- bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
 1 = Current-limit interrupt is enabled
 0 = Current-limit interrupt is disabled and the CLSTAT bit is cleared
- bit 10 **TRGIEN:** Trigger Interrupt Enable bit
 1 = A trigger event generates an interrupt request
 0 = Trigger event interrupts are disabled and the TRGSTAT bit is cleared
- bit 9 **ITB:** Independent Time Base Mode bit⁽³⁾
 1 = PHASEx/SPHASEx registers provide the time base period for this PWMx generator
 0 = PTPER register provides timing for this PWMx generator
- bit 8 **MDCS:** Master Duty Cycle Register Select bit⁽³⁾
 1 = MDC register provides duty cycle information for this PWMx generator
 0 = PDCx and SDCx registers provide duty cycle information for this PWMx generator

- Note 1:** Software must clear the interrupt status here and in the corresponding IFSx register in the interrupt controller.
- 2:** The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
- 3:** These bits should not be changed after the PWM is enabled by setting PTEN (PTCON<15>) = 1.
- 4:** Center-Aligned mode ignores the Least Significant 3 bits of the Duty Cycle, Phase and Dead-Time registers. The highest Center-Aligned mode resolution available is 8.32 ns with the clock prescaler set to the fastest clock.
- 5:** Configure CLMOD (FCLCONx<8>) = 0 and ITB (PWMCONx<9>) = 1 to operate in External Period Reset mode.

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REGISTER 15-12: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

| | |
|---------|---|
| bit 7-6 | DTC<1:0> : Dead-Time Control bits 11 = Reserved 10 = Dead-time function is disabled 01 = Negative dead time is actively applied for Complementary Output mode 00 = Positive dead time is actively applied for all Output modes |
| bit 5-4 | Unimplemented : Read as '0' |
| bit 3 | MTBS : Master Time Base Select bit 1 = PWMx generator uses the secondary master time base for synchronization and the clock source for the PWMx generation logic (if secondary time base is available) 0 = PWMx generator uses the primary master time base for synchronization and the clock source for the PWMx generation logic |
| bit 2 | CAM : Center-Aligned Mode Enable bit ^(2,3,4) 1 = Center-Aligned mode is enabled 0 = Edge-Aligned mode is enabled |
| bit 1 | XPRES : External PWMx Reset Control bit ⁽⁵⁾ 1 = Current-limit source resets the time base for this PWMx generator if it is in Independent Time Base mode 0 = External pins do not affect the PWMx time base |
| bit 0 | IUE : Immediate Update Enable bit 1 = Updates to the active Duty Cycle, Phase Offset, Dead-Time and local Time Base Period registers are immediate 0 = Updates to the active Duty Cycle, Phase Offset, Dead-Time and local Time Base Period registers are synchronized to the local PWMx time base |

- Note 1:** Software must clear the interrupt status here and in the corresponding IFSx register in the interrupt controller.
- 2:** The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
- 3:** These bits should not be changed after the PWM is enabled by setting PTEN (PTCON<15>) = 1.
- 4:** Center-Aligned mode ignores the Least Significant 3 bits of the Duty Cycle, Phase and Dead-Time registers. The highest Center-Aligned mode resolution available is 8.32 ns with the clock prescaler set to the fastest clock.
- 5:** Configure CLMOD (FCLCONx<8>) = 0 and ITB (PWMCONx<9>) = 1 to operate in External Period Reset mode.

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REGISTER 15-13: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER^(1,2,3)

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PDCx<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PDCx<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-0 **PDCx<15:0>**: PWMx Generator Duty Cycle Value bits

- Note 1:** In Independent PWM mode, the PDCx register controls the PWMxH duty cycle only. In the Complementary, Redundant and Push-Pull PWM modes, the PDCx register controls the duty cycle of both the PWMxH and PWMxL.
- 2:** The smallest pulse width that can be generated on the PWMx output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of Period – 0x0008.
- 3:** As the duty cycle gets closer to 0% or 100% of the PWM period (0 to 40 ns, depending on the mode of operation), PWM duty cycle resolution will increase from one to three LSBs.

REGISTER 15-14: SDCx: PWMx SECONDARY DUTY CYCLE REGISTER^(1,2,3)

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SDCx<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SDCx<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-0 **SDCx<15:0>**: Secondary Duty Cycle for PWMxL Output Pin bits

- Note 1:** The SDCx register is used in Independent PWM mode only. When used in Independent PWM mode, the SDCx register controls the PWMxL duty cycle.
- 2:** The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of Period – 0x0008.
- 3:** As the duty cycle gets closer to 0% or 100% of the PWM period (0 to 40 ns, depending on the mode of operation), PWM duty cycle resolution will increase from one to three LSBs.

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REGISTER 15-15: PHASE_x: PWM_x PRIMARY PHASE-SHIFT REGISTER^(1,2)

| | | | | | | | |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PHASE _x <15:8> | | | | | | | |
| bit 15 | | | | | | | |
| bit 8 | | | | | | | |

| | | | | | | | |
|--------------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PHASE _x <7:0> | | | | | | | |
| bit 7 | | | | | | | |
| bit 0 | | | | | | | |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15-0 **PHASE_x<15:0>**: PWM_x Phase-Shift Value or Independent Time Base Period for the PWM_x Generator bits

Note 1: If PWMCON_x<9> = 0, the following applies based on the mode of operation:

- Complementary, Redundant and Push-Pull Output mode (IOCON_x<11:10> = 00, 01 or 10); PHASE_x<15:0> = Phase-shift value for PWM_xH and PWM_xL outputs
- True Independent Output mode (IOCON_x<11:10> = 11); PHASE_x<15:0> = Phase-shift value for PWM_xH only
- When the PHASE_x/SPHASE_x registers provide the phase shift with respect to the master time base; therefore, the valid range is 0x0000 through period

2: If PWMCON_x<9> = 1, the following applies based on the mode of operation:

- Complementary, Redundant, and Push-Pull Output mode (IOCON_x<11:10> = 00, 01 or 10); PHASE_x<15:0> = Independent time base period value for PWM_xH and PWM_xL
- True Independent Output mode (IOCON_x<11:10> = 11); PHASE_x<15:0> = Independent time base period value for PWM_xH only
- When the PHASE_x/SPHASE_x registers provide the local period, the valid range is 0x0000 through 0xFFFF8

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REGISTER 15-16: SPHASE_x: PWM_x SECONDARY PHASE-SHIFT REGISTER^(1,2)

| | | | | | | | |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SPHASE _x <15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SPHASE _x <7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-0 **SPHASE_x<15:0>**: Secondary Phase Offset for PWM_xL Output Pin bits
(used in Independent PWM mode only)

Note 1: If PWMCON_x<9> = 0, the following applies based on the mode of operation:

- Complementary, Redundant and Push-Pull Output mode (IOCON_x<11:10> = 00, 01 or 10);
SPHASE_x<15:0> = Not used
- True Independent Output mode (IOCON_x<11:10> = 11), SPHASE_x<15:0> = Phase-shift value for PWM_xL only

2: If PWMCON_x<9> = 1, the following applies based on the mode of operation:

- Complementary, Redundant and Push-Pull Output mode (IOCON_x<11:10> = 00, 01 or 10);
SPHASE_x<15:0> = Not used
- True Independent Output mode (IOCON_x<11:10> = 11); SPHASE_x<15:0> = Independent time base period value for PWM_xL only
- When the PHASE_x/SPHASE_x registers provide the local period, the valid range of values is 0x0010-0xFFFF8

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REGISTER 15-17: DTRx: PWMx DEAD-TIME REGISTER

| | | | | | | | |
|--------|-----|------------|-------|-------|-------|-------|-------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | DTRx<13:8> | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DTRx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'
 bit 13-0 **DTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 15-18: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

| | | | | | | | |
|--------|-----|---------------|-------|-------|-------|-------|-------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | ALTDTRx<13:8> | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| ALTDTRx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'
 bit 13-0 **ALTDTRx<13:0>:** Unsigned 14-Bit Alternate Dead-Time Value for PWMx Dead-Time Unit bits

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REGISTER 15-19: TRGCONx: PWMx TRIGGER CONTROL REGISTER

| | | | | | | | |
|---------|---------|---------|---------|-----|-----|-----|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
| TRGDIV3 | TRGDIV2 | TRGDIV1 | TRGDIV0 | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------------------|-----|----------|----------|----------|----------|----------|----------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DTM ⁽¹⁾ | — | TRGSTRT5 | TRGSTRT4 | TRGSTRT3 | TRGSTRT2 | TRGSTRT1 | TRGSTRT0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **TRGDIV<3:0>**: Trigger # Output Divider bits
 1111 = Trigger output for every 16th trigger event
 1110 = Trigger output for every 15th trigger event
 1101 = Trigger output for every 14th trigger event
 1100 = Trigger output for every 13th trigger event
 1011 = Trigger output for every 12th trigger event
 1010 = Trigger output for every 11th trigger event
 1001 = Trigger output for every 10th trigger event
 1000 = Trigger output for every 9th trigger event
 0111 = Trigger output for every 8th trigger event
 0110 = Trigger output for every 7th trigger event
 0101 = Trigger output for every 6th trigger event
 0100 = Trigger output for every 5th trigger event
 0011 = Trigger output for every 4th trigger event
 0010 = Trigger output for every 3rd trigger event
 0001 = Trigger output for every 2nd trigger event
 0000 = Trigger output for every trigger event

bit 11-8 **Unimplemented**: Read as '0'

bit 7 **DTM**: Dual Trigger Mode bit⁽¹⁾

1 = Secondary trigger event is combined with the primary trigger event to create a PWM trigger
 0 = Secondary trigger event is not combined with the primary trigger event to create a PWM trigger;
 two separate PWM triggers are generated

bit 6 **Unimplemented**: Read as '0'

bit 5-0 **TRGSTRT<5:0>**: Trigger Postscaler Start Enable Select bits

111111 = Wait 63 PWM cycles before generating the first trigger event after the module is enabled
 •
 •
 •
 000010 = Wait 2 PWM cycles before generating the first trigger event after the module is enabled
 000001 = Wait 1 PWM cycle before generating the first trigger event after the module is enabled
 000000 = Wait 0 PWM cycles before generating the first trigger event after the module is enabled

Note 1: The secondary PWMx generator cannot generate PWM trigger interrupts.

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REGISTER 15-20: IOCONx: PWMx I/O CONTROL REGISTER

| | | | | | | | |
|--------|-------|-------|-------|----------------------|----------------------|--------|--------|
| R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PENH | PENL | POLH | POLL | PMOD1 ⁽¹⁾ | PMOD0 ⁽¹⁾ | OVRENH | OVRENL |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|---------|---------|------------------------|------------------------|-----------------------|-----------------------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| OVRDAT1 | OVRDAT0 | FLTDAT1 ⁽²⁾ | FLTDAT0 ⁽²⁾ | CLDAT1 ⁽²⁾ | CLDAT0 ⁽²⁾ | SWAP | OSYNC |
| bit 7 | | | | | | bit 0 | |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 15 **PENH:** PWMxH Output Pin Ownership bit
 1 = PWM module controls the PWMxH pin
 0 = GPIO module controls the PWMxH pin
- bit 14 **PENL:** PWMxL Output Pin Ownership bit
 1 = PWM module controls the PWMxL pin
 0 = GPIO module controls the PWMxL pin
- bit 13 **POLH:** PWMxH Output Pin Polarity bit
 1 = PWMxH pin is active-low
 0 = PWMxH pin is active-high
- bit 12 **POLL:** PWMxL Output Pin Polarity bit
 1 = PWMxL pin is active-low
 0 = PWMxL pin is active-high
- bit 11-10 **PMOD<1:0>:** PWMx I/O Pin Mode bits⁽¹⁾
 11 = PWMx I/O pin pair is in the True Independent Output mode
 10 = PWMx I/O pin pair is in the Push-Pull Output mode
 01 = PWMx I/O pin pair is in the Redundant Output mode
 00 = PWMx I/O pin pair is in the Complementary Output mode
- bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
 1 = OVRDAT1 provides data for output on the PWMxH pin
 0 = PWMx generator provides data for the PWMxH pin
- bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
 1 = OVRDAT0 provides data for output on the PWMxL pin
 0 = PWMx generator provides data for the PWMxL pin
- bit 7-6 **OVRDAT<1:0>:** Data for PWMxH, PWMxL Pins if Override is Enabled bits
 If OVERENH = 1, OVRDAT1 provides the data for the PWMxH pin.
 If OVERENL = 1, OVRDAT0 provides the data for the PWMxL pin.
- bit 5-4 **FLTDAT<1:0>:** State for PWMxH and PWMxL Pins if FLTMOD<1:0> are Enabled bits⁽²⁾
IFLTMOD (FCLCONx<15>) = 0: Normal Fault mode:
 If Fault is active, then FLTDAT1 provides the state for the PWMxH pin.
 If Fault is active, then FLTDAT0 provides the state for the PWMxL pin.
IFLTMOD (FCLCONx<15>) = 1: Independent Fault mode:
 If current-limit is active, then FLTDAT1 provides the state for the PWMxH pin.
 If Fault is active, then FLTDAT0 provides the state for the PWMxL pin.

Note 1: These bits should not be changed after the PWM module is enabled (PTEN = 1).

2: State represents the active/inactive state of the PWMx depending on the POLH and POLL bits settings.

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REGISTER 15-20: IOCONx: PWMx I/O CONTROL REGISTER (CONTINUED)

- bit 3-2 **CLDAT<1:0>**: State for PWMxH and PWMxL Pins if CLMOD is Enabled bits⁽²⁾
IFLTMOD (FCLCONx<15>) = 0: Normal Fault mode:
 If current-limit is active, then CLDAT1 provides the state for the PWMxH pin.
 If current-limit is active, then CLDAT0 provides the state for the PWMxL pin.
IFLTMOD (FCLCONx<15>) = 1: Independent Fault mode:
 CLDAT<1:0> bits are ignored.
- bit 1 **SWAP**: SWAP PWMxH and PWMxL Pins bit
 1 = PWMxH output signal is connected to the PWMxL pins; PWMxL output signal is connected to the PWMxH pins
 0 = PWMxH and PWMxL pins are mapped to their respective pins
- bit 0 **OSYNC**: Output Override Synchronization bit
 1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWMx time base
 0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary

- Note 1:** These bits should not be changed after the PWM module is enabled (PTEN = 1).
Note 2: State represents the active/inactive state of the PWMx depending on the POLH and POLL bits settings.

REGISTER 15-21: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| TRGCMP<12:5> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------------|-------|-------|-------|-------|-----|-----|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| TRGCMP<4:0> | | | | | — | — | — |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15-3 **TRGCMP<12:0>**: Trigger Compare Value bits
 When the primary PWM functions in the local time base, this register contains the compare values that can trigger the ADC module.
- bit 2-0 **Unimplemented**: Read as '0'

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REGISTER 15-22: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER

| | | | | | | | |
|---------|--------|--------|--------|--------|--------|----------------------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| IFLTMOD | CLSRC4 | CLSRC3 | CLSRC2 | CLSRC1 | CLSRC0 | CLPOL ⁽¹⁾ | CLMOD |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|---------|---------|---------|---------|---------|-----------------------|---------|---------|
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
| FLTSRC4 | FLTSRC3 | FLTSRC2 | FLTSRC1 | FLTSRC0 | FLTPOL ⁽¹⁾ | FLTMOD1 | FLTMOD0 |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **IFLTMOD:** Independent Fault Mode Enable bit
 1 = Independent Fault mode: Current-limit input maps FLTDAT1 to the PWMxH output and the Fault input maps FLTDAT0 to the PWMxL output. The CLDAT<1:0> bits are not used for override functions.
 0 = Normal Fault mode: Current-Limit mode maps the CLDAT<1:0> bits to the PWMxH and PWMxL outputs. The PWM Fault mode maps FLTDAT<1:0> to the PWMxH and PWMxL outputs.
- bit 14-10 **CLSRC<4:0>:** Current-Limit Control Signal Source Select for PWMx Generator bits
 11111 = Fault 31
 10001 = Reserved
 10000 = Reserved
 01111 = Reserved
 01110 = Analog Comparator 2
 01101 = Analog Comparator 1
 01100 = Reserved
 01011 = Reserved
 01010 = Reserved
 01001 = Reserved
 01000 = Fault 8
 00111 = Fault 7
 00110 = Fault 6
 00101 = Fault 5
 00100 = Fault 4
 00011 = Fault 3
 00010 = Fault 2
 00001 = Fault 1
 00000 = Reserved
- bit 9 **CLPOL:** Current-Limit Polarity for PWMx Generator # bit⁽¹⁾
 1 = The selected current-limit source is active-low
 0 = The selected current-limit source is active-high
- bit 8 **CLMOD:** Current-Limit Mode Enable for PWMx Generator # bit
 1 = Current-Limit mode is enabled
 0 = Current-Limit mode is disabled

Note 1: These bits should be changed only when PTEN (PTCON<15>) = 0.

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REGISTER 15-22: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER (CONTINUED)

- bit 7-3 **FLTSRC<4:0>**: Fault Control Signal Source Select for PWMx Generator # bits
- 11111 = Fault 31 (Default)
 - 10001 = Reserved
 - 10000 = Reserved
 - 01111 = Reserved
 - 01110 = Analog Comparator 2
 - 01101 = Analog Comparator 1
 - 01100 = Reserved
 - 01011 = Reserved
 - 01010 = Reserved
 - 01001 = Reserved
 - 01000 = Fault 8
 - 00111 = Fault 7
 - 00110 = Fault 6
 - 00101 = Fault 5
 - 00100 = Fault 4
 - 00011 = Fault 3
 - 00010 = Fault 2
 - 00001 = Fault 1
 - 00000 = Reserved
- bit 2 **FLTPOL**: Fault Polarity for PWMx Generator # bit⁽¹⁾
- 1 = The selected Fault source is active-low
 - 0 = The selected Fault source is active-high
- bit 1-0 **FLTMOD<1:0>**: Fault Mode for PWMx Generator # bits
- 11 = Fault input is disabled
 - 10 = Reserved
 - 01 = The selected Fault source forces the PWMxH, PWMxL pins to the FLTDATx values (cycle)
 - 00 = The selected Fault source forces the PWMxH, PWMxL pins to the FLTDATx values (latched condition)

Note 1: These bits should be changed only when PTEN (PTCON<15>) = 0.

REGISTER 15-23: STRIGx: PWMx SECONDARY TRIGGER COMPARE VALUE REGISTER⁽¹⁾

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| STRGCMP<12:5> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------------|-------|-------|-------|-------|-----|-----|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| STRGCMP<4:0> | | | | | — | — | — |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15-3 **STRGCMP<12:0>**: Secondary Trigger Compare Value bits
- When the secondary PWMx functions in the local time base, this register contains the compare values that can trigger the ADC module.

bit 2-0 **Unimplemented:** Read as '0'

Note 1: STRIGx cannot generate the PWMx trigger interrupts.

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REGISTER 15-24: LEBCONx: PWMx LEADING-EDGE BLANKING (LEB) CONTROL REGISTER

| | | | | | | | |
|--------|-------|--------------------|--------------------|----------|---------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — |
| bit 15 | | | | | | bit 8 | |
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | BCH ⁽¹⁾ | BCL ⁽¹⁾ | BPHH | BPHL | BPLH | BPLL |
| bit 7 | | | | | | bit 0 | |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
 1 = Rising edge of PWMxH will trigger the Leading-Edge Blanking counter
 0 = Leading-Edge Blanking ignores the rising edge of PWMxH
- bit 14 **PHF:** PWMxH Falling Edge Trigger Enable bit
 1 = Falling edge of PWMxH will trigger the Leading-Edge Blanking counter
 0 = Leading-Edge Blanking ignores the falling edge of PWMxH
- bit 13 **PLR:** PWMxL Rising Edge Trigger Enable bit
 1 = Rising edge of PWMxL will trigger the Leading-Edge Blanking counter
 0 = Leading-Edge Blanking ignores the rising edge of PWMxL
- bit 12 **PLF:** PWMxL Falling Edge Trigger Enable bit
 1 = Falling edge of PWMxL will trigger the Leading-Edge Blanking counter
 0 = Leading-Edge Blanking ignores the falling edge of PWMxL
- bit 11 **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit
 1 = Leading-Edge Blanking is applied to the selected Fault input
 0 = Leading-Edge Blanking is not applied to the selected Fault input
- bit 10 **CLLEBEN:** Current-Limit Leading-Edge Blanking Enable bit
 1 = Leading-Edge Blanking is applied to the selected current-limit input
 0 = Leading-Edge Blanking is not applied to the selected current-limit input
- bit 9-6 **Unimplemented:** Read as '0'
- bit 5 **BCH:** Blanking in Selected Blanking Signal High Enable bit⁽¹⁾
 1 = State blanking (of current-limit and/or Fault input signals) when the selected blanking signal is high
 0 = No blanking when the selected blanking signal is high
- bit 4 **BCL:** Blanking in Selected Blanking Signal Low Enable bit⁽¹⁾
 1 = State blanking (of current-limit and/or Fault input signals) when the selected blanking signal is low
 0 = No blanking when the selected blanking signal is low
- bit 3 **BPHH:** Blanking in PWMxH High Enable bit
 1 = State blanking (of current-limit and/or Fault input signals) when the PWMxH output is high
 0 = No blanking when the PWMxH output is high
- bit 2 **BPHL:** Blanking in PWMxH Low Enable bit
 1 = State blanking (of current-limit and/or Fault input signals) when the PWMxH output is low
 0 = No blanking when the PWMxH output is low

Note 1: The blanking signal is selected via the BLANKSEL<3:0> bits in the AUXCONx register.

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REGISTER 15-24: LEBCONx: PWMx LEADING-EDGE BLANKING (LEB) CONTROL REGISTER (CONTINUED)

- bit 1 **BPLH:** Blanking in PWMxL High Enable bit
 1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is high
 0 = No blanking when the PWMxL output is high
- bit 0 **BPLL:** Blanking in PWMxL Low Enable bit
 1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is low
 0 = No blanking when the PWMxL output is low

Note 1: The blanking signal is selected via the BLANKSEL<3:0> bits in the AUXCONx register.

REGISTER 15-25: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER

| | | | | | | | |
|--------|-----|-----|-----|----------|-------|-------|-------|
| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | LEB<8:5> | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|----------|-------|-------|-------|-------|-------|-----|-----|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| LEB<4:0> | | | | | — | — | — |
| bit 7 | | | | | bit 0 | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15-12 **Unimplemented:** Read as '0'
- bit 11-3 **LEB<8:0>:** Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits
 The value is in 8.32 ns increments.
- bit 2-0 **Unimplemented:** Read as '0'

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REGISTER 15-26: AUXCONx: PWMx AUXILIARY CONTROL REGISTER

| | | | | | | | |
|--------|--------|-----|-----|-----------|-----------|-----------|-----------|
| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| HRPDIS | HRDDIS | — | — | BLANKSEL3 | BLANKSEL2 | BLANKSEL1 | BLANKSEL0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|----------|----------|----------|----------|---------|---------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSEL0 | CHOPHEN | CHOPLEN |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **HRPDIS:** High-Resolution PWMx Period Disable bit
 1 = High-resolution PWMx period is disabled to reduce power consumption
 0 = High-resolution PWMx period is enabled
- bit 14 **HRDDIS:** High-Resolution PWMx Duty Cycle Disable bit
 1 = High-resolution PWMx duty cycle is disabled to reduce power consumption
 0 = High-resolution PWMx duty cycle is enabled
- bit 13-12 **Unimplemented:** Read as '0'
- bit 11-8 **BLANKSEL<3:0>:** PWMx State Blank Source Select bits
 The selected state blank signal will block the current-limit and/or Fault input signals (if enabled via the BCH and BCL bits in the LEBCONx register).
 1001 = Reserved
 1000 = Reserved
 0111 = Reserved
 0110 = Reserved
 0101 = Reserved
 0100 = Reserved
 0011 = PWM3H is selected as the state blank source
 0010 = PWM2H is selected as the state blank source
 0001 = PWM1H is selected as the state blank source
 0000 = No state blanking
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-2 **CHOPSEL<3:0>:** PWMx Chop Clock Source Select bits
 The selected signal will enable and disable (chop) the selected PWMx outputs.
 1001 = Reserved
 1000 = Reserved
 0111 = Reserved
 0110 = Reserved
 0101 = Reserved
 0100 = Reserved
 0011 = PWM3H is selected as the chop clock source
 0010 = PWM2H is selected as the chop clock source
 0001 = PWM1H is selected as the chop clock source
 0000 = Chop clock generator is selected as the chop clock source
- bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit
 1 = PWMxH chopping function is enabled
 0 = PWMxH chopping function is disabled
- bit 0 **CHOPLEN:** PWMxL Output Chopping Enable bit
 1 = PWMxL chopping function is enabled
 0 = PWMxL chopping function is disabled

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REGISTER 15-27: PWMCAPx: PWMx PRIMARY TIME BASE CAPTURE REGISTER

| | | | | | | | |
|-----------------------------------|-----|-----|-----|-----|-----|-----|-------|
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| PWMCAP<12:5> ^(1,2,3,4) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|----------------------------------|-----|-----|-----|-----|-----|-----|-------|
| R-0 | R-0 | R-0 | R-0 | R-0 | U-0 | U-0 | U-0 |
| PWMCAP<4:0> ^(1,2,3,4) | | | | | — | — | — |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-3 **PWMCAP<12:0>**: Captured PWMx Time Base Value bits^(1,2,3,4)
 The value in this register represents the captured PWMx time base value when a leading edge is detected on the current-limit input.

bit 2-0 **Unimplemented**: Read as '0'

- Note 1:** The capture feature is only available on a primary output (PWMxH).
Note 2: This feature is active only after LEB processing on the current-limit input signal is complete.
Note 3: The minimum capture resolution is 8.32 ns.
Note 4: This feature can be used when the XPRES bit (PWMCONx<1>) is set to '0'.

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16.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Serial Peripheral Interface (SPI)**” (DS70005185) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 device family offers one SPI module on a single device.

The SPI1 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration.

The SPI1 serial interface consists of four pins, as follows:

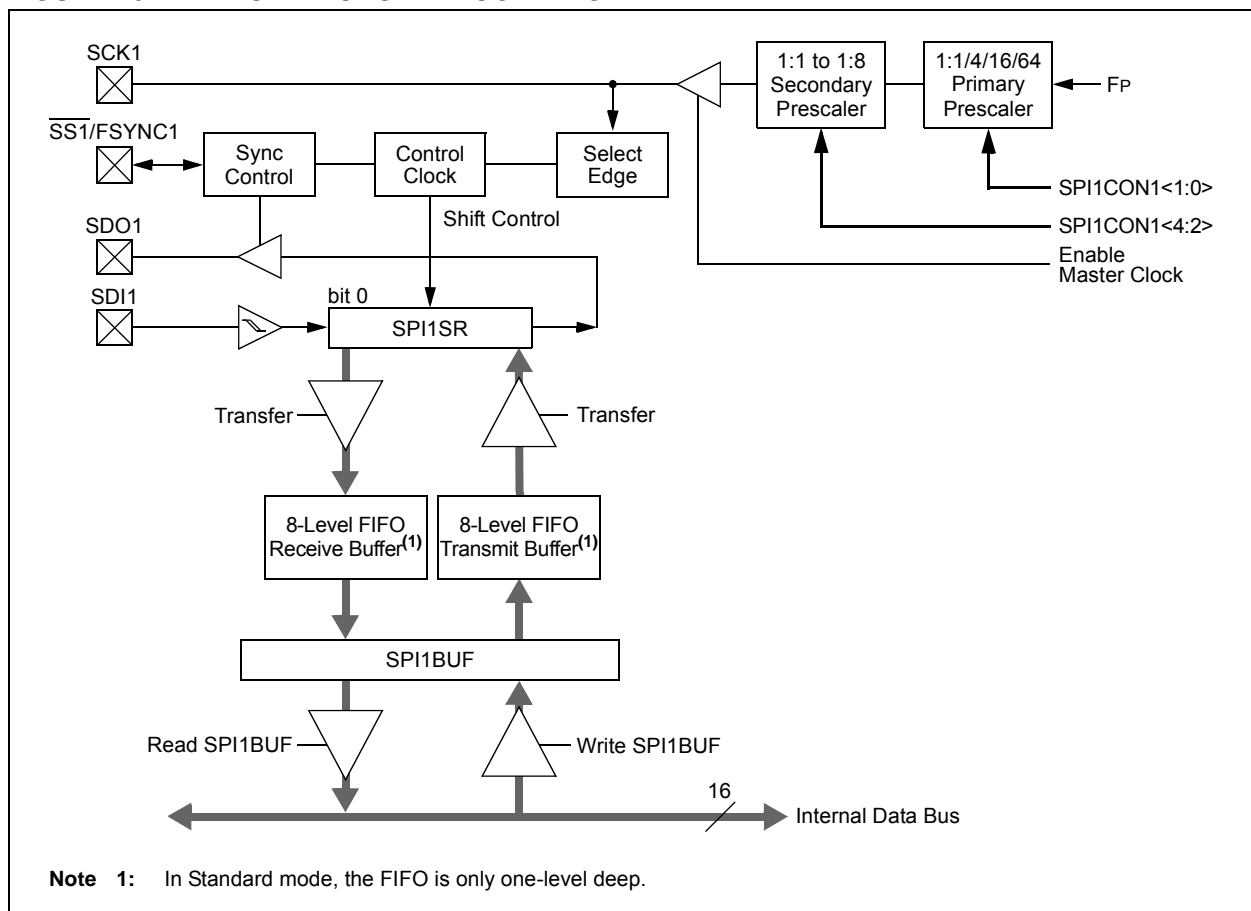
- SDI1: Serial Data Input
- SDO1: Serial Data Output
- SCK1: Shift Clock Input or Output
- $\overline{SS1}$ /FSYNC1: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPI1 module can be configured to operate with two, three or four pins. In 3-Pin mode, $\overline{SS1}$ is not used. In 2-Pin mode, neither SDO1 nor $\overline{SS1}$ is used.

Figure 16-1 illustrates the block diagram of the SPI1 module in Standard and Enhanced modes.

The SPI module is a synchronous serial interface, useful for communicating with other peripherals or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with Motorola® SPI and SIOP interfaces.

FIGURE 16-1: SPI1 MODULE BLOCK DIAGRAM



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16.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
 - a) If FRMPOL (SPI1CON2<13>) = 1, use a pull-down resistor on $\overline{SS1}$.
 - b) If FRMPOL = 0, use a pull-up resistor on $\overline{SS1}$.

Note: This ensures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode (i.e., not using $\overline{SS1}$ from a master):
 - a) If CKP (SPI1CON1<6>) = 1, always place a pull-up resistor on $\overline{SS1}$.
 - b) If CKP = 0, always place a pull-down resistor on $\overline{SS1}$.

Note: This will ensure that during power-up and initialization, the master/slave will not lose synchronization due to an errant SCK1 transition that would cause the slave to accumulate data shift errors for both transmit and receive, appearing as corrupted data.

3. FRMEN (SPI1CON2<15>) = 1 and SSEN (SPI1CON1<7>) = 1 are exclusive and invalid. In Frame mode, SCK1 is continuous and the frame sync pulse is active on the $\overline{SS1}$ pin, which indicates the start of a data frame.

Note: Not all third-party devices support Frame mode timing. Refer to the SPI1 specifications in [Section 25.0 “Electrical Characteristics”](#) for details.

4. In Master mode only, set the SMP bit (SPI1CON1<9>) to a '1' for the fastest SPI1 data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPI1CON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPI1BUF Transmit register in advance of the next master transaction cycle. SPI1BUF is transferred to the SPI1 Shift register and is empty once the data transmission begins.

16.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

16.2.1 KEY RESOURCES

- **“Serial Peripheral Interface (SPI)”** (DS70005185) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

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16.3 SPI Control and Status Registers

REGISTER 16-1: SPI1STAT: SPI1 STATUS AND CONTROL REGISTER

| | | | | | | | |
|--------|-----|---------|-----|-----|---------|---------|---------|
| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| SPIEN | — | SPISIDL | — | — | SPIBEC2 | SPIBEC1 | SPIBEC0 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-----------|--------|--------|--------|--------|-------------|-------------|
| R/W-0 | R/C-0, HS | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0, HS, HC | R-0, HS, HC |
| SRMPT | SPIROV | SRXMPT | SISEL2 | SISEL1 | SISEL0 | SPITBF | SPIRBF |
| bit 7 | | | | | | bit 0 | |

| | | | |
|-------------------|-------------------|------------------------------------|-----------------------------|
| Legend: | C = Clearable bit | HS = Hardware Settable bit | HC = Hardware Clearable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

- bit 15 **SPIEN:** SPI1 Enable bit
1 = Enables the module and configures SCK1, SDO1, SDI1 and $\overline{SS1}$ as serial port pins
0 = Disables the module
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SPISIDL:** SPI1 Stop in Idle Mode bit
1 = Discontinues the module operation when device enters Idle mode
0 = Continues the module operation in Idle mode
- bit 12-11 **Unimplemented:** Read as '0'
- bit 10-8 **SPIBEC<2:0>:** SPI1 Buffer Element Count bits (valid in Enhanced Buffer mode)
Master mode:
Number of SPI1 transfers that are pending.
Slave mode:
Number of SPI1 transfers that are unread.
- bit 7 **SRMPT:** SPI1 Shift Register (SPI1SR) Empty bit (valid in Enhanced Buffer mode)
1 = SPI1 Shift register is empty and ready to send or receive the data
0 = SPI1 Shift register is not empty
- bit 6 **SPIROV:** SPI1 Receive Overflow Flag bit
1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPI1BUF register
0 = No overflow has occurred
- bit 5 **SRXMPT:** SPI1 Receive FIFO Empty bit (valid in Enhanced Buffer mode)
1 = RX FIFO is empty
0 = RX FIFO is not empty
- bit 4-2 **SISEL<2:0>:** SPI1 Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)
111 = Interrupt when the SPI1 transmit buffer is full (SPITBF bit is set)
110 = Interrupt when last bit is shifted into SPI1SR, and as a result, the TX FIFO is empty
101 = Interrupt when the last bit is shifted out of SPI1SR and the transmit is complete
100 = Interrupt when one data is shifted into the SPI1SR, and as a result, the TX FIFO has one open memory location
011 = Interrupt when the SPI1 receive buffer is full (SPIRBF bit is set)
010 = Interrupt when the SPI1 receive buffer is 3/4 or more full
001 = Interrupt when data is available in the receive buffer (SRMPT bit is set)
000 = Interrupt when the last data in the receive buffer is read, and as a result, the buffer is empty (SRXMPT bit is set)

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REGISTER 16-1: SPI1STAT: SPI1 STATUS AND CONTROL REGISTER (CONTINUED)

- bit 1 **SPITBF:** SPI1 Transmit Buffer Full Status bit
1 = Transmit has not yet started, SPI1TXB is full
0 = Transmit has started, SPI1TXB is empty
Standard Buffer mode:
Automatically set in hardware when core writes to the SPI1BUF location, loading SPI1TXB. Automatically cleared in hardware when SPI1 module transfers data from SPI1TXB to SPI1SR.
Enhanced Buffer mode:
Automatically set in hardware when the CPU writes to the SPI1BUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.
- bit 0 **SPIRBF:** SPI1 Receive Buffer Full Status bit
1 = Receive is complete, SPI1RXB is full
0 = Receive is incomplete, SPI1RXB is empty
Standard Buffer mode:
Automatically set in hardware when SPI1 transfers data from SPI1SR to SPI1RXB. Automatically cleared in hardware when the core reads the SPI1BUF location, reading SPI1RXB.
Enhanced Buffer mode:
Automatically set in hardware when SPI1 transfers data from SPI1SR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPI1SR.

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REGISTER 16-2: SPI1CON1: SPI CONTROL REGISTER 1

| | | | | | | | |
|--------|-----|-----|--------|--------|--------|-------|--------------------|
| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE ⁽¹⁾ |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|---------------------|-------|-------|----------------------|----------------------|----------------------|----------------------|----------------------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SSEN ⁽²⁾ | CKP | MSTEN | SPRE2 ⁽³⁾ | SPRE1 ⁽³⁾ | SPRE0 ⁽³⁾ | PPRE1 ⁽³⁾ | PPRE0 ⁽³⁾ |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **DISSCK:** Disable SCK1 Pin bit (SPI1 Master modes only)
 1 = Internal SPI1 clock is disabled, pin functions as I/O
 0 = Internal SPI1 clock is enabled
- bit 11 **DISSDO:** Disable SDO1 Pin bit
 1 = SDO1 pin is not used by the module; pin functions as I/O
 0 = SDO1 pin is controlled by the module
- bit 10 **MODE16:** Word/Byte Communication Select bit
 1 = Communication is word-wide (16 bits)
 0 = Communication is byte-wide (8 bits)
- bit 9 **SMP:** SPI1 Data Input Sample Phase bit
 Master mode:
 1 = Input data is sampled at the end of data output time
 0 = Input data is sampled at the middle of data output time
 Slave mode:
 SMP must be cleared when SPI1 is used in Slave mode.
- bit 8 **CKE:** SPI1 Clock Edge Select bit⁽¹⁾
 1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)
 0 = Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)
- bit 7 **SSEN:** Slave Select Enable bit (Slave mode)⁽²⁾
 1 = $\overline{SS1}$ pin is used for Slave mode
 0 = $\overline{SS1}$ pin is not used by the module; pin is controlled by port function
- bit 6 **CKP:** Clock Polarity Select bit
 1 = Idle state for clock is a high level; active state is a low level
 0 = Idle state for clock is a low level; active state is a high level
- bit 5 **MSTEN:** Master Mode Enable bit
 1 = Master mode
 0 = Slave mode

- Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
Note 2: This bit must be cleared when FRMEN = 1.
Note 3: Do not set both primary and secondary prescalers to the value of 1:1.

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REGISTER 16-2: SPI1CON1: SPI1 CONTROL REGISTER 1 (CONTINUED)

bit 4-2 **SPRE<2:0>**: Secondary Prescale bits (Master mode)⁽³⁾

111 = Secondary prescale 1:1

110 = Secondary prescale 2:1

•

•

•

000 = Secondary prescale 8:1

bit 1-0 **PPRE<1:0>**: Primary Prescale bits (Master mode)⁽³⁾

11 = Primary prescale 1:1

10 = Primary prescale 4:1

01 = Primary prescale 16:1

00 = Primary prescale 64:1

Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).

2: This bit must be cleared when FRMEN = 1.

3: Do not set both primary and secondary prescalers to the value of 1:1.

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REGISTER 16-3: SPI1CON2: SPI1 CONTROL REGISTER 2

| | | | | | | | |
|--------|--------|--------|-----|-----|-----|-----|-------|
| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| FRMEN | SPIFSD | FRMPOL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|--------|--------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | — | FRMDLY | SPIBEN |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **FRMEN:** Framed SPI1 Support bit
1 = Framed SPI1 support is enabled ($\overline{SS1}$ pin is used as frame sync pulse input/output)
0 = Framed SPI1 support is disabled
- bit 14 **SPIFSD:** Frame Sync Pulse Direction Control bit
1 = Frame sync pulse input (slave)
0 = Frame sync pulse output (master)
- bit 13 **FRMPOL:** Frame Sync Pulse Polarity bit
1 = Frame sync pulse is active-high
0 = Frame sync pulse is active-low
- bit 12-2 **Unimplemented:** Read as '0'
- bit 1 **FRMDLY:** Frame Sync Pulse Edge Select bit
1 = Frame sync pulse coincides with first bit clock
0 = Frame sync pulse precedes first bit clock
- bit 0 **SPIBEN:** Enhanced Buffer Enable bit
1 = Enhanced buffer is enabled
0 = Enhanced buffer is disabled (Standard mode)

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NOTES:

17.0 INTER-INTEGRATED CIRCUIT (I²C)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Inter-Integrated Circuit™ (I²C)**” (DS70000195) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 family of devices contains one Inter-Integrated Circuit (I²C) module.

The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard, with a 16-bit interface.

The I²C module has a 2-pin interface:

- The SCL1 pin is clock
- The SDA1 pin is data

The I²C module offers the following key features:

- I²C Interface Supporting Both Master and Slave modes of Operation
- I²C Slave mode Supports 7 and 10-Bit Addressing
- I²C Master mode Supports 7 and 10-Bit Addressing
- I²C Port allows Bidirectional Transfers between Master and Slaves
- Serial Clock Synchronization for I²C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control)
- I²C Supports Multi-Master Operation, Detects Bus Collision and Arbitrates Accordingly
- System Management Bus (SMBus) Support

17.1 I²C Resources

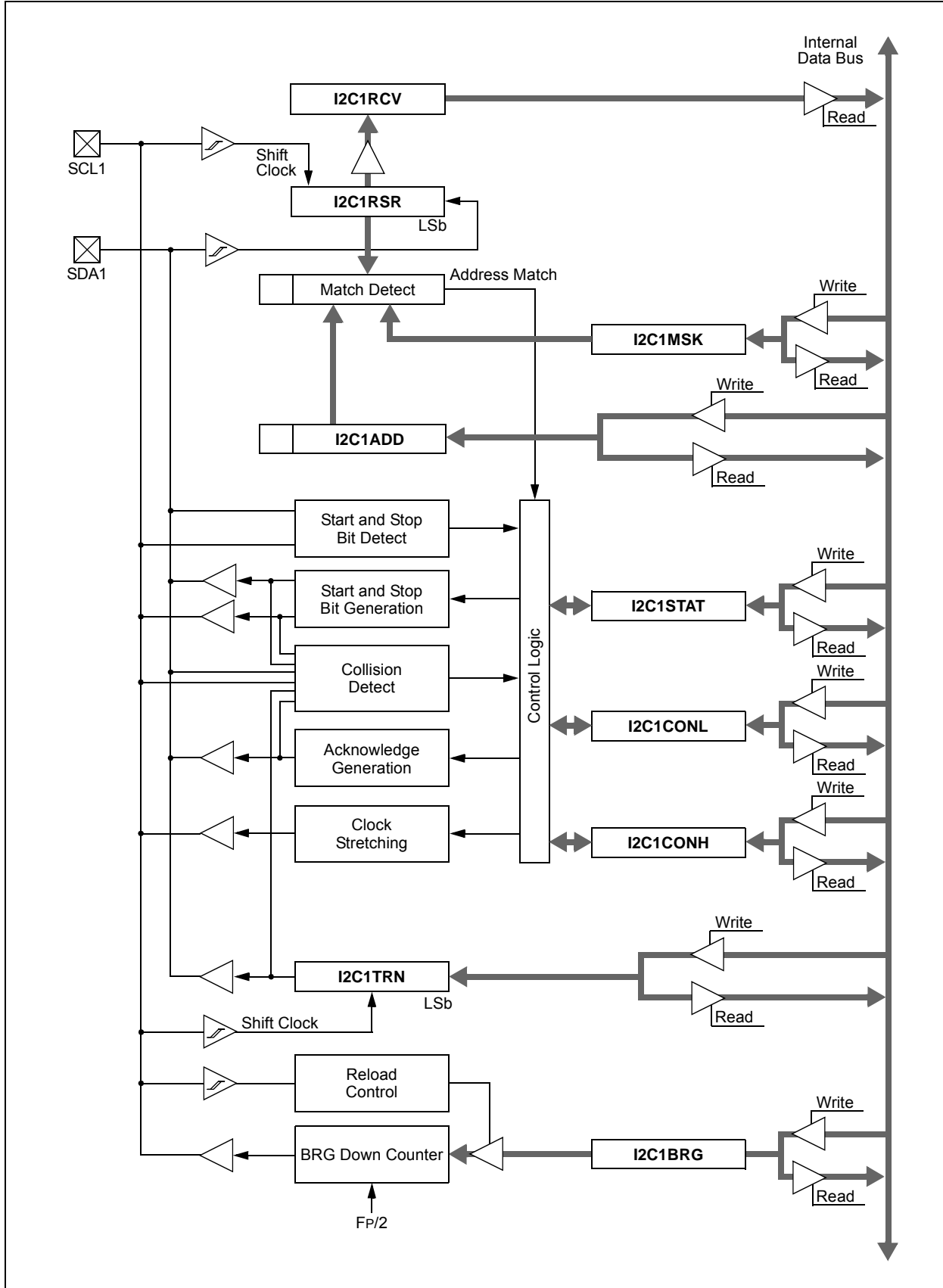
Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

17.1.1 KEY RESOURCES

- “**Inter-Integrated Circuit™ (I²C)**” (DS70000195) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

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FIGURE 17-1: I2C1 BLOCK DIAGRAM



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17.2 I²C Control and Status Registers

REGISTER 17-1: I2C1CONL: I2C1 CONTROL REGISTER LOW

| | | | | | | | |
|--------|-----|---------|-----------|--------|-------|--------|-------|
| R/W-0 | U-0 | R/W-0 | R/W-1, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| I2CEN | — | I2CSIDL | SCLREL | STRICT | A10M | DISSLW | SMEN |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-------|-------|-----------|-----------|-----------|-----------|-----------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0, HC | R/W-0, HC | R/W-0, HC | R/W-0, HC | R/W-0, HC |
| GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN |
| bit 7 | | | | | | bit 0 | |

| | |
|-------------------|------------------------------------|
| Legend: | HC = Hardware Clearable bit |
| R = Readable bit | W = Writable bit |
| -n = Value at POR | '1' = Bit is set |
| | U = Unimplemented bit, read as '0' |
| | '0' = Bit is cleared |
| | x = Bit is unknown |

- bit 15 **I2CEN:** I2C1 Enable bit
1 = Enables the I2C1 module and configures the SDA1 and SCL1 pins as serial port pins
0 = Disables the I2C1 module; all I²C pins are controlled by port functions
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **I2CSIDL:** I2C1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode
- bit 12 **SCLREL:** SCL1 Release Control bit (when operating as I²C slave)
1 = Releases SCL1 clock
0 = Holds SCL1 clock low (clock stretch)
If STREN = 1:
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware is clear at the beginning of every slave data byte transmission. Hardware is clear at the end of every slave address byte reception. Hardware is clear at the end of every slave data byte reception.
If STREN = 0:
Bit is R/S (i.e., software can only write '1' to release clock). Hardware is clear at the beginning of every slave data byte transmission. Hardware is clear at the end of every slave address byte reception.
- bit 11 **STRICT:** Strict I2C1 Reserved Address Enable bit
1 = Strict Reserved Addressing is Enabled:
In Slave mode, the device will NACK any reserved address. In Master mode, the device is allowed to generate addresses within the reserved address space.
0 = Reserved Addressing is Acknowledged:
In Slave mode, the device will ACK any reserved address. In Master mode, the device should not address a slave device with a reserved address.
- bit 10 **A10M:** 10-Bit Slave Address bit
1 = I2C1ADD is a 10-bit slave address
0 = I2C1ADD is a 7-bit slave address
- bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control is disabled
0 = Slew rate control is enabled
- bit 8 **SMEN:** SMBus Input Levels bit
1 = Enables I/O pin thresholds compliant with SMBus specification
0 = Disables SMBus input thresholds
- bit 7 **GCEN:** General Call Enable bit (when operating as I²C slave)
1 = Enables interrupt when a general call address is received in I2C1RSR (module is enabled for reception)
0 = General call address is disabled

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REGISTER 17-1: I2C1CONL: I2C1 CONTROL REGISTER LOW (CONTINUED)

- bit 6 **STREN:** SCL1 Clock Stretch Enable bit (when operating as I²C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching
- bit 5 **ACKDT:** Acknowledge Data bit (when operating as I²C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge
- bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I²C master, applicable during master receive)
1 = Initiates Acknowledge sequence on the SDA1 and SCL1 pins and transmits the ACKDT data bit.
Hardware clears it at the end of the master Acknowledge sequence.
0 = Acknowledge sequence is not in progress
- bit 3 **RCEN:** Receive Enable bit (when operating as I²C master)
1 = Enables Receive mode for I²C. Hardware clears it at the end of the eighth bit of the master receive data byte.
0 = Receive sequence is not in progress
- bit 2 **PEN:** Stop Condition Enable bit (when operating as I²C master)
1 = Initiates Stop condition on the SDA1 and SCL1 pins. Hardware clears it at the end of the master Stop sequence.
0 = Stop condition is not in progress
- bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I²C master)
1 = Initiates Repeated Start condition on the SDA1 and SCL1 pins. Hardware clears it at the end of the master Repeated Start sequence.
0 = Repeated Start condition is not in progress
- bit 0 **SEN:** Start Condition Enable bit (when operating as I²C master)
1 = Initiates Start condition on the SDA1 and SCL1 pins. Hardware clears it at the end of the master Start sequence.
0 = Start condition is not in progress

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REGISTER 17-2: I2C1CONH: I2C1 CONTROL REGISTER HIGH

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | PCIE | SCIE | BOEN | SDAHT | SBCDE | AHEN | DHEN |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I²C Slave mode only)

1 = Enables interrupt on detection of Stop condition

0 = Stop detection interrupts are disabled

bit 5 **SCIE:** Start Condition Interrupt Enable bit (I²C Slave mode only)

1 = Enables interrupt on detection of Start or Restart conditions

0 = Start detection interrupts are disabled

bit 4 **BOEN:** Buffer Overwrite Enable bit (I²C Slave mode only)

1 = I2C1RCV is updated and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if the RBF bit = 0

0 = I2C1RCV is only updated when I2COV is clear

bit 3 **SDAHT:** SDA1 Hold Time Selection bit

1 = Minimum of 300 ns hold time on SDA1 after the falling edge of SCL1

0 = Minimum of 100 ns hold time on SDA1 after the falling edge of SCL1

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I²C Slave mode only)

1 = Enables slave bus collision interrupts

0 = Slave bus collision interrupts are disabled

If the rising edge of SCL1 and SDA1 is sampled low when the module is in a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.

bit 1 **AHEN:** Address Hold Enable bit (I²C Slave mode only)

1 = Following the 8th falling edge of SCL1 for a matching received address byte, the SCLREL (I2C1CONL<12>) bit will be cleared and SCL1 will be held low

0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I²C Slave mode only)

1 = Following the 8th falling edge of SCL1 for a received data byte, the slave hardware clears the SCLREL (I2C1CONL<12>) bit and SCL1 is held low

0 = Data holding is disabled

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REGISTER 17-3: I2C1STAT: I2C1 STATUS REGISTER

| | | | | | | | |
|----------|----------|----------|-----|-----|-----------|----------|----------|
| R-0, HSC | R-0, HSC | R-0, HSC | U-0 | U-0 | R/C-0, HS | R-0, HSC | R-0, HSC |
| ACKSTAT | TRSTAT | ACKTIM | — | — | BCL | GCSTAT | ADD10 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-----------|-----------|----------|------------|------------|----------|----------|----------|
| R/C-0, HS | R/C-0, HS | R-0, HSC | R/C-0, HSC | R/C-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
| IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF |
| bit 7 | | | | | | bit 0 | |

| | | | |
|-------------------|-------------------|------------------------------------|---------------------------------------|
| Legend: | C = Clearable bit | HS = Hardware Settable bit | HSC = Hardware Settable/Clearable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

- bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I²C master, applicable to master transmit operation)
 1 = NACK was received from slave
 0 = ACK was received from slave
 It is set or cleared by the hardware at the end of a slave Acknowledge.
- bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
 1 = Master transmit is in progress (8 bits + ACK)
 0 = Master transmit is not in progress
 It is set by the hardware at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
- bit 13 **ACKTIM:** Acknowledge Time Status bit (I²C Slave mode only)
 1 = I²C bus is an Acknowledge sequence, set on the 8th falling edge of SCL1
 0 = Not an Acknowledge sequence, cleared on the 9th rising edge of SCL1
- bit 12-11 **Unimplemented:** Read as '0'
- bit 10 **BCL:** Master Bus Collision Detect bit
 1 = A bus collision has been detected during a master operation
 0 = No bus collision detected
 It is set by the hardware at detection of a bus collision.
- bit 9 **GCSTAT:** General Call Status bit
 1 = General call address was received
 0 = General call address was not received
 It is set by the hardware when the address matches the general call address. Hardware is clear at Stop detection.
- bit 8 **ADD10:** 10-Bit Address Status bit
 1 = 10-bit address was matched
 0 = 10-bit address was not matched
 Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
- bit 7 **IWCOL:** I2C1 Write Collision Detect bit
 1 = An attempt to write to the I2C1TRN register failed because the I²C module is busy
 0 = No collision
 Hardware is set at the occurrence of a write to I2C1TRN while busy (cleared by software).
- bit 6 **I2COV:** I2C1 Receive Overflow Flag bit
 1 = A byte was received while the I2C1RCV register was still holding the previous byte
 0 = No overflow
 It is set by the hardware at an attempt to transfer I2C1RSR to I2C1RCV (cleared by software).
- bit 5 **D_A:** Data/Address bit (I²C Slave mode only)
 1 = Indicates that the last byte received was data
 0 = Indicates that the last byte received was a device address
 It is cleared by the hardware at a device address match. Hardware is set by reception of a slave byte.

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REGISTER 17-3: I2C1STAT: I2C1 STATUS REGISTER (CONTINUED)

- bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.
- bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.
- bit 2 **R_W:** Read/Write Information bit (I²C Slave mode only)
1 = Read – Indicates data transfer is output from the slave
0 = Write – Indicates data transfer is input to the slave
Hardware is set or clear after reception of an I²C device address byte.
- bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive is complete, I2C1RCV is full
0 = Receive is not complete, I2C1RCV is empty
Hardware is set when I2C1RCV is written with a received byte. Hardware is clear when software reads I2C1RCV.
- bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit is in progress, I2C1TRN is full
0 = Transmit is complete, I2C1TRN is empty
Hardware is set when software writes to I2C1TRN. Hardware is clear at completion of a data transmission.

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REGISTER 17-4: I2C1MSK: I2C1 SLAVE MODE ADDRESS MASK REGISTER

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----------|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | — | AMSK<9:8> | |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| AMSK<7:0> | | | | | | | |
| bit 7 | | | | | | bit 0 | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **AMSK<9:0>:** Address Mask Select bits

For 10-Bit Address:

- 1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position
- 0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2C1MSK<6:0> only):

- 1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position
- 0 = Disables masking for bit Ax + 1; bit match is required in this position

18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Universal Asynchronous Receiver Transmitter (UART)**” (DS70000582) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 family of devices contains one UART module.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXGS202 device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{U1CTS}$ and $\overline{U1RTS}$ pins, and also includes an IrDA® encoder and decoder.

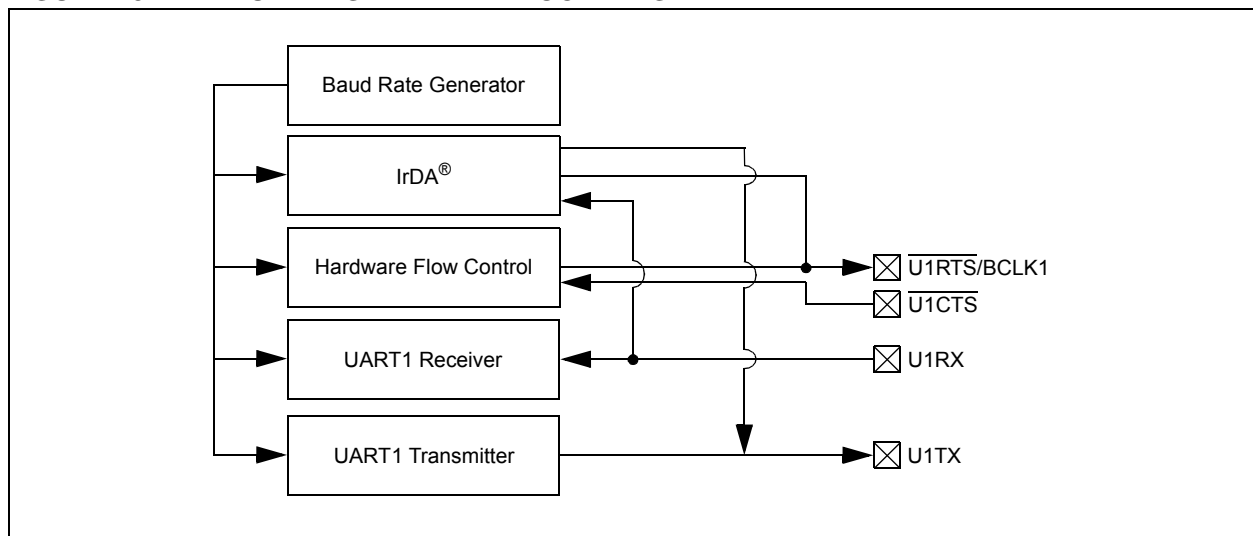
The primary features of the UART1 module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the U1TX and U1RX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with $\overline{U1CTS}$ and $\overline{U1RTS}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps in 16x mode at 60 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps in 4x mode at 60 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for all UART1 Error Conditions
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UART1 module is shown in **Figure 18-1**. The UART1 module consists of these key hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

FIGURE 18-1: UART1 SIMPLIFIED BLOCK DIAGRAM



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18.1 UART Helpful Tips

1. In multi-node, direct connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (U1MODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
 - a) If UR1INV = 0, use a pull-up resistor on the UxRX pin.
 - b) If UR1INV = 1, use a pull-down resistor on the UxRX pin.
2. The first character received on a wake-up from Sleep mode, caused by activity on the U1RX pin of the UART1 module, will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming U1RX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

18.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

18.2.1 KEY RESOURCES

- **“Universal Asynchronous Receiver Transmitter (UART)”** (DS70000582) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

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18.3 UART Control and Status Registers

REGISTER 18-1: U1MODE: UART1 MODE REGISTER

| | | | | | | | |
|-----------------------|-----|-------|---------------------|-------|-----|-------|-------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| UARTEN ⁽¹⁾ | — | USIDL | IREN ⁽²⁾ | RTSMD | — | UEN1 | UEN0 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-----------|--------|-----------|--------|-------|--------|--------|-------|
| R/W-0, HC | R/W-0 | R/W-0, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL1 | PDSEL0 | STSEL |
| bit 7 | | | | | | bit 0 | |

| | |
|-------------------|------------------------------------|
| Legend: | HC = Hardware Clearable bit |
| R = Readable bit | W = Writable bit |
| -n = Value at POR | '1' = Bit is set |
| | U = Unimplemented bit, read as '0' |
| | '0' = Bit is cleared |
| | x = Bit is unknown |

- bit 15 **UARTEN:** UART1 Enable bit⁽¹⁾
 1 = UART1 is enabled; all UART1 pins are controlled by UART1, as defined by UEN<1:0>
 0 = UART1 is disabled; all UART1 pins are controlled by PORT latches; UART1 power consumption is minimal
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **USIDL:** UART1 Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **IREN:** IrDA[®] Encoder and Decoder Enable bit⁽²⁾
 1 = IrDA encoder and decoder are enabled
 0 = IrDA encoder and decoder are disabled
- bit 11 **RTSMD:** Mode Selection for $\overline{U1RTS}$ Pin bit
 1 = $\overline{U1RTS}$ pin is in Simplex mode
 0 = $\overline{U1RTS}$ pin is in Flow Control mode
- bit 10 **Unimplemented:** Read as '0'
- bit 9-8 **UEN<1:0>:** UART1 Pin Enable bits
 11 = U1TX, U1RX and BCLK1 pins are enabled and used; $\overline{U1CTS}$ pin is controlled by PORT latches
 10 = U1TX, U1RX, $\overline{U1CTS}$ and $\overline{U1RTS}$ pins are enabled and used
 01 = U1TX, U1RX and $\overline{U1RTS}$ pins are enabled and used; $\overline{U1CTS}$ pin is controlled by PORT latches
 00 = U1TX and U1RX pins are enabled and used; $\overline{U1CTS}$ and $\overline{U1RTS}/BCLK1$ pins are controlled by PORT latches
- bit 7 **WAKE:** Wake-up on Start bit Detect During Sleep Mode Enable bit
 1 = UART1 continues to sample the U1RX pin, interrupt is generated on the falling edge; bit is cleared in hardware on the following rising edge
 0 = No wake-up is enabled
- bit 6 **LPBACK:** UART1 Loopback Mode Select bit
 1 = Enables Loopback mode
 0 = Loopback mode is disabled
- bit 5 **ABAUD:** Auto-Baud Enable bit
 1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion
 0 = Baud rate measurement is disabled or completed

- Note 1:** Refer to “**Universal Asynchronous Receiver Transmitter (UART)**” (DS70000582) in the “*dsPIC33/PIC24 Family Reference Manual*” for information on enabling the UART1 module for receive or transmit operation.
- 2:** This feature is only available for the 16x BRG mode (BRGH = 0).

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REGISTER 18-1: U1MODE: UART1 MODE REGISTER (CONTINUED)

- bit 4 **URXINV:** UART1 Receive Polarity Inversion bit
1 = U1RX Idle state is '0'
0 = U1RX Idle state is '1'
- bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
- bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity
- bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

- Note 1:** Refer to “**Universal Asynchronous Receiver Transmitter (UART)**” (DS70000582) in the “*dsPIC33/PIC24 Family Reference Manual*” for information on enabling the UART1 module for receive or transmit operation.
- 2:** This feature is only available for the 16x BRG mode (BRGH = 0).

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REGISTER 18-2: U1STA: UART1 STATUS AND CONTROL REGISTER

| | | | | | | | |
|----------|--------|----------|-----|-----------|----------------------|-------|------|
| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0, HC | R/W-0 | R-0 | R-1 |
| UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN ⁽¹⁾ | UTXBF | TRMT |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|----------|----------|-------|------|------|------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R-1 | R-0 | R-0 | R/C-0 | R-0 |
| URXISEL1 | URXISEL0 | ADDEN | RIDL | PERR | FERR | OERR | URXDA |
| bit 7 | | | | | | bit 0 | |

| | | |
|-------------------|-------------------|--|
| Legend: | C = Clearable bit | HC = Hardware Clearable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15,13 **UTXISEL<1:0>**: UART1 Transmission Interrupt Mode Selection bits
 11 = Reserved; do not use
 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 **UTXINV**: UART1 Transmit Polarity Inversion bit
 If IREN = 0:
 1 = U1TX Idle state is '0'
 0 = U1TX Idle state is '1'
 If IREN = 1:
 1 = IrDA[®] encoded, U1TX Idle state is '1'
 0 = IrDA encoded, U1TX Idle state is '0'
- bit 12 **Unimplemented**: Read as '0'
- bit 11 **UTXBRK**: UART1 Transmit Break bit
 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 0 = Sync Break transmission is disabled or completed
- bit 10 **UTXEN**: UART1 Transmit Enable bit⁽¹⁾
 1 = Transmit is enabled, U1TX pin is controlled by UART1
 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; U1TX pin is controlled by the PORT
- bit 9 **UTXBF**: UART1 Transmit Buffer Full Status bit (read-only)
 1 = Transmit buffer is full
 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT**: Transmit Shift Register Empty bit (read-only)
 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 **URXISEL<1:0>**: UART1 Receive Interrupt Mode Selection bits
 11 = Interrupt is set on U1RSR transfer, making the receive buffer full (i.e., has four data characters)
 10 = Interrupt is set on U1RSR transfer, making the receive buffer 3/4 full (i.e., has three data characters)
 0x = Interrupt is set when any character is received and transferred from the U1RSR to the receive buffer; receive buffer has one or more characters

Note 1: Refer to “**Universal Asynchronous Receiver Transmitter (UART)**” (DS70000582) in the “*dsPIC33/PIC24 Family Reference Manual*” for information on enabling the UART1 module for transmit operation.

dsPIC33EPXXGS202 FAMILY

REGISTER 18-2: U1STA: UART1 STATUS AND CONTROL REGISTER (CONTINUED)

- bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled
- bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active
- bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected
- bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected
- bit 1 **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receiver buffer and the U1RSR to the empty state
- bit 0 **URXDA:** UART1 Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

Note 1: Refer to “**Universal Asynchronous Receiver Transmitter (UART)**” (DS70000582) in the “*dsPIC33/PIC24 Family Reference Manual*” for information on enabling the UART1 module for transmit operation.

19.0 HIGH-SPEED, 12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**12-Bit High-Speed, Multiple SARs A/D Converter (ADC)**” (DS70005213) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 devices have a high-speed, 12-bit Analog-to-Digital Converter (ADC) that features a low conversion latency, high resolution and oversampling capabilities to improve performance in AC/DC, DC/DC power converters.

19.1 Features Overview

The 12-Bit High Speed Multiple SARs Analog-to-Digital Converter (ADC) includes the following features:

- 12-Bit Resolution
- Up to 3.25 Msps Conversion Rate per ADC Core @ 12-Bit Resolution
- Two Dedicated ADC Cores
- One Shared (common) ADC Core
- Up to Fifteen Analog Inputs (external and internal)
- Conversion Result can be Formatted as Unsigned or Signed Data on a per Channel Basis for All Channels
- Separate 16-Bit Conversion Result Register for each Analog Input
- Simultaneous Sampling of up to Three Analog Inputs

- Flexible Trigger Options
- Early Interrupt Generation to Enable Fast Processing of Converted Data
- Two Integrated Digital Comparators:
 - Multiple comparison options
 - Assignable to specific analog inputs
- Oversampling Filters:
 - Provides increased resolution
 - Assignable to a specific analog input
- Operation During CPU Sleep and Idle modes

Simplified block diagrams of the Multiple SARs 12-Bit ADC are shown in [Figure 19-1](#), [Figure 19-2](#) and [Figure 19-3](#).

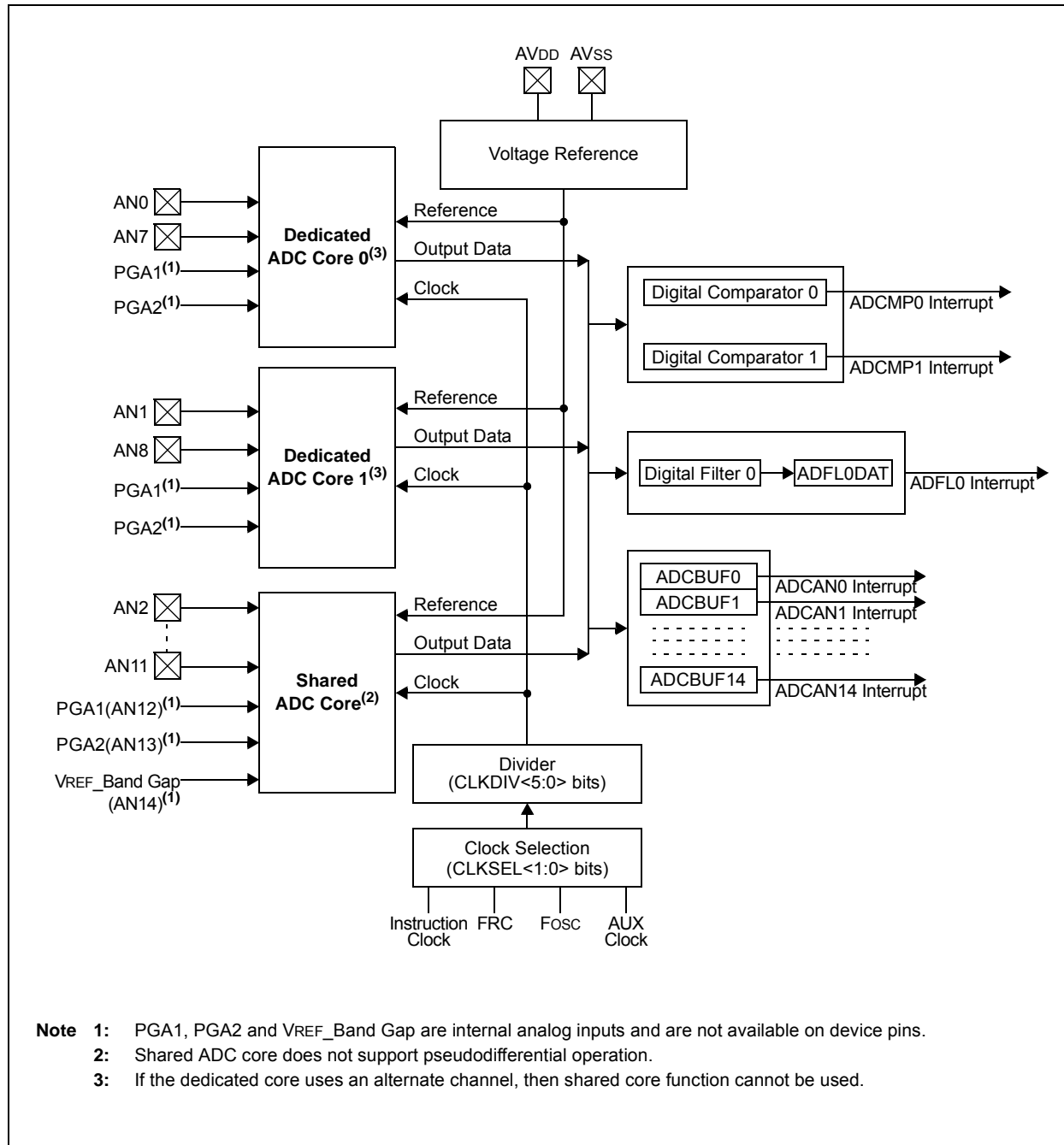
The module consists of two independent SAR ADC cores. The analog inputs (channels) are connected through multiplexers and switches to the Sample-and-Hold (S/H) circuit of each ADC core. The core uses the channel information (the output format, the measurement mode and the input number) to process the analog sample. When conversion is complete, the result is stored in the result buffer for the specific analog input and passed to the digital filter and digital comparator if they were configured to use data from this particular channel.

The ADC module can sample up to three inputs at a time (two inputs from the dedicated SAR ADC cores and one from the shared SAR ADC cores). If multiple ADC inputs request conversion, the ADC module will convert them in a sequential manner, starting with the lowest order input.

The ADC provides each analog input the ability to specify its own trigger source. This capability allows the ADC to sample and convert analog inputs that are associated with PWM generators operating on independent time bases.

dsPIC33EPXXGS202 FAMILY

FIGURE 19-1: ADC MODULE BLOCK DIAGRAM



dsPIC33EPXGS202 FAMILY

FIGURE 19-2: DEDICATED ADC CORE 0-1 BLOCK DIAGRAM

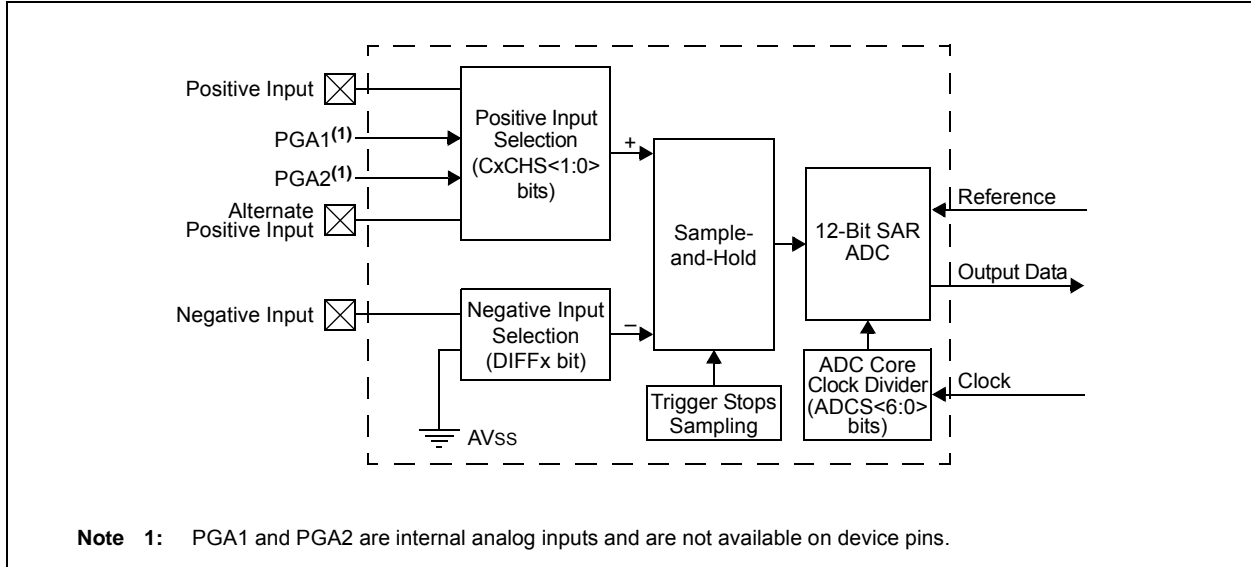
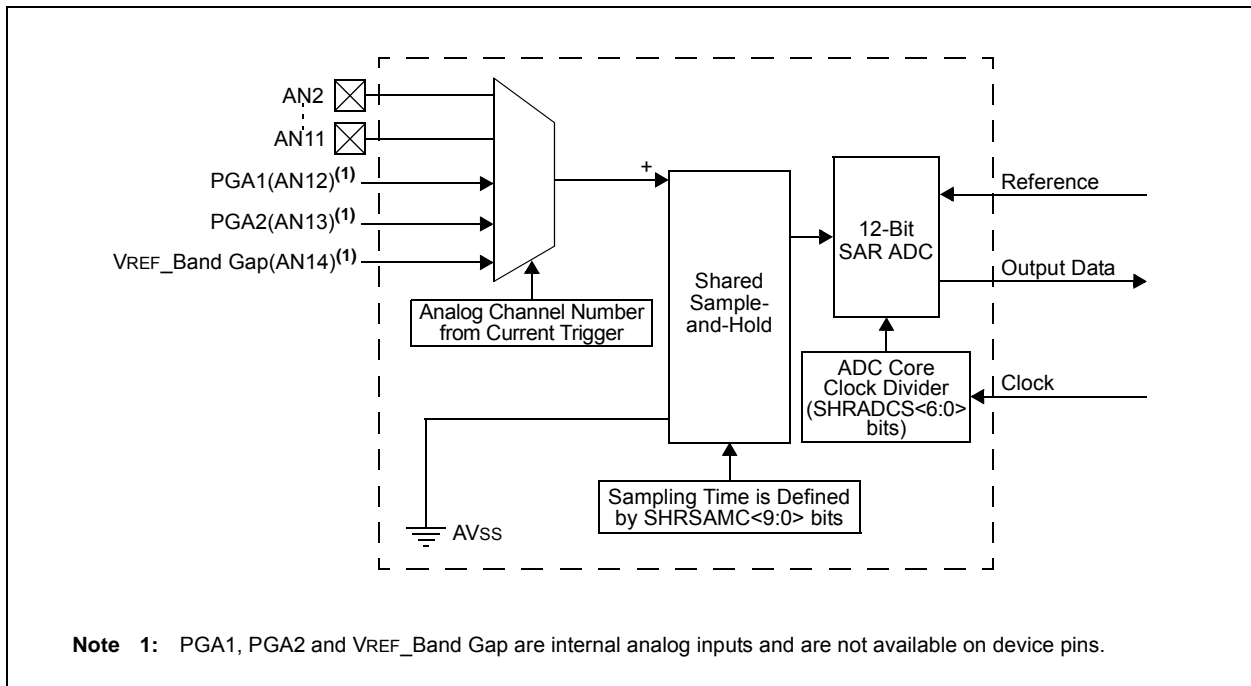


FIGURE 19-3: SHARED ADC CORE BLOCK DIAGRAM



dsPIC33EPXXGS202 FAMILY

19.2 Analog-to-Digital Converter Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

19.2.1 KEY RESOURCES

- “12-Bit High-Speed, Multiple SARs A/D Converter (ADC)” (DS70005213) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

19.3 Analog-to-Digital Converter Control and Status Registers

REGISTER 19-1: ADCON1L: ADC CONTROL REGISTER 1 LOW

| | | | | | | | |
|---------------------|-----|--------|-----|-----|-----|-----|-------|
| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| ADON ⁽¹⁾ | — | ADSIDL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------------------|-----|-----|-----|-----|-----|-----|-------|
| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| NRE ⁽²⁾ | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| | | | |
|-------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

- bit 15 **ADON:** ADC Enable bit⁽¹⁾
 1 = ADC module is enabled
 0 = ADC module is off
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **ADSIDL:** ADC Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-8 **Unimplemented:** Read as '0'
- bit 7 **NRE:** Noise Reduction Enable bit⁽²⁾
 1 = Holds conversion process for 1 TADCORE when another core completes conversion to reduce noise between cores
 0 = Noise reduction feature is disabled
- bit 6-0 **Unimplemented:** Read as '0'

- Note 1:** Set the ADON bit only after the ADC module has been configured. Changing ADC Configuration bits when ADON = 1 will result in unpredictable behavior.
- 2:** If the NRE bit in the ADCON1L register is set, the end of conversion time is adjusted to reduce the noise between ADC cores. Depending on the number of cores converting and the priority of the input, a few additional TADs may be inserted, making the conversion time slightly less deterministic.

dsPIC33EPXXGS202 FAMILY

REGISTER 19-2: ADCON1H: ADC CONTROL REGISTER 1 HIGH

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|---------|---------|-----|-----|-----|-----|-------|
| R/W-0 | R/W-1 | R/W-1 | U-0 | U-0 | U-0 | U-0 | U-0 |
| FORM | SHRRES1 | SHRRES0 | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 **FORM:** Fractional Data Output Format bit
 - 1 = Fractional
 - 0 = Integer
- bit 6-5 **SHRRES<1:0>:** Shared ADC Core Resolution Selection bits
 - 11 = 12-bit resolution
 - 10 = 10-bit resolution
 - 01 = 8-bit resolution
 - 00 = 6-bit resolution
- bit 4-0 **Unimplemented:** Read as '0'

dsPIC33EPXXGS202 FAMILY

REGISTER 19-3: ADCON2L: ADC CONTROL REGISTER 2 LOW

| | | | | | | | |
|--------|-------------------------|-----|-------|-----|--------------------------|--------------------------|--------------------------|
| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| REFCIE | REFERCIE ⁽²⁾ | — | EIEN | — | SHREISEL2 ⁽¹⁾ | SHREISEL1 ⁽¹⁾ | SHREISEL0 ⁽¹⁾ |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|----------|----------|----------|----------|----------|----------|----------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | SHRADCS6 | SHRADCS5 | SHRADCS4 | SHRADCS3 | SHRADCS2 | SHRADCS1 | SHRADCS0 |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **REFCIE:** Band Gap and Reference Voltage Ready Common Interrupt Enable bit
 1 = Common interrupt will be generated when the band gap will become ready
 0 = Common interrupt is disabled for the band gap ready event
- bit 14 **REFERCIE:** Band Gap or Reference Voltage Error Common Interrupt Enable bit⁽²⁾
 1 = Common interrupt will be generated when the band gap or reference voltage error is detected
 0 = Common interrupt is disabled for the band gap and reference voltage error event
- bit 13 **Unimplemented:** Read as '0'
- bit 12 **EIEN:** Early Interrupts Enable bit
 1 = The early interrupt feature is enabled for the input channels interrupts (when E1STATx flag is set)
 0 = The individual interrupts are generated when conversion is done (when ANxRDY flag is set)
- bit 11 **Unimplemented:** Read as '0'
- bit 10-8 **SHREISEL<2:0>:** Shared Core Early Interrupt Time Selection bits⁽¹⁾
 111 = Early interrupt is set and interrupt is generated 8 TADCORE clocks prior to when the data is ready
 110 = Early interrupt is set and interrupt is generated 7 TADCORE clocks prior to when the data is ready
 101 = Early interrupt is set and interrupt is generated 6 TADCORE clocks prior to when the data is ready
 100 = Early interrupt is set and interrupt is generated 5 TADCORE clocks prior to when the data is ready
 011 = Early interrupt is set and interrupt is generated 4 TADCORE clocks prior to when the data is ready
 010 = Early interrupt is set and interrupt is generated 3 TADCORE clocks prior to when the data is ready
 001 = Early interrupt is set and interrupt is generated 2 TADCORE clocks prior to when the data is ready
 000 = Early interrupt is set and interrupt is generated 1 TADCORE clock prior to when the data is ready
- bit 7 **Unimplemented:** Read as '0'
- bit 6-0 **SHRADCS<6:0>:** Shared ADC Core Input Clock Divider bits
 These bits determine the number of TCORESRC (Core Source Clock) periods for one shared TADCORE (ADC Core Clock) period.
 1111111 = 254 Core Source Clock periods
 .
 .
 .
 0000011 = 6 Core Source Clock periods
 0000010 = 4 Core Source Clock periods
 0000001 = 2 Core Source Clock periods
 0000000 = 2 Core Source Clock periods

- Note 1:** For the 6-bit shared ADC core resolution (SHRRES<1:0> = 00), the SHREISEL<2:0> settings, from '100' to '111', are not valid and should not be used. For the 8-bit shared ADC core resolution (SHRRES<1:0> = 01), the SHREISEL<2:0> settings, '110' and '111', are not valid and should not be used.
- 2:** To avoid false interrupts, the REFCIE bit must be set only after the module is enabled (ADON = 1).

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REGISTER 19-4: ADCON2H: ADC CONTROL REGISTER 2 HIGH

| | | | | | | | |
|-------------|-------------|-----|-----|-----|-----|----------|----------|
| R-0, HS, HC | R-0, HS, HC | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| REFRDY | REFERR | — | — | — | — | SHRSAMC9 | SHRSAMC8 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SHRSAMC7 | SHRSAMC6 | SHRSAMC5 | SHRSAMC4 | SHRSAMC3 | SHRSAMC2 | SHRSAMC1 | SHRSAMC0 |
| bit 7 | | | | | | bit 0 | |

| | | |
|-------------------|----------------------------|------------------------------------|
| Legend: | HS = Hardware Settable bit | HC = Hardware Clearable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15 **REFRDY:** Band Gap and Reference Voltage Ready Flag bit

1 = Band gap is ready
0 = Band gap is not ready

bit 14 **REFERR:** Band Gap or Reference Voltage Error Flag bit

1 = Band gap was removed after the ADC module was enabled (ADON = 1)
0 = No band gap error was detected

bit 13-10 **Unimplemented:** Read as '0'

bit 9-0 **SHRSAMC<9:0>:** Shared ADC Core Sample Time Selection bits

These bits specify the number of shared ADC Core Clock (TADCORE) periods for the shared ADC core sample time.

1111111111 = 1025 TADCORE

•
•
•

0000000001 = 3 TADCORE

0000000000 = 2 TADCORE

dsPIC33EPXXGS202 FAMILY

REGISTER 19-5: ADCON3L: ADC CONTROL REGISTER 3 LOW

| | | | | | | | |
|---------|---------|---------|---------|---------|-------------|---------|-------------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0, HS, HC | R/W-0 | R-0, HS, HC |
| REFSEL2 | REFSEL1 | REFSEL0 | SUSPEND | SUSPCIE | SUSPRDY | SHRSAMP | CNVRTCH |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|---------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|
| R/W-0 | R-0, HS, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SWLCTRG | SWCTRG | CNVCHSEL5 | CNVCHSEL4 | CNVCHSEL3 | CNVCHSEL2 | CNVCHSEL1 | CNVCHSEL0 |
| bit 7 | | | | | | | bit 0 |

| | | |
|-------------------|----------------------------|------------------------------------|
| Legend: | HS = Hardware Settable bit | HC = Hardware Clearable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15-13 **REFSEL<2:0>**: ADC Reference Voltage Selection bits

| Value | VREFH | VREFL |
|-------|-------|-------|
| 000 | AVDD | AVSS |

001-111 = **Unimplemented**: Should not be used

bit 12 **SUSPEND**: All ADC Cores Triggers Disable bit

1 = All new triggers events for all ADC cores are disabled

0 = All ADC cores can be triggered

bit 11 **SUSPCIE**: Suspend All ADC Cores Common Interrupt Enable bit

1 = Common interrupt will be generated when ADC cores triggers are suspended (SUSPEND bit = 1) and all previous conversions are finished (SUSPRDY bit becomes set)

0 = Common interrupt is not generated for suspend ADC cores event

bit 10 **SUSPRDY**: All ADC Cores Suspended Flag bit

1 = All ADC cores are suspended (SUSPEND bit = 1) and have no conversions in progress

0 = ADC cores have previous conversions in progress

bit 9 **SHRSAMP**: Shared ADC Core Sampling Direct Control bit

This bit should be used with the individual channel conversion trigger controlled by the CNVRTCH bit. It connects an analog input, specified by CNVCHSEL<5:0> bits, to the shared ADC core and allows extending the sampling time. This bit is not controlled by hardware and must be cleared before the conversion starts (setting CNVRTCH to '1').

1 = Shared ADC core samples an analog input specified by the CNVCHSEL<5:0> bits

0 = Sampling is controlled by the shared ADC core hardware

bit 8 **CNVRTCH**: Software Individual Channel Conversion Trigger bit

1 = Single trigger is generated for an analog input specified by the CNVCHSEL<5:0> bits. When the bit is set, it is automatically cleared by hardware on the next instruction cycle.

0 = Next individual channel conversion trigger can be generated

bit 7 **SWLCTRG**: Software Level-Sensitive Common Trigger bit

1 = Triggers are continuously generated for all channels with the software, level-sensitive, common trigger selected as a source in the ADTRIGxL and ADTRIGxH registers

0 = No software, level-sensitive, common triggers are generated

bit 6 **SWCTRG**: Software Common Trigger bit

1 = Single trigger is generated for all channels with the software, common trigger selected as a source in the ADTRIGxL and ADTRIGxH registers. When the bit is set, it is automatically cleared by hardware on the next instruction cycle

0 = Ready to generate the next software, common trigger

bit 5-0 **CNVCHSEL <5:0>**: Channel Number Selection for Software Individual Channel Conversion Trigger bits

These bits define a channel to be converted when the CNVRTCH bit is set.

dsPIC33EPXXGS202 FAMILY

REGISTER 19-6: ADCON3H: ADC CONTROL REGISTER 3 HIGH

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CLKSEL1 | CLKSEL0 | CLKDIV5 | CLKDIV4 | CLKDIV3 | CLKDIV2 | CLKDIV1 | CLKDIV0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-------|-------|
| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| SHREN | — | — | — | — | — | C1EN | COEN |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15-14 **CLKSEL<2:0>**: ADC Module Clock Source Selection bits

11 = APLL
 10 = FRC
 01 = FOSC (System Clock x 2)
 00 = FSYS (System Clock)

bit 13-8 **CLKDIV<5:0>**: ADC Module Clock Source Divider bits

The divider forms a Tcoresrc clock used by all ADC cores (shared and dedicated) from the Tsrc ADC module clock source selected by the CLKSEL<2:0> bits. Then, each ADC core individually divides the Tcoresrc clock to get a core-specific TadcCore clock using the ADCS<6:0> bits in the ADCORExH register or the SHRADCS<6:0> bits in the ADCON2L register.

111111 = 64 Core Source Clock periods

•
•
•

000011 = 4 Core Source Clock periods
 000010 = 3 Core Source Clock periods
 000001 = 2 Core Source Clock periods
 000000 = 1 Core Source Clock period

bit 7 **SHREN**: Shared ADC Core Enable bit

This bit does not disable the core clock and analog bias circuitry.
 1 = Shared ADC core is enabled
 0 = Shared ADC core is disabled

bit 6-2 **Unimplemented**: Read as '0'

bit 1-0 **C1EN:COEN**: Dedicated ADC Core x Enable bits

This bit does not disable the core clock and analog bias circuitry.
 1 = Dedicated ADC Core x is enabled
 0 = Dedicated ADC Core x is disabled

dsPIC33EPXXGS202 FAMILY

REGISTER 19-7: ADCON4L: ADC CONTROL REGISTER 4 LOW

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-------|-----|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | r-0 | r-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|---------|---------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | — | SAMC1EN | SAMC0EN |
| bit 7 | | | | | | bit 0 | |

| | | | |
|-------------------|------------------|------------------------------------|--------------------|
| Legend: | r = Reserved bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-10 **Unimplemented:** Read as '0'

bit 9-8 **Reserved:** Maintain as '0'

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **SAMC1EN:SAMC0EN:** Dedicated ADC Core x Conversion Delay Enable bits

- 1 = After trigger, the conversion will be delayed and the ADC core will continue sampling during the time specified by the SAMC<9:0> bits in the ADCORExL register
- 0 = After trigger, the sampling will be stopped immediately and the conversion will be started on the next core clock cycle.

dsPIC33EPXXGS202 FAMILY

REGISTER 19-8: ADCON4H: ADC CONTROL REGISTER 4 HIGH

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|--------|--------|--------|--------|
| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | C1CHS1 | C1CHS0 | C0CHS1 | C0CHS0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3-2 **C1CHS<1:0>:** Dedicated ADC Core 1 Input Channel Selection bits

11 = PGA2

10 = PGA1

01 = AN8

00 = AN1

AN8 is a negative input when DIFF1 (ADM0D0L<3>) = 1.

bit 1-0 **C0CHS<1:0>:** Dedicated ADC Core 0 Input Channel Selection bits

11 = PGA2

10 = PGA1

01 = AN7

00 = AN0

AN7 is a negative input when DIFF0 (ADM0D0L<1>) = 1.

dsPIC33EPXXGS202 FAMILY

REGISTER 19-9: ADCON5L: ADC CONTROL REGISTER 5 LOW

| | | | | | | | |
|-------------|-----|-----|-----|-----|-----|-------------|-------------|
| R-0, HC, HS | U-0 | U-0 | U-0 | U-0 | U-0 | R-0, HC, HS | R-0, HC, HS |
| SHRRDY | — | — | — | — | — | C1RDY | C0RDY |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-------|-------|
| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| SHRPWR | — | — | — | — | — | C1PWR | C0PWR |
| bit 7 | | | | | | bit 0 | |

| | | |
|-------------------|----------------------------|--|
| Legend: | HS = Hardware Settable bit | HC = Hardware Clearable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15 **SHRRDY:** Shared ADC Core Ready Flag bit
1 = ADC core is powered and ready for operation
0 = ADC core is not ready for operation
- bit 14-10 **Unimplemented:** Read as '0'
- bit 9-8 **C1RDY:C0RDY:** Dedicated ADC Core x Ready Flag bits
1 = ADC Core x is powered and ready for operation
0 = ADC Core x is not ready for operation
- bit 7 **SHRPWR:** Shared ADC Core x Power Enable bit
1 = ADC Core x is powered
0 = ADC Core x is off
- bit 6-2 **Unimplemented:** Read as '0'
- bit 1-0 **C1PWR:C0PWR:** Dedicated ADC Core x Power Enable bits
1 = ADC Core x is powered
0 = ADC Core x is off

dsPIC33EPXXGS202 FAMILY

REGISTER 19-10: ADCON5H: ADC CONTROL REGISTER 5 HIGH

| | | | | | | | |
|--------|-----|-----|-----|-----------|-----------|-----------|-----------|
| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | WARMTIME3 | WARMTIME2 | WARMTIME1 | WARMTIME0 |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-------|-------|
| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| SHRCIE | — | — | — | — | — | C1CIE | C0CIE |
| bit 7 | | | | | | bit 0 | |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **WARMTIME<3:0>:** ADC Cores Power-up Delay bits

These bits determine the power-up delay in the number of the Core Source Clock (TCORESRC) periods for all ADC cores.

1111 = 32768 Core Source Clock periods

1110 = 16384 Core Source Clock periods

1101 = 8192 Core Source Clock periods

1100 = 4096 Core Source Clock periods

1011 = 2048 Core Source Clock periods

1010 = 1024 Core Source Clock periods

1001 = 512 Core Source Clock periods

1000 = 256 Core Source Clock periods

0111 = 128 Core Source Clock periods

0110 = 64 Core Source Clock periods

0101 = 32 Core Source Clock periods

0000-0100 = 16 Core Source Clock periods

bit 7 **SHRCIE:** Shared ADC Core Ready Common Interrupt Enable bit

1 = Common interrupt will be generated when ADC core is powered and ready for operation

0 = Common interrupt is disabled for an ADC core ready event

bit 6-2 **Unimplemented:** Read as '0'

bit 1-0 **C1CIE:C0CIE:** Dedicated ADC Core x Ready Common Interrupt Enable bits

1 = Common interrupt will be generated when ADC Core x is powered and ready for operation

0 = Common interrupt is disabled for an ADC Core x ready event

dsPIC33EPXXGS202 FAMILY

REGISTER 19-11: ADCORExL: DEDICATED ADC CORE x CONTROL REGISTER LOW (x = 0,1)

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----------|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | — | SAMC<9:8> | |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SAMC<7:0> | | | | | | | |
| bit 7 | | | | | | bit 0 | |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **SAMC<9:0>:** Dedicated ADC Core x Conversion Delay Selection bits

These bits determine the time between the trigger event and the start of conversion in the number of the ADC Core Clock (TADCORE) periods. During this time, the ADC Core x still continues sampling. This feature is enabled by the SAMCxEN bit in the ADCON4L register.

1111111111 = 1025 TADCORE

•

•

•

0000000001 = 3 TADCORE

0000000000 = 2 TADCORE

dsPIC33EPXXGS202 FAMILY

REGISTER 19-12: ADCORExH: DEDICATED ADC CORE x CONTROL REGISTER HIGH (x = 0,1)

| | | | | | | | |
|--------|-----|-----|-----------------------|-----------------------|-----------------------|-------|-------|
| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
| — | — | — | EISEL2 ⁽¹⁾ | EISEL1 ⁽¹⁾ | EISEL0 ⁽¹⁾ | RES1 | RES0 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | ADCS6 | ADCS5 | ADCS4 | ADCS3 | ADCS2 | ADCS1 | ADCS0 |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-10 **EISEL<2:0>:** ADC Core x Early Interrupt Time Selection bits⁽¹⁾

111 = Early interrupt is set and an interrupt is generated 8 TADCORE clocks prior to when the data is ready
 110 = Early interrupt is set and an interrupt is generated 7 TADCORE clocks prior to when the data is ready
 101 = Early interrupt is set and an interrupt is generated 6 TADCORE clocks prior to when the data is ready
 100 = Early interrupt is set and an interrupt is generated 5 TADCORE clocks prior to when the data is ready
 011 = Early interrupt is set and an interrupt is generated 4 TADCORE clocks prior to when the data is ready
 010 = Early interrupt is set and an interrupt is generated 3 TADCORE clocks prior to when the data is ready
 001 = Early interrupt is set and an interrupt is generated 2 TADCORE clocks prior to when the data is ready
 000 = Early interrupt is set and an interrupt is generated 1 TADCORE clock prior to when the data is ready

bit 9-8 **RES<1:0>:** ADC Core x Resolution Selection bits

11 = 12-bit resolution
 10 = 10-bit resolution
 01 = 8-bit resolution
 00 = 6-bit resolution

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ADCS<6:0>:** ADC Core x Input Clock Divider bits

These bits determine the number of Core Source Clock (TCORESRC) periods for one ADC Core Clock (TADCORE) period.

1111111 = 254 Core Source Clock periods

•
•
•

0000011 = 6 Core Source Clock periods

0000010 = 4 Core Source Clock periods

0000001 = 2 Core Source Clock periods

0000000 = 2 Core Source Clock periods

Note 1: For the 6-bit ADC core resolution (RES<1:0> = 00), the EISEL<2:0> bits settings, from '100' to '111', are not valid and should not be used. For the 8-bit ADC core resolution (RES<1:0> = 01), the EISEL<2:0> bits settings, '110' and '111', are not valid and should not be used.

dsPIC33EPXXGS202 FAMILY

REGISTER 19-13: ADLVLTRGL: ADC LEVEL-SENSITIVE TRIGGER CONTROL REGISTER LOW

| | | | | | | | | |
|--------|-------------|-------|-------|-------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | |
| — | LVLEN<14:8> | | | | | | | |
| bit 15 | | | | | | | | bit 8 |

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| LVLEN<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | | |
|-------------------|------------------|------------------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **LVLEN<14:0>:** Level Trigger x Enable bits
 1 = Input Channel x trigger is level-sensitive
 0 = Input Channel x trigger is edge-sensitive

dsPIC33EPXXGS202 FAMILY

REGISTER 19-14: ADEIEL: ADC EARLY INTERRUPT ENABLE REGISTER LOW

| | | | | | | | |
|--------|------------|-------|-------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | EIEN<14:8> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| EIEN<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **EIEN<14:0>:** Early Interrupt Enable for Corresponding Analog Inputs bits

1 = Early interrupt is enabled for the channel

0 = Early interrupt is disabled for the channel

REGISTER 19-15: ADEISTATL: ADC EARLY INTERRUPT STATUS REGISTER LOW

| | | | | | | | |
|--------|--------------|-------|-------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | EISTAT<14:8> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| EISTAT<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **EISTAT<14:0>:** Early Interrupt Status for Corresponding Analog Inputs bits

1 = Early interrupt was generated

0 = Early interrupt was not generated since the last ADCBUFx read

dsPIC33EPXXGS202 FAMILY

REGISTER 19-16: ADMOD0L: ADC INPUT MODE CONTROL REGISTER 0 LOW

| | | | | | | | |
|--------|-------|-----|-------|-----|-------|-------|-------|
| U-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 |
| — | SIGN7 | — | SIGN6 | — | SIGN5 | — | SIGN4 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-------|-----|-------|----------------------|-------|----------------------|-------|
| U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | SIGN3 | — | SIGN2 | DIFF1 ⁽²⁾ | SIGN1 | DIFF0 ⁽¹⁾ | SIGN0 |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit (odd)15-5 **Unimplemented:** Read as '0'
- bit (3,1) **DIFF<x>:** Pseudodifferential Mode for Corresponding Analog Inputs bits^(1,2)
 - 1 = Channel is pseudodifferential
 - 0 = Channel is single-ended
- bit (even) **SIGNx:** Output Data Sign for Corresponding Analog Inputs bits
 - 1 = Channel output data is signed
 - 0 = Channel output data is unsigned

- Note 1:** AN7 is a negative input when DIFF0 = 1.
- Note 2:** AN8 is a negative input when DIFF1 = 1.

REGISTER 19-17: ADMOD0H: ADC INPUT MODE CONTROL REGISTER 0 HIGH

| | | | | | | | |
|--------|-----|-----|--------|-----|--------|-------|--------|
| U-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 |
| — | — | — | SIGN14 | — | SIGN13 | — | SIGN12 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|--------|-----|--------|-----|-------|-------|-------|
| U-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 |
| — | SIGN11 | — | SIGN10 | — | SIGN9 | — | SIGN8 |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit (odd) **Unimplemented:** Read as '0'
- bit (even) **SIGN<x>:** Output Data Sign for Corresponding Analog Inputs bits
 - 1 = Channel output data is signed
 - 0 = Channel output data is unsigned

dsPIC33EPXXGS202 FAMILY

REGISTER 19-18: ADIEL: ADC INTERRUPT ENABLE REGISTER LOW

| | | | | | | | |
|--------|----------|-------|-------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | IE<14:8> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|---------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| IE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| | | | |
|-------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **IE<14:0>:** Common Interrupt Enable bits
 1 = Common and individual interrupts are enabled for the corresponding channel
 0 = Common and individual interrupts are disabled for the corresponding channel

REGISTER 19-19: ADSTATL: ADC DATA READY STATUS REGISTER LOW

| | | | | | | | |
|--------|-------------|----------|----------|----------|----------|----------|----------|
| U-0 | R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
| — | AN<14:8>RDY | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|------------|----------|----------|----------|----------|----------|----------|----------|
| R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
| AN<7:0>RDY | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| | | | |
|-------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **AN<14:0>RDY:** ADC Conversion Data Ready for Corresponding Analog Input bits
 1 = Channel conversion result is ready in the corresponding ADCBUFx register
 0 = Channel conversion result is not ready

dsPIC33EPXXGS202 FAMILY

REGISTER 19-20: ADTRIGxL: ADC CHANNEL TRIGGER x SELECTION REGISTER LOW (x = 0 to 3)

| | | | | | | | |
|--------|-----|-----|-------------------|-------|-------|-------|-------|
| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | TRGSRC(4x+1)<4:0> | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----------------|-------|-------|-------|-------|
| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | TRGSRC(4x)<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC(4x+1)<4:0>:** Trigger Source Selection for Corresponding Analog Inputs bits

- 11111 = ADTRG31
- 11110 = Reserved
- 11101 = Reserved
- 11100 = Reserved
- 11011 = Reserved
- 11010 = PWM Generator 3 current-limit trigger
- 11001 = PWM Generator 2 current-limit trigger
- 11000 = PWM Generator 1 current-limit trigger
- 10111 = Reserved
- 10110 = Output Compare 1 trigger
- 10101 = Reserved
- 10100 = Reserved
- 10011 = Reserved
- 10010 = Reserved
- 10001 = PWM Generator 3 secondary trigger
- 10000 = PWM Generator 2 secondary trigger
- 01111 = PWM Generator 1 secondary trigger
- 01110 = PWM secondary Special Event Trigger
- 01101 = Timer2 period match
- 01100 = Timer1 period match
- 01011 = Reserved
- 01010 = Reserved
- 01001 = Reserved
- 01000 = Reserved
- 00111 = PWM Generator 3 primary trigger
- 00110 = PWM Generator 2 primary trigger
- 00101 = PWM Generator 1 primary trigger
- 00100 = PWM Special Event Trigger
- 00011 = Reserved
- 00010 = Level software trigger
- 00001 = Common software trigger
- 00000 = No trigger is enabled

bit 7-5 **Unimplemented:** Read as '0'

dsPIC33EPXXGS202 FAMILY

REGISTER 19-20: ADTRIGxL: ADC CHANNEL TRIGGER x SELECTION REGISTER LOW (x = 0 to 3) (CONTINUED)

bit 4-0 **TRGSRC(4x)<4:0>**: Trigger Source Selection for Corresponding Analog Inputs bits

11111 = ADTRG31
11110 = Reserved
11101 = Reserved
11100 = Reserved
11011 = Reserved
11010 = PWM Generator 3 current-limit trigger
11001 = PWM Generator 2 current-limit trigger
11000 = PWM Generator 1 current-limit trigger
10111 = Reserved
10110 = Output Compare 1 trigger
10101 = Reserved
10100 = Reserved
10011 = Reserved
10010 = Reserved
10001 = PWM Generator 3 secondary trigger
10000 = PWM Generator 2 secondary trigger
01111 = PWM Generator 1 secondary trigger
01110 = PWM secondary Special Event Trigger
01101 = Timer2 period match
01100 = Timer1 period match
01011 = Reserved
01010 = Reserved
01001 = Reserved
01000 = Reserved
00111 = PWM Generator 3 primary trigger
00110 = PWM Generator 2 primary trigger
00101 = PWM Generator 1 primary trigger
00100 = PWM Special Event Trigger
00011 = Reserved
00010 = Level software trigger
00001 = Common software trigger
00000 = No trigger is enabled

dsPIC33EPXXGS202 FAMILY

REGISTER 19-21: ADTRIGxH: ADC CHANNEL TRIGGER x SELECTION REGISTER HIGH (x = 0 to 3)

| | | | | | | | |
|--------|-----|-----|-------------------|-------|-------|-------|-------|
| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | TRGSRC(4x+3)<4:0> | | | | |
| bit 15 | | | bit 8 | | | | |

| | | | | | | | |
|-------|-----|-----|-------------------|-------|-------|-------|-------|
| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | TRGSRC(4x+2)<4:0> | | | | |
| bit 7 | | | bit 0 | | | | |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC(4x+3)<4:0>**: Trigger Source Selection for Corresponding Analog Inputs bits

11111 = ADTRG31
 11110 = Reserved
 11101 = Reserved
 11100 = Reserved
 11011 = Reserved
 11010 = PWM Generator 3 current-limit trigger
 11001 = PWM Generator 2 current-limit trigger
 11000 = PWM Generator 1 current-limit trigger
 10111 = Reserved
 10110 = Output Compare 1 trigger
 10101 = Reserved
 10100 = Reserved
 10011 = Reserved
 10010 = Reserved
 10001 = PWM Generator 3 secondary trigger
 10000 = PWM Generator 2 secondary trigger
 01111 = PWM Generator 1 secondary trigger
 01110 = PWM secondary Special Event Trigger
 01101 = Timer2 period match
 01100 = Timer1 period match
 01011 = Reserved
 01010 = Reserved
 01001 = Reserved
 01000 = Reserved
 00111 = PWM Generator 3 primary trigger
 00110 = PWM Generator 2 primary trigger
 00101 = PWM Generator 1 primary trigger
 00100 = PWM Special Event Trigger
 00011 = Reserved
 00010 = Level software trigger
 00001 = Common software trigger
 00000 = No trigger is enabled

bit 7-5 **Unimplemented:** Read as '0'

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REGISTER 19-21: ADTRIGxH: ADC CHANNEL TRIGGER x SELECTION REGISTER HIGH (x = 0 to 3) (CONTINUED)

bit 4-0 **TRGSRC(4x+2)<4:0>**: Trigger Source Selection for Corresponding Analog Inputs bits

11111 = ADTRG31
11110 = Reserved
11101 = Reserved
11100 = Reserved
11011 = Reserved
11010 = PWM Generator 3 current-limit trigger
11001 = PWM Generator 2 current-limit trigger
11000 = PWM Generator 1 current-limit trigger
10111 = Reserved
10110 = Output Compare 1 trigger
10101 = Reserved
10100 = Reserved
10011 = Reserved
10010 = Reserved
10001 = PWM Generator 3 secondary trigger
10000 = PWM Generator 2 secondary trigger
01111 = PWM Generator 1 secondary trigger
01110 = PWM secondary Special Event Trigger
01101 = Timer2 period match
01100 = Timer1 period match
01011 = Reserved
01010 = Reserved
01001 = Reserved
01000 = Reserved
00111 = PWM Generator 3 primary trigger
00110 = PWM Generator 2 primary trigger
00101 = PWM Generator 1 primary trigger
00100 = PWM Special Event Trigger
00011 = Reserved
00010 = Level software trigger
00001 = Common software trigger
00000 = No trigger is enabled

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REGISTER 19-22: ADCAL0L: ADC CALIBRATION REGISTER 0 LOW

| | | | | | | | |
|----------|-----|-----|-----|-----|----------|--------|---------|
| R-0, HSC | U-0 | U-0 | U-0 | r-0 | R/W-0 | R/W-0 | R/W-0 |
| CAL1RDY | — | — | — | — | CAL1DIFF | CAL1EN | CAL1RUN |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|----------|-----|-----|-----|-----|----------|--------|---------|
| R-0, HSC | U-0 | U-0 | U-0 | r-0 | R/W-0 | R/W-0 | R/W-0 |
| CAL0RDY | — | — | — | — | CAL0DIFF | CAL0EN | CAL0RUN |
| bit 7 | | | | | | | bit 0 |

| | | |
|-------------------|------------------|--|
| Legend: | r = Reserved bit | HSC= Hardware Settable/Clearable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15 **CAL1RDY:** Dedicated ADC Core 1 Calibration Status Flag bit
 1 = Dedicated ADC Core 1 calibration is finished
 0 = Dedicated ADC Core 1 calibration is in progress
- bit 14-12 **Unimplemented:** Read as '0'
- bit 11 **Reserved:** Must be written as '0'
- bit 10 **CAL1DIFF:** Dedicated ADC Core 1 Pseudodifferential Input Mode Calibration bit
 1 = Dedicated ADC Core 1 will be calibrated in Pseudodifferential Input mode
 0 = Dedicated ADC Core 1 will be calibrated in Single-Ended Input mode
- bit 9 **CAL1EN:** Dedicated ADC Core 1 Calibration Enable bit
 1 = Dedicated ADC Core 1 calibration bits (CALxRDY, CALxDIFF and CALxRUN) can be accessed by software
 0 = Dedicated ADC Core 1 calibration bits are disabled
- bit 8 **CAL1RUN:** Dedicated ADC Core 1 Calibration Start bit
 1 = If this bit is set by software, the dedicated ADC Core 1 calibration cycle is started; this bit is automatically cleared by hardware
 0 = Software can start the next calibration cycle
- bit 7 **CAL0RDY:** Dedicated ADC Core 0 Calibration Status Flag bit
 1 = Dedicated ADC Core 0 calibration is finished
 0 = Dedicated ADC Core 0 calibration is in progress
- bit 6-4 **Unimplemented:** Read as '0'
- bit 3 **Reserved:** Must be written as '0'
- bit 2 **CAL0DIFF:** Dedicated ADC Core 0 Pseudodifferential Input Mode Calibration bit
 1 = Dedicated ADC Core 0 will be calibrated in Pseudodifferential Input mode
 0 = Dedicated ADC Core 0 will be calibrated in Single-Ended Input mode
- bit 1 **CAL0EN:** Dedicated ADC Core 0 Calibration Enable bit
 1 = Dedicated ADC Core 0 calibration bits (CALxRDY, CALxDIFF and CALxRUN) can be accessed by software
 0 = Dedicated ADC Core 0 calibration bits are disabled
- bit 0 **CAL0RUN:** Dedicated ADC Core 0 Calibration Start bit
 1 = If this bit is set by software, the dedicated ADC Core 0 calibration cycle is started; this bit is automatically cleared by hardware
 0 = Software can start the next calibration cycle

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REGISTER 19-23: ADCAL1H: ADC CALIBRATION REGISTER 1 HIGH

| | | | | | | | |
|-----------|-----|-----|-----|-----|-----|--------|---------|
| R/W-0, HS | U-0 | U-0 | U-0 | r-0 | U-0 | R/W-0 | R/W-0 |
| CSHRRDY | — | — | — | — | — | CSHREN | CSHRRUN |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-------|-----|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | bit 0 | |

| | | |
|-------------------|----------------------------|------------------------------------|
| Legend: | HS = Hardware Settable bit | r = Reserved bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 15 **CSHRRDY:** Shared ADC Core Calibration Status Flag bit
1 = Shared ADC core calibration is finished
0 = Shared ADC core calibration is in progress
- bit 14-12 **Unimplemented:** Read as '0'
- bit 11 **Reserved:** Must be written as '0'
- bit 10 **Unimplemented:** Read as '0'
- bit 9 **CSHREN:** Shared ADC Core Calibration Enable bit
1 = Shared ADC core calibration bits (CSHRRDY and CSHRRUN) can be accessed by software
0 = Shared ADC core calibration bits are disabled
- bit 8 **CSHRRUN:** Shared ADC Core Calibration Start bit
1 = If this bit is set by software, the shared ADC core calibration cycle is started; this bit is cleared automatically by hardware
0 = Software can start the next calibration cycle
- bit 7-0 **Unimplemented:** Read as '0'

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REGISTER 19-24: ADCMPxCON: ADC DIGITAL COMPARATOR x CONTROL REGISTER (x = 0,1)

| | | | | | | | |
|--------|-----|-----|----------|----------|----------|----------|----------|
| U-0 | U-0 | U-0 | R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
| — | — | — | CHNL4 | CHNL3 | CHNL2 | CHNL1 | CHNL0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-------|-------------|-------|-------|-------|-------|-------|
| R/W/0 | R/W-0 | R-0, HC, HS | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CMPEN | IE | STAT | BTWN | HIHI | HILO | LOHI | LOLO |
| bit 7 | | | | | | | bit 0 |

| | | |
|-------------------|----------------------------|---------------------------------------|
| Legend: | HS = Hardware Settable bit | HSC = Hardware Settable/Clearable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | HC = Hardware Clearable bit |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **CHNL<4:0>:** Input Channel Number bits

If the comparator has detected an event for a channel, this channel number is written to these bits.

01111-11111 = Reserved

01110 = BG (AN14)

01101 = PGA2 (AN13)

01100 = PGA1 (AN12)

•

•

•

00001 = AN1

00000 = AN0

bit 7 **CMPEN:** Digital Comparator Enable bit

1 = Digital comparator is enabled

0 = Digital comparator is disabled and the STAT status bit is cleared

bit 6 **IE:** Comparator Common ADC Interrupt Enable bit

1 = Common ADC interrupt will be generated if the comparator detects a comparison event

0 = Common ADC interrupt will not be generated for the comparator

bit 5 **STAT:** Comparator Event Status bit

This bit is cleared by hardware when the channel number is read from the CHNL<4:0> bits.

1 = A comparison event has been detected since the last read of the CHNL<4:0> bits

0 = A comparison event has not been detected since the last read of the CHNL<4:0> bits

bit 4 **BTWN:** Between Low/High Comparator Event bit

1 = Generates a digital comparator event when $ADCMPxLO \leq ADCBUFx < ADCMPxHI$

0 = Does not generate a digital comparator event when $ADCMPxLO \leq ADCBUFx < ADCMPxHI$

bit 3 **HIHI:** High/High Comparator Event bit

1 = Generates a digital comparator event when $ADCBUFx \geq ADCMPxHI$

0 = Does not generate a digital comparator event when $ADCBUFx \geq ADCMPxHI$

bit 2 **HILO:** High/Low Comparator Event bit

1 = Generates a digital comparator event when $ADCBUFx < ADCMPxHI$

0 = Does not generate a digital comparator event when $ADCBUFx < ADCMPxHI$

bit 1 **LOHI:** Low/High Comparator Event bit

1 = Generates a digital comparator event when $ADCBUFx \geq ADCMPxLO$

0 = Does not generate a digital comparator event when $ADCBUFx \geq ADCMPxLO$

bit 0 **LOLO:** Low/Low Comparator Event bit

1 = Generates a digital comparator event when $ADCBUFx < ADCMPxLO$

0 = Does not generate a digital comparator event when $ADCBUFx < ADCMPxLO$

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REGISTER 19-25: ADCMP_xENL: ADC DIGITAL COMPARATOR x CHANNEL ENABLE REGISTER LOW (x = 0,1)

| | | | | | | | | |
|--------|-------------|-------|-------|-------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | |
| — | CMPEN<14:8> | | | | | | | |
| bit 15 | | | | | | | | bit 8 |

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W/0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CMPEN<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **CMPEN<14:0>:** Comparator Enable for Corresponding Input Channels bits

1 = Conversion result for corresponding channel is used by the comparator

0 = Conversion result for corresponding channel is not used by the comparator

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REGISTER 19-26: ADFL0CON: ADC DIGITAL FILTER 0 CONTROL REGISTER

| | | | | | | | |
|--------|-------|-------|---------|---------|---------|-------|----------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0, HSC |
| FLEN | MODE1 | MODE0 | OVRSAM2 | OVRSAM1 | OVRSAM0 | IE | RDY |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|----------|----------|----------|----------|----------|
| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | FLCHSEL4 | FLCHSEL3 | FLCHSEL2 | FLCHSEL1 | FLCHSEL0 |
| bit 7 | | | | | | | bit 0 |

| | | | |
|-------------------|---------------------------------------|------------------------------------|--------------------|
| Legend: | HSC = Hardware Settable/Clearable bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

- bit 15 **FLEN:** Filter Enable bit
 1 = Filter is enabled
 0 = Filter is disabled and the RDY bit is cleared
- bit 14-13 **MODE<1:0>:** Filter Mode bits
 11 = Averaging mode
 10 = Reserved
 01 = Reserved
 00 = Oversampling mode
- bit 12-10 **OVRSAM<2:0>:** Filter Averaging/Oversampling Ratio bits
 If MODE<1:0> = 00:
 111 = 128x (16-bit result in the ADFL0DAT register is in 12.4 format)
 110 = 32x (15-bit result in the ADFL0DAT register is in 12.3 format)
 101 = 8x (14-bit result in the ADFL0DAT register is in 12.2 format)
 100 = 2x (13-bit result in the ADFL0DAT register is in 12.1 format)
 011 = 256x (16-bit result in the ADFL0DAT register is in 12.4 format)
 010 = 64x (15-bit result in the ADFL0DAT register is in 12.3 format)
 001 = 16x (14-bit result in the ADFL0DAT register is in 12.2 format)
 000 = 4x (13-bit result in the ADFL0DAT register is in 12.1 format)
 If MODE<1:0> = 11 (12-bit result in the ADFL0DAT register):
 111 = 256x
 110 = 128x
 101 = 64x
 100 = 32x
 011 = 16x
 010 = 8x
 001 = 4x
 000 = 2x
- bit 9 **IE:** Filter Common ADC Interrupt Enable bit
 1 = Common ADC interrupt will be generated when the filter result will be ready
 0 = Common ADC interrupt will not be generated for the filter
- bit 8 **RDY:** Oversampling Filter Data Ready Flag bit
 This bit is cleared by hardware when the result is read from the ADFL0DAT register.
 1 = Data in the ADFL0DAT register is ready
 0 = The ADFL0DAT register has been read and new data in the ADFL0DAT register is not ready
- bit 7-5 **Unimplemented:** Read as '0'

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REGISTER 19-26: ADFL0CON: ADC DIGITAL FILTER 0 CONTROL REGISTER (CONTINUED)

bit 4-0 **FLCHSEL<4:0>**: Oversampling Filter Input Channel Selection bits

01111-11111 = Reserved

01110 = BG (AN14)

01101 = PGA2 (AN13)

01100 = PGA1 (AN12)

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00001 = AN1

00000 = AN0

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NOTES:

20.0 HIGH-SPEED ANALOG COMPARATOR

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**High-Speed Analog Comparator Module**” (DS70005128) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to [Section 4.0 “Memory Organization”](#) in this data sheet for device-specific register and bit information.

The high-speed analog comparator module monitors current and/or voltage transients that may be too fast for the CPU and ADC to capture.

20.1 Features Overview

The SMPS comparator module offers the following major features:

- Two Rail-to-Rail Analog Comparators
- Dedicated 12-Bit DAC for each Analog Comparator
- Up to Six Selectable Input Sources per Comparator:
 - Four external inputs
 - Two internal inputs from the PGAx module
- Programmable Comparator Hysteresis
- Programmable Output Polarity
- Voltage References for the DACx:
 - AVDD
- Interrupt Generation Capability
- Functional Support for PWM:
 - PWM duty cycle control
 - PWM period control
 - PWM Fault detected

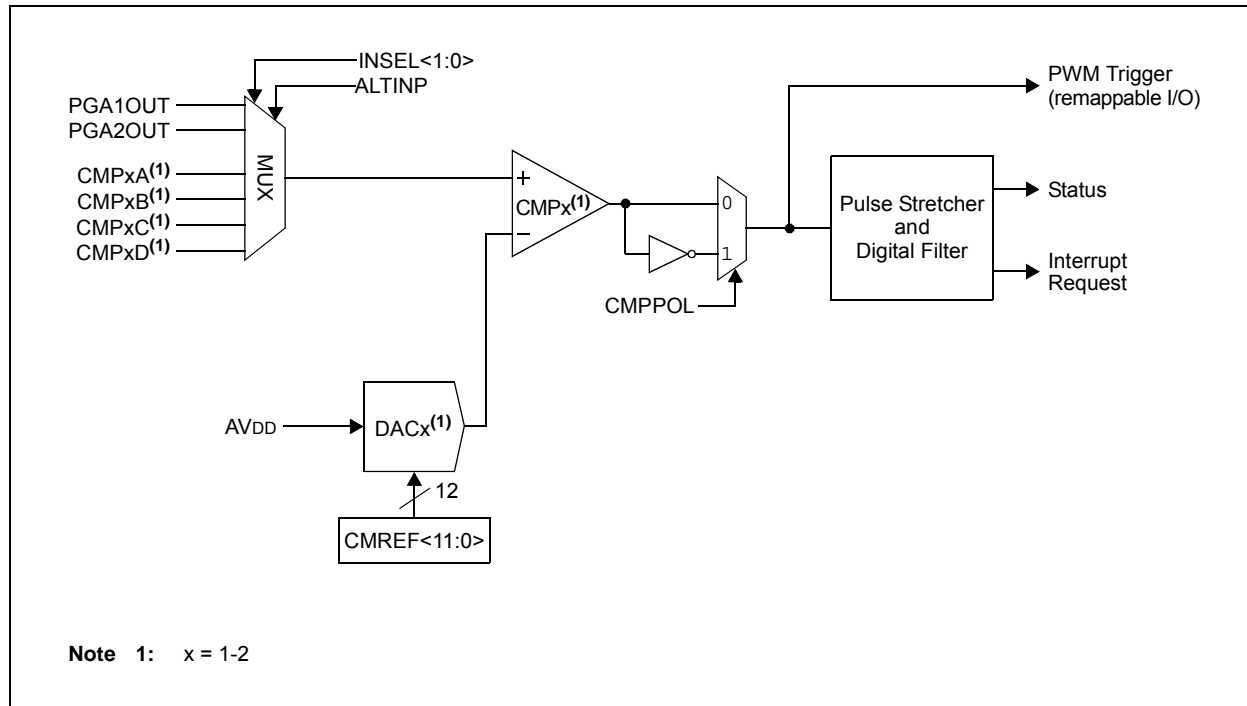
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20.2 Module Description

Figure 20-1 shows a functional block diagram of one analog comparator from the high-speed analog comparator module. The analog comparator provides high-speed operation with a typical delay of 15 ns. The negative input of the comparator is always connected to the DACx circuit. The positive input of the comparator is connected to an analog multiplexer that selects the desired source pin.

The analog comparator input pins are typically shared with pins used by the Analog-to-Digital Converter (ADC) module. Both the comparator and the ADC can use the same pins at the same time. This capability enables a user to measure an input voltage with the ADC and detect voltage transients with the comparator.

FIGURE 20-1: HIGH-SPEED ANALOG COMPARATOR x MODULE BLOCK DIAGRAM



20.3 Module Applications

This module provides a means for the SMPS dsPIC® DSC devices to monitor voltage and currents in a power conversion application. The ability to detect transient conditions, and stimulate the dsPIC DSC processor and/or peripherals, without requiring the processor and ADC to constantly monitor voltages or currents, frees the dsPIC DSC to perform other tasks.

The comparator module has a high-speed comparator and an associated 12-bit DAC that provides a programmable reference voltage to the inverting input of the comparator. The polarity of the comparator output is user-programmable. The output of the module can be used in the following modes:

- Generate an Interrupt
- Trigger an ADC Sample and Convert Process
- Truncate the PWM Signal (current-limit)
- Truncate the PWM Period (current minimum)
- Disable the PWM Outputs (Fault latch)

The output of the comparator module may be used in multiple modes at the same time, such as: 1) Generate an interrupt, 2) Have the ADC take a sample and convert it, and 3) Truncate the PWM output in response to a voltage being detected beyond its expected value.

The comparator module can also be used to wake-up the system from Sleep or Idle mode when the analog input voltage exceeds the programmed threshold voltage.

20.4 DAC

Each analog comparator has a dedicated 12-bit DAC that is used to program the comparator threshold voltage via the CMPxDAC register.

20.5 Pulse Stretcher and Digital Logic

The analog comparator can respond to very fast transient signals. After the comparator output is given the desired polarity, the signal is passed to a pulse stretching circuit. The pulse stretching circuit has an asynchronous set function and a delay circuit that ensures the minimum pulse width is three system clock cycles wide to allow the attached circuitry to properly respond to a narrow pulse event.

The pulse stretcher circuit is followed by a digital filter. The digital filter is enabled via the FLTREN bit in the CMPxCON register. The digital filter operates with the clock specified via the FCLKSEL bit in the CMPxCON register. The comparator signal must be stable in a high or low state, for at least three of the selected clock cycles, for it to pass through the digital filter.

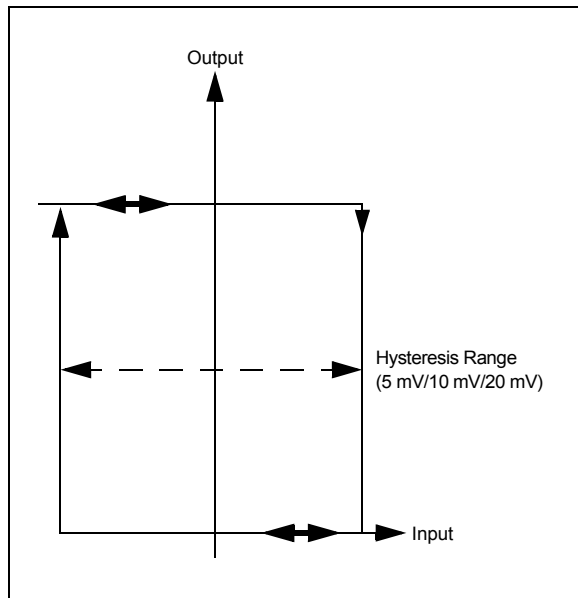
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20.6 Hysteresis

An additional feature of the module is hysteresis control. Hysteresis can be enabled or disabled and its amplitude can be controlled by the HYSSEL<1:0> bits in the CMPxCON register. Three different values are available: 5 mV, 10 mV and 20 mV. It is also possible to select the edge (rising or falling) to which hysteresis is to be applied.

Hysteresis control prevents the comparator output from continuously changing state because of small perturbations (noise) at the input (see [Figure 20-2](#)).

FIGURE 20-2: HYSTERESIS CONTROL



20.7 Analog Comparator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

20.7.1 KEY RESOURCES

- **“High-Speed Analog Comparator Module”** (DS70005128) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

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20.8 High-Speed Analog Comparator Control Registers

REGISTER 20-1: CMPxCON: COMPARATOR x CONTROL REGISTER (x = 1,2)

| | | | | | | | |
|--------|-----|---------|---------|---------|--------|---------|-------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
| CMPON | — | CMPSIDL | HYSSEL1 | HYSSEL0 | FLTREN | FCLKSEL | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|--------|--------|-----|--------|---------|--------|--------|-------|
| R/W-0 | R/W-0 | U-0 | R/W-0 | HC/HS-0 | R/W-0 | R/W-0 | U-0 |
| INSEL1 | INSEL0 | — | HYSPOL | CMPSTAT | ALTINP | CMPPOL | — |
| bit 7 | | | | | | | bit 0 |

| | | |
|-------------------|-----------------------------|------------------------------------|
| Legend: | HC = Hardware Clearable bit | HS = Hardware Settable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 15 **CMPON:** Comparator Operating Mode bit
 1 = Comparator module is enabled
 0 = Comparator module is disabled (reduces power consumption)
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **CMPSIDL:** Comparator Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode.
 0 = Continues module operation in Idle mode
 If a device has multiple comparators, any CMPSIDL bit set to '1' disables all comparators while in Idle mode.
- bit 12-11 **HYSSEL<1:0>:** Comparator Hysteresis Select bits
 11 = 20 mV hysteresis
 10 = 10 mV hysteresis
 01 = 5 mV hysteresis
 00 = No hysteresis is selected
- bit 10 **FLTREN:** Digital Filter Enable bit
 1 = Digital filter is enabled
 0 = Digital filter is disabled
- bit 9 **FCLKSEL:** Digital Filter and Pulse Stretcher Clock Select bit
 1 = Digital filter and pulse stretcher operate with the PWM clock
 0 = Digital filter and pulse stretcher operate with the system clock
- bit 8 **Unimplemented:** Read as '0'
- bit 7-6 **INSEL<1:0>:** Input Source Select for Comparator bits
If ALTINP = 0, Select from Comparator Inputs:
 11 = Selects CMPxD input pin
 10 = Selects CMPxC input pin
 01 = Selects CMPxB input pin
 00 = Selects CMPxA input pin
If ALTINP = 1, Select from Alternate Inputs:
 11 = Reserved
 10 = Reserved
 01 = Selects PGA2 output
 00 = Selects PGA1 output
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **HYSPOL:** Comparator Hysteresis Polarity Select bit
 1 = Hysteresis is applied to the falling edge of the comparator output
 0 = Hysteresis is applied to the rising edge of the comparator output
- bit 3 **CMPSTAT:** Current State of Comparator Output Including CMPPOL Selection bit

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REGISTER 20-1: CMPxCON: COMPARATOR x CONTROL REGISTER (x = 1,2) (CONTINUED)

- bit 2 **ALTINP:** Alternate Input Select bit
 1 = INSEL<1:0> bits select alternate inputs
 0 = INSEL<1:0> bits select comparator inputs
- bit 1 **CMPPOL:** Comparator Output Polarity Control bit
 1 = Output is inverted
 0 = Output is non-inverted
- bit 0 **Unimplemented:** Read as '0'

REGISTER 20-2: CMPxDAC: COMPARATOR DACx CONTROL REGISTER (x = 1,2)

| | | | | | | | |
|--------|-----|-----|-----|-------------|-------|-------|-------|
| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | CMREF<11:8> | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CMREF<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15-12 **Unimplemented:** Read as '0'
- bit 11-0 **CMREF<11:0>:** Comparator Reference Voltage Select bits
 111111111111 = (CMREF<11:0> * (AVDD)/4096)
 •
 •
 •
 000000000000 = 0.0 volts

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21.0 PROGRAMMABLE GAIN AMPLIFIER (PGA)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Programmable Gain Amplifier (PGA)**” (DS70005146) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

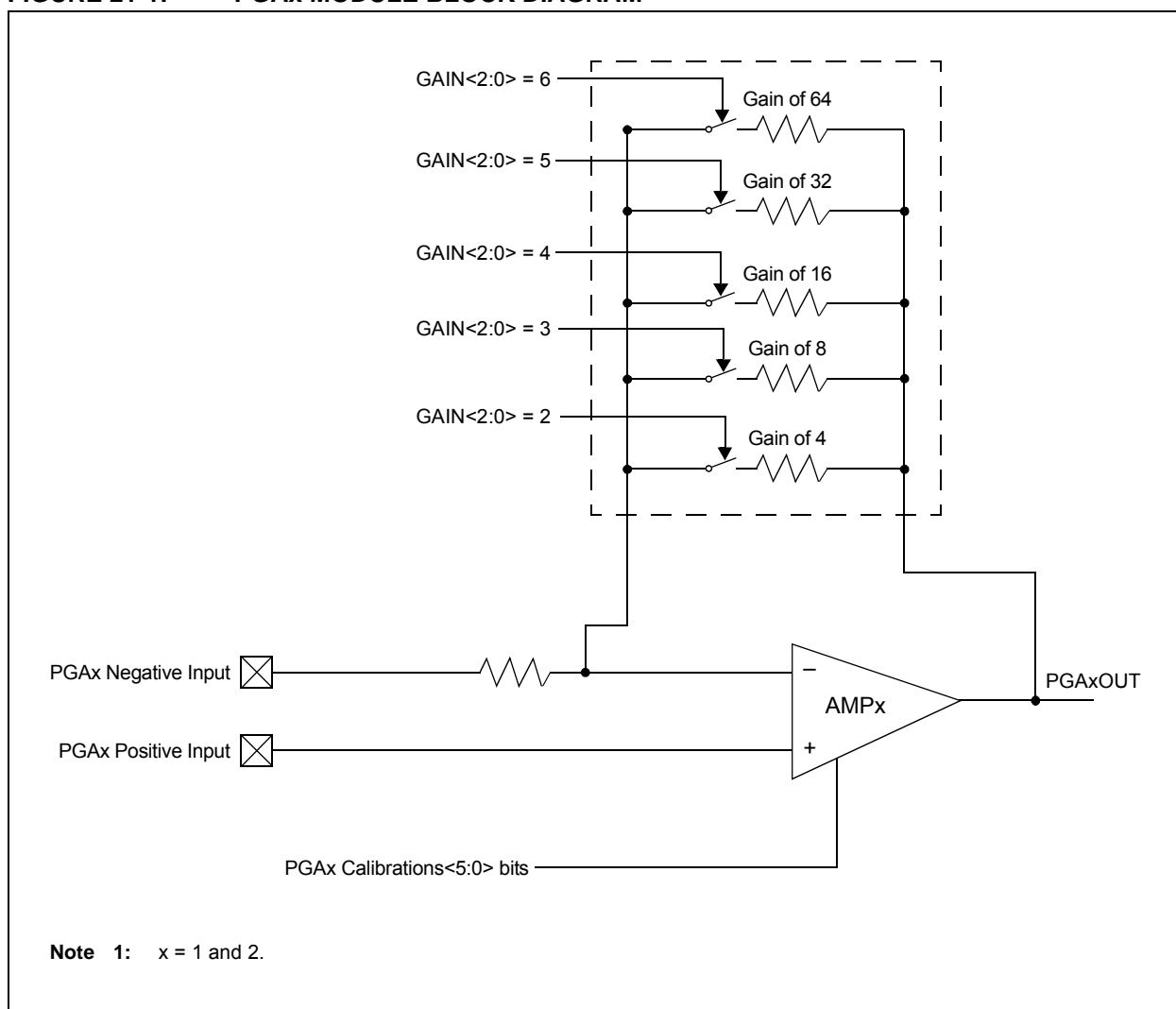
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 family devices have two Programmable Gain Amplifiers (PGA1, PGA2). The PGA is an op amp-based, non-inverting amplifier with user-programmable gains. The output of the PGA can be connected to a number of dedicated Sample-and-Hold inputs of the Analog-to-Digital Converter and/or to the high-speed analog comparator module. The PGA has five selectable gains and may be used as a ground referenced amplifier (single-ended) or used with an independent ground reference point.

Key features of the PGA module include:

- Single-Ended or Independent Ground Reference
- Selectable Gains: 4x, 8x, 16x, 32x and 64x
- High Gain Bandwidth
- Rail-to-Rail Output Voltage
- Wide Input Voltage Range

FIGURE 21-1: PGAx MODULE BLOCK DIAGRAM



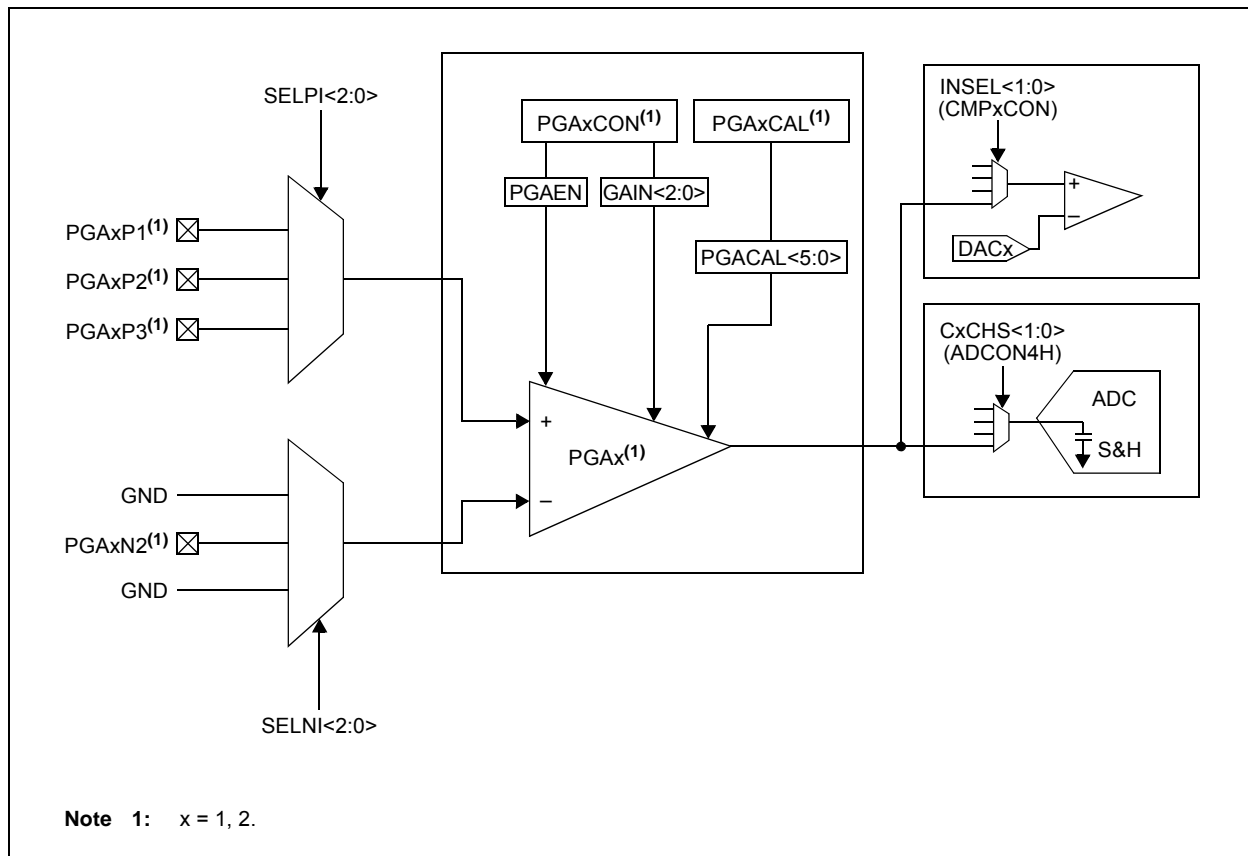
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21.1 Module Description

The programmable gain amplifiers are used to amplify small voltages (e.g., voltages across burden/shunt resistors) to improve the signal-to-noise ratio of the measured signal. The PGAx output voltage can be read by the two dedicated Sample-and-Hold circuits on the ADC module. The output voltage can also be fed to the comparator module for overcurrent/voltage protection. Figure 21-2 shows a functional block diagram of the PGAx module. Refer to Section 19.0 “High-Speed, 12-Bit Analog-to-Digital Converter (ADC)” and Section 20.0 “High-Speed Analog Comparator” for more interconnection details.

The gain of the PGAx module is selectable via the GAIN<2:0> bits in the PGAxCON register. There are five selectable gains, ranging from 4x to 64x. The SELPI<2:0> and SELNI<2:0> bits in the PGAxCON register select one of three positive/negative inputs to the PGAx module. For single-ended applications, the SELNI<2:0> bits will select ground as the negative input source. To provide an independent ground reference, the PGAxN2 pin is available as the negative input source to the PGAx module.

FIGURE 21-2: PGAx FUNCTIONAL BLOCK DIAGRAM



21.2 PGA Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page contains the latest updates and additional information.

21.2.1 KEY RESOURCES

- **“Programmable Gain Amplifier (PGA)”** (DS70005146) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

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21.3 PGA Control Registers

REGISTER 21-1: PGAxCON: PGAx CONTROL REGISTER (x = 1,2)

| | | | | | | | |
|--------|-----|--------|--------|--------|--------|--------|--------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PGAEN | — | SELPI2 | SELPI1 | SELPI0 | SELNI2 | SELNI1 | SELNI0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-------|-------|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | GAIN2 | GAIN1 | GAIN0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **PGAEN:** PGAx Enable bit
 1 = PGAx module is enabled
 0 = PGAx module is disabled (reduces power consumption)

bit 14 **Unimplemented:** Read as '0'

bit 13-11 **SELPI<2:0>:** PGAx Positive Input Selection bits
 111 = Reserved
 110 = Reserved
 101 = Reserved
 100 = Reserved
 011 = Reserved
 010 = PGAxP3
 001 = PGAxP2
 000 = PGAxP1

bit 10-8 **SELNI<2:0>:** PGAx Negative Input Selection bits
 111 = Reserved
 110 = Reserved
 101 = Reserved
 100 = Reserved
 011 = Ground (Single-Ended mode)
 010 = Reserved
 001 = PGAxN2
 000 = Ground (Single-Ended mode)

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **GAIN<2:0>:** PGAx Gain Selection bits
 111 = Reserved
 110 = Gain of 64
 101 = Gain of 32
 100 = Gain of 16
 011 = Gain of 8
 010 = Gain of 4
 001 = Reserved
 000 = Reserved

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REGISTER 21-2: PGAxCAL: PGAx CALIBRATION REGISTER (x = 1,2)

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-------------|-------|-------|-------|-------|-------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | PGACAL<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6

Unimplemented: Read as '0'

bit 5-0

PGACAL<5:0>: PGAx Offset Calibration bits

The calibration values for PGA1 and PGA2 must be copied from Flash addresses, 0x800E48 and 0x800E4C, respectively, into these bits before the module is enabled. Refer to the Device Calibration Addresses table (Table 22-3) in Section 22.0 "Special Features" for more information.

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NOTES:

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22.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXGS202 family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation
- Brown-out Reset (BOR)

22.1 Configuration Bits

In the dsPIC33EPXXGS202 family devices, the Configuration Words are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored at the end of the on-chip program memory space, known as the Flash Configuration Words. Their specific locations are shown in [Table 22-1](#) with detailed descriptions in [Table 22-2](#). The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration Shadow registers during device Resets.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Words for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled. Program code executing out of configuration space will cause a device Reset.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration Words.

TABLE 22-1: CONFIGURATION REGISTER MAP

| Name | Address | Device Memory Size (Kbytes) | Bits 23-16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|---------|-----------------------------|------------|-------------------------|--------|--------|--------------|-----------|--------|-------|-------|-------------------------|------------|-------------|---------|--------|---------------|-------------------------|-------------------------|
| FSEC | 002B80 | 16 | — | AIVTDIS | — | — | — | CSS <2:0> | | | CWRP | GSS <1:0> | | GWRP | — | BSEN | BSS <1:0> | | BWRP |
| | 005780 | 32 | — | — | — | — | BSLIM <12:0> | | | | | | | | | | | | |
| FBSLIM | 002B90 | 16 | — | — | — | — | BSLIM <12:0> | | | | | | | | | | | | |
| | 005790 | 32 | — | — | — | — | BSLIM <12:0> | | | | | | | | | | | | |
| FSIGN | 002B94 | 16 | — | Reserved ⁽²⁾ | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| | 005794 | 32 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| FOSCSSEL | 002B98 | 16 | — | — | — | — | — | — | — | — | — | IESO | — | — | — | — | FNOSC<2:0> | | |
| | 005798 | 32 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FNOSC<2:0> | | |
| FOSC | 002B9C | 16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| | 00579C | 32 | — | — | — | — | — | — | — | — | — | PLLKEN | FCKSM<1:0> | | IOL1WAY | — | — | OSCI0FNC | POSCMD<1:0> |
| FWDT | 002BA0 | 16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| | 0057A0 | 32 | — | — | — | — | — | — | — | — | — | WDTWIN<1:0> | WINDIS | WDTEN<1:0> | | WDTPRE | WDTPOST <3:0> | | |
| FPOR | 002BA4 | 16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| | 0057A4 | 32 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | Reserved ⁽¹⁾ |
| FICD | 002BA8 | 16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| | 0057A8 | 32 | — | — | — | — | — | — | — | — | — | Reserved ⁽¹⁾ | — | JTAGEN | — | — | — | — | ICS <1:0> |
| FDEVOPT | 002BAC | 16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| | 0057AC | 32 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | Reserved ⁽¹⁾ | PWMLOCK |
| FALTREG | 002BB0 | 16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| | 0057B0 | 32 | — | — | — | — | — | — | — | — | — | — | — | CTXT2 <2:0> | | — | CTXT1 <2:0> | | |

Note 1: These bits are reserved and must be programmed as '1'.
Note 2: This bit is reserved and must be programmed as '0'.

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TABLE 22-2: CONFIGURATION BITS DESCRIPTION

| Bit Field | Description |
|------------------------|---|
| BSS<1:0> | Boot Segment Code-Protect Level bits 11 = Boot Segment is not code-protected other than BWRP 10 = Standard security 0x = High security |
| BSEN | Boot Segment Control bit 1 = No Boot Segment is enabled 0 = Boot Segment size is determined by the BSLIM<12:0> bits |
| BWRP | Boot Segment Write-Protect bit 1 = Boot Segment can be written 0 = Boot Segment is write-protected |
| BSLIM<12:0> | Boot Segment Flash Page Address Limit bits Contains the last active Boot Segment page. The value to be programmed is the inverted page address, such that programming additional '0's can only increase the Boot Segment size (i.e., 0x1FFD = 2 Pages or 1024 IW). |
| GSS<1:0> | General Segment Code-Protect Level bits 11 = User program memory is not code-protected 10 = Standard security 0x = High security |
| GWRP | General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected |
| CWRP | Configuration Segment Write-Protect bit 1 = Configuration data is not write-protected 0 = Configuration data is write protected |
| CSS<2:0> | Configuration Segment Code-Protect Level bits 111 = Configuration data is not code-protected 110 = Standard security 10x = Enhanced security 0xx = High security |
| AIVTDIS ⁽¹⁾ | Alternate Interrupt Vector Table bit 1 = Alternate Interrupt Vector Table is disabled 0 = Alternate Interrupt Vector Table is enabled if INTCON2<8> = 1 |
| IESO | Two-Speed Oscillator Start-up Enable bit 1 = Starts up device with FRC, then automatically switches to the user-selected oscillator source when ready 0 = Starts up device with the user-selected oscillator source |
| PWMLOCK | PWM Lock Enable bit 1 = Certain PWM registers may only be written after a key sequence 0 = PWM registers may be written without a key sequence |

Note 1: The Boot Segment must be present to use the Alternate Interrupt Vector Table.

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TABLE 22-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

| Bit Field | Description |
|--------------|---|
| FNOSC<2:0> | Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Fast RC Oscillator with Divide-by-16 101 = Low-Power RC Oscillator (LPRC) 100 = Reserved; do not use 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC) |
| FCKSM<1:0> | Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled |
| IOL1WAY | Peripheral Pin Select Configuration bit 1 = Allows only one reconfiguration 0 = Allows multiple reconfigurations |
| OSCIOfNC | OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is a general purpose digital I/O pin |
| POSCMD<1:0> | Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode |
| WDTEN<1:0> | Watchdog Timer Enable bits 11 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled; clearing the SWDTEN bit in the RCON register will have no effect) 10 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register) 01 = Watchdog Timer is enabled only while device is active and is disabled while in Sleep mode; software control is disabled in this mode 00 = Watchdog Timer and the SWDTEN bit are disabled |
| WINDIS | Watchdog Timer Window Enable bit 1 = Watchdog Timer is in Non-Window mode 0 = Watchdog Timer is in Window mode |
| PLLKEN | PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled |
| WDTPRE | Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32 |
| WDTPOST<3:0> | Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1 |

Note 1: The Boot Segment must be present to use the Alternate Interrupt Vector Table.

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TABLE 22-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

| Bit Field | Description |
|-------------|--|
| WDTWIN<1:0> | Watchdog Timer Window Select bits 11 = WDT window is 25% of the WDT period 10 = WDT window is 37.5% of the WDT period 01 = WDT window is 50% of the WDT period 00 = WDT window is 75% of the WDT period |
| JTAGEN | JTAG Enable bit 1 = JTAG is enabled 0 = JTAG is disabled |
| ICS<1:0> | ICD Communication Channel Select bits 11 = Communicates on PGEC1 and PGED1 10 = Communicates on PGEC2 and PGED2 01 = Communicates on PGEC3 and PGED3 00 = Reserved, do not use |
| CTXT1<2:0> | Specifies Interrupt Priority Level (IPL) Associated to Alternate Working Register 1 bits 111 = Reserved 110 = Assigned to IPL of 7 101 = Assigned to IPL of 6 100 = Assigned to IPL of 5 011 = Assigned to IPL of 4 010 = Assigned to IPL of 3 001 = Assigned to IPL of 2 000 = Assigned to IPL of 1 |
| CTXT2<2:0> | Specifies Interrupt Priority Level (IPL) Associated to Alternate Working Register 2 bits 111 = Reserved 110 = Assigned to IPL of 7 101 = Assigned to IPL of 6 100 = Assigned to IPL of 5 011 = Assigned to IPL of 4 010 = Assigned to IPL of 3 001 = Assigned to IPL of 2 000 = Assigned to IPL of 1 |

Note 1: The Boot Segment must be present to use the Alternate Interrupt Vector Table.

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22.2 Device Calibration and Identification

The PGAX modules on the dsPIC33EPXXGS202 family devices require Calibration Data registers to improve performance of the module over a wide operating range. These Calibration registers are read-only and are stored in configuration memory space. Prior to enabling the module, the calibration data must be read (TBLPAG and Table Read instruction) and loaded into their respective SFR registers. The device calibration addresses are shown in [Table 22-3](#).

The dsPIC33EPXXGS202 devices have two Identification registers near the end of configuration memory space that store the Device ID (DEVID) and Device Revision (DEVREV). These registers are used to determine the mask, variant and manufacturing information about the device. These registers are read-only and are shown in [Register 22-1](#) and [Register 22-2](#).

TABLE 22-3: DEVICE CALIBRATION ADDRESSES⁽¹⁾

| Calibration Name | Address | Bits 23-16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------|---------|------------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|----------------------------|-------|-------|-------|-------|-------|
| PGA1CAL | 800E48 | — | — | — | — | — | — | — | — | — | — | — | PGA1 Calibration Data bits | | | | | |
| PGA2CAL | 800E4C | — | — | — | — | — | — | — | — | — | — | — | PGA2 Calibration Data bits | | | | | |

Note 1: The calibration data must be copied into its respective registers prior to enabling the module.

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REGISTER 22-1: DEVID: DEVICE ID REGISTER

| | | | | | | | | |
|--------------|---|---|---|---|---|---|---|--------|
| R | R | R | R | R | R | R | R | R |
| DEVID<23:16> | | | | | | | | |
| bit 23 | | | | | | | | bit 16 |

| | | | | | | | | |
|-------------|---|---|---|---|---|---|---|-------|
| R | R | R | R | R | R | R | R | R |
| DEVID<15:8> | | | | | | | | |
| bit 15 | | | | | | | | bit 8 |

| | | | | | | | | |
|------------|---|---|---|---|---|---|---|-------|
| R | R | R | R | R | R | R | R | R |
| DEVID<7:0> | | | | | | | | |
| bit 7 | | | | | | | | bit 0 |

Legend: R = Read-Only bit U = Unimplemented bit

bit 23-0 **DEVID<23:0>**: Device Identifier bits

REGISTER 22-2: DEVREV: DEVICE REVISION REGISTER

| | | | | | | | | |
|---------------|---|---|---|---|---|---|---|--------|
| R | R | R | R | R | R | R | R | R |
| DEVREV<23:16> | | | | | | | | |
| bit 23 | | | | | | | | bit 16 |

| | | | | | | | | |
|--------------|---|---|---|---|---|---|---|-------|
| R | R | R | R | R | R | R | R | R |
| DEVREV<15:8> | | | | | | | | |
| bit 15 | | | | | | | | bit 8 |

| | | | | | | | | |
|-------------|---|---|---|---|---|---|---|-------|
| R | R | R | R | R | R | R | R | R |
| DEVREV<7:0> | | | | | | | | |
| bit 7 | | | | | | | | bit 0 |

Legend: R = Read-only bit U = Unimplemented bit

bit 23-0 **DEVREV<23:0>**: Device Revision bits

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22.3 One-Time-Programmable (OTP) Memory Area

dsPIC33EPXXGS202 family devices contain thirty-two OTP areas, located at addresses, 0x800F80 through 0x800FFC. The OTP area can be used for storing product information, such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

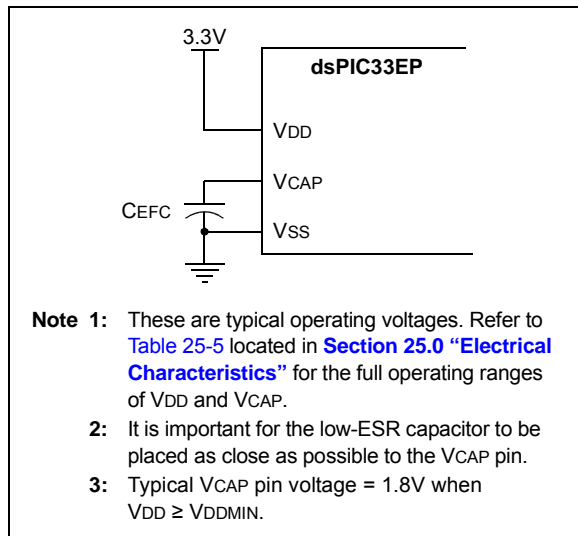
22.4 On-Chip Voltage Regulator

All the dsPIC33EPXXGS202 family devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXGS202 family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 22-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 25-5, located in Section 25.0 “Electrical Characteristics”.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

FIGURE 22-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR^(1,2,3)



22.5 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is ‘1’.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 25-23 of Section 25.0 “Electrical Characteristics” for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

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22.6 Watchdog Timer (WDT)

For dsPIC33EPXXGS202 family devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

22.6.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT Time-out Period (TWDT), as shown in Parameter SY12 in Table 25-23.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods, ranges from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC_x bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

22.6.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3:2>) needs to be cleared in software after the device wakes up.

22.6.3 ENABLING WDT

The WDT is enabled or disabled by the WDTEN<1:0> Configuration bits in the FWDT Configuration register. When the WDTEN<1:0> Configuration bits have been programmed to '0b11', the WDT is always enabled.

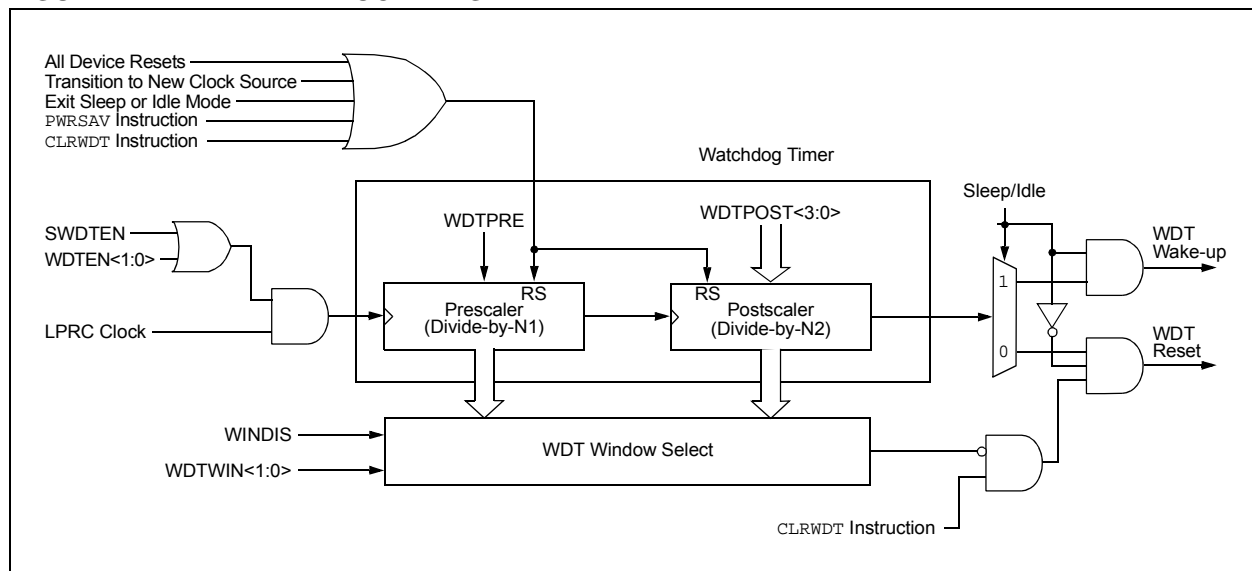
The WDT can be optionally controlled in software when the WDTEN<1:0> Configuration bits have been programmed to '0b10'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical Code Segments and disables the WDT during non-critical segments for maximum power savings.

The WDT Time-out flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

22.6.4 WDT WINDOW

The Watchdog Timer has an optional Windowed mode, enabled by programming the WINDIS bit in the WDT Configuration register (FWDT<7>). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window select bits (WDTWIN<1:0>).

FIGURE 22-2: WDT BLOCK DIAGRAM



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22.7 JTAG Interface

The dsPIC33EPXXGS202 family devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface is provided in future revisions of the document.

Note: Refer to “**Programming and Diagnostics**” (DS70608) in the “*dsPIC33/PIC24 Family Reference Manual*” for further information on usage, configuration and operation of the JTAG interface.

22.8 In-Circuit Serial Programming

The dsPIC33EPXXGS202 family devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the “*dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits*” (DS70663) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

22.9 In-Circuit Debugger

When MPLAB® ICD 3 or REAL ICE™ is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB X IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to MCLR, VDD, VSS and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins (PGECx and PGEDx).

22.10 Code Protection and CodeGuard™ Security

dsPIC33EPXXGS202 devices offer multiple levels of security for protecting individual intellectual property. The program Flash protection can be broken up into three segments: Boot Segment (BS), General Segment (GS) and Configuration Segment (CS). Boot Segment has the highest security privilege and can be thought to have limited restrictions when accessing other segments. General Segment has the least security and is intended for the end user system code. Configuration Segment contains only the device user configuration data which is located at the end of the program memory space.

The code protection features are controlled by the Configuration registers, FSEC and FBSLIM. The FSEC register controls the code-protect level for each segment and if that segment is write-protected. The size of the BS and GS will depend on the BSLIM<12:0> setting and if the Alternate Interrupt Vector Table (AIVT) is enabled. The BSLIM<12:0> bits define the number of pages for BS with each page containing 512 IW. The smallest BS size is one page, which will consist of the Interrupt Vector Table (IVT) and 256 IW of code protection.

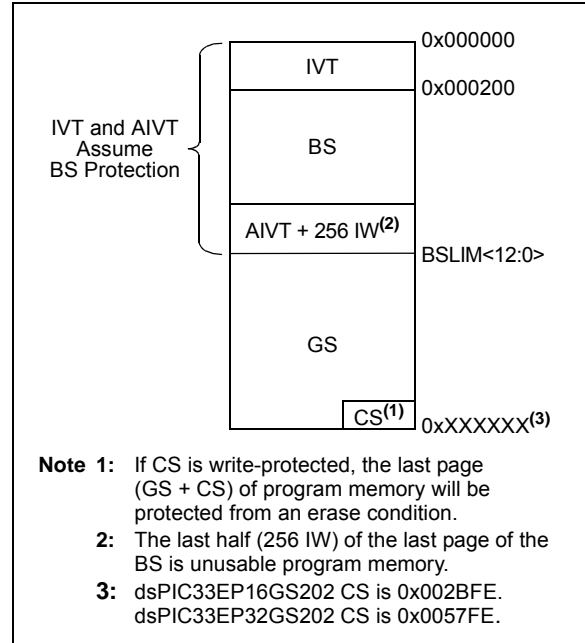
If the AIVT is enabled, the last page of BS will contain the AIVT and will not contain any BS code. With AIVT enabled, the smallest BS size is now two pages (1024 IW), with one page for the IVT and BS code, and the other page for the AIVT. Write protection of the Boot Segment does not cover the AIVT. The last page of the BS can always be programmed or erased by BS code. The General Segment will start at the next page and will consume the rest of program Flash except for the Flash Configuration Words. The IVT will assume GS security only if BS is not enabled. The IVT is protected from being programmed or page erased when either security segment has enabled write protection.

Note: Refer to “**CodeGuard™ Intermediate Security**” (DS70005182) in the “*dsPIC33/PIC24 Family Reference Manual*” for further information on usage, configuration and operation of CodeGuard Security.

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The different device security segments are shown in [Figure 22-3](#). Here, all three segments are shown but are not required. If only basic code protection is required, then the GS can be enabled independently or combined with the CS if desired.

FIGURE 22-3: dsPIC33EPXXGS202 SECURITY SEGMENTS EXAMPLE



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NOTES:

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23.0 INSTRUCTION SET SUMMARY

Note: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EP instruction set is almost identical to that of the dsPIC30F and dsPIC33F.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- DSP operations
- Control operations

Table 23-1 lists the general symbols used in describing the instructions.

The dsPIC33EP instruction set summary in Table 23-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register ‘Wb’ without any address modifier
- The second source operand, which is typically a register ‘Ws’ with or without an address modifier
- The destination of the result, which is typically a register ‘Wd’ with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value ‘f’
- The destination, which could be either the file register ‘f’ or the W0 register, which is denoted as ‘WREG’

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of ‘Ws’ or ‘f’)
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register ‘Wb’)

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by ‘k’)
- The W register or file register where the literal value is to be loaded (specified by ‘Wb’ or ‘f’)

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register ‘Wb’ without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register ‘Wd’ with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register ‘Wn’ or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

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Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSBs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed. In these

cases, the execution takes multiple instruction cycles, with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157).

TABLE 23-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

| Field | Description |
|---------------------|--|
| #text | Means literal defined by "text" |
| (text) | Means "content of text" |
| [text] | Means "the location addressed by text" |
| { } | Optional field or operation |
| $a \in \{b, c, d\}$ | a is selected from the set of values b, c, d |
| <n:m> | Register bit field |
| .b | Byte mode selection |
| .d | Double-Word mode selection |
| .S | Shadow register select |
| .w | Word mode selection (default) |
| Acc | One of two accumulators {A, B} |
| AWB | Accumulator write-back destination address register $\in \{W13, [W13]+ = 2\}$ |
| bit4 | 4-bit bit selection field (used in word addressed instructions) $\in \{0...15\}$ |
| C, DC, N, OV, Z | MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero |
| Expr | Absolute address, label or expression (resolved by the linker) |
| f | File register address $\in \{0x0000...0x1FFF\}$ |
| lit1 | 1-bit unsigned literal $\in \{0, 1\}$ |
| lit4 | 4-bit unsigned literal $\in \{0...15\}$ |
| lit5 | 5-bit unsigned literal $\in \{0...31\}$ |
| lit8 | 8-bit unsigned literal $\in \{0...255\}$ |
| lit10 | 10-bit unsigned literal $\in \{0...255\}$ for Byte mode, $\{0:1023\}$ for Word mode |
| lit14 | 14-bit unsigned literal $\in \{0...16384\}$ |
| lit16 | 16-bit unsigned literal $\in \{0...65535\}$ |
| lit23 | 23-bit unsigned literal $\in \{0...8388608\}$; LSB must be '0' |
| None | Field does not require an entry, can be blank |
| OA, OB, SA, SB | DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate |
| PC | Program Counter |
| Slit10 | 10-bit signed literal $\in \{-512...511\}$ |
| Slit16 | 16-bit signed literal $\in \{-32768...32767\}$ |
| Slit6 | 6-bit signed literal $\in \{-16...16\}$ |
| Wb | Base W register $\in \{W0...W15\}$ |
| Wd | Destination W register $\in \{Wd, [Wd], [Wd++] , [Wd--], [++Wd], [--Wd]\}$ |
| Wdo | Destination W register $\in \{Wnd, [Wnd], [Wnd++] , [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb]\}$ |
| Wm,Wn | Dividend, Divisor Working register pair (Direct Addressing) |

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TABLE 23-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

| Field | Description |
|-------|---|
| Wm*Wm | Multiplicand and Multiplier Working register pair for Square instructions $\in \{W4 * W4, W5 * W5, W6 * W6, W7 * W7\}$ |
| Wm*Wn | Multiplicand and Multiplier Working register pair for DSP instructions $\in \{W4 * W5, W4 * W6, W4 * W7, W5 * W6, W5 * W7, W6 * W7\}$ |
| Wn | One of 16 Working registers $\in \{W0...W15\}$ |
| Wnd | One of 16 Destination Working registers $\in \{W0...W15\}$ |
| Wns | One of 16 Source Working registers $\in \{W0...W15\}$ |
| WREG | W0 (Working register used in file register instructions) |
| Ws | Source W register $\in \{Ws, [Ws], [Ws++] , [Ws--], [++Ws], [--Ws] \}$ |
| Wso | Source W register $\in \{Wns, [Wns], [Wns++] , [Wns--], [++Wns], [--Wns], [Wns+Wb] \}$ |
| Wx | X Data Space Prefetch Address register for DSP instructions $\in \{[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], \text{none}\}$ |
| Wxd | X Data Space Prefetch Destination register for DSP instructions $\in \{W4...W7\}$ |
| Wy | Y Data Space Prefetch Address register for DSP instructions $\in \{[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], \text{none}\}$ |
| Wyd | Y Data Space Prefetch Destination register for DSP instructions $\in \{W4...W7\}$ |

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TABLE 23-2: INSTRUCTION SET OVERVIEW

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles | Status Flags Affected |
|--------------------|-------------------|-----------------------------|--|------------|-------------|-----------------------|
| 1 | ADD | ADD <i>Acc</i> | Add Accumulators | 1 | 1 | OA,OB,SA,SB |
| | | ADD <i>f</i> | $f = f + WREG$ | 1 | 1 | C,DC,N,OV,Z |
| | | ADD <i>f, WREG</i> | $WREG = f + WREG$ | 1 | 1 | C,DC,N,OV,Z |
| | | ADD <i>#lit10, Wn</i> | $Wd = lit10 + Wd$ | 1 | 1 | C,DC,N,OV,Z |
| | | ADD <i>Wb, Ws, Wd</i> | $Wd = Wb + Ws$ | 1 | 1 | C,DC,N,OV,Z |
| | | ADD <i>Wb, #lit5, Wd</i> | $Wd = Wb + lit5$ | 1 | 1 | C,DC,N,OV,Z |
| | | ADD <i>Wso, #slit4, Acc</i> | 16-bit Signed Add to Accumulator | 1 | 1 | OA,OB,SA,SB |
| 2 | ADDC | ADDC <i>f</i> | $f = f + WREG + (C)$ | 1 | 1 | C,DC,N,OV,Z |
| | | ADDC <i>f, WREG</i> | $WREG = f + WREG + (C)$ | 1 | 1 | C,DC,N,OV,Z |
| | | ADDC <i>#lit10, Wn</i> | $Wd = lit10 + Wd + (C)$ | 1 | 1 | C,DC,N,OV,Z |
| | | ADDC <i>Wb, Ws, Wd</i> | $Wd = Wb + Ws + (C)$ | 1 | 1 | C,DC,N,OV,Z |
| | | ADDC <i>Wb, #lit5, Wd</i> | $Wd = Wb + lit5 + (C)$ | 1 | 1 | C,DC,N,OV,Z |
| 3 | AND | AND <i>f</i> | $f = f .AND. WREG$ | 1 | 1 | N,Z |
| | | AND <i>f, WREG</i> | $WREG = f .AND. WREG$ | 1 | 1 | N,Z |
| | | AND <i>#lit10, Wn</i> | $Wd = lit10 .AND. Wd$ | 1 | 1 | N,Z |
| | | AND <i>Wb, Ws, Wd</i> | $Wd = Wb .AND. Ws$ | 1 | 1 | N,Z |
| | | AND <i>Wb, #lit5, Wd</i> | $Wd = Wb .AND. lit5$ | 1 | 1 | N,Z |
| 4 | ASR | ASR <i>f</i> | $f = \text{Arithmetic Right Shift } f$ | 1 | 1 | C,N,OV,Z |
| | | ASR <i>f, WREG</i> | $WREG = \text{Arithmetic Right Shift } f$ | 1 | 1 | C,N,OV,Z |
| | | ASR <i>Ws, Wd</i> | $Wd = \text{Arithmetic Right Shift } Ws$ | 1 | 1 | C,N,OV,Z |
| | | ASR <i>Wb, Wns, Wnd</i> | $Wnd = \text{Arithmetic Right Shift } Wb \text{ by } Wns$ | 1 | 1 | N,Z |
| | | ASR <i>Wb, #lit5, Wnd</i> | $Wnd = \text{Arithmetic Right Shift } Wb \text{ by } lit5$ | 1 | 1 | N,Z |
| 5 | BCLR | BCLR <i>f, #bit4</i> | Bit Clear <i>f</i> | 1 | 1 | None |
| | | BCLR <i>Ws, #bit4</i> | Bit Clear <i>Ws</i> | 1 | 1 | None |
| 7 | BRA | BRA <i>C, Expr</i> | Branch if Carry | 1 | 1 (4) | None |
| | | BRA <i>GE, Expr</i> | Branch if greater than or equal | 1 | 1 (4) | None |
| | | BRA <i>GEU, Expr</i> | Branch if unsigned greater than or equal | 1 | 1 (4) | None |
| | | BRA <i>GT, Expr</i> | Branch if greater than | 1 | 1 (4) | None |
| | | BRA <i>GTU, Expr</i> | Branch if unsigned greater than | 1 | 1 (4) | None |
| | | BRA <i>LE, Expr</i> | Branch if less than or equal | 1 | 1 (4) | None |
| | | BRA <i>LEU, Expr</i> | Branch if unsigned less than or equal | 1 | 1 (4) | None |
| | | BRA <i>LT, Expr</i> | Branch if less than | 1 | 1 (4) | None |
| | | BRA <i>LTU, Expr</i> | Branch if unsigned less than | 1 | 1 (4) | None |
| | | BRA <i>N, Expr</i> | Branch if Negative | 1 | 1 (4) | None |
| | | BRA <i>NC, Expr</i> | Branch if Not Carry | 1 | 1 (4) | None |
| | | BRA <i>NN, Expr</i> | Branch if Not Negative | 1 | 1 (4) | None |
| | | BRA <i>NOV, Expr</i> | Branch if Not Overflow | 1 | 1 (4) | None |
| | | BRA <i>NZ, Expr</i> | Branch if Not Zero | 1 | 1 (4) | None |
| | | BRA <i>OA, Expr</i> | Branch if Accumulator A overflow | 1 | 1 (4) | None |
| | | BRA <i>OB, Expr</i> | Branch if Accumulator B overflow | 1 | 1 (4) | None |
| | | BRA <i>OV, Expr</i> | Branch if Overflow | 1 | 1 (4) | None |
| | | BRA <i>SA, Expr</i> | Branch if Accumulator A saturated | 1 | 1 (4) | None |
| | | BRA <i>SB, Expr</i> | Branch if Accumulator B saturated | 1 | 1 (4) | None |
| | | BRA <i>Expr</i> | Branch Unconditionally | 1 | 4 | None |
| BRA <i>Z, Expr</i> | Branch if Zero | 1 | 1 (4) | None | | |
| BRA <i>Wn</i> | Computed Branch | 1 | 4 | None | | |
| 8 | BSET | BSET <i>f, #bit4</i> | Bit Set <i>f</i> | 1 | 1 | None |
| | | BSET <i>Ws, #bit4</i> | Bit Set <i>Ws</i> | 1 | 1 | None |

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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TABLE 23-2: INSTRUCTION SET OVERVIEW (CONTINUED)

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles | Status Flags Affected |
|--------------|-------------------|---------------------------|---|------------|---------------|-----------------------|
| 9 | BSW | BSW.C Ws,Wb | Write C bit to Ws<Wb> | 1 | 1 | None |
| | | BSW.Z Ws,Wb | Write Z bit to Ws<Wb> | 1 | 1 | None |
| 10 | BTG | BTG f,#bit4 | Bit Toggle f | 1 | 1 | None |
| | | BTG Ws,#bit4 | Bit Toggle Ws | 1 | 1 | None |
| 11 | BTSC | BTSC f,#bit4 | Bit Test f, Skip if Clear | 1 | 1 (2 or 3) | None |
| | | BTSC Ws,#bit4 | Bit Test Ws, Skip if Clear | 1 | 1 (2 or 3) | None |
| 12 | BTSS | BTSS f,#bit4 | Bit Test f, Skip if Set | 1 | 1 (2 or 3) | None |
| | | BTSS Ws,#bit4 | Bit Test Ws, Skip if Set | 1 | 1 (2 or 3) | None |
| 13 | BTST | BTST f,#bit4 | Bit Test f | 1 | 1 | Z |
| | | BTST.C Ws,#bit4 | Bit Test Ws to C | 1 | 1 | C |
| | | BTST.Z Ws,#bit4 | Bit Test Ws to Z | 1 | 1 | Z |
| | | BTST.C Ws,Wb | Bit Test Ws<Wb> to C | 1 | 1 | C |
| | | BTST.Z Ws,Wb | Bit Test Ws<Wb> to Z | 1 | 1 | Z |
| 14 | BTSTS | BTSTS f,#bit4 | Bit Test then Set f | 1 | 1 | Z |
| | | BTSTS.C Ws,#bit4 | Bit Test Ws to C, then Set | 1 | 1 | C |
| | | BTSTS.Z Ws,#bit4 | Bit Test Ws to Z, then Set | 1 | 1 | Z |
| 15 | CALL | CALL lit23 | Call subroutine | 2 | 4 | SFA |
| | | CALL Wn | Call indirect subroutine | 1 | 4 | SFA |
| | | CALL.L Wn | Call indirect subroutine (long address) | 1 | 4 | SFA |
| 16 | CLR | CLR f | f = 0x0000 | 1 | 1 | None |
| | | CLR WREG | WREG = 0x0000 | 1 | 1 | None |
| | | CLR Ws | Ws = 0x0000 | 1 | 1 | None |
| | | CLR Acc,Wx,Wxd,Wy,Wyd,AWB | Clear Accumulator | 1 | 1 | OA,OB,SA,SB |
| 17 | CLRWDT | CLRWDT | Clear Watchdog Timer | 1 | 1 | WDTO,SLEEP |
| 18 | COM | COM f | f = \bar{f} | 1 | 1 | N,Z |
| | | COM f,WREG | WREG = \bar{f} | 1 | 1 | N,Z |
| | | COM Ws,Wd | Wd = \overline{Ws} | 1 | 1 | N,Z |
| 19 | CP | CP f | Compare f with WREG | 1 | 1 | C,DC,N,OV,Z |
| | | CP Wb,#lit8 | Compare Wb with lit8 | 1 | 1 | C,DC,N,OV,Z |
| | | CP Wb,Ws | Compare Wb with Ws (Wb – Ws) | 1 | 1 | C,DC,N,OV,Z |
| 20 | CP0 | CP0 f | Compare f with 0x0000 | 1 | 1 | C,DC,N,OV,Z |
| | | CP0 Ws | Compare Ws with 0x0000 | 1 | 1 | C,DC,N,OV,Z |
| 21 | CPB | CPB f | Compare f with WREG, with Borrow | 1 | 1 | C,DC,N,OV,Z |
| | | CPB Wb,#lit8 | Compare Wb with lit8, with Borrow | 1 | 1 | C,DC,N,OV,Z |
| | | CPB Wb,Ws | Compare Wb with Ws, with Borrow (Wb – Ws – C) | 1 | 1 | C,DC,N,OV,Z |
| 22 | CPSEQ | CPSEQ Wb,Wn | Compare Wb with Wn, skip if = | 1 | 1 (2 or 3) | None |
| | CPBEQ | CPBEQ Wb,Wn,Expr | Compare Wb with Wn, branch if = | 1 | 1 (5) | None |
| 23 | CPSGT | CPSGT Wb,Wn | Compare Wb with Wn, skip if > | 1 | 1 (2 or 3) | None |
| | CPBGT | CPBGT Wb,Wn,Expr | Compare Wb with Wn, branch if > | 1 | 1 (5) | None |
| 24 | CPSLT | CPSLT Wb,Wn | Compare Wb with Wn, skip if < | 1 | 1 (2 or 3) | None |
| | CPBLT | CPBLT Wb,Wn,Expr | Compare Wb with Wn, branch if < | 1 | 1 (5) | None |
| 25 | CPSNE | CPSNE Wb,Wn | Compare Wb with Wn, skip if ≠ | 1 | 1 (2 or 3) | None |
| | CPBNE | CPBNE Wb,Wn,Expr | Compare Wb with Wn, branch if ≠ | 1 | 1 (5) | None |

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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TABLE 23-2: INSTRUCTION SET OVERVIEW (CONTINUED)

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles | Status Flags Affected |
|--------------|-------------------|------------------------------|---|------------|-------------|-----------------------|
| 26 | CTXTSWP | CTXTSWP #lit3 | Switch CPU register context to context defined by lit3 | 1 | 2 | None |
| | | CTXTSWP Wn | Switch CPU register context to context defined by Wn | 1 | 2 | None |
| 27 | DAW | DAW Wn | Wn = decimal adjust Wn | 1 | 1 | C |
| 28 | DEC | DEC f | $f = f - 1$ | 1 | 1 | C,DC,N,OV,Z |
| | | DEC f, WREG | WREG = $f - 1$ | 1 | 1 | C,DC,N,OV,Z |
| | | DEC Ws, Wd | $Wd = Ws - 1$ | 1 | 1 | C,DC,N,OV,Z |
| 29 | DEC2 | DEC2 f | $f = f - 2$ | 1 | 1 | C,DC,N,OV,Z |
| | | DEC2 f, WREG | WREG = $f - 2$ | 1 | 1 | C,DC,N,OV,Z |
| | | DEC2 Ws, Wd | $Wd = Ws - 2$ | 1 | 1 | C,DC,N,OV,Z |
| 30 | DISI | DISI #lit14 | Disable Interrupts for k instruction cycles | 1 | 1 | None |
| 31 | DIV | DIV.S Wm, Wn | Signed 16/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| | | DIV.SD Wm, Wn | Signed 32/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| | | DIV.U Wm, Wn | Unsigned 16/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| | | DIV.UD Wm, Wn | Unsigned 32/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| 32 | DIVF | DIVF Wm, Wn | Signed 16/16-bit Fractional Divide | 1 | 18 | N,Z,C,OV |
| 33 | DO | DO #lit15, Expr | Do code to PC + Expr, lit15 + 1 times | 2 | 2 | None |
| | | DO Wn, Expr | Do code to PC + Expr, (Wn) + 1 times | 2 | 2 | None |
| 34 | ED | ED Wm*Wm, Acc, Wx, Wy, Wxd | Euclidean Distance (no accumulate) | 1 | 1 | OA,OB,OAB,SA,SB,SAB |
| 35 | EDAC | EDAC Wm*Wm, Acc, Wx, Wy, Wxd | Euclidean Distance | 1 | 1 | OA,OB,OAB,SA,SB,SAB |
| 36 | EXCH | EXCH Wns, Wnd | Swap Wns with Wnd | 1 | 1 | None |
| 37 | FBCL | FBCL Ws, Wnd | Find Bit Change from Left (MSb) Side | 1 | 1 | C |
| 38 | FF1L | FF1L Ws, Wnd | Find First One from Left (MSb) Side | 1 | 1 | C |
| 39 | FF1R | FF1R Ws, Wnd | Find First One from Right (LSb) Side | 1 | 1 | C |
| 40 | GOTO | GOTO Expr | Go to address | 2 | 4 | None |
| | | GOTO Wn | Go to indirect | 1 | 4 | None |
| | | GOTO.L Wn | Go to indirect (long address) | 1 | 4 | None |
| 41 | INC | INC f | $f = f + 1$ | 1 | 1 | C,DC,N,OV,Z |
| | | INC f, WREG | WREG = $f + 1$ | 1 | 1 | C,DC,N,OV,Z |
| | | INC Ws, Wd | $Wd = Ws + 1$ | 1 | 1 | C,DC,N,OV,Z |
| 42 | INC2 | INC2 f | $f = f + 2$ | 1 | 1 | C,DC,N,OV,Z |
| | | INC2 f, WREG | WREG = $f + 2$ | 1 | 1 | C,DC,N,OV,Z |
| | | INC2 Ws, Wd | $Wd = Ws + 2$ | 1 | 1 | C,DC,N,OV,Z |
| 43 | IOR | IOR f | $f = f .IOR. WREG$ | 1 | 1 | N,Z |
| | | IOR f, WREG | WREG = $f .IOR. WREG$ | 1 | 1 | N,Z |
| | | IOR #lit10, Wn | $Wd = lit10 .IOR. Wd$ | 1 | 1 | N,Z |
| | | IOR Wb, Ws, Wd | $Wd = Wb .IOR. Ws$ | 1 | 1 | N,Z |
| | | IOR Wb, #lit5, Wd | $Wd = Wb .IOR. lit5$ | 1 | 1 | N,Z |
| 44 | LAC | LAC Wso, #Slit4, Acc | Load Accumulator | 1 | 1 | OA,OB,OAB,SA,SB,SAB |
| 45 | LNK | LNK #lit14 | Link Frame Pointer | 1 | 1 | SFA |
| 46 | LSR | LSR f | $f = \text{Logical Right Shift } f$ | 1 | 1 | C,N,OV,Z |
| | | LSR f, WREG | WREG = $\text{Logical Right Shift } f$ | 1 | 1 | C,N,OV,Z |
| | | LSR Ws, Wd | $Wd = \text{Logical Right Shift } Ws$ | 1 | 1 | C,N,OV,Z |
| | | LSR Wb, Wns, Wnd | $Wnd = \text{Logical Right Shift } Wb \text{ by } Wns$ | 1 | 1 | N,Z |
| | | LSR Wb, #lit5, Wnd | $Wnd = \text{Logical Right Shift } Wb \text{ by } lit5$ | 1 | 1 | N,Z |

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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TABLE 23-2: INSTRUCTION SET OVERVIEW (CONTINUED)

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles | Status Flags Affected |
|--------------|-------------------|---------------------------------------|--|------------------|-------------|-----------------------|
| 47 | MAC | MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AWB | Multiply and Accumulate | 1 | 1 | OA,OB,OAB,SA,SB,SAB |
| | | MAC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd | Square and Accumulate | 1 | 1 | OA,OB,OAB,SA,SB,SAB |
| 48 | MOV | MOV f, Wn | Move f to Wn | 1 | 1 | None |
| | | MOV f | Move f to f | 1 | 1 | None |
| | | MOV f, WREG | Move f to WREG | 1 | 1 | None |
| | | MOV #lit16, Wn | Move 16-bit literal to Wn | 1 | 1 | None |
| | | MOV.b #lit8, Wn | Move 8-bit literal to Wn | 1 | 1 | None |
| | | MOV Wn, f | Move Wn to f | 1 | 1 | None |
| | | MOV Wso, Wdo | Move Ws to Wd | 1 | 1 | None |
| | | MOV WREG, f | Move WREG to f | 1 | 1 | None |
| | | MOV.D Wns, Wd | Move Double from W(ns):W(ns + 1) to Wd | 1 | 2 | None |
| | | MOV.D Ws, Wnd | Move Double from Ws to W(nd + 1):W(nd) | 1 | 2 | None |
| 49 | MOVDPAG | MOVDPAG #lit10, DSRPAG | Move 10-bit literal to DSRPAG | 1 | 1 | None |
| | | MOVDPAG #lit8, TBLPAG | Move 8-bit literal to TBLPAG | 1 | 1 | None |
| | | MOVDPAGW Ws, DSRPAG | Move Ws<9:0> to DSRPAG | 1 | 1 | None |
| | | MOVDPAGW Ws, TBLPAG | Move Ws<7:0> to TBLPAG | 1 | 1 | None |
| 50 | MOVSAC | MOVSAC Acc, Wx, Wxd, Wy, Wyd, AWB | Prefetch and store accumulator | 1 | 1 | None |
| 51 | MPY | MPY Wm*Wn, Acc, Wx, Wxd, Wy, Wyd | Multiply Wm by Wn to Accumulator | 1 | 1 | OA,OB,OAB,SA,SB,SAB |
| | | MPY Wm*Wm, Acc, Wx, Wxd, Wy, Wyd | Square Wm to Accumulator | 1 | 1 | OA,OB,OAB,SA,SB,SAB |
| 52 | MPY.N | MPY.N Wm*Wn, Acc, Wx, Wxd, Wy, Wyd | -(Multiply Wm by Wn) to Accumulator | 1 | 1 | None |
| 53 | MSC | MSC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd, AWB | Multiply and Subtract from Accumulator | 1 | 1 | OA,OB,OAB,SA,SB,SAB |
| 54 | MUL | MUL.SS Wb, Ws, Wnd | {Wnd + 1, Wnd} = signed(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.SS Wb, Ws, Acc | Accumulator = signed(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.SU Wb, Ws, Wnd | {Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.SU Wb, Ws, Acc | Accumulator = signed(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.SU Wb, #lit5, Acc | Accumulator = signed(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.US Wb, Ws, Wnd | {Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.US Wb, Ws, Acc | Accumulator = unsigned(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.UU Wb, Ws, Wnd | {Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.UU Wb, #lit5, Acc | Accumulator = unsigned(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.UU Wb, Ws, Acc | Accumulator = unsigned(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MULW.SS Wb, Ws, Wnd | Wnd = signed(Wb) * signed(Ws) | 1 | 1 | None |
| | | MULW.SU Wb, Ws, Wnd | Wnd = signed(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MULW.US Wb, Ws, Wnd | Wnd = unsigned(Wb) * signed(Ws) | 1 | 1 | None |
| | | MULW.UU Wb, Ws, Wnd | Wnd = unsigned(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.SU Wb, #lit5, Wnd | {Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.SU Wb, #lit5, Wnd | Wnd = signed(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.UU Wb, #lit5, Wnd | {Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.UU Wb, #lit5, Wnd | Wnd = unsigned(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL | f | W3:W2 = f * WREG | 1 | 1 |

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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TABLE 23-2: INSTRUCTION SET OVERVIEW (CONTINUED)

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles | Status Flags Affected |
|--------------|-------------------|-------------------------------|---|------------|-------------|-----------------------|
| 55 | NEG | NEG <i>Acc</i> | Negate Accumulator | 1 | 1 | OA,OB,OAB,SA,SB,SAB |
| | | NEG <i>f</i> | $f = \bar{f} + 1$ | 1 | 1 | C,DC,N,OV,Z |
| | | NEG <i>f, WREG</i> | WREG = $\bar{f} + 1$ | 1 | 1 | C,DC,N,OV,Z |
| | | NEG <i>Ws, Wd</i> | $Wd = \overline{Ws} + 1$ | 1 | 1 | C,DC,N,OV,Z |
| 56 | NOP | NOP | No Operation | 1 | 1 | None |
| | | NOPR | No Operation | 1 | 1 | None |
| 57 | POP | POP <i>f</i> | Pop <i>f</i> from Top-of-Stack (TOS) | 1 | 1 | None |
| | | POP <i>Wdo</i> | Pop from Top-of-Stack (TOS) to <i>Wdo</i> | 1 | 1 | None |
| | | POP.D <i>Wnd</i> | Pop from Top-of-Stack (TOS) to <i>W(nd):W(nd + 1)</i> | 1 | 2 | None |
| | | POP.S | Pop Shadow Registers | 1 | 1 | All |
| 58 | PUSH | PUSH <i>f</i> | Push <i>f</i> to Top-of-Stack (TOS) | 1 | 1 | None |
| | | PUSH <i>Wso</i> | Push <i>Wso</i> to Top-of-Stack (TOS) | 1 | 1 | None |
| | | PUSH.D <i>Wns</i> | Push <i>W(ns):W(ns + 1)</i> to Top-of-Stack (TOS) | 1 | 2 | None |
| | | PUSH.S | Push Shadow Registers | 1 | 1 | None |
| 59 | PWRSVAV | PWRSVAV #lit1 | Go into Sleep or Idle mode | 1 | 1 | WDTO,SLEEP |
| 60 | RCALL | RCALL <i>Expr</i> | Relative Call | 1 | 4 | SFA |
| | | RCALL <i>Wn</i> | Computed Call | 1 | 4 | SFA |
| 61 | REPEAT | REPEAT #lit15 | Repeat Next Instruction lit15 + 1 times | 1 | 1 | None |
| | | REPEAT <i>Wn</i> | Repeat Next Instruction (<i>Wn</i>) + 1 times | 1 | 1 | None |
| 62 | RESET | RESET | Software device Reset | 1 | 1 | None |
| 63 | RETFIE | RETFIE | Return from interrupt | 1 | 6 (5) | SFA |
| 64 | RETLW | RETLW #lit10, <i>Wn</i> | Return with literal in <i>Wn</i> | 1 | 6 (5) | SFA |
| 65 | RETURN | RETURN | Return from Subroutine | 1 | 6 (5) | SFA |
| 66 | RLC | RLC <i>f</i> | <i>f</i> = Rotate Left through Carry <i>f</i> | 1 | 1 | C,N,Z |
| | | RLC <i>f, WREG</i> | WREG = Rotate Left through Carry <i>f</i> | 1 | 1 | C,N,Z |
| | | RLC <i>Ws, Wd</i> | <i>Wd</i> = Rotate Left through Carry <i>Ws</i> | 1 | 1 | C,N,Z |
| 67 | RLNC | RLNC <i>f</i> | <i>f</i> = Rotate Left (No Carry) <i>f</i> | 1 | 1 | N,Z |
| | | RLNC <i>f, WREG</i> | WREG = Rotate Left (No Carry) <i>f</i> | 1 | 1 | N,Z |
| | | RLNC <i>Ws, Wd</i> | <i>Wd</i> = Rotate Left (No Carry) <i>Ws</i> | 1 | 1 | N,Z |
| 68 | RRC | RRC <i>f</i> | <i>f</i> = Rotate Right through Carry <i>f</i> | 1 | 1 | C,N,Z |
| | | RRC <i>f, WREG</i> | WREG = Rotate Right through Carry <i>f</i> | 1 | 1 | C,N,Z |
| | | RRC <i>Ws, Wd</i> | <i>Wd</i> = Rotate Right through Carry <i>Ws</i> | 1 | 1 | C,N,Z |
| 69 | RRNC | RRNC <i>f</i> | <i>f</i> = Rotate Right (No Carry) <i>f</i> | 1 | 1 | N,Z |
| | | RRNC <i>f, WREG</i> | WREG = Rotate Right (No Carry) <i>f</i> | 1 | 1 | N,Z |
| | | RRNC <i>Ws, Wd</i> | <i>Wd</i> = Rotate Right (No Carry) <i>Ws</i> | 1 | 1 | N,Z |
| 70 | SAC | SAC <i>Acc, #Slit4, Wdo</i> | Store Accumulator | 1 | 1 | None |
| | | SAC.R <i>Acc, #Slit4, Wdo</i> | Store Rounded Accumulator | 1 | 1 | None |
| 71 | SE | SE <i>Ws, Wnd</i> | <i>Wnd</i> = sign-extended <i>Ws</i> | 1 | 1 | C,N,Z |
| 72 | SETM | SETM <i>f</i> | <i>f</i> = 0xFFFF | 1 | 1 | None |
| | | SETM WREG | WREG = 0xFFFF | 1 | 1 | None |
| | | SETM <i>Ws</i> | <i>Ws</i> = 0xFFFF | 1 | 1 | None |
| 73 | SFTAC | SFTAC <i>Acc, Wn</i> | Arithmetic Shift Accumulator by (<i>Wn</i>) | 1 | 1 | OA,OB,OAB,SA,SB,SAB |
| | | SFTAC <i>Acc, #Slit6</i> | Arithmetic Shift Accumulator by Slit6 | 1 | 1 | OA,OB,OAB,SA,SB,SAB |

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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TABLE 23-2: INSTRUCTION SET OVERVIEW (CONTINUED)

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles | Status Flags Affected |
|--------------|-------------------|---------------------|---------------------------------|------------|-------------|-----------------------|
| 74 | SL | SL f | f = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL f, WREG | WREG = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL Ws, Wd | Wd = Left Shift Ws | 1 | 1 | C,N,OV,Z |
| | | SL Wb, Wns, Wnd | Wnd = Left Shift Wb by Wns | 1 | 1 | N,Z |
| | | SL Wb, #lit5, Wnd | Wnd = Left Shift Wb by lit5 | 1 | 1 | N,Z |
| 75 | SUB | SUB Acc | Subtract Accumulators | 1 | 1 | OA,OB,OAB,SA,SB,SAB |
| | | SUB f | f = f – WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB f, WREG | WREG = f – WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB #lit10, Wn | Wn = Wn – lit10 | 1 | 1 | C,DC,N,OV,Z |
| | | SUB Wb, Ws, Wd | Wd = Wb – Ws | 1 | 1 | C,DC,N,OV,Z |
| | | SUB Wb, #lit5, Wd | Wd = Wb – lit5 | 1 | 1 | C,DC,N,OV,Z |
| 76 | SUBB | SUBB f | f = f – WREG – (\bar{C}) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB f, WREG | WREG = f – WREG – (\bar{C}) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB #lit10, Wn | Wn = Wn – lit10 – (\bar{C}) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB Wb, Ws, Wd | Wd = Wb – Ws – (\bar{C}) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB Wb, #lit5, Wd | Wd = Wb – lit5 – (\bar{C}) | 1 | 1 | C,DC,N,OV,Z |
| 77 | SUBR | SUBR f | f = WREG – f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR f, WREG | WREG = WREG – f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR Wb, Ws, Wd | Wd = Ws – Wb | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR Wb, #lit5, Wd | Wd = lit5 – Wb | 1 | 1 | C,DC,N,OV,Z |
| 78 | SUBBR | SUBBR f | f = WREG – f – (\bar{C}) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR f, WREG | WREG = WREG – f – (\bar{C}) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR Wb, Ws, Wd | Wd = Ws – Wb – (\bar{C}) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR Wb, #lit5, Wd | Wd = lit5 – Wb – (\bar{C}) | 1 | 1 | C,DC,N,OV,Z |
| 79 | SWAP | SWAP.b Wn | Wn = nibble swap Wn | 1 | 1 | None |
| | | SWAP Wn | Wn = byte swap Wn | 1 | 1 | None |
| 80 | TBLRDH | TBLRDH Ws, Wd | Read Prog<23:16> to Wd<7:0> | 1 | 5 | None |
| 81 | TBLRDL | TBLRDL Ws, Wd | Read Prog<15:0> to Wd | 1 | 5 | None |
| 82 | TBLWTH | TBLWTH Ws, Wd | Write Ws<7:0> to Prog<23:16> | 1 | 2 | None |
| 83 | TBLWTL | TBLWTL Ws, Wd | Write Ws to Prog<15:0> | 1 | 2 | None |
| 84 | ULNK | ULNK | Unlink Frame Pointer | 1 | 1 | SFA |
| 85 | XOR | XOR f | f = f .XOR. WREG | 1 | 1 | N,Z |
| | | XOR f, WREG | WREG = f .XOR. WREG | 1 | 1 | N,Z |
| | | XOR #lit10, Wn | Wd = lit10 .XOR. Wd | 1 | 1 | N,Z |
| | | XOR Wb, Ws, Wd | Wd = Wb .XOR. Ws | 1 | 1 | N,Z |
| | | XOR Wb, #lit5, Wd | Wd = Wb .XOR. lit5 | 1 | 1 | N,Z |
| 86 | ZE | ZE Ws, Wnd | Wnd = Zero-extend Ws | 1 | 1 | C,Z,N |

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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NOTES:

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24.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for
Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICKit™ 3
- Device Programmers
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,
Evaluation Kits and Starter Kits
- Third-party development tools

24.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

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24.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

24.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

24.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

24.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

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24.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

24.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

24.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

24.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

24.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

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24.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

24.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

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25.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the dsPIC33EPXXGS202 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXGS202 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings⁽¹⁾

| | |
|---|-----------------------|
| Ambient temperature under bias | -40°C to +125°C |
| Storage temperature | -65°C to +150°C |
| Voltage on VDD with respect to VSS | -0.3V to +4.0V |
| Voltage on any pin that is not 5V tolerant with respect to VSS ⁽³⁾ | -0.3V to (VDD + 0.3V) |
| Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V ⁽³⁾ | -0.3V to +5.5V |
| Voltage on any 5V tolerant pin with respect to VSS when VDD < 3.0V ⁽³⁾ | -0.3V to +3.6V |
| Maximum current out of VSS pin | 300 mA |
| Maximum current into VDD pin ⁽²⁾ | 300 mA |
| Maximum current sunk/sourced by any 4x I/O pin | 15 mA |
| Maximum current sunk/sourced by any 8x I/O pin | 25 mA |
| Maximum current sunk by all ports ⁽²⁾ | 200 mA |

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those, or any other conditions above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see [Table 25-2](#)).

3: See the “[Pin Diagrams](#)” section for the 5V tolerant pins.

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25.1 DC Characteristics

TABLE 25-1: OPERATING MIPS vs. VOLTAGE

| Characteristic | VDD Range (in Volts) | Temperature Range (in °C) | Maximum MIPS |
|----------------|-----------------------------|------------------------------|-------------------------|
| | | | dsPIC33EPXXGS202 Family |
| — | 3.0V to 3.6V ⁽¹⁾ | -40°C to +85°C | 70 |
| — | 3.0V to 3.6V ⁽¹⁾ | -40°C to +125°C | 60 |

Note 1: Device is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$. Analog modules (ADC, PGAs and comparators) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter [BO10](#) in [Table 25-13](#) for the minimum and maximum BOR values.

TABLE 25-2: THERMAL OPERATING CONDITIONS

| Rating | Symbol | Min. | Typ. | Max. | Unit |
|--|--------|---------------------------|------|------|------|
| Industrial Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +125 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +85 | °C |
| Extended Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +140 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +125 | °C |
| Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \sum I_{OH})$ I/O Pin Power Dissipation: $I/O = \sum (\{V_{DD} - V_{OH}\} \times I_{OH}) + \sum (V_{OL} \times I_{OL})$ | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | $(T_J - T_A)/\theta_{JA}$ | | | W |

TABLE 25-3: THERMAL PACKAGING CHARACTERISTICS

| Characteristic | Symbol | Typ. | Max. | Unit | Notes |
|--|---------------|------|------|------|-------|
| Package Thermal Resistance, 28-Pin QFN-S | θ_{JA} | 30.0 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin UQFN | θ_{JA} | 26.0 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SOIC | θ_{JA} | 69.7 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SSOP | θ_{JA} | 71.0 | — | °C/W | 1 |

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

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TABLE 25-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V ⁽¹⁾ (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------------|--------|---|--|------|------|-------|---------------|
| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
| Operating Voltage | | | | | | | |
| DC10 | VDD | Supply Voltage | 3.0 | — | 3.6 | V | |
| DC12 | VDR | RAM Data Retention Voltage⁽²⁾ | 2.0 | — | — | V | |
| DC16 | VPOR | VDD Start Voltage to Ensure Internal Power-on Reset Signal | — | — | VSS | V | |
| DC17 | SVDD | VDD Rise Rate to Ensure Internal Power-on Reset Signal | 1.0 | — | — | V/ms | 0V-3V in 3 ms |

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, PGAs and comparators) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter [BO10](#) in [Table 25-13](#) for the minimum and maximum BOR values.

2: This is the limit to which VDD may be lowered without losing RAM data.

TABLE 25-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

| Standard Operating Conditions (unless otherwise stated): Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | | | | |
|---|--------|---|------|------|------|-------|--|
| Param No. | Symbol | Characteristics | Min. | Typ. | Max. | Units | Comments |
| | CEFC | External Filter Capacitor Value ⁽¹⁾ | 4.7 | 10 | — | μF | Capacitor must have a low series resistance (<1 Ohm) |

Note 1: Typical VCAP Voltage = 1.8V when VDD ≥ VDDMIN.

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TABLE 25-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | |
|--|------|------|---|------------|------|---------|
| Parameter No. | Typ. | Max. | Units | Conditions | | |
| Operating Current (IDD)⁽¹⁾ | | | | | | |
| DC20d | 5 | 10 | mA | -40°C | 3.3V | 10 MIPS |
| DC20a | 5 | 10 | mA | +25°C | | |
| DC20b | 5 | 10 | mA | +85°C | | |
| DC20c | 5 | 10 | mA | +125°C | | |
| DC22d | 10 | 15 | mA | -40°C | 3.3V | 20 MIPS |
| DC22a | 10 | 15 | mA | +25°C | | |
| DC22b | 10 | 15 | mA | +85°C | | |
| DC22c | 10 | 15 | mA | +125°C | | |
| DC24d | 15 | 20 | mA | -40°C | 3.3V | 40 MIPS |
| DC24a | 15 | 20 | mA | +25°C | | |
| DC24b | 15 | 20 | mA | +85°C | | |
| DC24c | 15 | 20 | mA | +125°C | | |
| DC25d | 20 | 28 | mA | -40°C | 3.3V | 60 MIPS |
| DC25a | 20 | 28 | mA | +25°C | | |
| DC25b | 20 | 28 | mA | +85°C | | |
| DC25c | 20 | 28 | mA | +125°C | | |
| DC26d | 30 | 35 | mA | -40°C | 3.3V | 70 MIPS |
| DC26a | 30 | 35 | mA | +25°C | | |
| DC26b | 30 | 35 | mA | +85°C | | |

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing:


```
while(1)
{
  NOP();
}
```
- JTAG is disabled

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TABLE 25-7: DC CHARACTERISTICS: IDLE CURRENT (IDLE)

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | |
|--|------|------|---|------------|------|---------|
| Parameter No. | Typ. | Max. | Units | Conditions | | |
| Idle Current (IDLE)⁽¹⁾ | | | | | | |
| DC40d | 1 | 3 | mA | -40°C | 3.3V | 10 MIPS |
| DC40a | 1 | 3 | mA | +25°C | | |
| DC40b | 1 | 3 | mA | +85°C | | |
| DC40c | 1 | 3 | mA | +125°C | | |
| DC42d | 3 | 5 | mA | -40°C | 3.3V | 20 MIPS |
| DC42a | 3 | 5 | mA | +25°C | | |
| DC42b | 3 | 5 | mA | +85°C | | |
| DC42c | 3 | 5 | mA | +125°C | | |
| DC44d | 5 | 7 | mA | -40°C | 3.3V | 40 MIPS |
| DC44a | 5 | 7 | mA | +25°C | | |
| DC44b | 5 | 7 | mA | +85°C | | |
| DC44c | 5 | 7 | mA | +125°C | | |
| DC45d | 7 | 9 | mA | -40°C | 3.3V | 60 MIPS |
| DC45a | 7 | 9 | mA | +25°C | | |
| DC45b | 7 | 9 | mA | +85°C | | |
| DC45c | 7 | 9 | mA | +125°C | | |
| DC46d | 9 | 12 | mA | -40°C | 3.3V | 70 MIPS |
| DC46a | 9 | 12 | mA | +25°C | | |
| DC46b | 9 | 12 | mA | +85°C | | |

Note 1: Base Idle current (IDLE) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- $\overline{\text{MCLR}} = V_{\text{DD}}$, WDT and FSCM are disabled
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

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TABLE 25-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | |
|---|------|------|---|------------|
| Parameter No. | Typ. | Max. | Units | Conditions |
| Power-Down Current (IPD)⁽¹⁾ | | | | |
| DC60d | 10 | 30 | μA | -40°C |
| DC60a | 16 | 60 | μA | +25°C |
| DC60b | 60 | 300 | μA | +85°C |
| DC60c | 300 | 800 | μA | +125°C |

Note 1: IPD (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as output and driving low.
- $\overline{MCLR} = V_{DD}$, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all set)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

TABLE 25-9: DC CHARACTERISTICS: WATCHDOG TIMER DELTA CURRENT (ΔI_{WDT})⁽¹⁾

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | |
|--------------------|------|------|---|------------|
| Parameter No. | Typ. | Max. | Units | Conditions |
| DC61d | 1 | 2 | μA | -40°C |
| DC61a | 1 | 2 | μA | +25°C |
| DC61b | 1 | 3 | μA | +85°C |
| DC61c | 2 | 5 | μA | +125°C |

Note 1: The ΔI_{WDT} current is the additional current consumed when the module is enabled. This current should be added to the base IPD current. All parameters are characterized but not tested during manufacturing.

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TABLE 25-10: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|------|------|---|-------|------------|------|----------------|
| Parameter No. | Typ. | Max. | Doze Ratio | Units | Conditions | | |
| Doze Current (IDOZE)⁽¹⁾ | | | | | | | |
| DC73a ⁽²⁾ | 15 | 20 | 1:2 | mA | -40°C | 3.3V | Fosc = 140 MHz |
| DC73g | 7 | 9 | 1:128 | mA | | | |
| DC70a ⁽²⁾ | 15 | 20 | 1:2 | mA | +25°C | 3.3V | Fosc = 140 MHz |
| DC70g | 7 | 9 | 1:128 | mA | | | |
| DC71a ⁽²⁾ | 15 | 20 | 1:2 | mA | +85°C | 3.3V | Fosc = 140 MHz |
| DC71g | 7 | 9 | 1:128 | mA | | | |
| DC72a ⁽²⁾ | 15 | 20 | 1:2 | mA | +125°C | 3.3V | Fosc = 120 MHz |
| DC72g | 7 | 9 | 1:128 | mA | | | |

Note 1: IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- $\overline{\text{MCLR}} = \text{VDD}$, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing:


```
while(1)
{
    NOP();
}
```
- JTAG is disabled

2: These parameters are characterized but not tested in manufacturing.

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TABLE 25-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|----------------------|-----------------|--|---|---------------------|---------------------|-------|--|
| Param No. | Symbol | Characteristic | Min. | Typ. ⁽¹⁾ | Max. | Units | Conditions |
| DI10 DI18 DI19 | V _{IL} | Input Low Voltage | | | | | |
| | | Any I/O Pin and MCLR | V _{SS} | — | 0.2 V _{DD} | V | |
| | | I/O Pins with SDA1, SCL1 | V _{SS} | — | 0.3 V _{DD} | V | SMBus disabled |
| | | I/O Pins with SDA1, SCL1 | V _{SS} | — | 0.8 | V | SMBus enabled |
| DI20 | V _{IH} | Input High Voltage | | | | | |
| | | I/O Pins Not 5V Tolerant ⁽⁴⁾ | 0.8 V _{DD} | — | V _{DD} | V | |
| | | I/O Pins 5V Tolerant and MCLR ⁽⁴⁾ | 0.8 V _{DD} | — | 5.5 | V | |
| | | 5V Tolerant I/O Pins with SDA1, SCL1 ⁽⁴⁾ | 0.8 V _{DD} | — | 5.5 | V | SMBus disabled |
| | | 5V I/O Pins with SDA1, SCL1 ⁽⁴⁾ | 2.1 | — | 5.5 | V | SMBus enabled |
| | | I/O Pins with SDA1, SCL1 Not 5V Tolerant ⁽⁴⁾ | 0.8 V _{DD} | — | V _{DD} | V | SMBus disabled |
| | | I/O Pins with SDA1, SCL1 Not 5V Tolerant ⁽⁴⁾ | 2.1 | — | V _{DD} | V | SMBus enabled |
| DI30 | ICNPU | Input Change Notification Pull-up Current | 50 | 250 | 600 | μA | V _{DD} = 3.3V, V _{PIN} = V _{SS} |
| DI31 | ICNPD | Input Change Notification Pull-Down Current⁽⁵⁾ | — | 50 | — | μA | V _{DD} = 3.3V, V _{PIN} = V _{DD} |

- Note 1:** Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.
- Note 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- Note 3:** Negative current is defined as current sourced by the pin.
- Note 4:** See the “Pin Diagrams” section for the 5V tolerant I/O pins.
- Note 5:** V_{IL} Source < (V_{SS} – 0.3). Characterized but not tested.
- Note 6:** V_{IH} source > (V_{DD} + 0.3) for non-5V tolerant pins only.
- Note 7:** Digital 5V tolerant pins do not have an internal high side diode to V_{DD}, and therefore, cannot tolerate any “positive” input injection current.
- Note 8:** |Injection Currents| > 0 can affect the ADC results by approximately 4-6 counts.
- Note 9:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted, provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

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TABLE 25-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|--------------------|-----------------|---|---|---------------------|------|-------|--|
| Param No. | Symbol | Characteristic | Min. | Typ. ⁽¹⁾ | Max. | Units | Conditions |
| DI50 | I _{IL} | Input Leakage Current^(2,3) I/O Pins 5V Tolerant ⁽⁴⁾ | -1 | — | +1 | μA | V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at high-impedance |
| DI51 | | I/O Pins Not 5V Tolerant ⁽⁴⁾ | -1 | — | +1 | μA | V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at high-impedance, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ |
| DI51a | | I/O Pins Not 5V Tolerant ⁽⁴⁾ | -1 | — | +1 | μA | Analog pins shared with external reference pins, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ |
| DI51b | | I/O Pins Not 5V Tolerant ⁽⁴⁾ | -1 | — | +1 | μA | V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at high-impedance, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ |
| DI51c | | I/O Pins Not 5V Tolerant ⁽⁴⁾ | -1 | — | +1 | μA | Analog pins shared with external reference pins, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ |
| DI55 | | $\overline{\text{MCLR}}$ | -5 | — | +5 | μA | V _{SS} ≤ V _{PIN} ≤ V _{DD} |
| DI56 | | OSC1 | -5 | — | +5 | μA | V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT and HS modes |

- Note 1:** Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.
- 2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** See the “[Pin Diagrams](#)” section for the 5V tolerant I/O pins.
- 5:** V_{IL} Source < (V_{SS} – 0.3). Characterized but not tested.
- 6:** V_{IH} source > (V_{DD} + 0.3) for non-5V tolerant pins only.
- 7:** Digital 5V tolerant pins do not have an internal high side diode to V_{DD}, and therefore, cannot tolerate any “positive” input injection current.
- 8:** |Injection Currents| > 0 can affect the ADC results by approximately 4-6 counts.
- 9:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted, provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

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TABLE 25-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|--------------------|------------------|--|---|---------------------|-----------------------|-------|---|
| Param No. | Symbol | Characteristic | Min. | Typ. ⁽¹⁾ | Max. | Units | Conditions |
| DI60a | I _{ICL} | Input Low Injection Current | 0 | — | -5 ^(5,8) | mA | All pins except V _{DD} , V _{SS} , AV _{DD} , AV _{SS} , M _{CLR} , V _{CAP} and RB7 |
| DI60b | I _{ICH} | Input High Injection Current | 0 | — | +5 ^(6,7,8) | mA | All pins except V _{DD} , V _{SS} , AV _{DD} , AV _{SS} , M _{CLR} , V _{CAP} , RB7 and all 5V tolerant pins ⁽⁷⁾ |
| DI60c | ΣI_{ICT} | Total Input Injection Current (sum of all I/O and control pins) | -20 ⁽⁷⁾ | — | +20 ⁽⁷⁾ | mA | Absolute instantaneous sum of all \pm input injection currents from all I/O pins ($ I_{ICL} + I_{ICH} $) $\leq \Sigma I_{ICT}$ |

- Note 1:** Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.
- 2:** The leakage current on the M_{CLR} pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** See the “[Pin Diagrams](#)” section for the 5V tolerant I/O pins.
- 5:** V_{IL} Source < (V_{SS} – 0.3). Characterized but not tested.
- 6:** V_{IH} source > (V_{DD} + 0.3) for non-5V tolerant pins only.
- 7:** Digital 5V tolerant pins do not have an internal high side diode to V_{DD}, and therefore, cannot tolerate any “positive” input injection current.
- 8:** |Injection Currents| > 0 can affect the ADC results by approximately 4-6 counts.
- 9:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted, provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

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TABLE 25-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------|--------|--|---|------|------|-------|--|
| Param. | Symbol | Characteristic | Min. ⁽¹⁾ | Typ. | Max. | Units | Conditions |
| DO10 | VOL | Output Low Voltage 4x Sink Driver Pins ⁽²⁾ | — | — | 0.4 | V | VDD = 3.3V, IOL ≤ 6 mA, -40°C ≤ TA ≤ +85°C, IOL ≤ 5 mA, +85°C < TA ≤ +125°C |
| | | Output Low Voltage 8x Sink Driver Pins ⁽³⁾ | — | — | 0.4 | V | VDD = 3.3V, IOL ≤ 12 mA, -40°C ≤ TA ≤ +85°C, IOL ≤ 8 mA, +85°C < TA ≤ +125°C |
| DO20 | VOH | Output High Voltage 4x Source Driver Pins ⁽²⁾ | 2.4 | — | — | V | IOH ≥ -10 mA, VDD = 3.3V |
| | | Output High Voltage 8x Source Driver Pins ⁽³⁾ | 2.4 | — | — | V | IOH ≥ -15 mA, VDD = 3.3V |
| DO20A | VOH1 | Output High Voltage 4x Source Driver Pins ⁽²⁾ | 1.5 | — | — | V | IOH ≥ -14 mA, VDD = 3.3V |
| | | | 2.0 | — | — | V | IOH ≥ -12 mA, VDD = 3.3V |
| | | | 3.0 | — | — | V | IOH ≥ -7 mA, VDD = 3.3V |
| | | Output High Voltage 8x Source Driver Pins ⁽³⁾ | 1.5 | — | — | V | IOH ≥ -22 mA, VDD = 3.3V |
| | | | 2.0 | — | — | V | IOH ≥ -18 mA, VDD = 3.3V |
| | | | 3.0 | — | — | V | IOH ≥ -10 mA, VDD = 3.3V |

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: 4x Drive Pins – RA<1:0>, RB1, RB<10:9>.

3: 8x Drive Pins – MCLR, RA<4:2>, RB0, RB<8:2>, RB<15:11>.

TABLE 25-13: ELECTRICAL CHARACTERISTICS: BOR

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------|--------|--|--|------|------|-------|------------------|
| Param No. | Symbol | Characteristic | Min. ⁽²⁾ | Typ. | Max. | Units | Conditions |
| BO10 | VBOR | BOR Event on VDD Transition High-to-Low | 2.65 | — | 2.95 | V | VDD (Notes 2, 3) |

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, PGAs and comparators) may have degraded performance.

2: Parameters are for design guidance only and are not tested in manufacturing.

3: The VBOR specification is relative to VDD.

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TABLE 25-14: DC CHARACTERISTICS: PROGRAM MEMORY

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|-----------------------------|--------|--|---|---------------------|------|-------|--|
| Param No. | Symbol | Characteristic | Min. | Typ. ⁽¹⁾ | Max. | Units | Conditions |
| Program Flash Memory | | | | | | | |
| D130 | EP | Cell Endurance | 10,000 | — | — | E/W | -40°C to +125°C |
| D131 | VPR | VDD for Read | 3.0 | — | 3.6 | V | |
| D132b | VPEW | VDD for Self-Timed Write | 3.0 | — | 3.6 | V | |
| D134 | TRETD | Characteristic Retention | 20 | — | — | Year | Provided no other specifications are violated, -40°C to +125°C |
| D135 | IDDP | Supply Current during Programming ⁽²⁾ | — | 10 | — | mA | |
| D136 | IPEAK | Instantaneous Peak Current During Start-up | — | — | 150 | mA | |
| D137a | TPE | Page Erase Time | 19.7 | — | 20.1 | ms | TPE = 146893 FRC Cycles, TA = +85°C (Note 3) |
| D137b | TPE | Page Erase Time | 19.5 | — | 20.3 | ms | TPE = 146893 FRC Cycles, TA = +125°C (Note 3) |
| D138a | TWW | Word Write Cycle Time | 46.5 | — | 47.3 | μs | TWW = 346 FRC Cycles, TA = +85°C (Note 3) |
| D138b | TWW | Word Write Cycle Time | 46.0 | — | 47.9 | μs | TWW = 346 FRC Cycles, TA = +125°C (Note 3) |
| D139a | TRW | Row Write Time | 667 | — | 679 | μs | TRW = 4965 FRC Cycles, TA = +85°C (Note 3) |
| D139b | TRW | Row Write Time | 660 | — | 687 | μs | TRW = 4965 FRC Cycles, TA = +125°C (Note 3) |

Note 1: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

2: Parameters are for design guidance only and are not tested in manufacturing.

3: Other conditions: FRC = 7.37 MHz, TUN<5:0> = 011111 (for Min.), TUN<5:0> = 100000 (for Max.). This parameter depends on the FRC accuracy (see [Table 25-20](#)) and the value of the FRC Oscillator Tuning register (see [Register 8-4](#)). For complete details on calculating the Minimum and Maximum time, see [Section 5.3 “Programming Operations”](#).

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25.2 AC Characteristics and Timing Parameters

This section defines the dsPIC33EPXXGS202 family AC characteristics and timing parameters.

TABLE 25-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

| | |
|---------------------------|---|
| AC CHARACTERISTICS | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) |
| | Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Operating voltage V_{DD} range as described in Section 25.1 “DC Characteristics” . |

FIGURE 25-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

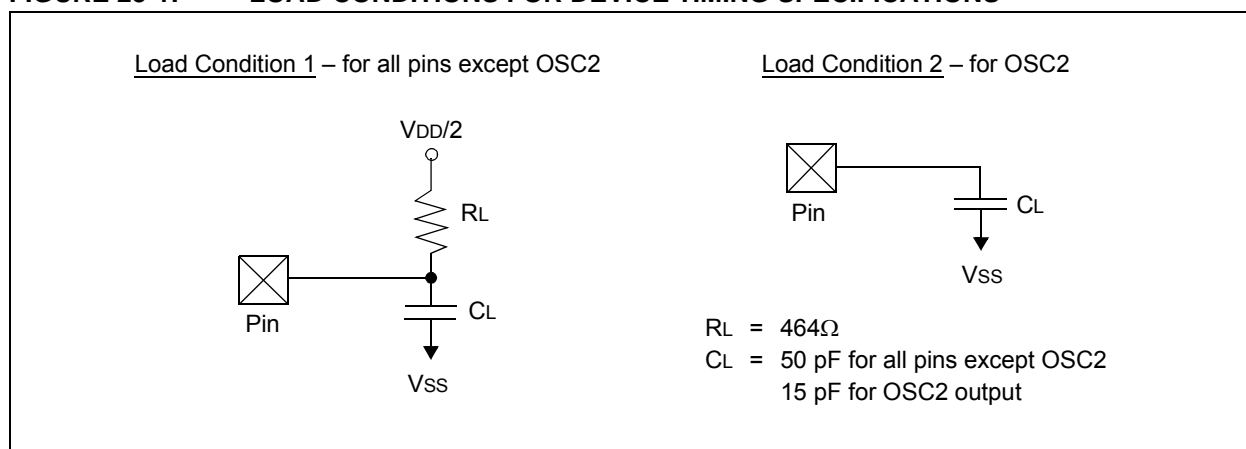


TABLE 25-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
|-----------|--------|-----------------------|------|------|------|-------|---|
| DO50 | Cosco | OSC2 Pin | — | — | 15 | pF | In XT and HS modes, when external clock is used to drive OSC1 |
| DO56 | Cio | All I/O Pins and OSC2 | — | — | 50 | pF | EC mode |
| DO58 | Cb | SCL1, SDA1 | — | — | 400 | pF | In I ² C mode |

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FIGURE 25-2: EXTERNAL CLOCK TIMING

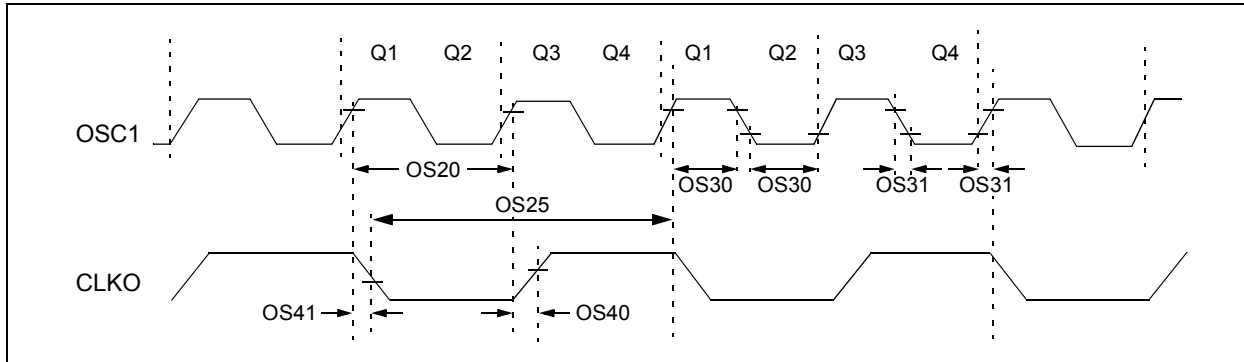


TABLE 25-17: EXTERNAL CLOCK TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------|---------------|---|---|---------------------|-------------|------------|-------------------------------|
| Param No. | Symb | Characteristic | Min. | Typ. ⁽¹⁾ | Max. | Units | Conditions |
| OS10 | FIN | External CLKI Frequency (External clocks allowed only in EC and ECPLL modes) | DC | — | 60 | MHz | EC |
| | | Oscillator Crystal Frequency | 3.5 10 | — — | 10 40 | MHz MHz | XT HS |
| OS20 | Tosc | Tosc = 1/Fosc | 8.33 | — | DC | ns | +125°C |
| | | Tosc = 1/Fosc | 7.14 | — | DC | ns | +85°C |
| OS25 | Tcy | Instruction Cycle Time ⁽²⁾ | 16.67 | — | DC | ns | +125°C |
| | | Instruction Cycle Time ⁽²⁾ | 14.28 | — | DC | ns | +85°C |
| OS30 | TosL, TosH | External Clock in (OSC1) High or Low Time | 0.45 x Tosc | — | 0.55 x Tosc | ns | EC |
| OS31 | TosR, TosF | External Clock in (OSC1) Rise or Fall Time | — | — | 20 | ns | EC |
| OS40 | TckR | CLKO Rise Time ^(3,4) | — | 5.2 | — | ns | |
| OS41 | TckF | CLKO Fall Time ^(3,4) | — | 5.2 | — | ns | |
| OS42 | GM | External Oscillator Transconductance ⁽⁴⁾ | — | 12 | — | mA/V | HS, VDD = 3.3V, TA = +25°C |
| | | | — | 6 | — | mA/V | XT, VDD = 3.3V, TA = +25°C |

Note 1: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

2: Instruction cycle period (Tcy) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Minimum” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “Maximum” cycle time limit is “DC” (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

4: Parameters are for design guidance only and are not tested in manufacturing.

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TABLE 25-18: PLL CLOCK TIMING SPECIFICATIONS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------|--------|---|---|---------------------|------|-------|--------------------|
| Param No. | Symbol | Characteristic | Min. | Typ. ⁽¹⁾ | Max. | Units | Conditions |
| OS50 | FPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range | 0.8 | — | 8.0 | MHz | ECPLL, XTPLL modes |
| OS51 | FVCO | On-Chip VCO System Frequency | 120 | — | 340 | MHz | |
| OS52 | TLOCK | PLL Start-up Time (Lock Time) | 0.9 | 1.5 | 3.1 | ms | |
| OS53 | DCLK | CLKO Stability (Jitter) ⁽²⁾ | -3 | 0.5 | 3 | % | |

Note 1: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested in manufacturing.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases, or communication clocks used by the application, use the following formula:

$$Effective\ Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Time\ Base\ or\ Communication\ Clock}}}$$

For example, if Fosc = 120 MHz and the SPI1 Bit Rate = 10 MHz, the effective jitter is as follows:

$$Effective\ Jitter = \frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

TABLE 25-19: AUXILIARY PLL CLOCK TIMING SPECIFICATIONS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------|--------|--|---|---------------------|-----|-------|------------|
| Param No. | Symbol | Characteristic | Min | Typ. ⁽¹⁾ | Max | Units | Conditions |
| OS56 | FHPOUT | On-Chip 16x PLL CCO Frequency | 112 | 118 | 120 | MHz | |
| OS57 | FHPIN | On-Chip 16x PLL Phase Detector Input Frequency | 7.0 | 7.37 | 7.5 | MHz | |
| OS58 | Tsu | Frequency Generator Lock Time | — | — | 10 | μs | |

Note 1: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested in manufacturing.

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TABLE 25-20: INTERNAL FRC ACCURACY

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|----------------|--|------|------|-------|---------------------|----------------|
| Param No. | Characteristic | Min. | Typ. | Max. | Units | Conditions | |
| Internal FRC Accuracy @ FRC Frequency = 7.37 MHz^(1,2) | | | | | | | |
| F20a | FRC | -2 | 0.5 | +2 | % | -40°C ≤ TA ≤ -10°C | VDD = 3.0-3.6V |
| | | -0.9 | 0.5 | +0.9 | % | -10°C ≤ TA ≤ +85°C | VDD = 3.0-3.6V |
| F20b | FRC | -2 | 1 | +2 | % | +85°C ≤ TA ≤ +125°C | VDD = 3.0-3.6V |

Note 1: Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

Note 2: Over the lifetime of the 28-Lead 4x4 UQFN package device, the internal FRC accuracy could vary between ±4%.

TABLE 25-21: INTERNAL LPRC ACCURACY

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | | |
|--|----------------|--|------|------|-------|---------------------|----------------|
| Param No. | Characteristic | Min. | Typ. | Max. | Units | Conditions | |
| LPRC @ 32.768 kHz⁽¹⁾ | | | | | | | |
| F21a | LPRC | -30 | — | +30 | % | -40°C ≤ TA ≤ -10°C | VDD = 3.0-3.6V |
| | | -20 | — | +20 | % | -10°C ≤ TA ≤ +85°C | VDD = 3.0-3.6V |
| F21b | LPRC | -30 | — | +30 | % | +85°C ≤ TA ≤ +125°C | VDD = 3.0-3.6V |

Note 1: This is the change of the LPRC frequency as VDD changes.

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FIGURE 25-3: I/O TIMING CHARACTERISTICS

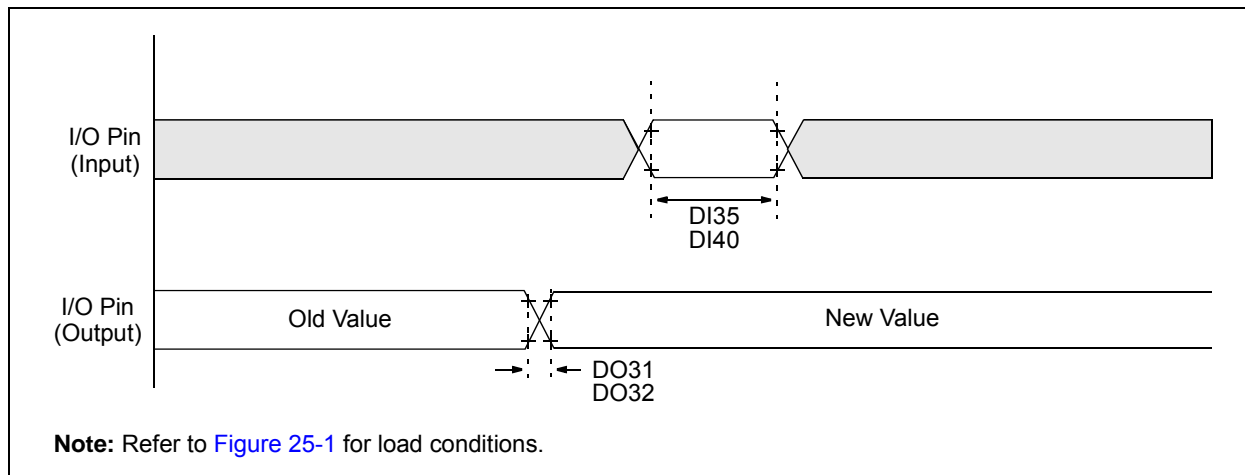
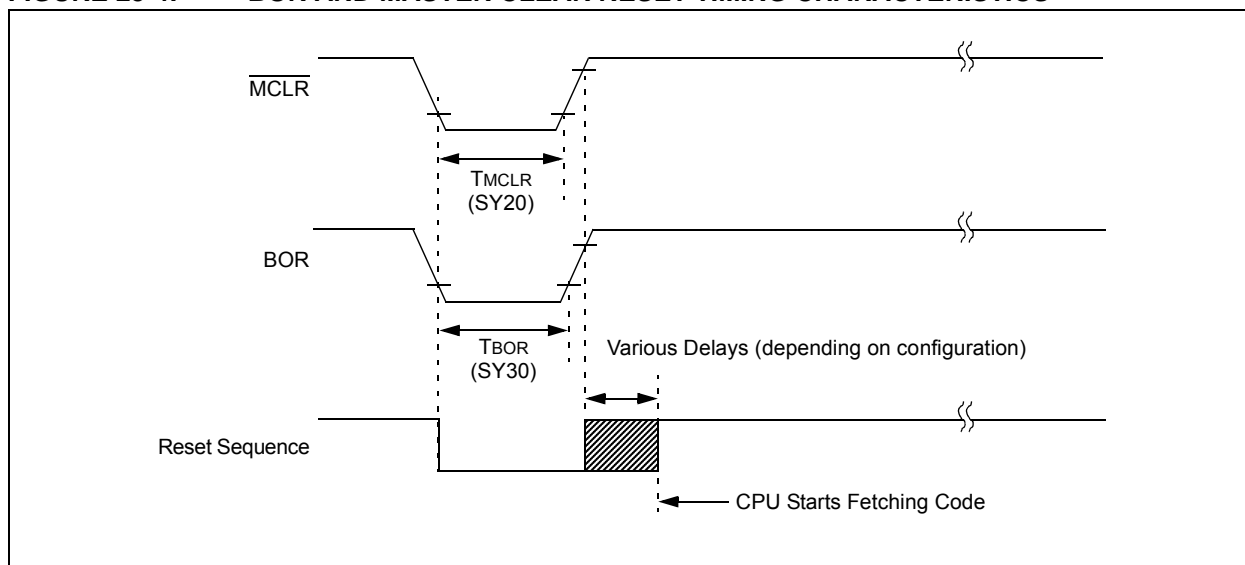


TABLE 25-22: I/O TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | |
|--------------------|--------|-----------------------------------|------|---|------|-------|------------|
| Param No. | Symbol | Characteristic | Min. | Typ. ⁽¹⁾ | Max. | Units | Conditions |
| DO31 | TioR | Port Output Rise Time | — | 5 | 10 | ns | |
| DO32 | TioF | Port Output Fall Time | — | 5 | 10 | ns | |
| DI35 | TINP | INTx Pin High or Low Time (input) | 20 | — | — | ns | |
| DI40 | TRBP | CNx High or Low Time (input) | 2 | — | — | Tcy | |

Note 1: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

FIGURE 25-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS



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TABLE 25-23: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|--------------------|-----------|--|---|---------------------|------|---------------|--|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units | Conditions |
| SY00 | TPU | Power-up Period | — | 400 | 600 | μs | |
| SY10 | TOST | Oscillator Start-up Time | — | 1024 TOSC | — | — | TOSC = OSC1 Period |
| SY12 | TWDT | Watchdog Timer Time-out Period | 0.81 | — | 1.22 | ms | WDTPRE = 0, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21a/F21b (see Table 25-21) at +85°C |
| | | | 3.25 | — | 4.88 | ms | WDTPRE = 1, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21a/F21b (see Table 25-21) at +85°C |
| SY13 | TIOZ | I/O High-Impedance from MCLR Low or Watchdog Timer Reset | 0.68 | 0.72 | 1.2 | μs | |
| SY20 | TMCLR | MCLR Pulse Width (low) | 2 | — | — | μs | |
| SY30 | TBOR | BOR Pulse Width (low) | 1 | — | — | μs | |
| SY35 | TFSCM | Fail-Safe Clock Monitor Delay | — | 500 | 900 | μs | -40°C to $+85^{\circ}\text{C}$ |
| SY36 | TVREG | Voltage Regulator Standby-to-Active mode Transition Time | — | — | 30 | μs | |
| SY37 | TOSCDFRC | FRC Oscillator Start-up Delay | — | — | 29 | μs | |
| SY38 | TOSCDLPRC | LPRC Oscillator Start-up Delay | — | — | 70 | μs | |

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

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FIGURE 25-5: TIMER1-TIMER3 EXTERNAL CLOCK TIMING CHARACTERISTICS

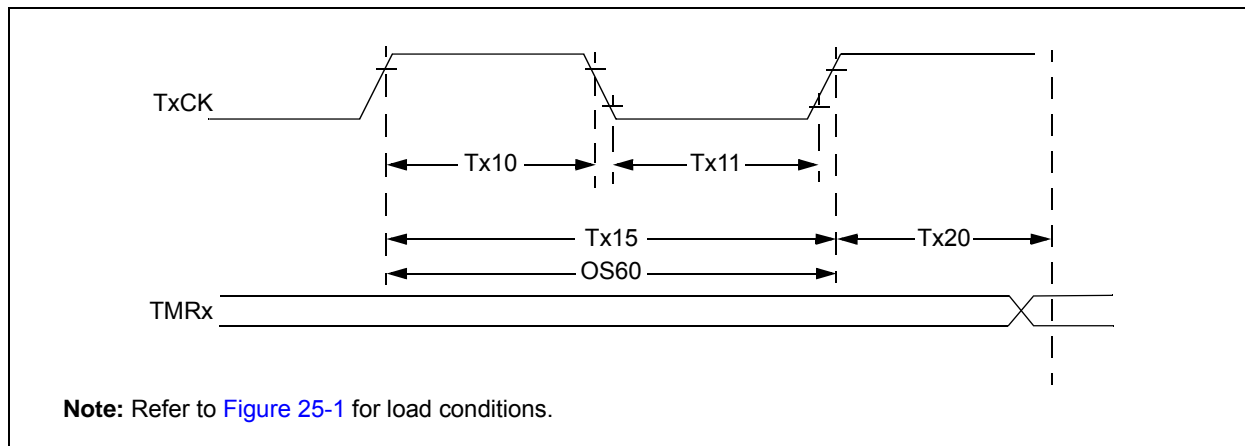


TABLE 25-24: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|--------------------|-----------|---|------------------|---|------|---------------|-------|--|
| Param No. | Symbol | Characteristic ⁽²⁾ | | Min. | Typ. | Max. | Units | Conditions |
| TA10 | TtxH | T1CK High Time | Synchronous mode | Greater of: 20 or (Tcy + 20)/N | — | — | ns | Must also meet Parameter TA15, N = Prescaler Value (1, 8, 64, 256) |
| | | | Asynchronous | 35 | — | — | ns | |
| TA11 | TtxL | T1CK Low Time | Synchronous mode | Greater of: 20 or (Tcy + 20)/N | — | — | ns | Must also meet Parameter TA15, N = Prescaler Value (1, 8, 64, 256) |
| | | | Asynchronous | 10 | — | — | ns | |
| TA15 | TtxP | T1CK Input Period | Synchronous mode | Greater of: 40 or (2 Tcy + 40)/N | — | — | ns | N = Prescale Value (1, 8, 64, 256) |
| OS60 | Ft1 | T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>)) | | DC | — | 50 | kHz | |
| TA20 | TckEXTMRL | Delay from External T1CK Clock Edge to Timer Increment | | 0.75 Tcy + 40 | — | 1.75 Tcy + 40 | ns | |

Note 1: Timer1 is a Type A timer.

Note 2: These parameters are characterized but not tested in manufacturing.

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TABLE 25-25: TIMER2 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|--------------------|-----------|--|------------------|---|------|---------------|-------|---|
| Param No. | Symbol | Characteristic ⁽¹⁾ | | Min. | Typ. | Max. | Units | Conditions |
| TB10 | TtxH | T2CK High Time | Synchronous mode | Greater of: 20 or (Tcy + 20)/N | — | — | ns | Must also meet Parameter TB15, N = Prescale Value (1, 8, 64, 256) |
| TB11 | TtxL | T2CK Low Time | Synchronous mode | Greater of: 20 or (Tcy + 20)/N | — | — | ns | Must also meet Parameter TB15, N = Prescale Value (1, 8, 64, 256) |
| TB15 | TtxP | T2CK Input Period | Synchronous mode | Greater of: 40 or (2 Tcy + 40)/N | — | — | ns | N = Prescale Value (1, 8, 64, 256) |
| TB20 | TCKEXTMRL | Delay from External T2CK Clock Edge to Timer Increment | | 0.75 Tcy + 40 | — | 1.75 Tcy + 40 | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 25-26: TIMER3 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|--------------------|-----------|--|----------------------------|---|------|---------------|-------|------------------------------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | | Min. | Typ. | Max. | Units | Conditions |
| TC10 | TtxH | T3CK High Time | Synchronous | Tcy + 20 | — | — | ns | Must also meet Parameter TC15 |
| TC11 | TtxL | T3CK Low Time | Synchronous | Tcy + 20 | — | — | ns | Must also meet Parameter TC15 |
| TC15 | TtxP | T3CK Input Period | Synchronous with Prescaler | 2 Tcy + 40 | — | — | ns | N = Prescale Value (1, 8, 64, 256) |
| TC20 | TCKEXTMRL | Delay from External T3CK Clock Edge to Timer Increment | | 0.75 Tcy + 40 | — | 1.75 Tcy + 40 | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

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FIGURE 25-6: INPUT CAPTURE 1 (IC1) TIMING CHARACTERISTICS

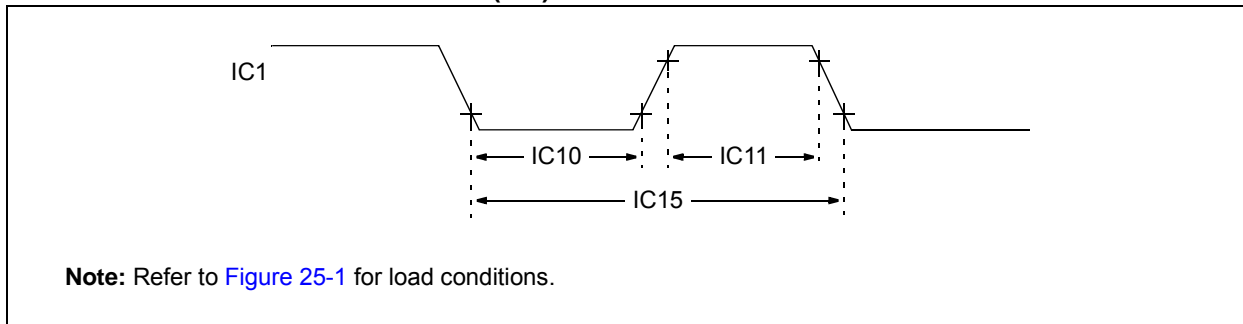


TABLE 25-27: INPUT CAPTURE 1 MODULE TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | |
|--------------------|--------|--------------------------------|---|------|-------|----------------------------------|
| Param. No. | Symbol | Characteristics ⁽¹⁾ | Min. | Max. | Units | Conditions |
| IC10 | TccL | IC1 Input Low Time | Greater of: 12.5 + 25 or (0.5 Tcy/N) + 25 | — | ns | Must also meet Parameter IC15 |
| IC11 | TccH | IC1 Input High Time | Greater of: 12.5 + 25 or (0.5 Tcy/N) + 25 | — | ns | Must also meet Parameter IC15 |
| IC15 | TccP | IC1 Input Period | Greater of: 25 + 50 or (1 Tcy/N) + 50 | — | ns | |

N = Prescale Value
(1, 4, 16)

Note 1: These parameters are characterized but not tested in manufacturing.

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FIGURE 25-7: OUTPUT COMPARE 1 MODULE (OC1) TIMING CHARACTERISTICS

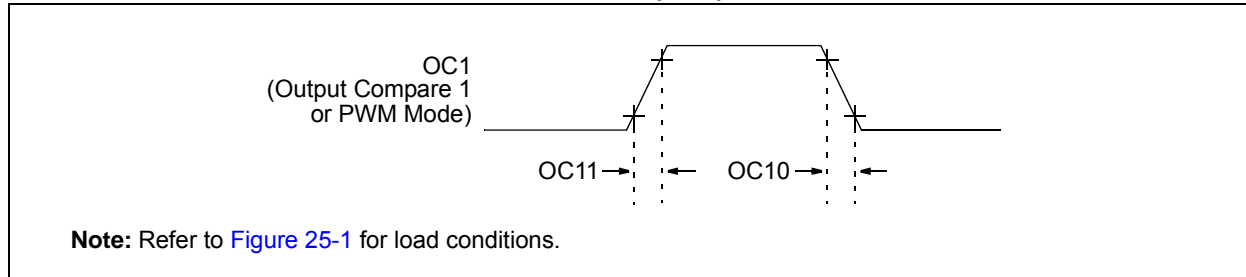


TABLE 25-28: OUTPUT COMPARE 1 MODULE TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|--------------------|--------|-------------------------------|---|------|------|-------|------------------------------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. | Max. | Units | Conditions |
| OC10 | TccF | OC1 Output Fall Time | — | — | — | ns | See Parameter DO32 |
| OC11 | TccR | OC1 Output Rise Time | — | — | — | ns | See Parameter DO31 |

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 25-8: OC1/PWMx MODULE TIMING CHARACTERISTICS

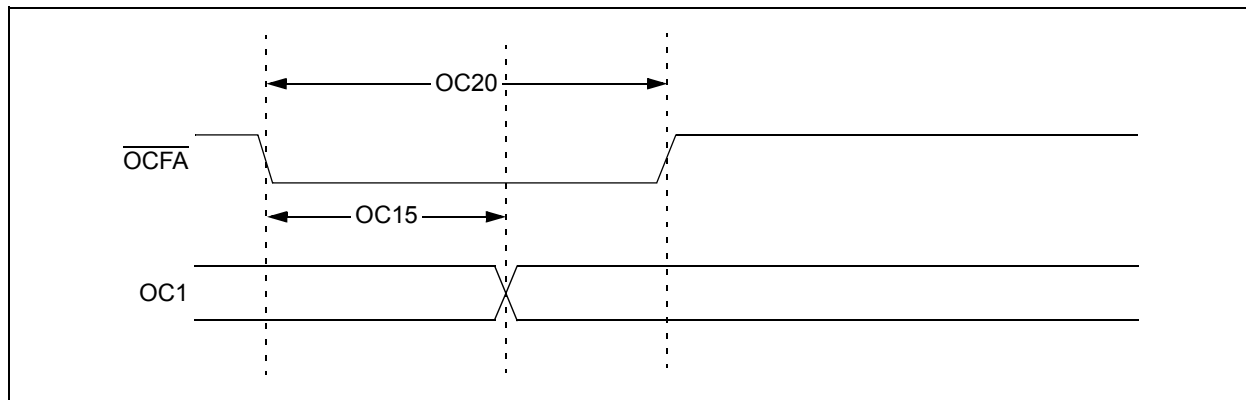


TABLE 25-29: OC1/PWMx MODULE TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|--------------------|--------|--------------------------------|---|------|---------------|-------|------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. | Max. | Units | Conditions |
| OC15 | TFD | Fault Input to PWMx I/O Change | — | — | $T_{CY} + 20$ | ns | |
| OC20 | TFLT | Fault Input Pulse Width | $T_{CY} + 20$ | — | — | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

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FIGURE 25-9: HIGH-SPEED PWMx MODULE FAULT TIMING CHARACTERISTICS

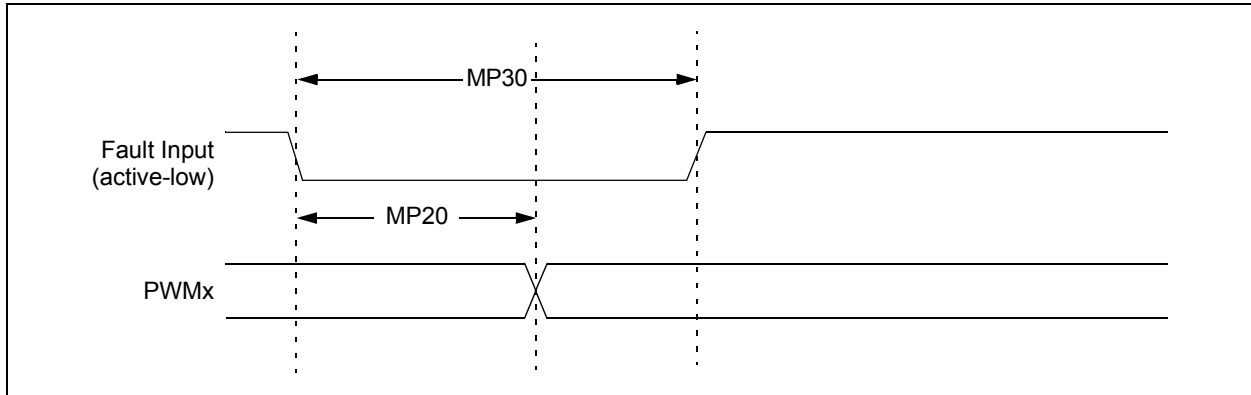


FIGURE 25-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS

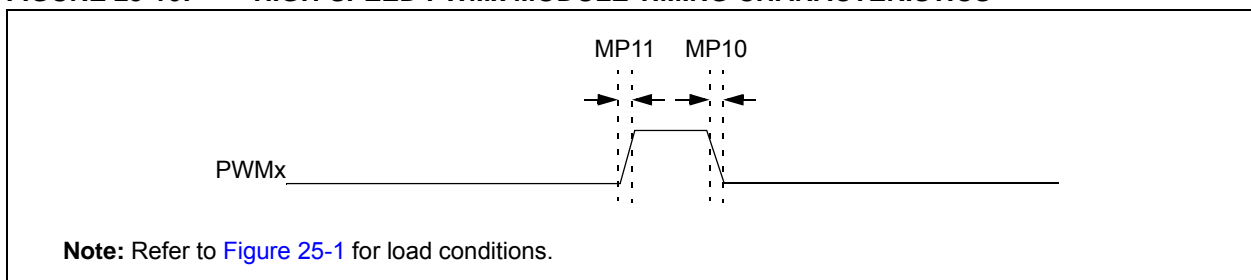


TABLE 25-30: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|--------------------|-------------------|----------------------------------|---|------|------|-------|------------------------------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. | Max. | Units | Conditions |
| MP10 | T _{FPWM} | PWMx Output Fall Time | — | — | — | ns | See Parameter DO32 |
| MP11 | T _{RPWM} | PWMx Output Rise Time | — | — | — | ns | See Parameter DO31 |
| MP20 | T _{FD} | Fault Input ↓ to PWMx I/O Change | — | — | 15 | ns | |
| MP30 | T _{FH} | Fault Input Pulse Width | 15 | — | — | ns | |

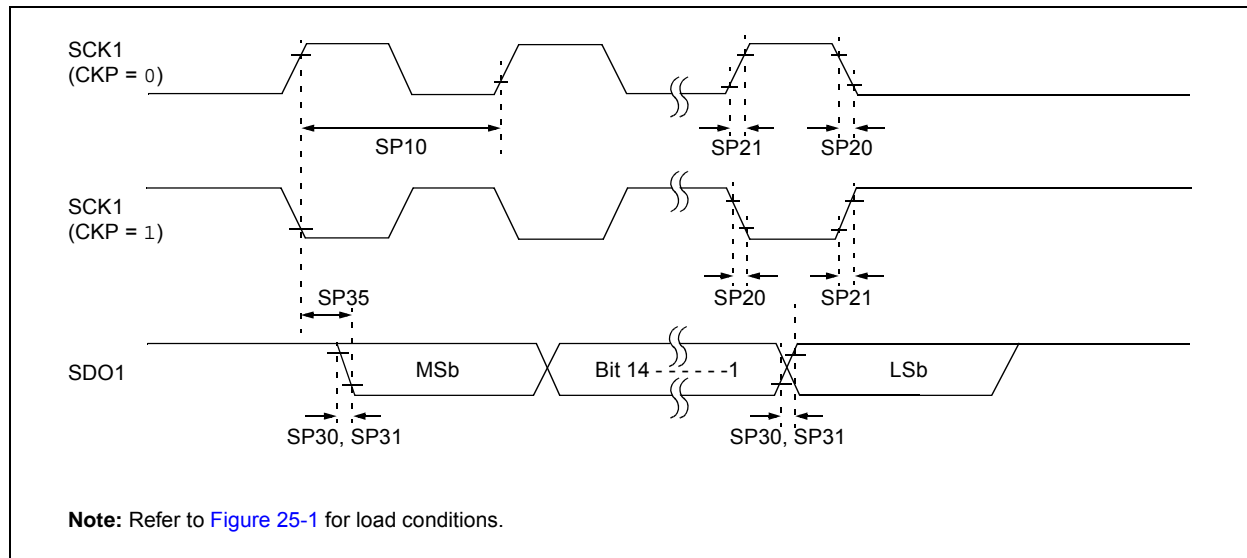
Note 1: These parameters are characterized but not tested in manufacturing.

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TABLE 25-31: SPI1 MAXIMUM DATA/CLOCK RATE SUMMARY

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | |
|--------------------|------------------------------------|---------------------------------------|---|-----|-----|-----|
| Maximum Data Rate | Master Transmit Only (Half-Duplex) | Master Transmit/Receive (Full-Duplex) | Slave Transmit/Receive (Full-Duplex) | CKE | CKP | SMP |
| 15 MHz | Table 25-31 | — | — | 0,1 | 0,1 | 0,1 |
| 9 MHz | — | Table 25-32 | — | 1 | 0,1 | 1 |
| 9 MHz | — | Table 25-33 | — | 0 | 0,1 | 1 |
| 15 MHz | — | — | Table 25-34 | 1 | 0 | 0 |
| 11 MHz | — | — | Table 25-35 | 1 | 1 | 0 |
| 15 MHz | — | — | Table 25-36 | 0 | 1 | 0 |
| 11 MHz | — | — | Table 25-37 | 0 | 0 | 0 |

FIGURE 25-11: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



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FIGURE 25-12: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS

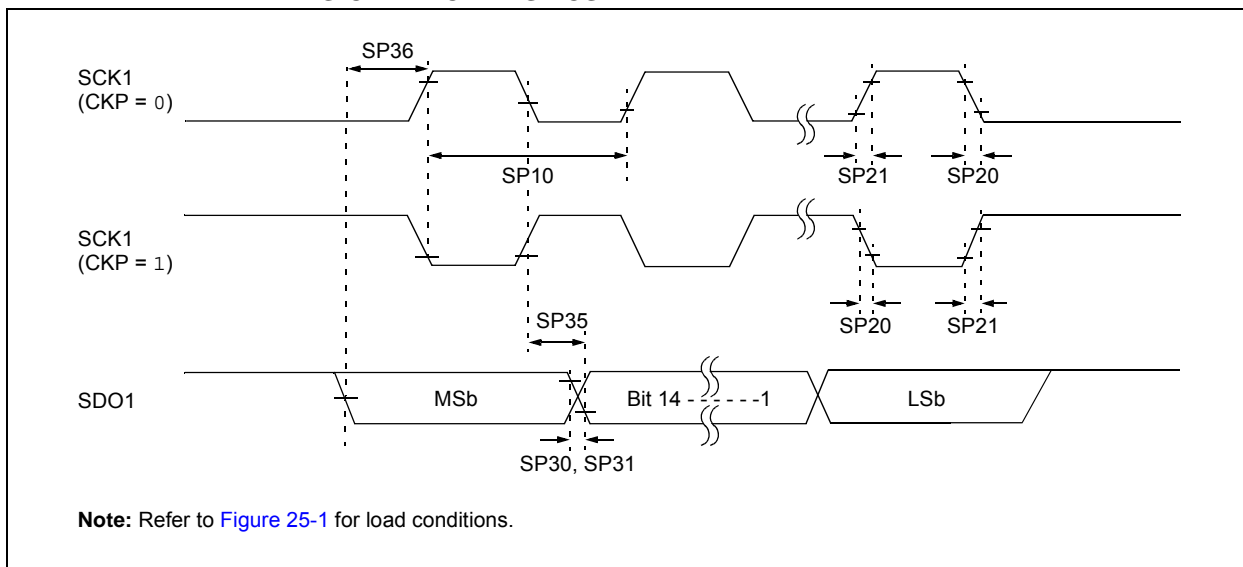


TABLE 25-32: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|--------------------|-----------------------|---|---|---------------------|------|-------|--------------------------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units | Conditions |
| SP10 | FscP | Maximum SCK1 Frequency | — | — | 15 | MHz | (Note 3) |
| SP20 | TscF | SCK1 Output Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP21 | TscR | SCK1 Output Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP35 | Tsch2doV, TscL2doV | SDO1 Data Output Valid After SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdiV2sch, TdiV2scl | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

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FIGURE 25-13: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS

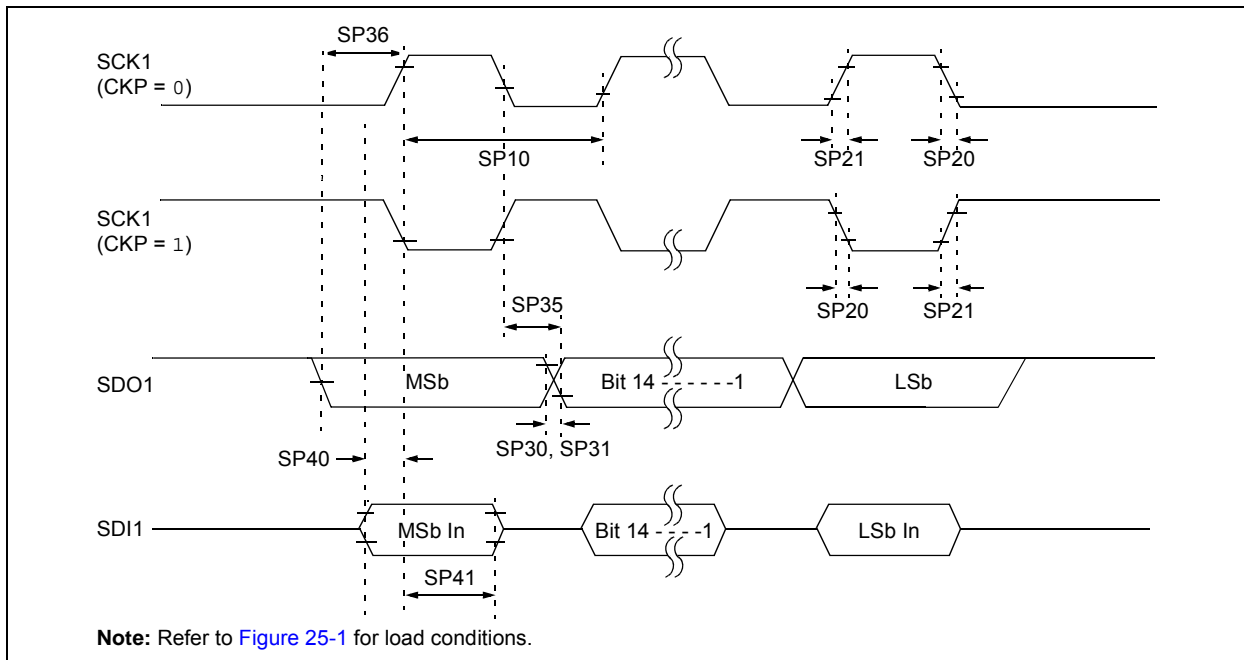


TABLE 25-33: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|--------------------|--------------------|--|--|---------------------|------|-------|-----------------------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units | Conditions |
| SP10 | FscP | Maximum SCK1 Frequency | — | — | 9 | MHz | (Note 3) |
| SP20 | TscF | SCK1 Output Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP21 | TscR | SCK1 Output Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP35 | Tsch2doV, TscL2doV | SDO1 Data Output Valid After SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2sc, TdoV2scl | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scl | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | Tsch2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

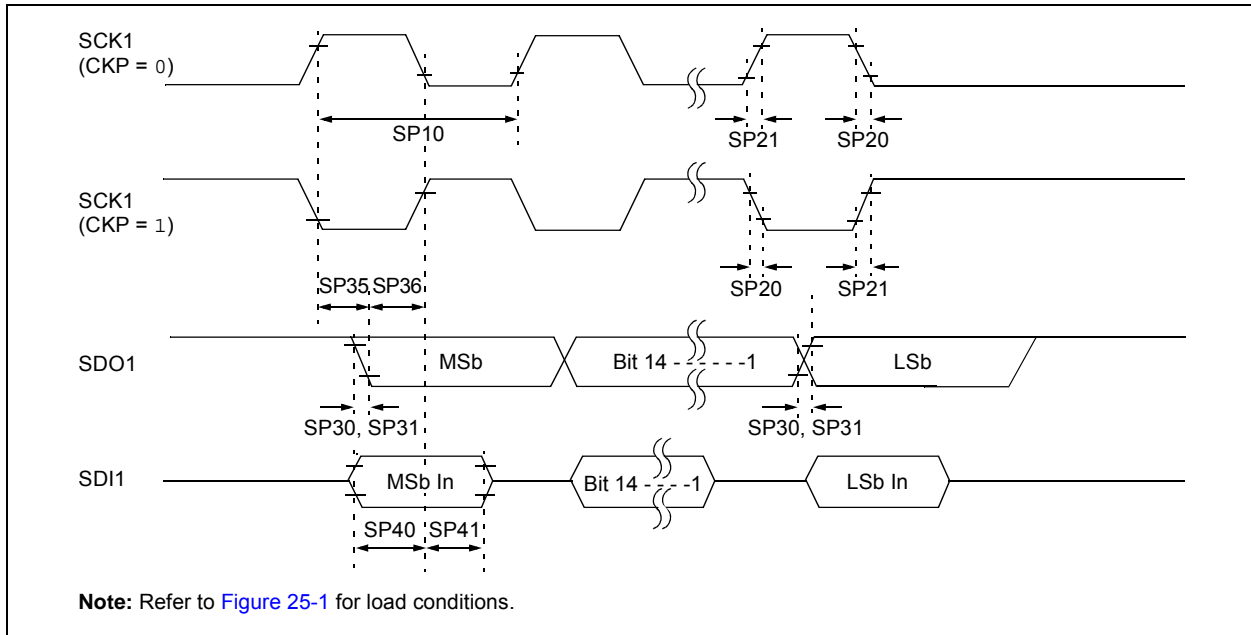
Note 2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

Note 3: The minimum clock period for SCK1 is 111 ns. The clock generated in Master mode must not violate this specification.

Note 4: Assumes 50 pF load on all SPI1 pins.

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**FIGURE 25-14: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING CHARACTERISTICS**



**TABLE 25-34: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------|-----------------------|---|---|---------------------|------|-------|--------------------------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units | Conditions |
| SP10 | FscP | Maximum SCK1 Frequency | — | — | 9 | MHz | -40°C to +125°C (Note 3) |
| SP20 | TscF | SCK1 Output Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP21 | TscR | SCK1 Output Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP35 | Tsch2doV, TscL2doV | SDO1 Data Output Valid After SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | Tsch2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

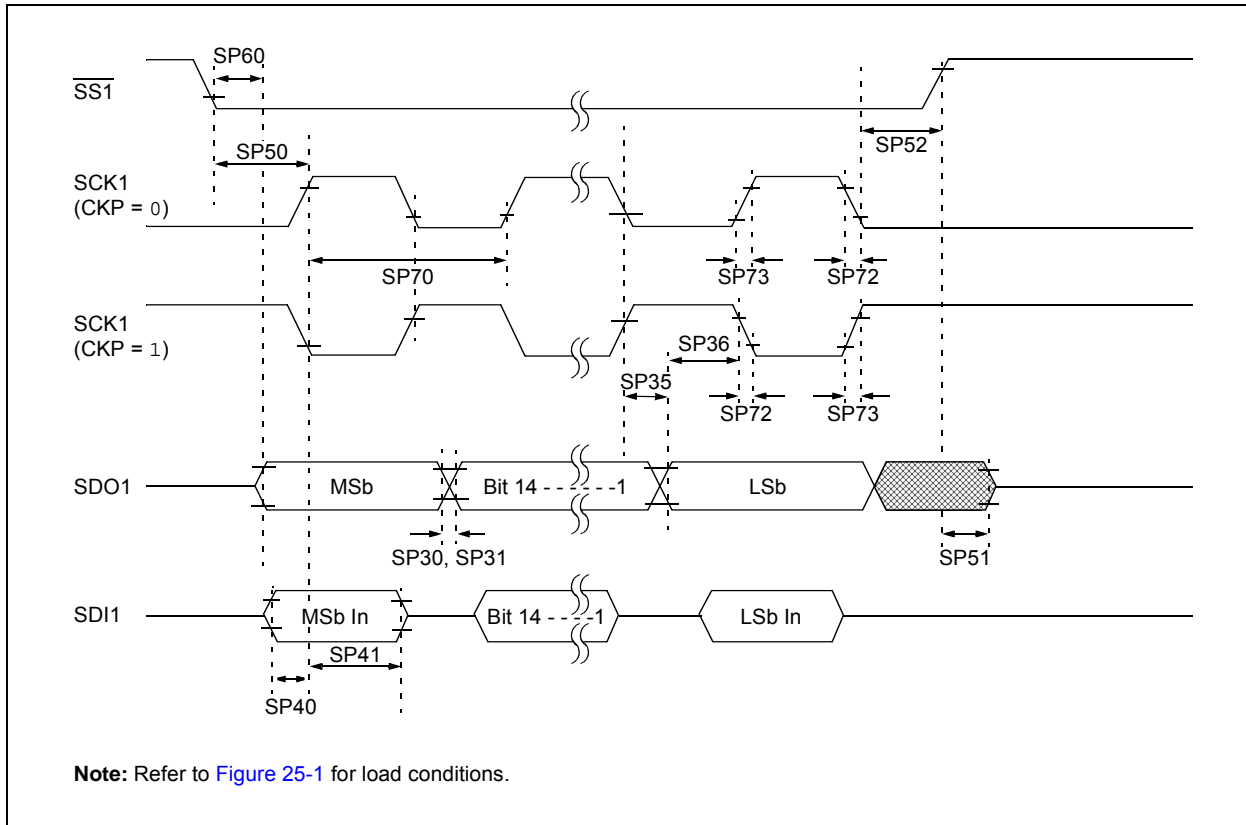
2: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

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FIGURE 25-15: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)
TIMING CHARACTERISTICS



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**TABLE 25-35: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)
TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------|------------------------|---|---|---------------------|------------------------|-------|--------------------------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units | Conditions |
| SP70 | FscP | Maximum SCK1 Input Frequency | — | — | Lesser of: FP or 15 | MHz | (Note 3) |
| SP72 | TscF | SCK1 Input Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP73 | TscR | SCK1 Input Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP35 | Tsch2doV, TscL2doV | SDO1 Data Output Valid After SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2schH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2schH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | Tsch2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP50 | TssL2schH, TssL2scL | $\overline{SS1} \downarrow$ to SCK1 \uparrow or SCK1 \downarrow Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS1} \uparrow$ to SDO1 Output High-Impedance | 10 | — | 50 | ns | (Note 4) |
| SP52 | Tsch2ssH, TscL2ssH | $\overline{SS1} \uparrow$ after SCK1 Edge | 1.5 T _{CY} + 40 | — | — | ns | (Note 4) |
| SP60 | TssL2doV | SDO1 Data Output Valid After $\overline{SS1}$ Edge | — | — | 50 | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

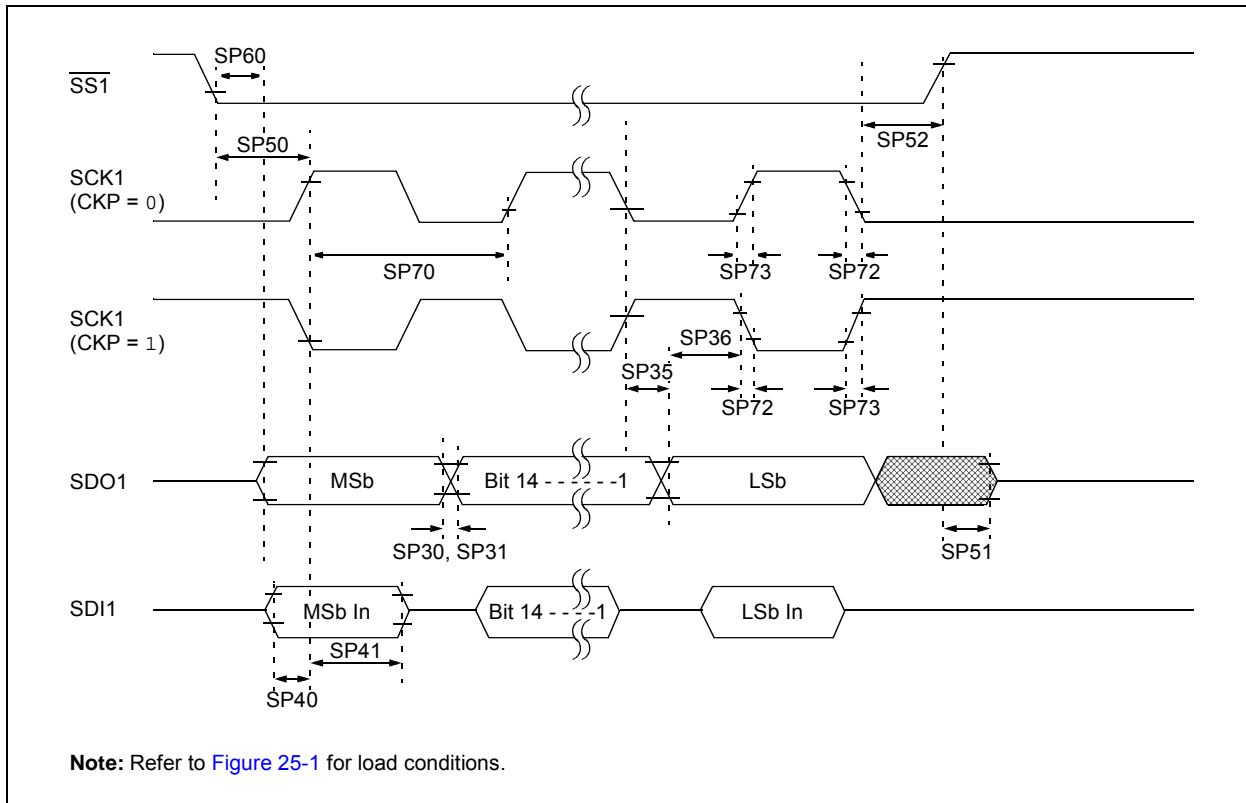
2: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

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FIGURE 25-16: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



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**TABLE 25-36: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)
TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------|-----------------------|---|---|---------------------|------------------------|-------|--------------------------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units | Conditions |
| SP70 | FscP | Maximum SCK1 Input Frequency | — | — | Lesser of: FP or 11 | MHz | (Note 3) |
| SP72 | TscF | SCK1 Input Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP73 | TscR | SCK1 Input Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP35 | Tsch2doV, TscL2doV | SDO1 Data Output Valid After SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2sch, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2sch, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | Tsch2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP50 | TssL2sch, TssL2scL | $\overline{SS1} \downarrow$ to SCK1 \uparrow or SCK1 \downarrow Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS1} \uparrow$ to SDO1 Output High-Impedance | 10 | — | 50 | ns | (Note 4) |
| SP52 | Tsch2ssH, TscL2ssH | $\overline{SS1} \uparrow$ after SCK1 Edge | 1.5 Tcy + 40 | — | — | ns | (Note 4) |
| SP60 | TssL2doV | SDO1 Data Output Valid after $\overline{SS1}$ Edge | — | — | 50 | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

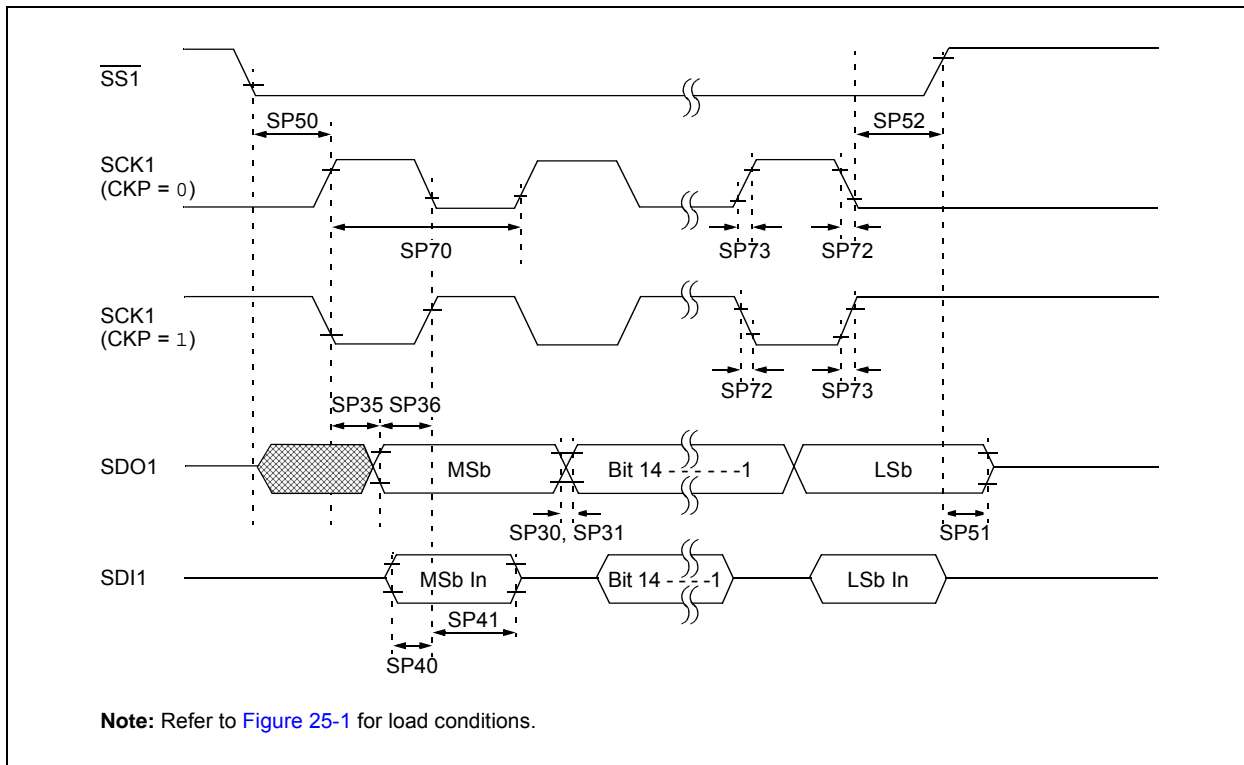
2: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

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FIGURE 25-17: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)
TIMING CHARACTERISTICS



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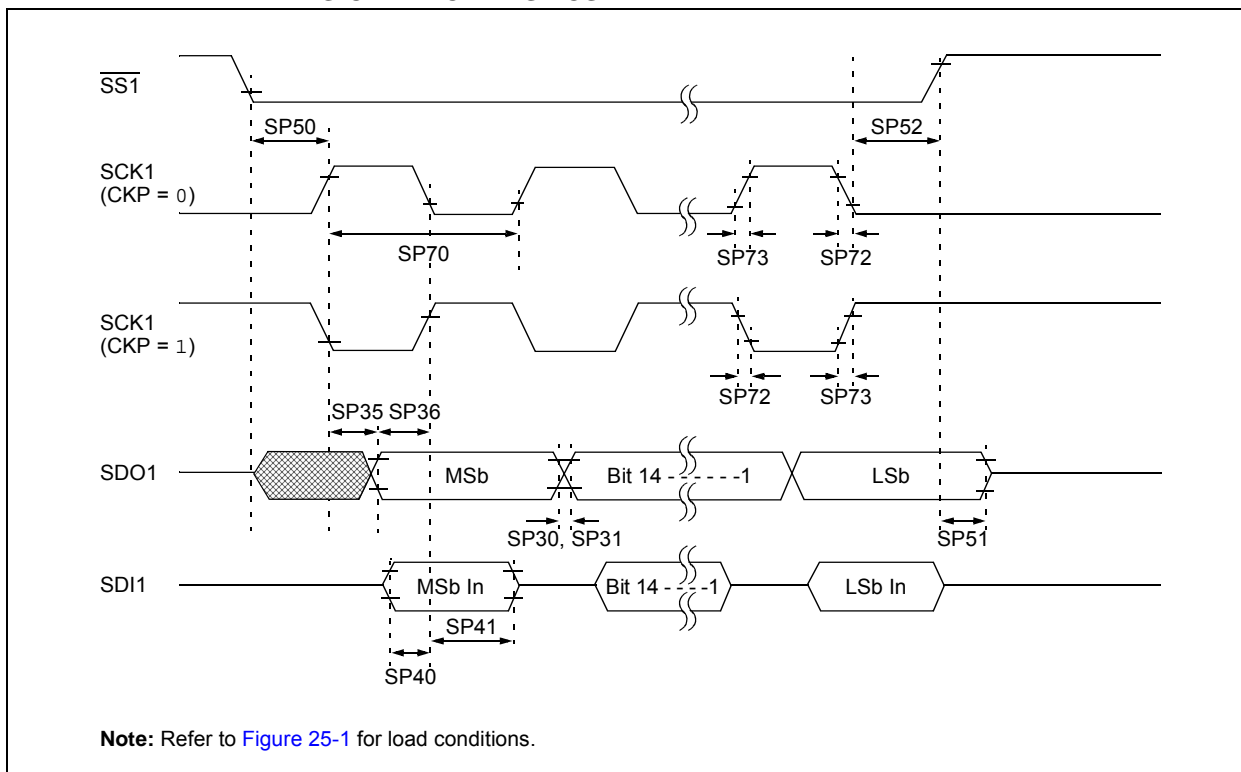
**TABLE 25-37: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)
TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------|-----------------------|--|---|---------------------|------|-------|--------------------------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units | Conditions |
| SP70 | FscP | Maximum SCK1 Input Frequency | — | — | 15 | MHz | (Note 3) |
| SP72 | TscF | SCK1 Input Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP73 | TscR | SCK1 Input Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP35 | Tsch2doV, TscL2doV | SDO1 Data Output Valid After SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | Tsch2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS1}$ ↑ to SDO1 Output High-Impedance | 10 | — | 50 | ns | (Note 4) |
| SP52 | Tsch2ssH, TscL2ssH | $\overline{SS1}$ ↑ After SCK1 Edge | 1.5 TCY + 40 | — | — | ns | (Note 4) |

- Note 1:** These parameters are characterized but not tested in manufacturing.
- Note 2:** Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.
- Note 3:** The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.
- Note 4:** Assumes 50 pF load on all SPI1 pins.

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FIGURE 25-18: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



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**TABLE 25-38: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)
TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------|-----------------------|---|---|---------------------|------|-------|--------------------------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units | Conditions |
| SP70 | FscP | Maximum SCK1 Input Frequency | — | — | 11 | MHz | (Note 3) |
| SP72 | TscF | SCK1 Input Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP73 | TscR | SCK1 Input Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (Note 4) |
| SP35 | Tsch2doV, TscL2doV | SDO1 Data Output Valid After SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | Tsch2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS1} \downarrow$ to SCK1 \uparrow or SCK1 \downarrow Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS1} \uparrow$ to SDO1 Output High-Impedance | 10 | — | 50 | ns | (Note 4) |
| SP52 | Tsch2ssH, TscL2ssH | $\overline{SS1} \uparrow$ After SCK1 Edge | 1.5 T _{CY} + 40 | — | — | ns | (Note 4) |

- Note 1:** These parameters are characterized but not tested in manufacturing.
Note 2: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.
Note 3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.
Note 4: Assumes 50 pF load on all SPI1 pins.

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FIGURE 25-19: I2C1 BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

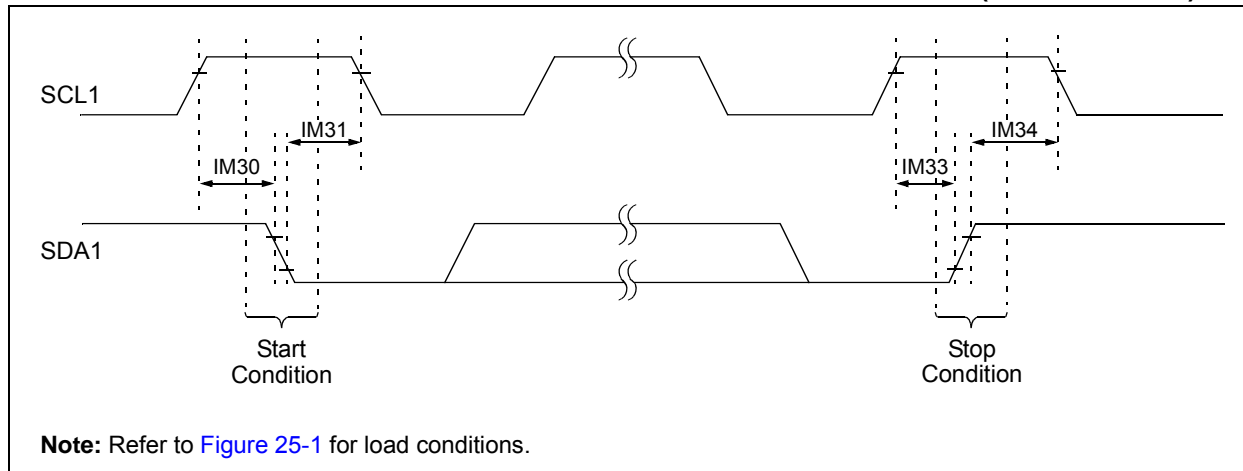
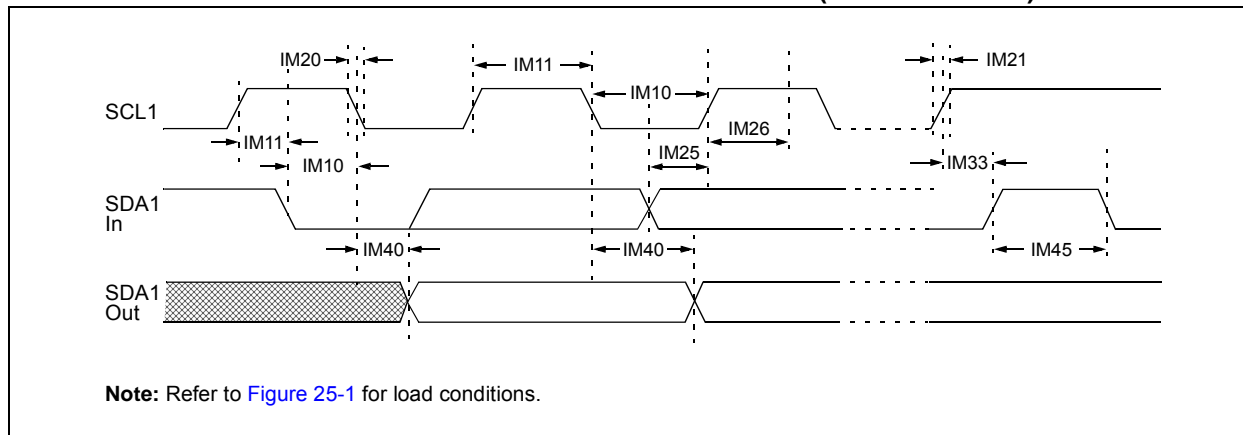


FIGURE 25-20: I2C1 BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



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TABLE 25-39: I2C1 BUS DATA TIMING REQUIREMENTS (MASTER MODE)

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | |
|--------------------|---------|-------------------------------|---------------------------|---|------|---------------|---|
| Param No. | Symbol | Characteristic ⁽⁴⁾ | | Min. ⁽¹⁾ | Max. | Units | Conditions |
| IM10 | TLO:SCL | Clock Low Time | 100 kHz mode | $T_{CY} (BRG + 1)$ | — | μs | |
| | | | 400 kHz mode | $T_{CY} (BRG + 1)$ | — | μs | |
| | | | 1 MHz mode ⁽²⁾ | $T_{CY} (BRG + 1)$ | — | μs | |
| IM11 | THI:SCL | Clock High Time | 100 kHz mode | $T_{CY} (BRG + 1)$ | — | μs | |
| | | | 400 kHz mode | $T_{CY} (BRG + 1)$ | — | μs | |
| | | | 1 MHz mode ⁽²⁾ | $T_{CY} (BRG + 1)$ | — | μs | |
| IM20 | TF:SCL | SDA1 and SCL1 Fall Time | 100 kHz mode | — | 300 | ns | Cb is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | $20 + 0.1 C_B$ | 300 | ns | |
| | | | 1 MHz mode ⁽²⁾ | — | 100 | ns | |
| IM21 | TR:SCL | SDA1 and SCL1 Rise Time | 100 kHz mode | — | 1000 | ns | Cb is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | $20 + 0.1 C_B$ | 300 | ns | |
| | | | 1 MHz mode ⁽²⁾ | — | 300 | ns | |
| IM25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode ⁽²⁾ | 40 | — | ns | |
| IM26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | μs | |
| | | | 400 kHz mode | 0 | 0.9 | μs | |
| | | | 1 MHz mode ⁽²⁾ | 0.2 | — | μs | |
| IM30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | $T_{CY} (BRG + 1)$ | — | μs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | $T_{CY} (BRG + 1)$ | — | μs | |
| | | | 1 MHz mode ⁽²⁾ | $T_{CY} (BRG + 1)$ | — | μs | |
| IM31 | THD:STA | Start Condition Hold Time | 100 kHz mode | $T_{CY} (BRG + 1)$ | — | μs | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | $T_{CY} (BRG + 1)$ | — | μs | |
| | | | 1 MHz mode ⁽²⁾ | $T_{CY} (BRG + 1)$ | — | μs | |
| IM33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | $T_{CY} (BRG + 1)$ | — | μs | |
| | | | 400 kHz mode | $T_{CY} (BRG + 1)$ | — | μs | |
| | | | 1 MHz mode ⁽²⁾ | $T_{CY} (BRG + 1)$ | — | μs | |
| IM34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | $T_{CY} (BRG + 1)$ | — | μs | |
| | | | 400 kHz mode | $T_{CY} (BRG + 1)$ | — | μs | |
| | | | 1 MHz mode ⁽²⁾ | $T_{CY} (BRG + 1)$ | — | μs | |
| IM40 | TAA:SCL | Output Valid from Clock | 100 kHz mode | — | 3500 | ns | |
| | | | 400 kHz mode | — | 1000 | ns | |
| | | | 1 MHz mode ⁽²⁾ | — | 400 | ns | |
| IM45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | μs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | μs | |
| | | | 1 MHz mode ⁽²⁾ | 0.5 | — | μs | |
| IM50 | CB | Bus Capacitive Loading | — | 400 | pF | | |
| IM51 | TPGD | Pulse Gobbler Delay | 65 | 390 | ns | (Note 3) | |

Note 1: BRG is the value of the I²C Baud Rate Generator.

2: Maximum Pin Capacitance = 10 pF for all I2C1 pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

4: These parameters are characterized but not tested in manufacturing.

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FIGURE 25-21: I2C1 BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

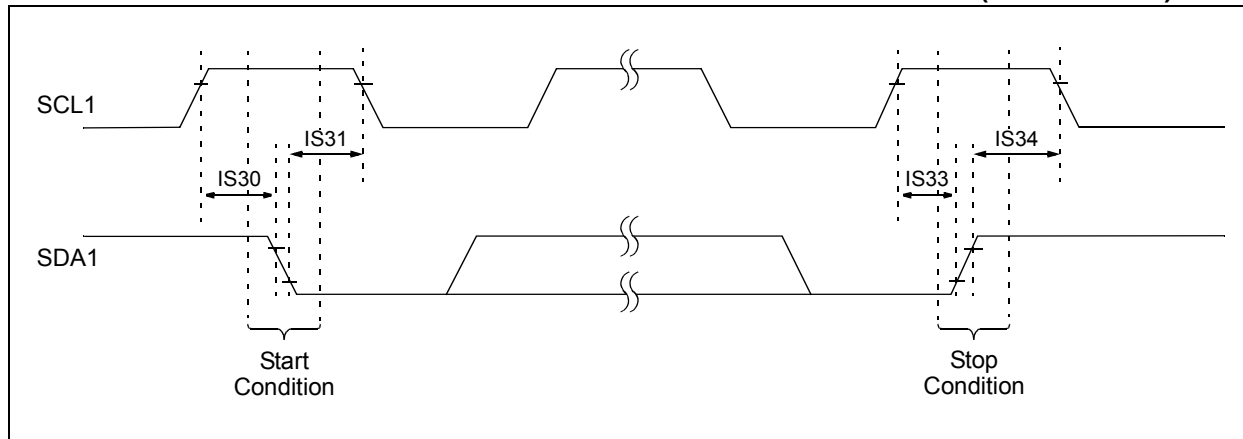
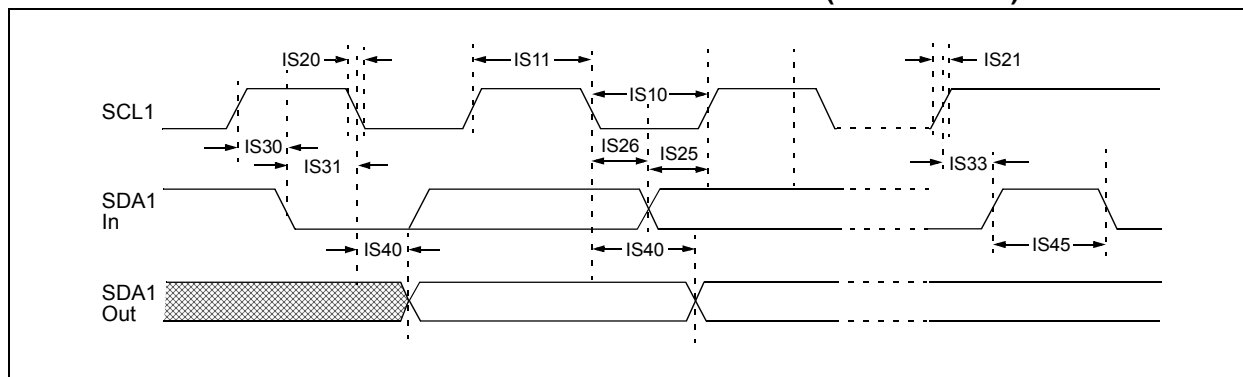


FIGURE 25-22: I2C1 BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



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TABLE 25-40: I2C1 BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | |
|--------------------|---------|-------------------------------|---------------------------|---|------|---------------|---|
| Param No. | Symbol | Characteristic ⁽³⁾ | | Min. | Max. | Units | Conditions |
| IS10 | TLO:SCL | Clock Low Time | 100 kHz mode | 4.7 | — | μs | |
| | | | 400 kHz mode | 1.3 | — | μs | |
| | | | 1 MHz mode ⁽¹⁾ | 0.5 | — | μs | |
| IS11 | THI:SCL | Clock High Time | 100 kHz mode | 4.0 | — | μs | Device must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 0.6 | — | μs | Device must operate at a minimum of 10 MHz |
| | | | 1 MHz mode ⁽¹⁾ | 0.5 | — | μs | |
| IS20 | TF:SCL | SDA1 and SCL1 Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | $20 + 0.1 \text{ CB}$ | 300 | ns | |
| | | | 1 MHz mode ⁽¹⁾ | — | 100 | ns | |
| IS21 | TR:SCL | SDA1 and SCL1 Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | $20 + 0.1 \text{ CB}$ | 300 | ns | |
| | | | 1 MHz mode ⁽¹⁾ | — | 300 | ns | |
| IS25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode ⁽¹⁾ | 100 | — | ns | |
| IS26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | μs | |
| | | | 400 kHz mode | 0 | 0.9 | μs | |
| | | | 1 MHz mode ⁽¹⁾ | 0 | 0.3 | μs | |
| IS30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | 4.7 | — | μs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 0.6 | — | μs | |
| | | | 1 MHz mode ⁽¹⁾ | 0.25 | — | μs | |
| IS31 | THD:STA | Start Condition Hold Time | 100 kHz mode | 4.0 | — | μs | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | 0.6 | — | μs | |
| | | | 1 MHz mode ⁽¹⁾ | 0.25 | — | μs | |
| IS33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | 4 | — | μs | |
| | | | 400 kHz mode | 0.6 | — | μs | |
| | | | 1 MHz mode ⁽¹⁾ | 0.25 | — | μs | |
| IS34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | 4 | — | μs | |
| | | | 400 kHz mode | 0.6 | — | μs | |
| | | | 1 MHz mode ⁽¹⁾ | 0.25 | — | μs | |
| IS40 | TAA:SCL | Output Valid from Clock | 100 kHz mode | 0 | 3500 | ns | |
| | | | 400 kHz mode | 0 | 1000 | ns | |
| | | | 1 MHz mode ⁽¹⁾ | 0 | 350 | ns | |
| IS45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | μs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | μs | |
| | | | 1 MHz mode ⁽¹⁾ | 0.5 | — | μs | |
| IS50 | CB | Bus Capacitive Loading | | — | 400 | pF | |
| IS51 | TPGD | Pulse Gobbler Delay | | 65 | 390 | ns | (Note 2) |

Note 1: Maximum Pin Capacitance = 10 pF for all I2C1 pins (for 1 MHz mode only).

2: Typical value for this parameter is 130 ns.

3: These parameters are characterized but not tested in manufacturing.

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FIGURE 25-23: UART1 MODULE I/O TIMING CHARACTERISTICS

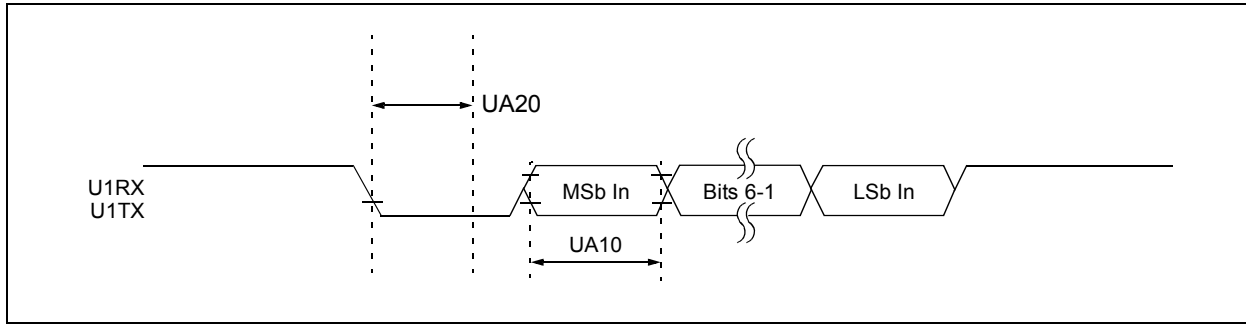


TABLE 25-41: UART1 MODULE I/O TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | | | | |
|--------------------|---------|---|--|---------------------|------|-------|------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units | Conditions |
| UA10 | TUABAUD | UART1 Baud Time | 66.67 | — | — | ns | |
| UA11 | FBAUD | UART1 Baud Frequency | — | — | 15 | Mbps | |
| UA20 | TCWF | Start Bit Pulse Width to Trigger UART1 Wake-up | 500 | — | — | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 25-42: ANALOG CURRENT SPECIFICATIONS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | | | | |
|--------------------|--------|---------------------------------------|--|---------------------|------|-------|---|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units | Conditions |
| AVD01 | IDD | Analog Modules Current Consumption | — | 9 | — | mA | Characterized data with the following modules enabled: APLL, 5 ADC Cores, 2 PGAs and 4 Analog Comparators |

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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TABLE 25-43: ADC MODULE SPECIFICATIONS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽⁴⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|-----------|--|--|---------|-----------------------------------|-------|---|
| Param No. | Symbol | Characteristics ⁽³⁾ | Min. | Typical | Max. | Units | Conditions |
| Device Supply | | | | | | | |
| AD01 | AVDD | Module VDD Supply | Greater of: VDD – 0.3 or 3.0 | — | Lesser of: VDD + 0.3 or 3.6 | V | The difference between AVDD supply and VDD supply must not exceed ±300 mV at all times, including device power-up |
| AD02 | AVSS | Module Vss Supply | Vss | — | Vss + 0.3 | V | |
| Analog Input | | | | | | | |
| AD12 | VINH-VINL | Full-Scale Input Span | AVSS | — | AVDD | V | |
| AD14 | VIN | Absolute Input Voltage | AVSS – 0.3 | — | AVDD + 0.3 | V | |
| AD15 | VIN+ | Pseudodifferential Mode | 0 | — | 3.3 | V | VIN- = (VR+ + VR-)/2 ±150 mV |
| AD16 | VIN- | Pseudodifferential Mode | 0 | — | 3.3 | V | VIN+ = (VR+ + VR-)/2 ±150 mV |
| AD17 | RIN | Recommended Impedance of Analog Voltage Source | — | 100 | — | Ω | For minimum sampling time (Note 1) |
| AD66 | VREF1 | Internal Voltage Reference Source | 1.176 | 1.2 | 1.224 | V | |
| ADC Accuracy: Pseudodifferential Input | | | | | | | |
| AD20a | Nr | Resolution | 12 | | | bits | |
| AD21a | INL | Integral Nonlinearity | > -4 | — | < 4 | LSb | AVSS = 0V, AVDD = 3.3V |
| AD22a | DNL | Pseudodifferential Nonlinearity | > -1 | — | < 1 | LSb | AVSS = 0V, AVDD = 3.3V (Note 5) |
| AD23a | GERR | Gain Error (Dedicated Core) | > -5 | — | < 5 | LSb | AVSS = 0V, AVDD = 3.3V |
| AD24a | EOFF | Offset Error (Dedicated Core) | > -5 | — | < 5 | LSb | AVSS = 0V, AVDD = 3.3V |
| AD25a | — | Monotonicity | — | — | — | — | Guaranteed |

- Note 1:** These parameters are not characterized or tested in manufacturing.
Note 2: These parameters are characterized but not tested in manufacturing.
Note 3: Characterized with a 1 kHz sine wave.
Note 4: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.
Note 5: No missing codes, limits are based on the characterization results.

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TABLE 25-43: ADC MODULE SPECIFICATIONS (CONTINUED)

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽⁴⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|--------|---------------------------------|--|---------|-------|-------|--|
| Param No. | Symbol | Characteristics ⁽³⁾ | Min. | Typical | Max. | Units | Conditions |
| ADC Accuracy: Single-Ended Input | | | | | | | |
| AD20b | Nr | Resolution | 12 | | | bits | |
| AD21b | INL | Integral Nonlinearity | > -4 | — | < 4 | LSb | AVSS = 0V, AVDD = 3.3V |
| AD22b | DNL | Pseudodifferential Nonlinearity | > -1 | — | < 1.5 | LSb | AVSS = 0V, AVDD = 3.3V (Note 5) |
| AD23b | GERR | Gain Error (Dedicated Core) | > -5 | — | < 5 | LSb | AVSS = 0V, AVDD = 3.3V |
| | | Gain Error (Shared Core) | > -5 | — | < 5 | LSb | AVSS = 0V, AVDD = 3.3V, -40°C < TA ≤ +85°C |
| | | | > -6 | — | < 6 | LSb | AVSS = 0V, AVDD = 3.3V, -85°C < TA ≤ +125°C |
| AD24b | EOFF | Offset Error (Dedicated Core) | 0 | 7 | < 12 | LSb | AVSS = 0V, AVDD = 3.3V |
| | | Offset Error (Shared Core) | 0 | 7 | < 12 | LSb | |
| AD25b | — | Monotonicity | — | — | — | — | Guaranteed |
| Dynamic Performance | | | | | | | |
| AD31b | SINAD | Signal-to-Noise and Distortion | 63 | — | > 65 | dB | (Notes 2, 3) |
| AD34b | ENOB | Effective Number of bits | 10.3 | — | — | bits | (Notes 2, 3) |

- Note 1:** These parameters are not characterized or tested in manufacturing.
- 2:** These parameters are characterized but not tested in manufacturing.
- 3:** Characterized with a 1 kHz sine wave.
- 4:** The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.
- 5:** No missing codes, limits are based on the characterization results.

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TABLE 25-44: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

| AC CHARACTERISTICS ⁽²⁾ | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽²⁾ Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|-----------------------------------|--------|------------------|--|---------------------|------|-------|--|
| Param No. | Symbol | Characteristics | Min. | Typ. ⁽¹⁾ | Max. | Units | Conditions |
| Clock Parameters | | | | | | | |
| AD50 | TAD | ADC Clock Period | 14.28 | — | — | ns | |
| Throughput Rate | | | | | | | |
| AD51 | FTP | ADC Core 0, 1, 2 | — | — | 3.25 | Msp | 70 MHz ADC clock, 12 bits, no pending conversions at time of trigger |

Note 1: These parameters are characterized but not tested in manufacturing.

2: The ADC module is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

TABLE 25-45: HIGH-SPEED ANALOG COMPARATOR MODULE SPECIFICATIONS

| AC/DC CHARACTERISTICS ⁽²⁾ | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended | | | | |
|--------------------------------------|-------------------|--|---|------|------------------|-------|---|
| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Comments |
| CM10 | V _{IOFF} | Input Offset Voltage | -35 | ±5 | +35 | mV | |
| CM11 | V _{ICM} | Input Common-Mode Voltage Range ⁽¹⁾ | 0 | — | AV _{DD} | V | |
| CM13 | CMRR | Common-Mode Rejection Ratio | 60 | — | — | dB | |
| CM14 | T _{RESP} | Large Signal Response | — | 15 | — | ns | V+ input step of 100 mV while V- input is held at AV _{DD} /2. Delay measured from analog input pin to PWMx output pin. |
| CM15 | V _{HYST} | Input Hysteresis | 5 | 10 | 20 | mV | Depends on HYSSEL<1:0> |
| CM16 | T _{ON} | Comparator Enabled to Valid Output | — | — | 1 | µs | |

Note 1: These parameters are for design guidance only and are not tested in manufacturing.

2: The comparator module is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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TABLE 25-46: DACx MODULE SPECIFICATIONS

| AC/DC CHARACTERISTICS ⁽²⁾ | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------------------------|--------|---------------------------------|---|------|------|-------|---|
| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Comments |
| DA02 | CVRES | Resolution | 12 | | | bits | |
| DA03 | INL | Integral Nonlinearity Error | — | -12 | — | LSb | |
| DA04 | DNL | Differential Nonlinearity Error | -1.8 | ±0.5 | 1.8 | LSb | |
| DA05 | E0FF | Offset Error | -8 | 3 | 15 | LSb | |
| DA06 | EG | Gain Error | -0.8 | -0.4 | — | % | |
| DA07 | TSET | Settling Time ⁽¹⁾ | — | 700 | — | ns | Output with 2% of desired output voltage with a 10-90% or 90-10% step |

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: The DACx module is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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TABLE 25-47: PGAx MODULE SPECIFICATIONS

| AC/DC CHARACTERISTICS ⁽¹⁾ | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | | |
|--------------------------------------|--------|---|---|-------------|------------|--------|--|--|
| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Comments | |
| PA01 | VIN | Input Voltage Range | AVSS – 0.3 | — | AVDD + 0.3 | V | | |
| PA02 | VCM | Common-Mode Input Voltage Range | AVSS | — | AVDD – 1.6 | V | | |
| PA03 | Vos | Input Offset Voltage | -20 | — | +20 | mV | | |
| PA04 | VOS | Input Offset Voltage Drift with Temperature | — | ±15 | — | µV/°C | | |
| PA05 | RIN+ | Input Impedance of Positive Input | — | >1M 7 pf | — | Ω pF | | |
| PA06 | RIN- | Input Impedance of Negative Input | — | 10K 7 pf | — | Ω pF | | |
| PA07 | GERR | Gain Error | -2 | — | +2 | % | Gain = 4x and 8x | |
| | | | -3 | — | +3 | % | Gain = 16x | |
| | | | -4 | — | +4 | % | Gain = 32x and 64x | |
| PA08 | LERR | Gain Nonlinearity Error | — | — | 0.5 | % | % of full scale, Gain = 16x | |
| PA09 | IDD | Current Consumption | — | 2.0 | — | mA | Module is enabled with a 2-volt P-P output voltage swing | |
| PA10a | BW | Small Signal Bandwidth (-3 dB) | G = 4x | — | 10 | — | MHz | |
| PA10b | | | G = 8x | — | 5 | — | MHz | |
| PA10c | | | G = 16x | — | 2.5 | — | MHz | |
| PA10d | | | G = 32x | — | 1.25 | — | MHz | |
| PA10e | | | G = 64x | — | 0.625 | — | MHz | |
| PA11 | OST | Output Settling Time to 1% of Final Value | — | 0.4 | — | µs | Gain = 16x, 100 mV input step change | |
| PA12 | SR | Output Slew Rate | — | 40 | — | V/µs | Gain = 16x | |
| PA13 | TGSEL | Gain Selection Time | — | 1 | — | µs | | |
| PA14 | TON | Module Turn On/Setting Time | — | — | 10 | µs | | |

Note 1: The PGAx module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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NOTES:

26.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 26-1: V_{OH} – 4x DRIVER PINS

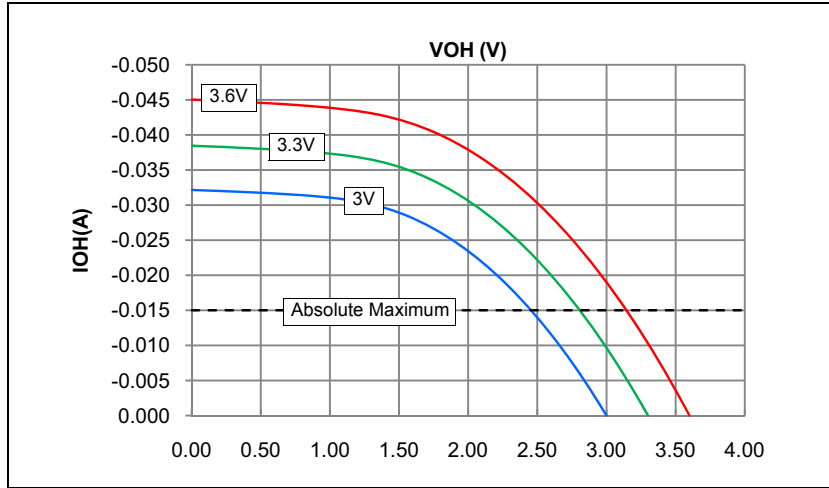


FIGURE 26-3: V_{OL} – 4x DRIVER PINS

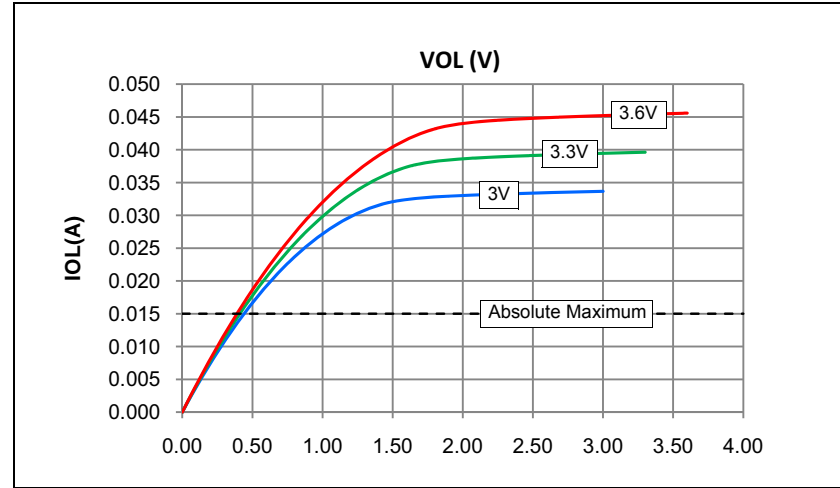


FIGURE 26-2: V_{OH} – 8x DRIVER PINS

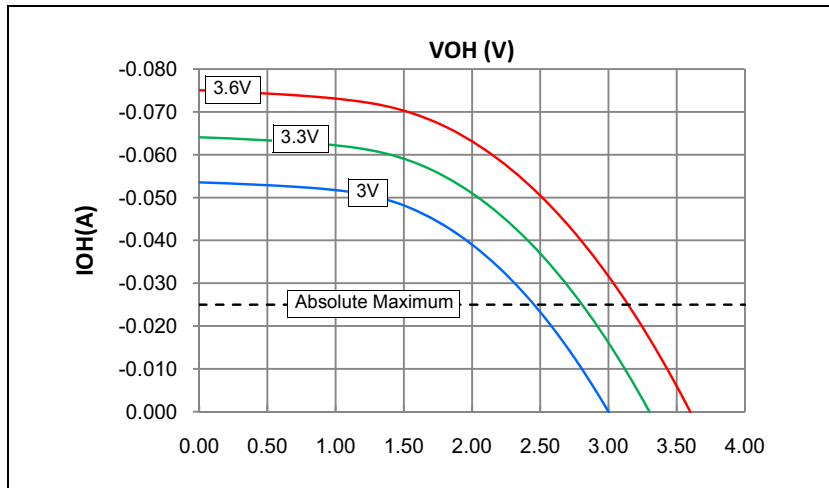


FIGURE 26-4: V_{OL} – 8x DRIVER PINS

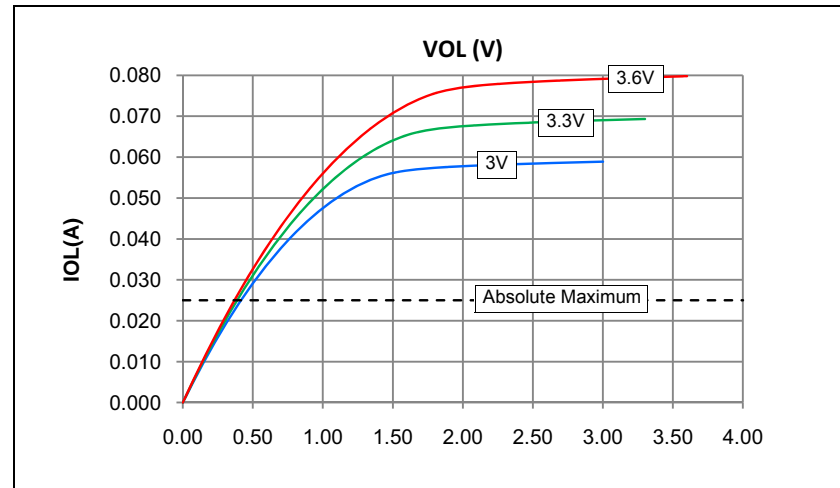


FIGURE 26-5: TYPICAL I_{PD} CURRENT @ V_{DD} = 3.3V

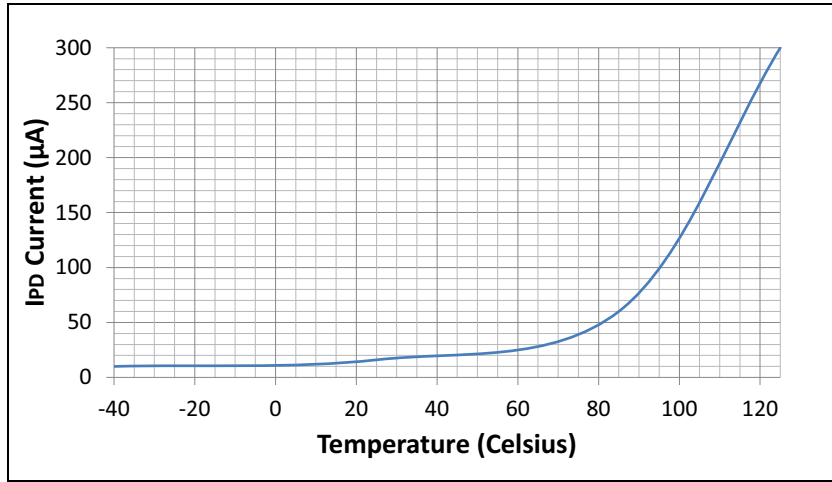


FIGURE 26-7: TYPICAL I_{DOZE} CURRENT @ V_{DD} = 3.3V, +25°C

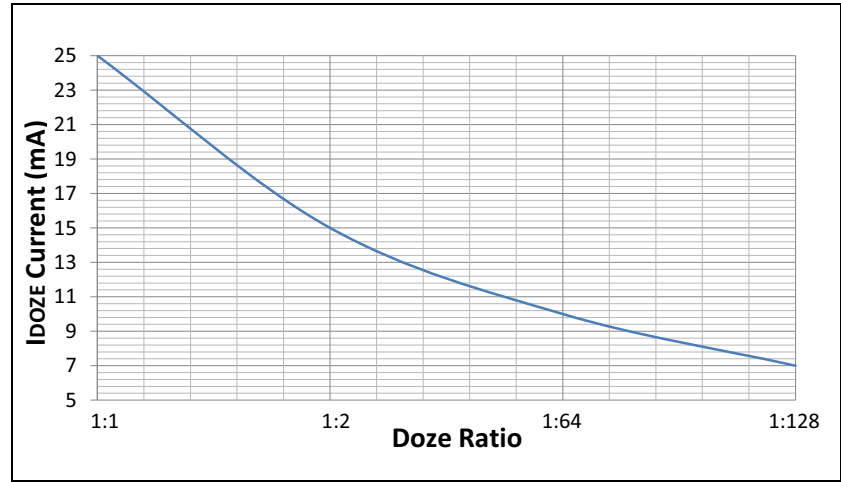


FIGURE 26-6: TYPICAL I_{DD} CURRENT @ V_{DD} = 3.3V, +25°C

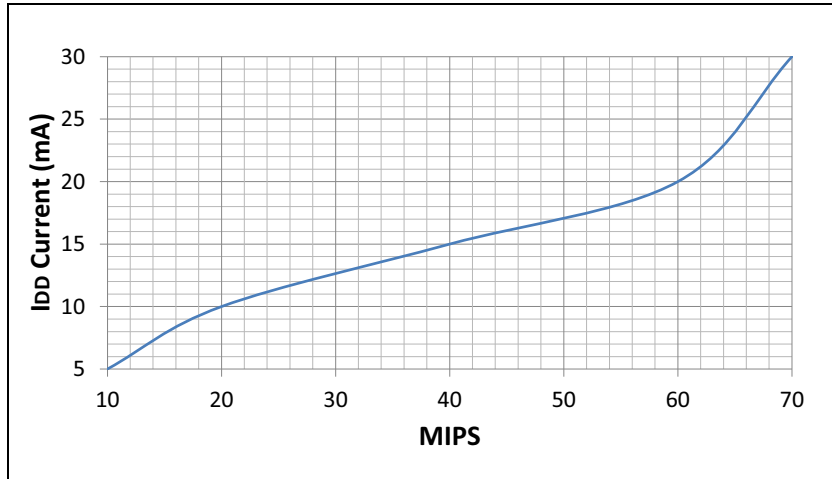


FIGURE 26-8: TYPICAL I_{IDLE} CURRENT @ V_{DD} = 3.3V, +25°C

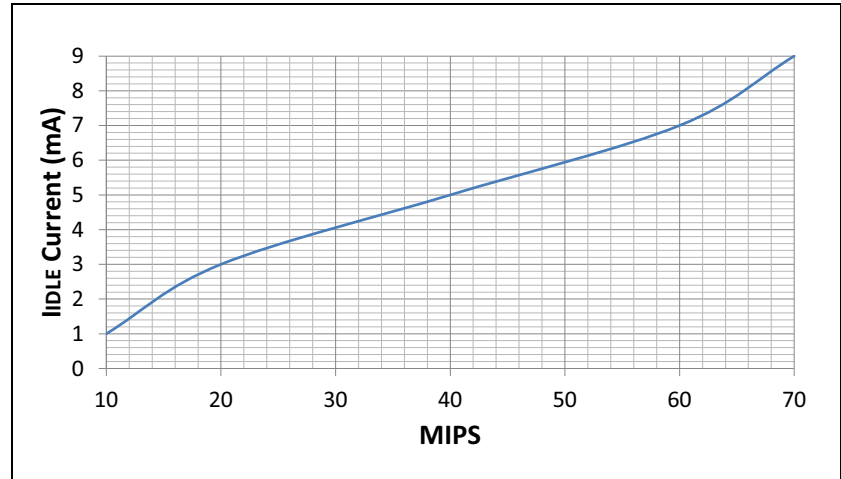


FIGURE 26-9: TYPICAL FRC FREQUENCY @ V_{DD} = 3.3V

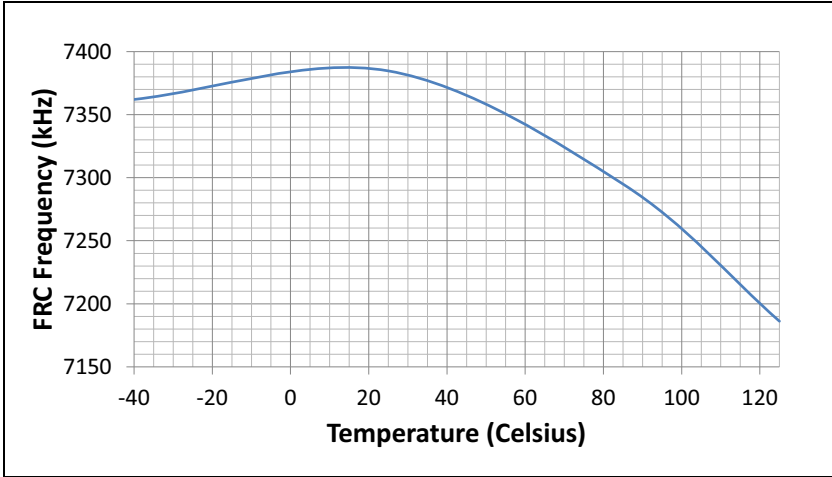
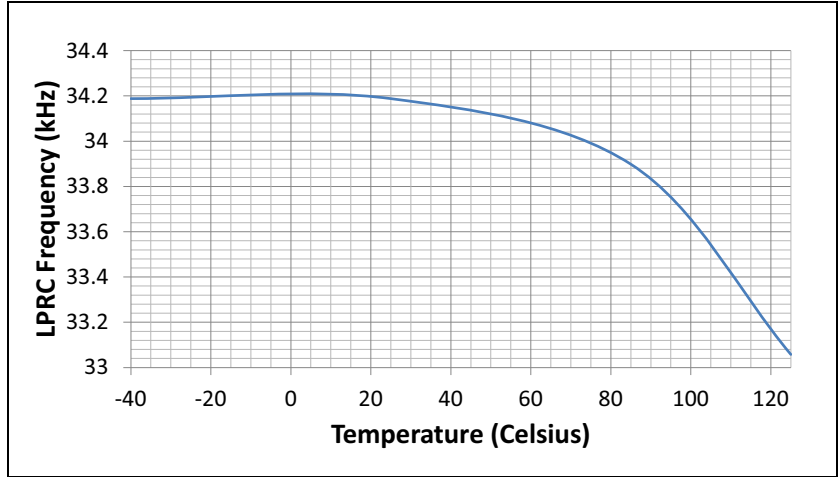


FIGURE 26-10: TYPICAL LPRC FREQUENCY @ V_{DD} = 3.3V



dsPIC33EPXXGS202 FAMILY

NOTES:

dsPIC33EPXXGS202 FAMILY

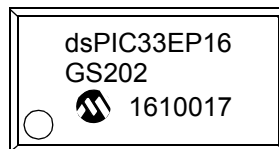
27.0 PACKAGING INFORMATION

27.1 Package Marking Information

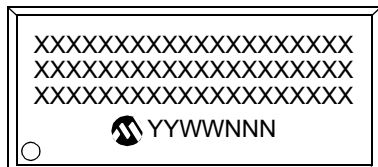
28-Lead SSOP



Example



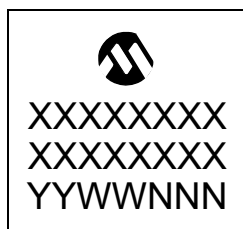
28-Lead SOIC (.300")



Example



28-Lead UQFN (4x4x0.6 mm)



Example



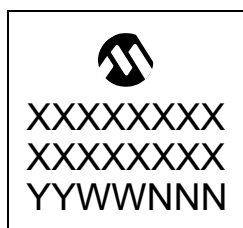
28-Lead UQFN (6x6x0.5 mm)



Example



28-Lead QFN-S (6x6x0.9 mm)



Example



Legend: XX...X Customer-specific information
 Y Year code (last digit of calendar year)
 YY Year code (last 2 digits of calendar year)
 WW Week code (week of January 1 is week '01')
 NNN Alphanumeric traceability code

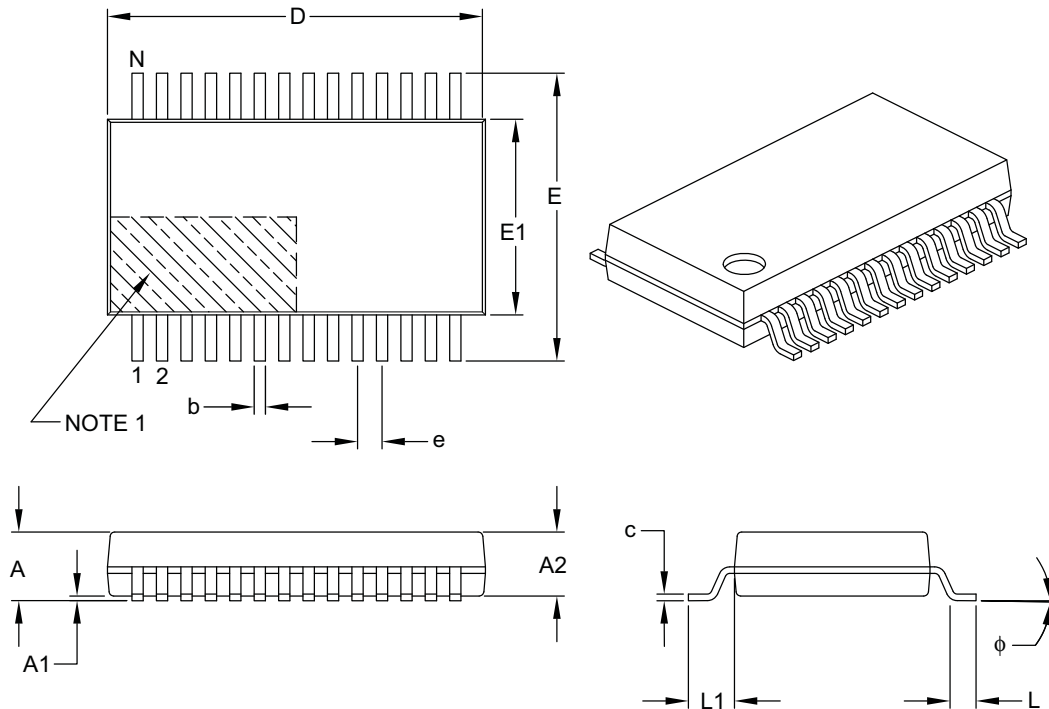
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

dsPIC33EPXXGS202 FAMILY

27.2 Package Details

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|--------|-------------|-------|-------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | – | – | 2.00 |
| Molded Package Thickness | A2 | 1.65 | 1.75 | 1.85 |
| Standoff | A1 | 0.05 | – | – |
| Overall Width | E | 7.40 | 7.80 | 8.20 |
| Molded Package Width | E1 | 5.00 | 5.30 | 5.60 |
| Overall Length | D | 9.90 | 10.20 | 10.50 |
| Foot Length | L | 0.55 | 0.75 | 0.95 |
| Footprint | L1 | 1.25 REF | | |
| Lead Thickness | c | 0.09 | – | 0.25 |
| Foot Angle | ϕ | 0° | 4° | 8° |
| Lead Width | b | 0.22 | – | 0.38 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

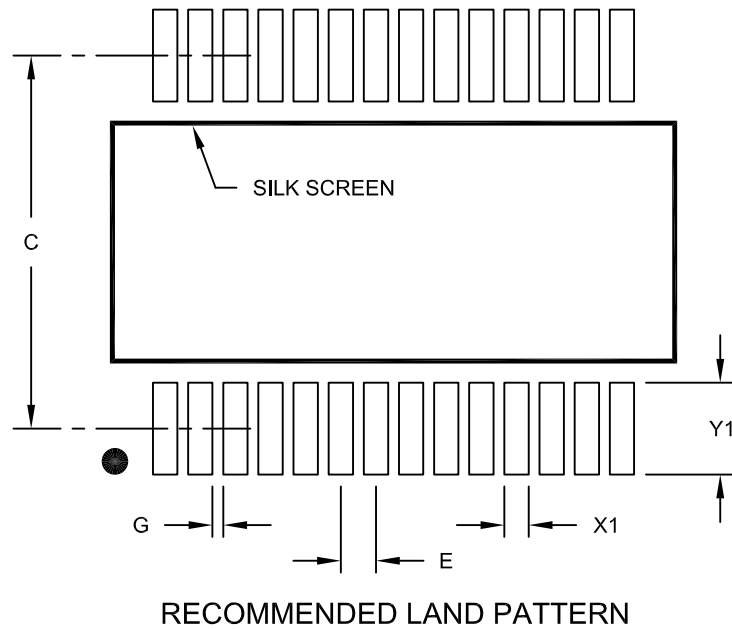
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

dsPIC33EPXXGS202 FAMILY

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 7.20 | |
| Contact Pad Width (X28) | X1 | | | 0.45 |
| Contact Pad Length (X28) | Y1 | | | 1.75 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

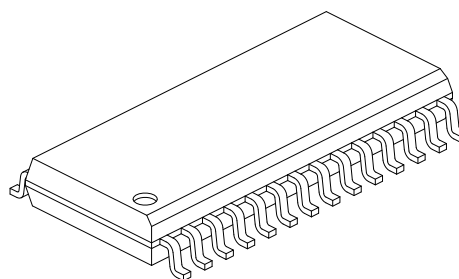
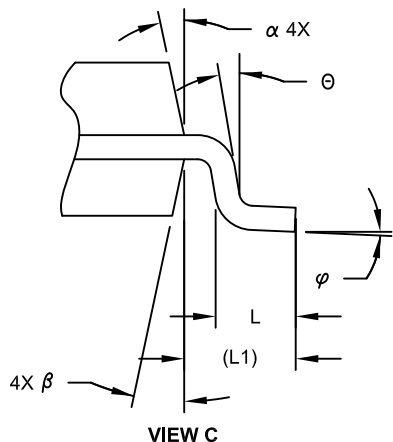
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

dsPIC33EPXXGS202 FAMILY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|-----------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | - | - | 2.65 |
| Molded Package Thickness | A2 | 2.05 | - | - |
| Standoff § | A1 | 0.10 | - | 0.30 |
| Overall Width | E | 10.30 BSC | | |
| Molded Package Width | E1 | 7.50 BSC | | |
| Overall Length | D | 17.90 BSC | | |
| Chamfer (Optional) | h | 0.25 | - | 0.75 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | 1.40 REF | | |
| Lead Angle | θ | 0° | - | - |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.18 | - | 0.33 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

Notes:

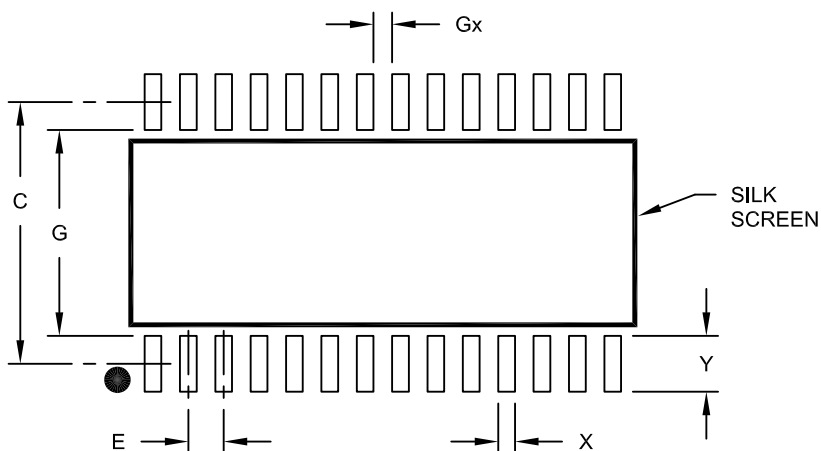
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

dsPIC33EPXXGS202 FAMILY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 9.40 | |
| Contact Pad Width (X28) | X | | | 0.60 |
| Contact Pad Length (X28) | Y | | | 2.00 |
| Distance Between Pads | Gx | 0.67 | | |
| Distance Between Pads | G | 7.40 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

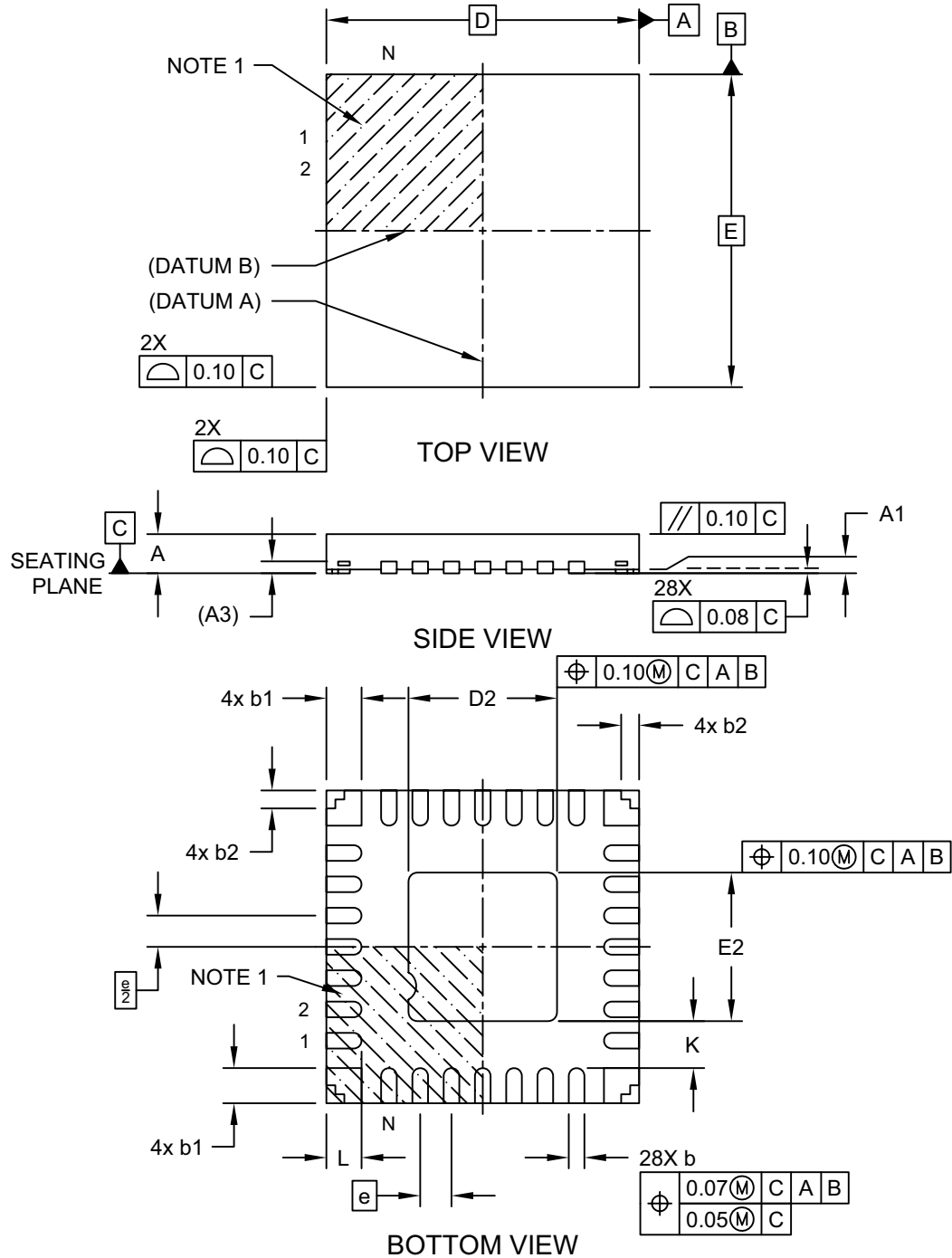
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

dsPIC33EPXXGS202 FAMILY

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

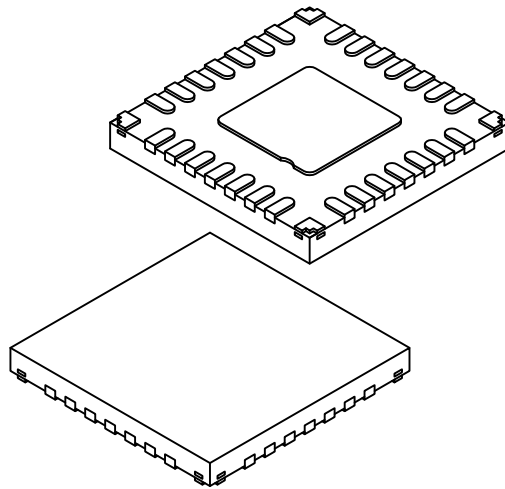


Microchip Technology Drawing C04-333-M6 Rev B Sheet 1 of 2

dsPIC33EPXXGS202 FAMILY

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|-----------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 0.40 BSC | | |
| Overall Height | A | - | - | 0.60 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | 0.152 REF | | |
| Overall Width | E | 4.00 BSC | | |
| Exposed Pad Width | E2 | 1.80 | 1.90 | 2.00 |
| Overall Length | D | 4.00 BSC | | |
| Exposed Pad Length | D2 | 1.80 | 1.90 | 2.00 |
| Terminal Width | b | 0.15 | 0.20 | 0.25 |
| Corner Anchor Pad | b1 | 0.40 | 0.45 | 0.50 |
| Corner Pad, Metal Free Zone | b2 | 0.18 | 0.23 | 0.28 |
| Terminal Length | L | 0.30 | 0.45 | 0.50 |
| Terminal-to-Exposed-Pad | K | - | 0.60 | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

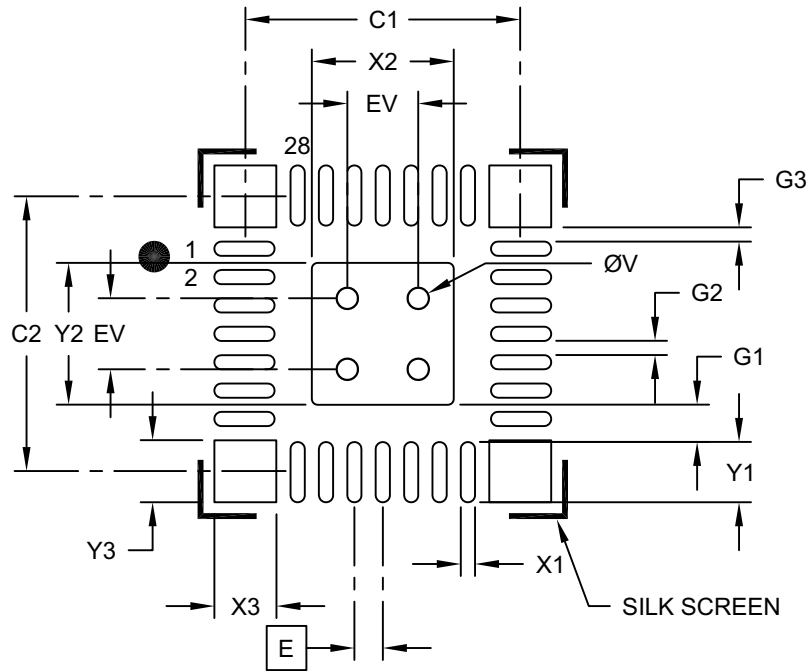
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-333-M6 Rev A Sheet 2 of 2

dsPIC33EPXXGS202 FAMILY

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|---------------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.40 BSC | | |
| Center Pad Width | X2 | | | 2.00 |
| Center Pad Length | Y2 | | | 2.00 |
| Contact Pad Spacing | C1 | | 3.90 | |
| Contact Pad Spacing | C2 | | 3.90 | |
| Contact Pad Width (X28) | X1 | | | 0.20 |
| Contact Pad Length (X28) | Y1 | | | 0.85 |
| Contact Pad to Center Pad (X28) | G1 | | 0.52 | |
| Contact Pad to Pad (X24) | G2 | 0.20 | | |
| Contact Pad to Corner Pad (X8) | G3 | 0.20 | | |
| Corner Anchor Width (X4) | X3 | | | 0.78 |
| Corner Anchor Length (X4) | Y3 | | | 0.78 |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

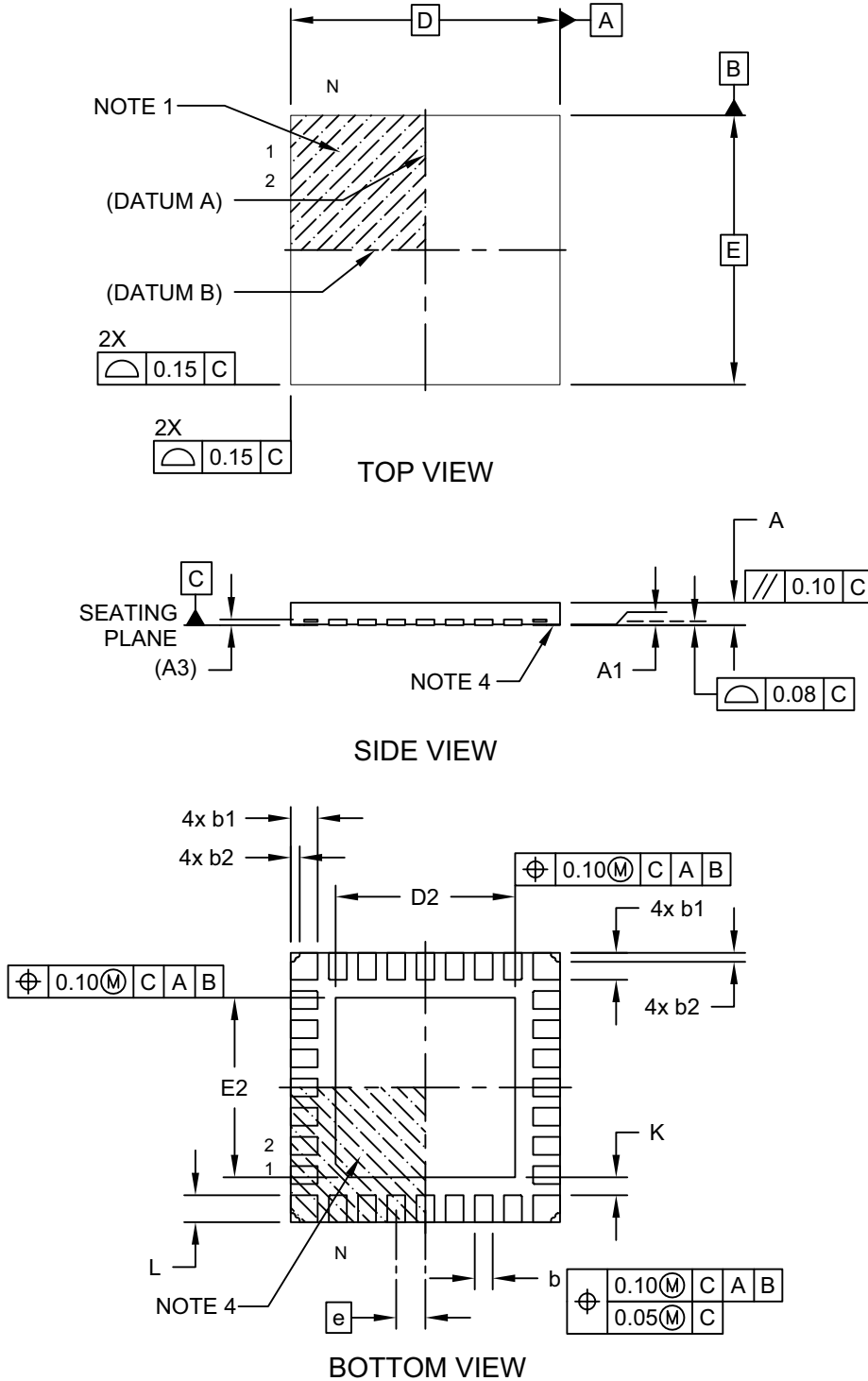
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2333-M6 Rev B

dsPIC33EPXXGS202 FAMILY

28-Lead Plastic Quad Flat, No Lead Package (MX) - 6x6x0.5mm Body [UQFN] Ultra-Thin with 0.40 x 0.60 mm Terminal Width/Length and Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

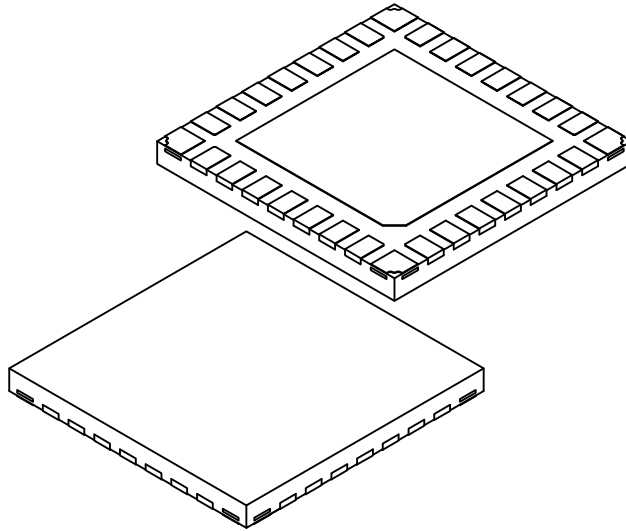


Microchip Technology Drawing C04-0209 Rev C Sheet 1 of 2

dsPIC33EPXXGS202 FAMILY

28-Lead Plastic Quad Flat, No Lead Package (MX) - 6x6x0.5mm Body [UQFN] Ultra-Thin with 0.40 x 0.60 mm Terminal Width/Length and Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|-----------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | 0.40 | 0.50 | 0.60 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | (A3) | 0.127 REF | | |
| Overall Width | E | 6.00 BSC | | |
| Exposed Pad Width | E2 | | 4.00 | |
| Overall Length | D | 6.00 BSC | | |
| Exposed Pad Length | D2 | | 4.00 | |
| Terminal Width | b | 0.35 | 0.40 | 0.45 |
| Corner Pad | b1 | 0.55 | 0.60 | 0.65 |
| Corner Pad, Metal Free Zone | b2 | 0.15 | 0.20 | 0.25 |
| Terminal Length | L | 0.55 | 0.60 | 0.65 |
| Terminal-to-Exposed Pad | K | 0.20 | - | - |

Notes:

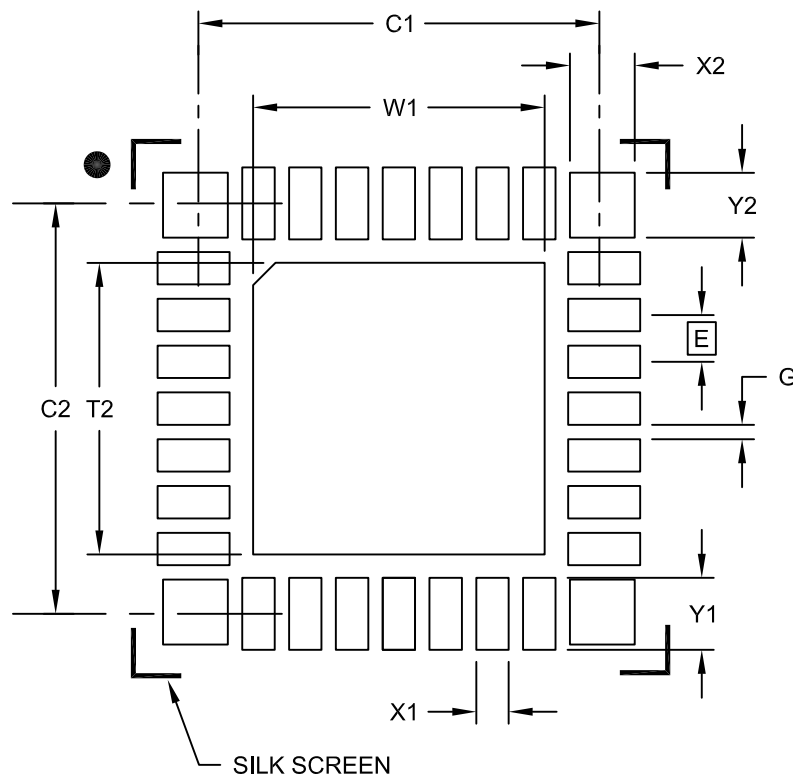
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Outermost portions of corner structures may vary slightly.

Microchip Technology Drawing C04-0209 Rev C Sheet 2 of 2

dsPIC33EPXXGS202 FAMILY

28-Lead Plastic Quad Flat, No Lead Package (MX) - 6x6 mm Body [UQFN] With 0.60mm Contact Length And Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|----------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Optional Center Pad Width | W1 | | | 4.05 |
| Optional Center Pad Length | T2 | | | 4.05 |
| Contact Pad Spacing | C1 | | 5.70 | |
| Contact Pad Spacing | C2 | | 5.70 | |
| Contact Pad Width (X28) | X1 | | | 0.45 |
| Contact Pad Length (X28) | Y1 | | | 1.00 |
| Corner Pad Width (X4) | X2 | | | 0.90 |
| Corner Pad Length (X4) | Y2 | | | 0.90 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

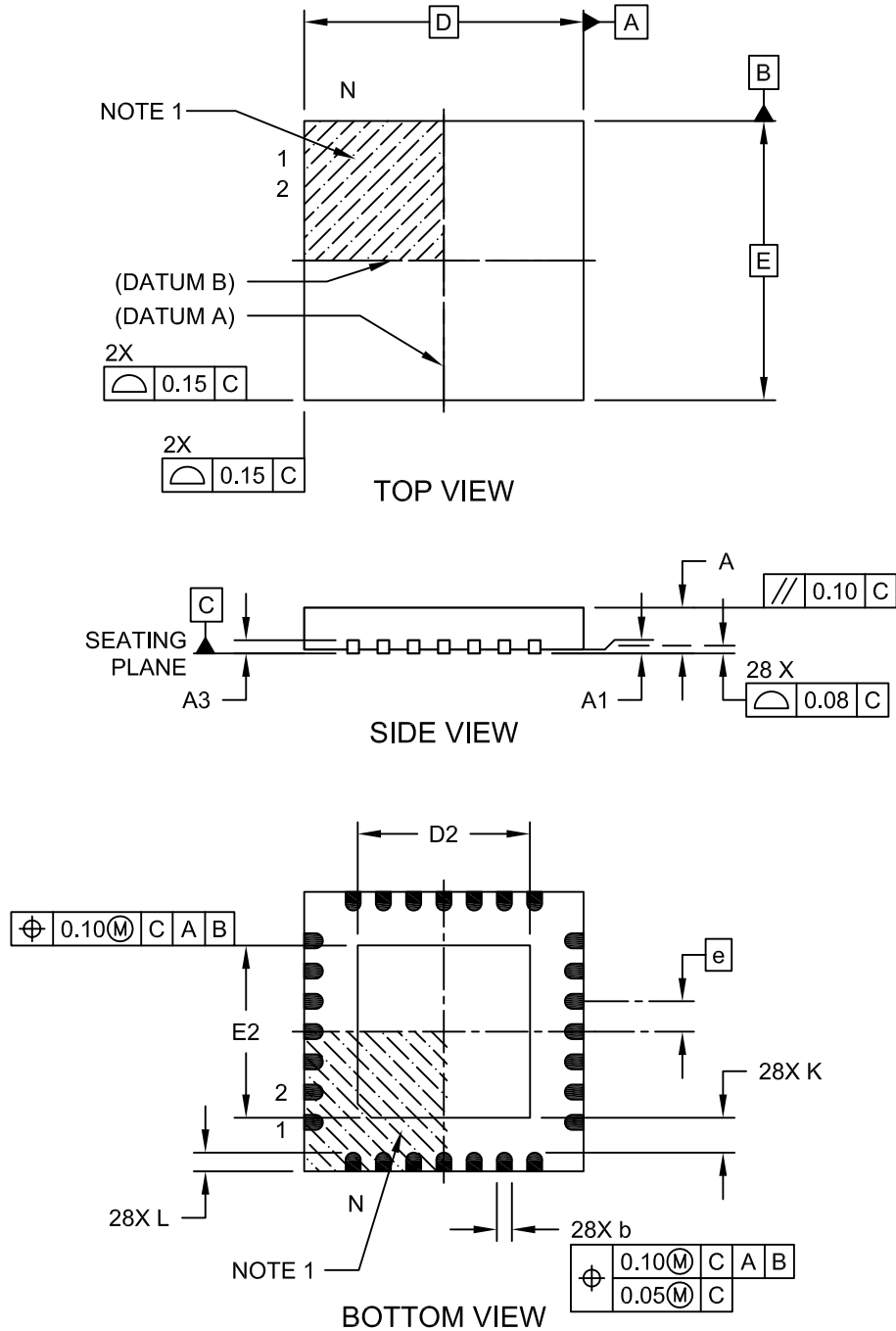
Microchip Technology Drawing No. C04-2209B

Note: Corner anchor pads are not connected internally and are designed as mechanical features when the package is soldered to the PCB.

dsPIC33EPXXGS202 FAMILY

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

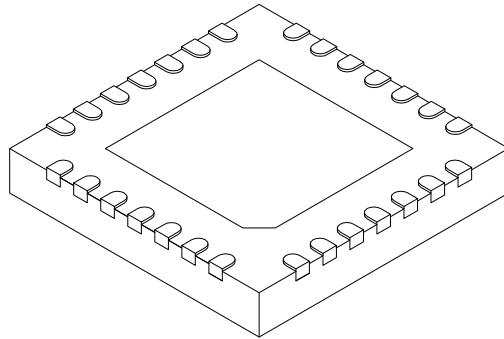


Microchip Technology Drawing C04-124C Sheet 1 of 2

dsPIC33EPXXGS202 FAMILY

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | 0.20 REF | | |
| Overall Width | E | 6.00 BSC | | |
| Exposed Pad Width | E2 | 3.65 | 3.70 | 4.70 |
| Overall Length | D | 6.00 BSC | | |
| Exposed Pad Length | D2 | 3.65 | 3.70 | 4.70 |
| Terminal Width | b | 0.23 | 0.30 | 0.35 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

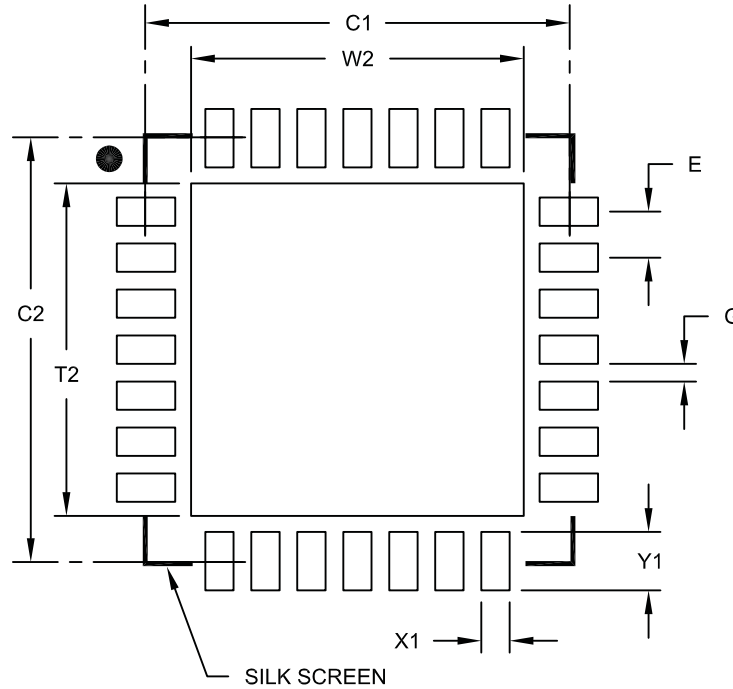
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124C Sheet 2 of 2

dsPIC33EPXXGS202 FAMILY

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|----------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Optional Center Pad Width | W2 | | | 4.70 |
| Optional Center Pad Length | T2 | | | 4.70 |
| Contact Pad Spacing | C1 | | 6.00 | |
| Contact Pad Spacing | C2 | | 6.00 | |
| Contact Pad Width (X28) | X1 | | | 0.40 |
| Contact Pad Length (X28) | Y1 | | | 0.85 |
| Distance Between Pads | G | 0.25 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

dsPIC33EPXXGS202 FAMILY

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (January 2015)

This is the initial version of this document.

Revision B (May 2015)

Changes to [Register 19-7](#) ADCON4L.

Changes to the hysteresis values in [Section 20.6 “Hysteresis”](#) and [Register 20-1](#) CMPxCON.

A note has been added to [Table 23-2](#) Instruction Set Overview.

Changes to [Section 25.0 “Electrical Characteristics”](#).

New packaging diagrams have been added to [Section 27.0 “Packaging Information”](#).

Minor text edits throughout document.

Revision C (November 2015)

Changes for this revision of the document have been effected in the following:

- Adds:
 - [Section 4.2 “Unique Device Identifier \(UDID\)”](#)
- Removes:
 - [Table 4-21](#): JTAG Interface Register Map
- Updates and modifies:
 - Tables:
 - [Table 4-3](#); [Table 4-14](#); [Table 4-17](#); [Table 22-1](#);
 - [Table 25-6](#); [Table 25-8](#); [Table 25-9](#); [Table 25-13](#);
 - [Table 25-43](#); [Table 25-45](#); [Table 25-46](#)
 - Figures:
 - [Figure 19-1](#); [Figure 19-2](#); [Figure 19-3](#)
 - Registers:
 - [Register 19-16](#); [Register 19-22](#); [Register 19-23](#)
- Replaces:
 - [Register 19-20](#)
 - Three revised drawings of 28-Lead Ultra Thin Plastic Quad Flat (M6) 4x4x0.6 mm Body in [Section 27.0 “Packaging Information”](#)

Revision D (May 2016)

This revision of the document:

- Adds a new chapter [Section 26.0 “DC and AC Device Characteristics Graphs”](#)
- Updates [Table 25-2](#) and [Register 19-23](#)
- Modifies the [“Qualification and Class B Support”](#) section
- Provides the family device number in [Section 4.2 “Unique Device Identifier \(UDID\)”](#)
- Wherever applicable, changes occurrences of PWMx to PWM

Revision E (April 2018)

This revision of the document adds all the Data Sheet Clarifications listed in the *“dsPIC33EPXXGS202 Family Silicon Errata and Data Sheet Clarification”* (DS80000655), along with the following updates:

- Registers:
 - Adds Note to [Register 8-4](#).
 - Updates [Register 19-1](#), [Register 19-13](#), [Register 19-14](#), [Register 19-15](#), [Register 19-18](#), [Register 19-19](#), [Register 19-22](#), [Register 19-23](#), [Register 19-24](#), [Register 19-25](#) and [Register 19-26](#).
- Tables:
 - Adds [Table 25-42](#).
 - Updates [Table 1-1](#), [Table 4-3](#), [Table 4-14](#), [Table 7-1](#), [Table 25-4](#), [Table 25-12](#), [Table 25-40](#), [Table 25-43](#) and [Table 25-46](#).
- Figures:
 - Updates [Pin Diagrams](#), [Figure 19-1](#), [Figure 19-3](#) and [Figure 25-22](#).

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NOTES:

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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| dsPIC 33 EP XX GS2 02 T - I / PT XXX | |
|--------------------------------------|-------|
| Microchip Trademark | _____ |
| Architecture | _____ |
| Flash Memory Family | _____ |
| Program Memory Size (Kbyte) | _____ |
| Product Group | _____ |
| Pin Count | _____ |
| Tape and Reel Flag (if applicable) | _____ |
| Temperature Range | _____ |
| Package | _____ |
| Pattern | _____ |

Examples:
dsPIC33EP32GS202-I/SS:
dsPIC33, Enhanced Performance,
32-Kbyte Program Memory, SMPS,
28-Pin, Industrial Temperature,
SSOP Package.

| | |
|-----------------------------|--|
| Architecture: | 33 = 16-Bit Digital Signal Controller |
| Flash Memory Family: | EP = Enhanced Performance |
| Product Group: | GS = SMPS Family |
| Pin Count: | 02 = 28-pin |
| Temperature Range: | I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended) |
| Package: | MM = Plastic Quad, No Lead Package – (28-pin) 6x6 mm body (QFN-S) M6 = Plastic Quad Flat, No Lead Package – (28-pin) 4x4x0.6 mm body (UQFN) MX = Plastic Quad Flat, No Lead Package – (28-pin) 6x6x0.5 mm body (UQFN) SO = Plastic Small Outline, Wide – (28-pin) 7.50 mm body (SOIC) SS = Plastic Shrink Small Outline – (28-pin) 5.30 mm body (SSOP) |

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NOTES:

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