ECE1088

GPIO Expansion via SMBus or BC-Link Bus

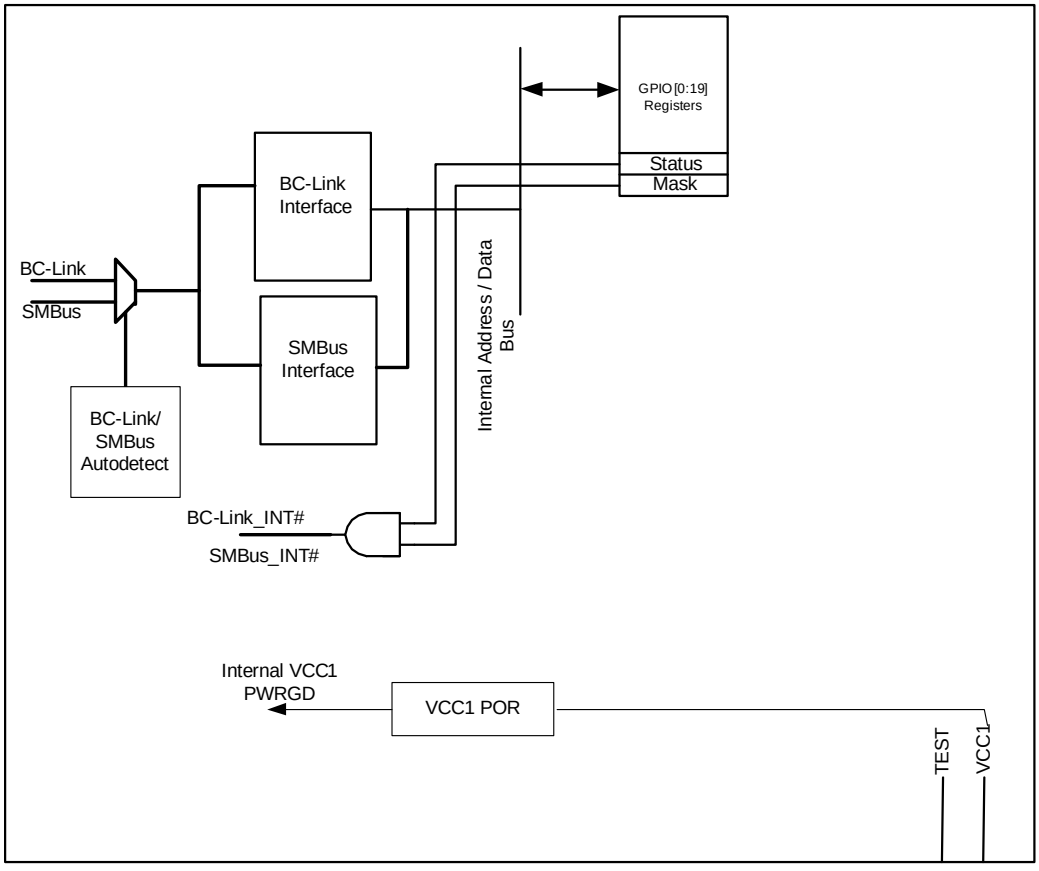
Highlights

The ECE1088 is a 28-Pin 3.3V GPIO Expansion device. The device is connected to a Master via the BC-Link interface or via the SMBus.

Features

- 20 Multiplexed General Purpose I/O pins
  - All are MCU addressable I/O Pins
- BC-Link Interconnect Bus
  - Link to embedded controller
- SMBus Interconnect
  - One of two address selection
- 3.3V Operation
  - 28-Pin, QFN RoHS Compliant package
  - 0.5mm Pitch
  - 5x5mm Body size

Block Diagram



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1.0 PIN FUNCTIONS

TABLE 1-1: ECE1088 PIN TABLE

Pin #	Name	Pin #	Name
1	GPIO13	15	GPIO36
2	GPIO14	16	GPIO37
3	GPIO15	17	GPIO00
4	GPIO16	18	GPIO01
5	GPIO17	19	GPIO02
6	GPIO20	20	GPIO03
7	VCC1	21	VCC1
8	GPIO24	22	BC_DAT/SMB_DATA
9	GPIO25	23	BC_CLK/SMB_CLK
10	GPIO26	24	BC_INT#/SMB_INT#
11	GPIO27	25	SMB_ADDR
12	GPIO30	26	GPIO07
13	GPIO31	27	RESERVED
14	GPIO32	28	TEST_PIN

FIGURE 1-1: ECE1088 PIN DIAGRAM (TOP VIEW, EXPOSED PAD IS ON THE BOTTOM)

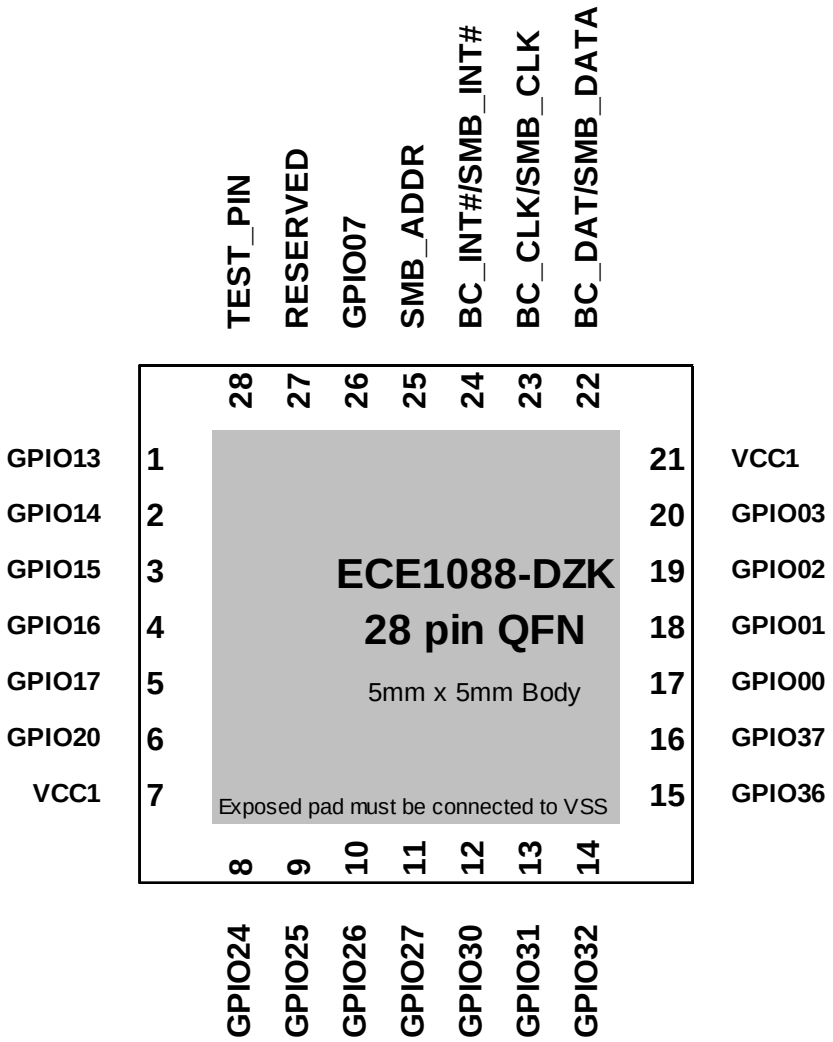


TABLE 1-2: ECE1088 PIN DESCRIPTIONS

Pin #	Name	Description	Buffer	Notes
1	GPIO13	General Purpose IO.	ISP/O8	3
2	GPIO14	General Purpose IO.	ISP/O8	3
3	GPIO15	General Purpose IO.	ISP/O8	3
4	GPIO16	General Purpose IO.	ISP/O8	3
5	GPIO17	General Purpose IO.	ISP/O8	3
6	GPIO20	General Purpose IO.	IP/O8	3
7	VCC1	PWR	PWR	
8	GPIO24	General Purpose IO.	IP/O8	3
9	GPIO25	General Purpose IO.	IP/O8	3
10	GPIO26	General Purpose IO.	IP/O8	3
11	GPIO27	General Purpose IO.	IP/O8	3
12	GPIO30	General Purpose IO.	IP/O8	3
13	GPIO31	General Purpose IO.	IP/O8	3
14	GPIO32	General Purpose IO.	IP/O8	3
15	GPIO36	General Purpose IO.	IP/O8	3
16	GPIO37	General Purpose IO.	IP/O8	3
17	GPIO00	General Purpose IO.	IP/O8	3
18	GPIO01	General Purpose IO.	IP/O8	3
19	GPIO02	General Purpose IO.	IP/O8	3

Pin #	Name	Description	Buffer	Notes
20	**GPIO03**	General Purpose IO.	IP/O8	3
21	**VCC1**	PWR	PWR	
22	BC_DAT/SMB_DATA	BC_DAT IO. SMBus Data IO	I/O8	
23	BC_CLK/SMB_CLK	BC_CLK. SMBus Slave Clock I	I	
24	BC_INT#/SMB_INT#	BCINT#t Output Active Low . SMBus Interrupt Output Active Low	O8	4
25	SMB_ADDR	SMBus Address Select Strap. Selects between one of two SMBus Slave Addresses	I	
26	GPIO07	General Purpose IO.	IP/O8	3
27	RESERVED	Reserved	NC	2
28	TEST_PIN	Test Pin Input	I	1
Exposed pad must be connected to VSS				

Note 1: This pin requires an external pull-down resister to ensure that the pin remains de-asserted.

2: NC Not Connected.

3: Full Function GPIO Refer to Table 2-4, "GPIO Configuration Register".

4: SMB_INT# is Open Drain / BC_INT# is Push-pull. SMBus is default.

TABLE 1-3: ALTERNATE PIN FUNCTIONS

Pin #	Primary	Alternate
1	GPIO13	
2	GPIO14	
3	GPIO15	
4	GPIO16	
5	GPIO17	
6	GPIO20	
7	VCC1	
8	GPIO24	
9	GPIO25	
10	GPIO26	
11	GPIO27	
12	GPIO30	
13	GPIO31	
14	GPIO32	
15	GPIO36	
16	GPIO37	
17	GPIO00	
18	GPIO01	
19	GPIO02	
20	GPIO03	
21	VCC1	
22	BC_DAT	SMB_DATA
23	BC_CLK	SMB_CLK
24	BC_INT#	SMB_INT#
25	SMB_ADDR	
26	GPIO07	
27	RESERVED	
28	TEST_PIN	

1.1 XNOR Chain Test Mode

An XNOR Chain test structure is in to the ECE1088 to allow users to confirm that all pins are in contact with the motherboard during assembly and test operations (Figure 1-2, "XNOR Chain Test Structure").

The XNOR Chain test structure must be activated to perform these tests. When the XNOR Chain is activated, the ECE1088 pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR Chain.

The tests that are performed when the XNOR Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR Chain output pin.

1.2 Pins in XNOR Chain Structure

All pins are inputs into the XNOR Chain with the exception of the following pins:

- TEST_PIN (this is the XNOR Chain enable input)
- RESERVED
- SMB_ADDR
- BC_INT#/SMB_INT#

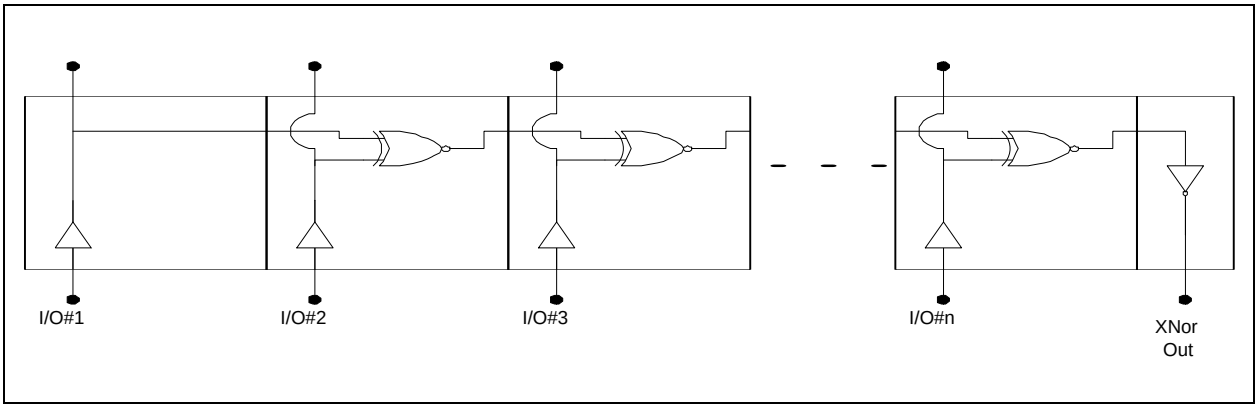
1.3 Entering and Exiting the XNOR Chain

The XNOR Chain test is entered by setting TEST_PIN to 1 while SMB_ADDR is 0.

When activated, the test mode allows one single input pin, when switched, to toggle the BC_INT#/SMB_INT# output.

The XNOR Chain is exited by setting TEST_PIN to 0, independent of the value of SMB_ADDR.

FIGURE 1-2: XNOR CHAIN TEST STRUCTURE



2.0 PRODUCT DESCRIPTION

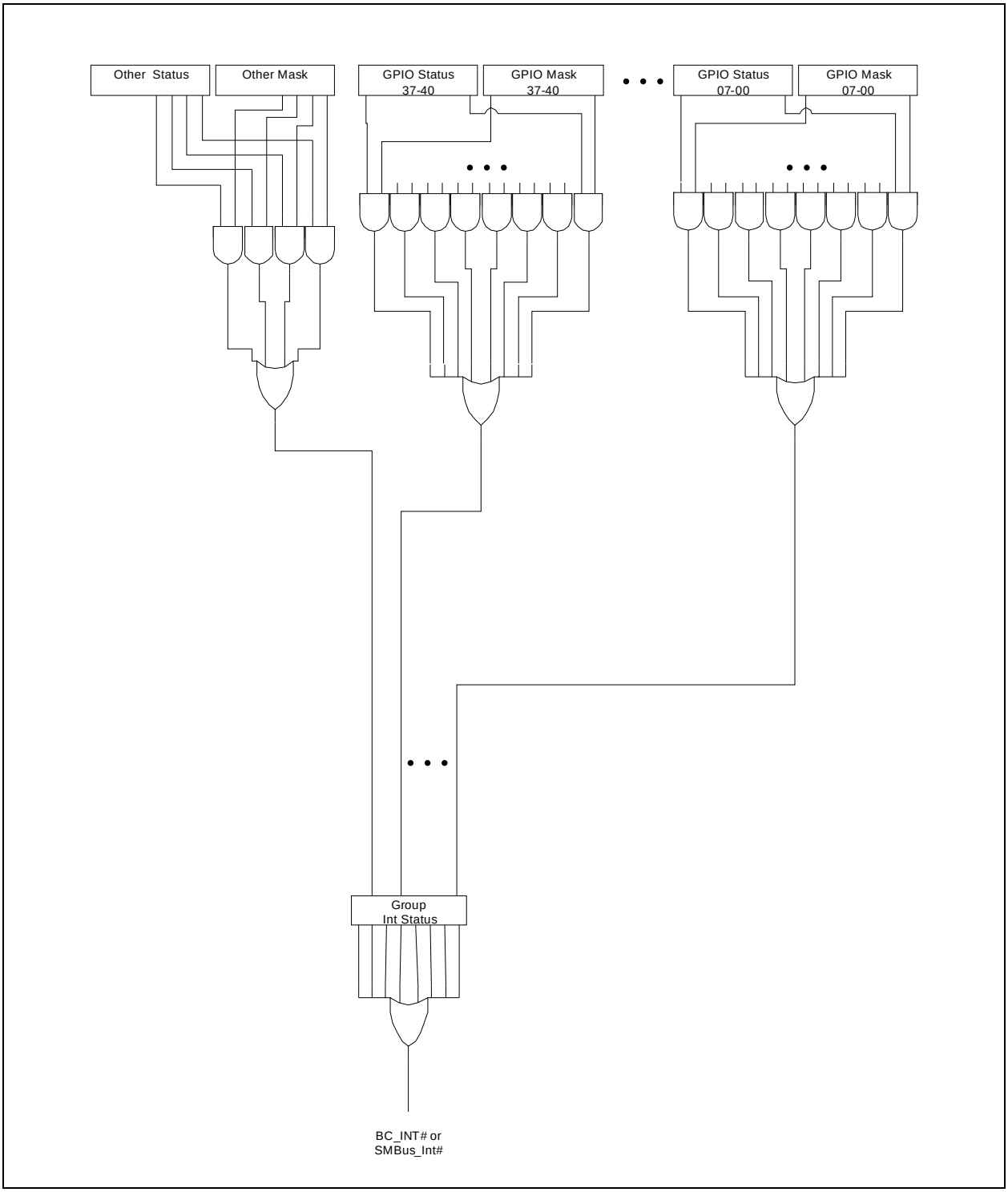
2.1 Summary

The ECE1088 is a 28-pin 3.3V GPIO Expansion device. The device is connected to a Master via the BC-Link interface or via the SMBus.

2.2 Interrupt Generation

Interrupts can be generated by an edge detection on a GPIO pin or an edge detection on one of the bus interface pins. The bus interrupt pin (BC_INT# or SMBUS_INT#) is asserted if any bit in one of the Interrupt Status registers is 1 and the corresponding Interrupt Mask bit is also 1. Interrupt generation is illustrated in Figure 2-1, "ECE1088 Interrupt Generation".

FIGURE 2-1: ECE1088 INTERRUPT GENERATION



In order for software to determine which device is the source of an interrupt, it should first read the Group Interrupt Status Register to determine which Status register group is a source for the interrupt. Software should read both the Status register and the associated Mask register, then AND the two values together. Bits that are 1 in the result of the AND are active interrupts.

Software clears an interrupt by writing a 1 to the corresponding bit in the Status register.

Note:	Although the ECE1088 can generate the SMBus interrupt signal SMBUS_INT# as described above, it will not respond to the SMBus Alert Response Address transaction unless Bit4 ARA in the Clock Control Register (Register FAh) is set to 1.

2.3 Integrated VCC1 Reset Generator

When VCC1 power is applied to the ECE1088, a VCC1 POR will be generated. This VCC1 POR will reset the device.

2.4 Register Address Table

TABLE 2-1: REGISTER SUMMARY

Address (HEX)	Register	VCC1 POR Default
00h	GPIO[7, 3:0] Input	00h
01h	GPIO[17:13] Input	00h
02h	GPIO[27,24:20] Input	00h
03h	GPIO[37:36,32:30] Input	00h
04h	Reserved	00h
05h	GPIO[7,3:0] Output	00h
06h	GPIO[17:10] Output	00h
07h	GPIO[27:24,20] Output	00h
08h	GPIO[37:36,32:30] Output	00h
09h	Reserved	00h
0Ah	GPIO00 Configuration	00h
0Bh	GPIO01 Configuration	00h
0Ch	GPIO02 Configuration	00h
0Dh	GPIO03 Configuration	00h
0E-10h	Reserved	00h
11h	GPIO07 Configuration	00h
12-14h	Reserved	00h
15h	GPIO13 Configuration	00h
16h	GPIO14 Configuration	00h
17h	GPIO15 Configuration	00h
18h	GPIO16 Configuration	00h
19h	GPIO17 Configuration	00h
1Ah	GPIO20 Configuration	00h
1B-1Dh	Reserved	00h
1Eh	GPIO24 Configuration	00h
1Fh	GPIO25 Configuration	00h
20h	GPIO26 Configuration	00h
21h	GPIO27 Configuration	00h
22h	GPIO30 Configuration	00h
23h	GPIO31 Configuration	00h

TABLE 2-1: REGISTER SUMMARY (CONTINUED)

Address (HEX)	Register	VCC1 POR Default
24h	GPIO32 Configuration	00h
25-27h	Reserved	00h
28h	GPIO36 Configuration	00h
29h	GPIO37 Configuration	00h
2A-31h	Reserved	00h
32h	GPIO[7,3:0] Interrupt Status	00h
33h	GPIO[17:13] Interrupt Status	00h
34h	GPIO[27:24.20] Interrupt Status	00h
35h	GPIO[37:36,32:30]Interrupt Status	00h
36h	Reserved	00h
37h	GPIO[7,3:0] Interrupt Mask	00h
38h	GPIO[17:13] Interrupt Mask	00h
39h	GPIO[27:24,20] Interrupt Mask	00h
3Ah	GPIO[37:36,32:30] Interrupt Mask	00h
3B-F4h	Reserved	00h
F5h	Reset	00h
F6h	MCHP test	00h
F7h-F8h	Reserved	00h
F9h	Group Interrupt	00h
FAh	Clock Control	00h
FBh	Wakeup Control	00h
FCH	Device ID	40h
FDh	Device Version Number	Current version
FEh	Vendor ID (LSB)	55h
FFh	Vendor ID (MSB)	10h

2.5 Detailed Register Descriptions

2.5.1 GPIO REGISTERS

2.5.2 GPIO INPUT REGISTER

TABLE 2-2: GPIO INPUT REGISTER

ADDRESS	**REFER TO** Table 2-1, "Register Summary"			8-bit			**SIZE**
POWER	VCC1			N/A			**VCC1 POR DEFAULT**
BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BC-LINK TYPE	R	R	R	R	R	R	R	R
BIT NAME	GPIOx7	GPIOx6	GPIOx5	GPIOx4	GPIOx3	GPIOx2	GPIOx1	GPIOx0

2.5.3 GPIO OUTPUT REGISTER

TABLE 2-3: GPIO OUTPUT REGISTER

ADDRESS	REFER TO Table 2-1, "Register Summary"			8-bit			SIZE
POWER	VCC1			00h			VCC1 POR DEFAULT
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	GPIOx7	GPIOx6	GPIOx5	GPIOx4	GPIOx3	GPIOx2	GPIOx1	GPIOx0

2.5.4 GPIO CONFIGURATION REGISTER

TABLE 2-4: GPIO CONFIGURATION REGISTER

ADDRESS	REFER TO Table 2-1, "Register Summary"			8-bit			SIZE
POWER	VCC1			00h			VCC1 POR DEFAULT
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK TYPE	R	R/W	R/W	R/W	R/W	R/W	R	R/W
BIT NAME	RES	ALT	DIR	TYPE		POL	RES	PU

2.5.4.1 ALT

ALT Function select bit should always be set as 0.

2.5.4.2 DIR, TYPE

The level/edge and output type are controlled by these fields. The effects are defined in Table 2-5, "Direction, Level/Edge, Output Type Bit Definition".

TABLE 2-5: DIRECTION, LEVEL/EDGE, OUTPUT TYPE BIT DEFINITION

Direction Bit 5	Type Bit 4	Type Bit 3	Selected Function
0	0	0	Input, Level Sensitive Low
0	0	1	Input, Rising Edge Triggered
0	1	0	Input, Falling Edge Triggered
0	1	1	Input, Both Edge Triggered
1	0	x	Output, Push-Pull
1	1	x	Output, Open Drain

In order to enable oscillator wakeup from Low Power Mode for any GPIO pin, the GPIO Configuration Register for that GPIO must be configured for Input in Bit 5). See Section 2.6.2, "Clock Control".

2.5.4.3 POL

When the **POL** bit is set to '1'' the signal output is inverted when routed to its pin and the interrupt level sense is inverted when a level-sensitive interrupt is selected by the **DIR, TYPE** fields. The state of the pin is always reported without inversion in the GPIO Input Register.

2.5.4.4 PU

When this bit is 1, an internal pull-up resistor is connected to the pin. When this bit is 0, the pullup is disabled.

2.5.5 GPIO INTERRUPT STATUS REGISTER

TABLE 2-6: GPIO INTERRUPT STATUS REGISTER

ADDRESS	**REFER TO** Table 2-1, "Register Summary"			8-bit			**SIZE**
POWER	VCC1			00h			**VCC1 POR DEFAULT**
BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BC-LINK TYPE	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC
BIT NAME	GPIOX7	GPIOX6	GPIOX5	GPIOX4	GPIOX3	GPIOX2	GPIOX1	GPIOX0

A bit in a GPIOX Interrupt Status Register is set to 1 when the DIRECTION field for that bit in the corresponding GPIOX*n* Configuration Register is set for Input and the bit in the corresponding GPIOX Input Register matches the conditions defined by the TYPE field in the GPIOX Configuration Register. For example, if the TYPE field for GPIO X*n* is set for Level Sensitive Low, then bit *n* in the GPIOX Interrupt Status Register is set to 1 when bit *n* in the GPIOX Input Register is 0. If the TYPE field specifies edge triggering, then the Status Register bit is set when the Input Register bit transitions with the specified edge.

Writing a bit in a GPIOX Interrupt Status Register clears that bit. Writing a bit with a 0 has no effect.

2.5.6 GPIO INTERRUPT MASK REGISTER

TABLE 2-7: GPIO INTERRUPT MASK REGISTER

ADDRESS	**REFER TO** Table 2-1, "Register Summary"			8-bit			**SIZE**
POWER	VCC1			00h			**VCC1 POR DEFAULT**
BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BC-LINK TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	GPIOX7 0 No Int 1 Int	GPIOX6 0 No Int 1 Int	GPIOX5 0 No Int 1 Int	GPIOX4 0 No Int 1 Int	GPIOX3 0 No Int 1 Int	GPIOX2 0 No Int 1 Int	GPIOX1 0 No Int 1 Int	GPIOX0 0 No Int 1 Int

An interrupt is signaled on either BC_INT# or SMBus_INT# when a GPIOX bit in a GPIO Interrupt Status Register is 1 and the corresponding GPIOX bit in the GPIO Interrupt Mask Register is also 1.

2.6 Other Control Registers

2.6.1 GROUP INTERRUPT STATUS

TABLE 2-8: GROUP INTERRUPT STATUS REGISTER

ADDRESS	F9h			8-bit			SIZE
POWER	VCC1			00h			VCC1 POR DEFAULT
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK TYPE	R	R	R	R	R	R	R	R
BIT NAME	Reserved	Reserved	Reserved	Reserved	Grp3	Grp2	Grp1	Grp0

2.6.1.1 Bit3 Grp3

0 No interrupts in GPIO Group 3

1 Interrupt in at least one of GPIO37-GPIO30

2.6.1.2 Bit2 Grp2

0 No interrupts in GPIO Group2

1 Interrupt in at least one of GPIO27-GPIO20

2.6.1.3 Bit1 Grp1

0 No interrupts in GPIO Group1

1 Interrupt in at least one of GPIO17-GPIO10

2.6.1.4 Bit0 Grp0

0 No interrupts in GPIO Group0

1 Interrupt in at least one of GPIO07-GPIO00

2.6.2 CLOCK CONTROL

TABLE 2-9: CLOCK CONTROL REGISTER

ADDRESS	FAh			8-bit			SIZE	
POWER	VCC1			00h			VCC1 POR DEFAULT	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK TYPE	R	R	R	R/W	R/W	R/W	R/W	R/W
BIT NAME	Reserved			ARA	Reserved	OSC Control	Interface Selection	

2.6.2.1 Bit4 ARA

If this bit is 1b and the SMBus interface is enabled (either by setting the Interface Selection field to 11b or by setting the Interface Selection field to 0xb and an SMBus transaction is detected), the ECE1088 will respond to an SMBus Alert Response Address Read Byte command as defined in the SMBus specification. If this bit is 0b, the ECE1088 will ignore the Alert Response Address at all times.

APPLICATION NOTE: Software must insure that the field Interface Selection in this register is ‘11b’ (SMBus Interface enabled) before setting ARA to ‘1b’.

2.6.2.2 Bit2 OSC Control

0b Oscillator Enabled (Default)

1b Oscillator Low Power Enable.

The Oscillator may be stopped and once stopped may be restarted by activity on either the bus interface pins or on inputs that are enabled for interrupts. See Section 2.6.3, "Wakeup Control" for conditions that restart the Oscillator

When OSC Control is set to Low Power Enable (1b) the Oscillator will stop only when the SMBus or BC-Link are idle. This means:

No Interrupts are pending

No traffic is on the bus

Transactions on the bus have completed

APPLICATION NOTE: When OSC Control is set to ‘1b’, the ring oscillator will be shut down after every BC-Link or SMBus transaction completes and no interrupts are pending. The oscillator will restart when a wakeup enabled by the Wakeup Control registers occurs. The Wakeup Control register **must** be configured properly before setting OSC Control to ‘1b’.

2.6.2.3 Bit[1:0] Interface Selection

0Xb Autodetect Mode (default)

10b BC-Link interface enabled.

11b SMBus interface enabled

APPLICATION NOTE: The first access to the ECE1088 must be a write to the Clock Control register to configure the Interface Selection field to the desired interface type (10b or 11b). This is required so that Oscillator control works properly and so that the bus type does not inadvertently switch during use.

2.6.3 WAKEUP CONTROL

The Wakeup Control Register determines which events restart the Oscillator when the Oscillator is in Low Power Mode.

TABLE 2-10: WAKEUP CONTROL REGISTER

ADDRESS	**FBh**			8-bit			**SIZE**
POWER	VCC1			00h			**VCC1 POR DEFAULT**
BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BC-LINK TYPE	R	R	R	R	R	R/W	R/W	R/W
BIT NAME	Reserved	Reserved	Reserved	Reserved	Reserved	GPIO	BUS_DAT	BUS_CLK

2.6.3.1 Bit2 GPIO

0 GPIO Interrupts do not affect the Oscillator

1 A GPIO interrupt that is requested on any GPIO pin for which GPIO function is selected and a GPIO interrupt is enabled will restart the Oscillator when the Oscillator is stopped in Low Power mode.

In order for edge detection to work on any GPIO pin the pin must be selected for input and the desired edges configured, as described in Table 2-5, "Direction, Level/Edge, Output Type Bit Definition", in the GPIO configuration register.

2.6.3.2 Bit1 BUS_DAT

0 The BUS_DAT signal (BC_DAT or SMB_DAT) does not affect the Oscillator

1 Either a rising edge or a falling edge on the BUS_DAT signal will restart the Oscillator when the Oscillator is stopped in Low Power mode.

2.6.3.3 Bit0 BUS_CLK

0 The BUS_Clk signal (BC_CLK or SMB_CLK) does not affect the Oscillator

1 Either a rising edge or a falling edge on the BUS_Clk signal will restart the Oscillator when the Oscillator is stopped in Low Power mode.

2.6.4 DEVICE ID REGISTER

TABLE 2-11: DEVICE ID REGISTER

ADDRESS	**FCH**			8-bit			**SIZE**	
POWER	VCC1			40h			**VCC1 POR DEFAULT**	
BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BC-LINK TYPE	R	R	R	R	R	R	R	R
ECE1088	**40h**							

TABLE 2-12: DEVICE REVISION REGISTER

ADDRESS	**FDh**			8-bit			**SIZE**	
POWER	VCC1			00h			**VCC1 POR DEFAULT**	
BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BC-LINK TYPE	R	R	R	R	R	R	R	R
BIT NAME	Current Revision Number							

TABLE 2-13: VENDOR ID (LSB) REGISTER

ADDRESS	**FEh**			8-bit			**SIZE**	
POWER	VCC1			55h			**VCC1 POR DEFAULT**	
BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BC-LINK TYPE	R	R	R	R	R	R	R	R
BIT NAME	55h							

TABLE 2-14: VENDOR ID (MSB) REGISTER

ADDRESS	FFh			8-bit			SIZE	
POWER	VCC1			10h			VCC1 POR DEFAULT	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK TYPE	R	R	R	R	R	R	R	R
BIT NAME	10h							

2.6.5 RESET REGISTER

TABLE 2-15: RESET REGISTER

ADDRESS	F5H			8-bit			SIZE	
POWER	VCC1			00h			VCC1 POR DEFAULT	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK TYPE	R	R	R	R	R	R	R	W
BIT NAME	Reserved							Force_ POR

2.6.5.1 Force_POR

Writing this bit with a 1 will force a VCC1 POR. All registers and state machines in the device will be reset to their default power-on values. Writing a 0 to this bit has no effect. This is a self clearing bit.

Note: The Force_POR bit does not affect the **Interface Selection** setting of the Clock Control register. Whichever bus interface is in effect at the time Force_POR is set (BC-Link or SMBus) will remain in effect after the POR.

2.6.6 MCHP TEST REGISTER

TABLE 2-16: MCHP TEST REGISTER

ADDRESS	F6H			8-bit			SIZE	
POWER	VCC1			00h			VCC1 POR DEFAULT	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK TYPE	R	R	R	R	R	R	R	R
BIT NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

2.6.6.1 RESERVED

Reserved for Microchip test purposes. Should not be written.

2.7 SMBus / BC-Link Autodetect Circuit

2.7.1 OVERVIEW

For either the SMBus or the BC-Link, by detecting difference in start conditions, the Bus type is indicated. From an idle condition, the device will sample the data line on the first falling edge of the clock. If it is low, a SMBus interface is selected; if it is high, a BC-Link interface is selected. The idle condition is defined as a POR or no activity for 75 ms. To safeguard against glitches selecting the wrong bus and locking the system, the device use time-outs that reload on a start from the respective bus interface. For SMBus, the timeout is 75 ms. For BC-Link, the timeout is 75 µs.

2.8 SMBus Slave Interface

The host processor communicates with the ECE1088 device through a series of read/write registers via the SMBus interface. SMBus is a serial communication protocol between a computer host and its peripheral devices.

The SMBus data rate is 10KHz minimum to 400 KHz maximum.

2.8.1 CLOCKING

The SMBus Slave interface is driven by an internal Ring Oscillator. This oscillator runs at a nominal frequency of 32MHz.

The Ring Oscillator may be started and stopped through firmware interactions. The that controls the operation of the Oscillator is described in Section 2.6.2, "Clock Control" and Section 2.6.3, "Wakeup Control".

2.8.2 SLAVE ADDRESS

Upon power up, the ECE1088 device will be placed into Address Select mode and assign itself an SMBus address according to the Address Select input. The device will latch the address during the first valid SMBus transaction in which the first five bits of the targeted address match those of the ECE1088 address. This feature eliminates the possibility of a glitch on the SMBus interfering with address selection.

TABLE 2-17: SMBUS SLAVE ADDRESS OPTIONS

Address Select	Board Implementation	SMBus Address [7:1]
0	Address Select Pulled to ground through a 10kΩ resistor	0111 000b
1	Address Select pulled to VCC1 through a 10kΩ resistor	0111 001b

2.8.3 SLAVE BUS INTERFACE

The ECE1088 device SMBus implementation is a subset of the SMBus interface to the host. The device is a *slave-only* SMBus device. The implementation in the device is a subset of SMBus since it only supports four protocols.

The Write Byte, Read Byte, Send Byte, and Receive Byte protocols are the only valid SMBus protocols for the device. This part responds to other protocols as described in the Invalid Protocol Section. Reference the System Management Bus Specification, Rev 2.0.

The SMBus interface is used to read and write the registers in the device. The register set is shown in Table 2-1, "Register Summary".

2.8.4 WRITE BYTE

The Write Byte protocol is used to write data to the registers. The data will only be written if the protocol shown in Table 2-18, "SMBus Write Byte Protocol" is performed correctly. Only one byte is transferred at time for a Write Byte protocol.

TABLE 2-18: SMBUS WRITE BYTE PROTOCOL

Field	Start	Slave Addr	Wr	Ack	Reg. Addr	Ack	Reg. Data	Ack	Stop
Bits	1	7	1	1	8	1	8	1	1

2.8.5 READ BYTE

The Read Byte protocol is used to read data from the registers. The data will only be read if the protocol shown in Table 2-19, "SMBus Read Byte Protocol" is performed correctly. Only one byte is transferred at time for a Read Byte protocol.

TABLE 2-19: SMBUS READ BYTE PROTOCOL

Field:	Start	Slave Addr	Wr	Ack	Reg. Addr	Ack	Start	Slave Addr	Rd	Ack	Reg. Data	Nack	Stop
Bits:	1	7	1	1	8	1	1	7	1	1	8	1	1

2.8.6 SEND BYTE

The Send Byte protocol is used to set the Internal Address Register to the correct register in the ECE1088. No data is transferred for a Send Byte protocol.The send byte protocol is shown in Table 2-20, "SMBus Send Byte Protocol".

TABLE 2-20: SMBUS SEND BYTE PROTOCOL

Field:	Start	Slave Addr	Wr	Ack	Reg. Addr	Ack	Stop
Bits:	1	7	1	1	8	1	1

2.8.7 RECEIVE BYTE

The Receive Byte protocol is used to read data from the registers when the register address is known to be at the desired address (using the Internal Address Register). Only one byte is transferred at time for a Receive Byte protocol.

TABLE 2-21: SMBUS RECEIVE BYTE PROTOCOL

Field:	Start	Slave Addr	Rd	Ack	Reg. Data	Nack	Stop
Bits:	1	7	1	1	8	1	1

Note: Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or stop condition.

2.8.8 STRETCHING THE SCLK SIGNAL

The ECE1088 supports stretching of the SCLK by other devices on the SMBus.

2.8.9 SMBUS TIMING

The SMBus Slave Interface complies with the SMBus AC Timing Specification. See the SMBus timing diagram shown in Section 4.2, "SMBus Timing".

2.8.10 SMBUS ALERT RESPONSE ADDRESS

This device responds to protocols with the SMBus Alert Response Address of 0001_100 if the ARA bit in the Clock Control register is set.

2.8.11 SMBUS TIME-OUT

The ECE1088 includes an SMBus time-out feature. Following a 30 ms period of inactivity on the SMBus, the device time-out and reset the SMBus interface.

2.9 BC-Link Interface

The BC-Link is a proprietary bus that allows communication between a Master device and a Companion device. The Master device uses this serial bus to read and write registers located on the Companion device.

The bus comprises three signals, BC_CLK, BC_DAT and BC_INT#. The Master device always provides the clock, BC_-CLK, and the Companion device is the source for an independent asynchronous interrupt signal, BC_INT#.

The ECE1088 supports BC-Link speeds up to 24MHz.

3.0 OPERATIONAL DESCRIPTION

3.1 Maximum Ratings

Maximum V_{cc1} ..... +5V

Negative Voltage on any pin, with respect to Ground ..... -0.3V

Operating Temperature Range ..... 0^oC to $+70^oC$

Storage Temperature Range ..... -55^o to $+150^oC$

Lead Temperature Range ..... Refer to JEDEC Spec. J-STD-020

Note: Stresses above those listed above and below could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

3.2 DC Electrical Characteristics

TABLE 3-1: DC ELECTRICAL CHARACTERISTICS $T_A = 0^oC – 70^oC$, $V_{CC1} = +3.3$ V ± 10%

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
ISP Type Input Buffer with 90µA Pull-up						Note 3-1 Schmitt Trigger
Low Input Level	V_{ILIS}			0.8	V	
High Input Level	V_{IHIS}	2.2		5.5	V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		100		mV	
IP/O8 Type Buffer with 90µA Pull-up						Note 3-1 TTL Levels
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4		V_{cc1} + 0.3	V	I_{OH} = -4mA
I/O8 Type Buffer						TTL Levels
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4		V_{cc1} + 0.3	V	I_{OH} = -4mA
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4		V_{cc1} + 0.3	V	I_{OH} = -4mA

TABLE 3-1: DC ELECTRICAL CHARACTERISTICS T_A = 0°C – 70°C, V_{CC1} = +3.3 V ± 10%

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
Leakage Current (ALL – except Buffers)						Note 3-2
Input High Current	$ILEAK_{IH}$			10	µA	V_{IN} = V_{cc1}
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
5V Tolerant Pins						V_{cc1} = 3.3V
Input High Current	$ILEAK_{IH}$			100	µA	V_{IN} =5.5V Max
Input High Current	$ILEAK_{IH}$			10	µA	V_{IN} <= V_{cc1}
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
V_{CC1} Supply Current Active	I_{CC}		3	8	mA	measured with SMBus/BC-Link traffic
V_{CC1} Supply Current Active with Ring Oscillator Off	I_{CC}			500	µA	measured with Ring Oscillator off (OCS Control bit set to Oscillator Low Power Enable mode)
Reset Voltage	V_{RST}	1.6	1.8	2.1	V	Device is in internal reset state when V_{cc1} is below min V_{RST}

- Voltages are measured from the local ground potential, unless otherwise specified.
- Typicals are at TA=25°C and represent most likely parametric norm.
- The maximum allowable power dissipation at any temperature is PD = (TJmax - TA) / QJA.
- Timing specifications are tested at the TTL logic levels, VIL=0.4V for a falling edge and VIH=2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.
- All pins except power and ground are 5V tolerant.

Note 3-1 90µA Pull-up with +/- 40% variation

Note 3-2 leakage currents are measured with all pins in high impedance.

3.3 AC Timing Specifications

Refer to the LSBC Bus Specification.

3.4 Capacitance Values for Pins

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC1} = 3.3V ±10%

TABLE 3-2: CAPACITANCE VALUES FOR PINS

Parameter	Symbol	Limits			Unit	Test Condition
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Note 3-3 The input capacitance of a port is measured at the connector pins.

4.0 TIMING DIAGRAMS

4.1 V_{CC1} Power

FIGURE 4-1: V_{CC1} POWER

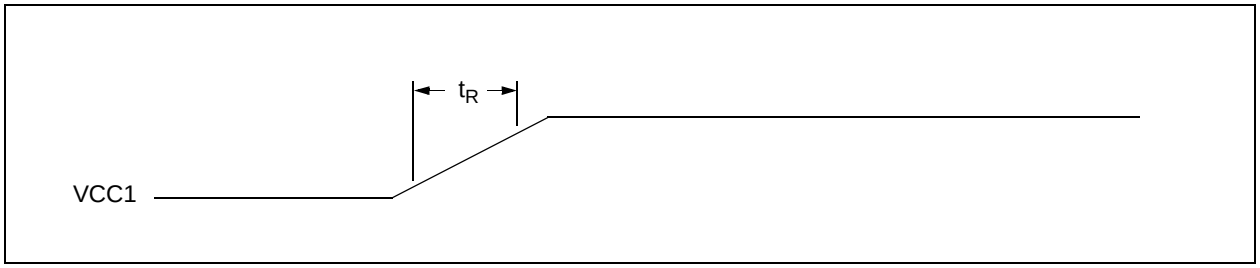


TABLE 4-1: V_{CC1} POWER PARAMETERS

Symbol	Parameter	Limits		Units	Comments
		Min	Max		
t_R	V_{CC1} Rise time, 10% to 90%	0.150	30	msec	

4.2 SMBus Timing

FIGURE 4-2: SMBUS TIMING

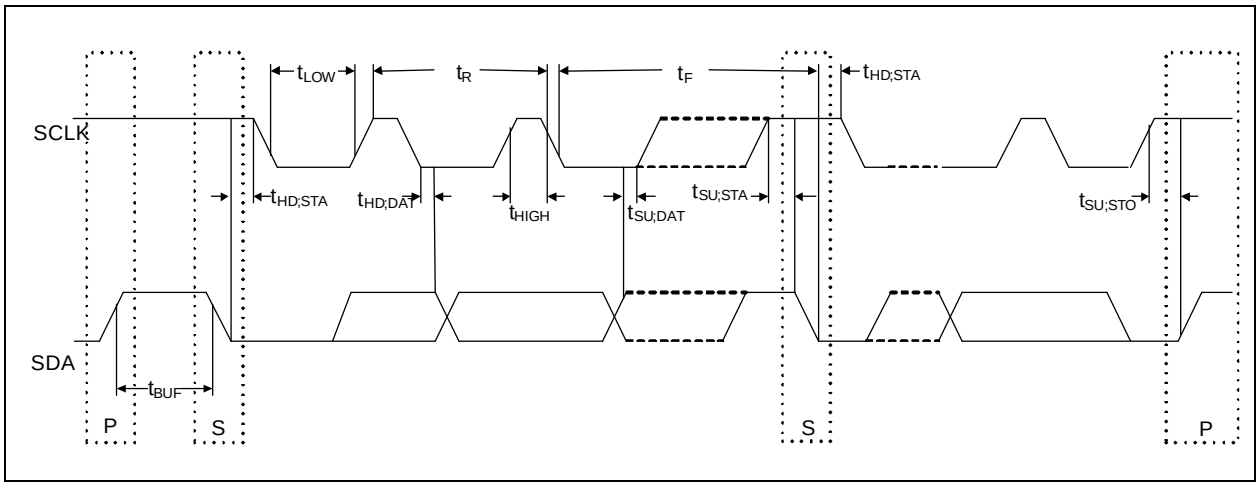


TABLE 4-2: SMBUS TIMING PARAMETERS

Symbol	Parameter	Limits		Units	Comments
		Min	Max		
Fsmb	SMB Operating Frequency	10	400	KHz	Note 4-1
Tsp	Spike Suppression		50	ns	Note 4-2
Tbuf	Bus free time between Stop and Start Condition	1.3		µs	
Thd:sta	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	0.6		µs	
Tsu:sta	Repeated Start Condition setup time	0.6		µs	
Tsu:sto	Stop Condition setup time	0.6		µs	
Thd:dat	Data hold time	0.3	0.9	µs	
Tsu:dat	Data setup time	100		ns	Note 4-3
Tlow	Clock low period	1.3		µs	
Thigh	Clock high period	0.6		µs	
Tf	Clock/Data Fall Time	$20+0.1C_b$	300	ns	
Tr	Clock/Data Rise Time	$20+0.1C_b$	300	ns	
C_b	Capacitive load for each bus line		400	pF	

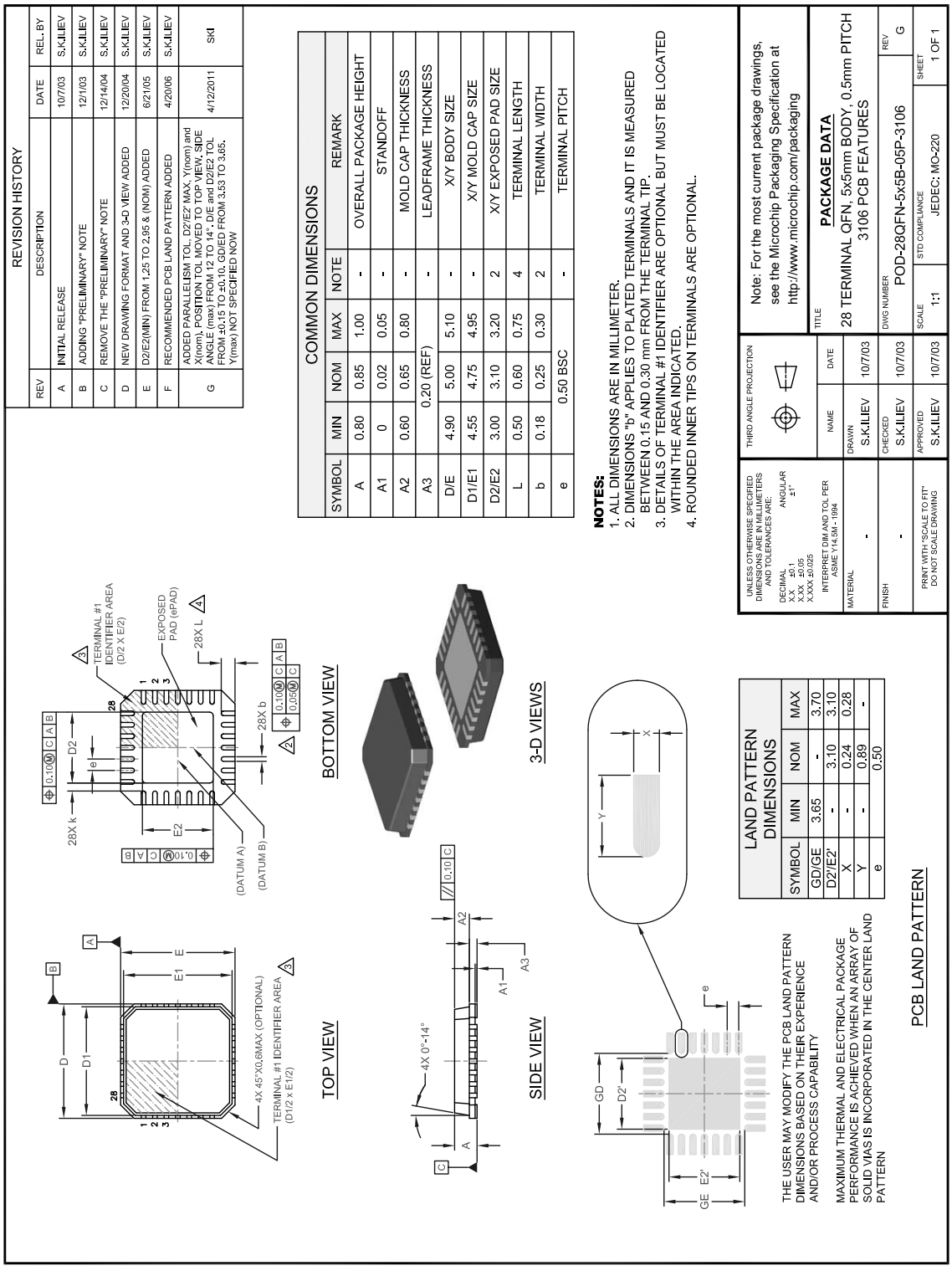
Note 4-1 The max SMBus timing operating frequency exceeds that specified in the System Management Bus Specification, Rev 1.1, but corresponds to the maximum clock frequency for fast mode devices on the I^2C bus (see the I^2C Bus Specification).

Note 4-2 At 400kHz, the input filter suppresses spikes of a maximum pulse width of 50ns.

Note 4-3 if using 100 KHz clock frequency, the next data bit output to the SDA line will be 1250 ns (1000 ns (T_R max) + 250 ns ($T_{SU:DAT}$ min) @ 100 kHz) before the SCLK line is released.

5.0 PACKAGE OUTLINE

FIGURE 5-1: PACKAGE OUTLINE: 28-PIN QFN BODY 5X5 MM BODY



APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002623A (01-15-18)	Public Release, REV A replaces previous SMSC version Rev. 1.6 (02-21-11)	

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