2ASC-12A1HP – 1200V Dual-Channel Augmented High Performance SiC Core 1

Optimized for Silicon Carbide (SiC) MOSFET Modules

Overview

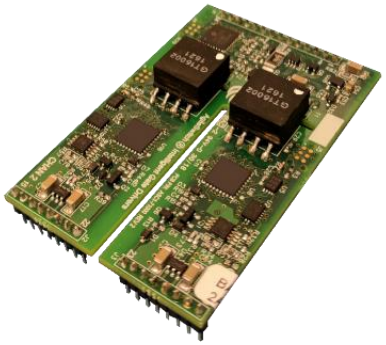
The AgileSwitch® 2ASC-12A1HP – 1200V Dual-Channel Augmented High Performance SiC Core 1 enables better control and protection of most SiC MOSFET-based power systems. The 2ASC-12A1HP provides up to 10A of peak current at an operating frequency of 100kHz. The high CMTI gate drive core includes an isolated DC/DC converter and low capacitance isolation barrier for PWM signals and fault feedback. The Intelligent Configuration Tool (ICT) will allow users to appropriately configure the Gate Driver Parameters to their application without having to worry about changing hardware.

Software Programmable Features

- Augmented Turn-Off™ (ATOff) (Patented)
- ± V_{GS} Gate Voltages
  - Vgs Pos from +15V to +21V
  - Vgs Neg from -5V to 0V
- Power supply under-voltage lockout (UVLO)
- Power supply over-voltage lockout (OVLO)
- Desaturation detection settings
- Dead time
- Fault lockout settings
- Automatic Reset settings

Key Driver Features

- UL Compliant - 1200V SiC MOSFET Modules
- Dual-Channel
- Robust High-Noise-Immunity Design
- Isolated Temperature Monitoring, PWM
- Isolated High Voltage Monitoring, PWM
- Compact 40x61mm form factor
- 2 X 3W output power
- RoHS compliant
- Up to 7 Unique Fault Conditions



Applications

- Heavy Duty Vehicles
- Induction Heating
- Auxiliary Power Units
- Battery Storage
- Inverters
- Wireless Charging

Required Accessory*

Part Number: **ASBK-014** (Device Programmer Kit)
Includes: Microchip PICKIT4, Adapter, Cables, and Intelligent Configuration Tool (ICT) Software

*Not included

Evaluation Tools*

ASDAK- AgileSwitch SiC Accelerated Development Kits provide the tools required to rapidly optimize the performance of SiC modules and systems. Each kit includes 2ASC Series Cores, ASBK-014, Module Adapter Boards, and optional Microchip SiC Modules.

Contents

System Overview

The basic topology of the driver core is shown in Figure 1.

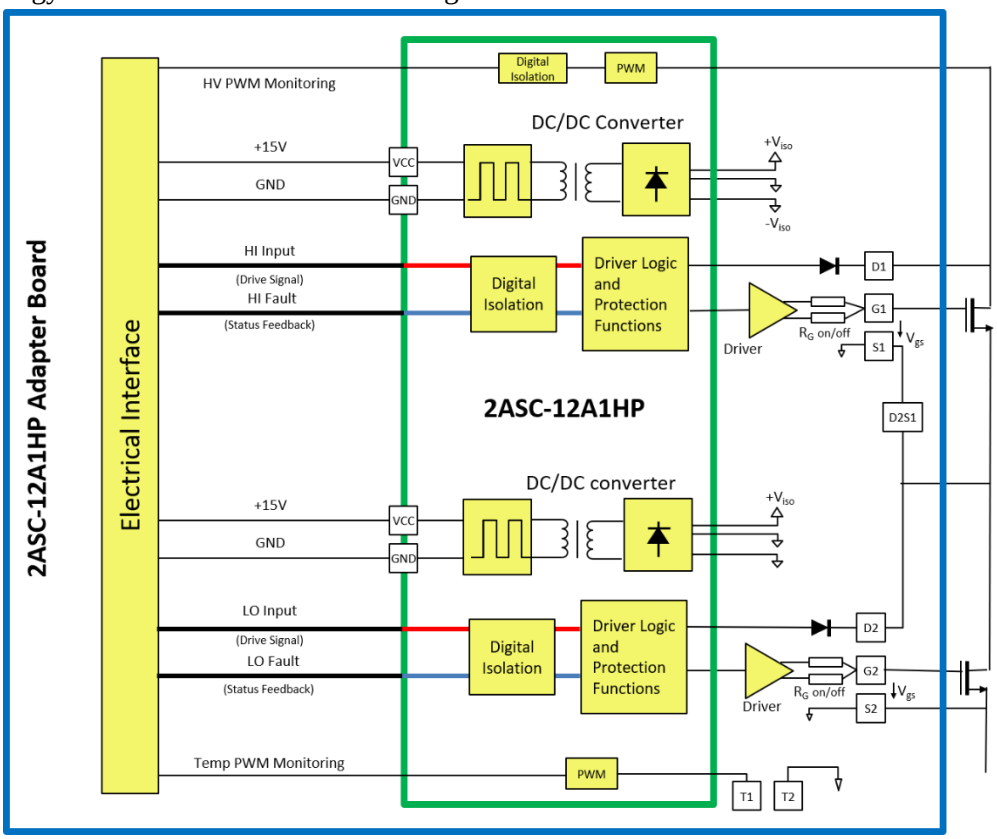


Figure 1: 2ASC-12A1HP Block Diagram

Absolute Maximum Ratings

Interaction of maximum ratings is dependent on operating conditions

Parameter	Description	Min	Max	Unit
Supply Voltage	VCC to GND	0	16.5	V
Peak Gate Current	Note 1	-10	10	A
Input Logic Levels	To GND	-0.5	5	V
Output Power per Gate			3	W
Switching Frequency	Note 2		100	kHz
Isolation Voltage	Primary to Secondary VAC RMS 1 min		3750	V
Working Voltage	Primary to Secondary, Secondary to Secondary		1200	V
Creepage Distance	Primary to Secondary Side	8		mm
dV/dt	Rate of change input to output	100		kV/µs
Operating Temperature	Ambient Operating Temperature	-40	+85	°C
Storage Temperature		-40	+90	°C

Electrical Characteristics

Conditions: V_{SUP} = +15.0 V, V_{IN_LOGIC} = 5V, MOSFET (Ciss = 11.7nF; Qg = 1025nC)

Power Supply	Description	Min	Typ	Max	Unit
Supply Voltage	VCC to GND	14	15	16	V
Supply Current	Without Load		110		mA
Supply Current	With Load, Note 3		250		mA
UVLO Level-HI and LO*	Primary Side low voltage detect fault level	13.2	13.5		V
UVLO Level-HI and LO*	Secondary Side low voltage detect fault level, Note 3	13.5	20.5		V
OVLO Level-HI and LO*	Primary Side high voltage detect fault level		16	16.5	V
OVLO Level-HI & LO*	Secondary Side high voltage fault detect level, Note 3		24.65		V

Signal I/O	Description	Min	Typ	Max	Unit
Input Impedance	5V - Hi and Lo side input	1			MΩ
V_{IN} Low	5V - Turn-off threshold			1.25	V
V_{IN} High	5V – Turn-on Threshold	3.5			V
Gate Output Voltage Low*	Note 5	-6		-4	V
Gate Output Voltage High*	Note 5	+17		+21	V
Fault Output Voltage	Fault lines are open collect with 5mA load	0.3		24	V
Fault Output Current	Note 4			10	mA
Switching Frequency	Note 2			TBD	kHz
DC Link & Temp Monitoring	High Voltage (HV) & Temp Monitoring Output	0		5	V
DC Link & Temp Monitoring	PWM Frequency		31.5		kHz
DC Link & Temp Monitoring	Output Impedance, User defined on Adapter Board		50 1%		Ω
DC Link Voltage Trip*	Note 5	0		1100	V
Temperature Trip*	Note 5	25		165	°C

MOSFET Short Protection	Description	Min	Typ	Max	Unit
Desat Monitor Voltage*	Between Drain and Sink of MOSFET, Note 3, Note 5	3	4.5	10	V
T_{DSAT}*	Activation after MOSFET Turn on, Note 5	0.5	1.5	1.75	µs
Response Time after Fault				200	ns

Note 1: Input signal should not be activated until 20 ms after power is applied to allow on board DC-DC converter to stabilize.
Note 2: Actual maximum switching speed is a function of gate capacitance.
Note 3: SiC MOSFET dependant, conditions listed above assume a MOSFET with Ciss = 11.7nF & Qg = 1025nC operating at 50kHz
Note 4: Fault lines are open collector and require a pull-up resistor, 2KΩ recommended
Note 5: Software Configurable
***Note:** For Software configurable parameters, the available range of values are listed in the table

Interconnects

Module Adapter to Driver Core Connectors

Ref	Connector	Type	Manufacturer Part Number
J1	Input	14 Pin, 2mm pitch spacing	NRPN141PAEN-RC
J2, J3	Ch 1, Ch 2	8 Pin, 2mm pitch spacing	NRPN081PAEN-RC

Core Programming Adapter

Ref	Connector	Type	Manufacturer Part Number
J4	Programming	6 Pin, 1.27mm pitch spacing	TC2030-IDC-NL

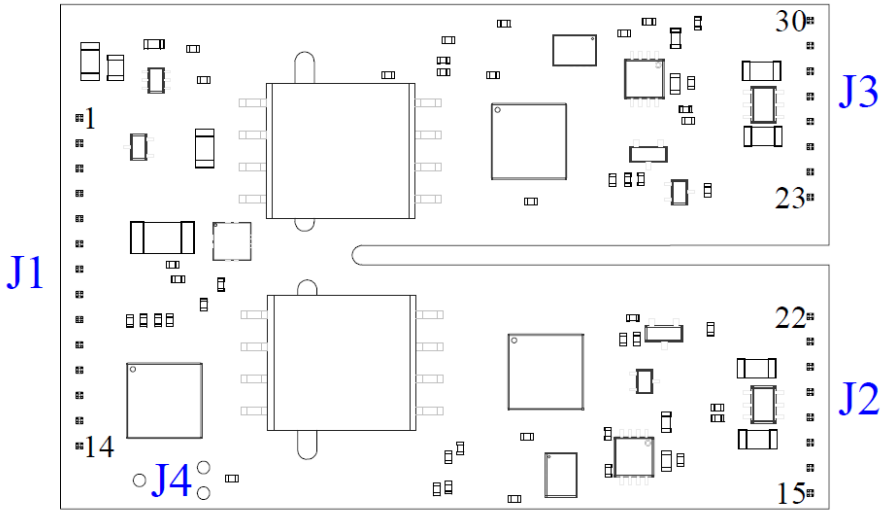


Figure 2: Interconnect Locations on PCB

Core Assembly on Adapter Board

Method 1 - Soldering

2ASC-12A1HP can be directly soldered onto an Adapter Board without the need for additional support.

Method 2 – Socket

2ASC-12A1HP can be plugged into female sockets on an Adapter Board.

Recommended Sockets

Ref	Connector	Type	Manufacturer Part Number
J1	Input	14 Pin, 2mm pitch spacing	NPPN141BFCN-RC
J2, J3	Ch 1, Ch 2	8 Pin, 2mm pitch spacing	NPPN081BFCN-RC

Pinout – Controller/Power to Driver Connection

14 PIN – J1 - Input

Pin No	Signal	Function
1	VCC	+15V Supply Voltage
2	VCC	+15V Supply Voltage
3	+5V Out	+5V Output to drive primary side electronics
4	AL-F	All Faults (Active when CH1-F or CH2-F)
5	CH2-F	Channel 2 Fault Output
6	CH2-Trig	Channel 2 Trigger Input
7	CH1-F	Channel 1 Fault Output
8	CH1-Trig	Channel 1 Trigger Input
9	TE-P	Non-Isolated Temperature Monitoring
10	HV-F	Isolated DC Link Voltage Monitoring
11	TE-F	Isolated Temperature Monitoring
12	F-RS	Fault Reset (Auto Reset Optional)
13	GND	Ground
14	GND	Ground

8 PIN – J2 – Channel 2 (CH2)

Pin No	Signal	Function
15	CH2_DC	DC Link Monitor
16	CH2_Temp	Temperature Monitor
17	CH2 – (-)V_Sec	Negative Secondary Voltage
18	CH2_Sink	Sink
19	CH2_Source	Source
20	CH2_GND	Ground
21	CH2 – (+)V_Sec	Positive Secondary Voltage
22	CH2 DSAT	Vds Monitor

8 PIN – J3 – Channel 1 (CH1)

Pin No	Signal	Function
23	CH1 DSAT	Vds Monitor
24	CH1 – (-)V_Sec	Negative Unregulated Voltage
25	CH1_GND	Ground
26	CH1_Sink	Sink
27	CH1_Source	Source
28	CH1 – (+)V_Sec	Positive Unregulated Voltage
29	CH1_DC	DC Link Monitor
30	CH1_Temp	Temperature Monitor

Recommended Interface Circuitry

Primary

Block Diagram

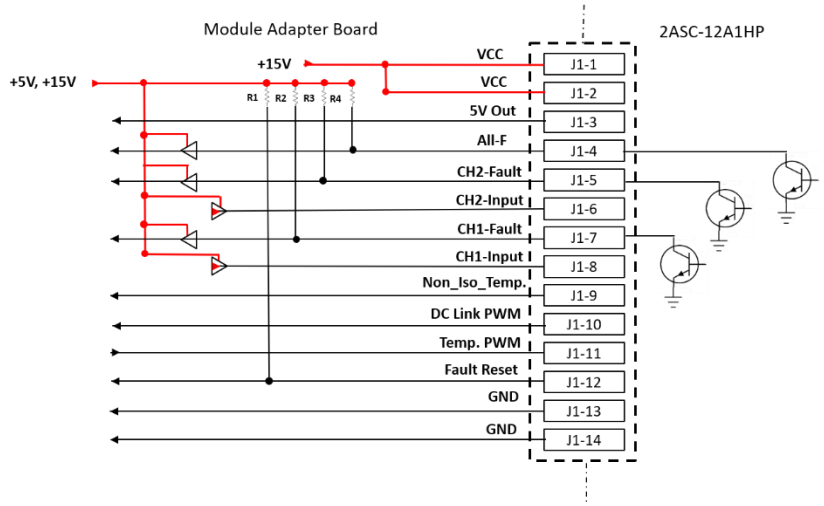


Figure 2 Input 14-Pin pinout diagram for 2ASC-12A1HP SiC Driver Core

Buffer Schematic for Inputs on the Module Adapter Board

The 2ASC-12A1HP has a standard 5V input logic. Based on the operating conditions, a 15V single ended input or differential input may be required.

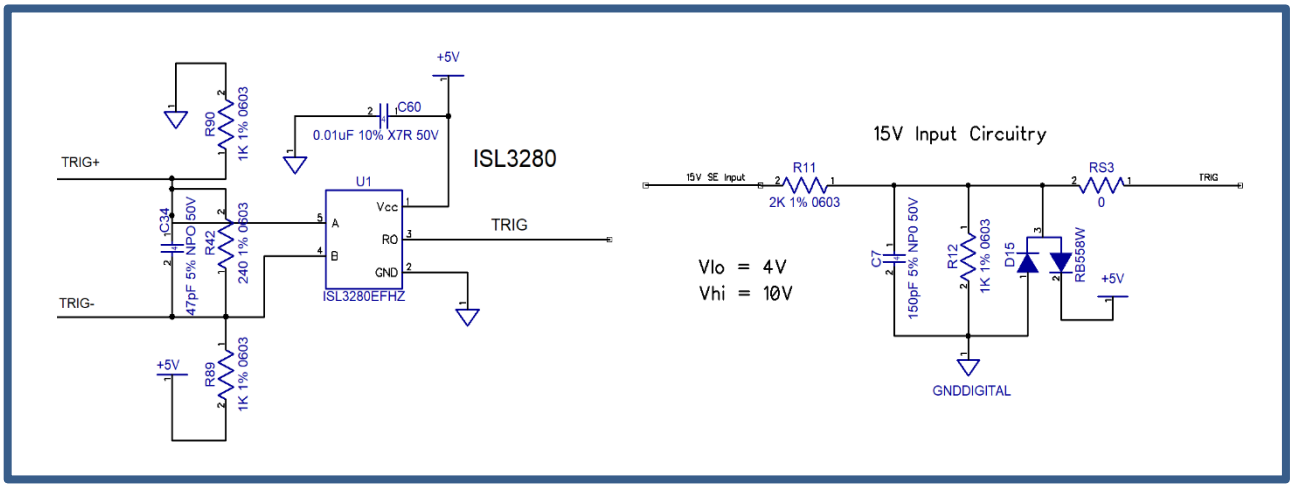


Figure 3 Input buffers on Module adapter board for differential & 15V Single Ended Inputs

Secondary

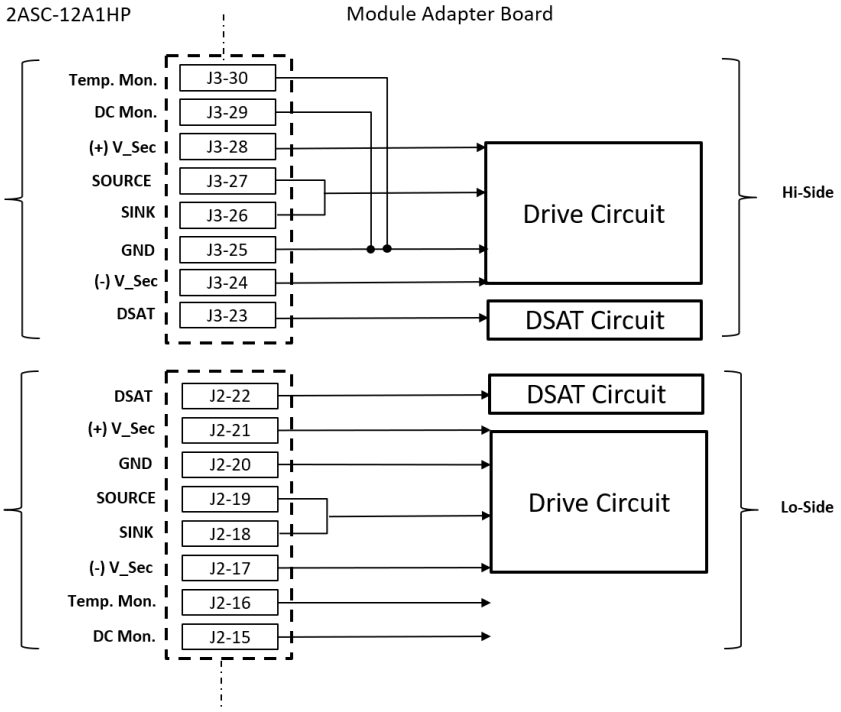


Figure 4 Output pinout diagram for 2ASC-12A1HP SiC Driver Core

Channels 1 & 2 can be used interchangeably as the HI or LO side.
On the HI Side the Temperature line should be floating and the DC Link monitor line should be grounded.

Drive Circuit

Gate Voltage (Vgs) limiting Zener diodes are recommend limiting the exposure of the SiC MOSFET Gate to high voltage transients. The Zener diodes should be chosen based on the Vgs ratings of the SiC MOSFET.

The 2ASC-12A1HP has separate Source & Sink outputs to separate the charging and discharging paths.

The below equation can be used to estimate the drive current required for a given SiC MOSFET module:

$$I_g peak = \frac{V_{gs+} + V_{gs-}}{Rg + RG}$$

$I_g peak$ – Peak Gate Current
V_{gs+} – Positive Gate Voltage recommended by the SiC MOSFET Manufacturer
V_{gs-} – Negative Gate Voltage recommended by the SiC MOSFET Manufacturer
Rg – SiC MOSFET Module Internal Gate Resistance
RG – External Gate Resistance on the Module Adapter Board

Note: $I_g peak$ is a strong function of the module gate charge
In the implementation shown below in Figure 6, a totem pole driver provides the 2ASC-12A1HP with ~20A peak current.

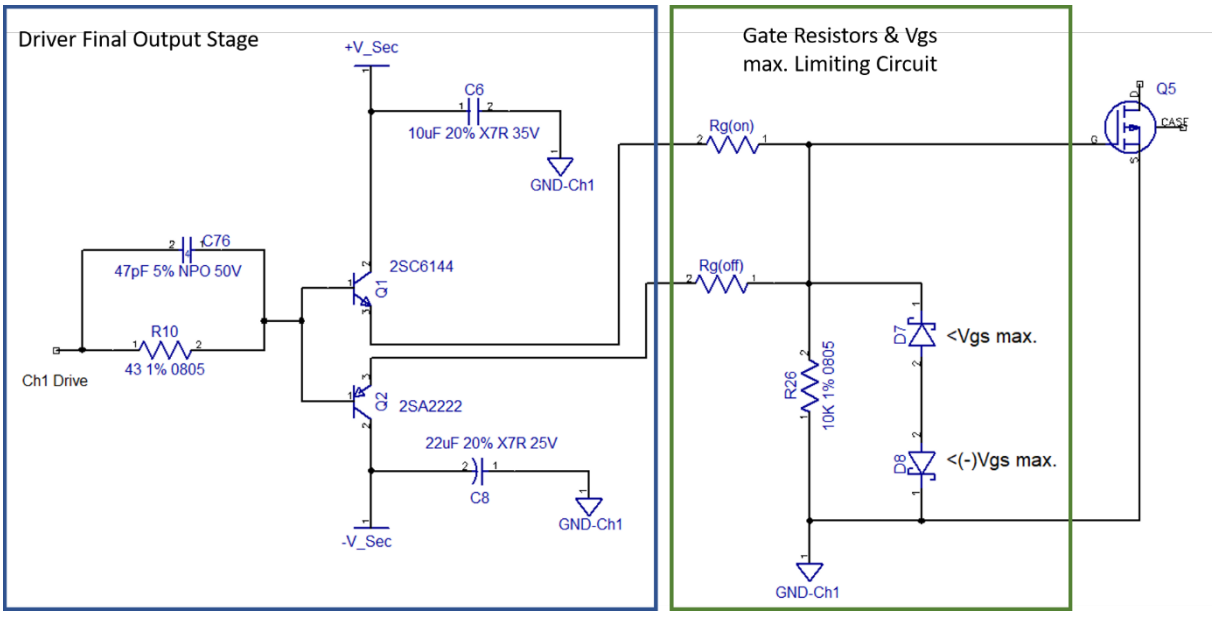


Figure 5 Recommended Hi-Side Drive Circuit for 2ASC-12A1HP SiC Driver Core

Short Circuit Protection - DSAT Circuit

SiC devices are limited in their Short Circuit withstand capability of 2-3us. It is therefore important to adopt the appropriate short circuit protection parameters for the Gate Driver.
DSAT Blanking time and DSAT threshold voltage are two such important parameters and are software configurable features on the 2ASC-12A1HP.

DSAT protection with sense diodes is the recommended method, shown below in Figure 7.
The DSAT lines are pulled up to +V_Sec via a 10kΩ pull up resistor on the 2ASC-12A1HP.

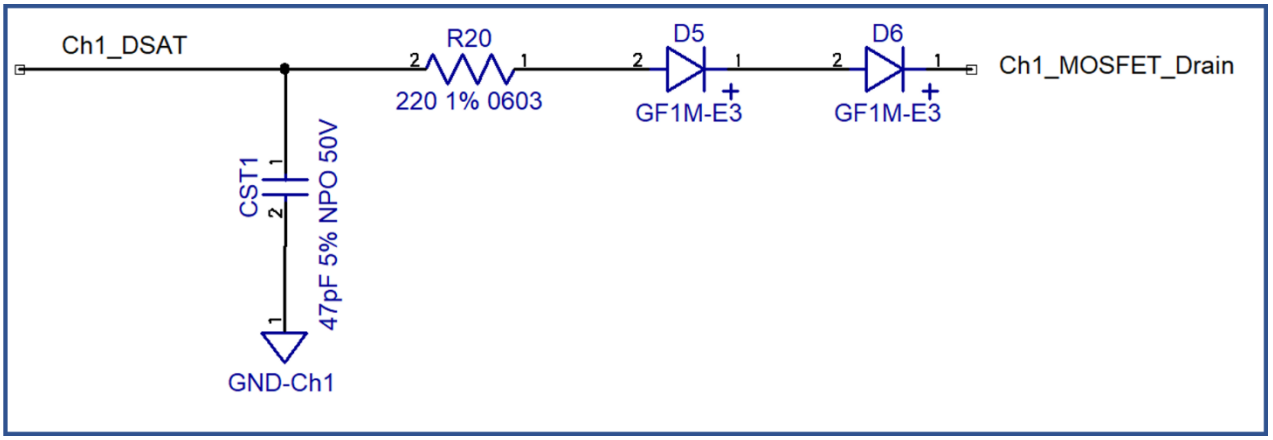


Figure 6 Recommended DSAT Sense Circuit for 2ASC-12A1HP SiC Driver Core

DC Link monitor

The 2ASC-12A1HP also features isolated DC Link Voltage monitoring and protection.

The 2ASC-12A1HP DC Link Monitor circuit performs two functions:

- Compares this monitored value against the DC Link Fault Threshold
- Converts the DC Link Voltage into a PWM

The resistor divider circuit shown in Figure 8 is recommended.

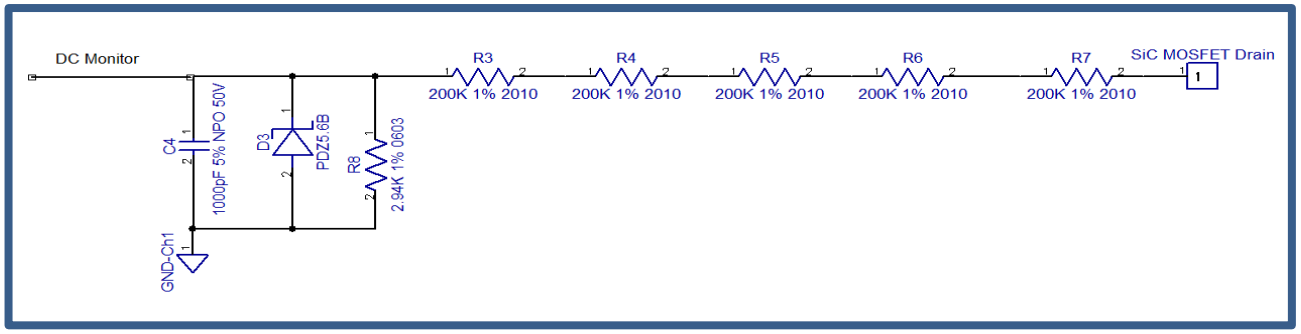


Figure 7 Recommended DC Link Monitor Circuit for 2ASC-12A1HP Core

Timing Diagrams

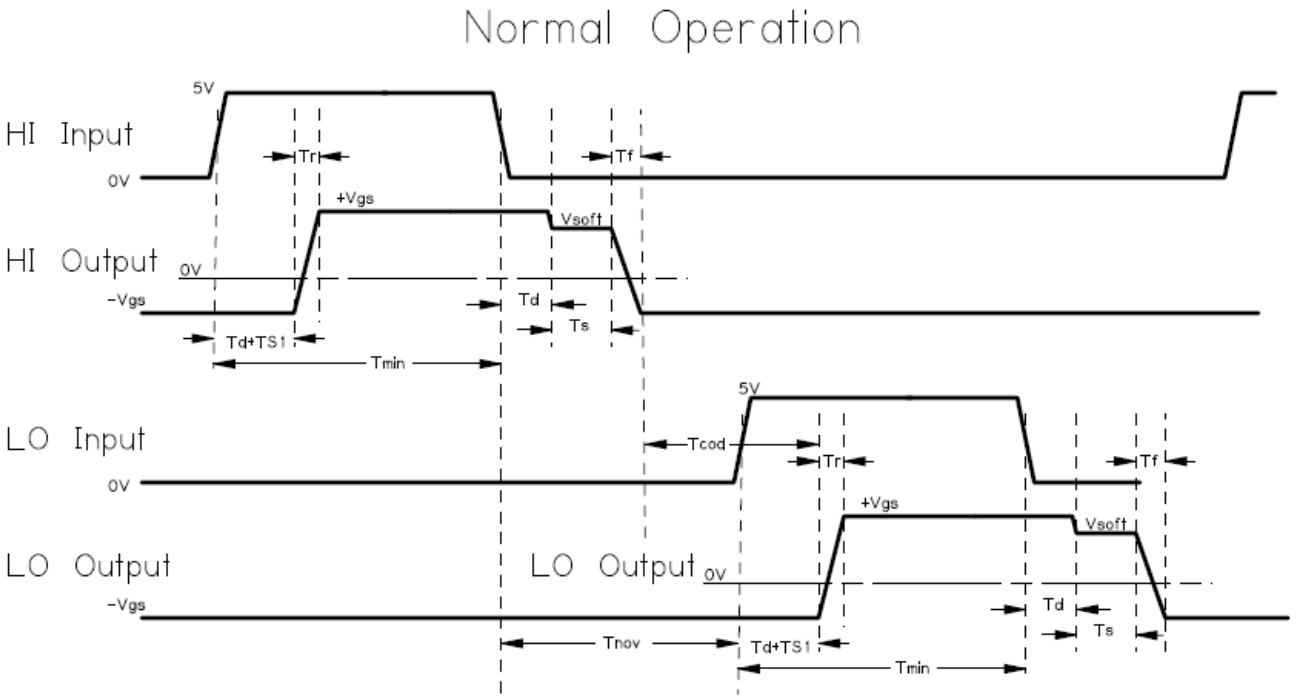


Figure 8 Signal input and output timing diagram.

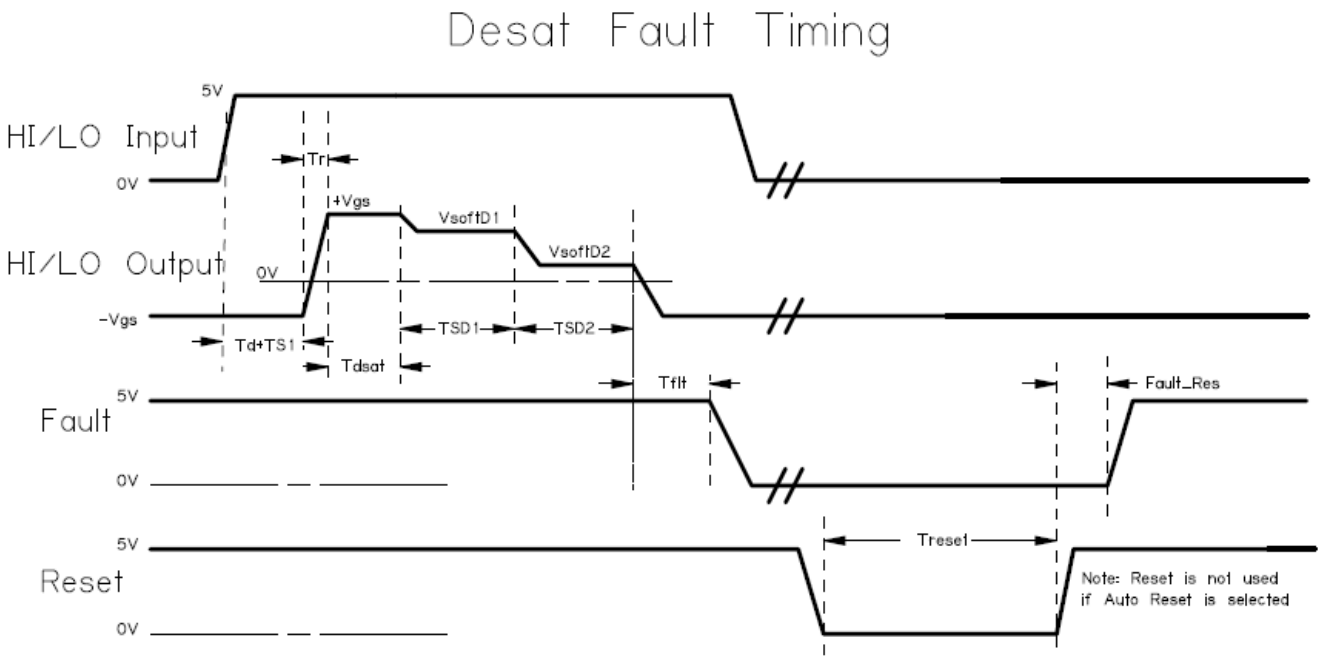


Figure 9 Signal desaturation and fault diagram.

Timing Diagram Values

Conditions: V_{SUP} = +15.0 V, Temp = 0 ºC to 85 ºC

Description	Symbol	Min	Typ	Max	Unit	Notes
Minimum Pulse Width	T_{MIN}	T_{S1}			ns	The minimum pulse width is a factor of the 2-Level Turn-Off Time
Delay Time	T_D			250	ns	
De-Glitch Time			200		ns	Input signal de-glitch time
Rise Time	T_R		80		ns	Measured from 10% to 90% points on edge Measurement Point 1 – Fig. 10
Fall Time	T_F		90		ns	Measured from 10% to 90% points on edge Measurement Point 2 – Fig. 10
2-Level Turn-Off Time	T_{S1}		360		ns	Software configurable
2-Level Turn-Off Voltage	Vsoft		1.5		V	Software configurable
Desaturation Time	T_{DSAT}	1400	1500	1600	ns	Software configurable
1st DSAT V	Vsoft D1		9		V	Multi-Level Turn-Off – First DSAT Step
First DSAT Time*	TSD1		400		ns	First DSAT 2-level turn-off time
2nd DSAT V	Vsoft D2		5		V	Multi-Level Turn-Off – Second DSAT Step
Second DSAT Time*	TSD2		200		ns	Second DSAT 2-level turn-off time
Fault Time Delay	T_{FLT}		5000		ns	
Fault Reset	Fault_Res		1000		ns	
Fault Response Time	T_{RESP}		200		ns	
Dead Time - Input	T_{NOV}		1000		ns	Recommended Minimum Time between Inputs
Dead Time – Driver	Tcod	1000			ns	Minimum Time between drive signals allowed by driver, software configurable
Reset Timing	Treset	1000			ns	Minimum Reset Time
Automatic Reset (Optional)			5		ms	Standard setting of 5 ms

*Note 3

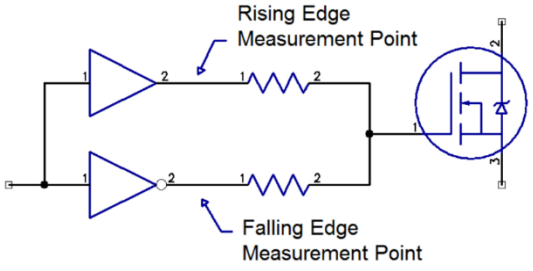


Figure 10 Measurement points for rise and fall time

Temperature and High Voltage PWM Monitoring

The AgileSwitch 2ASC-12A1HP Driver provides two 31.5 kHz, 5.0V PWM output signals that monitor the thermistor temperature (isolated or non-isolated) and the DC Link Voltage (High Side drain to Low Side source) of the SiC MOSFET power module. The PWM signals have an output impedance of 510Ω. When combined with an external low pass filter, these signals represent a real time, isolated voltage for both High Voltage and Thermistor Temperature. A Sallen-Key active low pass filter can be used with these outputs as shown below with a 2 kHz cut-off frequency. The cut-off frequency can be optimized for your application. For simplicity, a simple RC low pass filter with 100 Hz cut-off frequency can also be used.

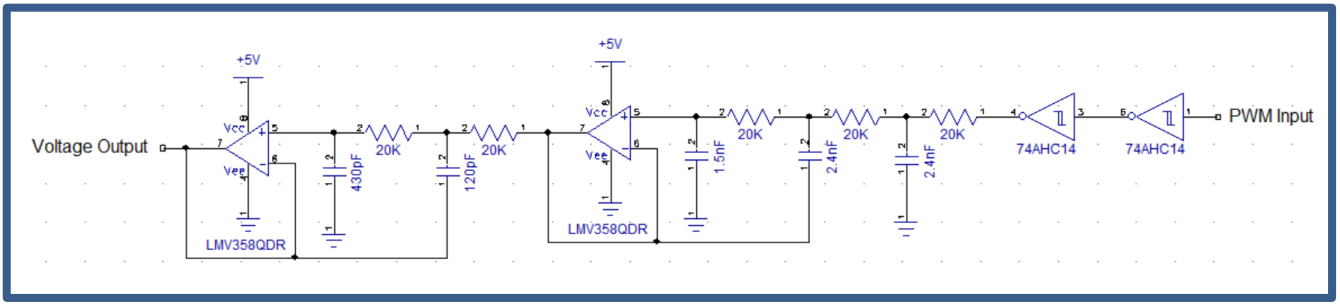


Figure 11 Example of a 2kHz Low Pass Filter

Temperature Monitor

The following table describes the correlation between the Thermistor Temperature and filtered Temperature Monitor Output. This is based on an NTC thermistor that measures 5kΩ @ 25°C. In the event that a thermistor is not part of the SiC Module the Recommended external Thermistor P/N is: TBD.

Output Voltage [V]	Temperature [°C]
0.8	-3
1.6	25
2.2	41
2.8	57
3.1	67
3.3	74
3.4	80
3.7	94
4.0	108
4.1	122
4.3	138
4.4	154

DC Link Voltage Monitor

The DC Link (HI Side drain to LO Side source) Monitor Output Voltage is 1% accurate from 50V to 1650V. The PWM output is the ratio of the DC Link Voltage / 1700V. For example, an 825V DC Link Voltage, the PWM output will be 50%. The linear equation for the Voltage Monitor PWM Output with a 2 kHz 4 pole filter is:

$$V_{DC}[V] = 340\ X\ Vmonitor$$

Generic Sample Factory Settings

AgileSwitch drivers are designed to provide safe, secure and efficient operation of the SiC MOSFET power module, as well as to provide unparalleled information on the condition of the overall system.

Generic samples are set at the factory to perform certain actions (e.g. turn off the HI side or LO side of the SiC MOSFET) and to report that a fault occurred based on performance parameters that occur outside of default ranges.

The tables below show the generic configuration.

Performance & Interconnect Settings

Parameter	Generic Factory Setting	Value	Unit
Fault Reset	Auto	5	ms
DC Link Voltage Fault	Enabled	900	V
Temperature Fault	Enabled	125	°C
UVLO Primary	Enabled	13.2	V
UVLO Secondary	Enabled	20.2	V
OVLO Primary	Enabled	16.5	V
OVLO Secondary	Enabled	24.65	V

Fault and Monitoring Conditions

Fault Condition/Action	Generic Sample Default Trigger Values	Action on IGBT if Active (Default Setting)	Faults Low Active			Faults High Active		
			HI Fault	LO Fault	All Faults	HI Fault	LO Fault	All Fault
NO FAULTS	N/A	N/A	HIGH	HIGH	HIGH	LOW	LOW	LOW
DSAT/UVLO – HI	See Electrical Characteristics	Turn Off HI & LO Side	LOW	HIGH	LOW	HIGH	LOW	HIGH
DSAT/UVLO – LO	See Electrical Characteristics	Turn Off HI &LO Side	HIGH	LOW	LOW	LOW	HIGH	HIGH
OVLO	See Electrical Characteristics	Turn Off HI & LO Side	HIGH	HIGH	LOW	LOW	LOW	HIGH
Temperature Fault	125 °C Thermistor Monitor	No Action	HIGH	HIGH	LOW	LOW	LOW	HIGH
DC Link Voltage Fault	DC Link Voltage above or below setting	Turn Off HI & LO Side	HIGH	HIGH	LOW	LOW	LOW	HIGH
Power On Configuration Fault*	Failure to Configure Gate drivers	Turn Off HI & LO Side	LOW	LOW	LOW	HIGH	HIGH	HIGH

*After power up, if all Fault lines are Active, then either there is a real fault (UVLO/DSAT) on both the HI and LO sides or there has been a software configuration failure.

Important Precautions

Caution: Handling devices with high voltages involves risk to life. It is imperative to comply with all respective precautions and safety regulations.

When installing the core and adapter board, please make sure that power is turned off. Hot swapping may cause damage to the IC components on the board.

AgileSwitch assumes that the core and adapter board have been mounted on the SiC MOSFET prior to start-up testing. It is recommended that the user checks that the SiC MOSFET power modules are operating inside the Specified Operating Area (SOA) as specified by the module manufacturer including short circuit testing under very low load conditions.

Software Configurable Parameters

The software configurable parameters on the 2ASC-12A1HP can be modified using a GUI developed by AgileSwitch. The code generated by this GUI is then downloaded to the driver. For further information regarding the parameters and instructions on programming the driver, please refer to the below documents.

Visit www.AgileSwitch.com/program.html for details.

Reference Designs

AgileSwitch has developed Reference Module Adapter Boards for the 2ASC-12A1HP. These design data of these adapter boards can be found here:

Module Package	Model Number	Module Manufacturers
SP6LI	SP6CA1	Microchip
SP6	SP6CA2	Microchip
62mm	62CA1	Wolfspeed, Semikron, Infineon, Global Power
62mm High Performance	62CA2	Wolfspeed
E, G Type Package	EDCA1	Rohm
C Type Package	EDCA2	Rohm
XM3 Type Package	XMCA1	Wolfspeed

Mechanical Dimensions

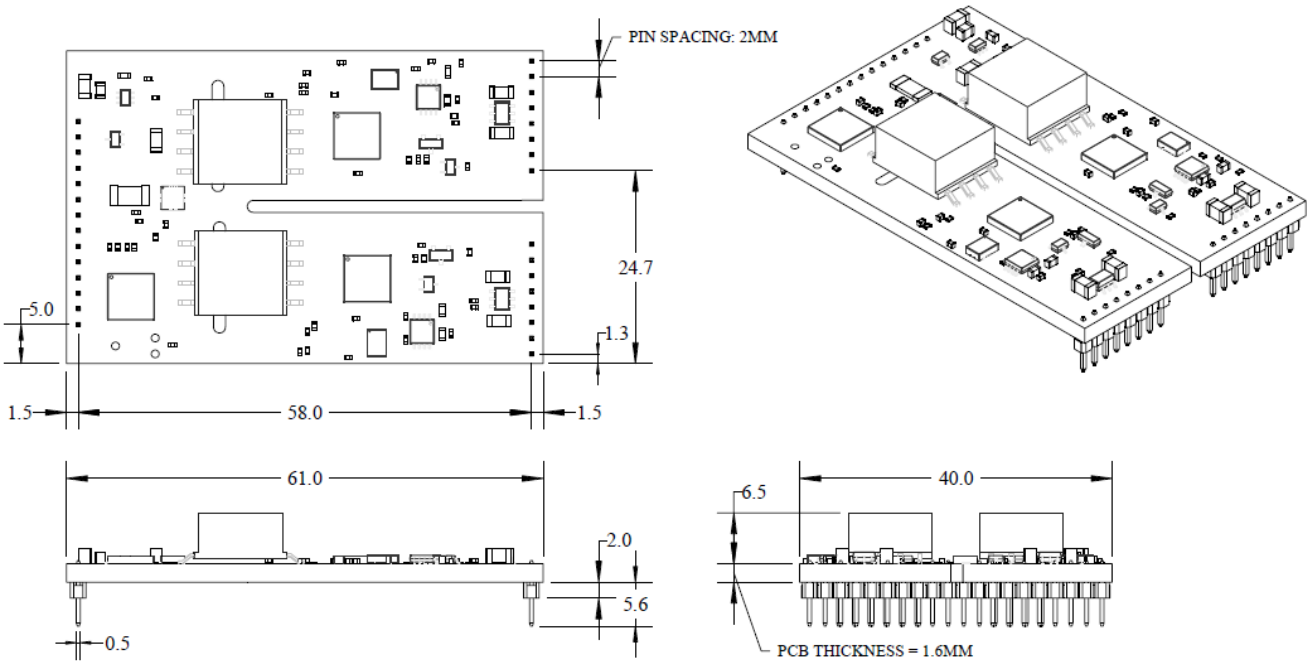


Figure 11: Dimensions of the 2ASC-12A1HP Core(+/- 0.1mm)

Dimensions are in mm.

Download the full drawing and model for additional details.

Revisions

Prepared By	Approved By	Version	Date	Description
N. Satheesh A. Fender		01	8/31/2018	Preliminary Release
N. Satheesh A. Fender		1.1	10/4/2018	Changed Secondary Pin-Out, Added Interface Circuits, Updated Mechanical Drawings
A. Fender		1.2	10/12/2018	Updated Mechanical Drawing
N. Satheesh		2	3/22/2019	Changed HI Side Termination; Clarified Software Configurable Features;
N. Satheesh		3	4/30/2019	Added to Adapter Board Compatibility Table
A. Fender		4	6/18/2020	Added Microchip logo, updated legal disclaimer, updated reference design table

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Patent Notices

Offering	Issued U.S. Patent Numbers
AgileStack™ Power stack control systems	8,984,197
Gate drive control system for SiC and IGBT power devices	9,490,798
Additional Patents Pending	

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