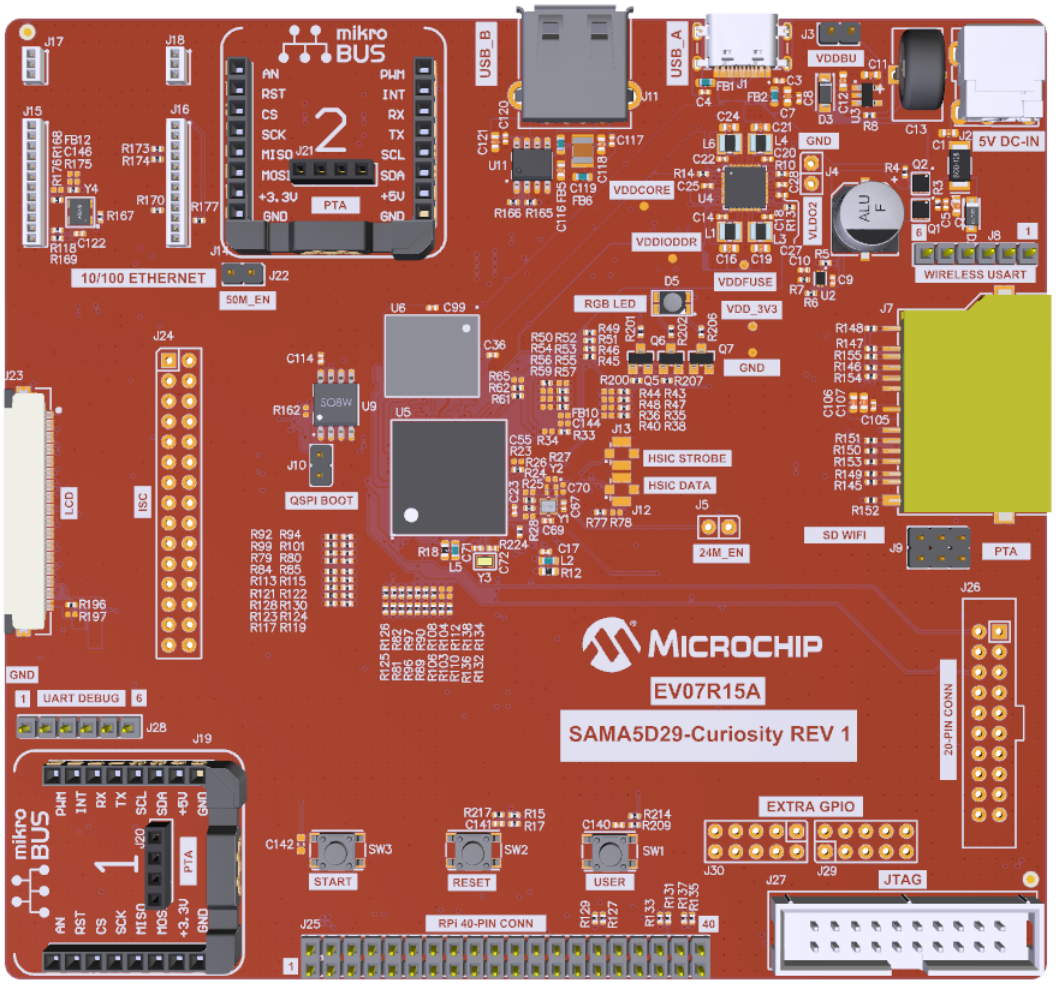
# SAMA5D29-Curiosity User Guide

## EV07R15A

## Scope

This user's guide introduces the SAMA5D29-Curiosity board (EV07R15A) and describes the development and debugging capabilities running on the SAMA5D29 Arm®-based embedded MPU.

**Figure 1.** SAMA5D29-Curiosity Overview



# 1. Introduction

## 1.1 Document layout

The document is organized as follows:

- Chapter 1. “Introduction”
- Chapter 2. “Product Overview” – Important information about the SAMA5D29-Curiosity board
- Chapter 3. “Function Blocks” – Specifications of the SAMA5D29-Curiosity and high-level description of the major components and interfaces
- Chapter 4. “Installation and Operation” – Instructions on how to get started with the SAMA5D29-Curiosity board
- Chapter 5. “Ordering Information”
- Chapter 6. “Errata”
- Chapter 7. “Schematics and Layouts” – SAMA5D29-Curiosity schematics and layout diagrams

## 1.2 Recommended Reading

The following Microchip documents are available and recommended as supplemental reference resources:

- SAMA5D29 Data Sheet. Lit. Number DS60001764
- SAMA5D29 Silicon Errata and Data Sheet Clarification. Lit. Number DS80001007

# 2. Product Overview

The SAMA5D29-Curiosity follows the Microchip MPU strategy for low-cost evaluation kits, showcasing all the features that the SAMA5D29 MPU offers.

## 2.1 SAMA5D29-Curiosity Features

**Table 2-1.** SAMA5D29-Curiosity Features

| Characteristic | Specification | Featured Components |
|---|---|---|
| Processor | 289-ball LFBGA, 14x14 mm, 0.8 mm pitch | Microchip SAMA5D29-CN |
| External clock | 24 MHz Crystal<br>32.768 kHz Crystal<br>50 MHz Clock generator for ETH RMII | ECS-240-10-37B2-JTN-TR<br>FC-12M 32.7680KA-A3<br>ASEMB-50.000MHZ-LC-T |
| Memory | 4 Gb LPDDR2<br>64 Mb QSPI NOR Flash | Alliance Memory AS4C128M32MD2A-18BIN<br>Microchip SST26VF064BEUI-104I/SM |
| SD/MMC | One µSD card interface<br>One SD Card / Radio Module interface | –<br>– |
| USB | One USB Type-C™ connector<br>One USB Type-A connector | MIC2025-1YM |
| Ethernet | One 10/100 RMII add-on slot | – |
| LCD | One LCD RGB666 interface | – |
| Camera | One ISC Camera header | – |
| Debug port | One UART Debug connector<br>One JTAG interface | –<br>– |
| Board monitor | One RGB (Red, Green, Blue) LED<br>Three push button switches | –<br>– |
| Expansion | Raspberry Pi(Note) 40-pin GPIO connector<br>Two mikroBUS™ connectors<br>One multipurpose 20-pin connector<br>Two PIOBU/System headers | –<br>Hundreds of possible Click™ extensions featuring Microchip functions inside<br>Exposes NAND Flash interface<br>– |
| Power management | Power Supply Unit | Microchip MCP16502TAC-E/S8B |
| Board supply | System 5 VDC from USB A<br>System 5 VDC from DC Jack | –<br>– |

**Note:** Raspberry Pi is a trademark of Raspberry Pi Trading.

## 2.2 SAMA5D29-Curiosity Specifications

**Table 2-2.** SAMA5D29-Curiosity Specifications

| Characteristic | Specification |
|---|---|
| Board Identification | SAMA5D29-Curiosity |
| Board Supply Voltage | External or USB-powered |
| Temperature | Operating: 0°C to +70°C |
| Relative Humidity | 0 to 90% (non-condensing) |
| Main board dimensions | 115 mm × 85 mm x 20 mm |
| RoHS Status | RoHS 3 Compliant |

| .....continued | |
|---|---|
| **Characteristic** | **Specification** |
| China RoHS Status | EFUP50 |
| REACH Status | REACH Compliant |

## 2.3 Kit Content

The SAMA5D29-Curiosity kit includes the following:

- The SAMA5D29-Curiosity board inside an ESD bag
- One USB-A to USB Type-C cable

## 2.4 Power Sources

Two options are available to power up the SAMA5D29-Curiosity board:

- Powering through the USB Type-C connector on the USBA port (J1)
- Powering through the DC Jack connector (J2)

**Table 2-3.** Electrical Characteristics

| Electrical Parameters | Value |
|---|---|
| Input voltage | 5 VDC |
| Maximum input voltage (limits) | 6 VDC |
| Maximum 3.3 VDC current | 300 mA |

**⚠ CAUTION** The SAMA5D29-Curiosity board runs at a 3.3V voltage level logic. The maximum voltage that the I/O pins can tolerate is 3.3V. Providing higher voltages (e.g., 5V) to an I/O pin could damage the board.

## 2.5 Connectors on Board

The fully-featured SAMA5D29-Curiosity board integrates multiple peripherals and interface connectors, as shown in the following figures.

**Figure 2-1.** SAMA5D29-Curiosity Connectors on Top Side

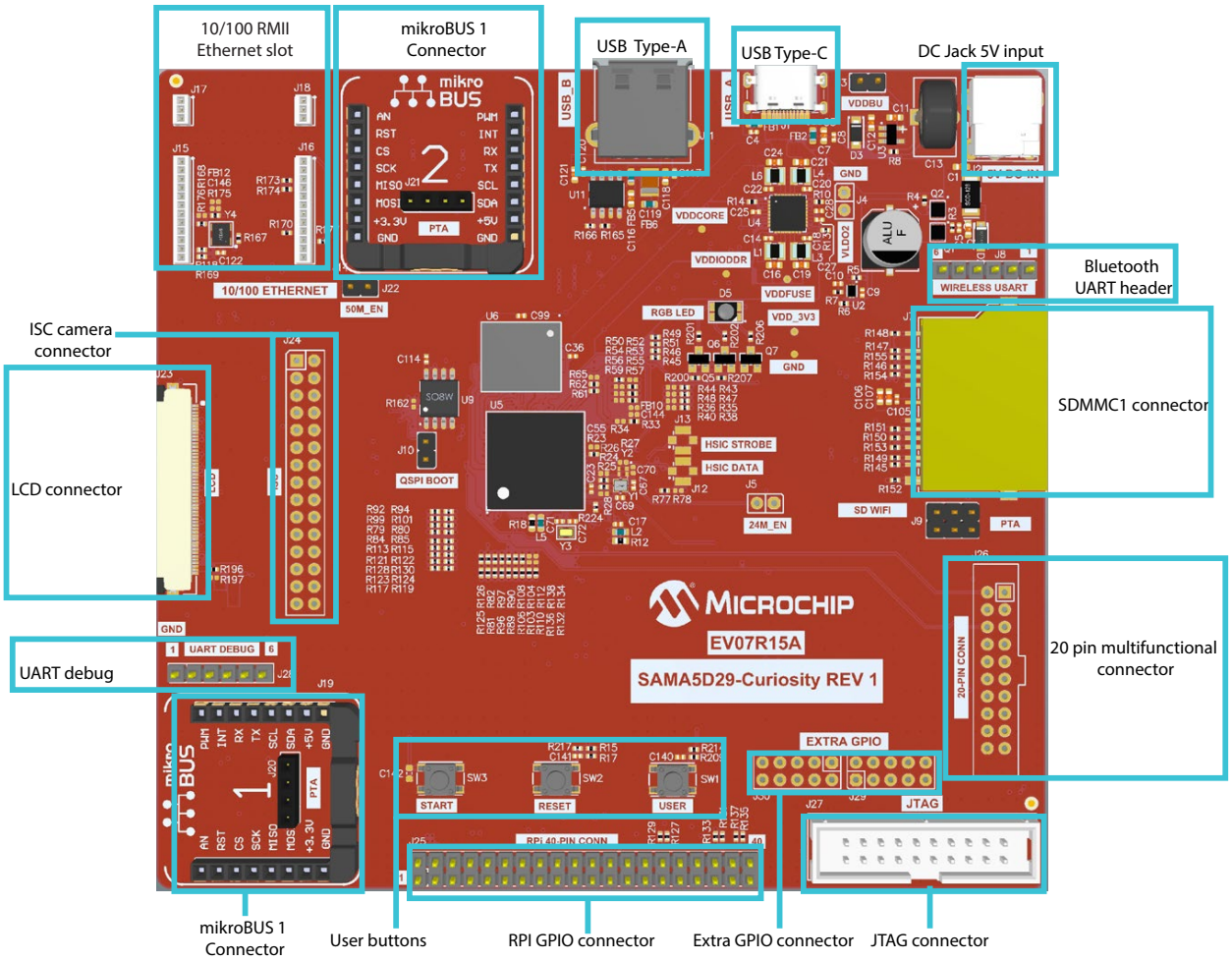


**Figure 2-2.** SAMA5D29-Curiosity Connectors on Bottom Side

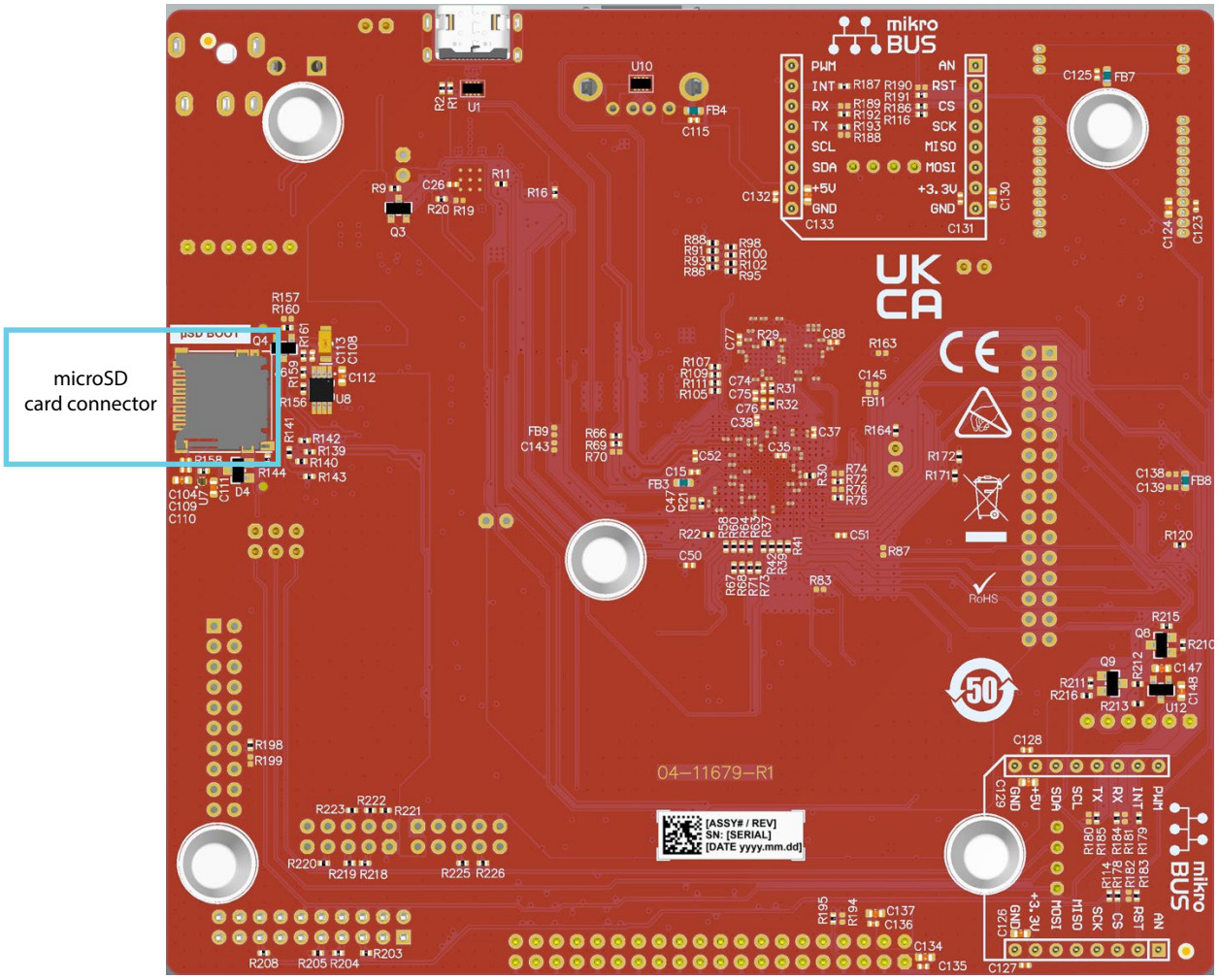



**Table 2-4.** SAMA5D29-Curiosity Board Interface Connectors

| Connector | Interfaces to |
|---|---|
| J1 | USB2.0 Type-C (USB-A) |
| J2 | DC Jack 5V power |
| J6 | µSD-CARD connector |
| J7 | SD Card / Radio module connector |
| J8 | USART header for Radio module |
| J9 | PTA header for SD Radio module |
| J11 | USB Type-A (USB-B) |
| J12, J13 | HSIC u.FL connectors (DNP) |
| J15, J16, J17, J18 | 10/100 RMII add-on slot |
| J19 | mikroBUS1 connector |
| J22 | mikroBUS2 connector |
| J23 | LCD connector |
| J24 | ISC Camera connector (DNP) |
| J25 | Raspberry Pi GPIO connector |

| .....continued | |
|---|---|
| **Connector** | **Interfaces to** |
| J26 | Multipurpose Header |
| J27 | JTAG connector |
| J28 | FTDI connector (UART debugger) |
| J29 | Tamper signals connector (DNP) |
| J30 | System signals connector (DNP) |

## 2.6 Default Jumper Settings

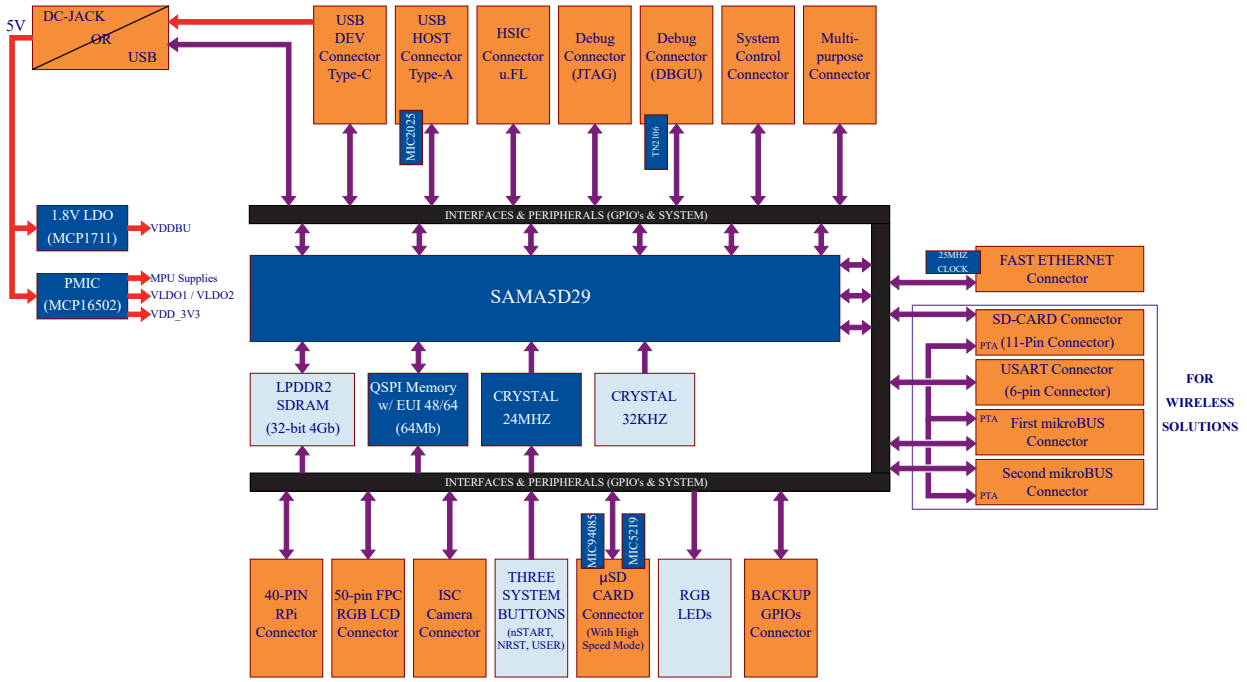
**Table 2-5.** SAMA5D29-Curiosity Jumper Settings

| Jumper | Default Setting | Function |
|---|---|---|
| J3 | Closed | VDDBU current measurement |
| J10 | Closed | Enables QSPI Flash boot |
| J22 | Closed | Enables RMII 50MHz clock |

# 3. Function Blocks

This section covers the SAMA5D29-Curiosity specifications and provides a high-level description of the board's major components and interfaces. This document is not intended to provide detailed information about the processor or about any other components used on the board. Refer to the component documentation for further details.

**Figure 3-1.** SAMA5D29-Curiosity Block Diagram




## 3.1 Power Supply Topology and Power Distribution

This section describes the implementation and circuitry that ensure adequate voltage stability for all the devices on the board and a correct power-up sequence for the MPU.

The power-up and power-down sequences indicated in the SAMA5D29 Data Sheet must be respected for a reliable operation of the device.

### 3.1.1 Input Power Options

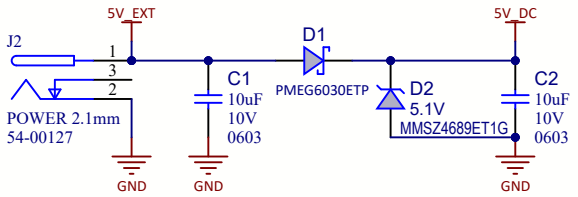
The SAMA5D29-Curiosity board can be powered through:

- An external AC to DC +5V wall adapter connected via a 2.1 mm center-positive plug into the power jack of the board (J2); the recommended output capacity of the power adapter is 2A
- USB port A (J1)

#### 3.1.1.1 Wall Adapter Input

The 5V_EXT from the wall adapter is protected through a pair of Schottky/Zener diodes (D1 and D2) that limit the input voltage to 5.1V. The following figure shows the wall adapter input power supply topology.

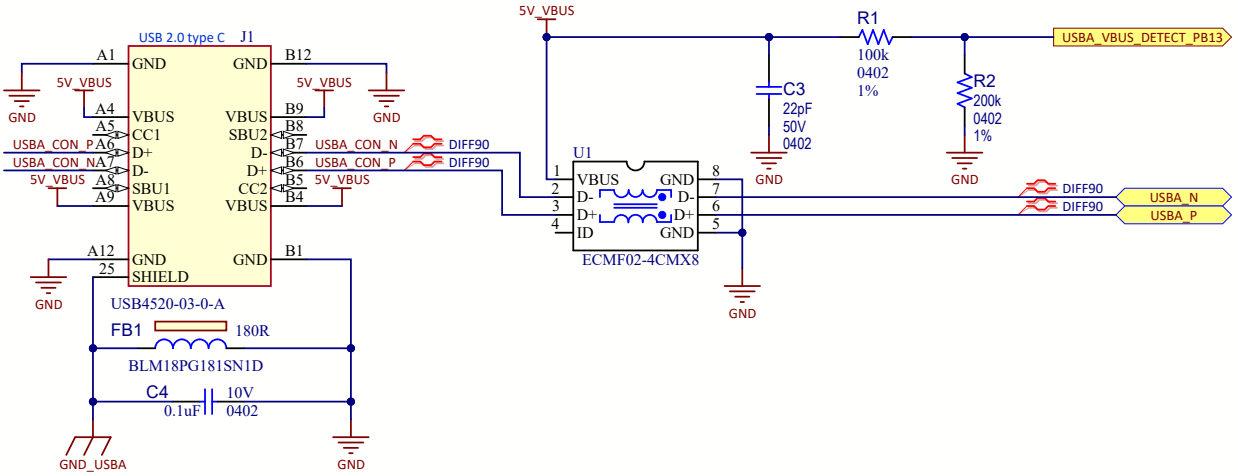
**Figure 3-2.** Wall Adapter Input Power Schematic




### 3.1.1.2 USB Supply Input

The USB-powered operation comes from the USB device port connected to a PC or a 5 VDC supply. The USB supply is enough to power the board in most applications. It is important to note that when the USB supply is used, the USB port has limited power. If a USB host port is required for the application, it is recommended to use the external DC supply or a more capable USB external power supply. The following figure shows the USB input power supply topology.

**Figure 3-3.** USB Input Power Schematic

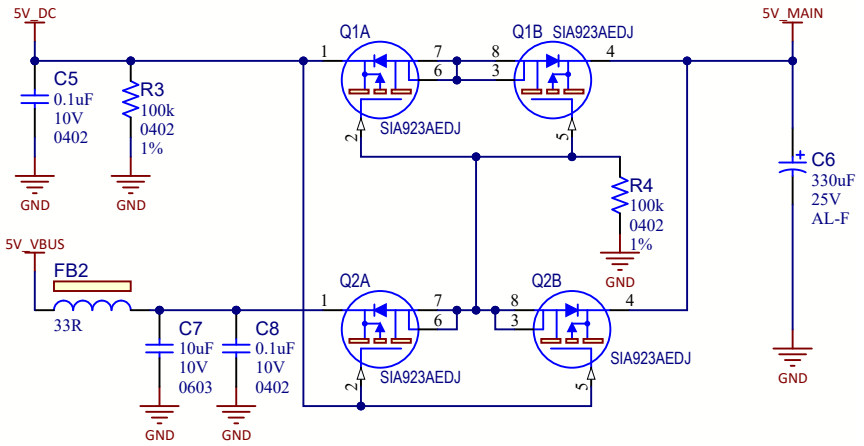



**Note:** USB-powered operation eliminates additional wires and batteries. It is the preferred mode of operation for any project that requires only a 5V source at up to 500 mA.

### 3.1.1.3 Automatic Power Switch

The switch between the two powering options, wall adapter or USB, is made by four transistors that ensure the separation between the two when both are plugged. The switch prioritizes powering from the wall adapter to maximize power transfer. The following figure shows the automatic power switch.

**Figure 3-4.** Automatic Power Switch




### 3.1.2 Power Management Integrated Circuit

The MCP16502 is a fully-featured PMIC optimized for Microchip MPU devices.

The MCP16502 integrates four DC-DC buck regulators and two auxiliary LDOs, and provides a comprehensive interface to the MPU, which includes an interrupt flag and an I2C interface.

All Buck channels can support loads up to 1A and are 100% duty cycle capable.

Two 300 mA LDOs are provided so that sensitive analog loads can be supported.

The default power channel sequencing is built-in, according to the requirements of the Microchip MPU device.

The MCP16502 features a low no-load operational quiescent current, and draws less than 10 µA in full shutdown.

Active discharge resistors are provided on each output. All buck channels support safe start-up into pre-biased outputs.

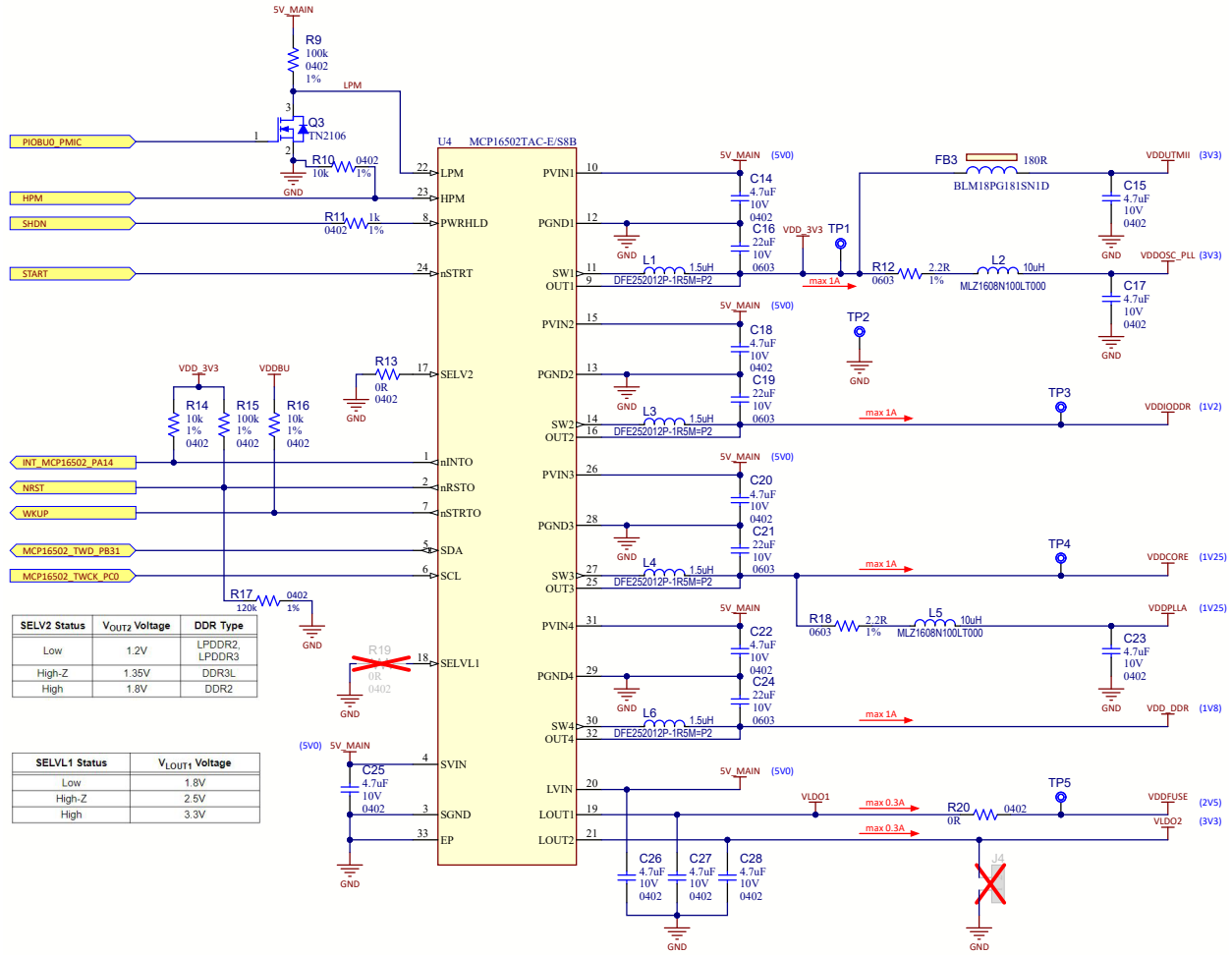
The MCP16502 is available in a 32-pin 5 mm x 5 mm VQFN package with an operating junction temperature range from –40°C to +125°C. It is AEC-Q100 Grade 2 (TAMB=105°C) qualified. For more information on the MCP16502, refer to the product web page.

The MCP16502TAC comes preset to supply all the voltage rails required by the system:

- 3.3V DC/DC supplies SAMA5D29 I/O pads and devices (VDD_3V3)
- 1.2V DC/DC supplies SAMA5D29 LPDDR2 pads (VDDIODDR) and device
- 1.25V DC/DC supplies SAMA5D29 core (VDDCORE)
- 1.8V DC/DC supplies LPDDR2 core (VDD_DDR)
- 2.5V LDO supplies SAMA5D29 fuse power input (VDDFUSE)

The figure below shows the power management scheme.

**Figure 3-5.** Power Management Unit Schematic




| SELV2 Status | $V_{OUT2}$ Voltage | DDR Type |
|---|---|---|
| Low | 1.2V | LPDDR2, LPDDR3 |
| High-Z | 1.35V | DDR3L |
| High | 1.8V | DDR2 |

| SELVL1 Status | $V_{LOUT1}$ Voltage |
|---|---|
| Low | 1.8V |
| High-Z | 2.5V |
| High | 3.3V |

**Table 3-1.** MCP16502 TWI Address

| Device | 7-bit client address |
|---|---|
| MCP16502 | 1011_011 |

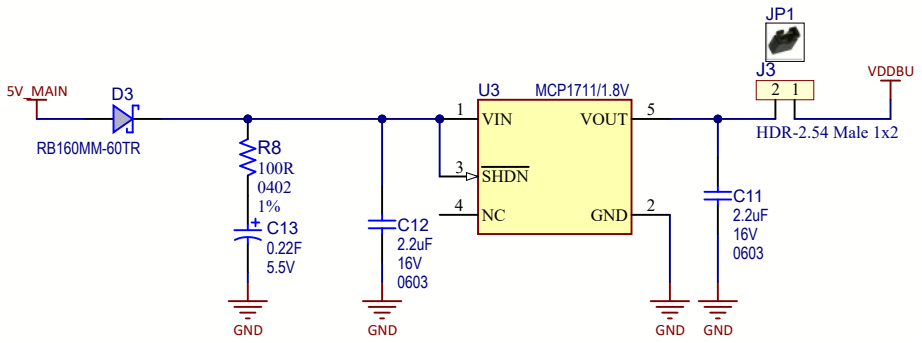
### 3.1.3 Battery Unit

A 5.0V battery (supercapacitor C13) is implemented to permanently maintain the VDDBU voltage. An LDO (U3 - MCP1711) is assigned to this supercap to decrease the VDDBU voltage down to 1.8V. This allows the VDDBU domain power consumption to be decreased. The LDO has an ultra-low quiescent current and can drive a very low load. For more information on the device, refer to the product web page.

This function allows the user to shut down the MPU and the system, thus entering low-power mode, and still maintain the custom configuration that was previously set in the MPU backup area.

Jumper JP1/J3 must be in place for proper operation of the MPU, and can be removed if the user wants to bring the MPU back to the initial configuration, by resetting the Backup registers (BUREG).

**Figure 3-6.** SAMA5D29-Curiosity Backup Circuitry Schematic




**WARNING** Ensure the board is powered off before removing the JP1/J3 jumper.

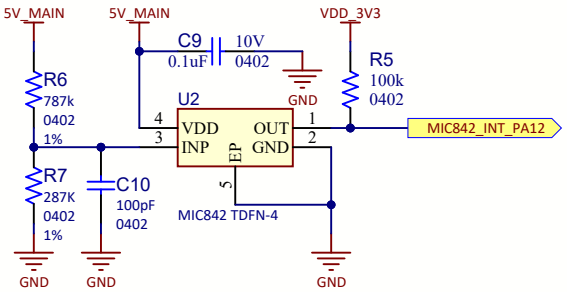
### 3.1.4 Power Input Voltage Supervisor

The SAMA5D29-Curiosity board is equipped with the MIC842 Voltage Supervisor. The purpose of this device is to signal the MPU via a fast interrupt of any power failure that might occur. The interrupt is then handled at system level to shut down the CKE enable signal from the LPDDR2 controller by using the bit LPDDR2_LPDDR3_PWOFF in the MPDDRC Low-Power register (MPDDRC_LPR), during the full period the power rails are powering down.

This mechanism is intended to preserve the LPDDR2 device against uncontrolled power-off sequences, which can be applied only up to 400 times in the life of an LPDDR2 device.

For more information on the MIC842 device, refer to the product web page.

**Figure 3-7.** Voltage Supervisor




## 3.2 Processor

The SAMA5D29 is a high-performance, ultra-low-power Arm Cortex®-A5 CPU-based embedded microprocessor (MPU) running up to 500 MHz, with support for multiple memories such as DDR2, DDR3, DDR3L, LPDDR1, LPDDR2, LPDDR3, QSPI and e.MMC Flash, and SLC/MLC parallel NAND Flash memory up to 32-bit ECC. It integrates the Arm Neon™ SIMD engine for accelerated multimedia and signal processing, a configurable 128-Kbyte L2 cache and a floating point unit (FPU) for high-precision computing.

The comprehensive peripheral set includes an LCD TFT controller with overlays for hardware-accelerated image composition, an image sensor controller, audio support through I2S, SSC, a stereo Class D amplifier and a digital microphone. Connectivity peripherals include a 10/100 EMAC with IEEE®1588 support, USBs, two ISO-compliant CAN-FD interfaces, FLEXCOMs, UARTs, SPIs and two QSPIs, SDIO/SD/e.MMCs, and TWIs/I2C.

Refer to the SAMA5D29 Data Sheet for more information.

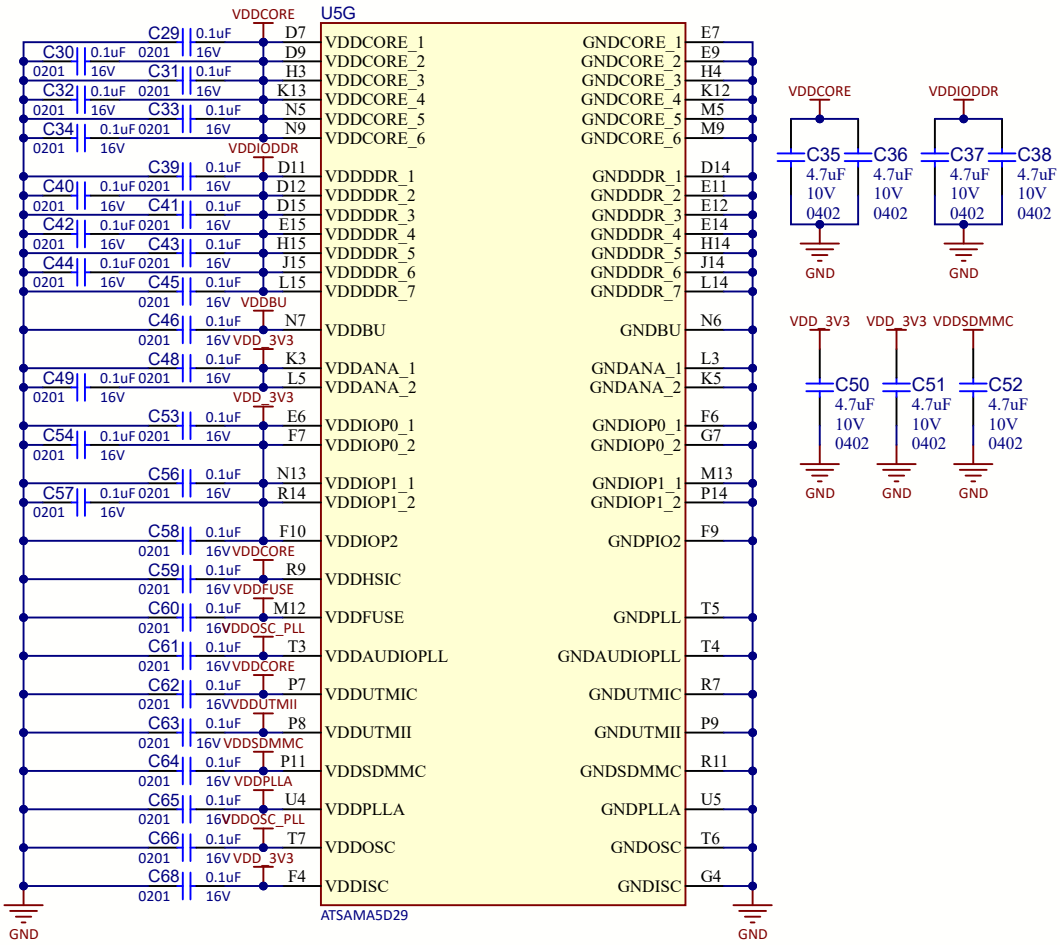
### 3.2.1 Processor Power Supplies

The power management unit IC (MCP16502) provides all power supplies required by the SAMA5D29 MPU:

- 1.25V for the core and PLL power rail (VDDCORE, VDDPLLA, VDDUTMIC, VDDHSIC)
- 1.2V for the memory I/O rail (VDDIODDR)
- 3.3V for I/Os, oscillators, analog and digital power rails (VDDANA, VDDIOP0, VDDIOP1, VDDIOP2, VDDOSC, VDDISC, etc.).
- 2.5V for fuse rail (VDDFUSE)

Decoupling capacitors are placed close to the MPU power pins to stabilize the voltage rails.

**Figure 3-8.** SAMA5D29 Power Decoupling




### 3.2.2 Main Configuration and Control

The figure below shows the main block for processor configuration and control.

**Figure 3-9.** Processor Main Configuration and Control

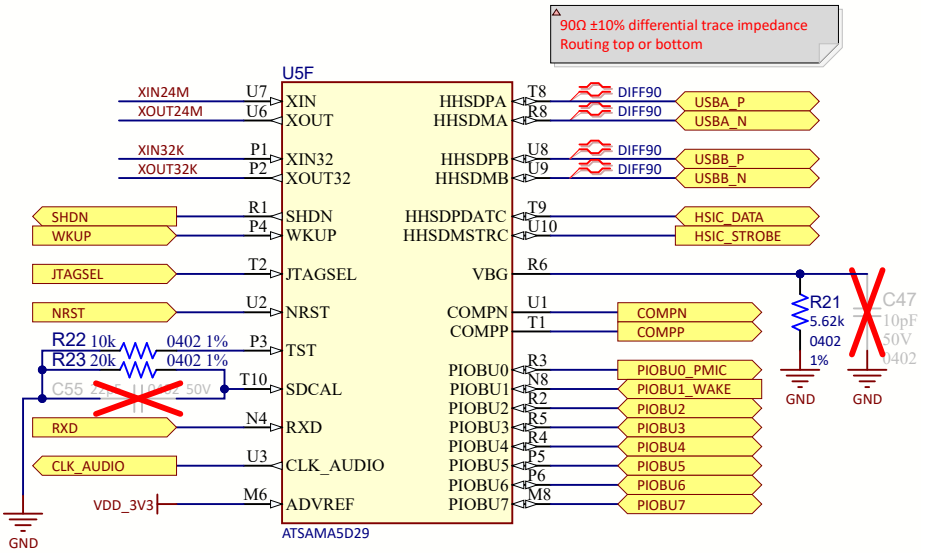



**Table 3-2.** Processor Main Configuration and Control

| Pin Name | Type | Used for |
|---|---|---|
| XIN | Input | Main clock oscillator input |
| XOUT | Output | Main clock oscillator output |
| XIN32 | Input | Slow clock oscillator input |
| XOUT32 | Output | Slow clock oscillator output |
| SHDN | Output | Signal used to enable and disable an external power supply circuit |
| WKUP | Input | Event detection input pin used to wake up the processor from Shutdown state |
| JTAGSEL | Input | When pulled high enables the JTAG boundary scan |
| NRST | Input | Processor reset input |
| TST | Input | Reserved for processor manufacturing tests |
| SDCAL | Input | SDMMC cell calibration |
| RXD | Input | Low Power Asynchronous Receiver. Wakes up the MPU on data matching. |
| CLK_AUDIO | Output | Audio PLL clock output |
| ADVREF | Input | ADC reference voltage input |
| HHSDPA | Bidirectional | USB A positive differential signal |
| HHSDMA | Bidirectional | USB A negative differential signal |
| HHSDPB | Bidirectional | USB B positive differential signal |
| HHSDMB | Bidirectional | USB B negative differential signal |
| HHSDPDATC | Bidirectional | HSIC Data signal |
| HHSDMSTRC | Bidirectional | HSIC Strobe signal |
| BG | Input | USB external tuning |
| COMPN | Input | Analog comparator inverting input |
| COMPP | Input | Analog comparator non-inverting input |
| PIOBU0 | Bidirectional | Tamper I/O pin 0 |
| PIOBU1 | Bidirectional | Tamper I/O pin 1 |

| .....continued | | |
|---|---|---|
| **Pin Name** | **Type** | **Used for** |
| PIOBU2 | Bidirectional | Tamper I/O pin 2 |
| PIOBU3 | Bidirectional | Tamper I/O pin 3 |
| PIOBU4 | Bidirectional | Tamper I/O pin 4 |
| PIOBU5 | Bidirectional | Tamper I/O pin 5 |
| PIOBU6 | Bidirectional | Tamper I/O pin 6 |
| PIOBU7 | Bidirectional | Tamper I/O pin 7 |

### 3.2.3 Clock Circuitry

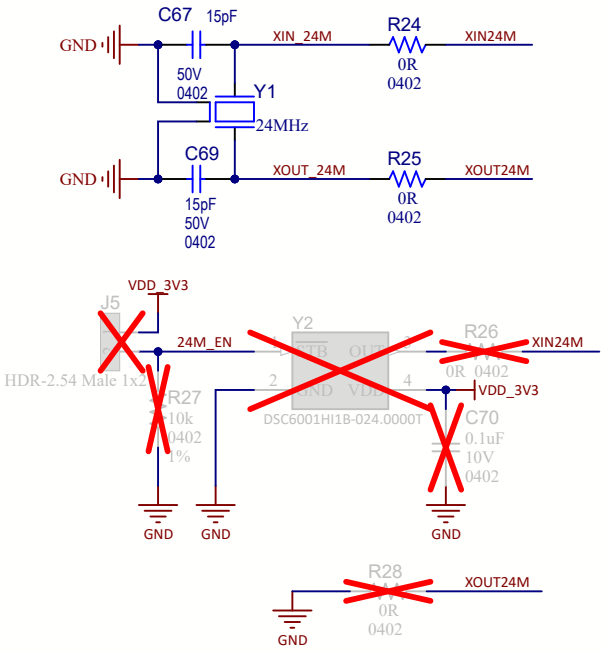
The embedded MPU generates the required clocks based on two oscillators: one slow clock (SLCK) oscillator running at 32.768 kHz and one main clock oscillator running at 24 MHz.

#### 3.2.3.1 Main Clock Circuitry

The main clock oscillator is implemented with the crystal oscillator ECS-240-10-37B2-JTN-TR.

For evaluation purposes, the user can mount a 1.6 mm x 1.2 mm size MEMS oscillator instead of the crystal, using the PCB footprint reservation (Y2). In that case, remove resistors R24 and R25, populate resistors R26 and R28, capacitor C70 and optionally R27 and J5.

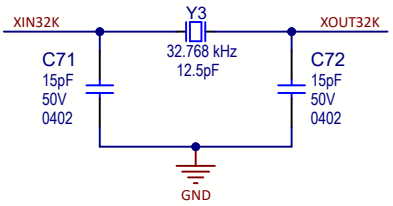
**Figure 3-10.** Processor Main Clock Schematic




#### 3.2.3.2 Slow Clock Circuitry

The slow clock oscillator is implemented with an FC-12M 32.7680KA-A3 crystal device.

**Figure 3-11.** Processor Slow Clock Schematic



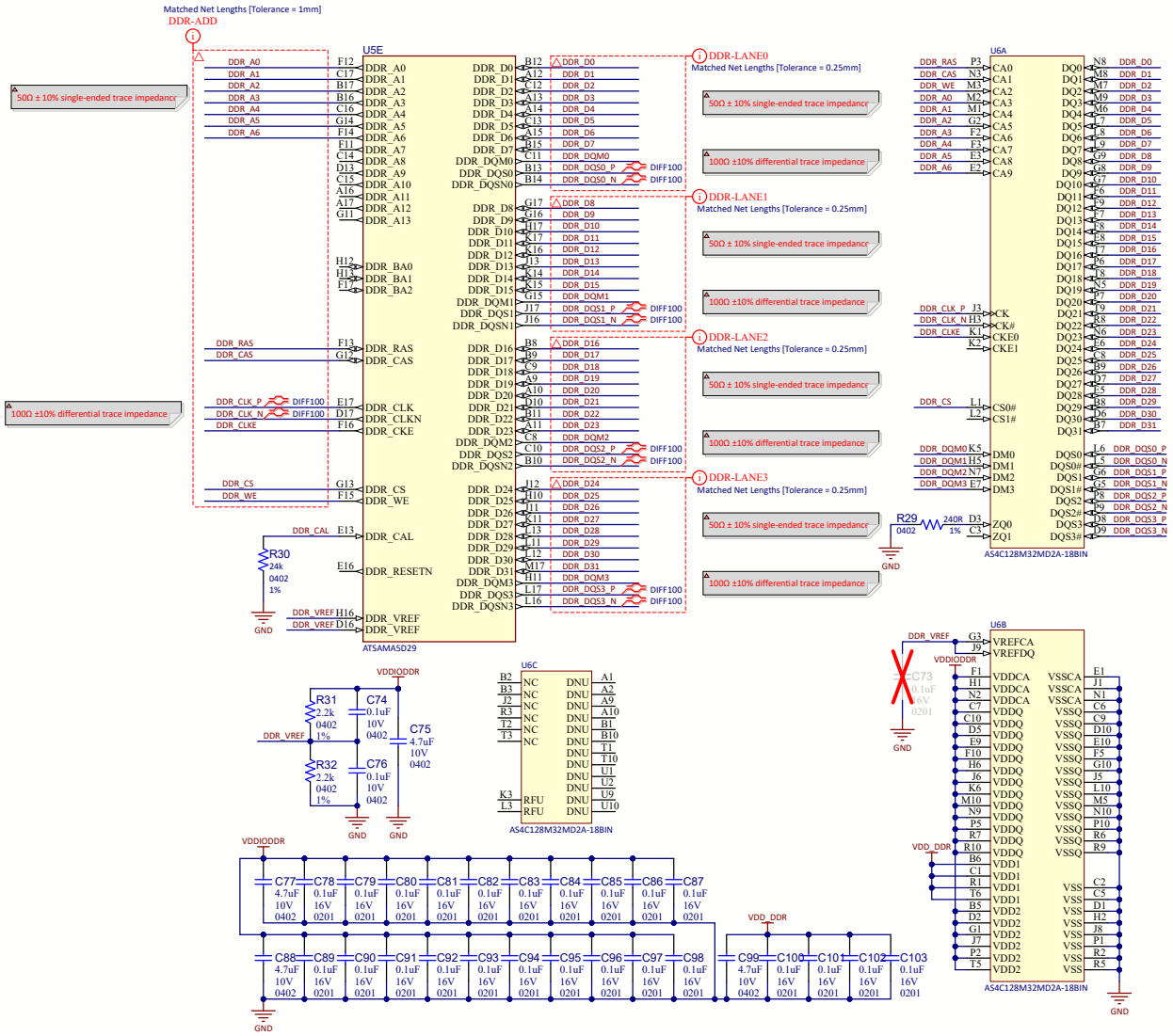

### 3.2.4 DDR Controller and DDR3L Memory Device

The DDR-SDRAM Controller (MPDDRC) maximizes memory bandwidth and minimizes transaction latency through the DDR-SDRAM protocol. The MPDDRC extends the memory capabilities of a chip by providing the interface to the external 16-bit or 32-bit DDR-SDRAM device.

One LPDDR2 memory (4-Gbit AS4C128M32MD2A-18BIN = 16 Mwords x 32 bits x 8 banks) is used as the main system memory, totaling 512 Mbytes of SDRAM on the board. The memory bus is 32 bits wide and operates with a frequency of up to 166 MHz.

The DDR_VREF pin serves as a voltage reference input for the DDR I/Os when DDR or LPDDR external SDRAM memories are used.

**Figure 3-12.** Processor MPDDRC Controller and LPDDR2 Memory Device Schematics




## 3.2.5 Processor PIOs

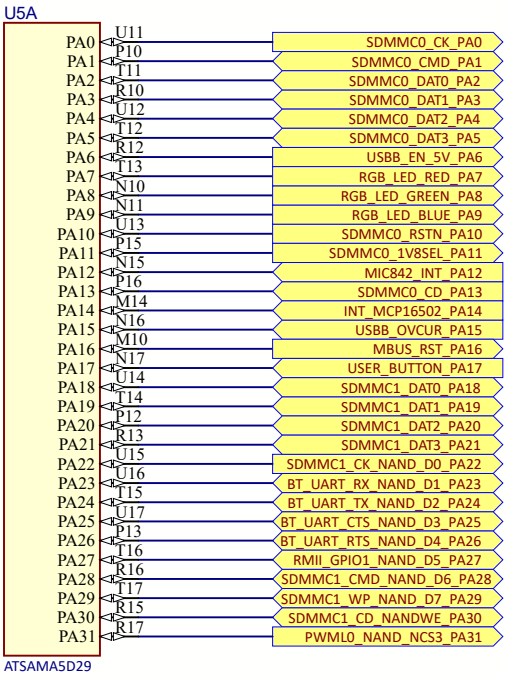
This section describes all the signals connected to the SAMA5D29 MPU ports. Some of the ports are multiplexed to accommodate more devices on the board and to showcase all the functions the SAMA5D29 MPU can address off a single PIO wire. Some of the ports that share multiple functions are split through passive resistors placed on the board as close to the MPU as possible, but are configured so that only one function is available at a time and it requires manual replacement of some resistors to access the alternate function.

### 3.2.5.1 PIOA Bank

The PIOA bank is mainly used for the two SDMMC interfaces over power rails VDDSDMMC and VDDIOP1, respectively.

The following schematic shows the PIOA bank distribution.

**Figure 3-13.** SAMA5D29 PIOA Bank Distribution




The following table describes each PIOA bank function.

**Note:** RPi stands for “Raspberry Pi”. Raspberry Pi is a trademark of Raspberry Pi Trading.

**Table 3-3.** SAMA5D29 PIOA Bank Pin Assignment and Signal Description

| PIO | Power Rail | Function | Signal Description |
|---|---|---|---|
| PA0 | VDDSDMMC | SDMMC0_CK | microSD Card clock signal |
| PA1 | VDDSDMMC | SDMMC0_CMD | microSD Card command line |
| PA2 | VDDSDMMC | SDMMC0_DAT0 | microSD Card data line 0 |
| PA3 | VDDSDMMC | SDMMC0_DAT1 | microSD Card data line 1 |
| PA4 | VDDSDMMC | SDMMC0_DAT2 | microSD Card data line 2 |
| PA5 | VDDSDMMC | SDMMC0_DAT3 | microSD Card data line 3 |
| PA6 | VDDSDMMC | PA6 | USBB 5V power enable |
| PA7 | VDDSDMMC | PA7 | RGB LED red control |
| PA8 | VDDSDMMC | PA8 | RGB LED green control |
| PA9 | VDDSDMMC | PA9 | RGB LED blue control |
| PA10 | VDDSDMMC | SDMMC0_RSTN | microSD Card power reset |
| PA11 | VDDIOP1 | SDMMC0_1V8SEL | microSD card 1V8/3V3 I/O switch |
| PA12 | VDDIOP1 | PA12 | MIC842 Voltage Supervisor interrupt line |
| PA13 | VDDIOP1 | SDMMC0_CD | microSD Card detect |
| PA14 | VDDIOP1 | PA14 | MCP16502 PMIC interrupt line |
| PA15 | VDDIOP1 | PA15 | USBB overcurrent interrupt line |
| PA16 | VDDIOP1 | PA16 | mikroBUS1/2 reset |
| PA17 | VDDIOP1 | PA17 | User button |
| PA18 | VDDIOP1 | SDMMC1_DAT0 | Wi-Fi® SDIO data line 0 |

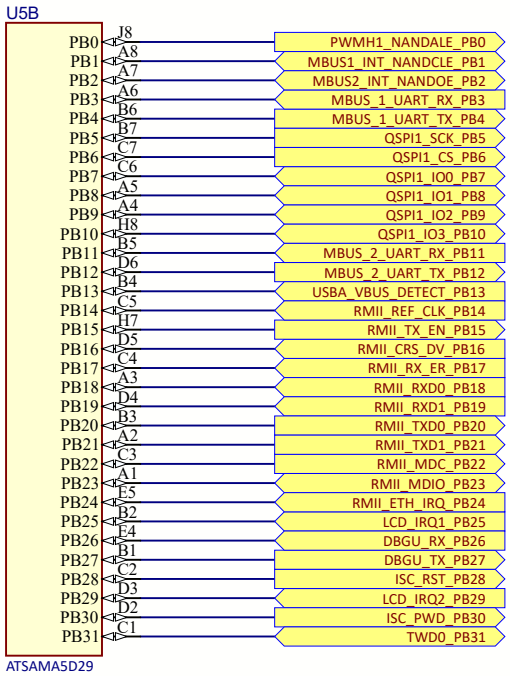
| .....continued | | | |
|---|---|---|---|
| **PIO** | **Power Rail** | **Function** | **Signal Description** |
| PA19 | VDDIOP1 | SDMMC1_DAT1 | Wi-Fi SDIO data line 1 |
| PA20 | VDDIOP1 | SDMMC1_DAT2 | Wi-Fi SDIO data line 2 |
| PA21 | VDDIOP1 | SDMMC1_DAT3 | Wi-Fi SDIO data line 3 |
| PA22 | VDDIOP1 | SDMMC1_CK | Wi-Fi SDIO clock signal |
| | | D0 | NAND Flash data line 0 |
| PA23 | VDDIOP1 | FLEXCOM1_IO1 | Bluetooth® UART RX |
| | | D1 | NAND Flash data line 1 |
| PA24 | VDDIOP1 | FLEXCOM1_IO0 | Bluetooth UART TX |
| | | D2 | NAND Flash data line 2 |
| PA25 | VDDIOP1 | FLEXCOM1_IO3 | Bluetooth UART CTS |
| | | D3 | NAND Flash data line 3 |
| PA26 | VDDIOP1 | FLEXCOM1_IO4 | Bluetooth UART RTS |
| | | D4 | NAND Flash data line 4 |
| PA27 | VDDIOP1 | PA27 | 10/100 RMII slot GPIO |
| | | D5 | NAND Flash data line 5 |
| PA28 | VDDIOP1 | SDMMC1_CMD | Wi-Fi SDIO command line |
| | | D6 | NAND Flash data line 6 |
| PA29 | VDDIOP1 | SDMMC1_WP | Wi-Fi SDIO write protect line |
| | | D7 | NAND Flash data line 7 |
| PA30 | VDDIOP1 | SDMMC1_CD | Wi-Fi SDIO card detect |
| | | NWE/NANDWE | NAND Flash write enable signal |
| PA31 | VDDIOP1 | PWML0 | mikroBUS PWM/RPi PWM0 |
| | | NCS3 | NAND Flash chip select signal |

#### 3.2.5.2 PIOB Bank

The PIOB bank is mainly used for the RMII interface, QSPI1 and mikroBUS UART over power rails VDDIOP0.

The following schematic shows the PIOB bank distribution.

**Figure 3-14.** SAMA5D29 PIOB Bank Distribution




The following table describes each PIOB bank function.

**Table 3-4.** SAMA5D29 PIOB Bank Pin Assignment and Signal Description

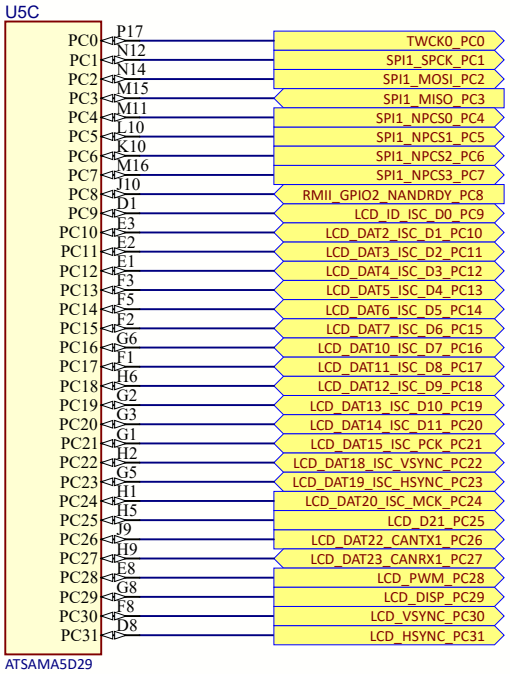
| PIO | Power Rail | Function | Signal Description |
|---|---|---|---|
| PB0 | VDDIOP0 | PWMH1 | mikroBUS2 PWM/RPi PWM1 |
| | | A21/NANDALE | NAND Flash ALE signal |
| PB1 | VDDIOP0 | PB1 | mikroBUS2 interrupt line |
| | | A22/NANDCLE | NAND Flash CLE signal |
| PB2 | VDDIOP0 | PB2 | mikroBUS1 interrupt line |
| | | NRD/NANDOE | NAND Flash output enable signal |
| PB3 | VDDIOP0 | URXD4 | mikroBUS1 UART RX line |
| PB4 | VDDIOP0 | UTXD4 | mikroBUS1 UART TX line |
| PB5 | VDDIOP0 | QSPI1_SCK | QSPI1 Flash clock signal |
| PB6 | VDDIOP0 | QSPI1_CS | QSPI1 Flash chip select line |
| PB7 | VDDIOP0 | QSPI1_IO0 | QSPI1 Flash data line 0 |
| PB8 | VDDIOP0 | QSPI1_IO1 | QSPI1 Flash data line 1 |
| PB9 | VDDIOP0 | QSPI1_IO2 | QSPI1 Flash data line 2 |
| PB10 | VDDIOP0 | QSPI1_IO3 | QSPI1 Flash data line 3 |
| PB11 | VDDIOP0 | URXD3 | mikroBUS2 UART RX line |
| PB12 | VDDIOP0 | UTXD3 | mikroBUS2 UART TX line |
| PB13 | VDDIOP0 | PB13 | USBA VBUS detect line |
| PB14 | VDDIOP0 | GTXCK | 10/100 RMII 50MHz reference clock signal |
| PB15 | VDDIOP0 | GTXEN | 10/100 RMII TX enable signal |
| PB16 | VDDIOP0 | GRXDV | 10/100 RMII RX data valid signal |

| .....continued | | | |
|---|---|---|---|
| **PIO** | **Power Rail** | **Function** | **Signal Description** |
| PB17 | VDDIOP0 | GRXER | 10/100 RMII RX error signal |
| PB18 | VDDIOP0 | GRX0 | 10/100 RMII RX data line 0 |
| PB19 | VDDIOP0 | GRX1 | 10/100 RMII RX data line 1 |
| PB20 | VDDIOP0 | GTX0 | 10/100 RMII TX data line 0 |
| PB21 | VDDIOP0 | GTX1 | 10/100 RMII TX data line 1 |
| PB22 | VDDIOP0 | GMDC | 10/100 RMII management data clock signal |
| PB23 | VDDIOP0 | GMDIO | 10/100 RMII management data I/O line |
| PB24 | VDDIOP0 | PB24 | 10/100 RMII interrupt line |
| PB25 | VDDIOP0 | PB25 | LCD touchscreen interrupt line |
| PB26 | VDDIOP0 | URXD0 | FTDI debug UART RX signal |
| PB27 | VDDIOP0 | UTXD0 | FTDI debug UART TX signal |
| PB28 | VDDIOP0 | PB28 | ISC camera reset line |
| PB29 | VDDIOP0 | PB29 | LCD capacitive buttons interrupt line |
| PB30 | VDDIOP0 | PB30 | ISC camera power down signal |
| PB31 | VDDIOP0 | TWD0 | TWI0 interface data line |

### 3.2.5.3 PIOC Bank

The PIOC bank is mainly used for the LCD interface and SPI1, over power rails VDDIOP1, VDDISC and VDDIOP2. The following schematic shows the PIOC bank distribution.

**Figure 3-15.** SAMA5D29 PIOC Bank Distribution




The following table describes each PIOC bank function.

**Table 3-5.** SAMA5D29 PIOC Bank Pin Assignment and Signal Description

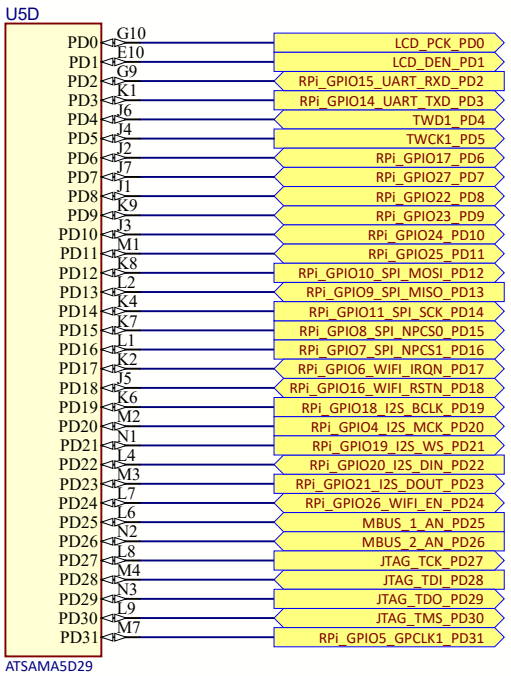
| PIO | Power Rail | Function | Signal Description |
|---|---|---|---|
| PC0 | VDDIOP1 | TWCK0 | TWI0 interface clock signal |
| PC1 | VDDIOP1 | SPI1_SPCK | SPI1 serial clock signal |
| PC2 | VDDIOP1 | SPI1_MOSI | SPI1 host output client input data line |
| PC3 | VDDIOP1 | SPI1_MISO | SPI1 host input client output data line |
| PC4 | VDDIOP1 | SPI1_NPCS0 | SPI1 chip select line 0 – mikroBUS1 |
| PC5 | VDDIOP1 | SPI1_NPCS1 | SPI1 chip select line 1 – mikroBUS2 |
| PC6 | VDDIOP1 | SPI1_NPCS2 | SPI1 chip select line 2 – 10/100 RMII |
| PC7 | VDDIOP1 | SPI1_NPCS3 | SPI1 chip select line 3 – LCD |
| PC8 | VDDIOP1 | PC8 | 10/100 RMII slot GPIO |
| | | NANDRDY | NAND Flash ready/busy signal |
| PC9 | VDDISC | PC9 | LCD one-wire ID memory interface |
| | | ISC_D0 | ISC camera data line 0 |
| PC10 | VDDISC | LCDDAT2 | LCD data line 2 |
| | | ISC_D1 | ISC camera data line 1 |
| | | CANTX0 | CAN0 TX line |
| PC11 | VDDISC | LCDDAT3 | LCD data line 3 |
| | | ISC_D2 | ISC camera data line 2 |
| | | CANRX0 | CAN0 RX line |
| PC12 | VDDISC | LCDDAT4 | LCD data line 4 |
| | | ISC_D3 | ISC camera data line 3 |
| PC13 | VDDISC | LCDDAT5 | LCD data line 5 |
| | | ISC_D4 | ISC camera data line 4 |
| PC14 | VDDISC | LCDDAT6 | LCD data line 6 |
| | | ISC_D5 | ISC camera data line 5 |
| PC15 | VDDISC | LCDDAT7 | LCD data line 7 |
| | | ISC_D6 | ISC camera data line 6 |
| PC16 | VDDISC | LCDDAT10 | LCD data line 10 |
| | | ISC_D7 | ISC camera data line 7 |
| PC17 | VDDISC | LCDDAT11 | LCD data line 11 |
| | | ISC_D8 | ISC camera data line 8 |
| PC18 | VDDISC | LCDDAT12 | LCD data line 12 |
| | | ISC_D9 | ISC camera data line 9 |
| PC19 | VDDISC | LCDDAT13 | LCD data line 13 |
| | | ISC_D10 | ISC camera data line 10 |
| PC20 | VDDISC | LCDDAT14 | LCD data line 14 |
| | | ISC_D11 | ISC camera data line 11 |
| PC21 | VDDISC | LCDDAT15 | LCD data line 15 |
| | | ISC_PCK | ISC camera pixel clock signal |

| .....continued | | | |
|---|---|---|---|
| **PIO** | **Power Rail** | **Function** | **Signal Description** |
| PC22 | VDDISC | LCDDAT18 | LCD data line 18 |
| | | ISC_VSYNC | ISC camera VSYNC signal |
| PC23 | VDDISC | LCDDAT19 | LCD data line 19 |
| | | ISC_HSYNC | ISC camera HSYNC signal |
| PC24 | VDDISC | LCDDAT20 | LCD data line 20 |
| | | ISC_MCK | ISC camera master clock signal |
| PC25 | VDDISC | LCDDAT21 | LCD data line 21 |
| PC26 | VDDIOP2 | LCDDAT22 | LCD data line 22 |
| | | CANTX1 | CAN1 TX signal |
| PC27 | VDDIOP2 | LCDDAT23 | LCD data line 23 |
| | | CANRX1 | CAN1 RX signal |
| PC28 | VDDIOP2 | LCDPWM | LCD backlight PWM signal |
| PC29 | VDDIOP2 | LCDDISP | LCD display enable signal |
| PC30 | VDDIOP2 | LCDVSYNC | LCD VSYNC signal |
| PC31 | VDDIOP2 | LCDHSYNC | LCD HSYNC signal |

### 3.2.5.4 PIOD Bank

The PIOD bank is mainly used for the RPi connector interfaces and GPIOs, and JTAG, over power rails VDDIOP2 and VDDANA. The following schematic shows the PIOD bank distribution.

**Figure 3-16.** SAMA5D29 PIOD Bank Distribution




The following table describes each PIOD bank function.

**Table 3-6.** SAMA5D29 PIOD Bank Pin Assignment and Signal Description

| PIO | Power Rail | Function | Signal Description |
|---|---|---|---|
| PD0 | VDDIOP2 | LCDPCK | LCD pixel clock signal |
| PD1 | VDDIOP2 | LCDDEN | LCD data enable signal |
| PD2 | VDDIOP2 | URXD1 | RPi 40-pin connector UART RX |
| PD3 | VDDANA | UTXD1 | RPi 40-pin connector UART TX |
| PD4 | VDDANA | TWD1 | TWI1 data line |
| PD5 | VDDANA | TWCK1 | TWI1 clock signal |
| PD6 | VDDANA | PD6 | RPi 40-pin connector GPIO17 |
| PD7 | VDDANA | PD7 | RPi 40-pin connector GPIO27 |
| PD8 | VDDANA | PD8 | RPi 40-pin connector GPIO22 |
| PD9 | VDDANA | PD9 | RPi 40-pin connector GPIO23 |
| PD10 | VDDANA | PD10 | RPi 40-pin connector GPIO24 |
| PD11 | VDDANA | PD11 | RPi 40-pin connector GPIO25 |
| PD12 | VDDANA | FLEXCOM4_IO0 | RPi 40-pin connector SPI host output client input data |
| PD13 | VDDANA | FLEXCOM4_IO1 | RPi 40-pin connector SPI host input client output data |
| PD14 | VDDANA | FLEXCOM4_IO2 | RPi 40-pin connector SPI clock signal |
| PD15 | VDDANA | FLEXCOM4_IO3 | RPi 40-pin connector SPI chip select 0 |
| PD16 | VDDANA | FLEXCOM4_IO4 | RPi 40-pin connector SPI chip select 1 |
| PD17 | VDDANA | PD17 | WIFI SDIO interrupt line |
| | | PD17 | RPi 40-pin connector GPIO6 |
| PD18 | VDDANA | PD18 | WIFI SDIO reset line |
| | | PD18 | RPi 40-pin connector GPIO16 |
| PD19 | VDDANA | I2SC0_CK | RPi 40-pin connector I2S bit clock signal |
| PD20 | VDDANA | I2SC0_MCK | RPi 40-pin connector I2S master clock signal |
| PD21 | VDDANA | I2SC0_WS | RPi 40-pin connector I2S word select signal |
| PD22 | VDDANA | I2SC0_DI0 | RPi 40-pin connector I2S data input line |
| PD23 | VDDANA | I2SC0_DO0 | RPi 40-pin connector I2S data output line |
| PD24 | VDDANA | PD24 | WIFI SDIO enable signal |
| | | PD24 | RPi 40-pin connector GPIO26 |
| PD25 | VDDANA | AD6 | mikroBUS1 analog input |
| PD26 | VDDANA | AD7 | mikroBUS2 analog input |
| PD27 | VDDANA | TCK | JTAG test clock signal |
| PD28 | VDDANA | TDI | JTAG test data input line |
| PD29 | VDDANA | TDO | JTAG test data output line |
| PD30 | VDDANA | TMS | JTAG test mode select signal |
| PD31 | VDDANA | PCK0 | RPi 40-pin connector general purpose clock 1 signal |

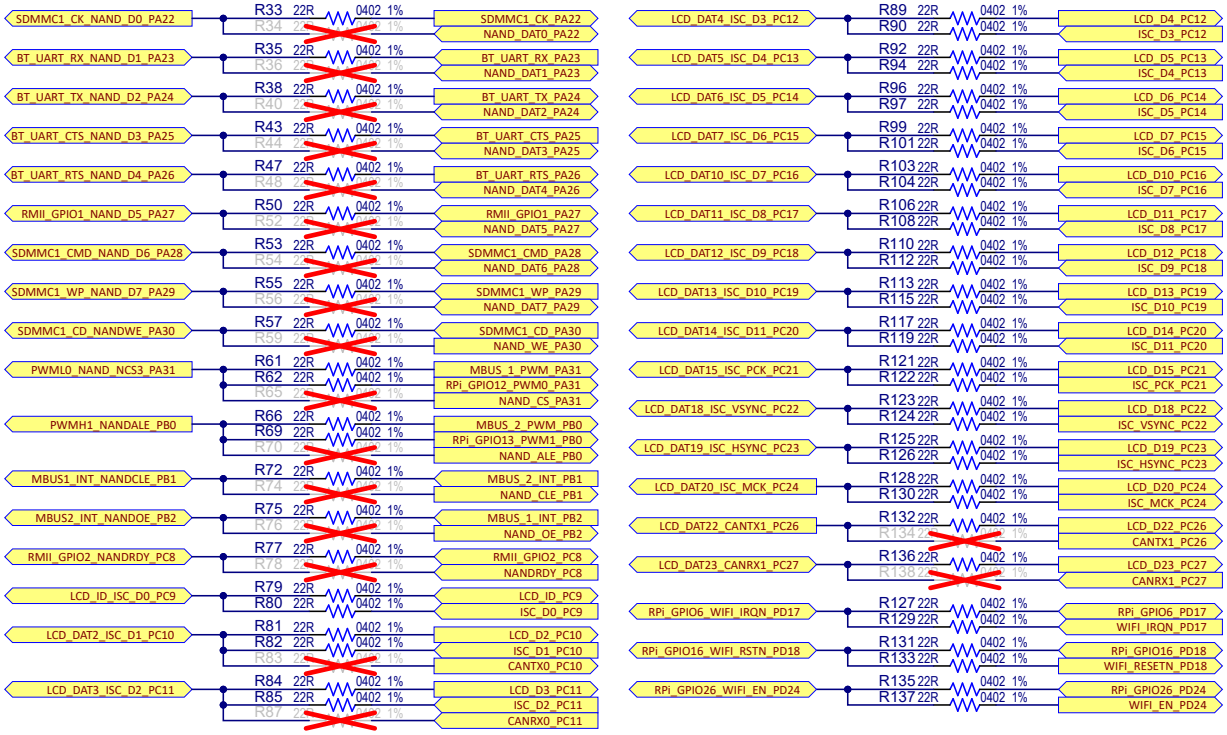
### 3.2.6 Processor Interface Distribution

This section details the processor PIO distribution and explains the procedure necessary to access the multiplexed functions.

### 3.2.6.1 GPIO Distribution

The following schematic shows the processor GPIO function distribution.

**Figure 3-17.** GPIO Distribution Schematic



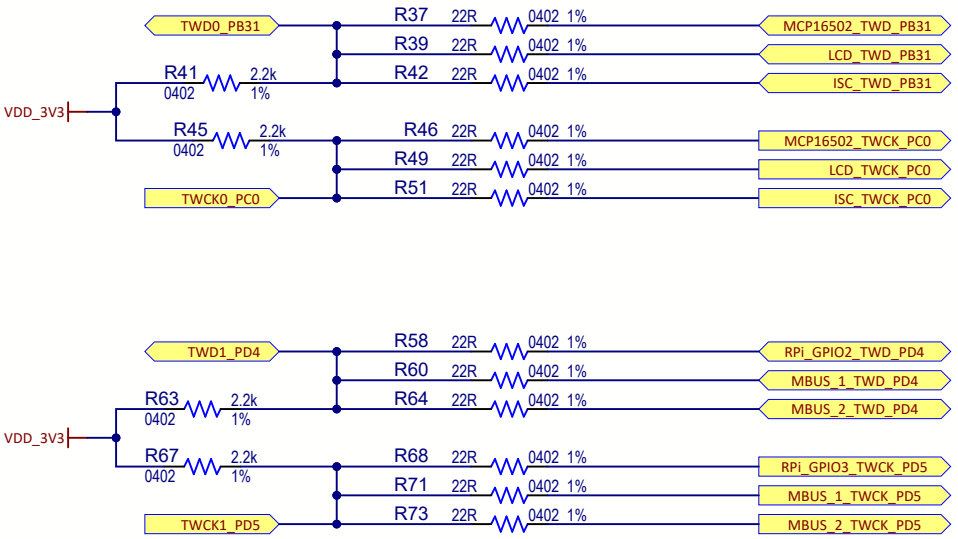

By default, the functions attached to a non-populated resistor (marked with a red cross) are not available. To make it available, the remaining resistors on the corresponding PIO port must be removed and the missing resistor of the desired unavailable function must be populated. This procedure should be repeated on all the required PIOs in order to obtain connectivity on the required signals of an unavailable function.

PIOs with functions that have all the resistors populated do not require any user intervention. In this case, the user can implement only one of the functions at a time, or can develop a composite driver enabling the use of multiple functions at the same time.

### 3.2.6.2 TWI Distribution

The SAMA5D29-Curiosity features two TWIs (Two-wire Interface). The following schematic shows the TWI distribution.

**Figure 3-18.** TWI Distribution Schematic



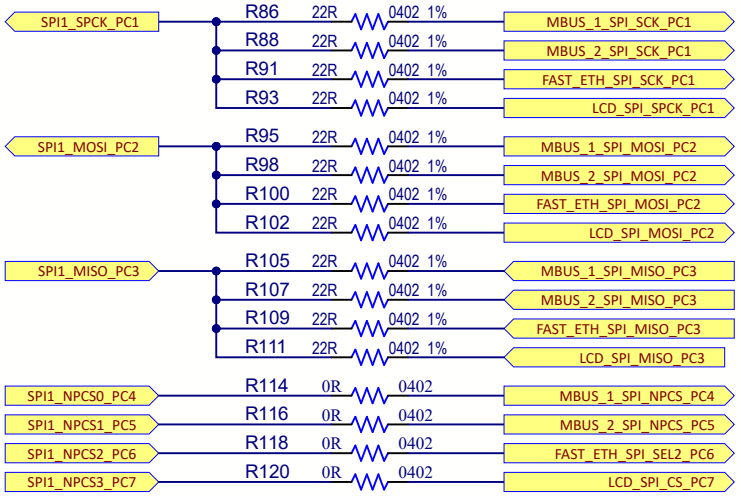

TWI0 (using ports PB31 and PC0) is attached to the MCP16502 PMIC, LCD display interface and ISC camera interface.

TWI1 (using ports PD4 and PD5) is attached to the RPi 40-pin connector, mikroBUS1 and mikroBUS2.

### 3.2.6.3 SPI istribution

The SAMA5D29-Curiosity features one SPI (Serial Peripheral Interface) with four dedicated chip select signals. The following schematic shows the SPI distribution.

**Figure 3-19.** SPI Distribution Schematic




The serial clock and data lines are all shared by the four connected peripherals. Each peripheral has its own dedicated chip select line, provided in the table below.

**Table 3-7.** SPI Chip Select Peripheral Distribution

| Peripheral | Chip Select Number | PIO |
|---|---|---|
| mikroBUS1 | NPCS0 | PC4 |
| mikroBUS2 | NPCS 1 | PC5 |

| .....continued | | |
|---|---|---|
| **Peripheral** | **Chip Select Number** | **PIO** |
| 10/100 RMII slot | NPCS 2 | PC6 |
| LCD display connector | NPCS 3 | PC7 |

## 3.3 On-board Memories

The SAMA5D29 MPU features a MultiPort DDR Memory Controller (MPDDRC), a Quad Serial Peripheral Interface (QSPI) and two Secure Digital MultiMedia Card Controller (SDMMC) to enable interfacing to a wide range of external memories. This section describes the memory devices mounted on the SAMA5D29-Curiosity board:

- One 32-bit, 4-Gbit LPDDR2 SDRAM
- One 64-Mbit Serial quad I/O Flash with pre-programmed EUI-48 MAC ID

Additional memory can be added to the board by:

- installing a microSD Card in the microSD Card slot
- installing an SD Card in the SD Card slot
- using the USB ports

Support depends on the OS driver support.

### 3.3.1 LPDDR2 SDRAM

Refer to 3.2.4. DDR Controller and DDR3L Memory Device for details related to the on-board LPDDR2 memory and the connectivity with the DDR memory controller.

### 3.3.2 Quad SPI Serial Flash

The SAMA5D29-Curiosity board features one Quad Serial Peripheral Interface (QSPI) memory SST26VF064BEUI-104I/SM.

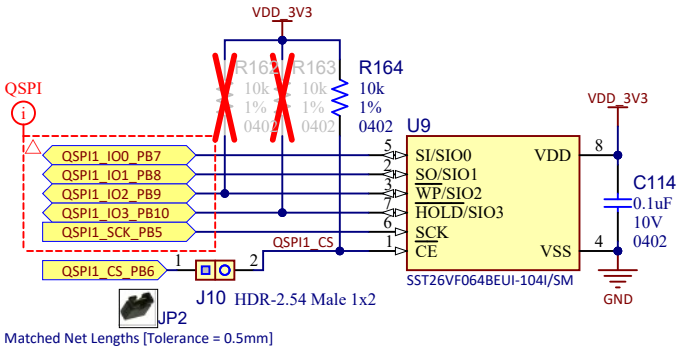
The QSPI is a synchronous serial data link that provides communication with external devices in Host mode.

The QSPI can be used in SPI mode to interface to serial peripherals, such as ADCs, DACs, LCD controllers, CAN controllers and sensors, or in Serial Memory mode to interface to serial Flash memories.

Using the QSPI, the system executes code directly from a serial Flash memory (XIP) without code shadowing to RAM. The serial Flash memory mapping is seen in the system as other memories such as ROM, SRAM, DRAM, embedded Flash memory, etc.

With the support of the Quad SPI protocol, the system can use high-performance serial Flash memories which are small and inexpensive compared to parallel Flash memories.

**Figure 3-20.** Quad SPI Serial Flash Schematic




Keep the JP2 jumper placed on the J10 header to be able to boot from (or use) the QSPI Flash memory.

Remove the JP2 jumper in order to prevent the system from booting from the QSPI Flash memory.

**Table 3-8.** QSPI Flash Signal Description

| PIO | Signal Name | Signal Description |
|---|---|---|
| PB5 | QSPI1_SCK_PB5 | QSPI clock signal |
| PB6 | QSPI1_CS_PB6 | QSPI chip select signal |
| PB7 | QSPI1_IO0_PB7 | QSPI data line 0 |
| PB8 | QSPI1_IO1_PB8 | QSPI data line 1 |
| PB9 | QSPI1_IO2_PB9 | QSPI data line 2 |
| PB10 | QSPI1_IO3_PB10 | QSPI data line 3 |

## 3.4 Peripheral Interfaces

Several interfaces and connectors are implemented in the SAMA5D29-Curiosity to enable the user to test all the features offered by the MPU and to facilitate a reference design for future customer applications.

This section describes the following peripherals mounted on the SAMA5D29-Curiosity board:

- 10/100 RMII Ethernet Interface
- USB Host/Device Interface
- Liquid Crystal Display (LCD) Interface
- ISC Camera Interface
- Secure Digital Multimedia Cards (SDMMC)
- Dual mikroBUS Click Interfaces
- RPi 40-pin GPIO Interface
- Multifunction 20-pin Connector
- Debug Interface
- User Interface
- Extra pin connectors

### 3.4.1 10/100 RMII Ethernet Interface

The SAMA5D29-Curiosity board exposes all the necessary RMII signals provided by the embedded Ethernet MAC controller. The RMII slot is a 4-piece (J15, J16, J17, J18) 30-pin connector. This allows

connectivity to multiple inexpensive add-on boards equipped with RMII compatible PHYs and switches. Microchip provides a wide range of compatible Ethernet daughter boards which can be used for testing and evaluation. The list of Ethernet device daughter boards is provided below and is subject to future additions.

- AC320004-3 - LAN8720A Ethernet PHY
- AC320004-4 - LAN9303 switch
- AC320004-5 - KSZ8041 Ethernet PHY
- AC320004-6 - KSZ8061 Ethernet PHY
- AC320004-7 - KSZ8863 switch
- EV06P90A - LAN8670 10BASE-T1S Ethernet PHY
- EV48S68A - LAN8770 100BASE-T1 Ethernet PHY

The SAMA5D29-Curiosity board supplies 3.3V power to the daughter board.

An on-board 50 MHz oscillator provides the RMII REFCLK to both the MPU and the RMII connector for the daughter board.

Separate SPI and MDIO interfaces at the connector allow the MPU to manage the daughter board device.

An individual unique 48-bit MAC address (Ethernet hardware address) is allocated to this product and is stored in the Microchip SST26VF064BEUI-104I/SM QSPI Flash memory.

**Figure 3-21.** 10/100 RMII Ethernet Interface Schematic

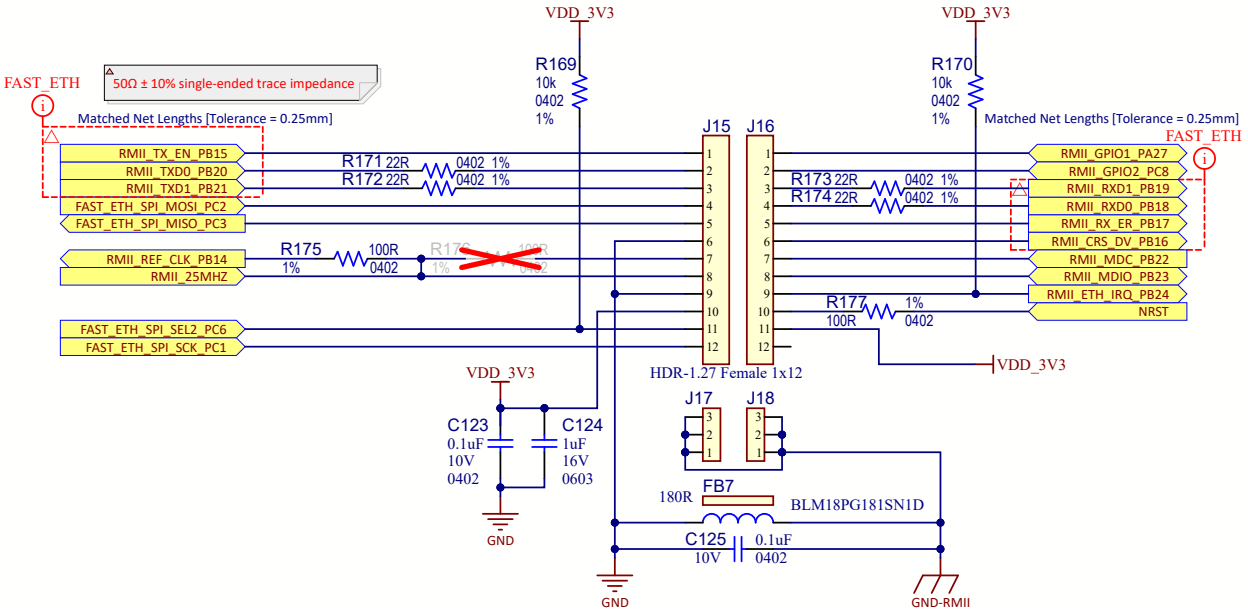



**Figure 3-22.** 50 MHz Clock Source for RMII Interface Schematic

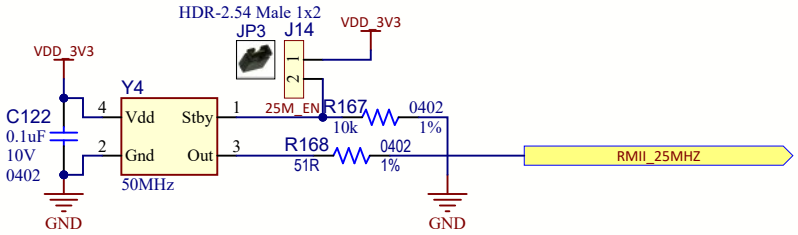


**Table 3-9.** 10/100 RMII Interface Signal Description

| PIO | Signal Name | Signal Description |
|---|---|---|
| PB14 | RMII_REF_CLK_PB14 | RMII 50 MHz reference clock signal |
| PB15 | RMII_TX_EN_PB15 | RMII transmit enable signal |
| PB16 | RMII_CRS_DV_PB16 | RMII receive data valid signal |
| PB17 | RMII_RX_ER_PB17 | RMII receive error signal |
| PB18 | RMII_RXD0_PB18 | RMII RX data line 0 |
| PB19 | RMII_RXD1_PB19 | RMII RX data line 1 |
| PB20 | RMII_TXD0_PB20 | RMII TX data line 0 |
| PB21 | RMII_TXD1_PB21 | RMII TX data line 1 |
| PB22 | RMII_MDC_PB22 | RMII management data clock signal |
| PB23 | RMII_MDIO_PB23 | RMII management data I/O line |
| PB24 | RMII_ETH_IRQ_PB24 | RMII interrupt line |
| PC1 | FAST_ETH_SPI_SCK_PC1 | Ethernet device SPI clock signal |
| PC2 | FAST_ETH_SPI_MOSI_PC2 | Ethernet device SPI host output client input data line |
| PC3 | FAST_ETH_SPI_MISO_PC3 | Ethernet device SPI host input client output data line |
| PC6 | FAST_ETH_SPI_SEL2_PC6 | Ethernet device SPI chip select signal |
| PC8 | RMII_GPIO2_PC8 | Ethernet device GPIO signal |
| PA27 | RMII_GPIO1_PA27 | Ethernet device GPIO signal |

### 3.4.2 USB Host/Device Interface

The USB (Universal Serial Bus) is a hot-pluggable general-purpose high-speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 Specification defines data transfer rates as high as 480 Mbps (also known as High-Speed USB). A USB host bus connector uses four pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin.

The SAMA5D29-Curiosity board features two USB communication ports named USB-A and USB-B.

The USB-A port can act only as a USB device interface and can be accessed via the USB Type-C connector (J1).

Two resistors are placed on its power rail to form a voltage divider, converting 5V into 3.3V that is then used to signal the presence of a USB host to the MPU.

The USB-A port is used as a power source, as mentioned in USB Supply Input. In most cases, this port is limited to 500 mA.

**Figure 3-23.** USB A Port

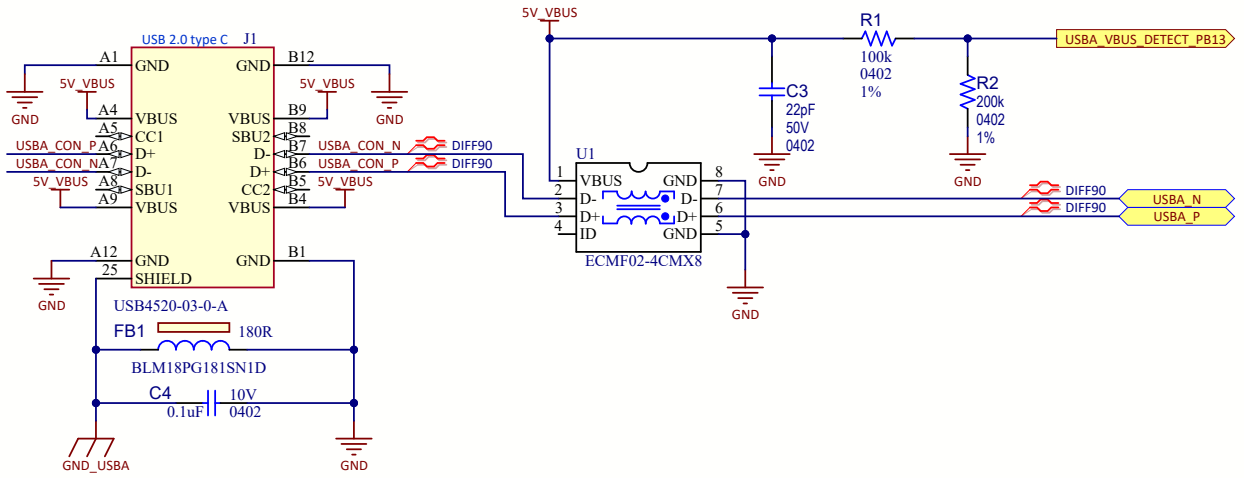



**Table 3-10.** USB-A Connector Signal Description

| Pin No | Signal Name | Signal Description |
|---|---|---|
| A4, A9, B4, B9 | 5V_VBUS | USB 5V power input |
| A6, B6 | USBA_CON_N | USB port data minus |
| A7, B7 | USBA_CON_B | USB port data plus |
| A1, A12, B1, B12 | GND | Ground |

**Table 3-11.** USB-A PIO Signal Description

| PIO | Signal Name | Signal Description |
|---|---|---|
| PB13 | USBA_VBUS_DETECT_PB13 | VBUS detection |

The USB-B port is connected to the USB Type-A connector and acts as host.

**Figure 3-24.** USB B Port Schematic

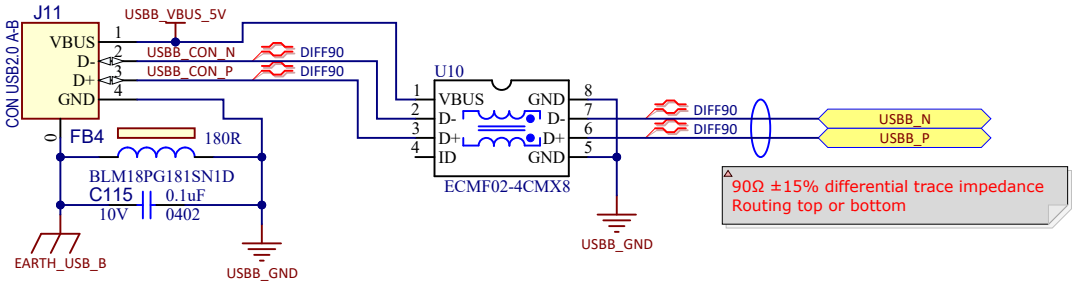



**Table 3-12.** USB-B Connector Signal Description

| Pin No | Signal Name | Signal Description |
|---|---|---|
| 1 | USBB_VBUS_5V | USB 5V power output |
| 2 | USBB_CON_N | USB port data minus |
| 3 | USBB_CON_B | USB port data plus |
| 4 | USBB_GND | Ground |

In Host mode, the USB Host port B is equipped with 500 mA high-side power switch to enable self-powered and bus-powered applications. The USBB_EN_PA6 signal controls the current limiting power switch MIC2025, which in turn supplies power to a client device. Per the USB specification, bus-powered USB 2.0 devices are limited to a maximum of 500 mA, therefore the MIC2025 limits the current and indicates an overcurrent with the USBB_OVCUR_PA15 signal. For more information about the MIC2025, refer to the product web page.

**Figure 3-25.** USB-B Host Power Schematic

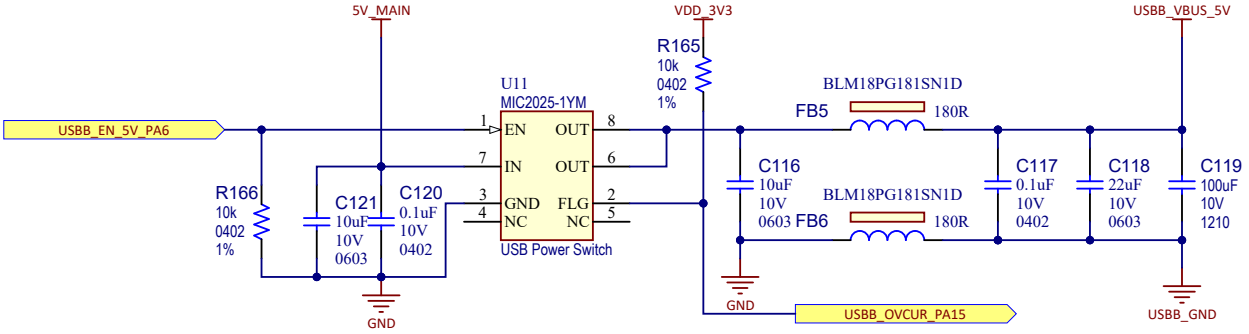



**Table 3-13.** USB-B PIO Signal Description

| PIO | Signal Name | Signal Description |
|---|---|---|
| PA6 | USBB_EN_PA6 | USB-B host power enable signal |
| PA15 | USBB_OVCUR_PA15 | USB-B power overcurrent interrupt line |

### 3.4.3 Liquid Crystal Display (LCD) Interface

The SAMA5D29-Curiosity board provides a connector with 18 bits of data and control signals to the LCD interface.

Optional displays such as AC320005-5 (refer to the product web page) or AC320005-4 (refer to the product web page) can be connected to the board.

The connector provides two PIOs as interrupts, one SPI and a TWI port to interface the MaXTouch® touch controller or QTouch® button controller embedded on the LCD module.

In order to operate correctly with various LCD modules, two power supplies are available: 3.3V and 5V DC (default). The selection is made with 0R resistors.

J23 is a 0.5-mm pitch, top contacts, 50-pin FPC header. It gives access to the LCD signals.

**Figure 3-26.** LCD Connector Schematic

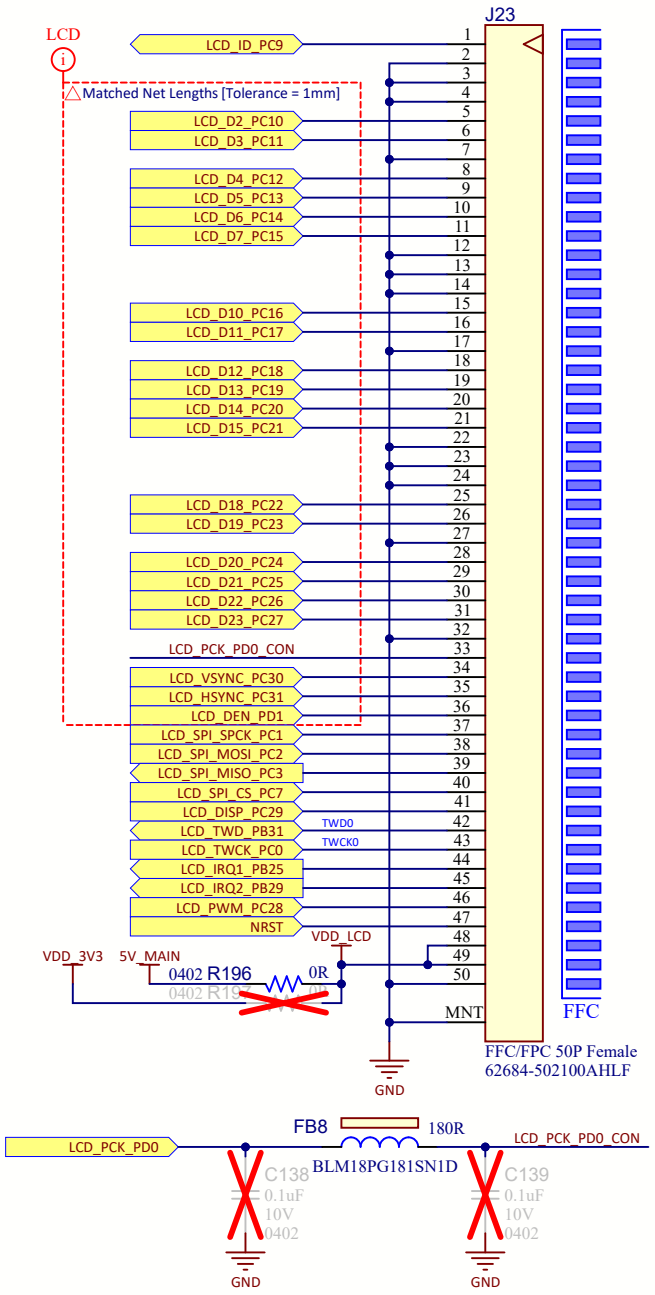



**Table 3-14.** LCD Connector Signal Description

| Pin No | LCD Pin | PIO | Signal | Function |
|---|---|---|---|---|
| 1 | ID | PC9 | LCD_ID_PC9 | LCD one-wire ID memory interface |
| 2 | GND | – | GND | Ground |
| 3 | GND | – | GND | Ground |
| 4 | GND | – | GND | Ground |
| 5 | LCDDAT2 | PC10 | LCD_D2_PC10 | LCD Data line 2 |
| 6 | LCDDAT3 | PC11 | LCD_D3_PC11 | LCD Data line 3 |
| 7 | GND | – | GND | Ground |

.....continued

| Pin No | LCD Pin | PIO | Signal | Function |
|---|---|---|---|---|
| 8 | LCDDAT4 | PC12 | LCD_D4_PC12 | LCD Data line 4 |
| 9 | LCDDAT5 | PC13 | LCD_D5_PC13 | LCD Data line 5 |
| 10 | LCDDAT6 | PC14 | LCD_D6_PC14 | LCD Data line 6 |
| 11 | LCDDAT7 | PC15 | LCD_D7_PC15 | LCD Data line 7 |
| 12 | GND | – | GND | Ground |
| 13 | GND | – | GND | Ground |
| 14 | GND | – | GND | Ground |
| 15 | LCDDAT10 | PC16 | LCD_D10_PC16 | LCD Data line 10 |
| 16 | LCDDAT11 | PC17 | LCD_D11_PC17 | LCD Data line 11 |
| 17 | GND | – | GND | Ground |
| 18 | LCDDAT12 | PC18 | LCD_D12_PC18 | LCD Data line 12 |
| 19 | LCDDAT13 | PC19 | LCD_D13_PC19 | LCD Data line 13 |
| 20 | LCDDAT14 | PC20 | LCD_D14_PC20 | LCD Data line 14 |
| 21 | LCDDAT15 | PC21 | LCD_D15_PC21 | LCD Data line 15 |
| 22 | GND | – | GND | Ground |
| 23 | GND | - | GND | Ground |
| 24 | GND | - | GND | Ground |
| 25 | LCDDAT18 | PC22 | LCD_D18_PC22 | LCD Data line 18 |
| 26 | LCDDAT19 | PC23 | LCD_D19_PC23 | LCD Data line 19 |
| 27 | GND | - | GND | Ground |
| 28 | LCDDAT20 | PC24 | LCD_D20_PC24 | LCD Data line 20 |
| 29 | LCDDAT21 | PC25 | LCD_D21_PC25 | LCD Data line 21 |
| 30 | LCDDAT22 | PC26 | LCD_D22_PC26 | LCD Data line 22 |
| 31 | LCDDAT23 | PC27 | LCD_D23_PC27 | LCD Data line 23 |
| 32 | GND | - | GND | Ground |
| 33 | LCDPCK | PD0 | LCD_PCK_PD0 | LCD pixel clock signal |
| 34 | LCDVSYNC | PC30 | LCD_VSYNC_PC30 | LCD VSYNC signal |
| 35 | LCDHSYNC | PC31 | LCD_HSYNC_PC31 | LCD HSYNC signal |
| 36 | LCDDEN | PD1 | LCD_DEN_PD1 | LCD data enable signal |
| 37 | SPI_SPCK | PC1 | LCD_SPI_SPCK_PC1 | LCD SPI clock signal |
| 38 | SPI_MOSI | PC2 | LCD_SPI_MOSI_PC2 | LCD SPI host output client input data line |
| 39 | SPI_MISO | PC3 | LCD_SPI_MISO_PC3 | LCD SPI host input client output data line |
| 40 | SPI_CS | PC7 | LCD_SPI_CS_PC7 | LCD SPI chip select signal |
| 41 | LCDDISP | PC29 | LCD_DISP_PC29 | LCD display enable |
| 42 | TWD | PB31 | LCD_TWD_PB31 | LCD TWI data line |
| 43 | TWCK | PC0 | LCD_TWCK_PC0 | LCD TWI clock signal |
| 44 | IRQ1 | PB25 | LCD_IRQ1_PB25 | LCD touchscreen interrupt line |
| 45 | IRQ2 | PB29 | LCD_IRQ2_PB29 | LCD capacitive buttons interrupt line |
| 46 | LCDPWM | PC28 | LCD_PWM_PC28 | LCD backlight PWM signal |

| .....continued | | | | |
|---|---|---|---|---|
| **Pin No** | **LCD Pin** | **PIO** | **Signal** | **Function** |
| 47 | NRST | – | NRST | Reset signal |
| 48 | VDD_LCD | – | VDD_LCD | 3.3V or 5V supply (0R) |
| 49 | VDD_LCD | – | VDD_LCD | 3.3V or 5V supply (0R) |
| 50 | GND | – | GND | Ground |

### 3.4.4 ISC Camera Interface

The Image Sensor Controller (ISC) system manages incoming data from a parallel CMOS/CCD sensor. The system supports a single active interface, as well as the ITU-R BT 656/1120 422 protocol with an 8-bit or 10-bit data width and raw Bayer format. The internal image processor includes adjustable white balance, color filter array interpolation, color correction, gamma correction, 12-bit to 10-bit compression, programmable color space conversion, as well as horizontal and vertical chrominance subsampling module.

On the SAMA5D29-Curiosity, the ISC connector (J24) is not mounted by default.

**Figure 3-27.** ISC Connector Schematic

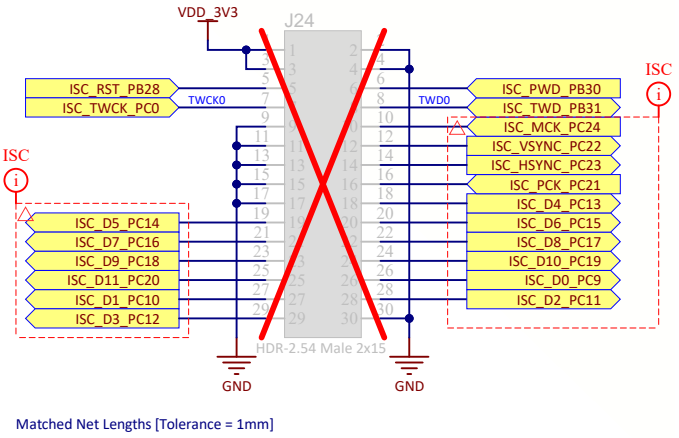



**Table 3-15.** ISC Connector Signal Description

| PIO | Signal Name | Signal Description |
|---|---|---|
| PB28 | ISC_RST_PB28 | ISC reset line |
| PB30 | ISC_PWD_PB30 | ISC power down signal |
| PC0 | ISC_TWCK_PC0 | ISC TWI clock signal |
| PB31 | ISC_TWD_PB31 | ISC TWI data line |
| PC24 | ISC_MCK_PC24 | ISC master clock signal |
| PC22 | ISC_VSYNC_PC22 | ISC VSYNC signal |
| PC23 | ISC_HSYNC_PC23 | ISC HSYNC signal |
| PC21 | ISC_PCK_PC21 | ISC pixel clock signal |
| PC13 | ISC_D4_PC13 | ISC data line 4 |
| PC14 | ISC_D5_PC14 | ISC data line 5 |
| PC15 | ISC_D6_PC15 | ISC data line 6 |
| PC16 | ISC_D7_PC16 | ISC data line 7 |
| PC17 | ISC_D8_PC17 | ISC data line 8 |

| .....continued | | |
|---|---|---|
| **PIO** | **Signal Name** | **Signal Description** |
| PC18 | ISC_D9_PC18 | ISC data line 9 |
| PC19 | ISC_D10_PC19 | ISC data line 10 |
| PC20 | ISC_D11_PC20 | ISC data line 11 |
| PC9 | ISC_D0_PC9 | ISC data line 0 |
| PC10 | ISC_D1_PC10 | ISC data line 1 |
| PC11 | ISC_D2_PC9 | ISC data line 2 |
| PC12 | ISC_D3_PC12 | ISC data line 3 |

### 3.4.5 Secure Digital Multimedia Cards (SDMMC)

The SD (Secure Digital) cards are a non-volatile memory card format used as a mass storage memory in mobile devices.

The SAMA5D29-Curiosity has two Secure Digital Multimedia Card (SDMMC) interfaces that support the MultiMedia Card (e.MMC) Specification V4.51, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. They are compliant with the SD Host Controller Standard V3.0 Specification.

#### 3.4.5.1 SDMMC1 Connector

An 8-bit SD/MMCplus card connector, J7, connected to the SDMMC1 interface, is mounted on the top side of the board. The SDMMC1 communication is based on an 8-pin interface (clock, command, four data and power lines). It includes a card detection switch. In addition, this interface has a write protect pin.

The main purpose of this connector is to accommodate radio modules, such as the ATWILC3000-SD Evaluation Kit (AC164158). Details are available on the Microchip web site. To allow control and additional functionality of the SD format radio module, additional signals are assigned to the SD connector, such as enable, reset, host interrupt and host wake-up.

The board can also use this interface to boot from normal SD cards.

**Figure 3-28.** SDMMC1 Connector Schematic

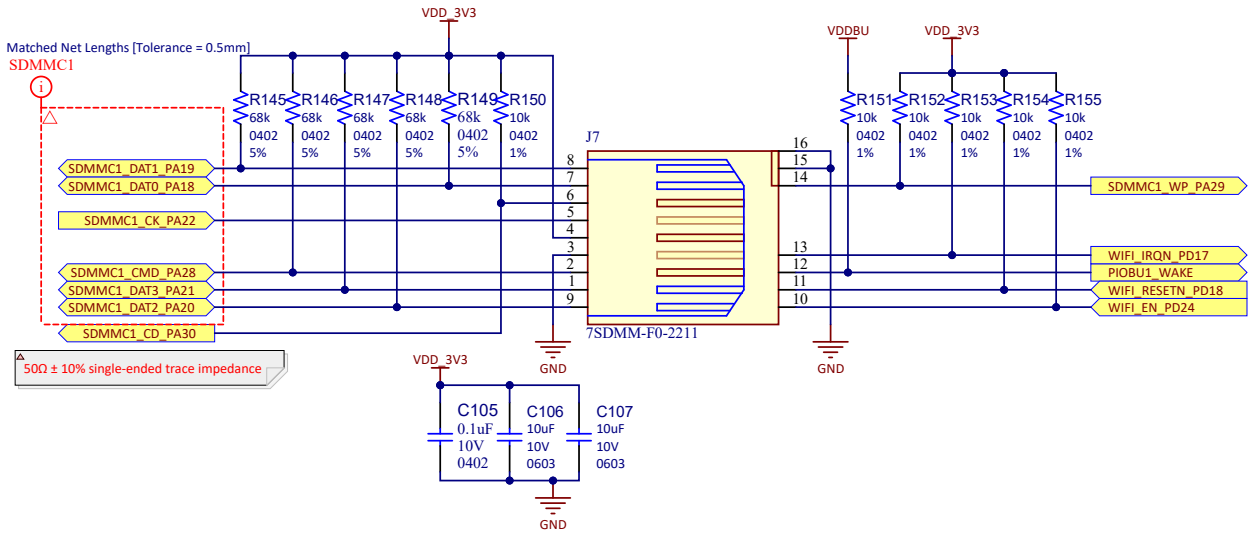


**Table 3-16.** SDMMC1 Connector Signal Description

| PIO | Signal Name | Signal Description |
|---|---|---|
| PA18 | SDMMC1_DAT0_PA18 | SDMMC1 data line 0 |
| PA19 | SDMMC1_DAT1_PA19 | SDMMC1 data line 1 |
| PA20 | SDMMC1_DAT2_PA20 | SDMMC1 data line 2 |
| PA21 | SDMMC1_DAT3_PA21 | SDMMC1 data line 3 |
| PA22 | SDMMC1_CK_PA22 | SDMMC1 clock signal |
| PA28 | SDMMC1_CMD_PA28 | SDMMC1 command line |
| PA29 | SDMMC1_WP_PA29 | SDMMC1 write protect signal |
| PA30 | SDMMC1_CD_PA30 | SDMMC1 card detect signal |
| PD17 | WIFI_IRQN_PD17 | Host interrupt line |
| PD18 | WIFI_RESETN_PD18 | Device reset line |
| PD24 | WIFI_EN_PD24 | Device enable signal |
| PIOBU1 | PIOBU1_WAKE | Host wake-up interrupt |

For radio modules which support Bluetooth, a 6-pin header (J8) providing an UART interface is located near the SD connector to allow the user to connect the Bluetooth UART from the device to the MPU using jumper wires. The provided Bluetooth UART interface supports hardware flow control.

**Figure 3-29.** Bluetooth UART Header Schematic

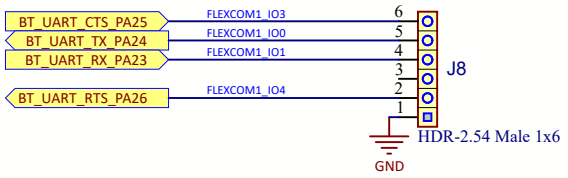
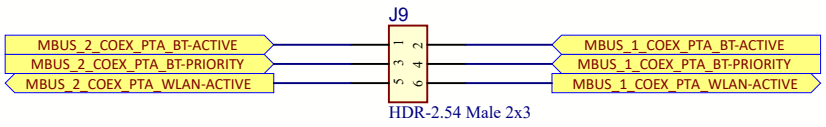



**Table 3-17.** Bluetooth UART Signal Description

| PIO | Signal Name | Signal Description |
|---|---|---|
| PA23 | BT_UART_RX_PA23 | Bluetooth UART host data receive line |
| PA24 | BT_UART_TX_PA24 | Bluetooth UART host data transmit line |
| PA25 | BT_UART_CTS_PA25 | Bluetooth UART host clear to send signal |
| PA26 | BT_UART_RTS_PA26 | Bluetooth UART host ready to send signal |

Because the SAMA5D29-Curiosity supports multiple radio modules, on SD and mikroBUS format, a PTA interface between the modules is provided. Featuring a set of 3-wired signals, the PTA connector (J9) organizes wireless packet traffic for communication protocols operating in the same frequency band without affecting the RF performance by intelligently sharing frequency band.

**Figure 3-30.** PTA Interface Connector



### 3.4.5.2 SDMMC0 Connector

A standard µSD card connector, connected to the SDMMC interface, is also mounted on the bottom side of the board. The SDMMC0 communication is based on an 8-pin interface (clock, command, four data and power lines). It includes a card detection switch. This connector gives access to the boot environment.

**Figure 3-31.** SDMMC0 Connector Schematic

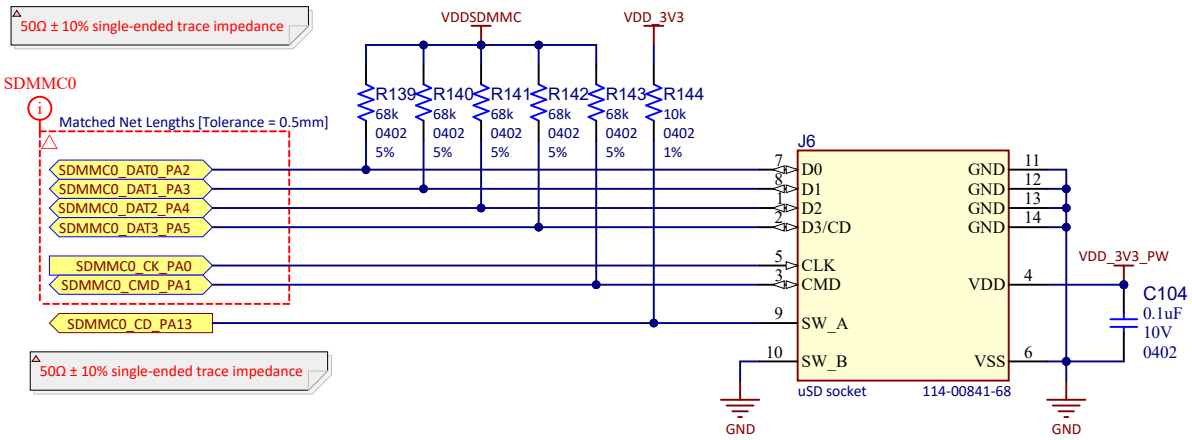


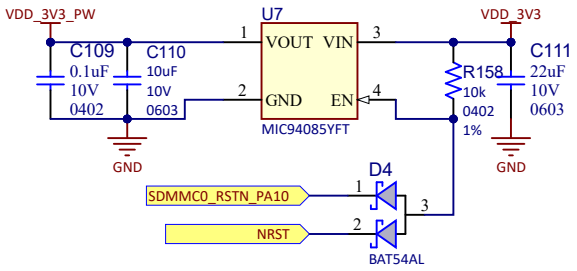

**Table 3-18.** SDMMC0 Connector Signal Description

| PIO | Signal Name | Signal Description |
|---|---|---|
| PA0 | SDMMC0_ CK_PA0 | SDMMC0 clock signal |
| PA1 | SDMMC0_CMD_PA1 | SDMMC0 command line |
| PA2 | SDMMC0_DAT0_PA2 | SDMMC0 data line 0 |
| PA3 | SDMMC0_DAT1_PA3 | SDMMC0 data line 1 |
| PA4 | SDMMC0_DAT2_PA4 | SDMMC0 data line 2 |
| PA5 | SDMMC0_DAT3_PA5 | SDMMC0 data line 3 |
| PA10 | SDMMC0_RSTN_PA10 | SDMMC0 reset line |
| PA11 | SDMMC0_1V8SEL_PA11 | SDMMC0 I/O voltage selection signal |
| PA13 | SDMMC0_CD_PA13 | SDMMC0 card detect signal |

The user can perform a hard reset of the µSD card by toggling PA10 PIO of the MPU, which corresponds to the reset line of the SDMMC0 interface. The same hard reset will be performed automatically at each system reset, when NRST is asserted low.

The hard reset is performed by power cycling the µSD card power using the MIC94085YFT high-side load switch. For more details about the MIC94085YFT device, refer to the product web site.

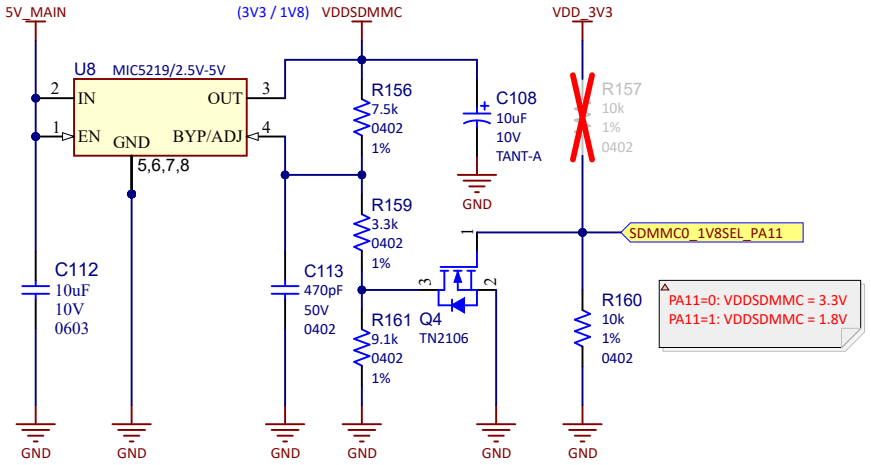
**Figure 3-32.** SDMMC0 Connector Power Switch Schematic



The SDMMC0 interface supports switching the I/O voltage level from 3.3 V to 1.8 V to enable high-speed modes for the µSD card. The SAMA5D29 MPU performs the switch by asserting the PA11 PIO on high when a card supporting high-speed modes is detected (depending on software support). The schematic below describes the circuit which generates the required 3.3/1.8V voltages using the adjustable LDO MIC5219.

For more details about the MIC5219 device, refer to the product web site.

**Figure 3-33.** SDMMC0 I/O Voltage Switch Schematic




## 3.4.6 Dual mikroBUS Click Interfaces

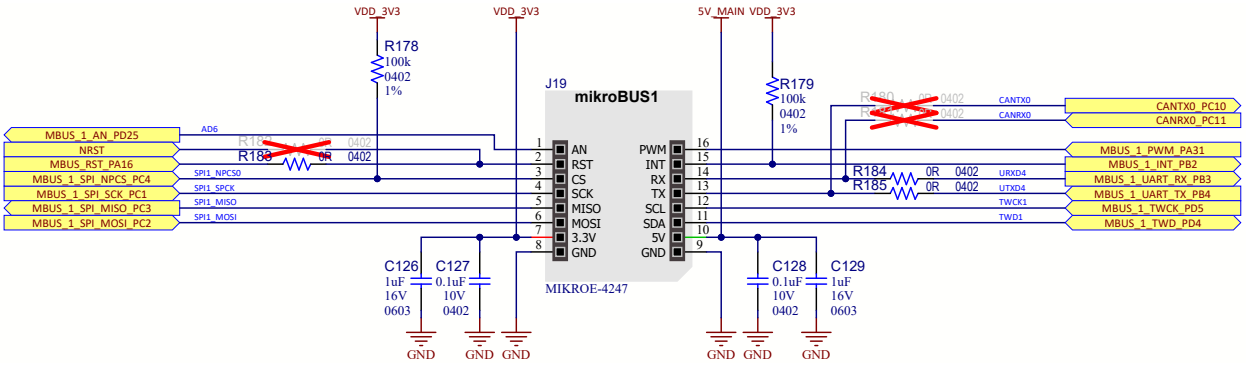
The SAMA5D29-Curiosity hosts two (J19 and J22) official mikroBUS sockets, implementing the mikroBUS standard. For details, refer to the mikroBUS documentation on www.mikroe.com/mikrobus.

In addition to the standard mikroBUS format, each socket features one 4-pin female header to implement the PTA feature for selected mikroBUS radio click boards.

### 3.4.6.1 mikroBUS 1 Connector

The first mikroBUS socket (J19) implements all mikroBUS features as described in the schematic below. The reset feature is ensured (by default) by the processor PA16 PIO and can be swapped to the general reset line by moving resistor R183 to R182.

**Figure 3-34.** mikroBUS 1 Interface




The first mikroBUS interface features an SPI bus shared with the second mikroBUS interface. Each interface has its own Chip Select line to its SPI interface (PC4 for the mikroBUS1 interface). I/Os in common are PC1, PC2 and PC3. That means that the SPI interface cannot be used at the same time on the two mikroBUS interfaces.

The first mikroBUS interface features a two-wire interface (PD4 and PD5) shared with the second mikroBUS interface and with the 40-pin RPi connector. The end user must pay attention to the I²C addresses used on these nodes.

The PWM feature of the first mikroBUS interface (PA31) is shared with the PWM0 signal on the 40-pin RPi connector and the 20-pin Multifunction header.

For evaluating the CAN-FD interface, the CAN0 RX/TX signals must be routed on the mikroBUS socket by moving resistors R184 to R181 and R185 to R180, and using selected mikroBUS click boards which have the CAN-FD transceivers implemented in place of the standard UART RX/TX signals. When evaluating CAN0, the LCD and ISC camera interface become unavailable.

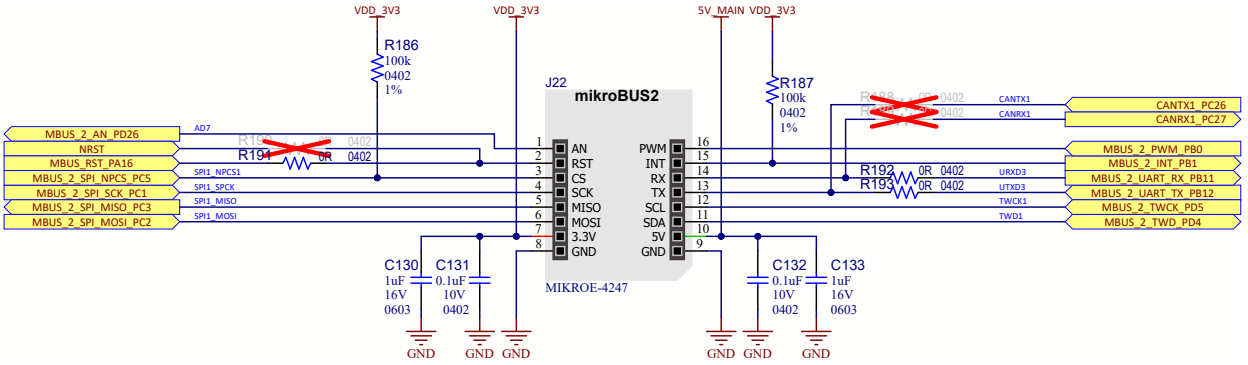
**Table 3-19.** mikroBUS 1 Connector J19 Pin Assignment

| Function | PIO | mBUS Signal | Pin No. | Pin No. | mBUS Signal | PIO | Function |
|---|---|---|---|---|---|---|---|
| Analog input | PD25 | AN | 1 | 16 | PWM | PA31 | PWM |
| Reset | PA16 | RST | 2 | 15 | INT | PB2 | Interrupt |
| SPI Chip Select | PC4 | SPI_NPCS | 3 | 14 | UART_RX | PB3 | UART receive (mBUS output to SAM) |
| SPI Clock | PC1 | SPI_SPCK | 4 | 13 | UART_TX | PB4 | UART transmit (mBUS input from SAM) |
| SPI MOSI | PC3 | SPI_MISO | 5 | 12 | TWI_SCL | PD5 | TWI clock |
| SPI MISO | PC2 | SPI_MOSI | 6 | 11 | TWI_SDA | PD4 | TWI data |
| VCC | – | 3.3V supply | 7 | 10 | 5V supply | – | VDD |
| Ground | – | GND | 8 | 9 | GND | – | Ground |

### 3.4.6.2 mikroBUS 2 Connector

The second mikroBUS socket (J22) implements all mikroBUS features as described in the schematic below. The reset feature is ensured (by default) by the processor PA16 PIO and can be swapped to the general reset line by moving resistor R191 to R190.

**Figure 3-35.** mikroBUS 2 Interface




The second mikroBUS interface features an SPI bus shared with the first mikroBUS interface. Each interface has its own Chip Select line to its SPI interface (PC5 for the mikroBUS2 interface). I/Os in common are PC1, PC2 and PC3. That means that the SPI interface cannot be used at the same time on the two mikroBUS interfaces.

The second mikroBUS interface features a two-wire interface (PD4 and PD5) shared with the second mikroBUS interface and with the 40-pin RPi connector. The end user must pay attention to the I²C addresses used on these nodes.

The PWM feature of the first mikroBUS interface (PB0) is shared with the PWM1 signal on the 40-pin RPi connector and the 20-pin Multifunction header.

For evaluating the CAN-FD interface, the CAN1 RX/TX signals must be routed on the mikroBUS socket by moving resistors R192 to R189 and R193 to R188, and using selected mikroBUS click boards which have the CAN-FD transceivers implemented in place of the standard UART RX/TX signals. When evaluating CAN1, the LCD and ISC camera interface become unavailable.

**Table 3-20.** mikroBUS 2 Connector J22 Pin Assignment

| Function | PIO | mBUS Signal | Pin No. | Pin No. | mBUS Signal | PIO | Function |
|---|---|---|---|---|---|---|---|
| Analog input | PD26 | AN | 1 | 16 | PWM | PB0 | PWM |
| Reset | PA16 | RST | 2 | 15 | INT | PB1 | Interrupt |
| SPI Chip Select | PC5 | SPI_NPCS | 3 | 14 | UART_RX | PB11 | UART receive (mBUS output to SAM) |
| SPI Clock | PC1 | SPI_SPCK | 4 | 13 | UART_TX | PB12 | UART transmit (mBUS input from SAM) |
| SPI MOSI | PC3 | SPI_MISO | 5 | 12 | TWI_SCL | PD5 | TWI clock |
| SPI MISO | PC2 | SPI_MOSI | 6 | 11 | TWI_SDA | PD4 | TWI data |
| VCC | – | 3.3V supply | 7 | 10 | 5V supply | – | VDD |
| Ground | – | GND | 8 | 9 | GND | – | Ground |

### 3.4.7 RPi 40-pin GPIO Interface

The SAMA5D29-Curiosity board features a 40-pin connector (RPi-compatible) for free use.

By default, pin 7 of the connector is connected to the SAMA5D29 Audio clock PLL output to provide a high-quality clock for audio applications. To change to the MPU PIO PD20, move resistor R195 to R194.

**Figure 3-36.** 40-pin GPIO Connector Schematic

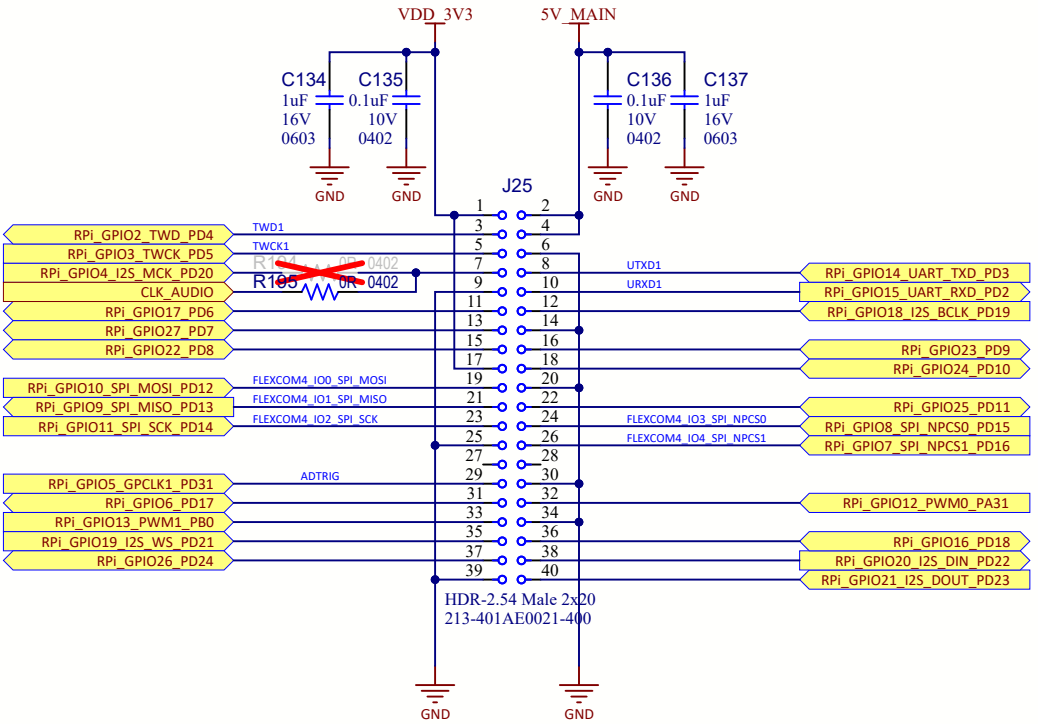


**Table 3-21.** 40-pin GPIO Pin Assignment

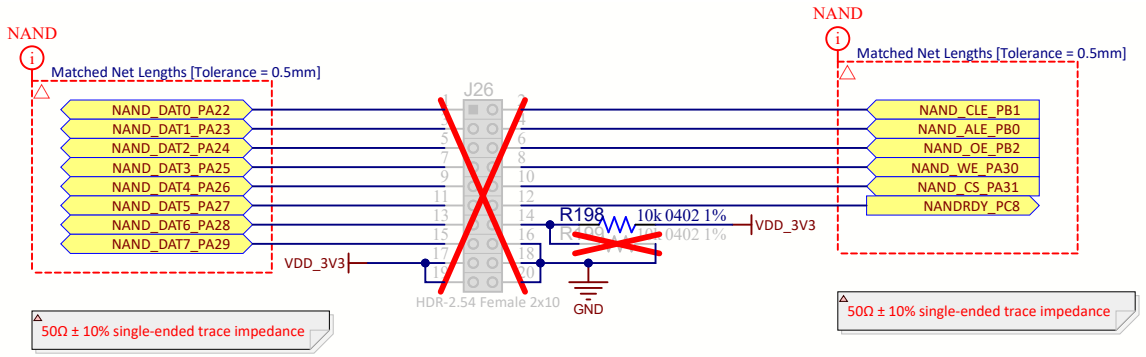
| Signal | Pin No | Pin No | Signal |
|---|---|---|---|
| VDD_3V3 | 1 | 2 | 5V_MAIN |
| RPi_GPIO2_TWD_PD4 | 3 | 4 | 5V_MAIN |
| RPi_GPIO3_TWCK_PD5 | 5 | 6 | GND |
| RPi_GPIO4_I2S_MCK_PD20 | 7 | 8 | RPi_GPIO14_UART_TXD_PD3 |
| GND | 9 | 10 | RPi_GPIO15_UART_RXD_PD2 |
| RPi_GPIO17_PD6 | 11 | 12 | RPi_GPIO18_I2S_BCLK_PD19 |
| RPi_GPIO27_PD7 | 13 | 14 | GND |
| RPi_GPIO22_PD8 | 15 | 16 | RPi_GPIO23_PD9 |
| VDD_3V3 | 17 | 18 | RPi_GPIO24_PD10 |
| RPi_GPIO10_SPI_MOSI_PD12 | 19 | 20 | GND |
| RPi_GPIO9_SPI_MISO_PD13 | 21 | 22 | RPi_GPIO25_PD11 |
| RPi_GPIO11_SPI_SCK_PD14 | 23 | 24 | RPi_GPIO8_SPI_NPCS0_PD15 |
| GND | 25 | 26 | RPi_GPIO7_SPI_NPCS1_PD16 |
| - | 27 | 28 | – |
| RPi_GPIO5_GPCLK1_PD31 | 29 | 30 | GND |
| RPi_GPIO6_PD17 | 31 | 32 | RPi_GPIO12_PWM0_PA31 |
| RPi_GPIO13_PWM1_PB0 | 33 | 34 | GND |
| RPi_GPIO19_I2S_WS_PD21 | 35 | 36 | RPi_GPIO16_PD18 |
| RPi_GPIO26_PD24 | 37 | 38 | RPi_GPIO20_I2S_DIN_PD22 |
| GND | 39 | 40 | RPi_GPIO21_I2S_DOUT_PD23 |

### 3.4.8 Multifunction 20-Pin Connector

The 20-pin multifunction connector providea connectivity to alternate functions of certain MPU PIOs. One such function is the NAND Flash interface, fully exposed on this connector. In order to evaluate the NAND Flash interface, inexpensive PCB adapters can be designed to match the provided connector pinout. Other functions are also exposed by the 20-pin connector:

- FLEXCOM1
- QSPI0
- CLASS D Left channel

**Figure 3-37.** Multifunction 20-Pin Connector Schematic



By default, the connector is not mounted. It requires user intervention to have connectivity with the MPU by moving some resistors. Refer to GPIO Distribution for details.

If connectivity is ensured so that the NAND Flash function is used, the following interfaces, or part of them, become unavailable:

- SDMMC1 connector
- Bluetooth UART header
- GPIO1 and GPIO2 of 10/100 RMII slot
- mikroBUS 1 PWM and RPi PWM0 signals
- mikroBUS 2 PWM and RPi PWM1 signals
- mikroBUS 1 and 2 interrupt signals

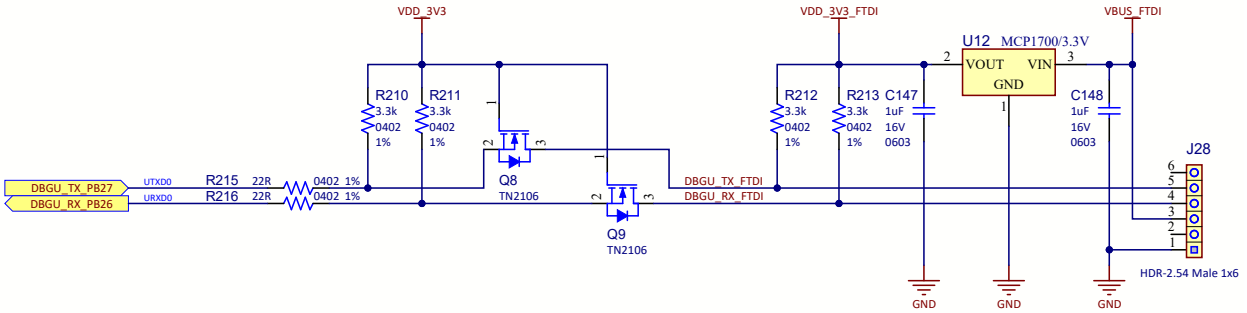
### 3.4.9 Debug Interface

The SAMA5D29-Curiosity includes two interfaces for debugging purposes.

#### 3.4.9.1 Serial Debug Com Port (FTDI)

The SAMA5D29-Curiosity board features a dedicated serial port for debugging, accessible through header J28. Various interfaces can be used as a USB/Serial DBGU port bridge, such as the FTDI TTL-232R USB-to-TTL serial cable.

**Figure 3-38.** Serial Debug Port Schematic




**Only Compatible with :**
**- TTL-232R-3V3**
**- TTL-232R-5V**

The DBGU serial port uses the MCP1700/3.3V LDO to prevent any voltage higher than 3.3V to be applied on any 3.3V-only tolerant external USB-to-UART converter. For more details about the MCP1700/3.3V device, refer to the product web page.

An inexpensive level shifter solution is also implemented using two TN2106 N-channel MOSFETs.

For more details about the TN2106 device, refer to the product web page.

**Table 3-22.** Serial Debug Port Signal Description

| PIO | Signal Name | Signal Description |
|---|---|---|
| PB26 | DBGU_RX_PB26 | UART receive data line |
| PB27 | DBGU_TX_PB27 | UART transmit data line |

#### 3.4.9.2 Debug JTAG

A 20-pin JTAG header (J27) is provided on the SAMA5D29-Curiosity board to facilitate software development and debugging using various JTAG emulators. The interface signals have a voltage level of 3.3V.

**Figure 3-39.** JTAG Connector Schematic

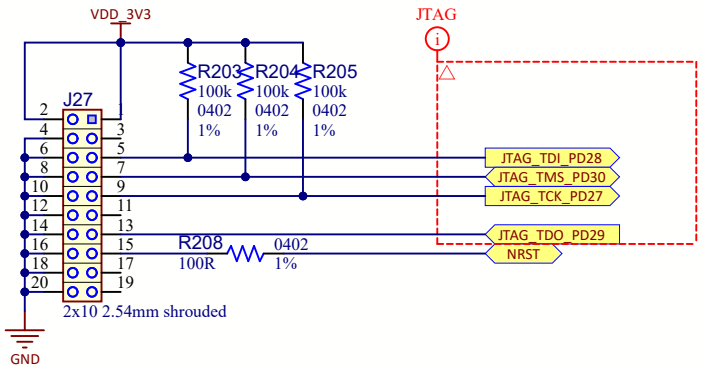



**Table 3-23.** JTAG Connector Pin Assignment

| Signal | Pin No | Pin No | Signal |
|---|---|---|---|
| VDD_3V3 | 2 | 1 | VDD_3V3 |
| GND | 4 | 3 | NC |
| GND | 6 | 5 | TDI |
| GND | 8 | 7 | TMS |
| GND | 10 | 9 | TCK |
| GND | 12 | 11 | NC |
| GND | 14 | 13 | TDO |
| GND | 16 | 15 | NRST |
| GND | 18 | 17 | NC |
| GND | 20 | 19 | NC |

## 3.4.10 User Interface

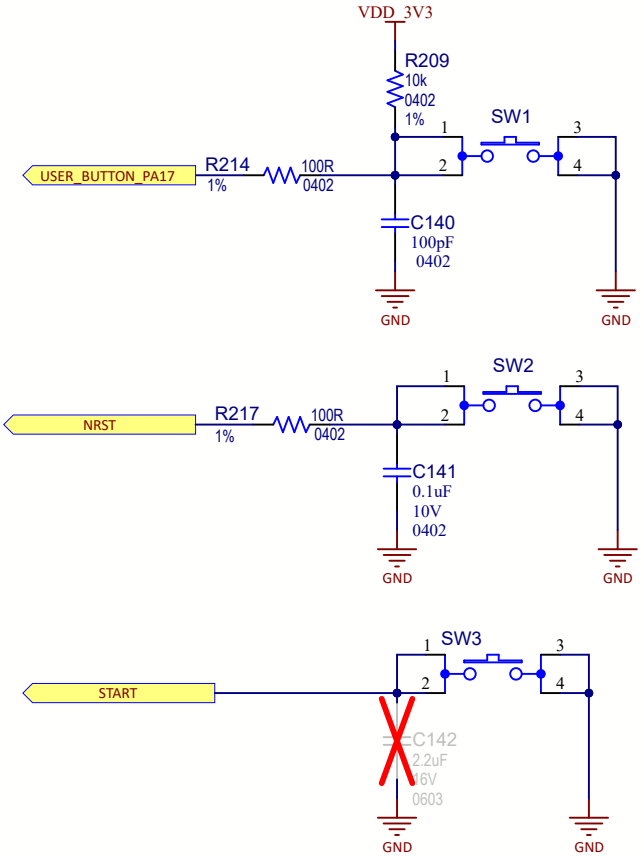
SAMA5D29-Curiosity includes several user interaction features, such as buttons and LEDs.

### 3.4.10.1 Push Button Switches

The SAMA5D29-Curiosity features three push buttons:

- One User push button (SW1) connected to PIO PA17. This is for user usage.
- One Board Reset push button (SW2). When pressed, the processor is reset.
- One Start push button (SW3) connected to the MCP16502 pin. When pressed, the PMIC start-up sequence is initiated if the Buck converters are off. Pressing the Start button will also assert the WKUP signal to wake up the MPU from a low-power state.

**Figure 3-40.** Push Buttons Schematic




The user can mount capacitor C142 to allow the board to automatically power-on when external power is applied.

### 3.4.10.2 RGB LED

The SAMA5D29-Curiosity board features one common anode RGB LED. The three LED cathodes are controlled via GPIO pins.

**Figure 3-41.** User LEDs

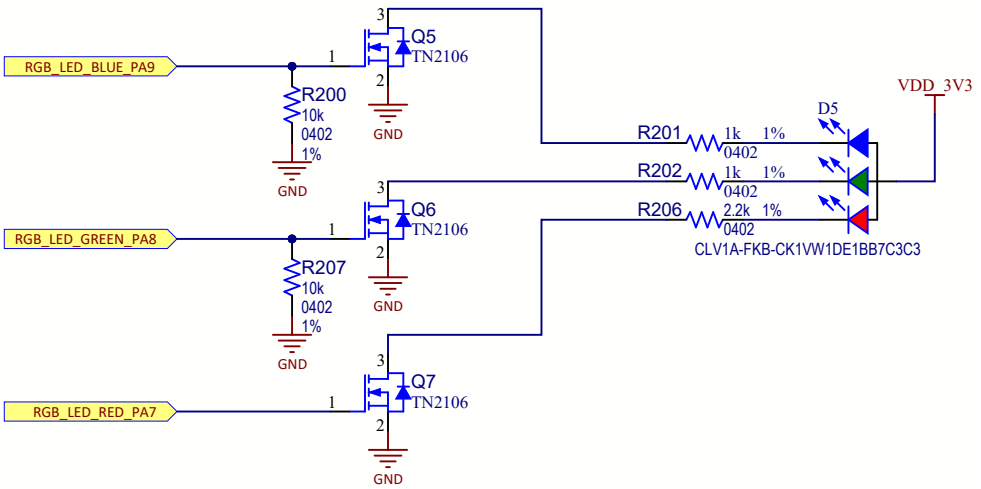


**Table 3-24.** RGB LED Signal Description

| PIO | Signal Name | Signal Description |
|---|---|---|
| PA7 | RGB_LED_RED_PA7 | Red LED |
| PA8 | RGB_LED_GREEN_PA8 | Green LED |
| PA9 | RGB_LED_BLUE_PA9 | Blue LED |

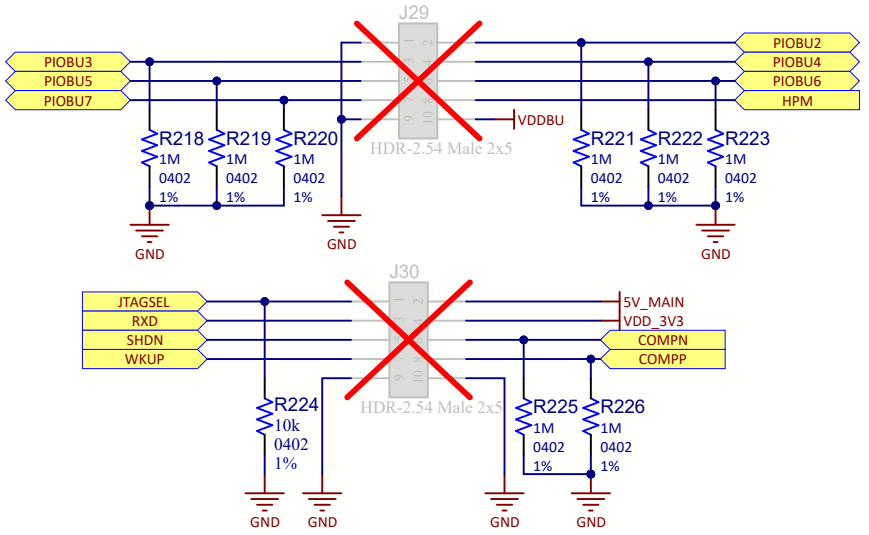
### 3.4.11 Tamper and System Signals Connectors

Unused signals and PIOs provided by the MPU are routed on separate connectors, J29 and J30 (not mounted). System signals are also accessible externally on these connectors.

The SAMA5D29-Curiosity board provides six tamper pins for static or dynamic intrusion detections on header J29. The HPM signal, used to enable the PMIC High-Power mode, is also present on the same connector.

Unused and available system signals are available on header J30.

**Figure 3-42.** Tamper and System Signals Connectors Schematic




The table below provides a signal description of header J29.

**Table 3-25.** J29 Signal Description

| Signal Name | Signal Description |
|---|---|
| PIOBU2 | Tamper I/O 2 |
| PIOBU3 | Tamper I/O 3 |
| PIOBU4 | Tamper I/O 4 |
| PIOBU5 | Tamper I/O 5 |
| PIOBU6 | Tamper I/O 6 |
| PIOBU7 | Tamper I/O 7 |
| HPM | PMIC High-Power Mode enable |

**Table 3-26.** J30 Signal Description

| Signal Name | Signal Description |
|---|---|
| JTAGSEL | JTAG boundary scan mode enable |

| .....continued | |
|---|---|
| **Signal Name** | **Signal Description** |
| RXD | Low-Power Asynchronous Receiver |
| SHDN | Enable/disable external power supply circuit |
| WKUP | Event detection input used to wake up the processor from Shutdown state |
| COMPN | Analog comparator inverting input |
| COMPP | Analog comparator non-inverting input |

# 4. Installation and Operation

## 4.1 System and Configuration Requirements

The SAMA5D29-Curiosity requires the following:

- A personal computer
- USB cable (provided in the kit box)
- One USB-UART converter (FTDI TTL-232R-3V3 or compatible)

## 4.2 Board Setup

Follow these steps before using the SAMA5D29-Curiosity:

1. Unpack the board, taking care to avoid electrostatic discharge.
2. Check the default jumper settings (see 2.5. Default Jumper Settings).
3. Connect the USB Type-C cable to connector J1 (USB-A port).
4. Connect the other end of the cable to a free port on your PC.
5. Connect a USB-UART converter to J28, making sure to also connect the VBUS_FTDI power source.
6. Open a terminal (console 115200, N, 8, 1) on your PC for the USB-UART converter.
7. Reset the board. The startup message “RomBOOT” appears on the console.

## 4.3 Board Operation Hints and Tips

- Only use the USB cable included in the kit box, or an equivalent one for powering the SAMA5D29-Curiosity board.
- When powering the board for the first time, the board will start automatically without the need to press the START button. This happens every time the backup supply supercapacitor depletes. Repowering the board afterwards will require pressing the START button to initialize the power-up sequence.
- Make sure the board is not powered when plugging and unplugging daughter boards (on mikroBUS, 10/100 RMII slot, RPi connector), cameras and displays. An exception to this rule can be made for add-on boards being plugged in the SD/µSD card connectors J7/J6 and the USB connectors.

# 5. Ordering Information

| Ordering Code | Board Marking |
|---|---|
| EV07R15A | SAMA5D29-Curiosity |

# 6. Errata

## 6.1 Large 10/100 RMII daughter boards and ISC connector limitation

If the user evaluates one of the Ethernet switch daughter boards (LAN9303 or KSZ8863), which are larger than the regular Ethernet PHY board, the inner side of the daughter board overlaps the optional ISC connector.

**Workaround**

Avoid evaluating large Ethernet daughter boards and the ISC connector at the same time.

A simple adapter can be made by pairing one female and one male 2x15 right-angled header to offset the ISC connector further away from the Ethernet board.

# 7. Appendix. Schematics and Layouts

## 7.1 SAMA5D29-Curiosity Schematics

This section contains the following schematics for the SAMA5D29-Curiosity board:

- Block Diagram Schematic
- Power Inputs Schematic
- Power Management Schematic
- MPU Clocks Power System Ports Schematic
- System Memory Schematic
- PIO Assignment Schematic
- PIO Distribution Schematic
- SD Card, QSPI Memory Schematic
- USB, Ethernet Schematic
- mikroBUS Schematic
- LCD, ISC, RPi, Multifunction Connectors Schematic
- User Debug and Interface Schematic
- Tamper, System Connectors, Accessories Schematic

**Figure 7-1.** Block Diagram Schematic

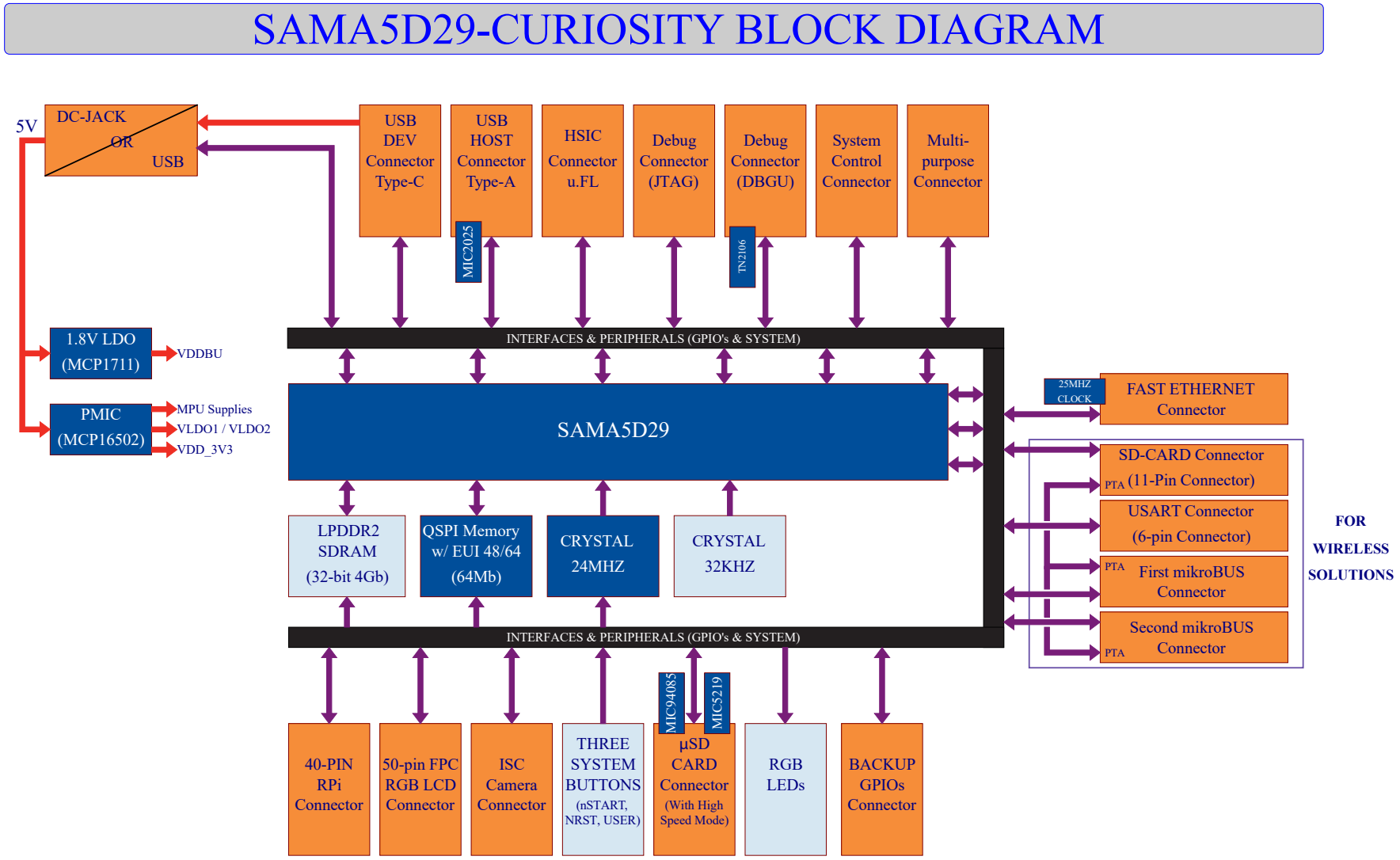


**Figure 7-2.** Power Inputs Schematic

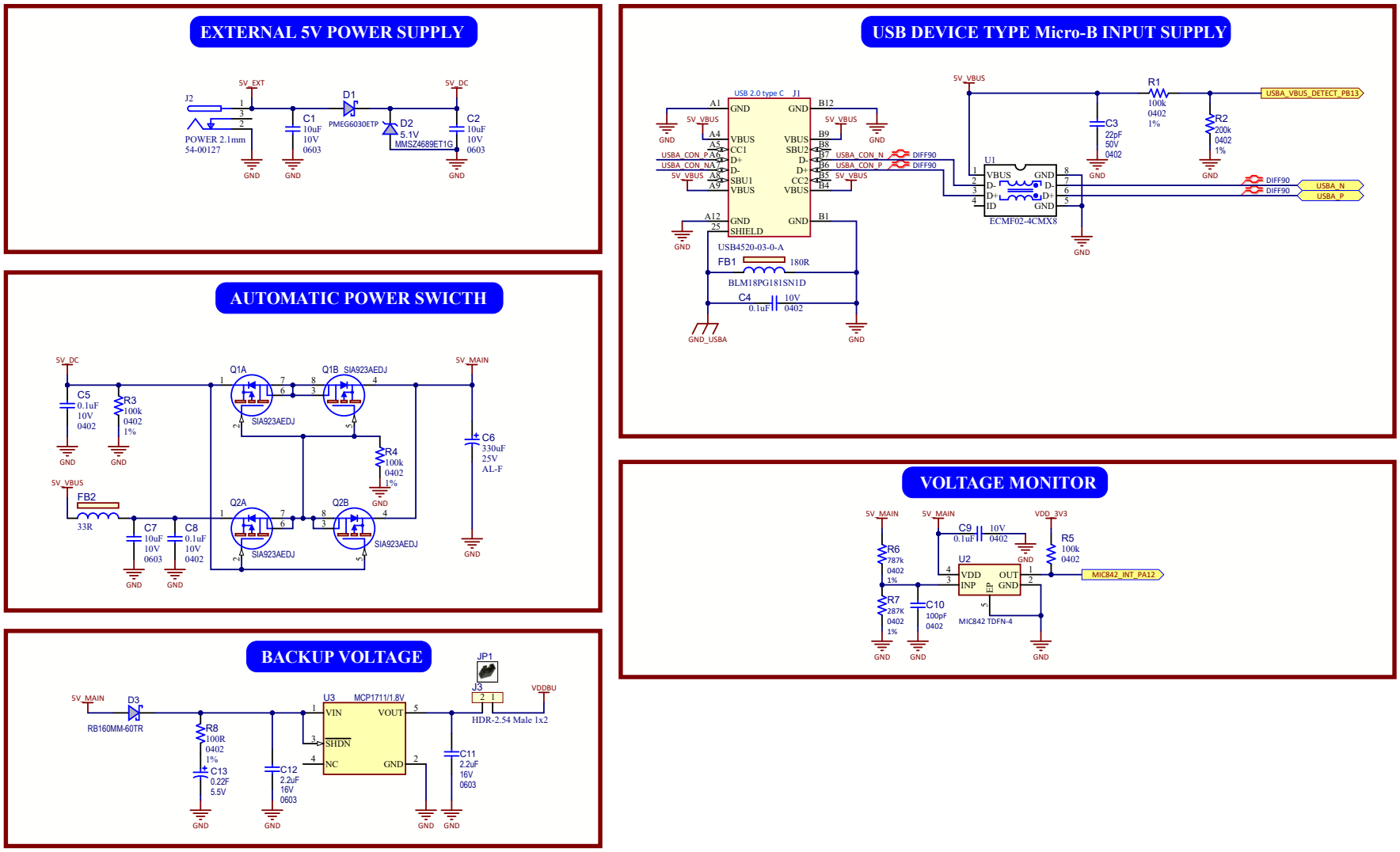


**Figure 7-3.** Power Management Schematic

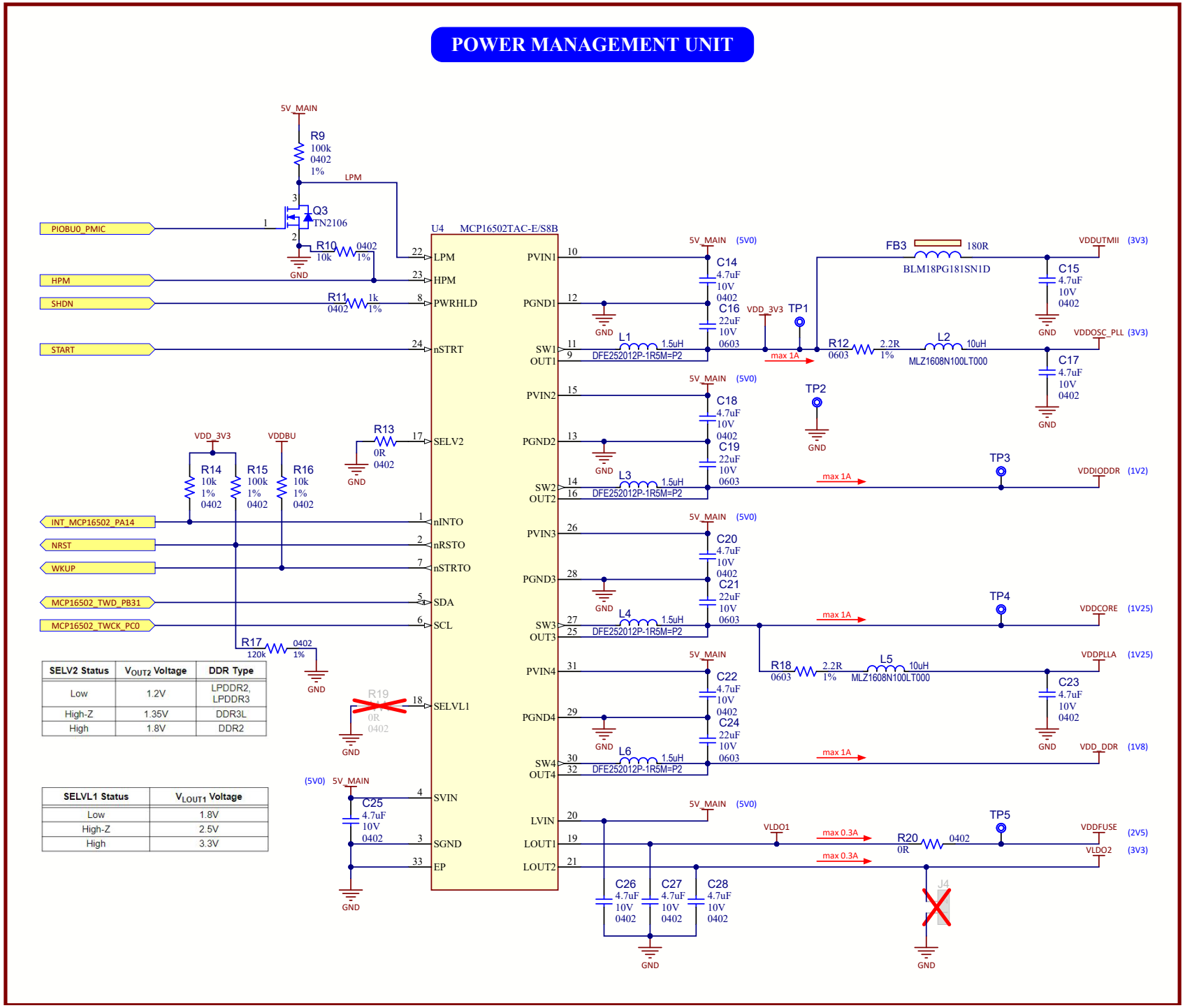
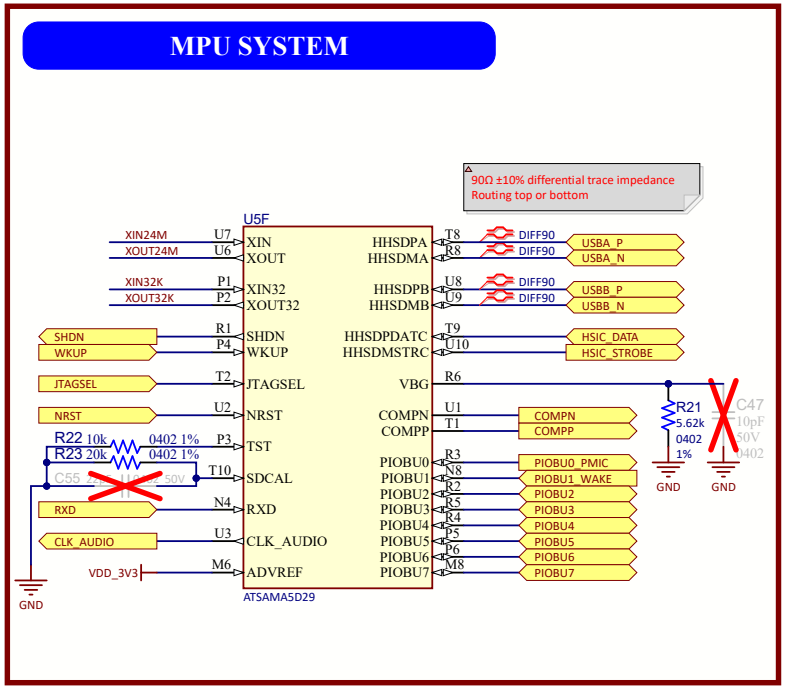
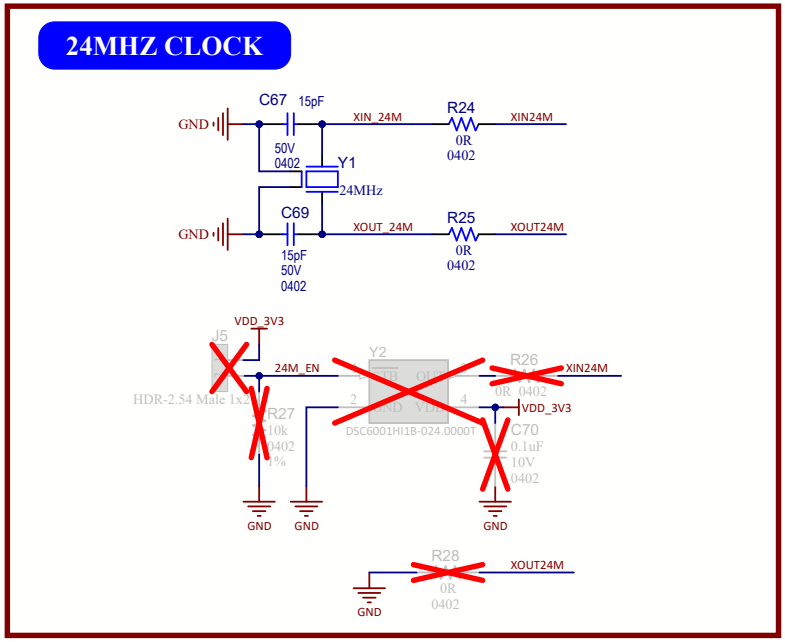
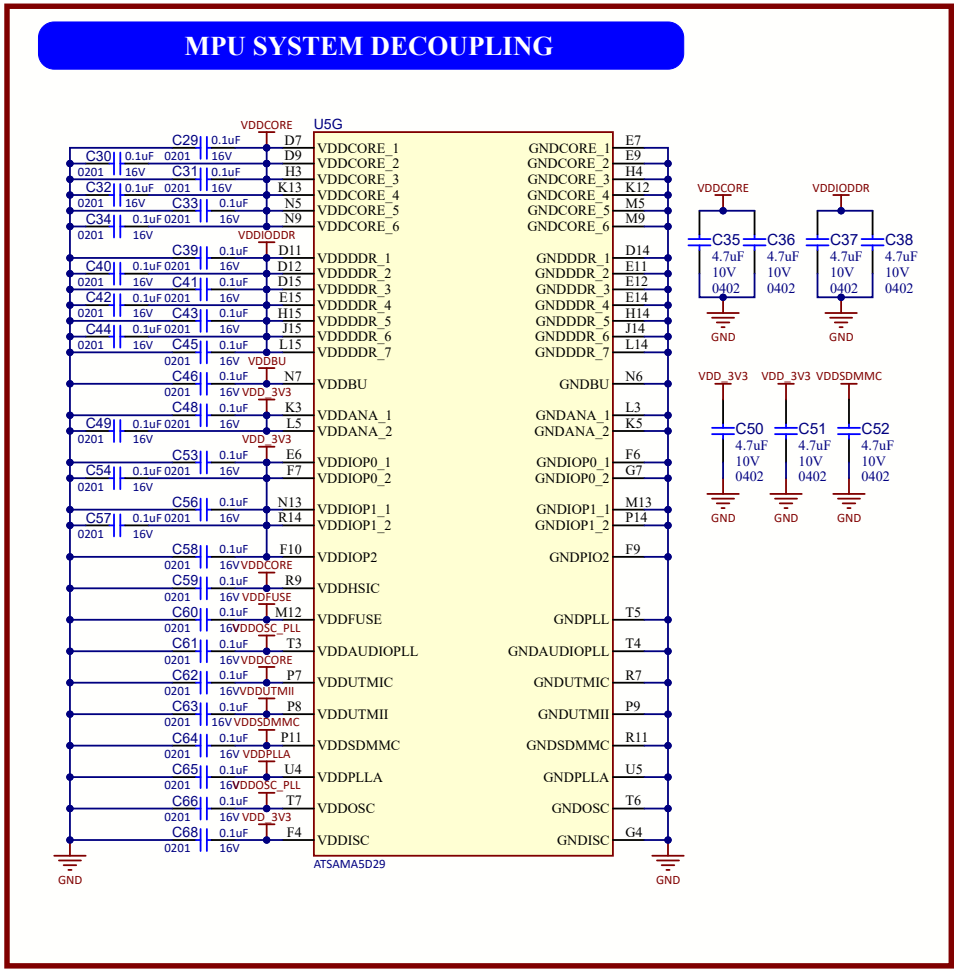


**Figure 7-4.** MPU Clocks, Power, System Ports Schematic



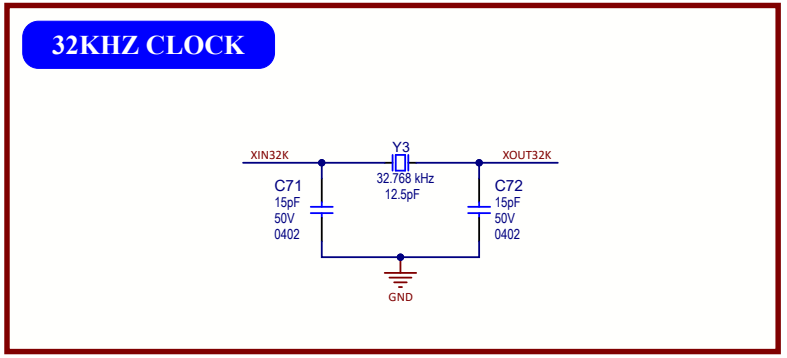



**Figure 7-5.** System Memory Schematic

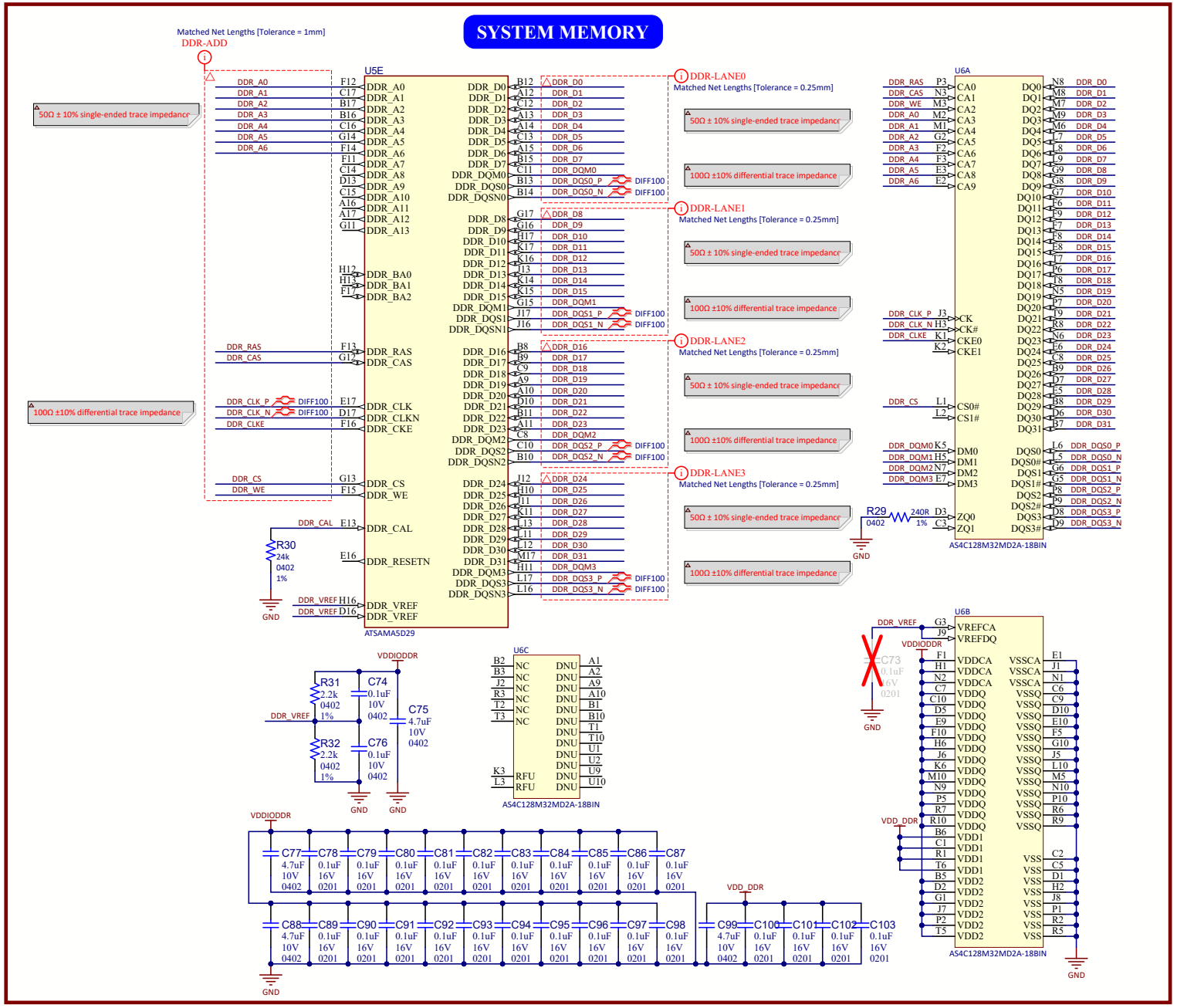


**Figure 7-6.** PIO Assignment Schematic

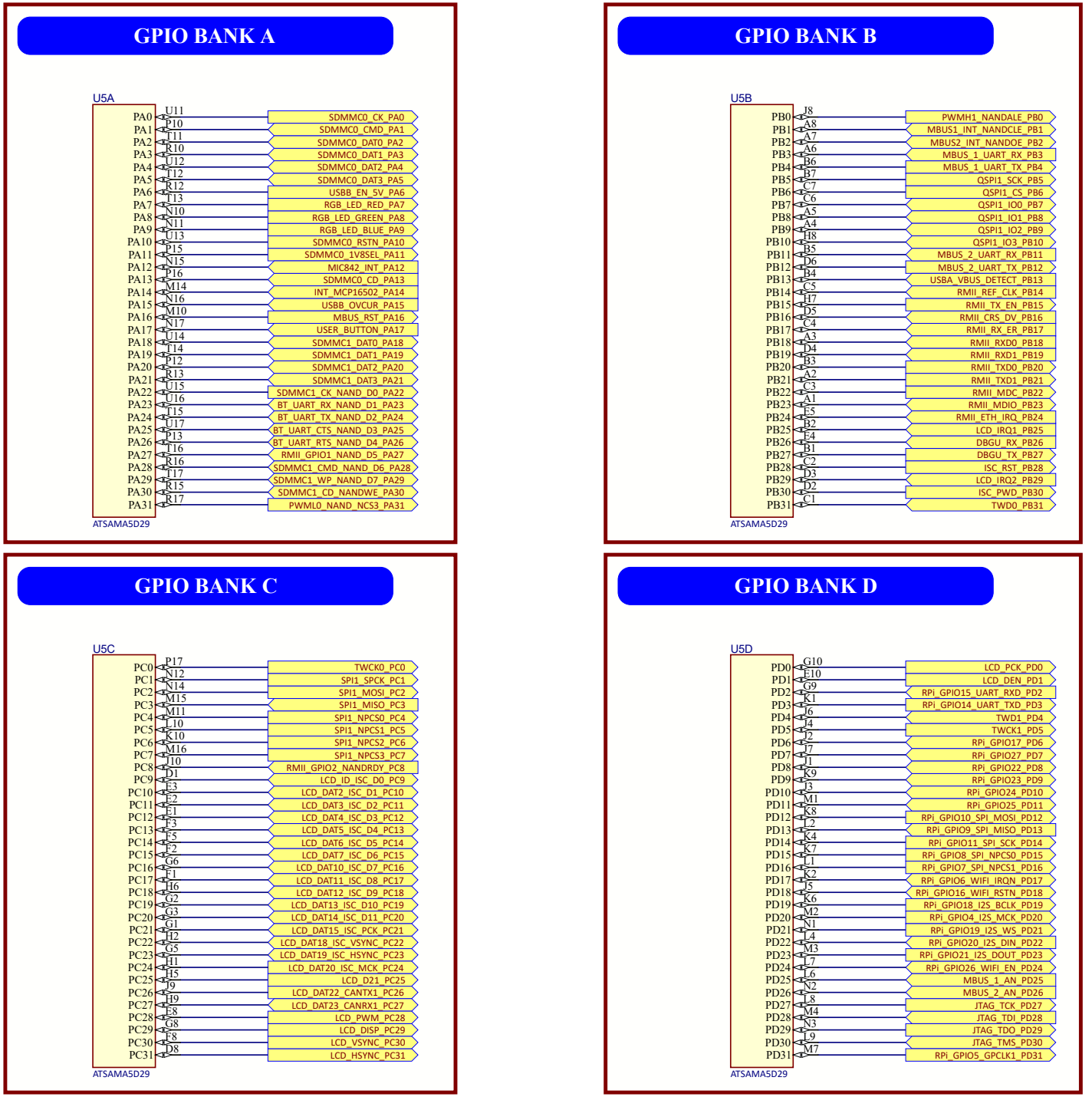


**Figure 7-7.** PIO Distribution Schematic

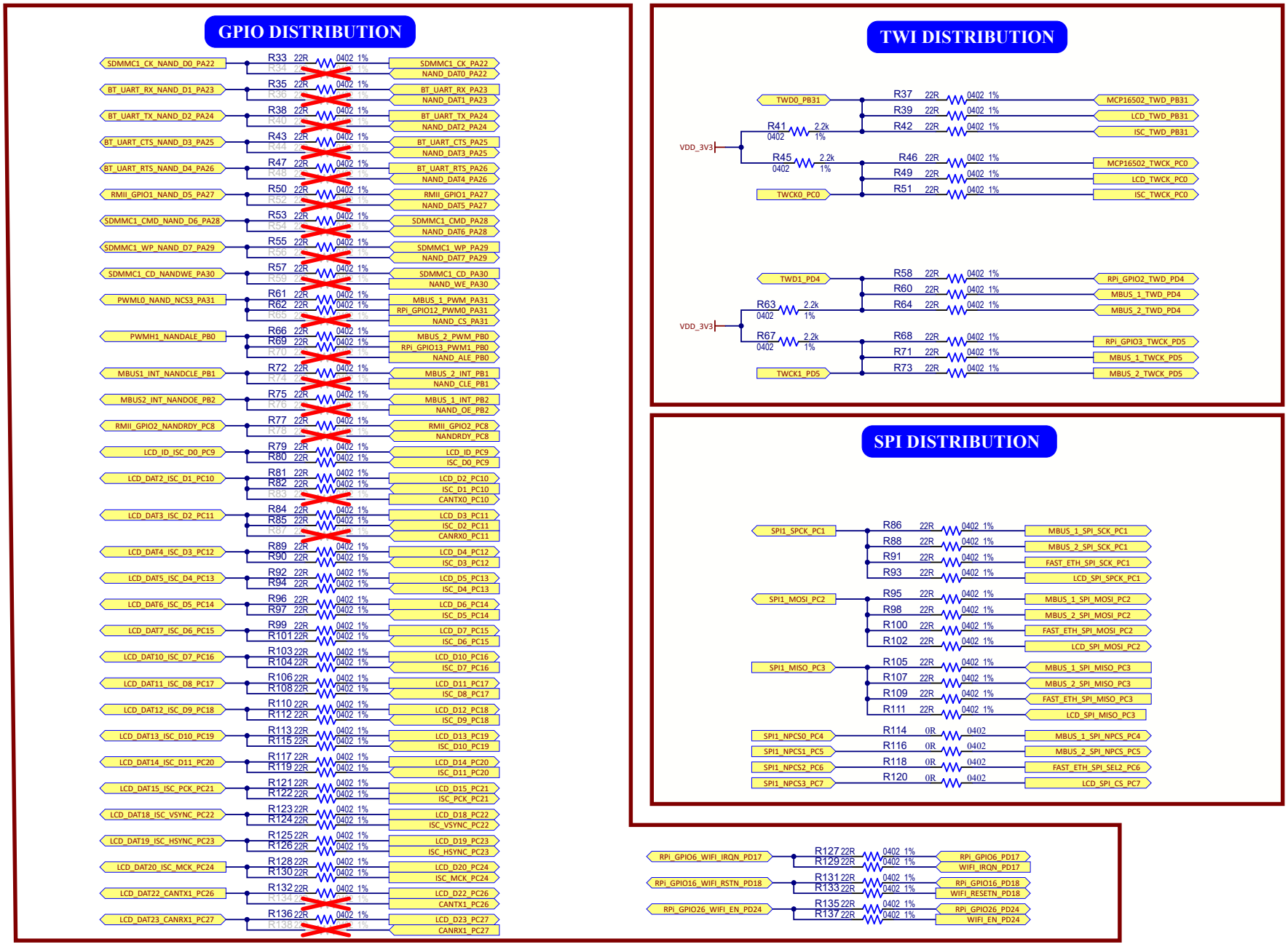


**Figure 7-8.** SD Card, QSPI Memory Schematic

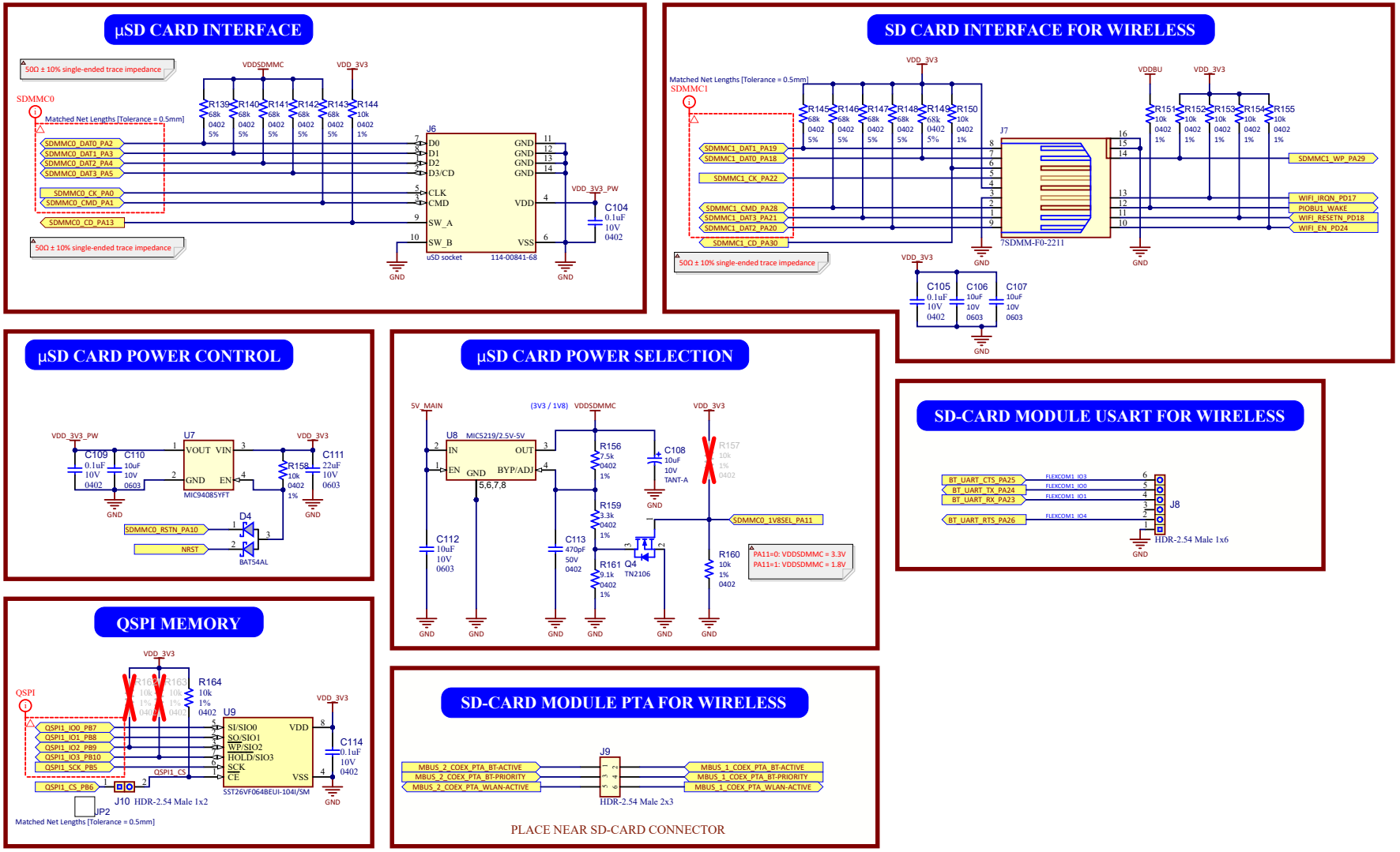


**Figure 7-9.** USB, Ethernet Schematic

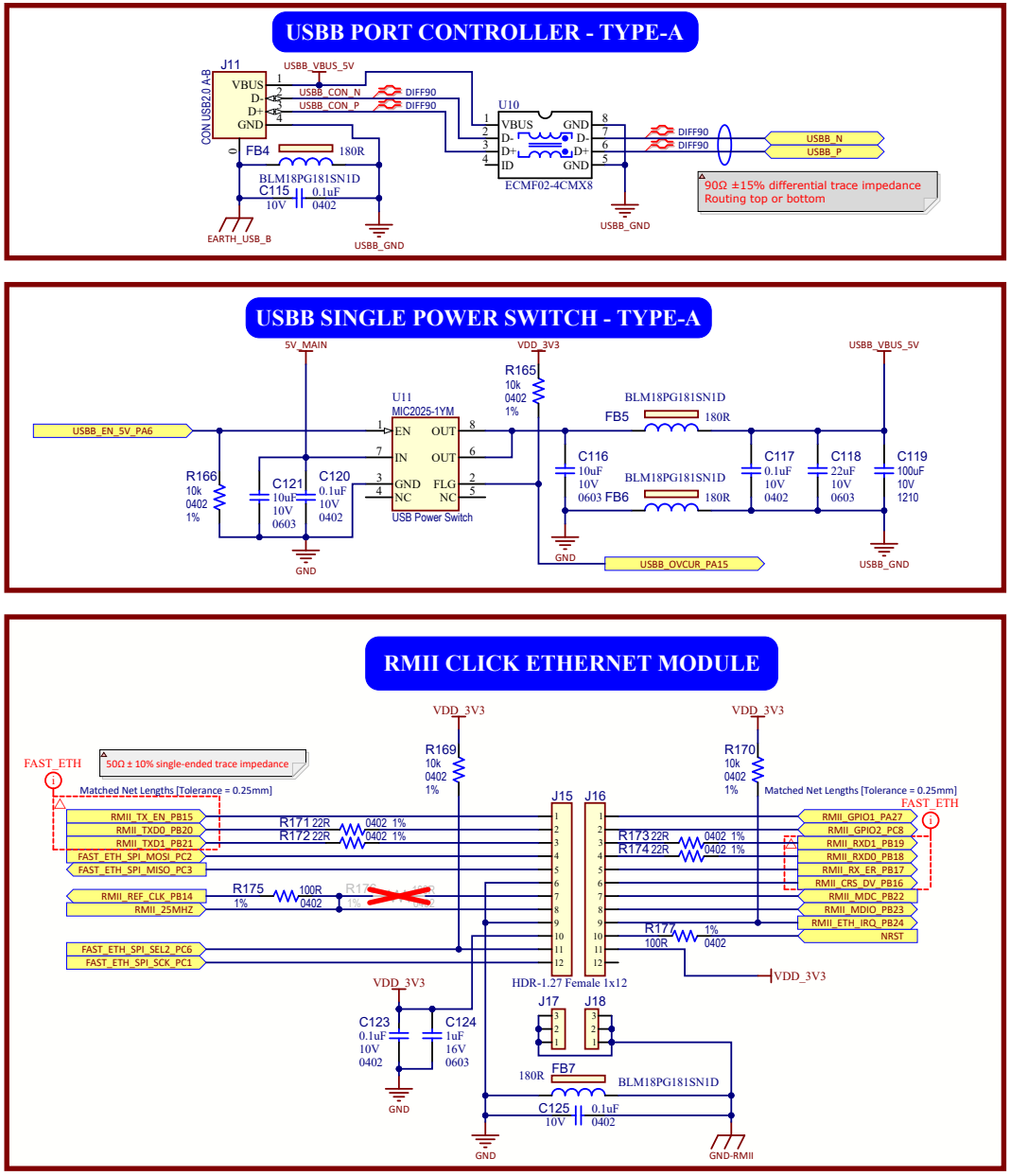


**Figure 7-10.** mikroBUS Schematic

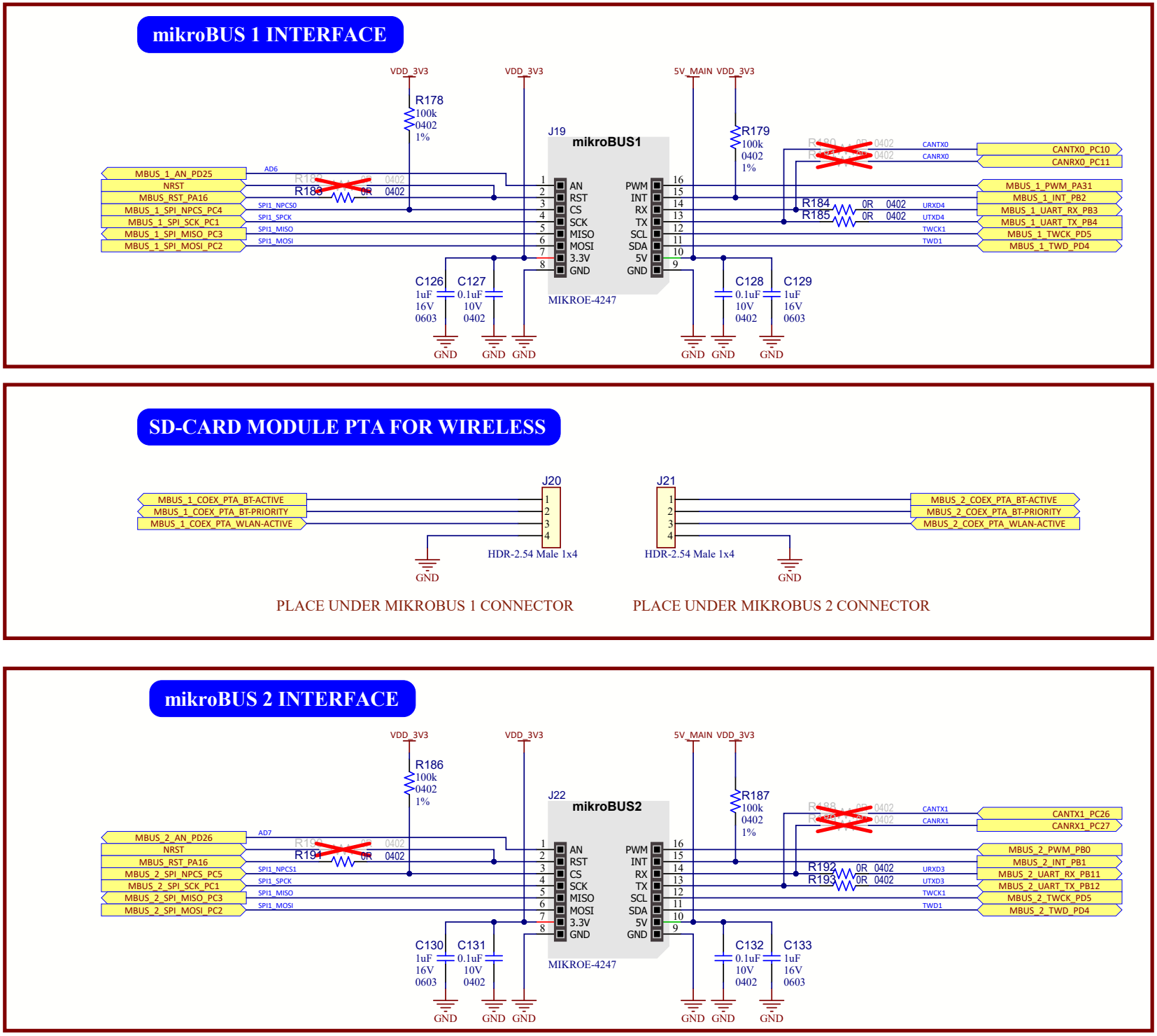


**Figure 7-11.** LCD, ISC, RPi, Multifunction Connectors Schematic

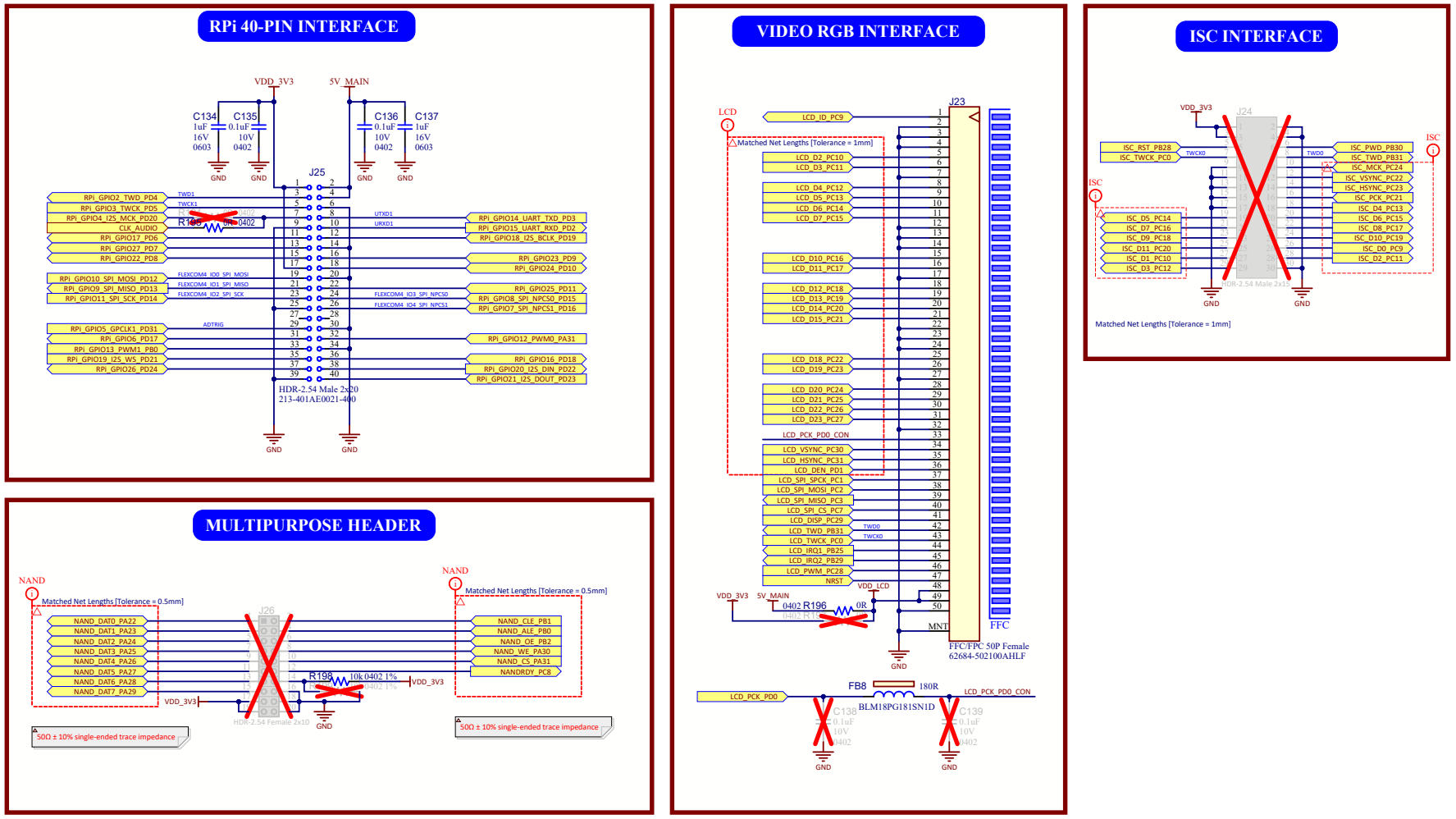


**Figure 7-12.** User Debug and Interface Schematic

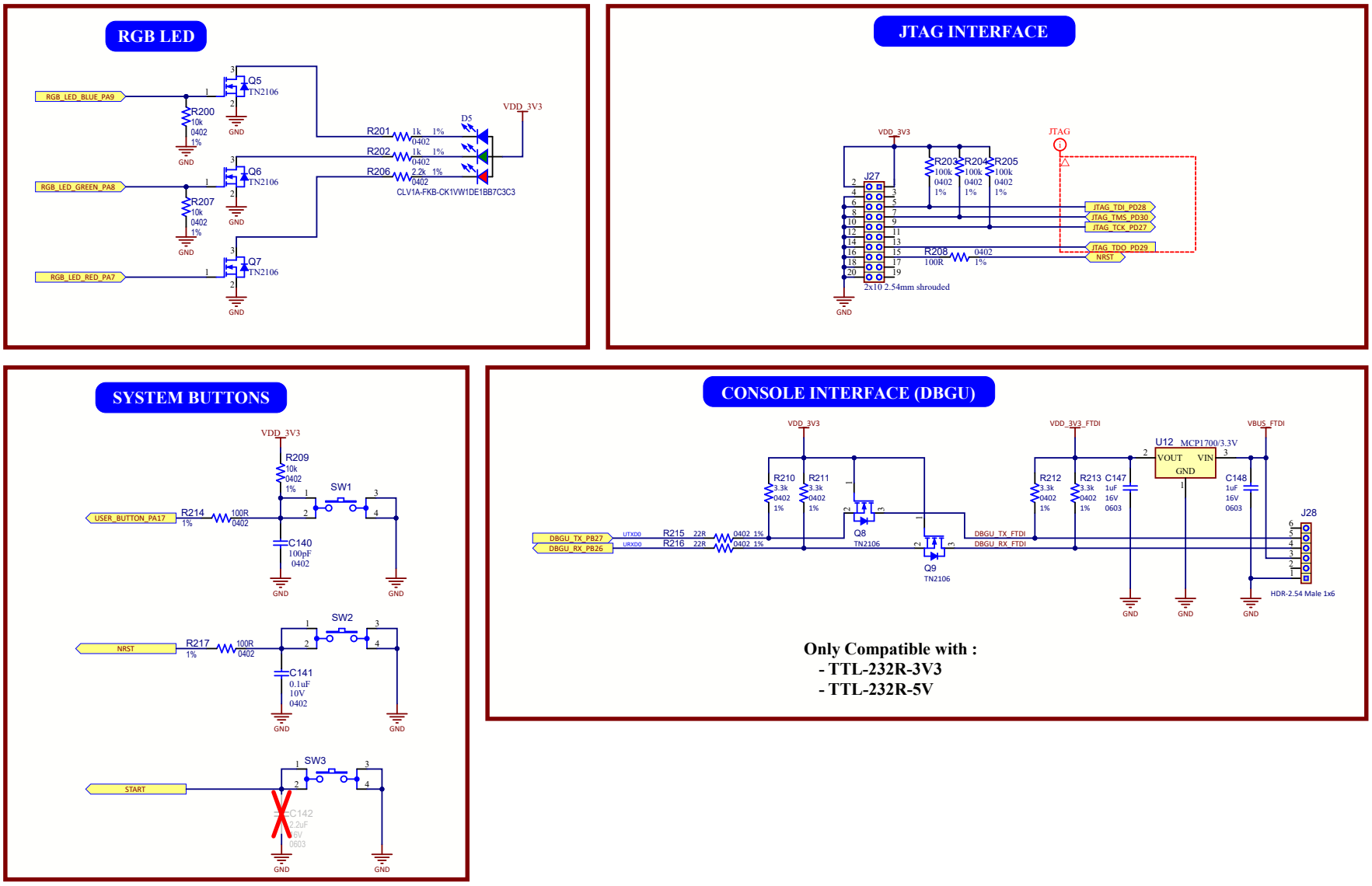
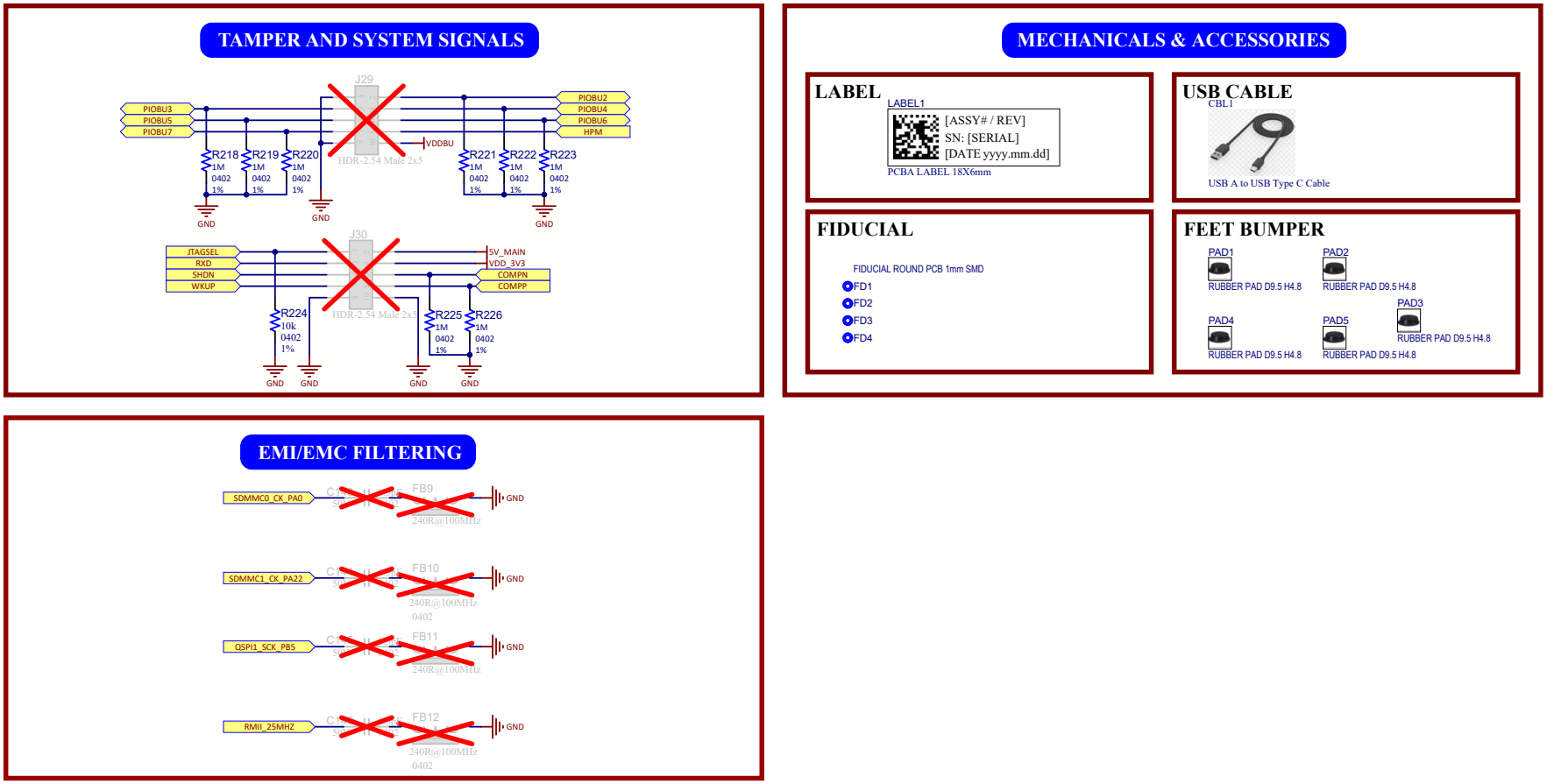


**Figure 7-13.** Tamper, System Connectors, Accessories Schematic



## 7.2 SAMA5D29-Curiosity Layout

This section contains the layout graphics for the SAMA5D29-Curiosity board:

- Layer 1: Top Layer
- Layer 2: Mid Layer 1
- Layer 3: Mid Layer 2
- Layer 4: Mid Layer 3
- Layer 5: Mid Layer 4
- Layer 6: Bottom Layer
- Top Components Placement
- Bottom Components Placement

**Figure 7-14.** SAMA5D29-Curiosity Layout: Top Layer

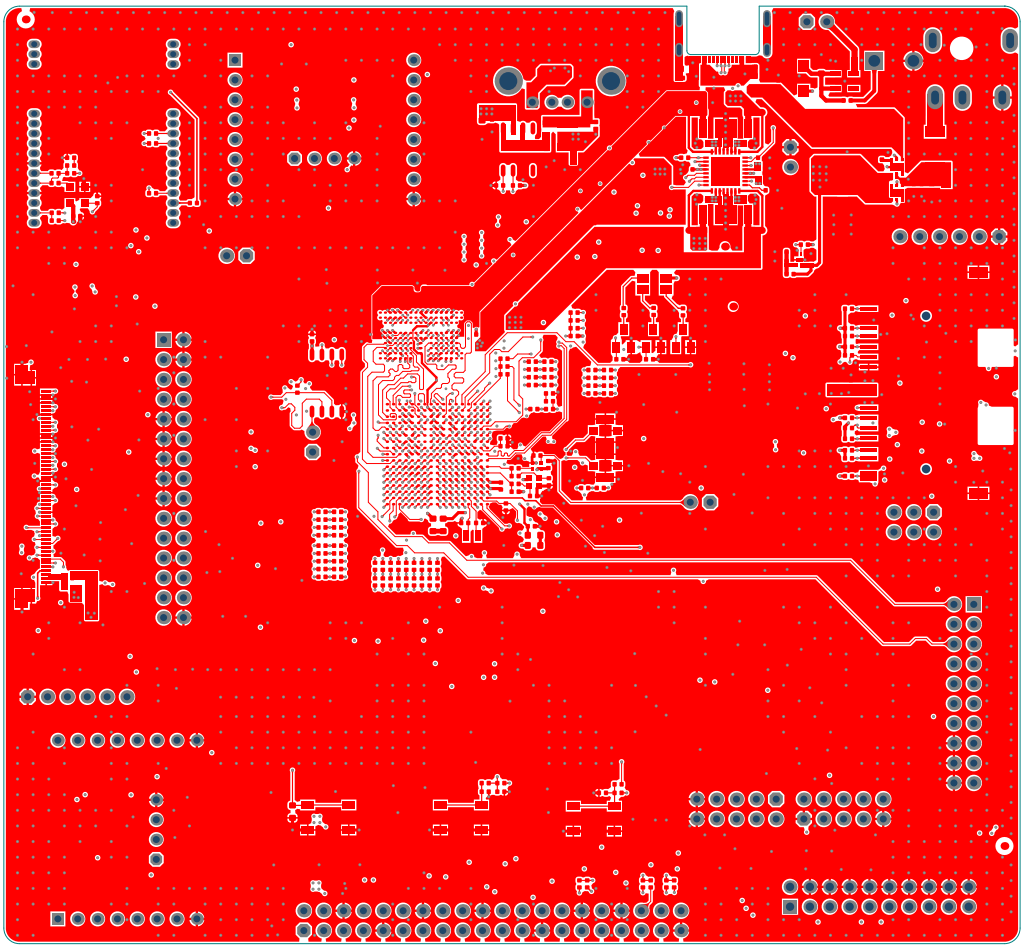


**Figure 7-15.** SAMA5D29-Curiosity Layout: Mid Layer 1 (Ground)

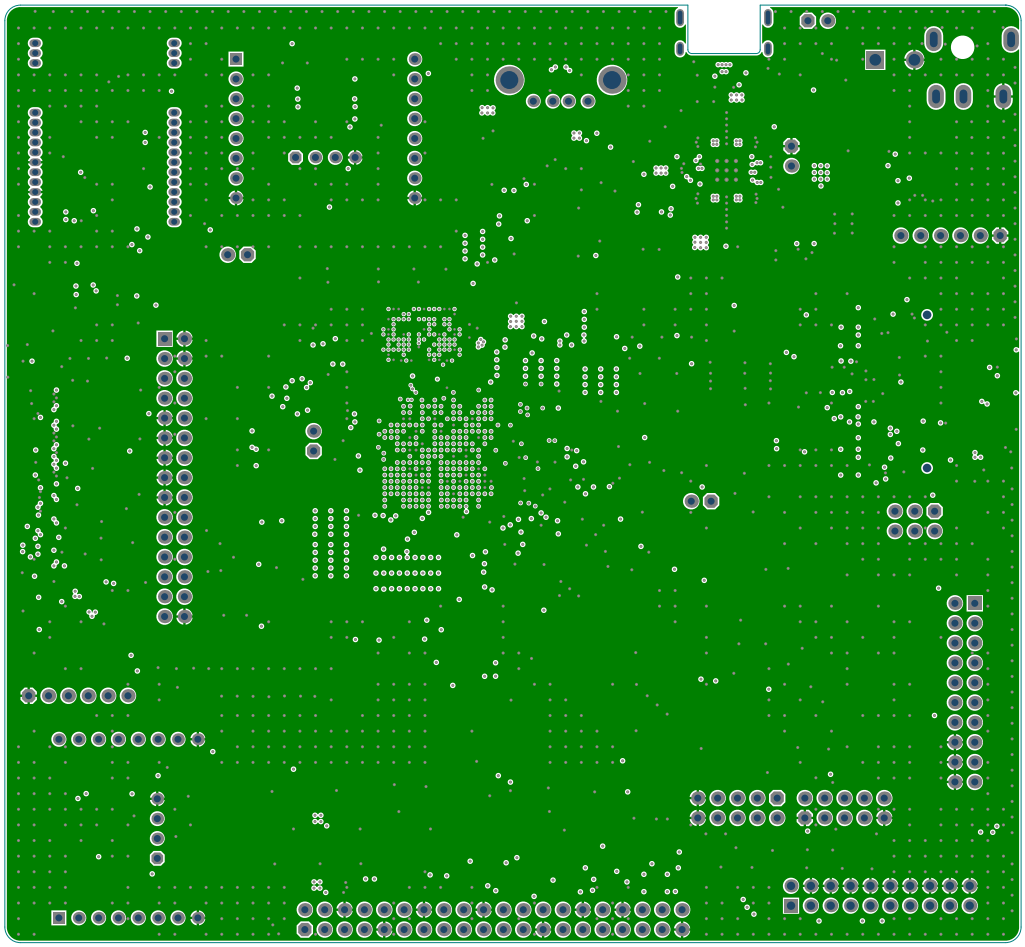


**Figure 7-16.** SAMA5D29-Curiosity Layout: Mid Layer 2 (Signal)

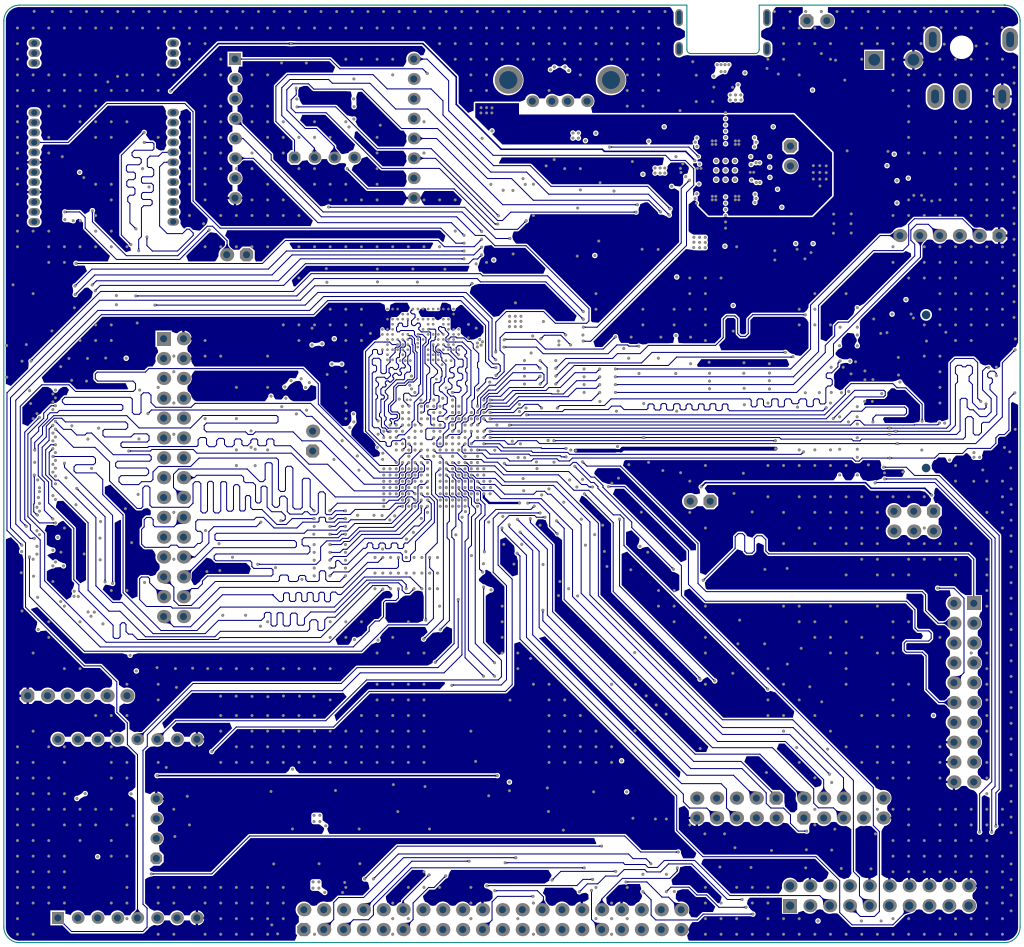


**Figure 7-17.** SAMA5D29-Curiosity Layout: Mid Layer 3 (Signal)

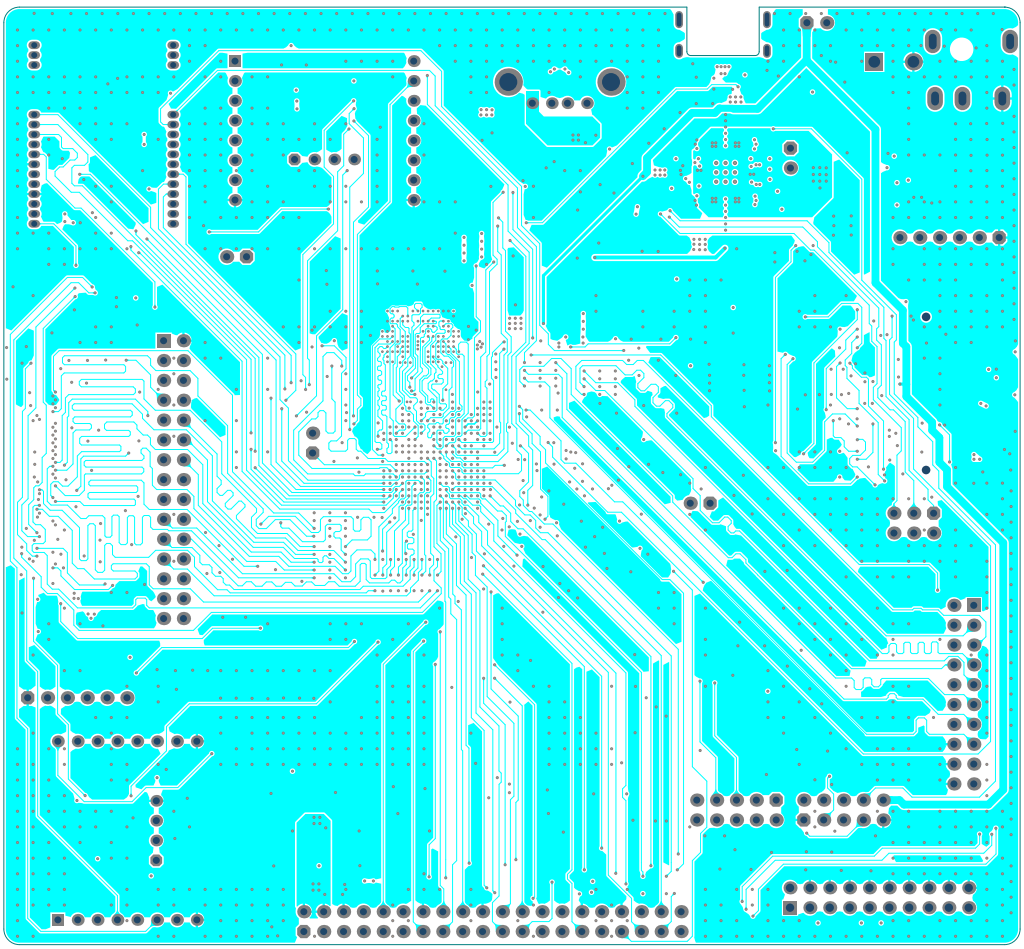


**Figure 7-18.** SAMA5D29-Curiosity Layout: Mid Layer 4 (Power)

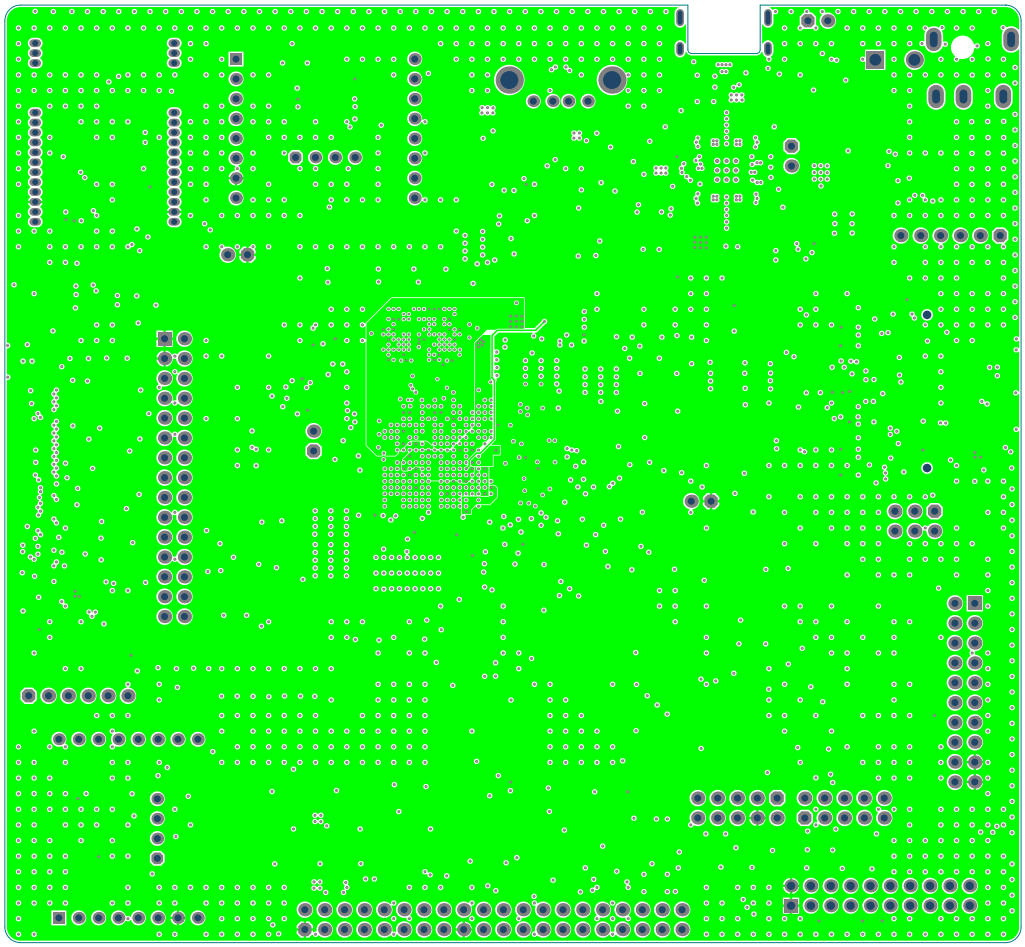


**Figure 7-19.** SAMA5D29-Curiosity Layout: Bottom Layer

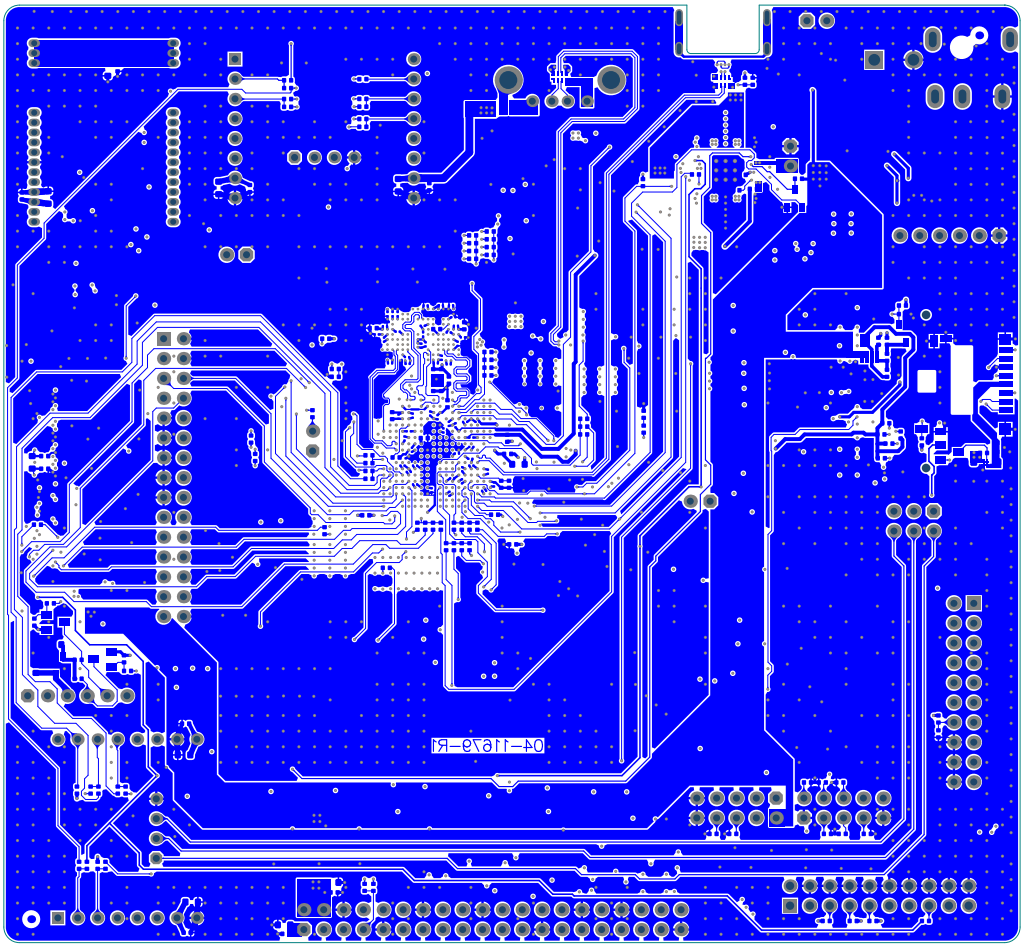


**Figure 7-20.** SAMA5D29-Curiosity Layout: Top Silkscreen

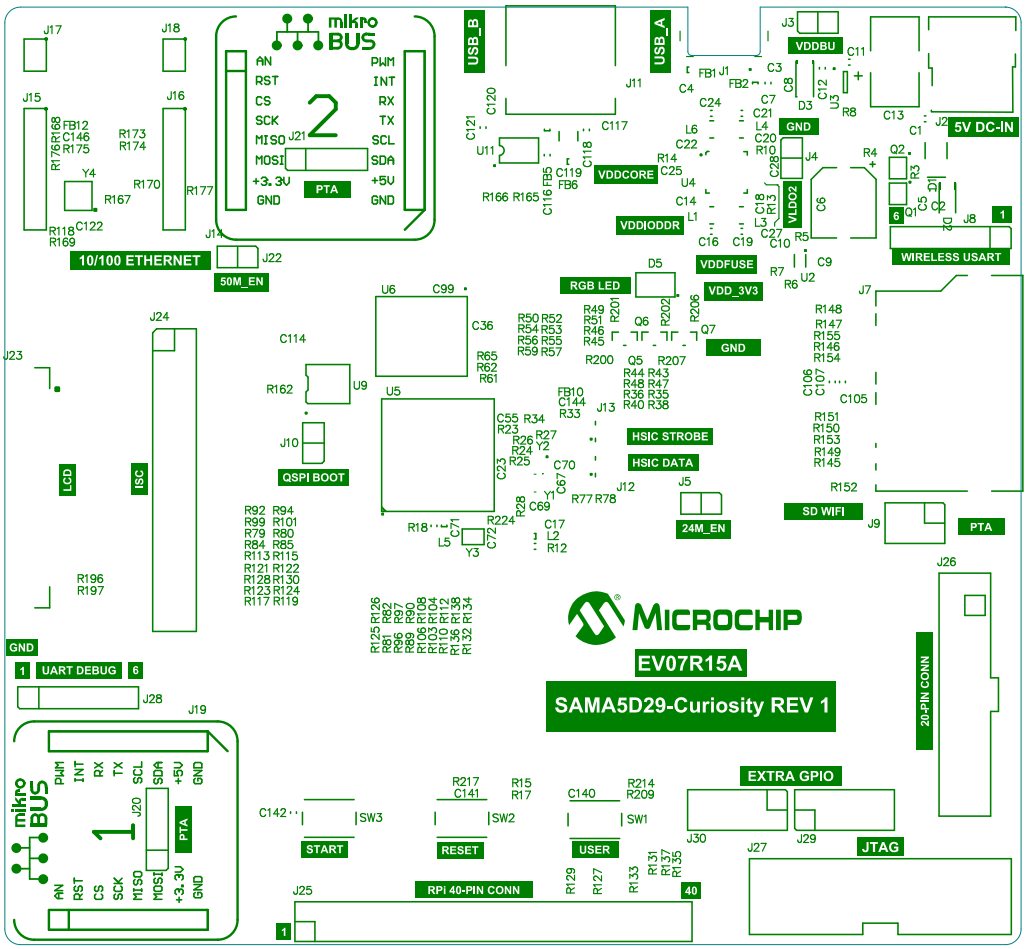
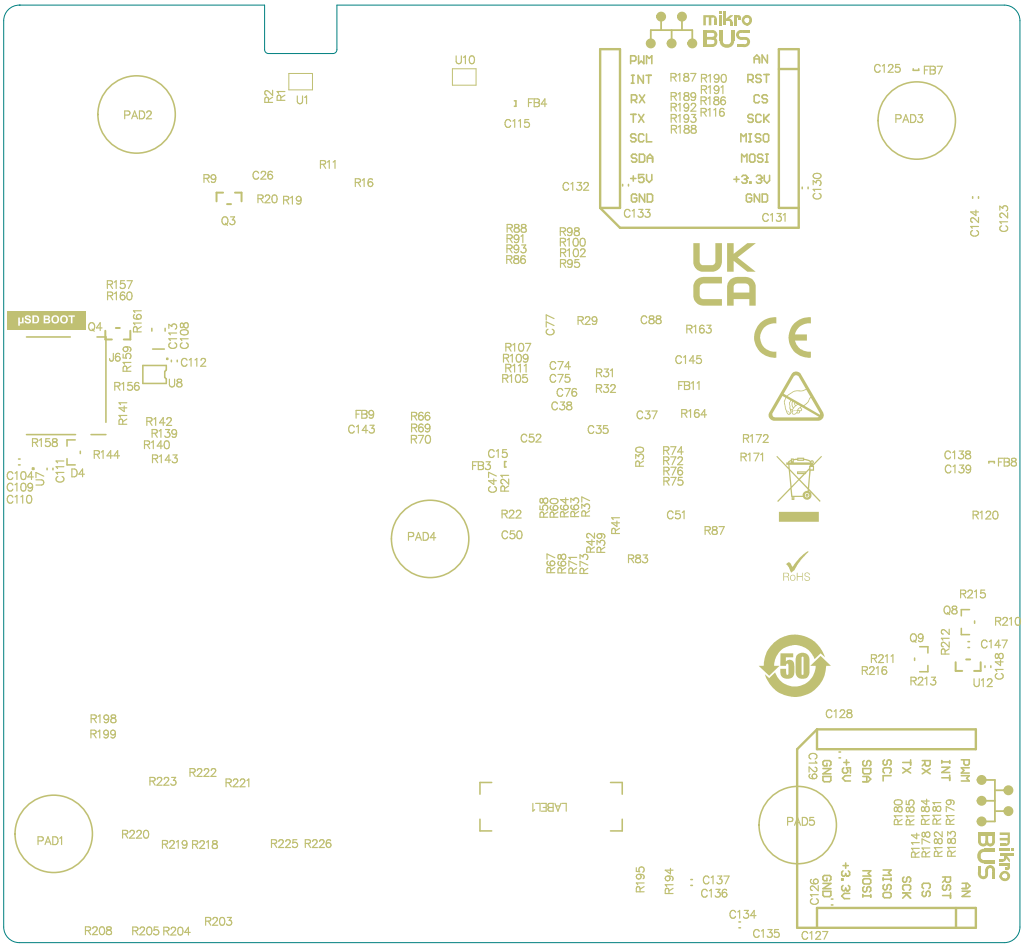


**Figure 7-21.** SAMA5D29-Curiosity Layout: Bottom Silkscreen



# 8. Revision History

## 8.1 Rev A - 09/2023

| |
|---|
| Initial release. |

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