ATSAMA5D2-ICP

SAMA5D2 Industrial Connectivity Platform (ICP) User's Guide

Scope

This user's guide describes how to use the SAMA5D2 Industrial Connectivity Platform (SAMA5D2-ICP) kit.

The SAMA5D2-ICP is a hardware and software platform that demonstrates the rich wired and wireless connectivity solutions around Microchip's SAMA5D2 Arm Cortex-A based microprocessors. It offers customers a starting point for their applications that include either EtherCAT, Ethernet 10/100 and 10/100/1000, CAN, Wi-Fi®, Bluetooth® or USB communications, or any combination of these. The board also features three mikroBUS™ click interface headers to support over 450 MikroElektronika Click boards™.

Figure 1. SAMA5D2-ICP Board

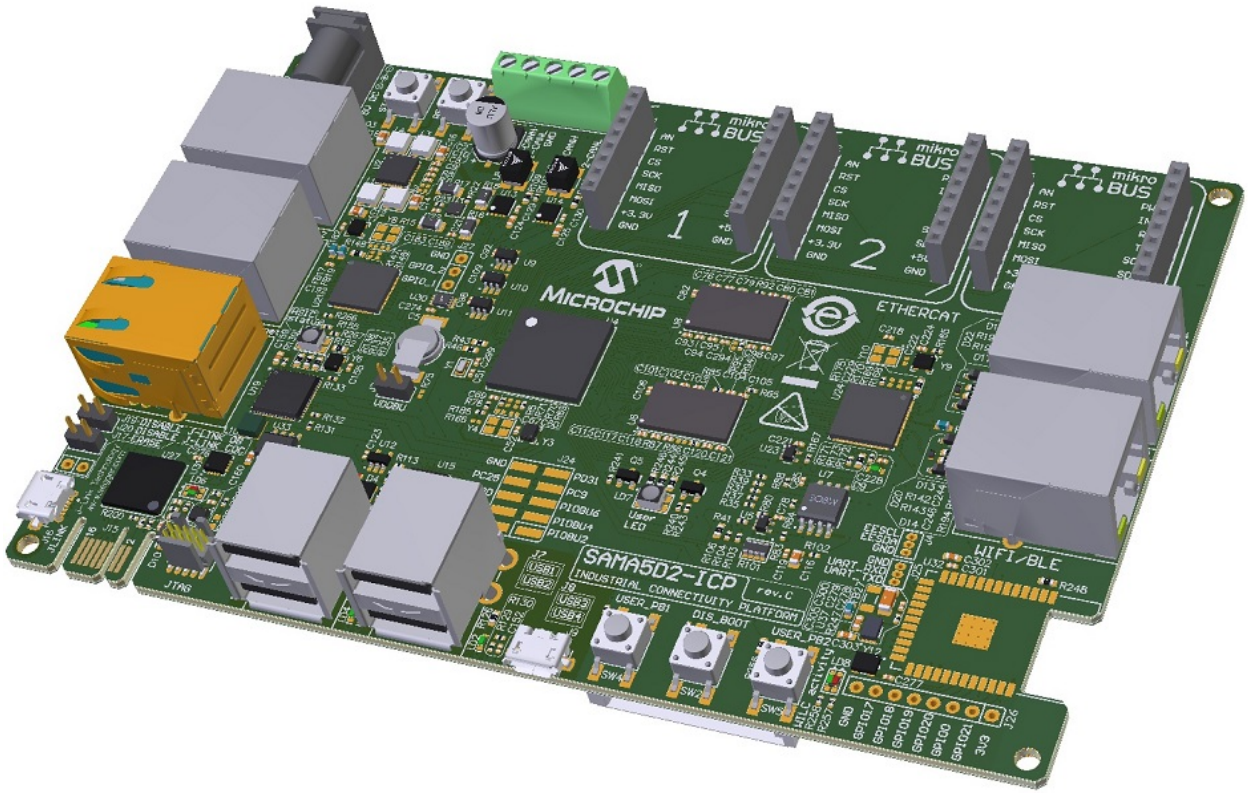


Table of Contents

1. Introduction

1.1 Document Layout

The document is organized as follows:

- Introduction
- Product Overview—Important information about the kit
- Board Components—Kit specifications and high-level description of the major components and interfaces
- Board Layout—Drawings
- Installation and Operation—Information on requirements and setup

1.2 Reference Documents

The following reference data sheets are available on www.microchip.com:

Table 1-1. SAMA5D2-ICP Component Data Sheets

Document Title	Available	Document Ref.
SAMA5D2 Series	https://www.microchip.com/ATSAMA5D27	DS60001476
MCP16502	https://www.microchip.com/MCP16502	DS20006275
PAC1932/3/4	https://www.microchip.com/PAC1934	DS20005850
SST26VF064B/SST26VF064BA	https://www.microchip.com/SST26VF064B	DS20005119
24AA02E48/24AA025E48/24AA02E64/24AA025E64	https://www.microchip.com/24AA025E48	DS20002124
MCP2542FD/4FD, MCP2542WFD/4WFD	https://www.microchip.com/MCP2542FD	DS20005514
USB2534	https://www.microchip.com/USB2534	DS00001713
MIC2026/2076	https://www.microchip.com/MIC2026	M9999-060410-B
LAN7850	https://www.microchip.com/LAN7850	DS00001993
KSZ8563R	https://www.microchip.com/KSZ8563	DS00002418
LAN9252	https://www.microchip.com/LAN9252	DS00001909
24AA512/24LC512/24FC512	https://www.microchip.com/24FC512	DS21754
ATWILC3000-MR110CA	https://www.microchip.com/ATWILC3000	DS70005327
93AA66A/B/C, 93LC66A/B/C, 93C66A/B/C	https://www.microchip.com/93AA66A	DS21795
ATECC608A	https://www.microchip.com/ATECC608A	DS40001977

2. Product Overview

The SAMA5D2 Industrial Connectivity Platform (SAMA5D2-ICP) provides a versatile Total System Solutions platform that highlights Microchip's MPU and connectivity ICs for industrial networking applications.

The board features three mikroBUS click interface headers to support over 450 MikroElektronika Click boards and provisions to solder a Microchip ATWILC3000-MR110CA or a ATWILC3000-MR110UA WiFi/BT module.

2.1 SAMA5D2-ICP Features

Table 2-1. SAMA5D2-ICP Features

Characteristics	Specifications	Components
Processor	SAMA5D27-CU (289-ball BGA), 14x14 mm body, 0.8 mm pitch	–
External Clocks	MPU: 12 MHz, 32.768 kHz Misc osc: 12, 24, 25 MHz	Oscillators and optional crystal
Memory	Two 16-bit, 2-Gbit DDR3L (total of 512 Mbytes) One QSPI Flash Three EEPROMs	Winbond® W632GU6MB Microchip SST26VF064B Microchip 24AA025E48
SD/MMC	One standard SD card interface	SD card connector
USB	One USB host switch 4 ports with power switch One USB device type Micro-AB	Microchip USB2534
CAN	Two CAN interfaces	Microchip MCP2542FDT
Ethernet	One Gigabit Ethernet PHY through HSIC One ETH switchport One EtherCAT interface	Microchip LAN7850T-I/8JX Microchip KSZ8563RNXI Microchip LAN9252I/ML
Wi-Fi/BT	Footprint for IEEE® 802.11 b/g/n Wi-Fi plus Bluetooth Module (Wi-Fi/BT), suitable for Microchip WILC3000-MR110CA or WILC3000-MR110UA	–
Debug port	One J-Link-OB/J-Link-CDC One JTAG interface	Embedded J-Link-OB and J-Link-CDC (ATSAM3U4C TFBGA100)
Board monitor	One RGB (Red, Green, Blue) LED DisableBoot, Reset, WakeUp, 2 x User Free push button switches	Common anode RGB LED 5 push button switches
Expansion	One PIOBU/PIO connector Three mikroBUS sockets	– –
Power management	One PMIC One power consumption measurement device	Microchip MCP16502 Microchip PAC1934
Board supply	From J16 and from external connector	µUSB and 2.1mm/5.5mm jack connector
Power saving	SuperCap	220 mF@3.3V

2.2 SAMA5D2-ICP Kit Content

The SAMA5D2-ICP kit includes the following:

- one SAMA5D2-ICP board
- one USB male A to USB male Micro-B cable

2.3 Evaluation Kit Specifications

Table 2-2. Evaluation Kit Specifications

Characteristic	Specification
Board	SAMA5D2-ICP
Board supply voltage	External and USB-powered
Temperature	Operating: 0°C to +70°C Storage: –40°C to +85°C
Relative humidity	0 to 90% (non-condensing)
Main board dimensions	150 × 100 × 20 mm
RoHS status	Compliant
Board identification	SAMA5D2-ICP Industrial Connectivity Platform

2.4 Power Sources

Two options are available to power up the SAMA5D2-ICP board:

- Through an external AC to DC +5V wall adapter connector (J1 – default configuration)
- Through the USB Micro-AB connector on the J-Link-OB Embedded Debugger interface (J16)

Table 2-3. Electrical Characteristics

Electrical Parameter	Value
Input voltage	5VCC
Maximum input voltage (limits)	6VCC
Maximum DC 3.3V current available	1.2A
I/O voltage	3.3V only

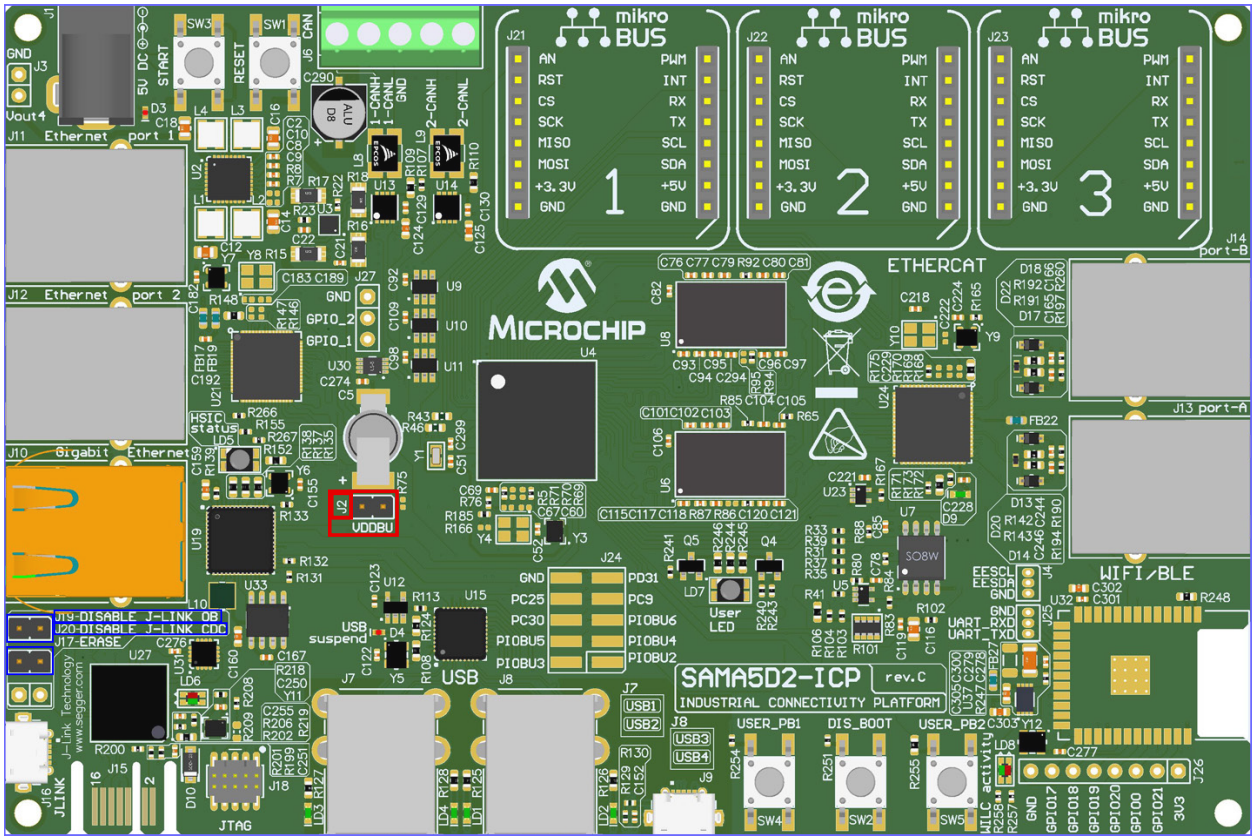
3. Board Components

This section covers the specifications of the SAMA5D2-ICP and provides a high-level description of the board's major components and interfaces. This document is not intended to provide a detailed documentation about the processor or about any other component used on the board. For detailed device documentation, refer to Reference Documents.

3.1 Board Overview

The fully-featured SAMA5D2-ICP board integrates multiple peripherals and interface connectors as shown in the figure below. J2, indicated in red below, offers current measurement connectivity. J19 and J20, indicated in blue, are configuration items.

Figure 3-1. Board Overview



3.1.1 Default Jumper Settings

The following table shows the default jumper settings.

Table 3-1. SAMA5D2-ICP Jumper Settings

Jumper	Default	Function
J2	Closed	VDDBU current measurement
J17	Open	Erases SAM3U firmware (not populated, reserved for factory configuration, should never be used by the end user).
J19	Open	Enables JTAG-OB (closed=disables JTAG-OB)
J20	Open	Enables JTAG-CDC (closed=disables JTAG-CDC)

3.1.2 On-Board Connectors

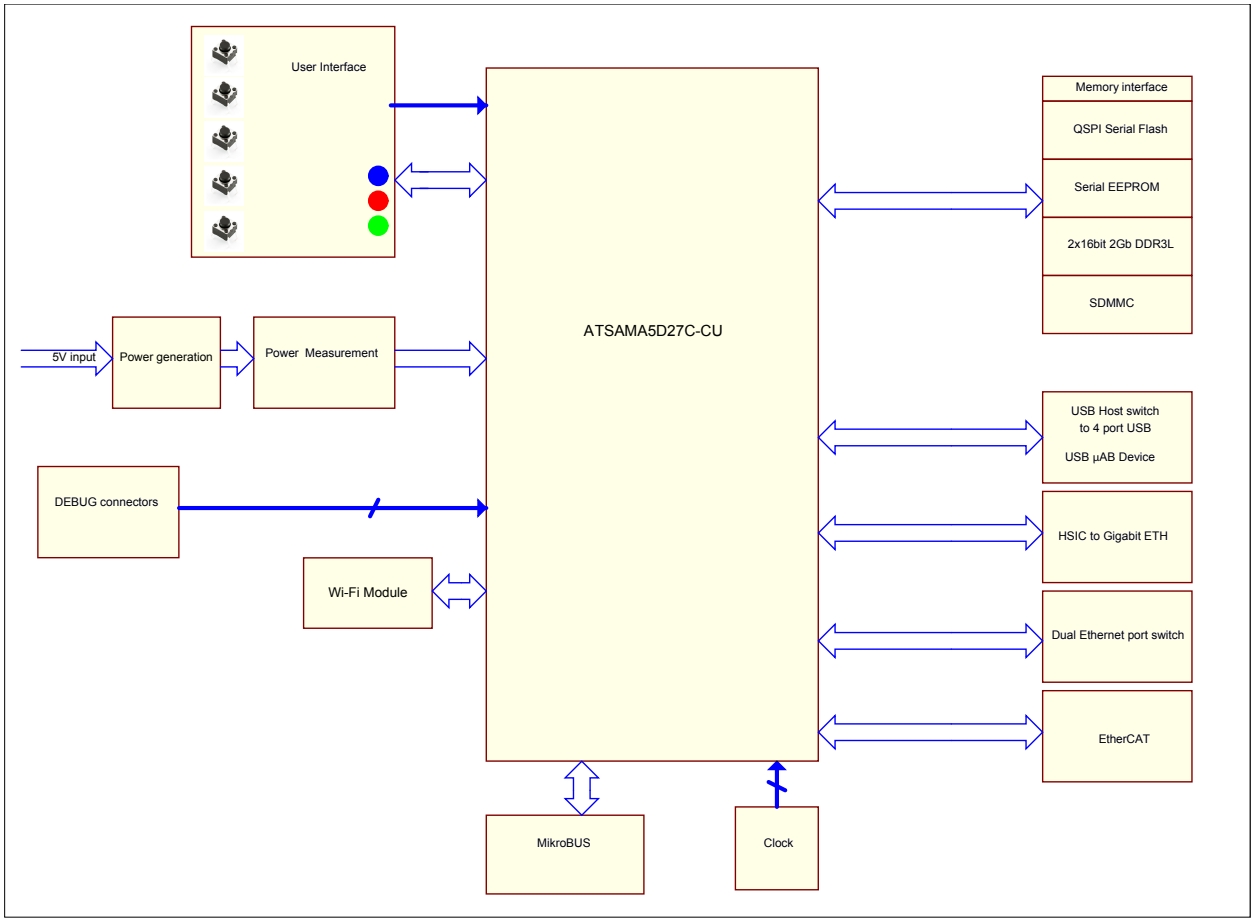
The following table describes the interface connectors on the SAMA5D2-ICP.

Table 3-2. SAMA5D2-ICP Board Interface Connectors

Connector	Interfaces to	Connector	Interfaces to
J1	External power jack	J14	EtherCAT RJ45 port B
J3	PMIC Vout4	J15	PCB connector for factory-programming the J-Link-OB
J4	Used for one-time programming of the EtherCAT EEPROM	J16	USB Micro-AB J-Link-OB/J-Link-CDC
J5	Standard SDMMC connector	J18	JTAG, 10-pin IDC connector
J6	Dual CAN	J21	mikroBUS1 connector
J7	Stacked USB type B (USB hub)	J22	mikroBUS2 connector
J8	Stacked USB type B (USB hub)	J23	mikroBUS3 connector
J9	USB Micro-AB (USB-A)	J24	Tampers and PIOs
J10	Ethernet 10/100/1000 RJ45 (HSIC)	J25	WILC3000 UART debug
J11	Ethernet 10/100 RJ45 (Etherswitch Port1)	J26	WILC3000 user-free GPIOs
J12	Ethernet 10/100 RJ45 (Etherswitch Port2)	J27	ETH switch user-free GPIOs
J13	EtherCAT RJ45 port A	–	

3.2 Function Blocks

Figure 3-2. SAMA5D2-ICP Block Diagram



3.2.1 Power Supply Topology and Power Distribution

3.2.1.1 Input Power Options

Two options are available to power up the SAMA5D2-ICP board:

1. an external AC to DC +5V wall adapter connected via a 2.1 mm center-positive plug into the board's power jack (J1). The recommended output voltage of the power adapter is 5V at 2A.
2. the USB J-Link-OB port (J16)

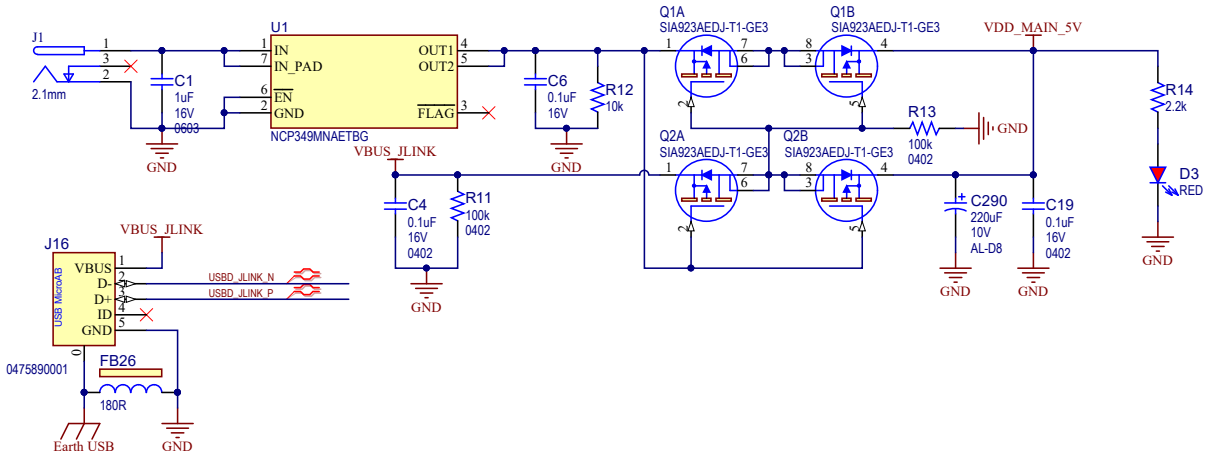
The +5V from the wall adapter is protected through an NCP349 positive overvoltage controller switch. The controller is able to disconnect the system from its output pin when incorrect input operating conditions are detected (5.83V max).

The USB-powered operation comes from the USB J-Link-OB port connected to a PC or a 5V DC supply. The USB supply is sufficient to power the board in most applications. It is important to note that when the USB supply is used, the USB port has limited power. If the USB host port is required for the application, it is recommended to use the external DC supply.

The red D3 ON LED indicates the presence of a 5V power supply from the wall adapter or from USB.

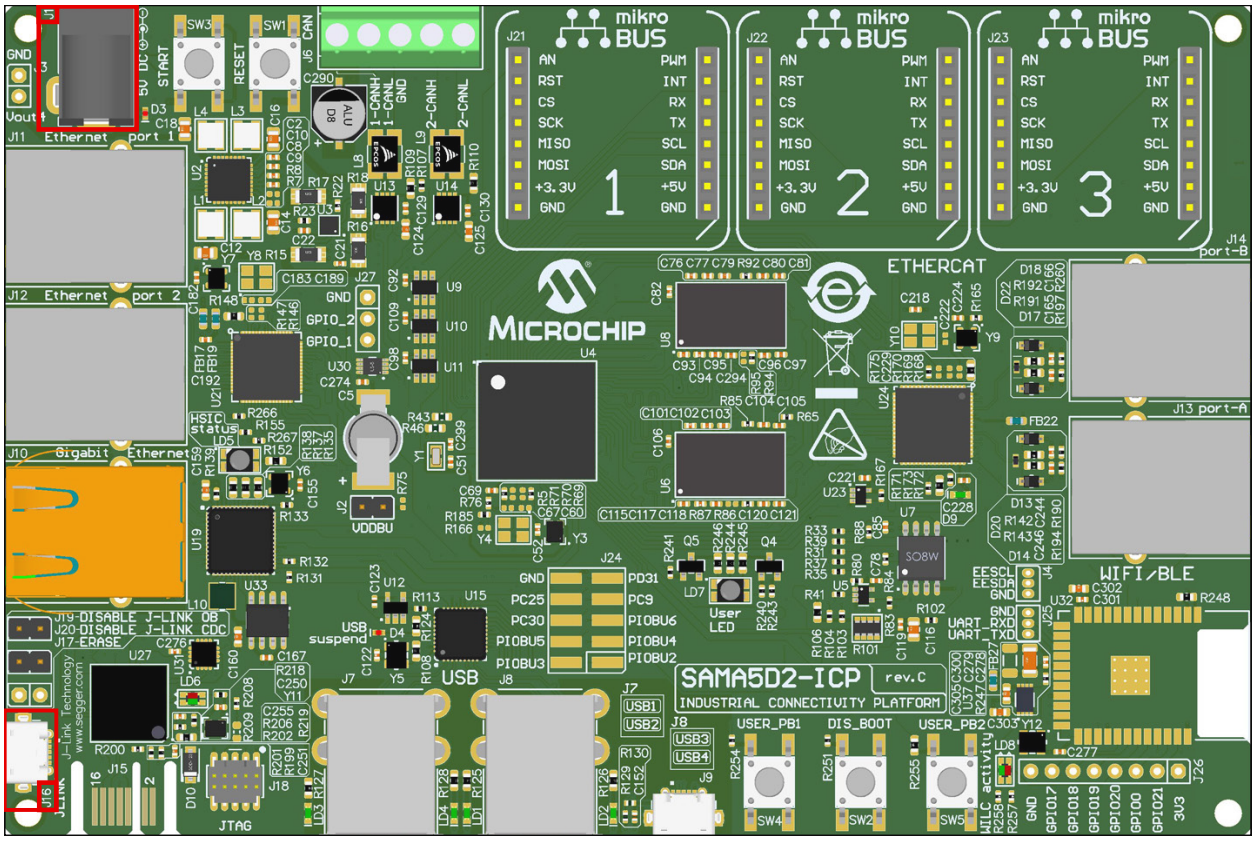
The figure below shows the input power supply topology.

Figure 3-3. Input Powering



USB-powered operation eliminates additional wires and batteries. It is the preferred mode of operation for any project that requires only a 5V source at up to 500 mA.

Figure 3-4. Power Supply Connector and USB J-Link-OB Port Location



3.2.1.2 Power Supply Requirements and Restrictions

Detailed information on the device power supplies is provided in tables “SAMA5D2 Power Supplies” and “Power Supply Connections” in the SAMA5D2 Series data sheet.

3.2.1.3 Power-Up and Power-Down Considerations

Power-up and power-down considerations are described in section “Power Considerations” in the SAMA5D2 Series data sheet.

3.2.1.4 Power Management

The board power management uses a Microchip PMIC, MCP16502. This is a complete, cost-effective and highly-efficient power management solution, optimized to provide a single-chip power solution and voltage sequencing for Microchip’s MPU series.

The MCP16502AA features:

- Four DC-DC buck regulators. Each buck channel can support loads up to 1A. Each DC-DC regulator is optimized for its target load, namely:
  - Buck 1: 3.3V for I/Os and other analog loads
  - Buck 2: 1.35V for DDR3L voltage
  - Buck 3: 1.25V for core voltage
  - Buck 4 is unused for this application, can be accessed by users via J3 connector.
- Two 300 mA LDOs, 2.5V for VDDFUSE and 3.3V for RGB LEDs
- Support of Hibernate, Low-Power and High-Performance modes
- Interrupt flag, control PIOs and I2C interface

The default power channel sequencing is built-in, according to the requirements of the MPU. A dedicated pin (LPM) facilitates the transition to Low-Power modes. The MCP16502 features a low no-load operational quiescent current and draws less than 10 µA in full shutdown. Active discharge resistors are provided on each output. All buck channels support safe start-up into pre-biased outputs.

3.2.1.4.1 Configuration

Buck 2 default voltage is selected by means of the hardwired SELV2 pin and cannot be changed on-the-fly during operation (high-Z 1.35V DDR3L).

LDO1 default voltage is selected by means of the hardwired SELVL1 pin and cannot be changed on-the-fly during operation (high-Z 2.5V VDDFUSE).

3.2.1.4.2 Interfacing Signals

The MCP16502 is interfaced to the host MPU by means of the following signals:

- nSTRTO (open-drain output)
- nRSTO (open-drain output)
- nINTO (open-drain output)
- PWRHLD (input)
- LPM (input) and HPM (input)
- SDA and SCL (I2C interface pins)

Note: The MCP16502 is a slave-only device without clock stretching capability. Therefore, the SCL pin is an input only.

3.2.1.4.3 nSTRT, nSTRTO, PWRHLD Functionality

The nSTRT (push button input) serves as an external initialization input to the PMIC. nSTRT is internally pulled up to SVIN and monitored. When the nSTRT is pulled/detected LOW (SW3 pressed), the MCP16502 initiates the turn-on sequence.

The nSTRTO signal is asserted LOW whenever the nSTRT is detected to be LOW, and it is high-Z otherwise (nSTRTO has an external pull-up resistor).

While nSTRT is LOW during the power-up sequence, the MCP16502 expects the assertion of the PWRHLD signal (power-hold) from the MPU to continue the sequence.

PWRHLD may be already HIGH in a typical application using a backup supply. If PWRHLD has NOT been asserted HIGH by the MPU before completion of the start-up sequence (i.e., when nRSTO is asserted high), the MCP16502 automatically initiates a turn-off sequence.

After the assertion of PWRHLD, nSTRT should be released before the long-press time-out timer expires.

During run time (PWRHLD=HIGH), the nSTRT (thus nSTRTO) can be asserted LOW again. No automatic action is taken by the MCP16502 in this case unless the push button interrupt assertion time-out delay expires without any action from the MPU.

3.2.1.4.4 nSTRT / PWRHLD Typical Use Cases

The MPU can assert the PWRHLD pin via the SHDN command (which is a VDDBU-powered I/O) to shut down all regulators and enter Backup mode. All regulators are also shut down by the action of the SHDN signal. NRST is asserted low.

Depending on the presence of a backup supply (supercap populated) and by action on the wakeup signal connected at nSTRT (SW1 push button), the MCP16502 initiates a turn-on sequence.

3.2.1.4.5 PWRHLD, LPM, HPM and Power States Definitions

PWRHLD, LPM and HPM define different power states.

Other logic combinations of PWRHLD, LPM and HPM (after HPM unmasking) are forbidden.

The initial state is the OFF state (shutdown).

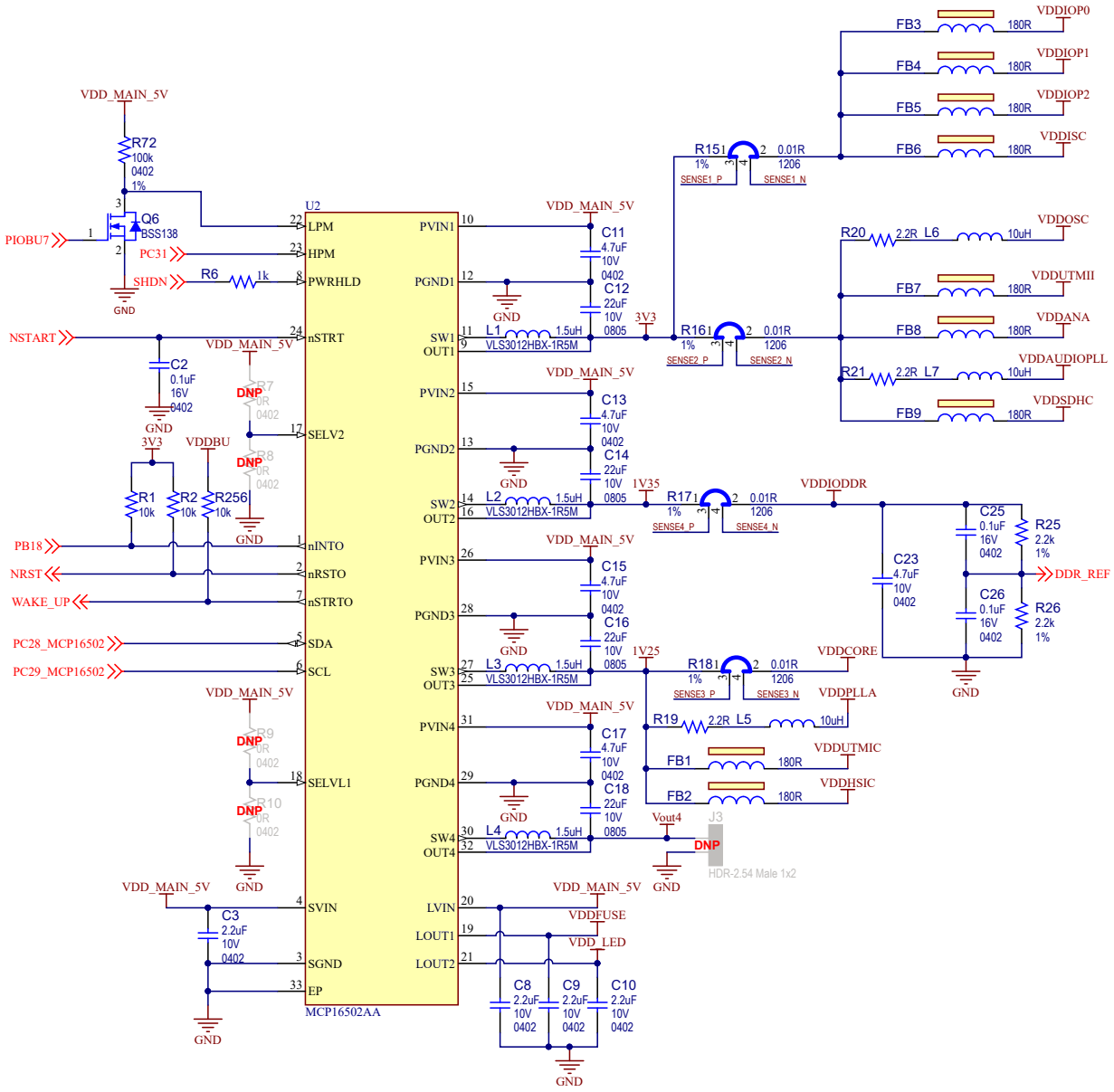
Table 3-3. PMIC Power States for Configurations of PWRHLD, LPM and HPM

PWRHLD	LPM	HPM	Buck1	Buck2	Buck3	Buck4	LDO1	LDO2	nRSTO	Power State
0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	LOW	OFF
0	1	0	OFF	ON Auto PFM	OFF	OFF	OFF	OFF	LOW	HIBERNATE
1	1	0	ON Auto PFM	ON Auto PFM	ON Auto PFM	ON Auto PFM	ON	OFF	High-Z	Low-Power mode 1 (default Low-Power mode)
						OFF				Low-Power mode 2 (achieved through I^2C programming)
1	0	0	ON FPWM	ON FPWM	ON FPWM	ON FPWM	ON	OFF	High-Z	Active
1	0	1	ON FPWM	ON FPWM	ON FPWM	ON FPWM	ON	OFF	High-Z	High-Performance Active

3.2.1.4.6 I^2C Interface Description

The figure below depicts MCP16502 power management.

Figure 3-5. Board Power Management



The MCP16502 is a Fast mode Plus device, supporting data transfers at up to 1 Mbit/s as described in the I²C Bus specification. The MCP16502 is a slave-only device without clock stretching capability. The MCP16502 assumes that the I²C logic levels on the bus are generated by a device operating from a nominal supply voltage of 3.3V (with ±10% tolerance). This is typically the I/O voltage generated by Buck1 (VDDIO). Therefore, VIH and VIL are not related to the SVIN voltage value. The SDA and SCL lines should not be pulled up to the MCP16502 SVIN voltage, but to the I²C master interface supply voltage (3.3V nominal). The MCP16502 I²C interface is always accessible, even in the OFF state, as long as the SVIN pin is powered. In the OFF state, the VDDIO voltage from Buck1 is turned off and therefore the I²C pullup rail must be provided externally.

For more information, refer to the PMIC MCP16502 data sheet.

Table 3-4. PMIC Signal Descriptions

PIO	Mnemonic	Shared PIO	Signal Description
PIOBU7	LPM	–	Low-Power mode input pin. In combination with PWRHLD and HPM, this pin defines the power mode status of the MCP16502.
PC31	HPM	–	High-Performance mode input pin. In combination with PWRHLD and LPM, this pin defines the power mode status of the MCP16502.
SHDN	PWRHLD	–	Power hold input. Typically asserted high by the MPU to maintain power after the initial startup triggered by nSTRT. PWRHLD will be asserted low by the MPU to initiate a PMIC shutdown sequence.
PB_NSTRT	nSTRT	–	Start event input. Drive nSTRT low to initiate a start-up sequence. nSTRT is internally pulled up.
PB18	nINT0	–	Active low, open-drain interrupt output
NRST	nRSTO	NRST	Active low, open-drain reset output
PC28	TWD	POWER TWI	TWI interface serial data
PC29	TWCK	POWER TWI	TWI interface serial clock

3.2.1.5 Current Measurement

The SAMA5D2-ICP board embeds one PAC1934. The PAC1934 is a four-channel DC power/energy monitor with accumulator. A 16-bit ADC is used to measure voltages across a current sense resistor, connected by a differential multiplexer to (+) and (-) inputs for each channel.

Four current sense resistors (10 mΩ) are populated on-board for measuring voltage on power rails:

- 3.3V VDDIOP group (SENSE1_P and SENSE1_N)
- 3.3V VDDOSC, VDDUTMII, VDDANA, VDDAUDIOPLL, VDDSDHC (SENSE2_P and SENSE2_N)
- 1.35V VDDIODDR (SENSE4_P and SENSE4_N)
- 1.25V VDDCORE (SENSE3_P and SENSE3_N)

The PAC1934 communicates with the MPU via a TWI bus.

The figure below shows the current measurement.

Figure 3-6. PAC1934 Current Measurement

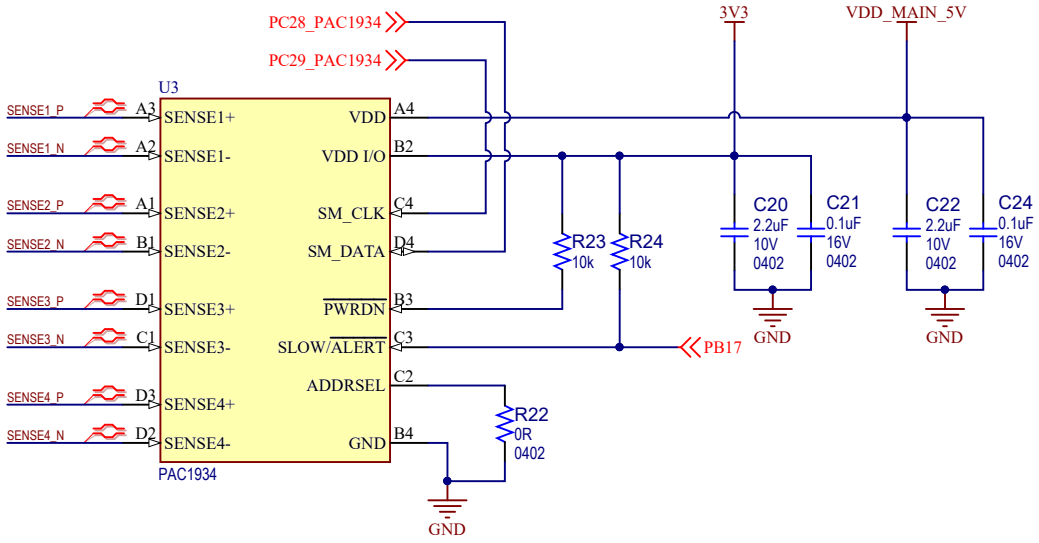


Table 3-5. PAC1934 Signal Descriptions

PIO	Mnemonic	Shared PIO	Signal Description
PC28	PC28_PAC1934	POWER TWI	TWI data
PC29	PC29_PAC1934	POWER TWI	TWI clock
PB17	INT_PAC1934	–	Interrupt

3.2.2 Processor

The Microchip SAMA5D2 Series is a high-performance, power-efficient embedded MPU based on the Arm® Cortex®-A5 processor running up to 500 MHz, with support for multiple memories such as DDR2, DDR3, DDR3L, LPDDR1, LPDDR2, LPDDR3, and QSPI Flash. The devices integrate powerful peripherals for connectivity and user interface applications, and offer advanced security functions (Arm TrustZone®, tamper detection, secure data storage, etc.), as well as high-performance cryptoprocessors AES, SHA and TRNG.

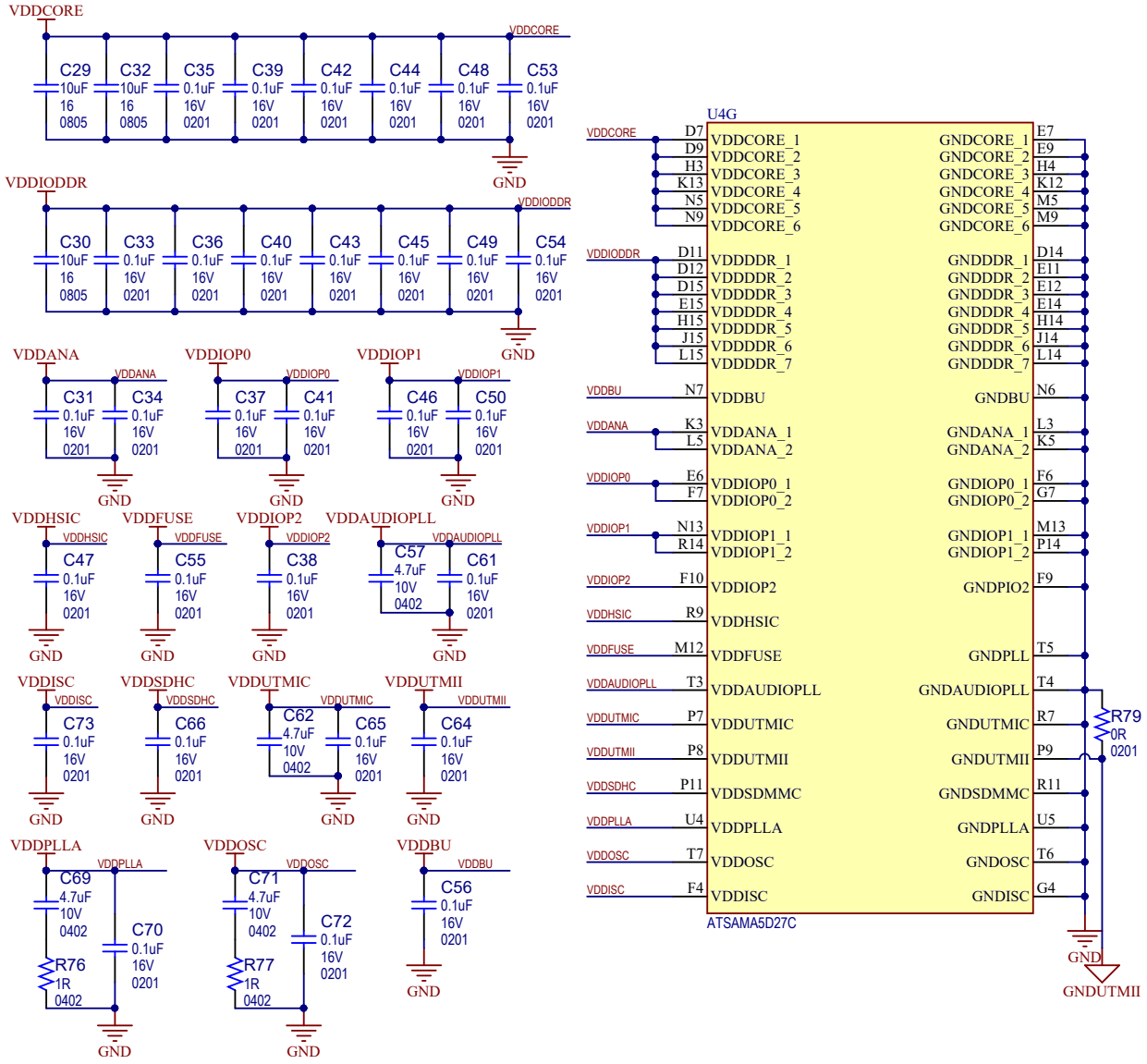
For more information about the SAMA5D27 MPU, refer to the SAMA5D2 Series data sheet.

3.2.2.1 Supply Group Configuration

The main regulators provide all power supplies required by the SAMA5D27 device:

- 1.25V VDDCORE, VDDPLLA, VDDUTMIC, VDDHSIC
- 1.35V VDDIODDR
- 2.5V VDDFUSE
- 3.3V VDDIOP0, VDDIOP1, VDDIOP2, VDDISC
- 3.3V VDDOSC, VDDUTMI, VDDANA, VDDAUDIOPLL, VDDSDHC
- 3.3V VDDBU

Figure 3-7. Processor Power Lines Supplies

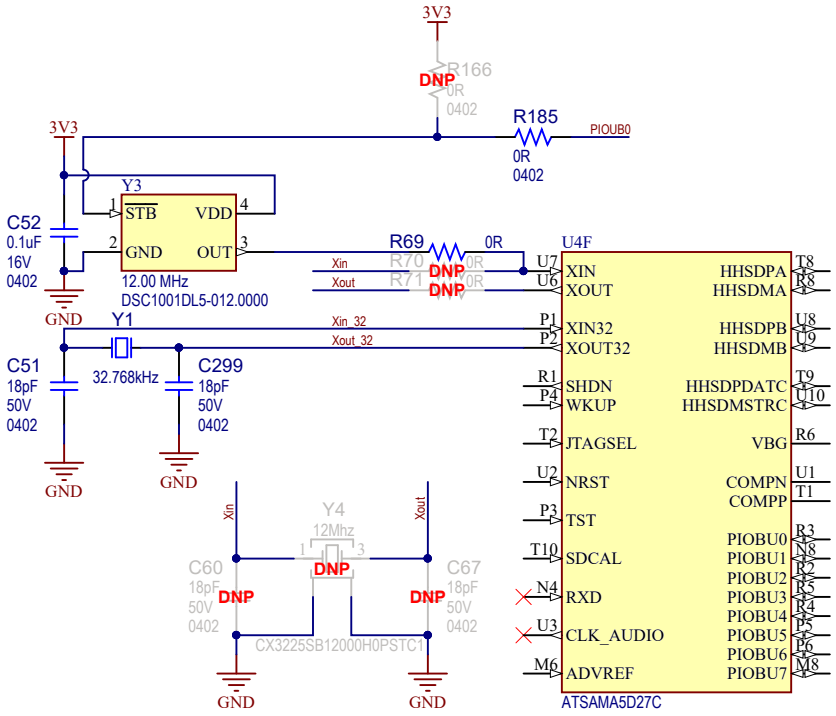


3.2.3 Clock Circuitry

The embedded MPU generates the necessary clocks based on two oscillators: one slow clock (SLCK) crystal running at 32.768 kHz and one main clock oscillator running at 12 MHz. An optional 12 MHz crystal is available as an alternative to the DSC1001DL5-012.0000 oscillator.

Note: PIOBU0 can be used to disable the 12 MHz main oscillator (Y3).

Figure 3-8. MPU Clock Circuitry

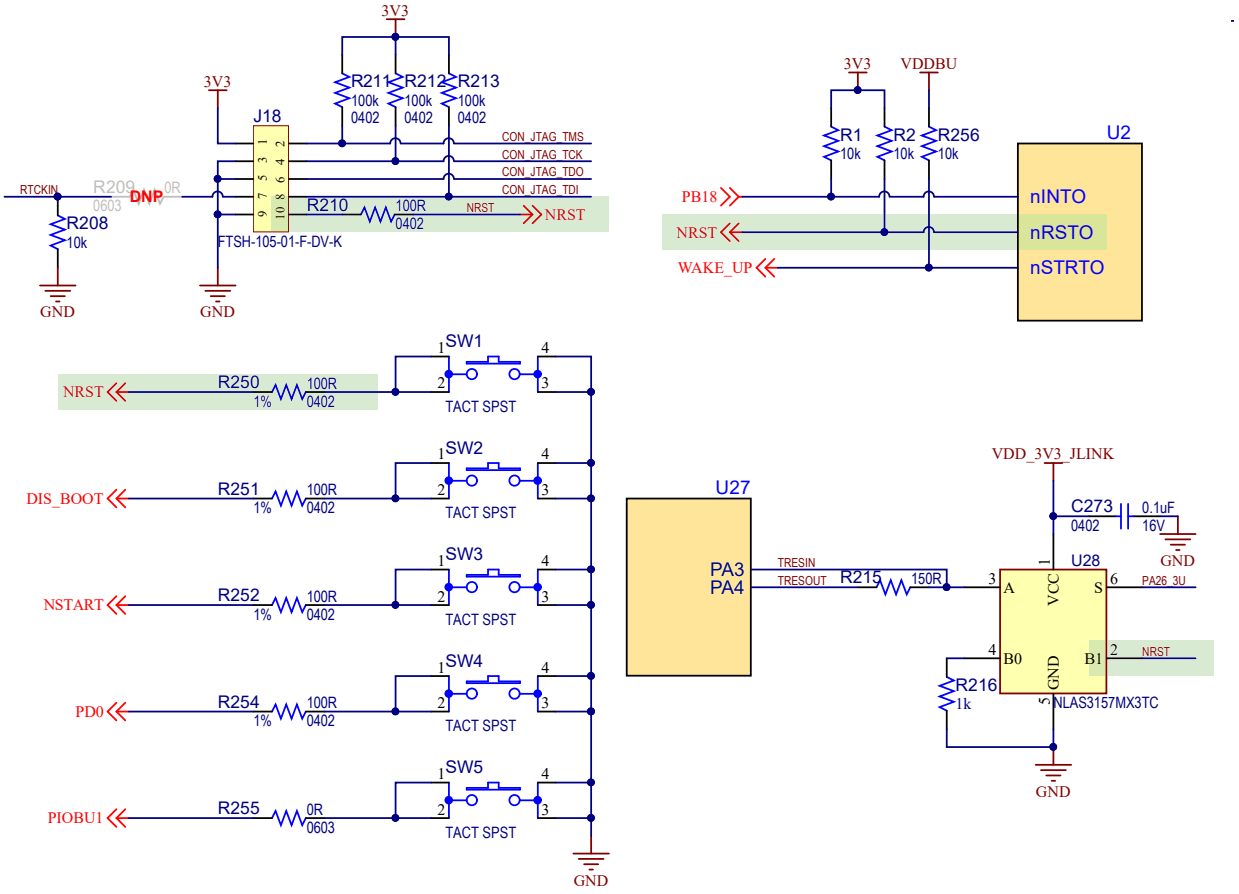


3.2.3.1 Reset Circuitry

The reset sources for the SAMA5D2-ICP board are:

- Power-on Reset from the PMIC MCP16502
- Push button reset SW1
- External JTAG or J-Link-OB reset from an in-circuit emulator

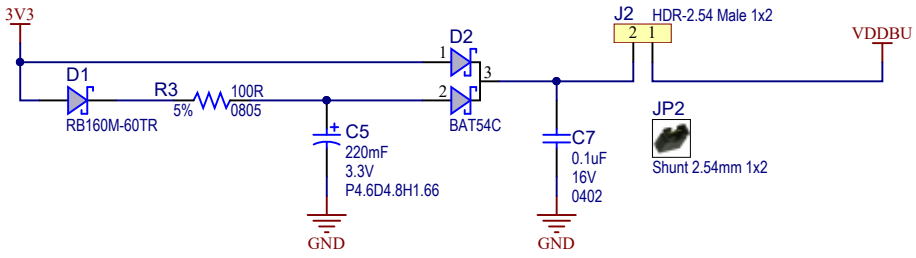
Figure 3-9. Reset Circuitry



3.2.3.2 Power Backup Supply

The SAMA5D2-ICP board requires a power source in order to permanently power the backup part of the SAMA5D27 device (refer to the SAMA5D2 Series data sheet). A super capacitor sustains such permanent power to VDDBU when all system power sources are off.

Figure 3-10. VDDBU Powering Option



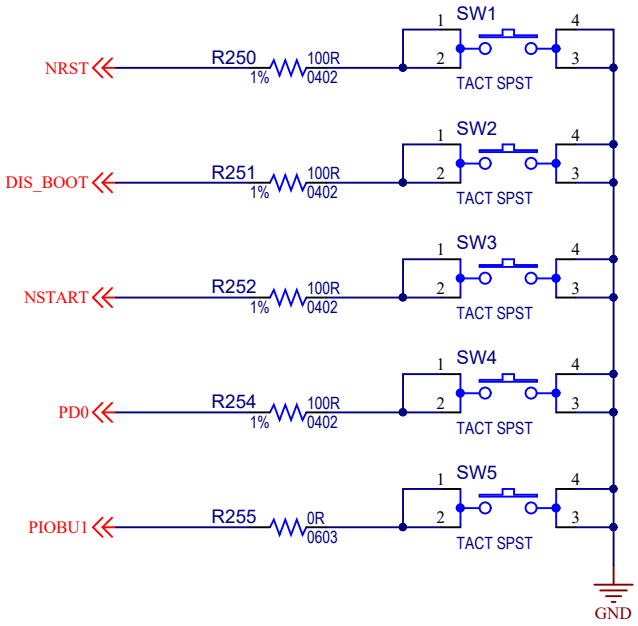
3.2.4 Push Button Switches

The SAMA5D2-ICP features five push buttons:

- One reset push button (SW1). When pressed and released, it causes a general reset of the board

- One wake-up push button (SW3) connected to the nSTRT pin of the PMIC, used to signal to the PMIC to initiate a power-on sequence and to make the processor exit Low-Power mode
- One disable boot push button (SW2) used to invalidate the boot memories (see the section CS Disable)
- Two user push buttons (SW4 and SW5) connected to PIO PD0 and PIOBU1

Figure 3-11. System Push Buttons



3.2.5 Memory

3.2.5.1 Memory Organization

The SAMA5D27 features a DDR/SDR memory interface and an External Bus Interface (EBI) to enable interfacing to a wide range of external memories and to a wide range of parallel peripherals.

This section describes the memory devices mounted on the SAMA5D2-ICP board:

- Two DDR3L SDRAMs
- One QSPI Flash
- Three serial EEPROMs

Additional memory can be added to the board by:

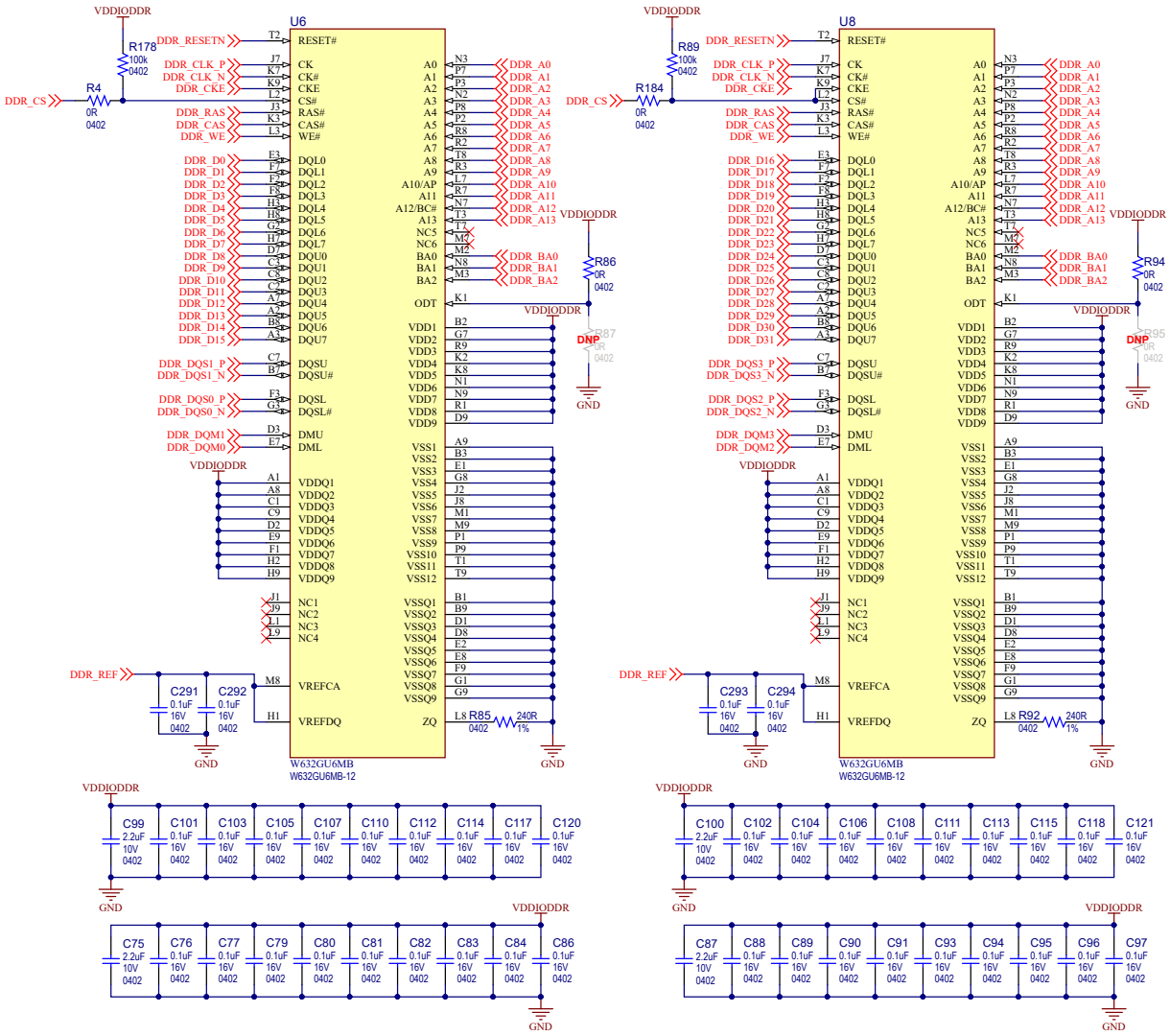
- Installing an SD or MMC card in the SD/MMC slot
- Using the USB ports

Support is dependent upon driver support in the OS.

3.2.5.2 DDR3L SDRAM

Two DDR3L SDRAMs (W632GU6MB 2 Gbits = 16, 777,216 words x 8 banks x 16 bits) are used as main system memory, totalling 4 Gbits of SDRAM on the board. The memory bus is 32 bits wide and operates with a frequency of up to 166 MHz.

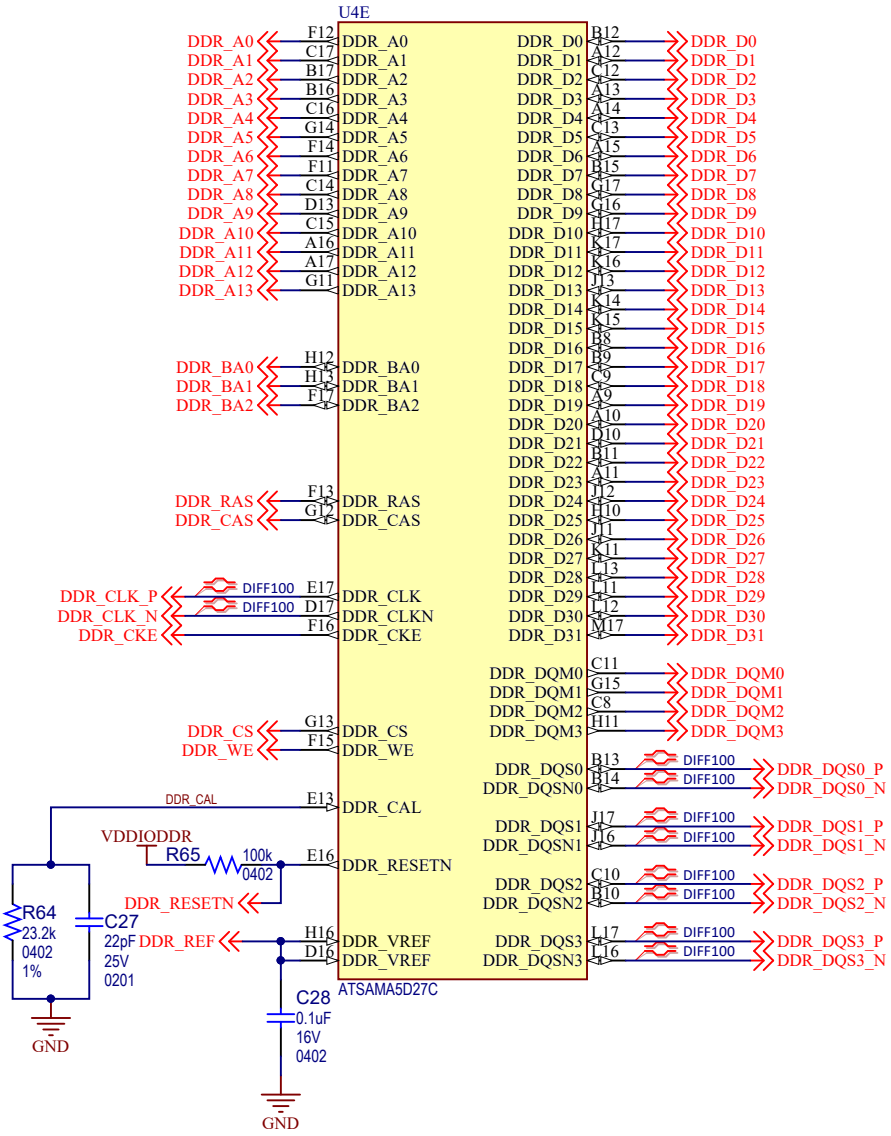
Figure 3-12. DDR3L SDRAM Implementation



3.2.5.3 DDR_CAL Analog Input

One specific analog input, DDR_CAL, is used to calibrate all DDR I/Os.

Figure 3-13. DDR Signals and CAL Analog Input



3.2.6 Additional Memories

3.2.6.1 QSPI Serial Flash

The SAMA5D27 provides one Quad Serial Peripheral Interface (QSPI).

A QSPI is a synchronous serial data link that provides communication with external devices in Master mode.

The QSPI can be used in SPI mode to interface with serial peripherals such as ADCs, DACs, LCD controllers, CAN controllers and sensors, or in Serial Memory mode to interface with serial Flash memories.

The QSPI allows the system to execute code directly from a serial Flash memory (XIP, or eXecute In Place, technology) without code shadowing to RAM. The serial Flash memory mapping is seen in the system as other memories (ROM, SRAM, DRAM, embedded Flash memory, etc.).

With the support of the Quad SPI protocol, the QSPI allows the system to use high-performance serial Flash memories which are small and inexpensive, instead of larger and more expensive parallel Flash memories.

The figure below illustrates a socket implementation for the QSPI Flash memory.

Figure 3-14. QSPI Serial Flash

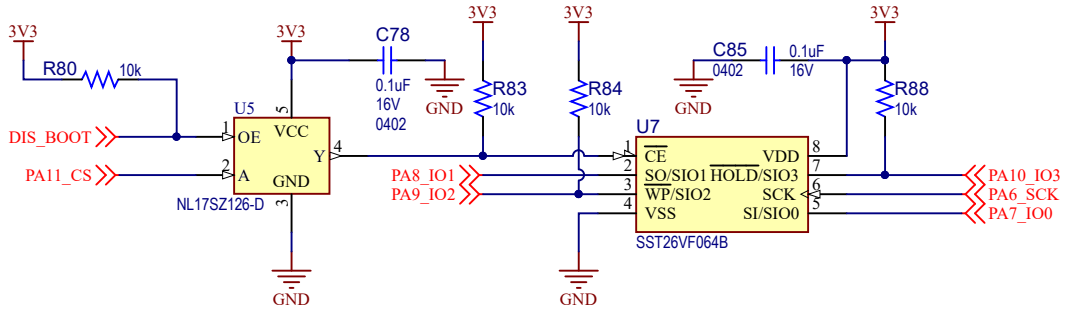


Table 3-6. QSPI Signal Description

PIO	Mnemonic	Shared PIO	Signal Description
PA6	QSPI0_SCK	WILC3000	QSPI clock
PA11	QSPI0_CS	–	Chip select
PA7	QSPI0_IO0	WILC3000	Data0
PA8	QSPI0_IO1	–	Data1
PA9	QSPI0_IO2	WILC3000	Data2
PA10	QSPI0_IO3	WILC3000	Data3

3.2.6.1.1 CS Disable

The on-board push button SW2 controls the selection (CS#) of the bootable memory components (QSPI) using a non-inverting 3-state buffer.

The rule of operation is:

SW2 (DISABLE_BOOT) pressed = booting from QSPI is disabled when a reset occurs

Refer to the SAMA5D2 Series data sheet for more information on standard boot strategies and sequencing.

3.2.6.2 CryptoAuthentication™

The ECC608A is a member of the Microchip CryptoAuthentication family of high-security cryptographic devices which combine world-class hardware-based key storage with hardware cryptographic accelerators to implement various authentication and encryption protocols.

The ECC608A includes an EEPROM array which can be used for storage of up to 16 keys, certificates, miscellaneous read/write, read-only or secret data, consumption logging, and security configurations. Access to the various sections of memory can be restricted in a variety of ways and then the configuration can be locked to prevent changes.

Table 3-7. ECC608A PIO Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PD19	TWD1	EEPROM TWI	TWI Data
PD20	TWCK1	EEPROM TWI	TWI Clock

ATECC608A-SSHDA is placed on the same TWI bus as the EEPROM memories and the three mikroBUS connectors.

Figure 3-15. ATECC608A-SSHDA Implementation

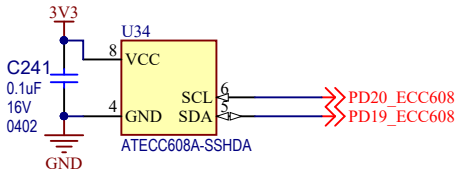
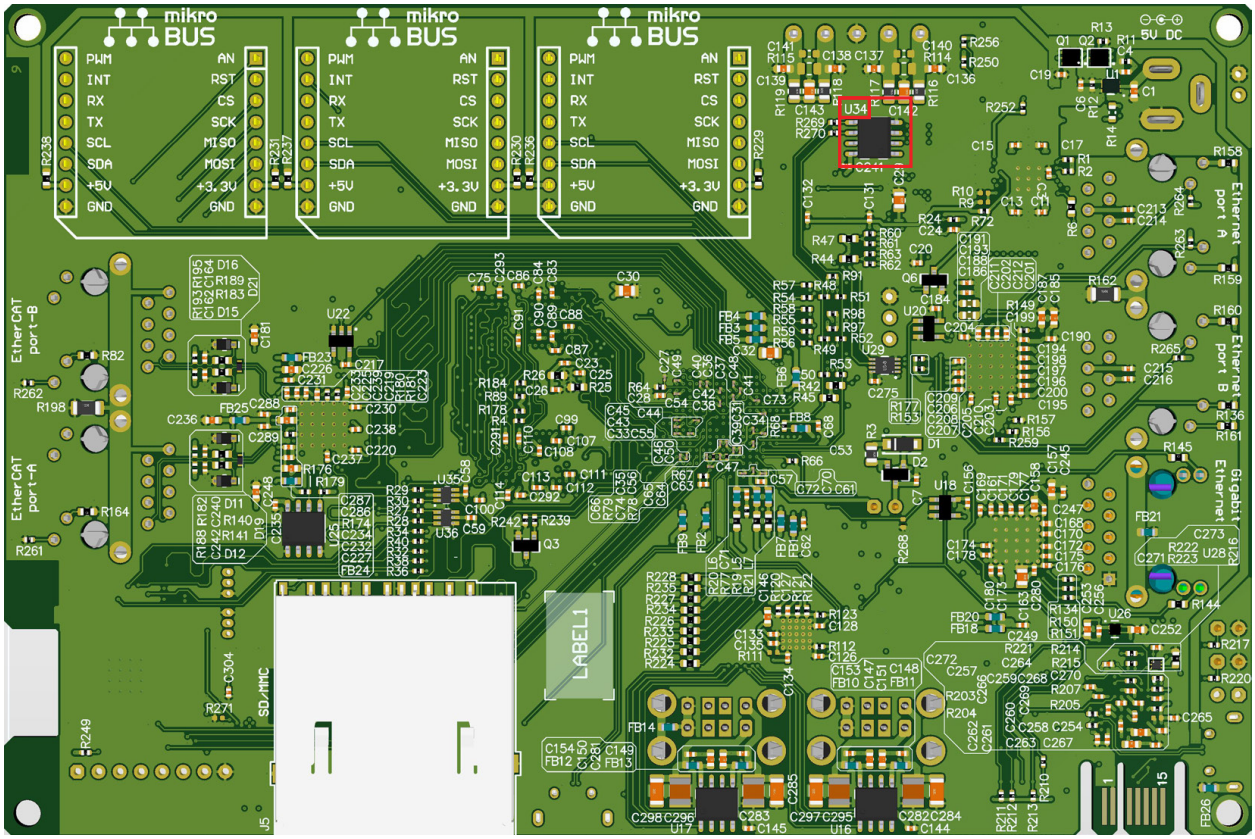


Figure 3-16. ATECC608A Location



3.2.6.3 Serial EEPROM with Unique MAC Address

The SAMA5D2-ICP board embeds three Microchip 24AA025E48 I2C serial EEPROMs using the TWI1 interface.

The TWI interface is I^2C compatible; it uses only two lines, namely serial data (SDA) and serial clock (SCL). According to the standard, the TWI clock rate is limited to 400 kHz in Fast mode and 100 kHz in Normal mode, but a configurable baud rate generator permits the output data rate to be adapted to a wide range of core clock frequencies. The TWI supports both Master and Slave modes.

The 24AA025E48 provides 2048 bits of serial Electrically-Erasable Programmable Read-Only Memory (EEPROM) organized as two blocks of 128 x 8-bit memory. In addition, the 24AA025E48 incorporates an easy and inexpensive method to obtain a globally unique MAC or EUI address (EUI-48™).

The EUI-48 addresses can be assigned as the actual physical address of a system hardware device or node, or it can be assigned to a software instance. These addresses are factory-programmed by Microchip and guaranteed unique.

⚠ CAUTION One EEPROM device at the address 50h is used as a “software label” to store board information such as chip type, manufacturer name and production date, using the last two 16-byte blocks in memory. The information contained in these blocks should not be modified.

Table 3-8. EEPROM TWI Address

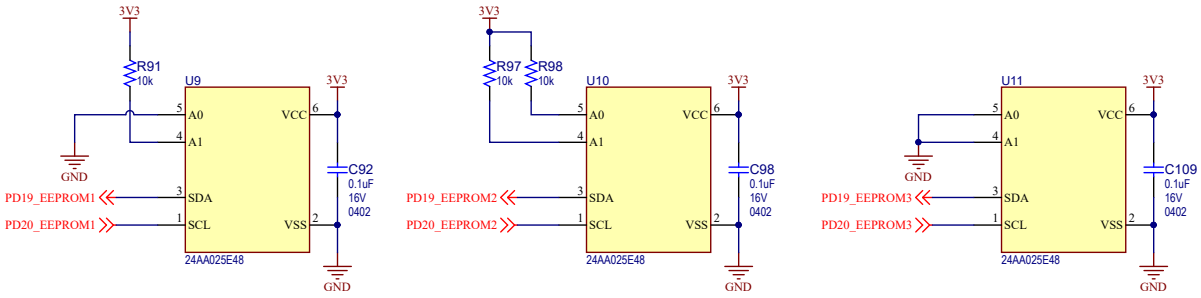
Address + Offset + R/W Bit	Component
Base (1010) + Offset (001) + R/W	EEPROM1(U9)
Base (1010) + Offset (011) + R/W	EEPROM2 (U10)
Base (1010) + Offset (000) + R/W	EEPROM3 (U11)

Table 3-9. EEPROM PIO Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PD19	TWD1	EEPROM TWI	TWI Data
PD20	TWCK1	EEPROM TWI	TWI Clock

The figure below illustrates the implementation of the three EEPROM memories.

Figure 3-17. EEPROM 24AA025E48



3.2.7 Secure Digital Multimedia Card (SDMMC) Interface

The SD (Secure Digital) Card is a non-volatile memory card format used as mass storage memory in mobile devices.

3.2.7.1 Secure Digital Multimedia (SDMMC) Controller

The SAMA5D2-ICP board has one Secure Digital Multimedia Card (SDMMC) interface that supports the MultiMedia Card (e.MMC) Specification V4.41, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. It is compliant with the SD Host Controller Standard V3.0 specification.

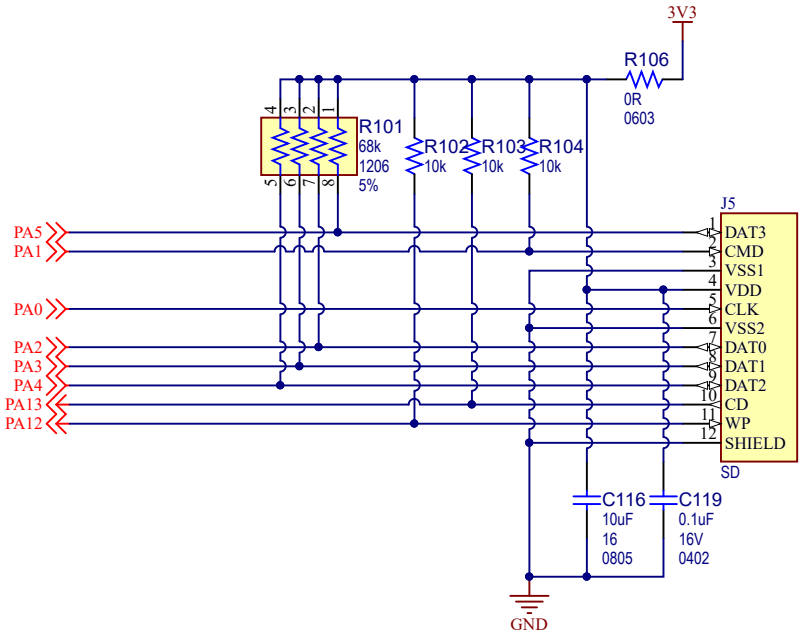
The SDMMC0 interface is connected to a standard SD card connector.

3.2.7.2 SD Card Socket

A standard MMC/SD card connector, connected to SDMMC0, is mounted on the bottom side of the board. The SDMMC0 communication is based on an 8-pin interface (clock, command, four data and power lines). It includes a card detection switch.

The figure below illustrates the implementation for the SDMMC0 interface.

Figure 3-18. SDMMC0 Interface and the Standard SD Socket



The table below describes the pin assignment of SD/MMC connector J5.

Table 3-10. Standard SD Socket J5 Pin Assignment Signal Description

Function	Pin	Shared	Signal Description
PA5	1	–	SDMMC0_DAT3_PA5
PA1	2	–	SDMMC0_CMD_PA1
GND	3	–	Ground
VCC	4	–	VDDSDHC (3v3)
PA0	5	–	SDMMC0_CK_PA0
PA13	6	–	SDMMC0_CD_PA13 (card detect)
PA2	7	–	SDMMC0_DAT0_PA2
PA3	8	–	SDMMC0_DAT1_PA3
PA4	9	–	SDMMC0_DAT2_PA4
PA13	10	–	SDMMC0_CD_PA13
PA12	11	–	SDMMC0_WP_PA12
GND	12	–	Ground

3.2.8 Communication Interfaces

The SAMA5D2-ICP embeds many communication interfaces and focuses on the following networking features:

- Dual port 10/100 Ethernet switch (Microchip KSZ8563)
- 1-Gbit Ethernet port (Microchip LAN7850)
- EtherCAT dual port (Microchip LAN9252)
- USB hub 4 ports (Microchip USB2534)
- USB device high-speed port

- Optional Wi-Fi/BT interface (Microchip WILC3000)
- Dual CAN interface (Microchip MCP2542)
- Serial links

3.2.8.1 Clock Generator

The clock sources of choice for the communication peripherals are MEMS oscillators.

The DSC1001 is a silicon MEMS-based CMOS oscillator offering excellent jitter and stability performance over a wide range of supply voltages and temperatures.

The DSC6000 family of MEMS oscillators combines industry-leading low power consumption with ultra-small packages.

Each communication interface uses its own source oscillator:

- One DSC1001DI5-025.0000 (25 MHz) oscillator used for the Ethernet dual switch
- One DSC1001DI5-025.0000 (25 MHz) oscillator used for the Ethernet HSIC interface
- One DSC1001DI5-025.0000 (25 MHz) oscillator used for the EtherCAT interface
- One DSC1001CI5-024.0000 (24 MHz) oscillator used for the USB hub chip
- One DSC6011JI1A-012.0000 oscillator used for the J-Link-OB (12 MHz)
- One DSC1001DL5-012.0000 oscillator used for the SAMA5D27 main clock (12 MHz)

3.2.8.2 10/100 Ethernet Switch

The KSZ8563 is a highly-integrated, IEEE 802.3 compliant networking device that incorporates a layer-2+ managed Ethernet switch, two 10Base-T/100Base-TX physical layer transceivers (PHYs) and associated MAC units, and one MAC port with a configurable RGMII/MII/RMII interface for direct connection to a host processor/ controller, another Ethernet switch, or an Ethernet PHY transceiver. KSZ8563 also implements IEEE 1588v2 Precision Timing Protocol one-step operation.

Additionally, for monitoring and control purposes, an LED functionality is carried on the RJ45 connectors to indicate activity, link, and speed status information.

For more information about the Ethernet controller device, refer to the KSZ8563 controller manufacturer's data sheet.

3.2.8.2.1 External Chip Reset

When the Reset push button switch is pressed, the device places all pins into their default state. An additional PIO resets the KSZ8563.

The figure below illustrates the implementation of the Ethernet switch interface.

Figure 3-19. Ethernet Switch

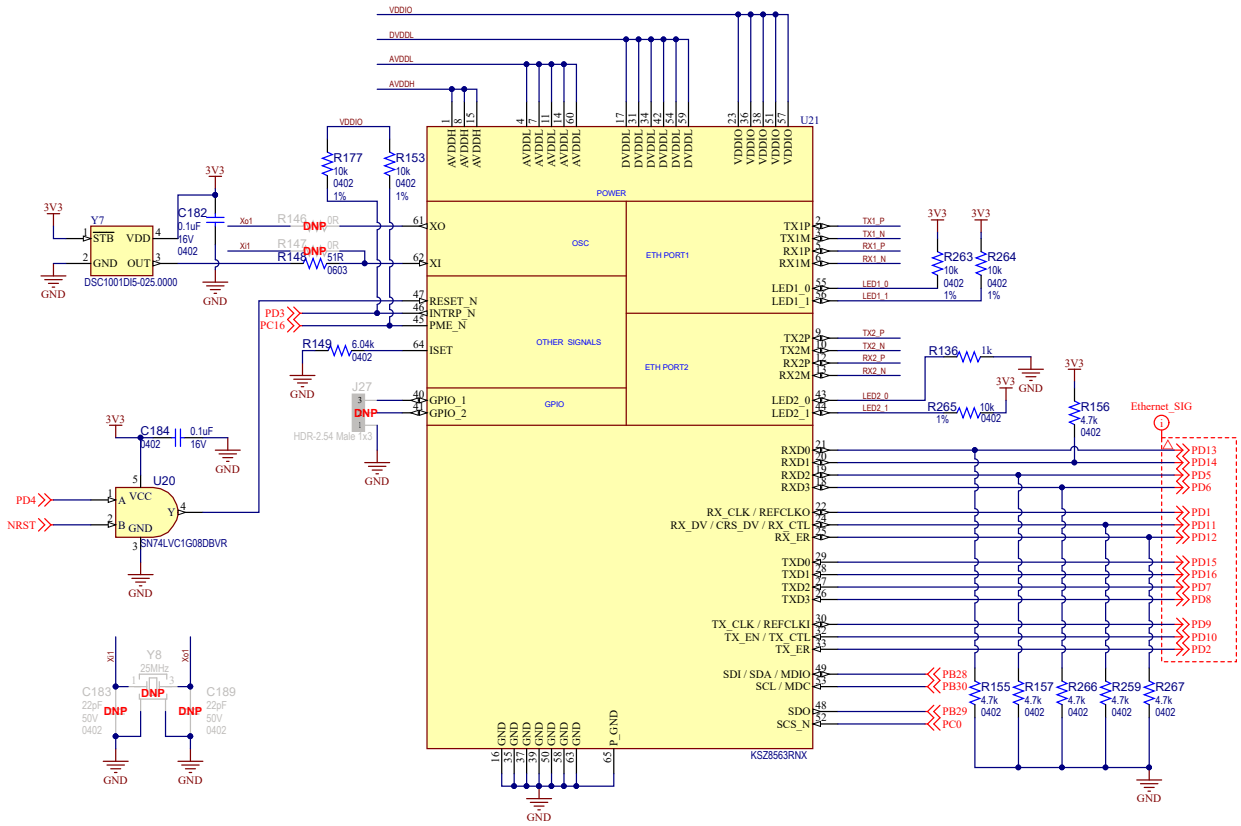


Table 3-11. 10/100 Mb/s Ethernet Switch Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PD9	ETH_GTXCK	–	Transmit clock
PD10	ETH_GTXEN	–	Transmit enable
PD2	ETH_GTXER	–	Transmit error
PD15	ETH_GTX0	–	Transmit data 0
PD16	ETH_GTX1	–	Transmit data 1
PD7	ETH_GTX2	–	Transmit data 2
PD8	ETH_GTX3	–	Transmit data 3
PD1	ETH_GRXCK	–	Receive clock
PD11	ETH_GRXDV	–	Receive data valid
PD12	ETH_GRXER	–	Receive error
PD13	ETH_GRX0	–	Receive data 0
PD14	ETH_GRX1	–	Receive data 1
PD5	ETH_GRX2	–	Receive data 2
PD6	ETH_GRX3	–	Receive data 3
PB30	ETH_GMDC	–	Management data clock

.....continued			
PIO	**Mnemonic**	**Shared**	**Signal Description**
PB28	ETH_GMDIO	–	Management data in/out
PD3	ETH_GTX_INT	–	Interrupt (open drain)
PD4	ETH_RST	–	PIO reset
PC16	ETH_PME_N	–	Power management event

Figure 3-20. Ethernet Switch Connectors J11 and J12

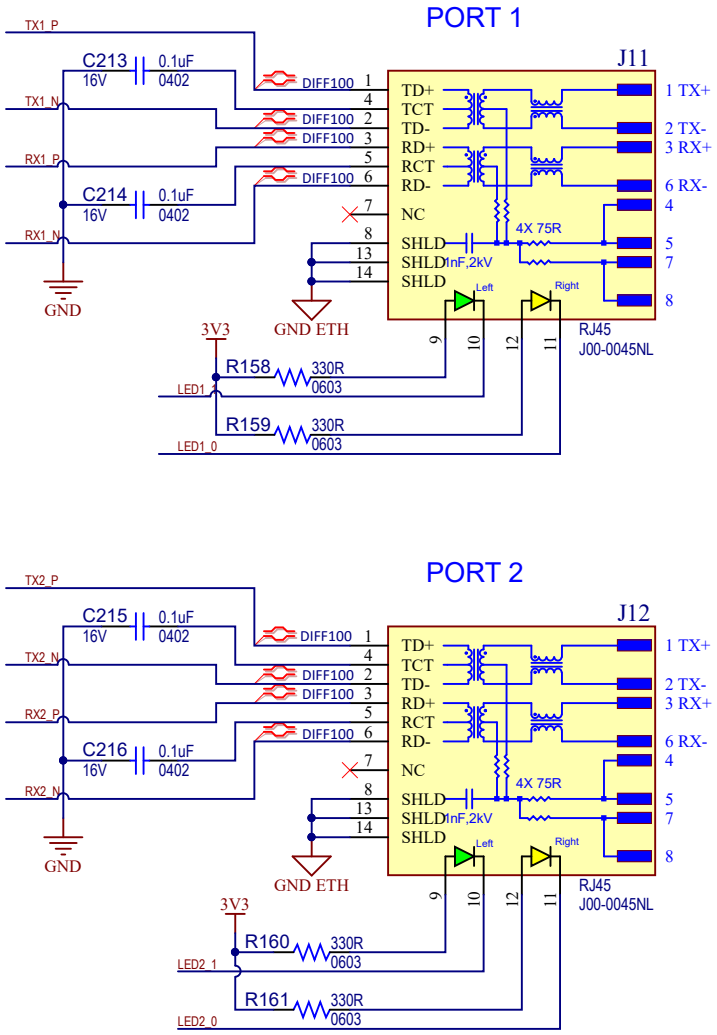
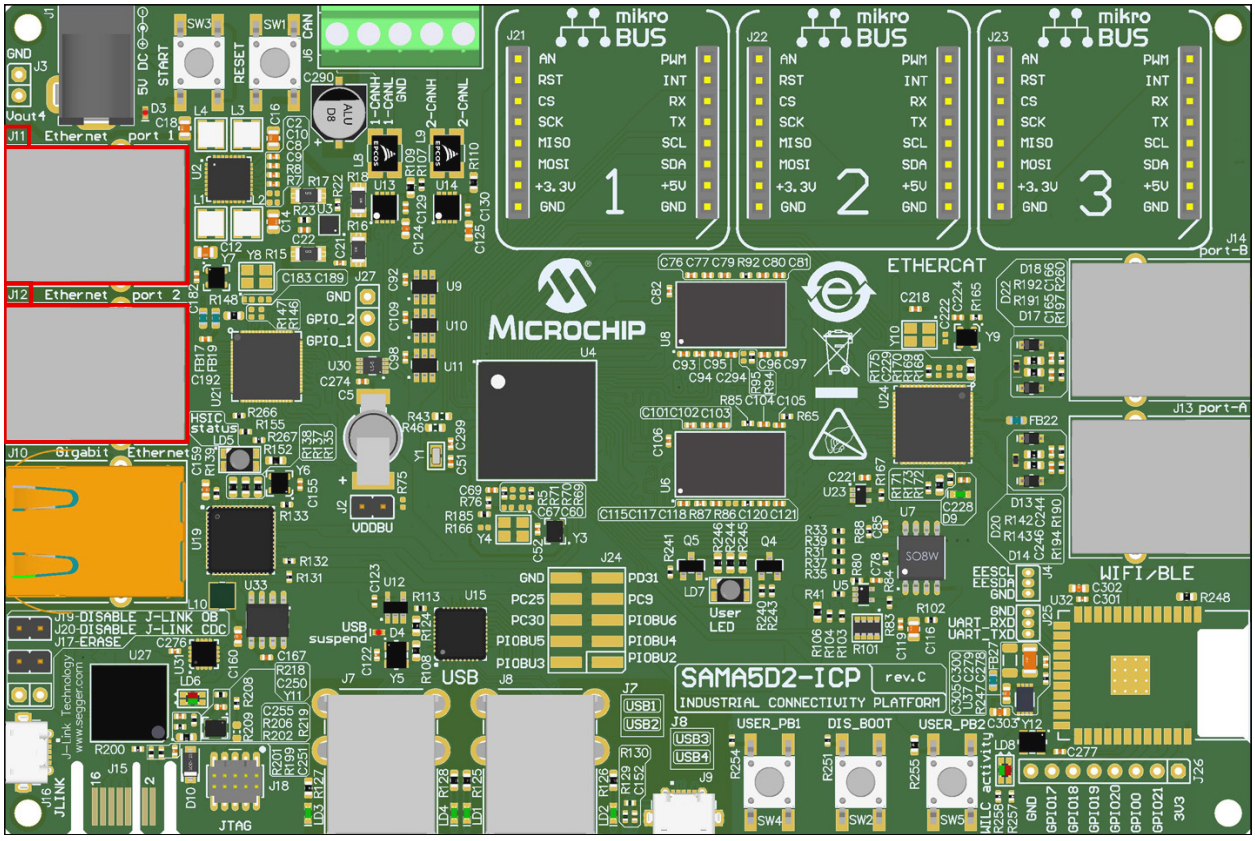


Figure 3-21. Ethernet Switch RJ45 Connectors J11 and J12 Location



The table below describes the pin assignment of Ethernet connectors J11 and J12.

Table 3-12. Ethernet Switch RJ45 Connectors J11 and J12 Pin Assignment Signal Descriptions

Pin No	Mnemonic	Signal Description
1	TX+	Transmit
2	TX-	Transmit
3	RX+	Receive
4	Decoupling capacitor	–
5	Decoupling capacitor	–
6	RX-	Receive
7	NC	–
8	EARTH / GND	Common ground
9	ACT LED	LED activity
10	ACT LED	LED activity
11	LINK LED	LED link connection
12	LINK LED	LED link connection
13	EARTH / GND	Common ground
14	EARTH / GND	Common ground

3.2.8.3 1-Gbit Ethernet HSIC

The Microchip LAN7850 is a USB 2.0 Gigabit Ethernet Controller with HSIC interface. The LAN7850 supports 10Base/100Base-TC/1000Base-T Ethernet (full duplex support), is configured for operation through internal default settings and supports custom configuration through the external 4-Kbit EEPROM device or interval one-time programmable (OTP) memory.

The LAN7850 contains an integrated 10/100/1000 Ethernet MAC and PHY, Filtering Engine, USB PHY (with HSIC interface), high-speed USB 2.0 device controller, TAP controller, EEPROM controller, and a FIFO controller with internal packet buffering.

The Ethernet controller supports auto-negotiation, auto-polarity correction and HP Auto-MDIX, and is compliant with the IEEE 802.3, IEEE 802.3u, IEEE 802.3ab, and 802.3az (Energy Efficient Ethernet) standards. ARP and NS offload are also supported.

An internal EEPROM controller exists to load various USB and Ethernet configuration parameters. For EEPROM-less applications, the LAN7850 provides 1 Kbyte of OTP memory that can be used to preload this same configuration data before enumeration.

3.2.8.3.1 External EEPROM / Internal OTP

At power-up, the LAN7850 searches for an external EEPROM. If an external EEPROM (93AA66A) is detected, the LAN7850 configuration is loaded from it. If no EEPROM is found, the device checks the OTP. If there is no OTP, the device uses default CSR settings. The EEPROM stores the default values for the USB descriptors and the MAC address.

3.2.8.3.2 Enable Link Status LEDs

When configured with the default internal register settings, the Ethernet link status LEDs are not enabled. To enable those LEDs, enable the EEPROM.

Each LED is detailed below:

- Link1000: yellow LED (RJ45 J10) is ON with a valid 1000 Mbps link.
- Link100: green LED (RJ45 J10) is ON with a valid 100 Mbps link.
- Link/Act: RGB LED (LD5) is ON and green with network activity.
- Duplex/Collision: RGB LED (LD5) is ON and red in Full Duplex mode. LED is OFF in Half-Duplex mode. LED blinks red during collision.
- Suspend: RGB LED (LD5) is ON and blue in Suspend mode.

3.2.8.3.3 External Chip Reset

When the Reset push button switch is pressed, the device places all pins into their default state and the entire contents of the EEPROM or OTP are reloaded. An additional PIO (PC2) allows the LAN7850 to be reset by software.

The figure below illustrates the implementation of the Ethernet HSIC interface.

Figure 3-22. Ethernet HSIC Interface

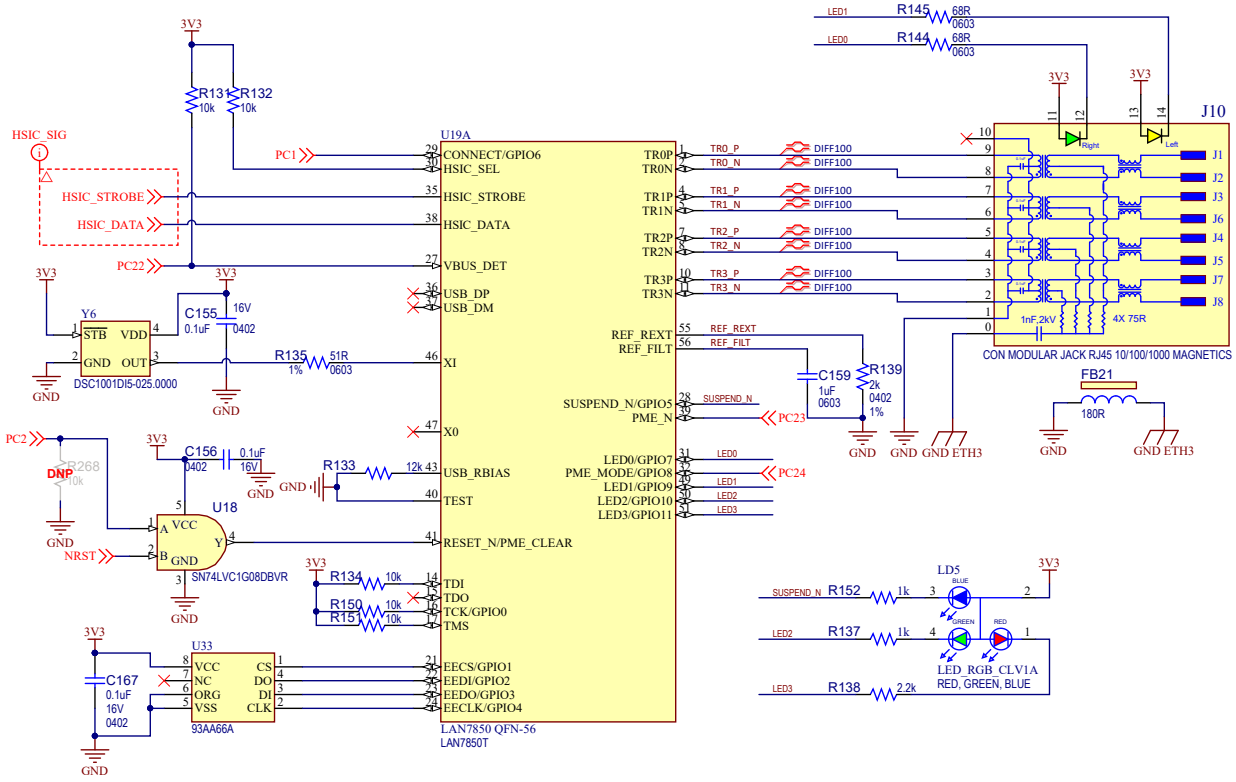
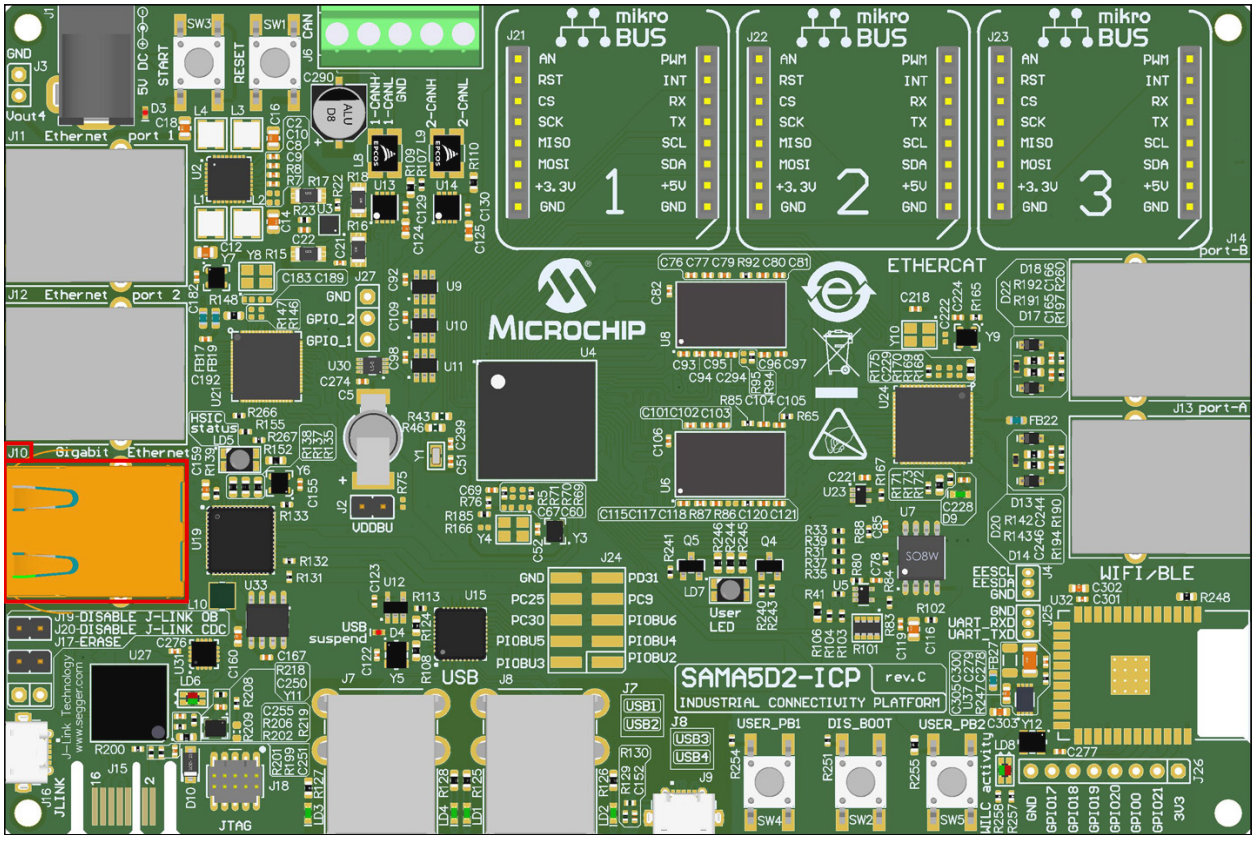


Table 3-13. Ethernet HSIC Signal Description

PIO	Mnemonic	Shared	Signal Description
–	HSIC_STROBE	–	Bidirectional data strobe signal
–	HSIC_DATA	–	Bidirectional Double Data Rate (DDR) data signal that is synchronous to the strobe signal
PC22	VBUS_DETECT	–	Sets the state of the upstream bus power
PC23	PME_N	–	Indicates Power Management Event when the PME mode of operation is in effect
PC24	PME_MODE	–	Serves as the Power Management Event mode selection input when the PME mode of operation is in effect

Figure 3-23. Ethernet HSIC RJ45 Connector J10 Location



3.2.8.4 EtherCAT

The LAN9252 is a 2-port EtherCAT Slave Controller (ESC) with dual integrated Ethernet PHYs. Each PHY contains a full-duplex transceiver and supports 100 Mbps (100Base-TX) operation.

PORT0 of LAN9252 is connected to the host processor through the PIOs in HBI Indexed mode. The HBI supports 8/16-bit operation with Big, Little, and Mixed Endian operations. Two process data RAM FIFOs interface the HBI to the EtherCAT slave controller and facilitate the transferring of process data information between the host CPU and the EtherCAT slave. A configurable host interrupt pin allows the device to inform the host CPU of any internal interrupts.

Several PIOs are shared with the Wi-Fi/BT WILC3000 interface. When the WILC3000 interface is enabled, the LAN9252 (NCS1 PC6) is disabled via the WILC3K_CE PC15 signal.

The LAN9252 is connected to two RJ45 Ethernet jacks with integrated magnetics for 100Base-TX connectivity. Additionally, for monitoring and control purposes, LED functionality is carried on the RJ45 connectors to indicate activity and link status information.

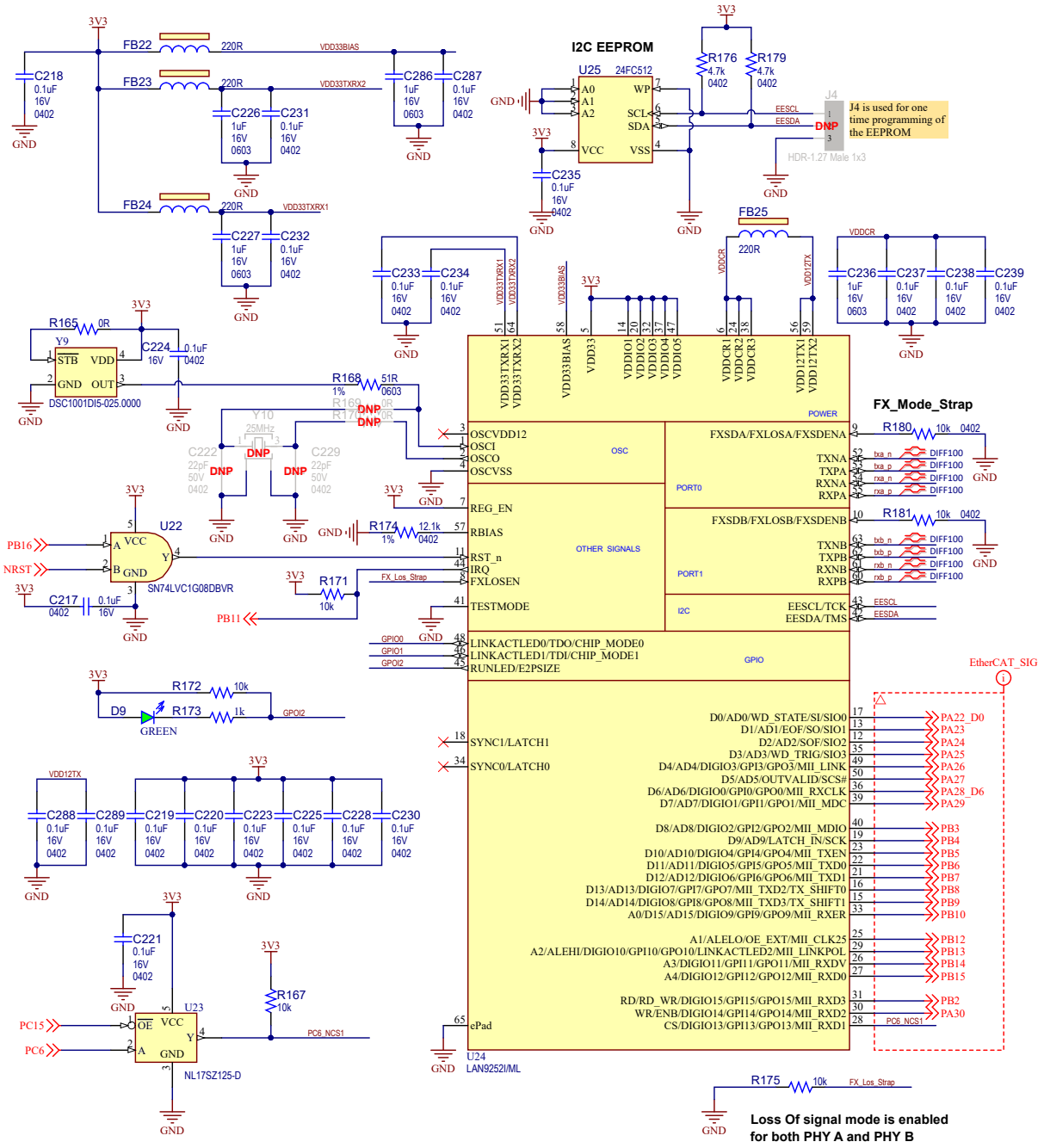
For more information about the Ethernet controller device, refer to the Microchip LAN9252 controller data sheet.

3.2.8.4.1 External Chip Reset

When the Reset push button switch is pressed, the device places all pins into their default state. An additional PIO (PB16) allows the LAN9252 to be reset by software.

The figure below illustrates the implementation of the EtherCAT interface.

Figure 3-24. EtherCAT Interface



The table below shows the signal assignment on the HBI interface between SAMA5D27 and LAN9252.

Table 3-14. EBI Signal Description

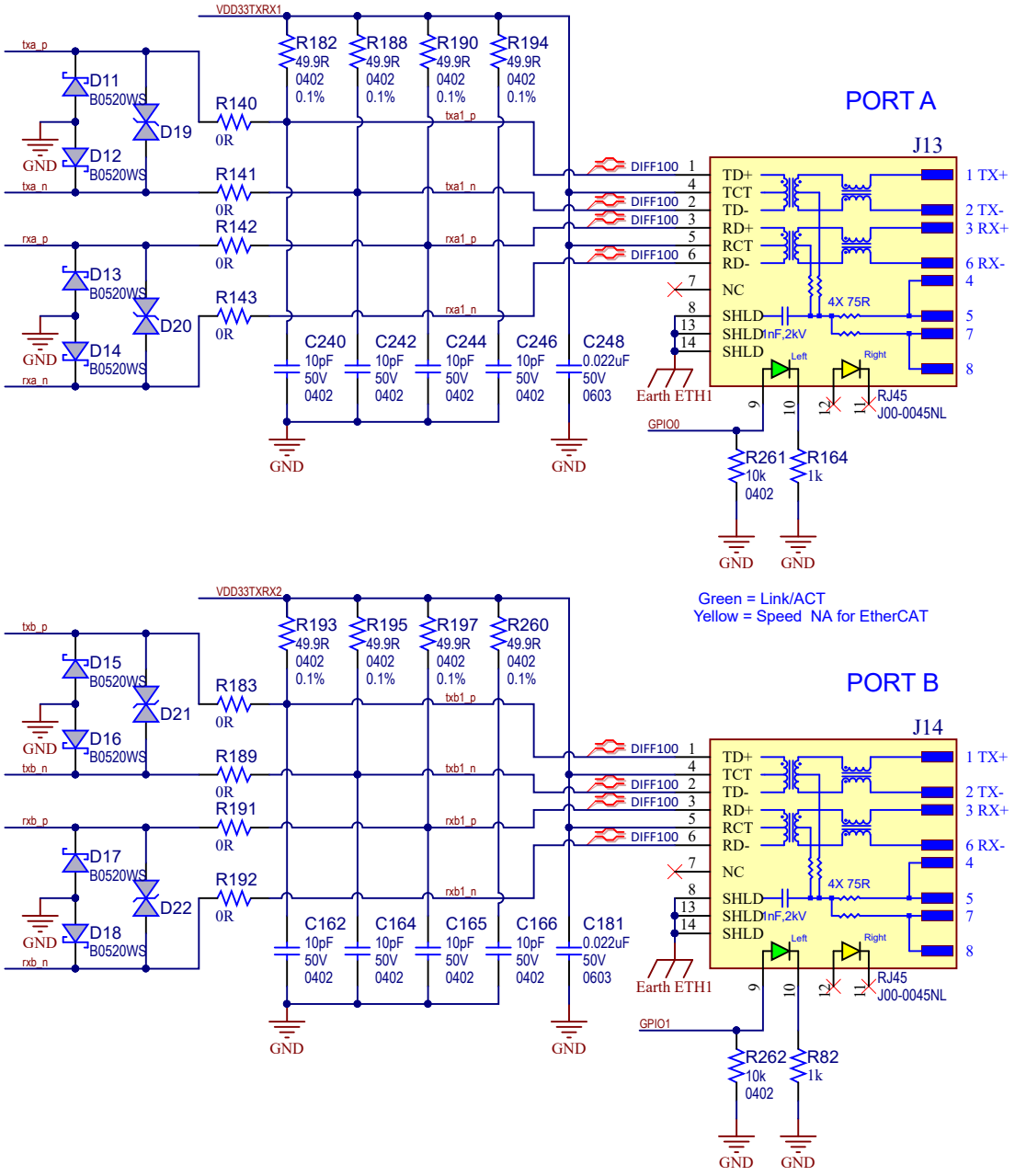
PIO	Mnemonic	Shared	Signal Description
PA22	D0	WILC3000	Data
PA23	D1	–	Data
PA24	D2	–	Data

.....continued

PIO	Mnemonic	Shared	Signal Description
PA25	D3	–	Data
PA26	D4	–	Data
PA27	D5	–	Data
PA28	D6	WILC3000	Data
PA29	D7	–	Data
PB3	D8	–	Data
PB4	D9	–	Data
PB5	D10	–	Data
PB6	D11	–	Data
PB7	D12	–	Data
PB8	D13	–	Data
PB9	D14	–	Data
PB10	A0/D15	–	Data
PB12	A1	–	Address
PB13	A2	–	Address
PB14	A3	–	Address
PB15	A4	–	Address
PB2	RD	–	Read
PA30	WR	–	Write
PC6	CS	–	Chip select
PB11	IRQ	–	Interrupt
PB16	RESET	–	Reset chip

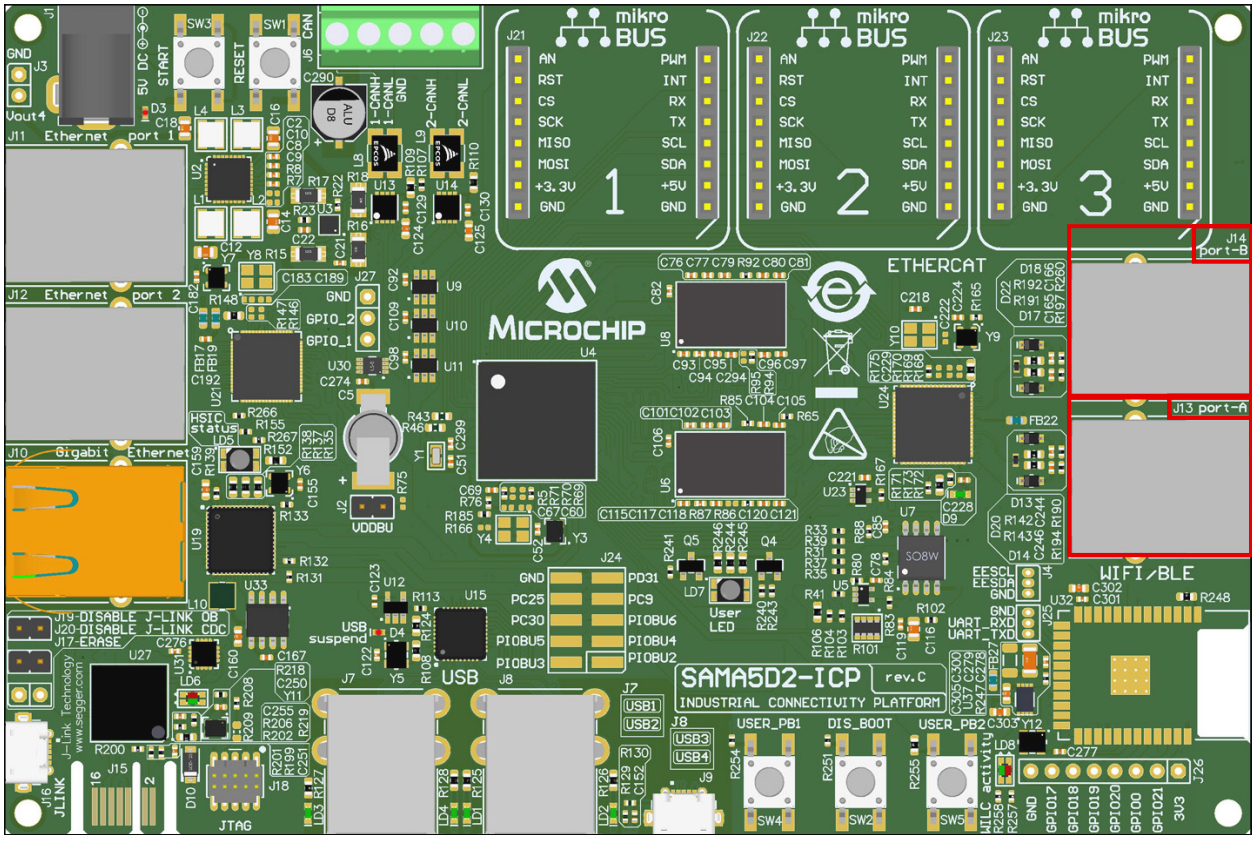
The figure below depicts the connection between LAN9252 and the two EtherCAT connectors.

Figure 3-25. EtherCAT Connectors J13 and J14



The position of the two connectors is shown in the picture below

Figure 3-26. RJ45 Connectors J13 and J14 Location



3.2.8.5 USB Host/Device Ports

The USB (Universal Serial Bus) is a hot-pluggable general-purpose high-speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 Specification defines data transfer rates as high as 480 Mbps (also known as High-speed USB). A USB host bus connector uses four pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin.

The SAMA5D2-ICP board features three USB communication ports, designated USB-A to USB-C:

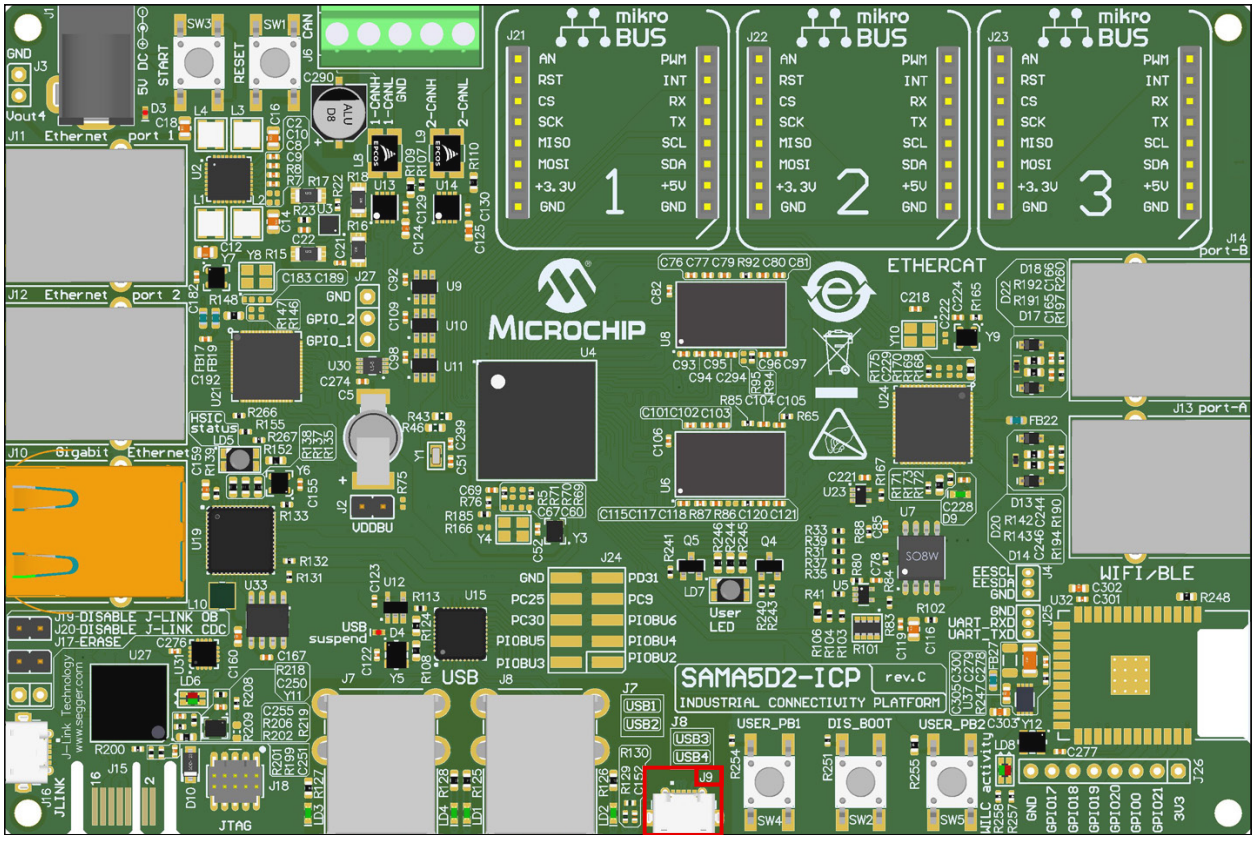
- USB-A interface connected to a standard Micro-AB connector with a VBUS detection function
- USB-B (host port B high- and full-speed interface) connected to a USB2534 hub, with four ports connected to two stacked USB type A connectors
- USB-C high-speed host port with an HSIC interface, connected to Ethernet Gigabit interface LAN7850

USB IO lines are not controlled by any PIO controller. The embedded USB high-speed physical transceivers are controlled by the USB host controller.

3.2.8.6 USB-A Interface

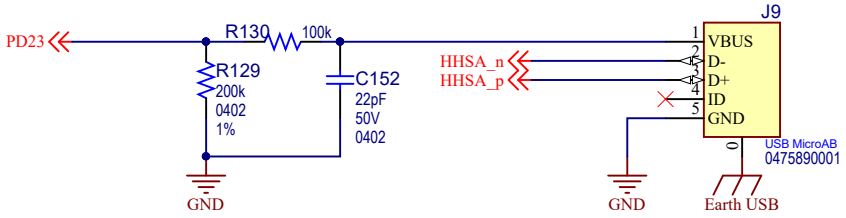
The USB Host Port controller is fully compliant with the Enhanced HCI specification. It handles the Open HCI (Open Host Controller Interface) protocol as well as the Enhanced HCI (Enhanced Host Controller Interface) protocol. The USB Host Port User interface can be found in the Enhanced HCI Rev 1.0 Specification.

Figure 3-27. Micro-AB Type USB Connector J9 Location



The figure below shows the USB implementation on the USB-A port terminated on a Micro-AB type USB connector.

Figure 3-28. USB-A and VBUS Detection



The table below describes the pin assignment of the USB-B downstream connectors.

Table 3-15. USB-A Connector Signal Descriptions

Pin No	Mnemonic	Signal Description
1	VBUS	5V power
2	DM	Data minus
3	DP	Data plus
4	NC	Not connected
5	GND	Common ground

3.2.8.6.1 USB-A VBUS Detection

The USB-A port (J9) features a VBUS (+5V) insert detection function through ladder-type resistors R129 and R130.

Table 3-16. USB-A PIO Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PD23	USBA_VBUS_5V	–	VBUS insertion detection

3.2.8.7 USB-B Hub Interface

The USB2534 is a low-power, full-featured, OEM configurable, high-speed USB 2.0 compliant hub with four downstream ports

All downstream USB 2.0 ports include a high current port power controller with LED indicator. Downstream port power is distributed by four independent power switches MIC2026 at up to 500 mA per port.

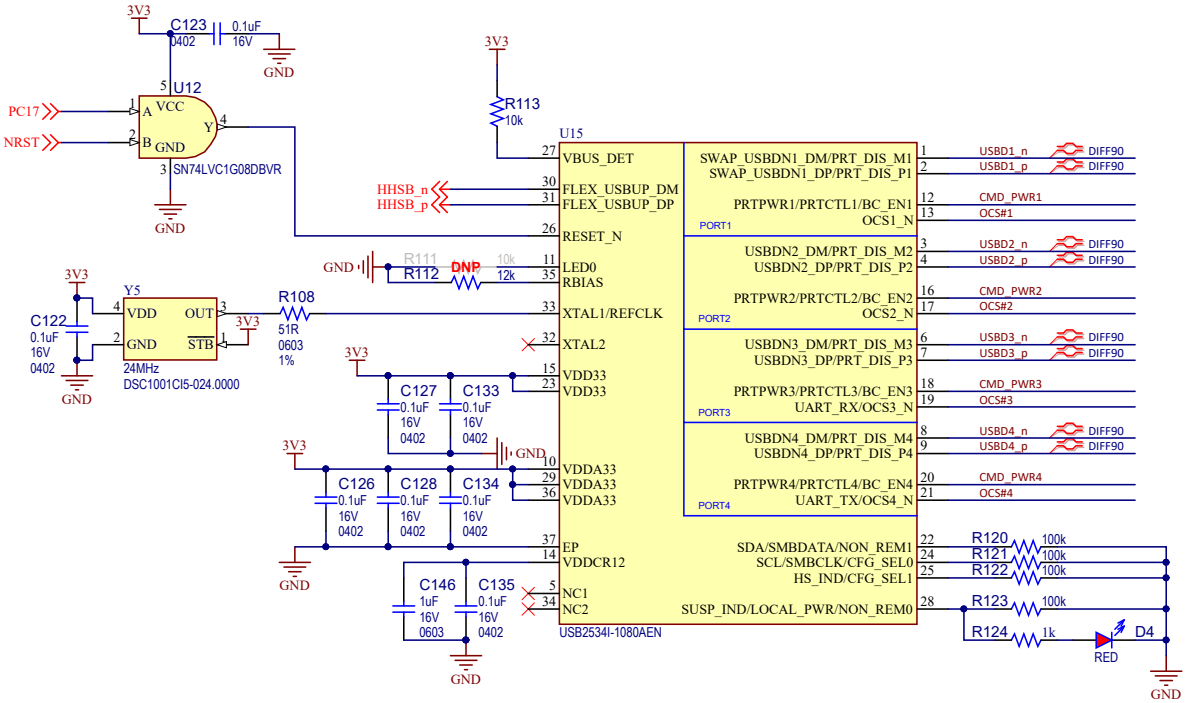
Note: Make sure the connected devices' current requirement does not exceed the total current available from 5V DC (500 mA per port).

3.2.8.7.1 External Chip Reset

When the Reset push button switch is pressed, the device places all pins into their default state. An additional PIO (PC17) resets the USB2534.

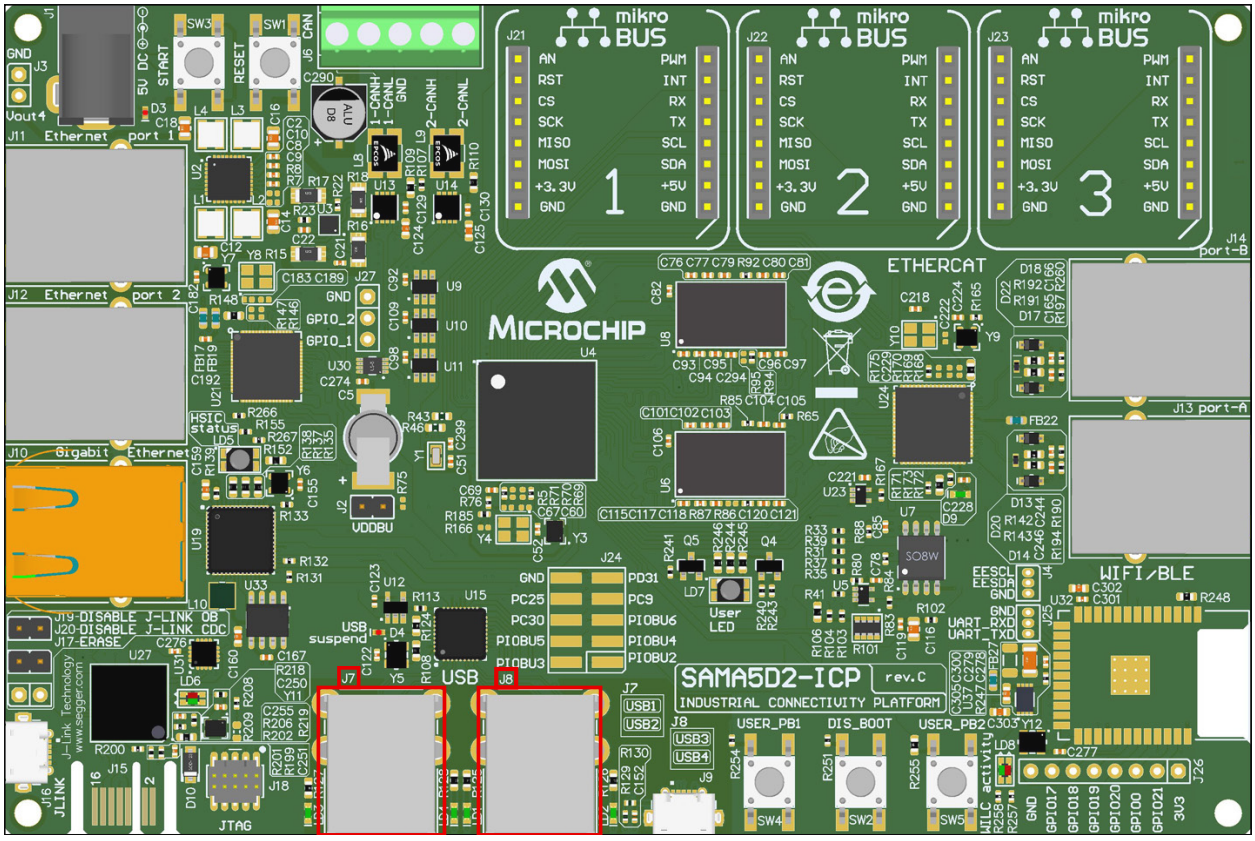
The figure below shows the USB hub implementation.

Figure 3-29. USB Hub Interface



The picture below shows the location of the two double stacked connectors, J7 and J8.

Figure 3-30. Connectors J7 and J8 Location



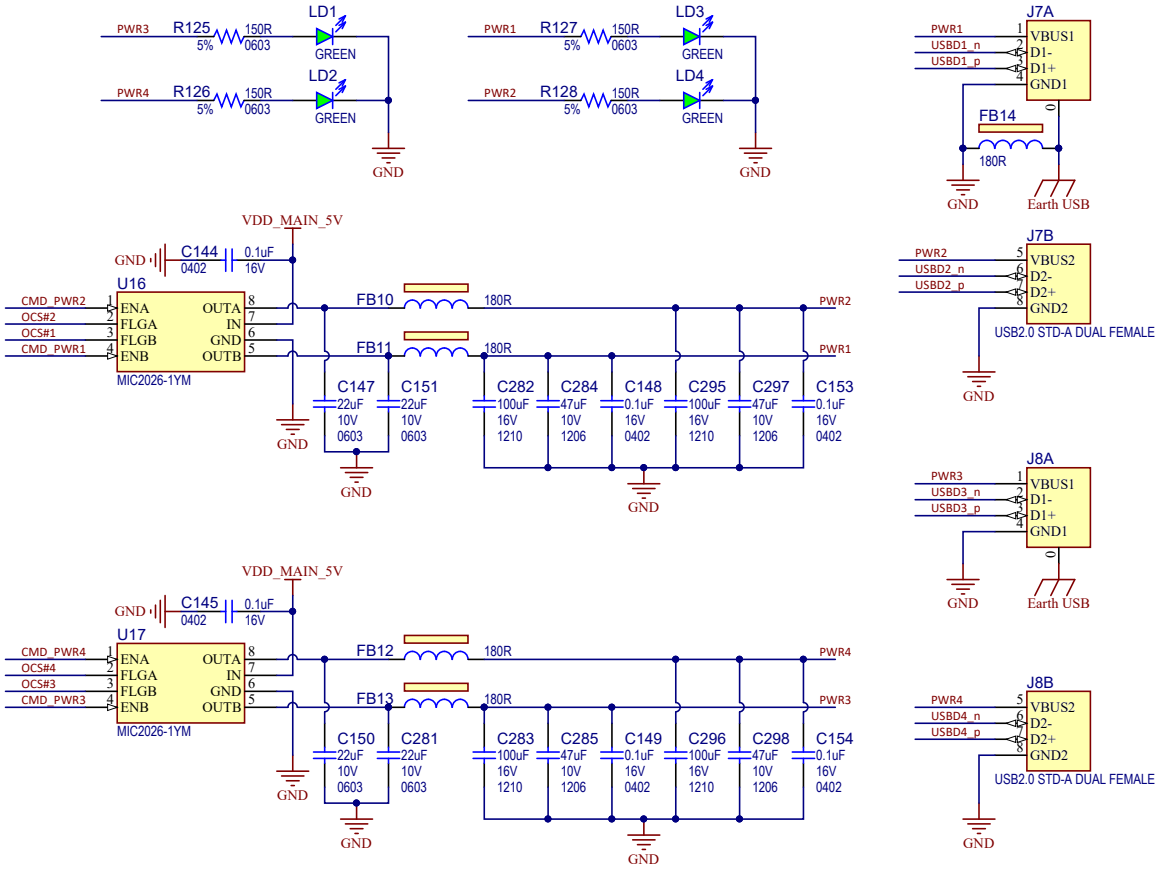
3.2.8.7.2 Port Power LEDs

LD1 to LD4 indicate when 5V DC port power is available to the associated downstream USB port(s).

3.2.8.7.3 Connectors

The USB2534 interface provides four connectors of type A for downstream ports. For more details on the pinout of these connectors, refer to the USB2534 schematics.

Figure 3-31. USB Hub Power and Connections



3.2.8.8 Wi-Fi/BT

The SAMA5D2-ICP is ready to host either a ATWILC3000-MR110CA or a ATWILC3000-MR110UA WiFi/BT module. These modules are designed to achieve reliable and power-efficient physical layer communication as specified by IEEE 802.11 b/g/n in Single Stream mode with 20 MHz bandwidth.

The main difference between these modules is that ATWILC3000-MR110CA features a chip antenna, while ATWILC3000-MR110UA hosts a u.FL connector which can connect to any WiFi/BT external antenna that has a u.FL mating connector.

Advanced algorithms have been employed to achieve maximum throughput in a real-world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as automatic gain control.

These modules are available in a fully certified, 22.428 x 17.732 mm, 36-pin module package. For more details on the module, refer to the product web page.

The figure below illustrates the implementation of the WILC3000 Wi-Fi/BT module. Note that it is not populated, thus the customer may choose the most suitable option. Application note AN_3227, *How to Manually Solder the ATWILC3000 Module on an MPU Board*, offers guidance on how to add the ATWILC3000 module to the board.

Figure 3-32. Wi-Fi/BT Module

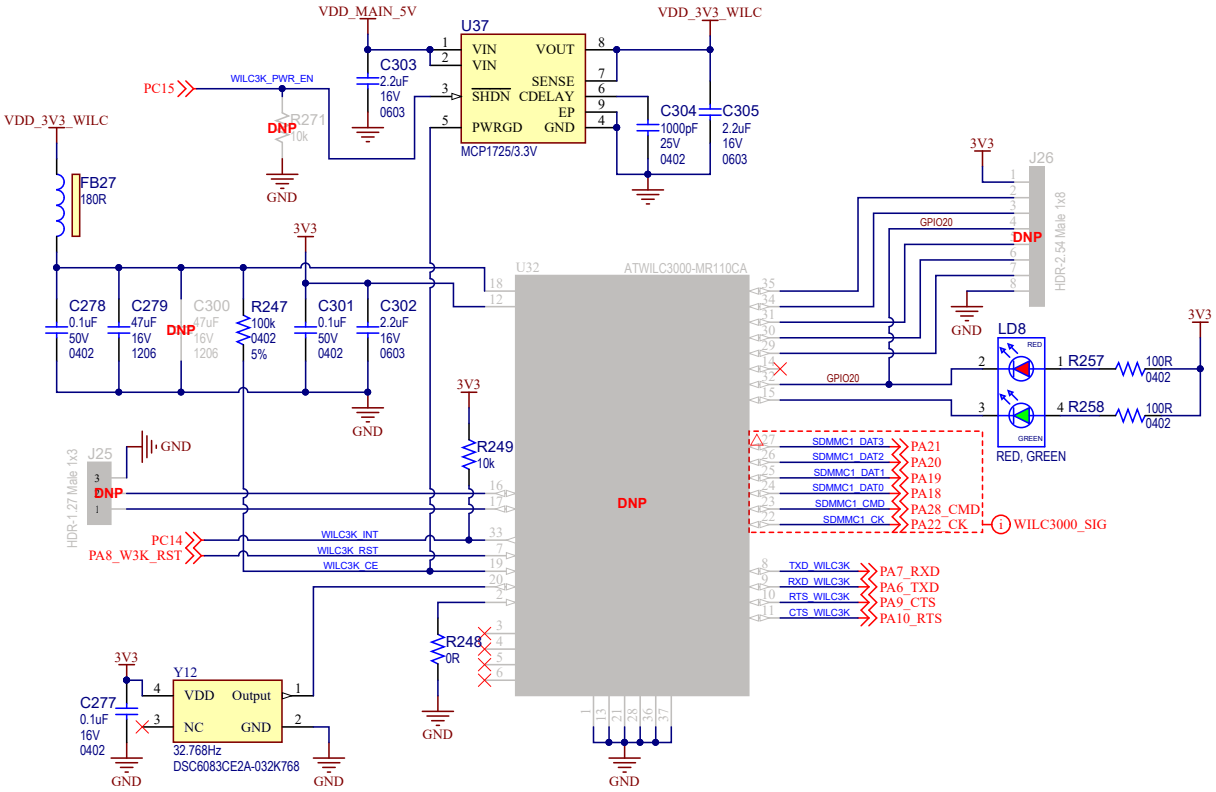
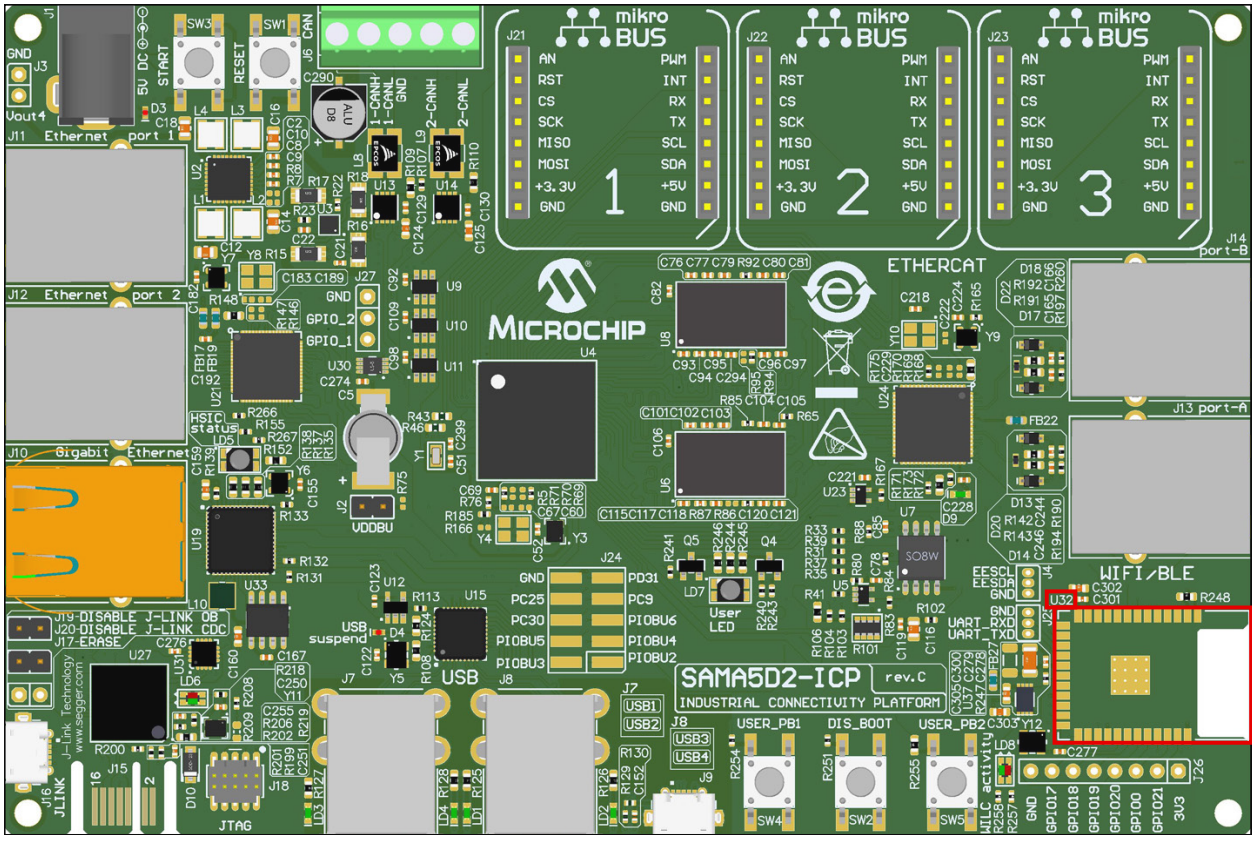


Table 3-17. Wi-Fi/BT Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PA18	SDIO_DATA0	–	SDIO data
PA19	SDIO_DATA1	–	SDIO data
PA20	SDIO_DATA2	–	SDIO data
PA21	SDIO_DATA3	–	SDIO data
PA28	SDIO_CMD	EtherCAT	SDIO command
PA22	SDIO_CLK	EtherCAT	SDIO clock
PA6	BT_TXD	QSPI	Bluetooth serial TX
PA7	BT_RXD	QSPI	Bluetooth serial RX
PA10	BT_RTS	QSPI	Bluetooth serial RTS
PA9	BT_CTS	QSPI	Bluetooth serial CTS
PA8	RESET_N	–	Module reset
PC14	IRQ_N	–	Interrupt
PC15	CHIP_EN	–	Chip enable

Figure 3-33. WILC3000 Location



3.2.8.9 CAN Interface

The dual Controller Area Network (CAN) interface is equipped with two MCP2542 transceivers. The MCP2542 is a high-speed CAN transceiver that provides the interface between the CAN protocol controller and the physical two-wire bus. Input/output signals from the transceiver are connected to a screw connector (J6).

3.2.8.9.1 Normal Mode

A low level on the STBY pin (PB25) together with a high level on pin TXD selects the Normal mode. In this mode, the transceiver is able to transmit and receive data via the bus lines.

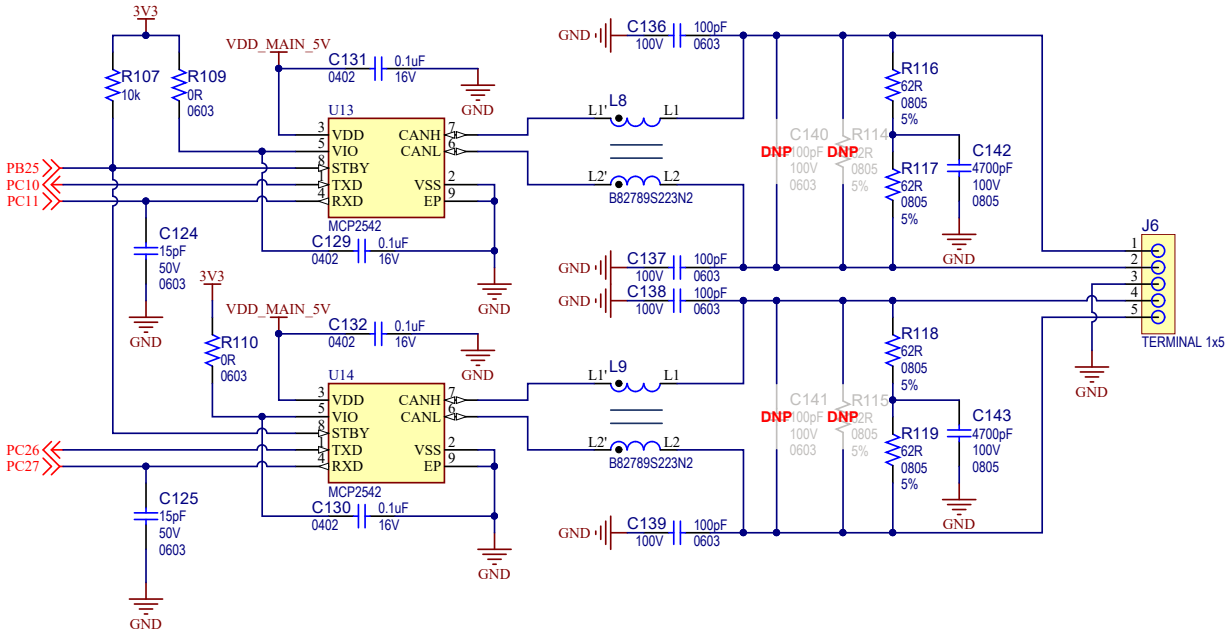
3.2.8.9.2 Standby Mode

A high level on the STBY pin (PB25) selects Standby mode. In this mode, the transceiver is not able to transmit or receive data via the bus lines. The transmitter and the high-speed comparator are switched off to reduce the power current consumption.

For more details on the module, refer to the product web page.

The figure below illustrates the implementation of the dual CAN interface.

Figure 3-34. Dual CAN Interface



The following tables describe the signals related to the CAN interface.

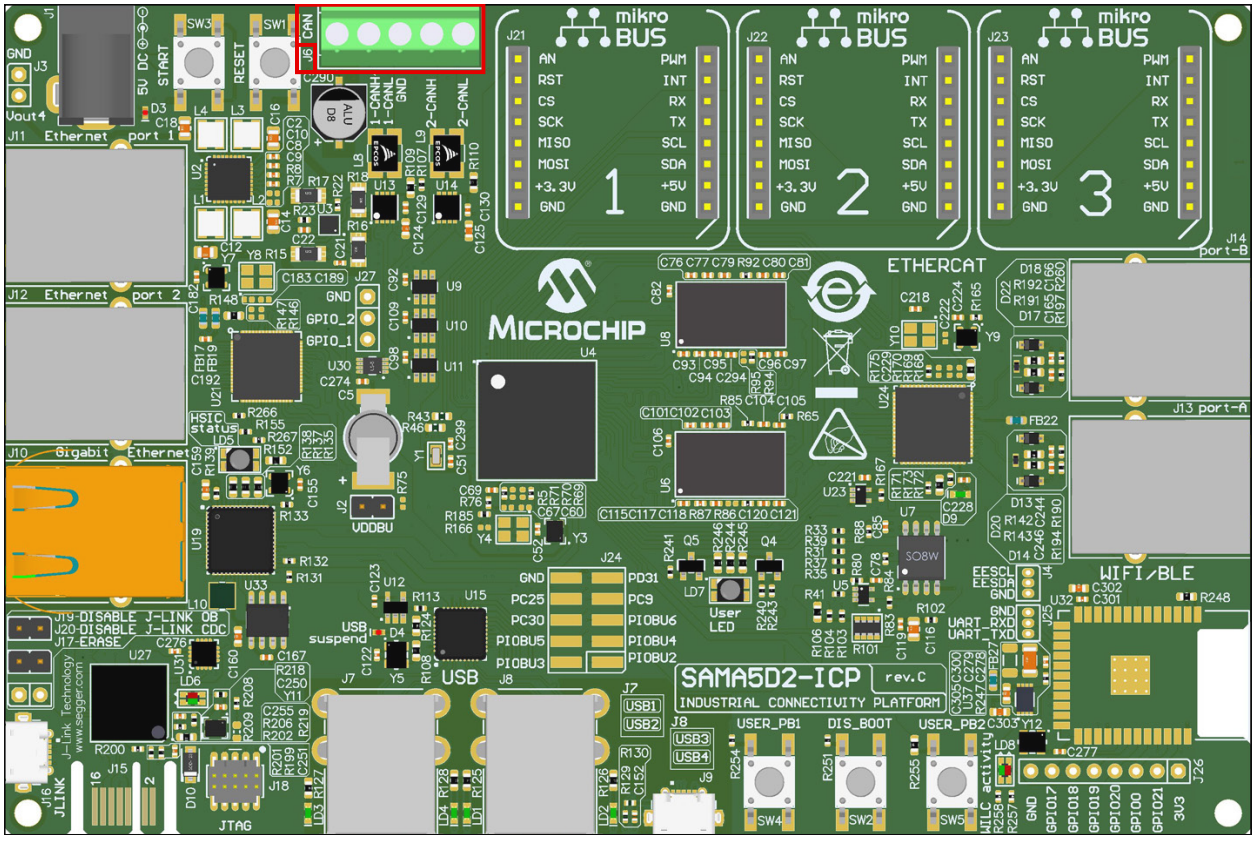
Table 3-18. CAN Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PB25	CAN_STBY	–	Dual CAN standby
PC10	CANTX0	–	CAN transmit port 0
PC11	CANRX0	–	CAN receive port 0
PC26	CANTX1	–	CAN transmit port 1
PC27	CANRX1	–	CAN receive port 1

Table 3-19. CAN Connector J6 Signal Description

Pin No	Mnemonic	Signal Description
1	CAN0H	Differential positive port 0
2	CAN0L	Differential negative port 0
3	GND	Common ground
4	CAN1H	Differential positive port 1
5	CAN1L	Differential negative port 1

Figure 3-35. CAN Connector J6 Location



3.3 External Interfaces

3.3.1 On-Board LEDs

The board features signaling LEDs for the USB Hub, the Ethernet HSIC, the on-board J-Link, the EtherCAT interface and the WILC3000 module. It also provides an RGB LED that is connected directly to the GPIOs of the MPU.

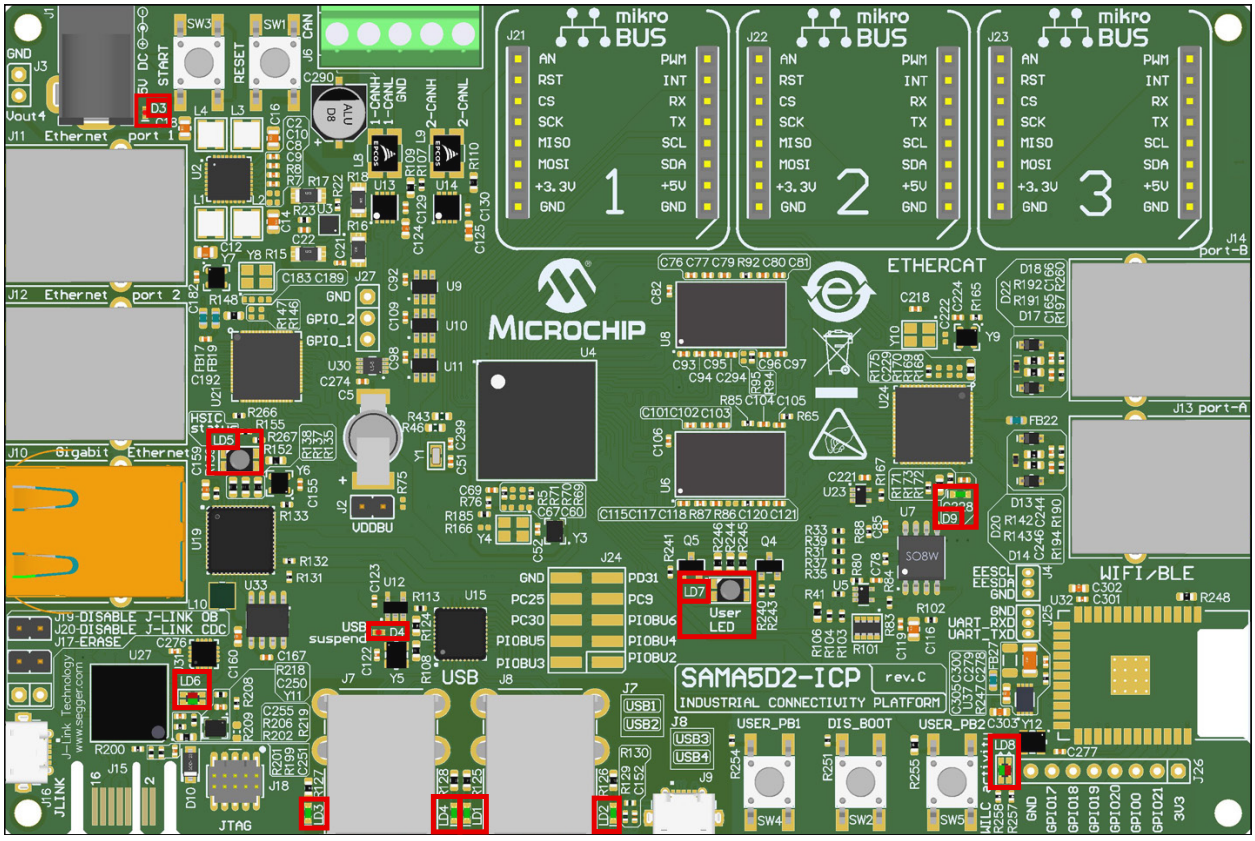
Table 3-20. On-Board LED Signal Descriptions

LED	STATE	Signal Description
D3	Red	Main power +5V
D4	Red	Hub USB2534 “SUSPEND”
LD1	Green	Power enabled on USB3
LD2	Green	Power enabled on USB4
LD3	Green	Power enabled on USB1
LD4	Green	Power enabled on USB2
LD5	Red	Ethernet HISC LAN7850 “DUPLEX/COLLISION”
LD5	Green	Ethernet HISC LAN7850 “LINK/ACTIVITY”
LD5	Blue	Ethernet HISC LAN7850 “SUSPEND”
LD6	Red	J-Link-OB/J-Link-CDC

.....continued		
LED	**STATE**	**Signal Description**
LD6	Green	J-Link-OB/J-Link-CDC
LD7	Red	User
LD7	Green	User
LD7	Blue	User
LD8	Red	WILC3000 status
LD8	Green	WILC3000 status
D9	Green	EtherCAT LAN9252 “RUNLED”

The picture below shows the positions of LEDs described above

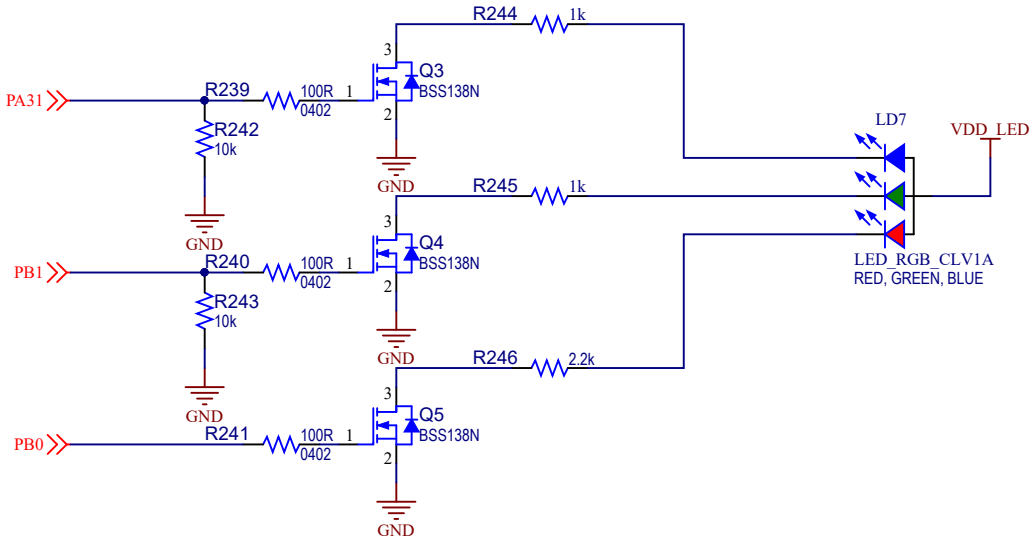
Figure 3-36. On-Board LEDs



3.3.1.1 RGB LED

The SAMA5D2-ICP board features one RGB LED. The three LED cathodes are controlled via GPIO PWM pins.

Figure 3-37. RGB LED Connection to the MPU



The connection of the LEDs to the MPU and the function of each GPIO is depicted in the table below.

Table 3-21. RGB LED PIOs

Signal	PIO	Function
LED_RED	PB0	PWMH1
LED_GREEN	PB1	PWML1
LED_BLUE	PA31	PWML0

3.4 Debugging Capability

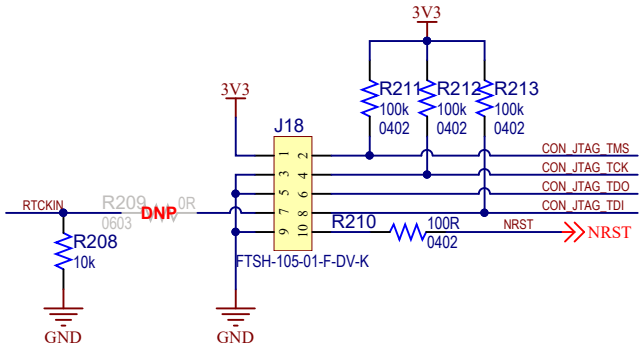
The SAMA5D2-ICP includes two main debugging interfaces to provide debug level access to the SAMA5D27:

- One UART through the USB J-Link-CDC
- Two JTAG interfaces, one connected directly to the MPU using connector J18 and one through the J-Link-OB interface USB port J16

3.4.1 Debug JTAG

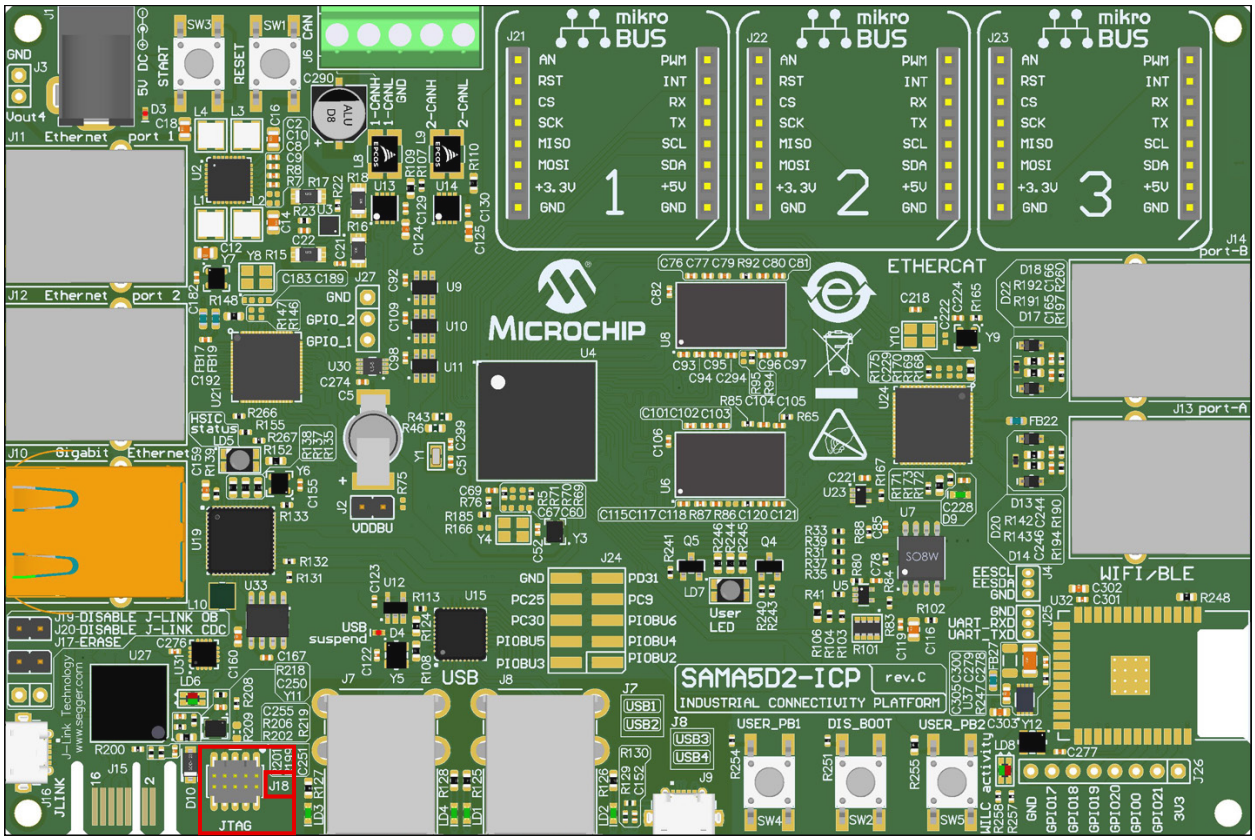
A 10-pin JTAG header (J18) is provided on the SAMA5D2-ICP board to facilitate software development and debug by using various JTAG emulators. The interface signals have a voltage level of 3.3V.

Figure 3-38. JTAG Interface



The location of the JTAG connector is shown in the picture below.

Figure 3-39. JTAG Connector J18 Location



The table below describes the pin assignment of JTAG connector J18.

Table 3-22. JTAG/ICE Connector J18 Pin Assignment Signal Descriptions

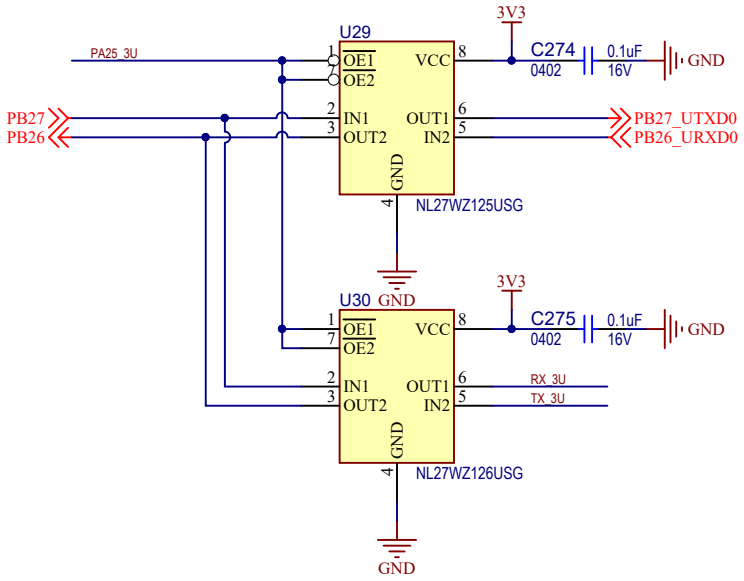
Pin No	Mnemonic	Signal Description
1	VTref. 3.3V power	Target reference voltage (main 3.3V)
2	TMS (Test Mode Select)	JTAG mode set input into target CPU
3	GND	Common ground

.....continued		
Pin No	**Mnemonic**	**Signal Description**
4	TCK Test clock - Output timing signal, for synchronizing test logic and control register access	JTAG clock signal into target CPU
5	GND	Common ground
6	JTAG TDO (Test Data Output) - Serial data input from the target	JTAG data output from target CPU
7	RTCK - Input Return test clock signal from the target	Some targets with a system clock that is too slow must synchronize the JTAG inputs to internal clocks. In the present case, such synchronization is unneeded and TCK merely looped back into RTCK.
8	TDI (Test Data Input) - Serial data output line, sampled on the rising edge of the TCK signal	JTAG data input into target CPU
9	GND	Common ground
10	nSRST RESET	Active-low reset signal. Target CPU reset signal.

3.4.1.1 Debug COM Port Interface

The debug interface is enabled by default and can be disabled by placing a jumper on connector J19. The UART signals can be accessed via the mikroBUS1 connector or via the integrated USB-UART bridge provided by J-Link-OB.

Figure 3-40. Debug COM Port Interface



The table below describes the COM port debug interface signals.

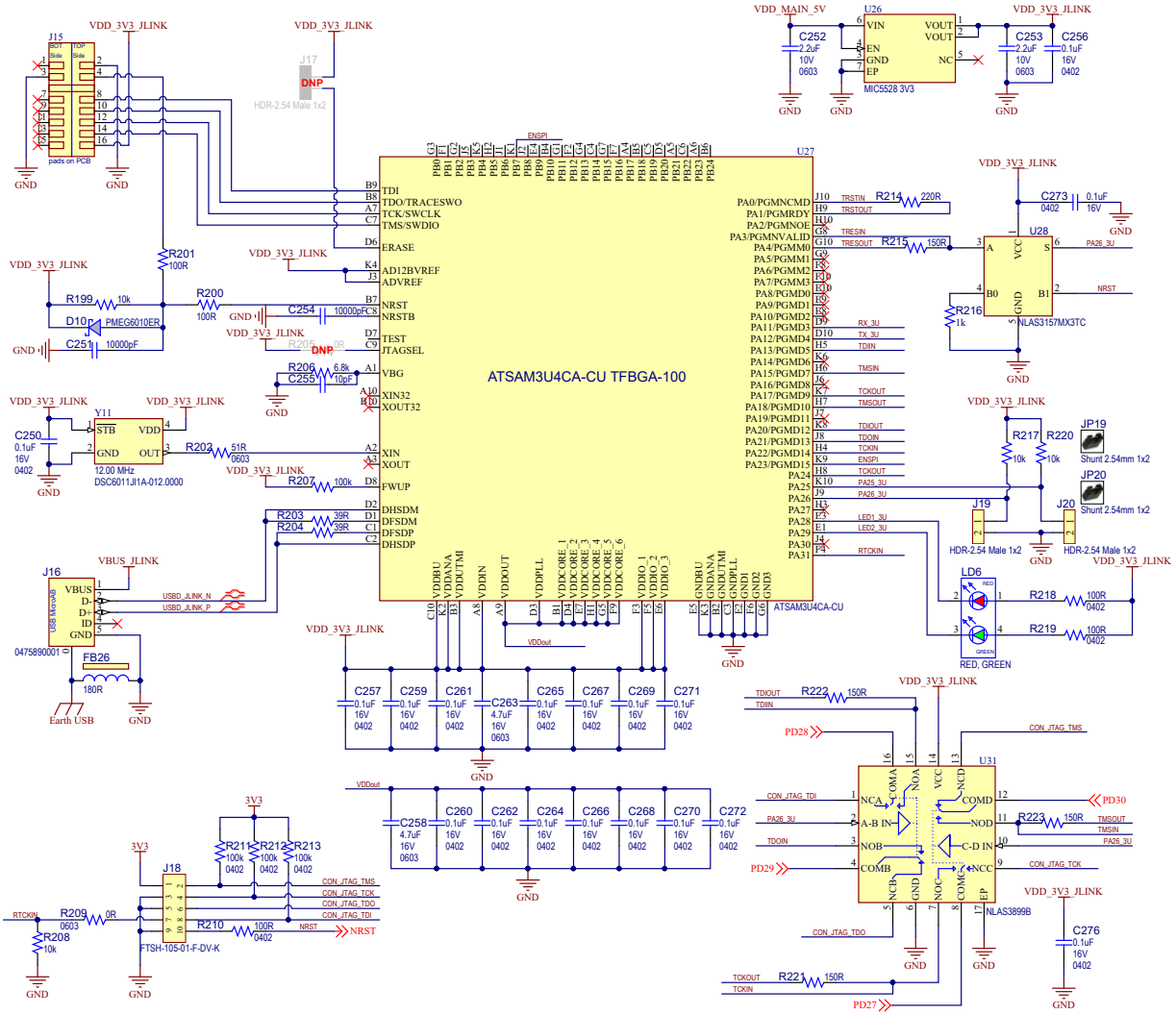
Table 3-23. Debug COM Port PIOs Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PB26	URXD0	DEBUG	Receive data
PB27	UTXD0	DEBUG	Transmit data

3.4.2 Embedded Debugger (J-Link-OB) Interface

The figure below illustrates the implementation of the J-Link-OB and J-Link-CDC interface.

Figure 3-41. J-Link-OB Interface



The SAMA5D2-ICP includes a built-in SEGGER J-Link-On-Board device. The functionality is implemented with an ATSAM3U4C microcontroller in an TFBGA100 package. The ATSAM3U4C provides the functions of JTAG and a bridge USB/Serial debug port (CDC). One two-colored LED (LD6) mounted on the main board shows the status of the J-Link-On-Board device.

The J-Link-OB-ATSAM3U4C was designed in order to provide an efficient, on-board alternative to the standard J-Link.

The USB J-Link-OB port is used as a secondary power source and as a communication link for the board, and derives power from the PC over the USB cable. This port is limited in most cases to 500 mA. A single PC USB port is sufficient to power the board.

3.4.2.1 Disabling J-Link-OB

Jumper JP19 disables the J-Link-OB-ATSAM3U4C JTAG functionality. When the jumper is installed, it grounds pin PA26 of the SAM3U4C that is normally pulled high. A quad analog switch (U31) is used to select the JTAG interface.

- Jumper JP19 not installed: J-Link-OB-ATSAM3U4C is enabled and fully functional.
- Jumper JP19 installed: J-Link-OB-ATSAM3U4C is disabled and an external JTAG controller can be used through the 10-pin JTAG port J18

Jumper JP19 disables only the J-Link functionality. The debug serial com port that is emulated through a Communication Device Class (CDC) of the same USB connector remains operational (if JP20 is open).

Table 3-24. J-Link-OB and CDC LED LD6 Status

LED LD6	State	USB Cable Connected
RED	Off	J-Link not programmed or JP19 and JP20 installed
GREEN	Off	J-Link not programmed or JP19 and JP20 installed
GREEN	Flashing	USB port not connected
GREEN	On	J-Link-OB connected and available

3.4.2.2 Hardware UART via CDC

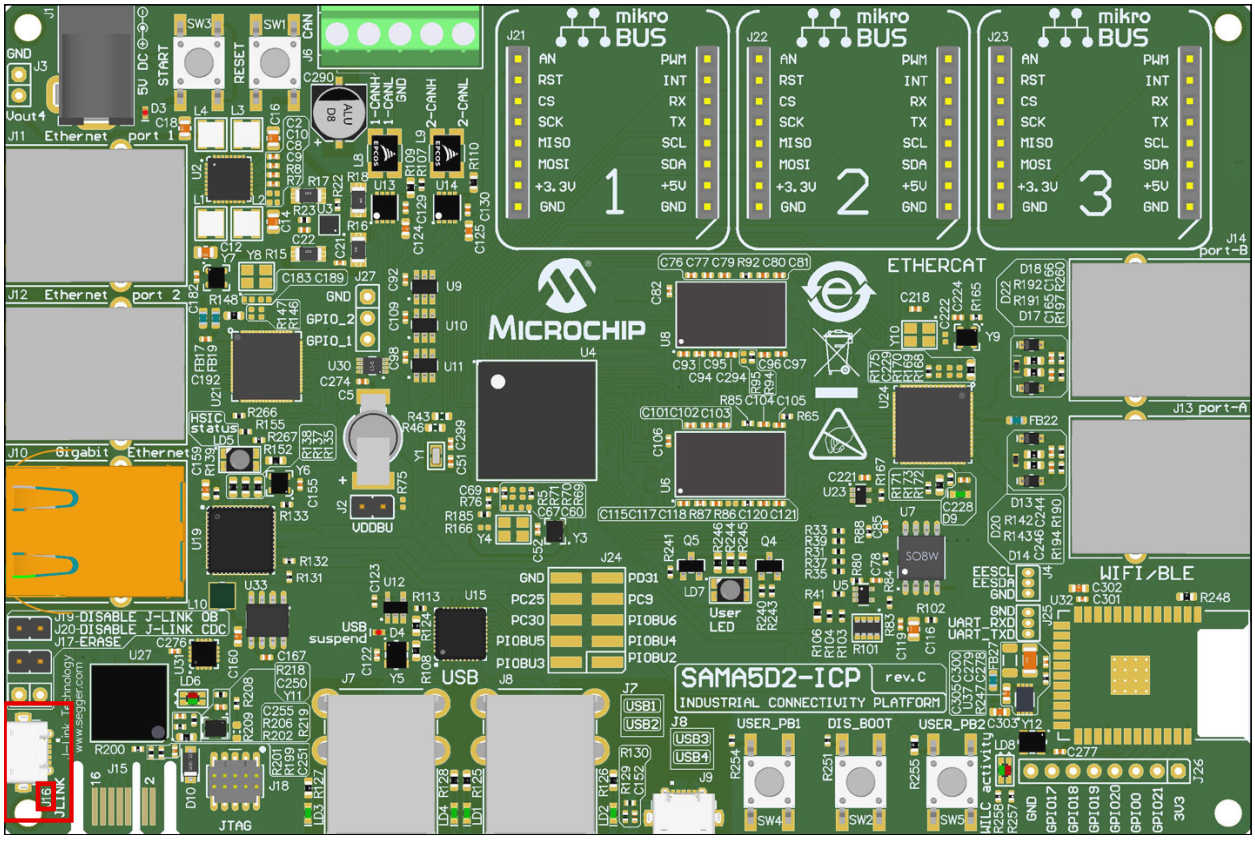
In addition to the J-Link-OB functionality, the SAM3U4C microcontroller provides a bridge to a debug serial port (DBGU) of the processor on a main board. The port is made accessible over the same USB connection used by JTAG by implementing Communication Device Class (CDC), which allows terminal communication with the target device.

This feature is enabled only if the microcontroller pin 25 is not grounded. The pin is normally pulled high and controlled by jumper JP20.

- Jumper JP20 not installed: J-Link-CDC is enabled and fully functional.
- Jumper JP20 installed: J-Link-CDC is disabled.

The USB Communications Device Class (CDC) enables conversion of the USB device into a serial communication device. The target device running USB-Device CDC is recognized by the host as a serial interface (USB2COM, virtual COM port), without the need to install a special host driver (since the CDC is standard). Any PC software using a COM port works without modifications with this virtual COM port. Under Windows®, the device shows up as a COM port; under Linux®, as a /dev/ACMx device. This enables the user to use host software which was not designed to be used with USB, such as a terminal program, giving access to UART0 on the SAMA5D27.

Figure 3-42. J-Link-OB and CDC USB Connector J16 Location



3.4.2.3 Board Edge Connector (J15)

This connector is used to upgrade or download code to the SAM3U4C microcontroller J-Link-OB. Use only for factory programming.

3.5 PIO Usage on Expansion Connectors

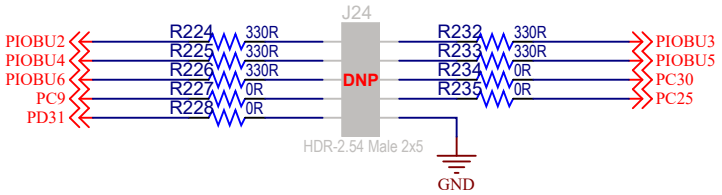
3.5.1 PIOBU Interface

The SAMA5D2-ICP board features five tamper pins for static or dynamic intrusion detections and PIO pins for free use.

For a description of intrusion detection, refer to the SAMA5D2 data sheet, section “Security Module”.

Contact a Microchip Sales Representative for further details.

Figure 3-43. PIOBU Connector



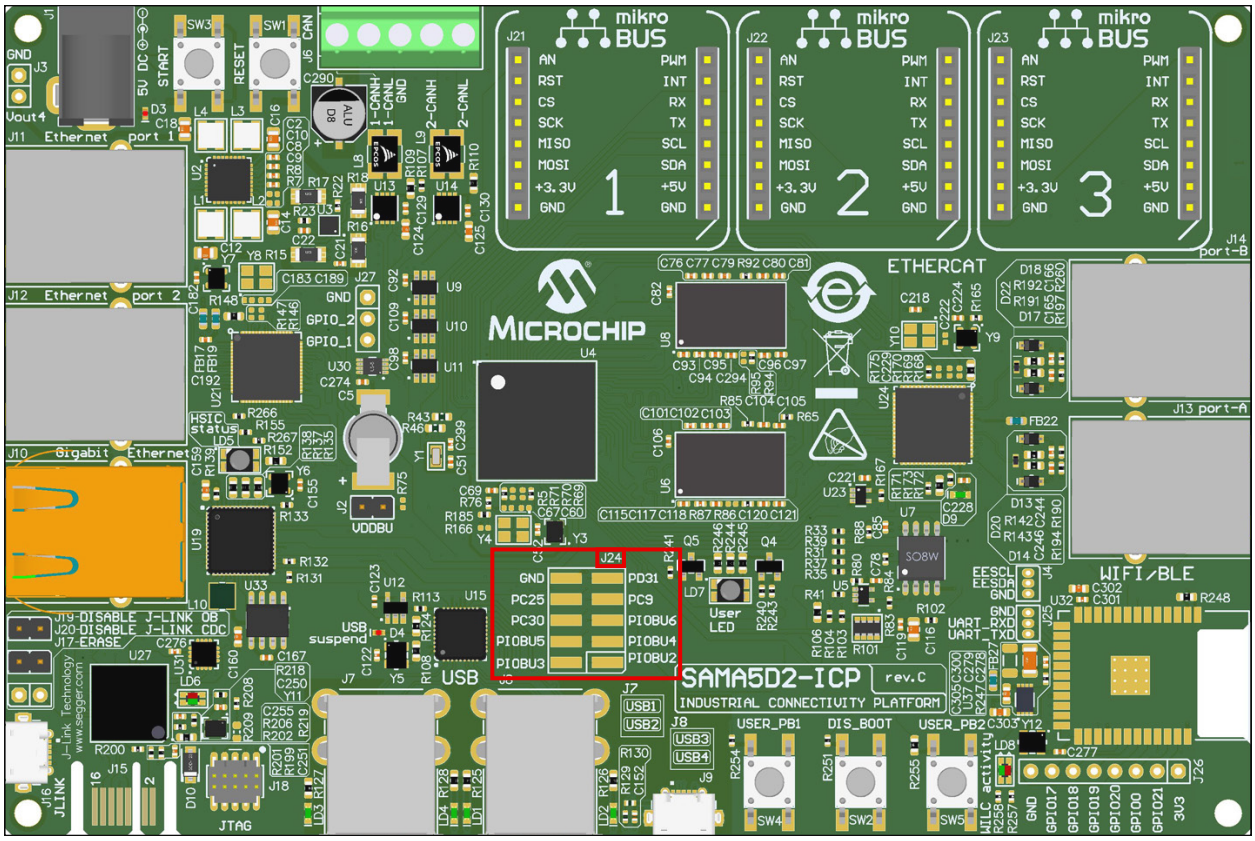
The table below describes the pin assignment of PIOBU connector J24.

Table 3-25. PIOBU Connector J24 Pin Assignment

Signal	Pin No.		Signal
PIOBU2	1	2	PIOBU3
PIOBU4	3	4	PIOBU5
PIOBU6	5	6	PC30
PC9	7	8	PC25
PD31	9	10	GND

The PIOBU connector is not populated and its position on the board is depicted below.

Figure 3-44. PIOBU Connector J24 Location



3.5.2 mikroBUS Interface

The SAMA5D2-ICP hosts three pairs of 8-pin female headers (J21, J22, J23) for the mikroBUS interfaces. The mikroBUS defines mainboard sockets and add-on boards used for interfacing microprocessors with integrated modules with proprietary pin configuration and silkscreen markings. The pinout consists of three groups of communication pins (SPI, UART and TWI), four additional pins (PWM, interrupt, analog input and reset) and two power groups (+3.3V and GND on the left, and 5V and GND on the right 1x8 header).

The figures below illustrates the implementation of the mikroBUS interfaces.

Figure 3-45. mikroBUS1 Interface

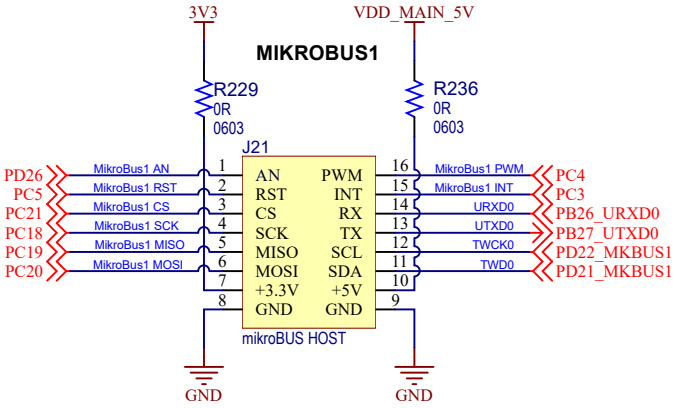


Table 3-26. mikroBUS1 Connector J21 Pin Assignment

SAMA5D27		MBUS Signal	Pin No.		MBUS Signal	SAMA5D27	
Function	PIO					PIO	Function
Analog input	PD26	AN	1	16	PWM	PC4	PWM
Reset	PC5	RST	2	15	INT	PC3	Interrupt
SPI CS	PC21	SPI_NPCS	3	14	UART_RX	PB26	UART receive
SPI clock	PC18	SPI_SPCK	4	13	UART_TX	PB27	UART transmit
SPI MISO	PC19	SPI_MISO	5	12	TWI_SCL	PD22	TWI clock
SPI MOSI	PC20	SPI_MOSI	6	11	TWI_SDA	PD21	TWI data
3.3VCC	–	3.3V supply	7	10	5V supply	–	5VDD
Ground	–	GND	8	9	GND	–	Ground

Figure 3-46. mikroBUS2 Interface

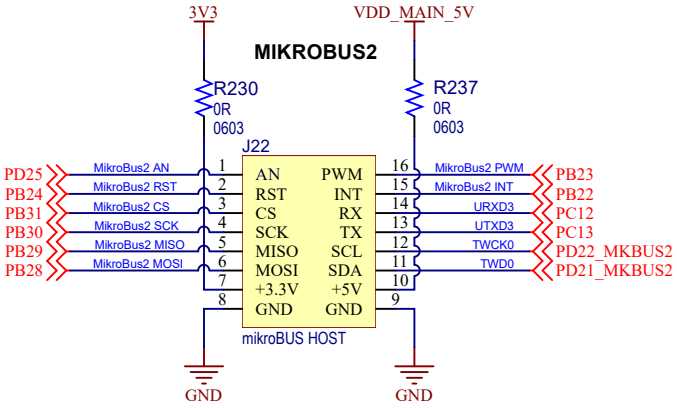


Table 3-27. mikroBUS2 Connector J22 Pin Assignment

SAMA5D27		MBUS Signal	Pin No.		MBUS Signal	SAMA5D27	
Function	PIO					PIO	Function
Analog input	PD25	AN	1	16	PWM	PB23	PWM

.....continued

SAMA5D27		MBUS Signal	Pin No.		MBUS Signal	SAMA5D27	
Function	PIO					PIO	Function
Reset	PB24	RST	2	15	INT	PB22	Interrupt
SPI CS	PB31	SPI_NPCS	3	14	UART_RX	PC12	UART receive
SPI clock	PB30	SPI_SPCK	4	13	UART_TX	PC13	UART transmit
SPI MISO	PB29	SPI_MISO	5	12	TWI_SCL	PD22	TWI clock
SPI MOSI	PB28	SPI_MOSI	6	11	TWI_SDA	PD21	TWI data
3.3VCC	–	3.3V supply	7	10	5V supply	–	5VDD
Ground	–	GND	8	9	GND	–	Ground

Figure 3-47. mikroBUS3 Interface

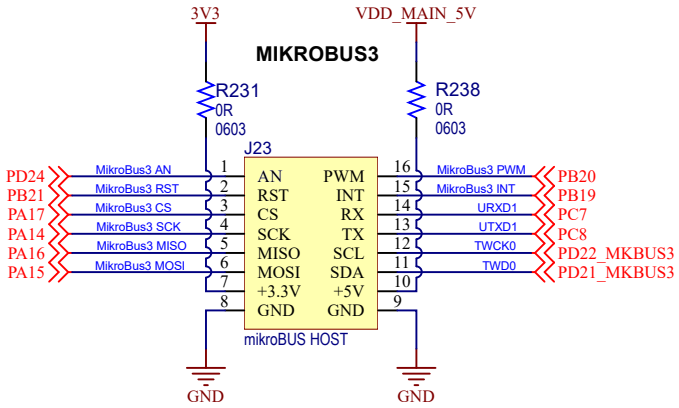
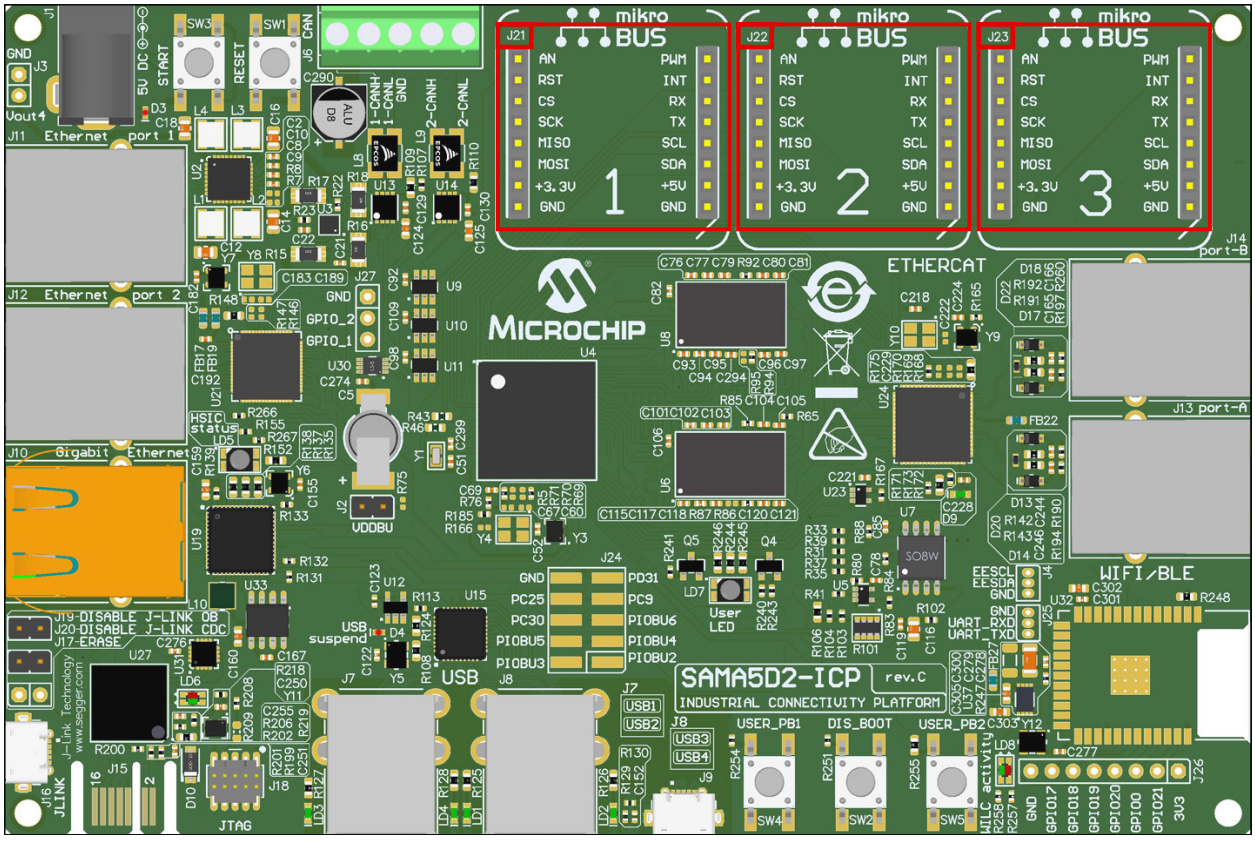


Table 3-28. mikroBUS3 Connector J23 Pin Assignment

SAMA5D27		MBUS Signal	Pin No.		MBUS Signal	SAMA5D27	
Function	PIO					PIO	Function
Analog input	PD24	AN	1	16	PWM	PB20	PWM
Reset	PB21	RST	2	15	INT	PB19	Interrupt
SPI CS	PA17	SPI_NPCS	3	14	UART_RX	PC7	UART receive
SPI clock	PA14	SPI_SPCK	4	13	UART_TX	PC8	UART transmit
SPI MISO	PA16	SPI_MISO	5	12	TWI_SCL	PD22	TWI clock
SPI MOSI	PA15	SPI_MOSI	6	11	TWI_SDA	PD21	TWI data
3.3VCC	–	3.3V supply	7	10	5V Supply	–	5VDD
Ground	–	GND	8	9	GND	–	Ground

Figure 3-48. mikroBUS Connectors Location



4. Board Layout

Figure 4-1. Board Assembly Drawing - Top

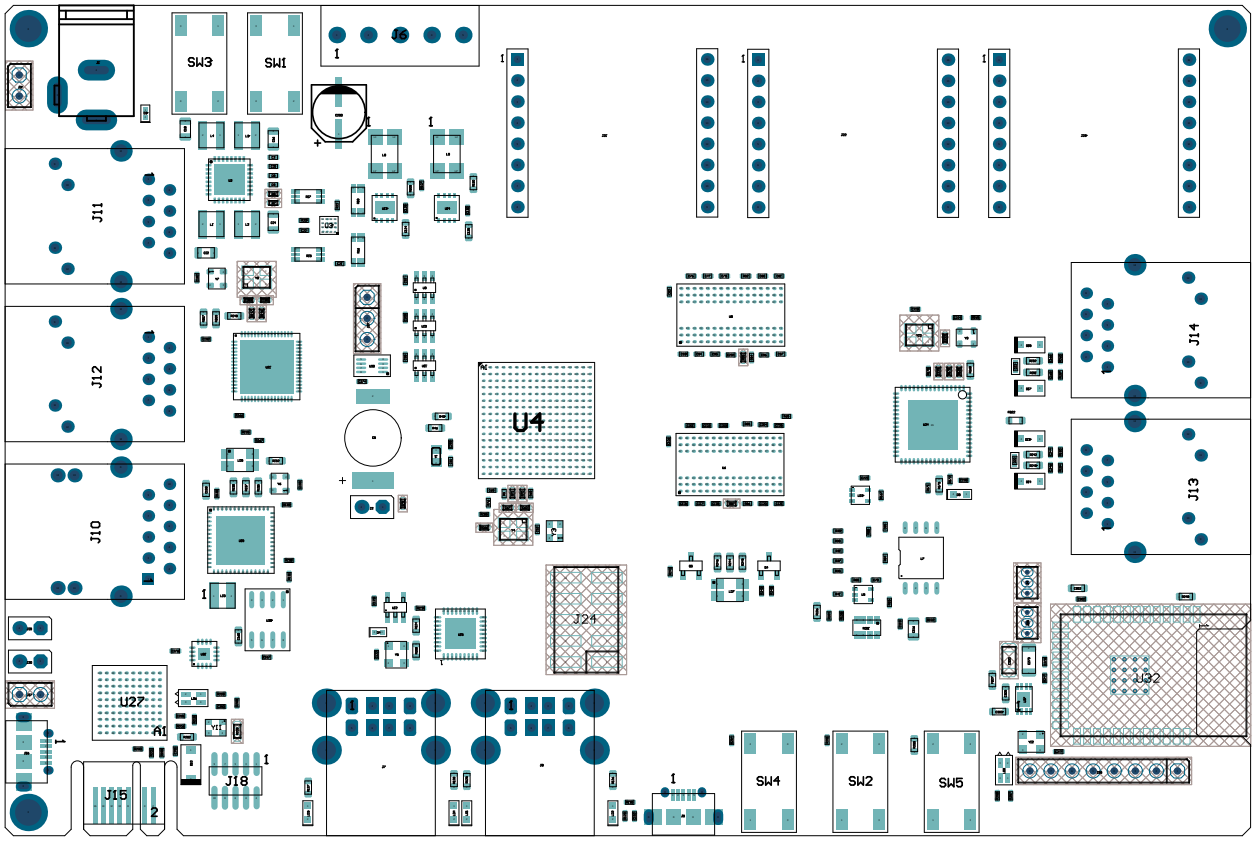
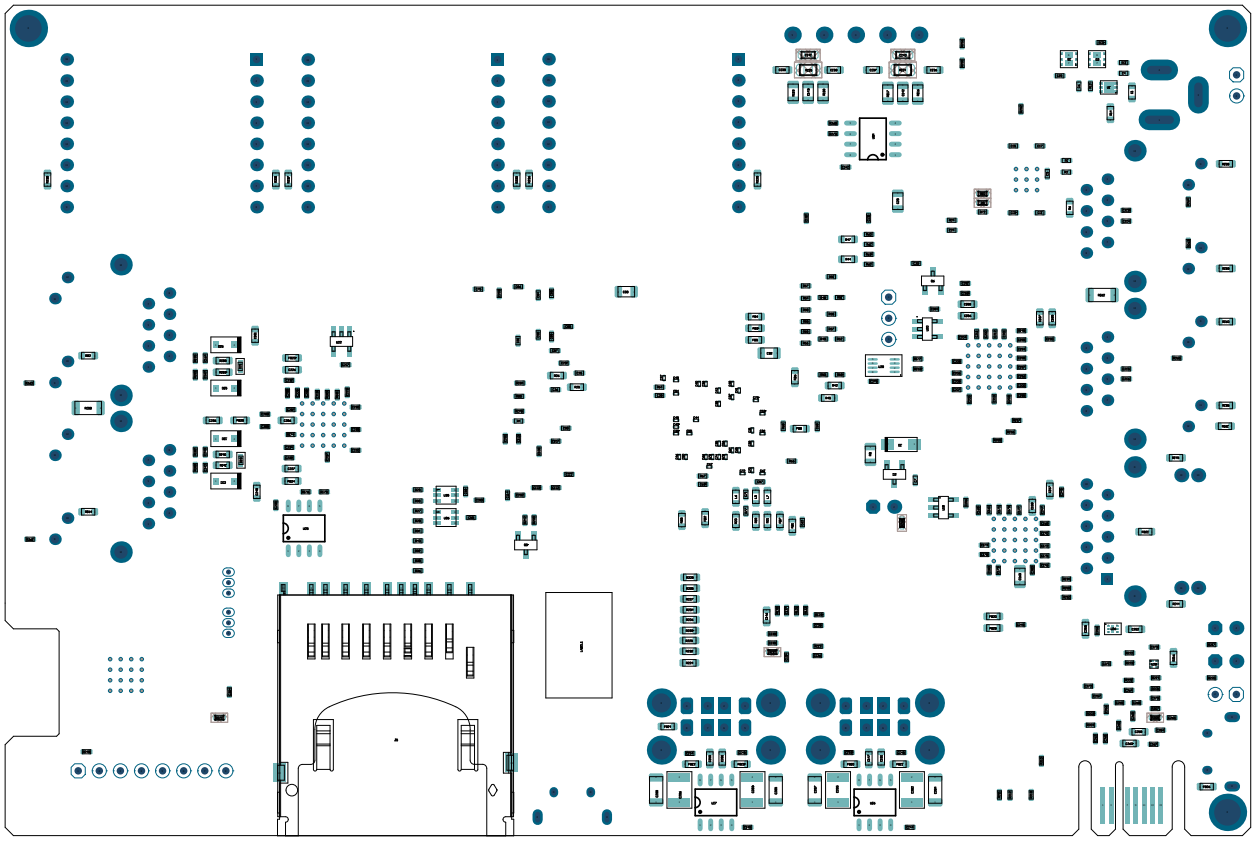


Figure 4-2. Board Assembly Drawing - Bottom



5. Installation and Operation

5.1 System and Configuration Requirements

The SAMA5D2-ICP requires the following:

- Personal computer
- USB A-to-USB-Micro-B cable (provided with the kit)

5.2 Board Setup

Follow these steps to verify proper operation of the kit:

1. Unpack the baseboard, taking care to avoid electrostatic discharge.
2. Check the default jumper settings.
3. Connect the USB Micro-B cable to connector J16 (JLINK-OB).
4. Connect the other end of the cable to a free port of your PC.
5. Open a terminal (console 115200, N, 8, 1) on your Personal Computer.
6. Reset the baseboard. A start-up message appears on the console.

6. Revision History

6.1 Rev. A - 02/2020

First issue.

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