MMA155AA

DC – 24 GHz 32 dBm Distributed Amplifier

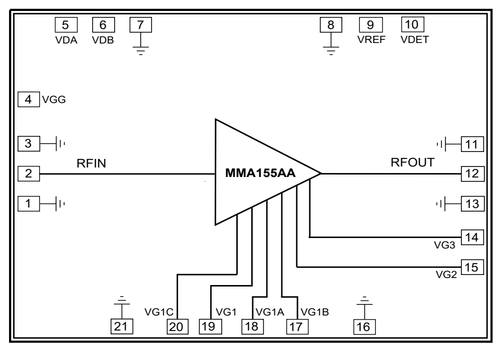
Product Overview

MMA155AA is a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pseudomorphic high-electron-mobility transistor (pHEMT) distributed amplifier that operates between DC and 24 GHz. It is ideal for test instrumentation and wide-band military and space applications. The amplifier provides a gain of 15 dB and 32.5 dBm of output power at 3 dB gain compression with a nominal bias condition of 650 mA from a + 13V supply. Output IP3 is typically 35 dBm. The MMA155AA amplifier is DC coupled and features RF I/Os that are internally matched to 50 Ω.

Key Features

- **Frequency range: DC to 24 GHz**
- **Gain: 15 dB**
- **Positive gain slope**
- **Flat power response to 20 GHz**
- **Low- IM3: –37 dBc at 18 dBm, 22 GHz**
- **Low noise figure: 3.0 dB at 10 GHz**
- **Supply: 650 mA @ + 13V**
- **Power level detector**
- **Passivated space-qualified process listed on EPPL007 – 38**
- **50 Ω matched input/output**
- **Die size: 3.3 mm × 1.68 mm × 0.075 mm**

Functional Block Diagram



Applications

- Test and measurement instrumentation
- Military and space
- Telecom infrastructure
- Wideband microwave radios
- Microwave and millimeter-wave communication systems

Gain, NF, OP1dB & OIP3 Performances

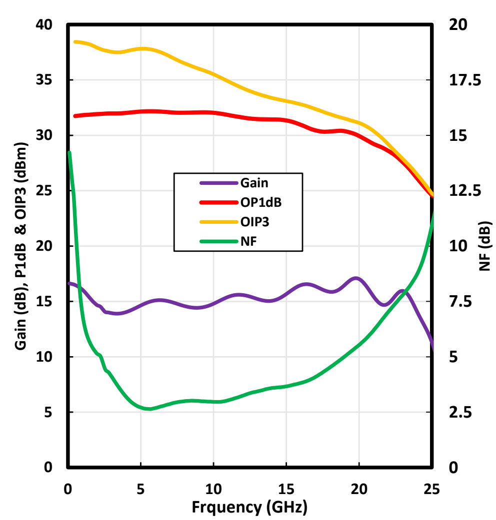


Table 1. Performance Overview

Parameter	Typ.	Units
Frequency range	DC – 24	GHz
Gain	15	dB
Gain flatness	±1	dB
P1dB	32	dBm
Psat	32.5	dBm
IMD3 @ Pout = 18dBm	–40	dBc

Export Classification: EAR99

Table of Contents

1. Electrical Performances

1.1 Typical Electrical Performance

Table 1-1. Typical Electrical Performance at + 25 °C and 13V/650mA (Unless otherwise specified)

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		DC		22	GHz
Gain	DC – 6 GHz		14		dB
	6 – 18 GHz		15		dB
	18 – 22 GHz		15		dB
	22 – 24 GHz		14		dB
Gain flatness	DC – 6 GHz		± 0.5		dB
	6 – 18 GHz		± 1.0		dB
	18 –22 GHz		± 1.5		dB
	22 – 24 GHz		± 1.5		dB
P1dB	DC – 6 GHz		32		dBm
	6 – 18 GHz		31		dBm
	18 – 22 GHz		29.5		dBm
	22 – 24 GHz		26.5		dBm
OIM3 @ Pout = +18 dBm	DC – 6 GHz		38		dBc
	6 – 18 GHz		34		dBc
	18 – 22 GHz		31		dBc
	22 – 24 GHz		28		
Noise Figure	2 – 6 GHz		4.5		dB
	6 – 18 GHz		4.0		dB
	18 – 22 GHz		6.5		dB
	22 – 24 GHz		8.5		dB
Input Return Loss	DC – 6 GHz		12.5		dB
	6 – 18 GHz		13.5		dB
	18 – 22 GHz		11.5		dB
	22 – 24 GHz		11.5		dB
Output Return Loss	DC – 6 GHz		8		dB
	6 – 18 GHz		8.5		dB
	18 – 22 GHz		6.5		dB
	22 – 24 GHz		6.5		dB
Vdd (Drain Voltage Supply)			13	15	V

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Parameter	**Frequency Range**	**Min**	**Typ.**	**Max**	**Units**
Idd (Drain Current)			650	750	mA

1.2 Typical Performance Curves

1.2.1 Typical Performance Curves at 11V

The following graphs show the typical performance curves of the MMA155AA device at 25 °C and 11V/550mA unless otherwise indicated.

Figure 1-1. Gain vs. Temperature

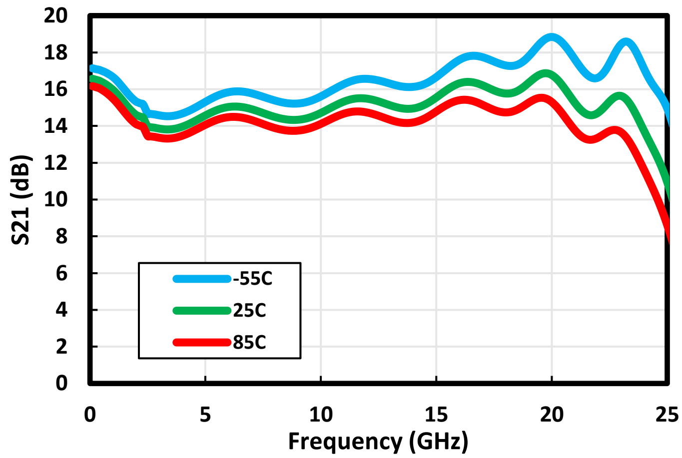


Figure 1-2. Output P1dB vs. Temperature

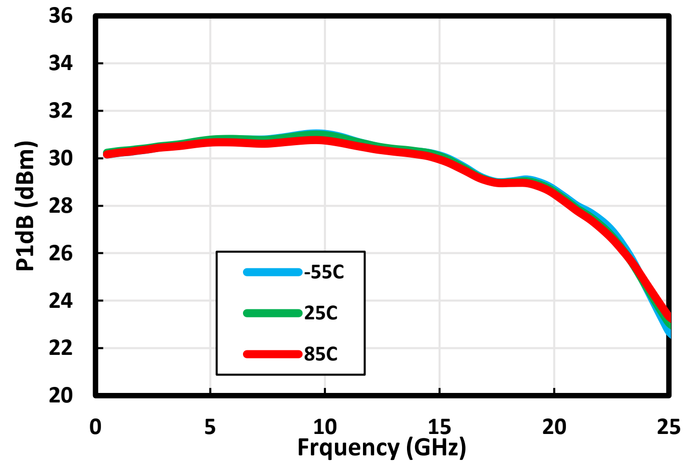


Figure 1-3. Output IP3 vs. Temperature

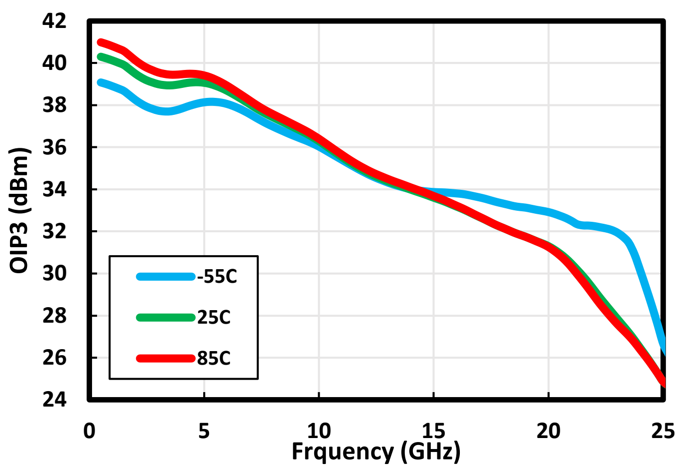


Figure 1-4. NF vs. Temperature

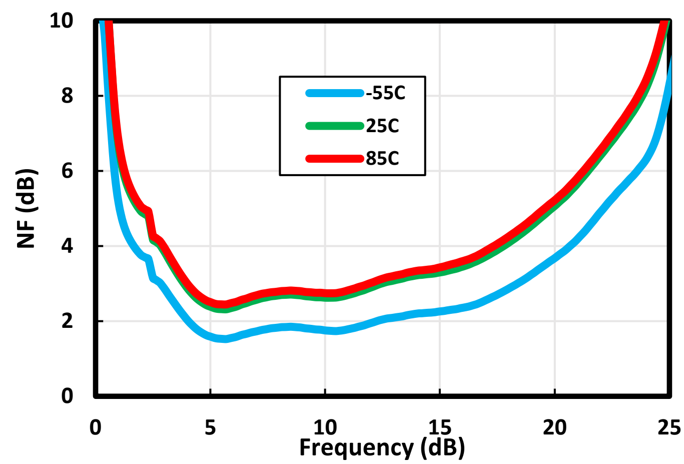


Figure 1-5. Output P3dB vs. Temperature

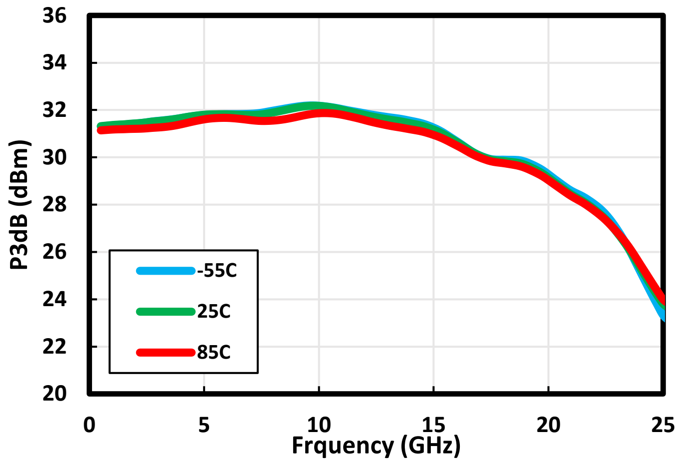


Figure 1-6. S12 vs. Temperature

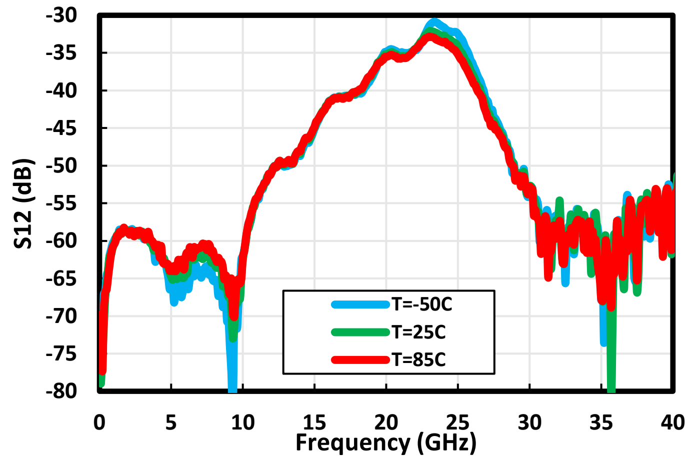


Figure 1-7. Input RL vs. Temperature

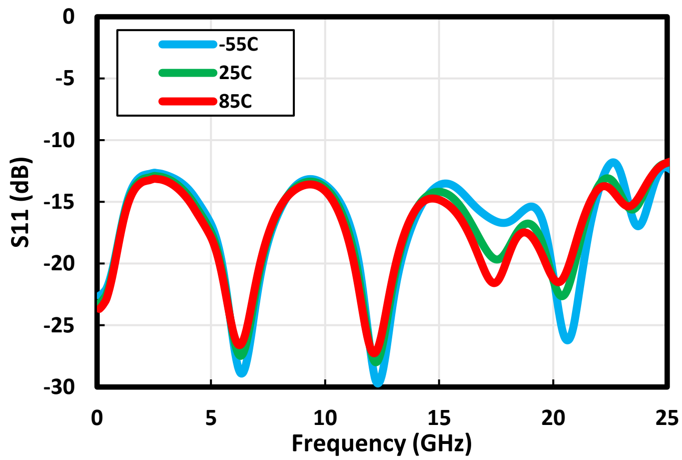


Figure 1-8. Output RL vs. Temperature

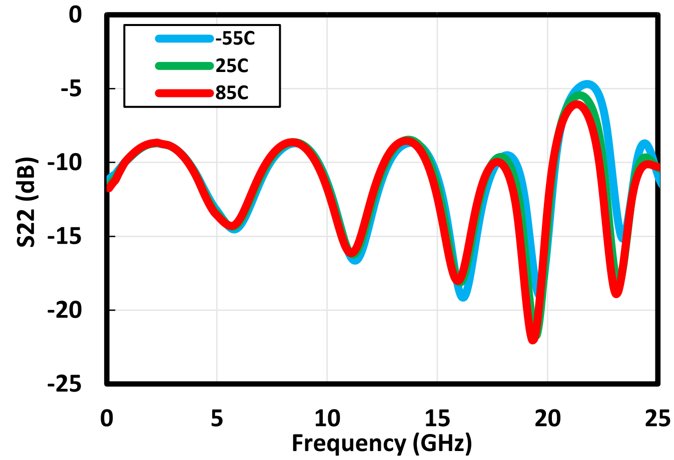


Figure 1-9. IM3 vs. Output Power @ 11V/470mA

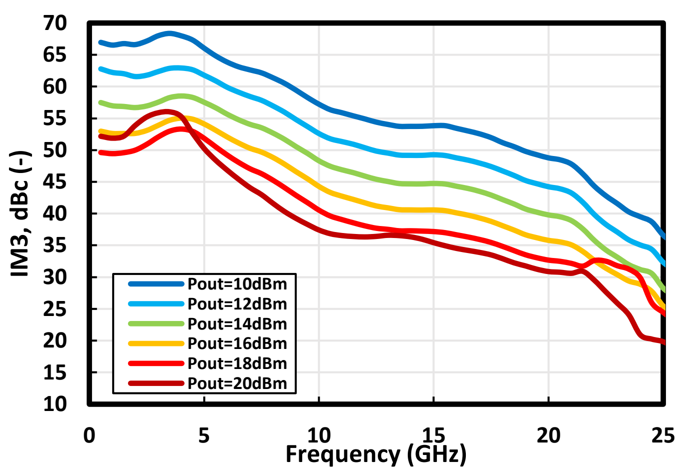


Figure 1-10. H2 vs. Output Power @ 11V/470mA

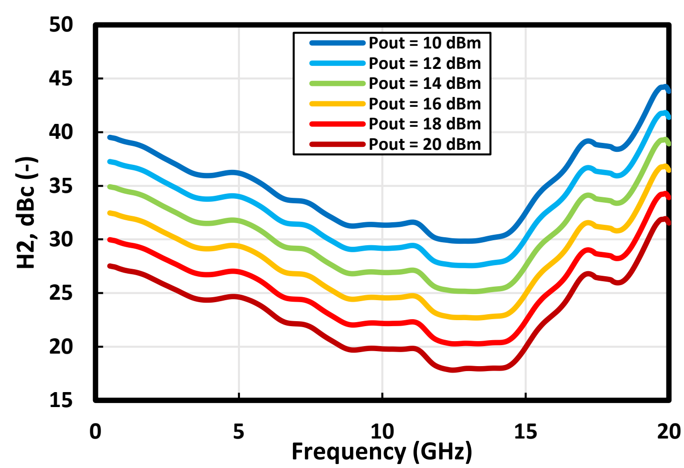


Figure 1-11. Detector Ouput vs. Output Power & Frequency @ 11V/470mA

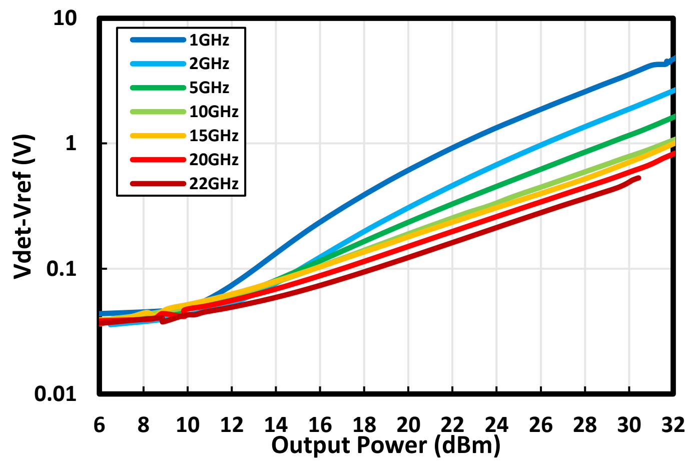
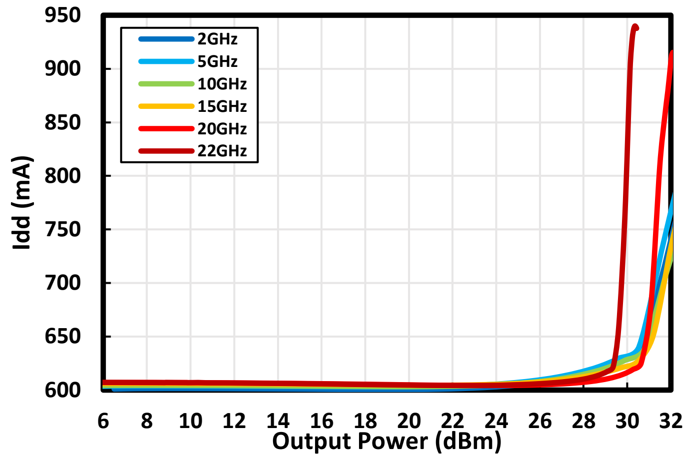


Figure 1-12. Idd vs. Output Power & Frequency @ 11V/470mA



1.2.2 Typical Performance Curves at 13V

The following graphs show the typical performance curves of the MMA155AA device at 25 °C and 13V/650mA unless otherwise indicated.

Figure 1-13. Gain vs. Temperature

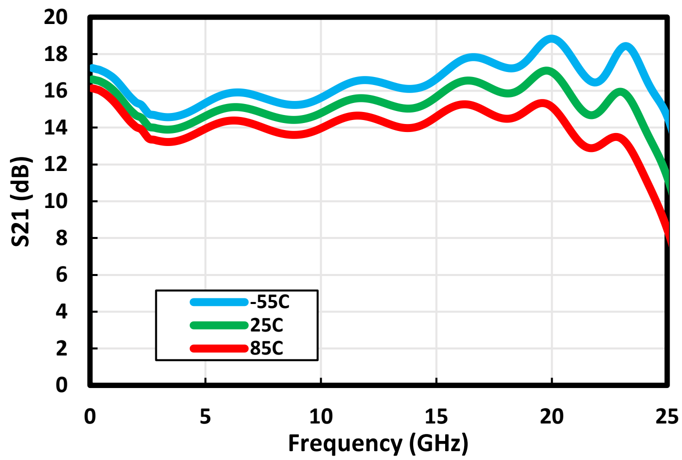


Figure 1-14. Output P1dB vs. Temperature

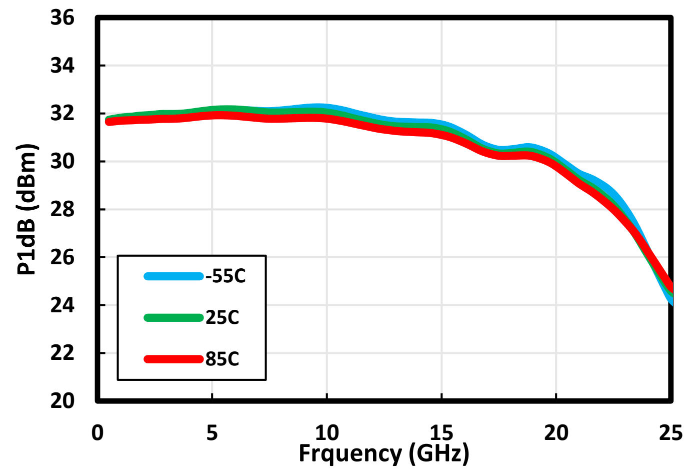


Figure 1-15. Output IP3 vs. Temperature

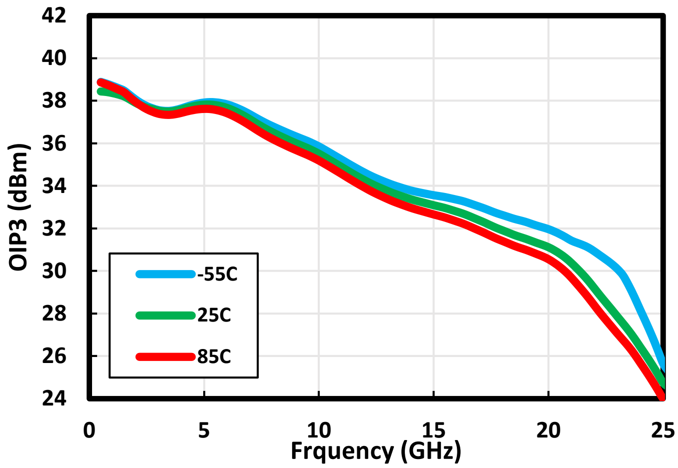


Figure 1-16. Noise Figure vs. Temperature

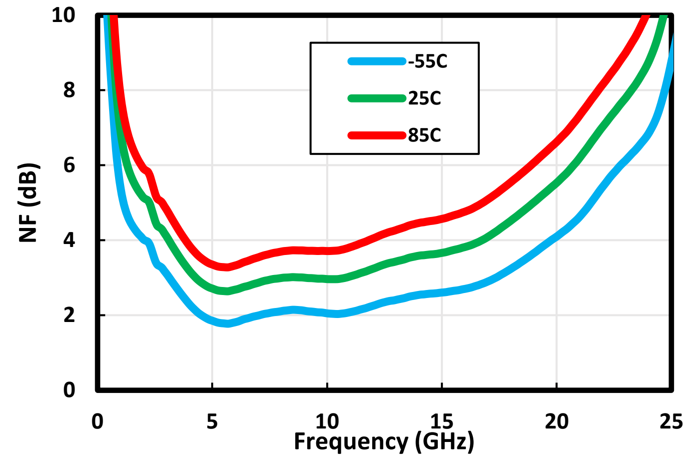


Figure 1-17. Output P3dB vs. Temperature

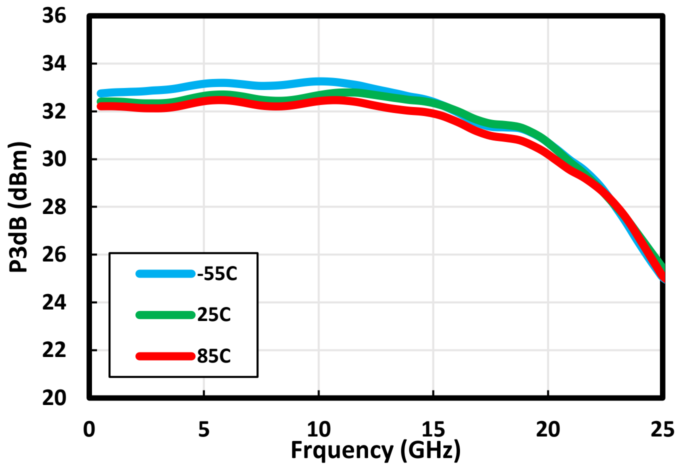


Figure 1-18. H2 vs. Output Power @ 13V/600mA

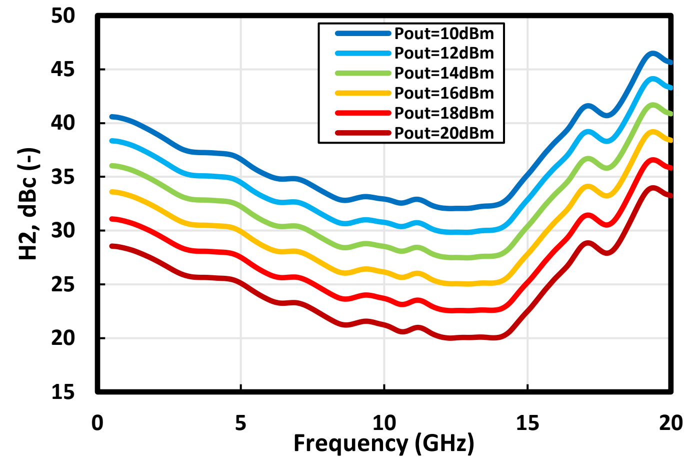


Figure 1-19. Input RL vs. Temperature

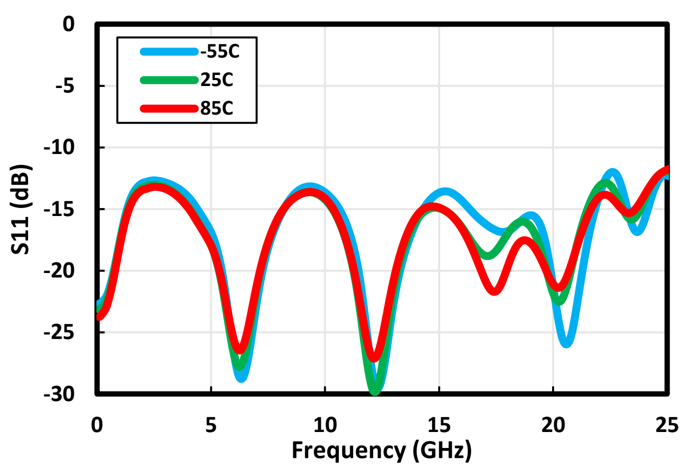
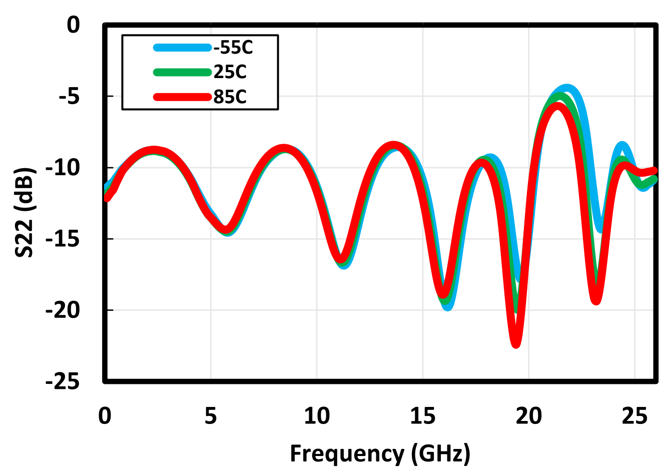


Figure 1-20. Output RL vs. Temperature



1.2.3 Typical Performance Curves at 15V

The following graphs show the typical performance curves of the MMA155AA device at 25 °C and 15V/750mA unless otherwise indicated.

Figure 1-21. Gain vs. Temperature

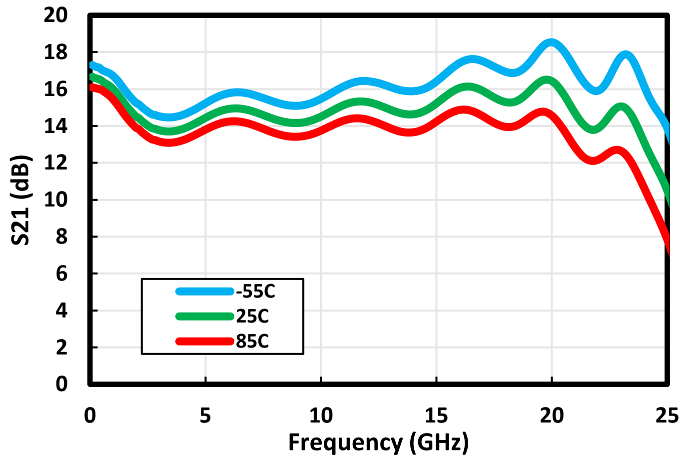


Figure 1-22. Output P1dB vs. Temperature

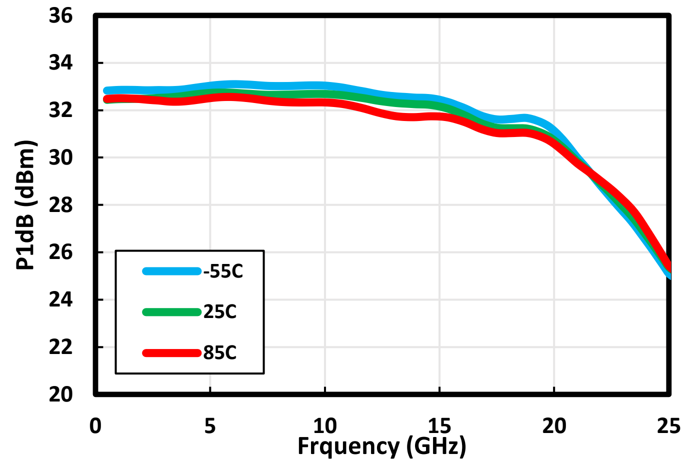


Figure 1-23. Output IP3 vs. Temperature

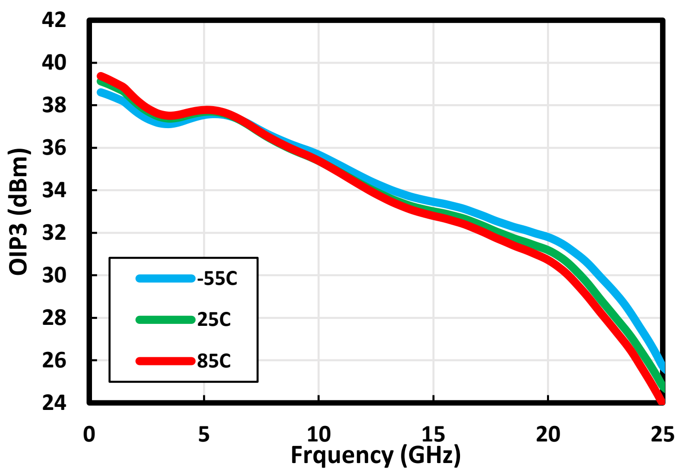


Figure 1-24. Noise Figure vs. Temperature

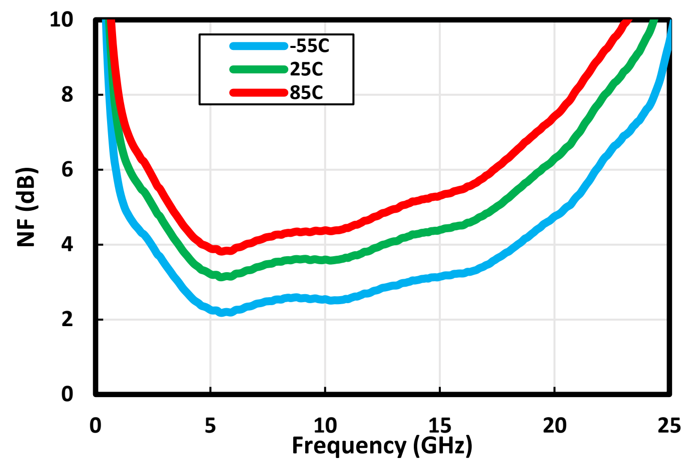


Figure 1-25. Output P3dB vs. Temperature

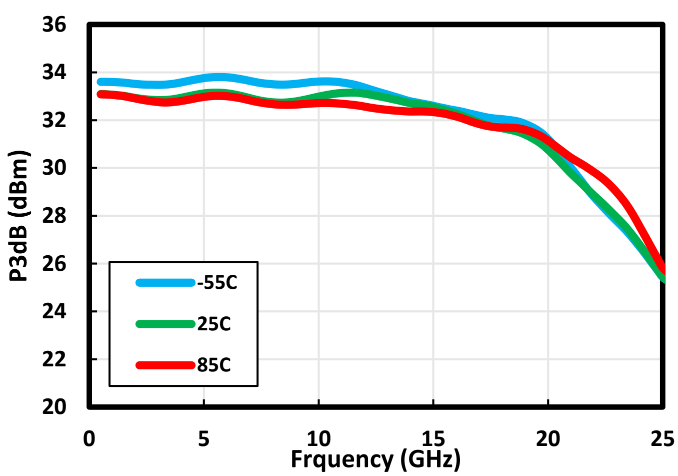


Figure 1-26. Input RL vs. Temperature

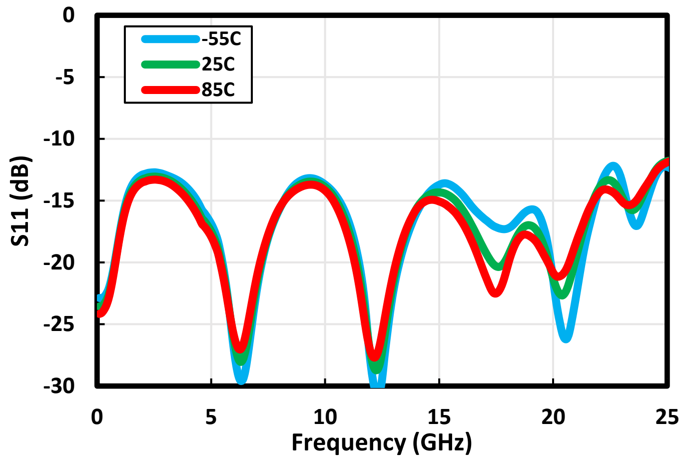
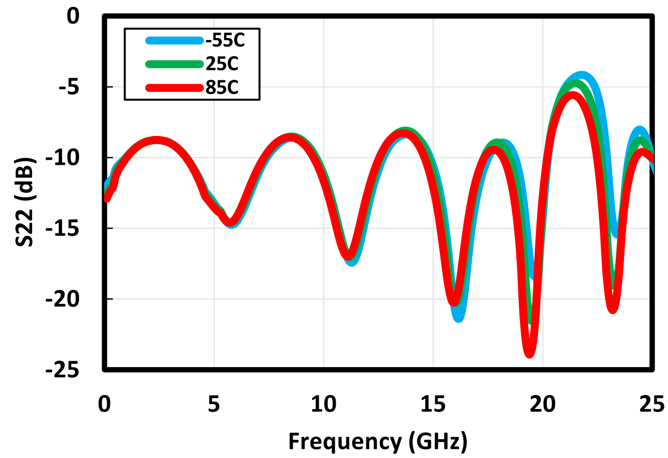


Figure 1-27. Output RL vs. Temperature



1.3 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the MMA155AA device at 25 °C, unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

Table 1-2. Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (Vdd)	18V
Vdd current (Idd)	800 mA
Gate bias voltage (VG)	–2V to +0.5V
RF input power (Pin)	+25 dBm (or 6 dB gain compression)
DC power dissipation (T = +85 °C) at Psat	9.4W
DC power dissipation (T = +85 °C) at Low Power	12.1W
Thermal Resistance at Psat	9.6 °C/W
Thermal Resistance at Low Power	7.4 °C/W
Channel Temperature	+175 °C
Operating Temperature	–55 °C to +85 °C
Storage Temperature	–65 °C to +150 °C

ESD Sensitive Device

2. Die Specifications

The following illustration shows the chip outline of the MMA155AA device. Dimensions are shown millimeters. The minimum bond pad size is 100 µm × 100 µm. The die thickness is 80 µm. The backside is the DC/RF ground.

For additional packaging information, contact your Microchip sales representative.

Figure 2-1. Die Outline Drawing

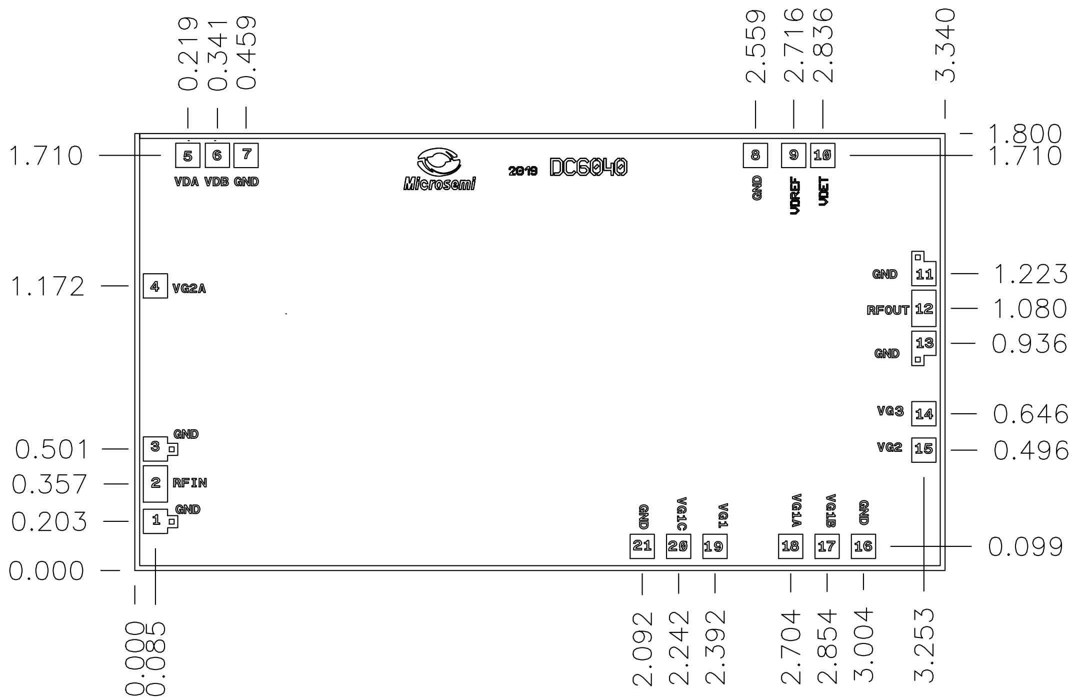


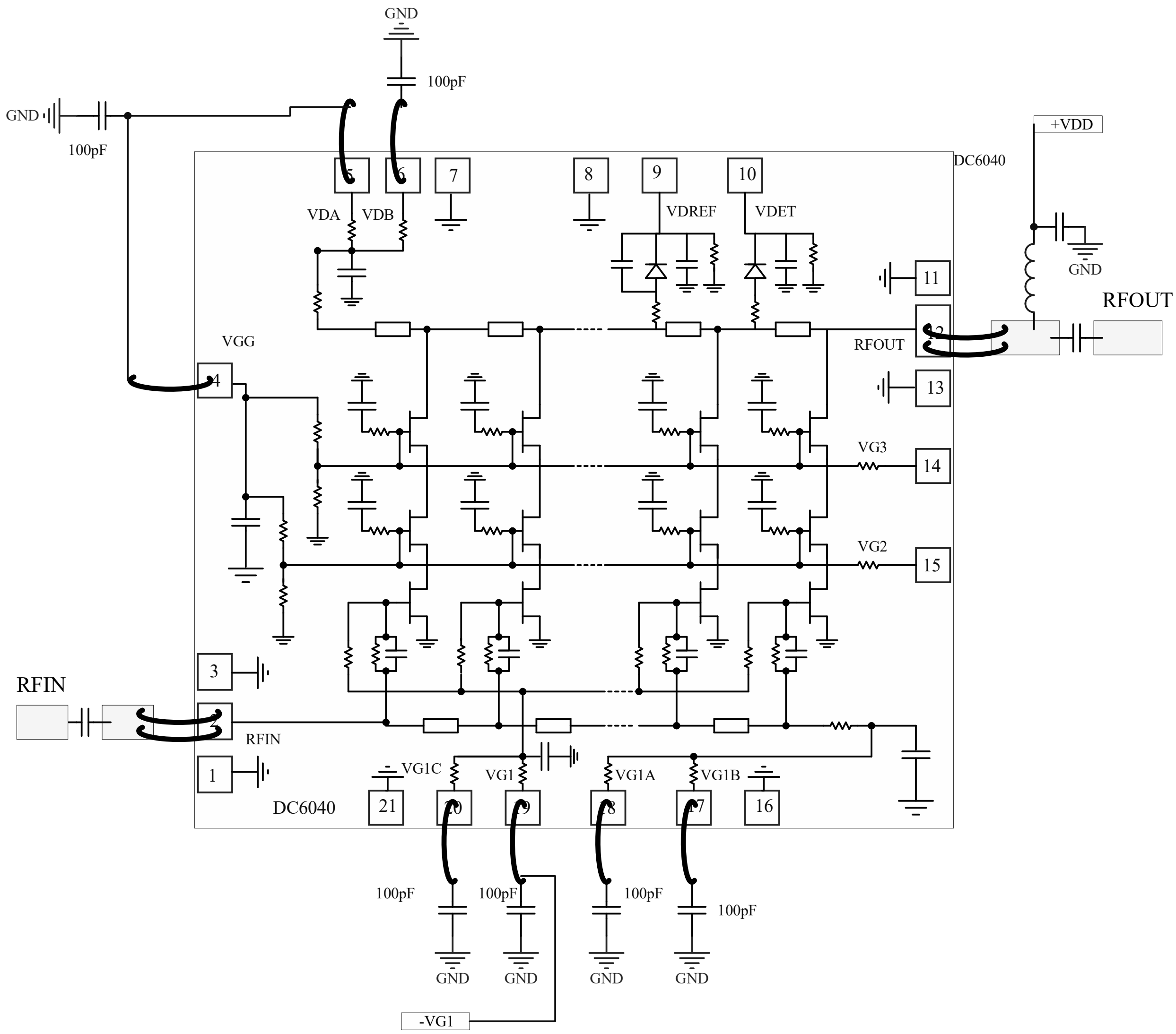
Table 2-1. I/O Pad Description

Pad Number	Pad Name	Pad Description
2	RFIN	RF Input, DC coupled to VDA and matched to 50Ω.
12	RFOUT	RF Output, DC coupled and matched to 50Ω. Used also to DC bias the Die through external Bias T
19	VG1	DC bias for Gate 1 (negative)
17, 18 & 20	VG1B, VG1A & VG1C	Complimentary Low Frequency terminations, for higher value capacitors connections, also DC coupled to VG1
15	VG2	2nd Gate Bias access, not used in normal operation
4	VG2A	2nd Gate Bias, have to be coupled to Vdd , for normal operation, use VDA (pad 6)
14	VG3	3rd Gate Bias access, not used in normal operation
5 & 6	VDA & VDB	Optional Low Frequency termination, connecting to high value cap, typically 10nF
10	VDET	Differential Detector Output voltage
9	VREF	Reference Voltage of the differential Detector
1, 3, 7, 8, 11, 13, 16 & 21	RF/DC GND	Must be connected to RF/DC Ground
Backside Paddle	RF/DC GND	Must be connected to RF/DC Ground

3. Application Ciruits

Enter a short description of your topic here (optional).

Figure 3-1. Application Circuit: Schematic



The following illustration shows the assembly diagram of the MMA155AA device. The carrier plate is gold plated. It is necessary to attach components using conductive epoxy. The bypass chip caps are ceramic and must be assembled within 10 mils of the die. Use 1 mil Au bond wires

Figure 3-2. Test Circuit DC – 26 GHz: Assembly Drawing

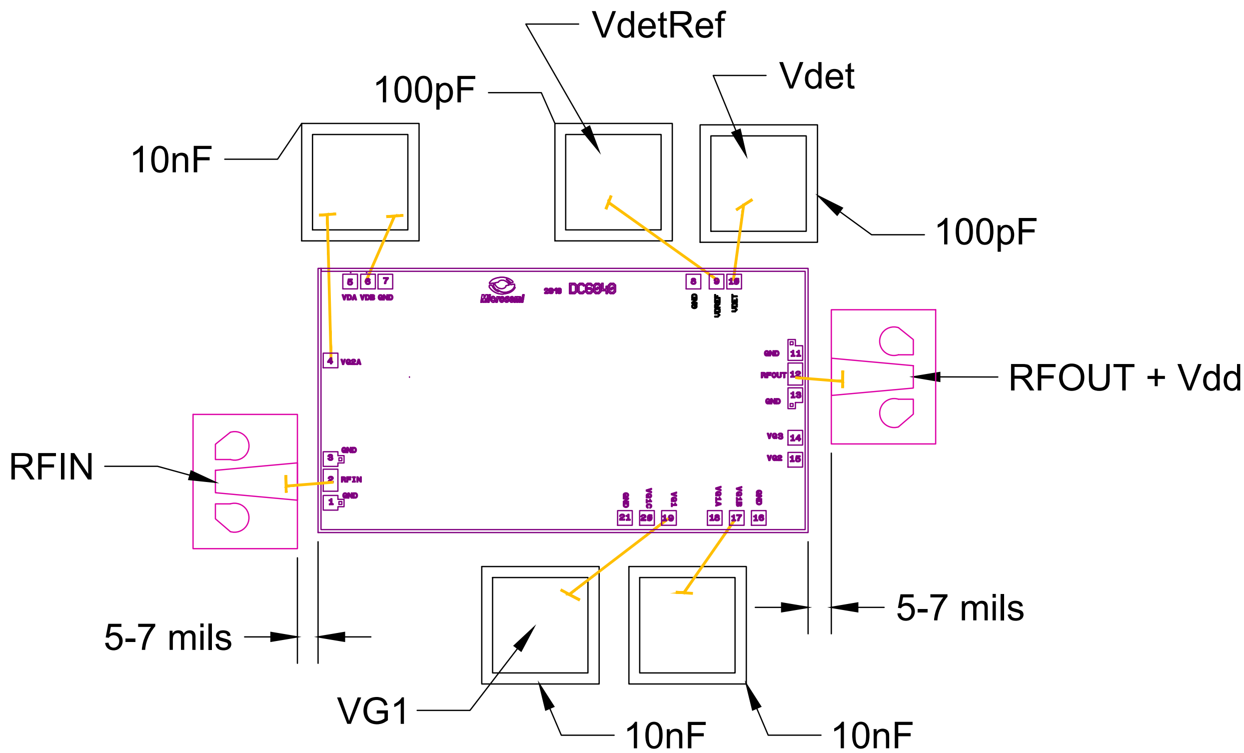


Table 3-1. Bill of material (BOM)

Component	Value	Part Number	Description
C1 & C2	0.1uF +/- 100 pF	MVB4040X104MEK5C1B	Presidio VB series dual caps. 40 mils X 40mils X17 mils

4. Ordering, Shipping and Handling

4.1 Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4.2 Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
MMA155AA	Die

4.3 Packing Information

Standard Format
Gel Pack

Note: Contact your Microchip sales representative for the minimum Die quantity order

5. Revision History

Table 5-1. Revision History

Revision	Date	Description
A	08/2021	Document created.

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