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**EVB-KSZ8563
Evaluation Board
User's Guide**

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NOTES:

Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXA”, where “XXXX” is the document number and “A” is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the KSZ8563. Items discussed in this chapter include:

- [Document Layout](#)
- [Conventions Used in this Guide](#)
- [The Microchip Web Site](#)
- [Development Systems Customer Change Notification Service](#)
- [Customer Support](#)
- [Document Revision History](#)

DOCUMENT LAYOUT

This document describes how to use the EVB-KSZ8563 Evaluation Board as a development tool for the KSZ8563, 3-Port Fast Ethernet Switch with RGMII Interface and IEEE 1588v2 / 802.1AS support.

- **Chapter 1. “Overview”** – This chapter provides a brief description of the EVB-KSZ8563 Evaluation Board.
- **Chapter 2. “Board Details and Configuration”** – This chapter includes instructions on how to get started with the EVB-KSZ8563 Evaluation Board.
- **Appendix A. “EVB-KSZ8563 Evaluation Board”** – This appendix shows the physical EVB-KSZ8563 Evaluation Board.
- **Appendix B. “EVB-KSZ8563 Schematics”** – This appendix shows the EVB-KSZ8563 Evaluation Board schematics.
- **Appendix C. “EVB-KSZ8563 Bill of Materials (BOM)”** – This appendix includes the EVB-KSZ8563 Evaluation Board Bill of Materials (BOM).
- **Appendix D. “EVB-KSZ8563 Silk Screen”** – This appendix includes the EVB-KSZ8563 Evaluation Board silk screen.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	<i>MPLAB® IDE User's Guide</i>
	Emphasized text	...is the <i>only</i> compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	<u><i>File>Save</i></u>
Bold characters	A dialog button	Click OK
	A tab	Click the Power tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	#define START
	Filenames	autoexec.bat
	File paths	c:\mcc18\h
	Keywords	_asm, _endasm, static
	Command-line options	-Opa+, -Opa-
	Bit values	0, 1
	Constants	0xFF, 'A'
Italic Courier New	A variable argument	<i>file.o</i> , where <i>file</i> can be any valid filename
Square brackets []	Optional arguments	mcc18 [options] <i>file</i> [options]
Curly brackets and pipe character: { }	Choice of mutually exclusive arguments; an OR selection	errorlevel {0 1}
Ellipses...	Replaces repeated text	var_name [, var_name...]
	Represents code supplied by user	void main (void) { ... }

THE MICROCHIP WEB SITE

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- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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The Development Systems product group categories are:

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- **Emulators** – The latest information on Microchip in-circuit emulators. This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

EVB-KSZ8563 Evaluation Board User's Guide

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at:

<http://www.microchip.com/support>

DOCUMENT REVISION HISTORY

Revisions	Section/Figure/Entry	Correction
DS50002755A (05-10-18)	Initial release.	

Chapter 1. Overview

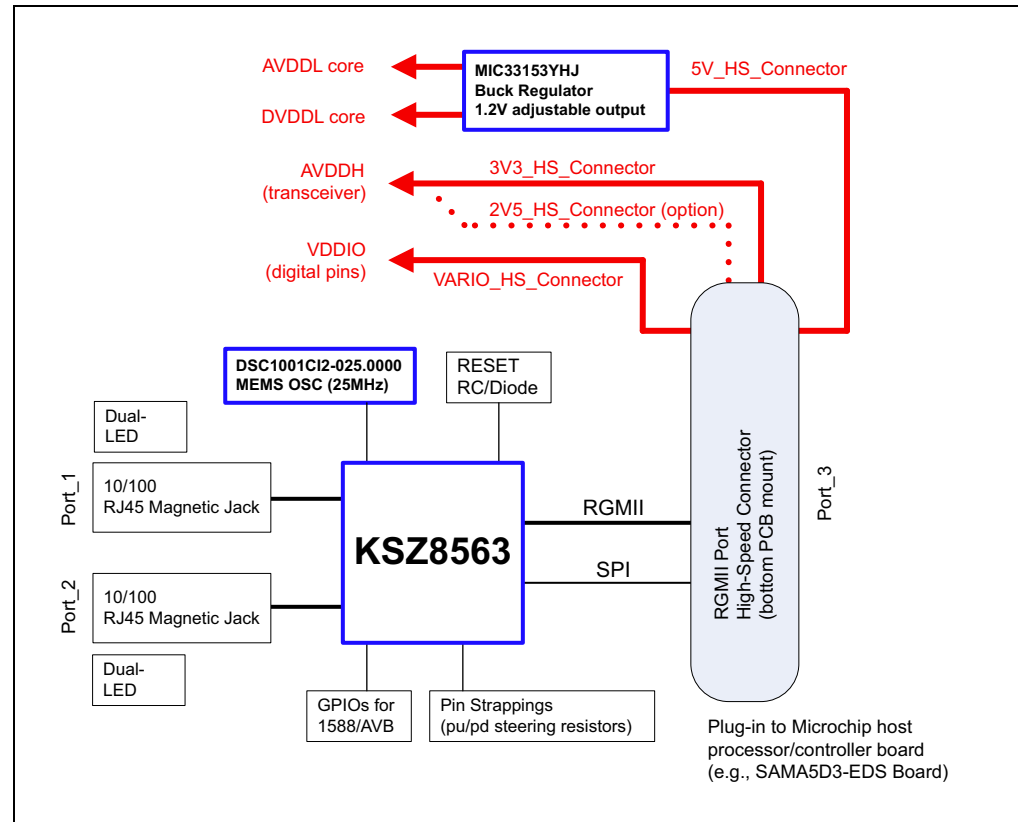
1.1 INTRODUCTION

The EVB-KSZ8563 evaluation board is a plug-in card that interfaces directly with a mating Microchip host processor/controller board, such as the SAMA5D3-EDS Board. It features the KSZ8563, a highly-integrated networking device that incorporates a layer-2+ managed Fast Ethernet switch, two 10BASE-T/100BASE-TX physical layer transceivers (PHYs) and associated MAC units, and one MAC port configured as the RGMII interface. The board's two PHY ports are connected to RJ45 Ethernet jacks with integrated magnetics, and the RGMII MAC interface is brought out to a high-speed multi-pin (HS) connector.

As a set, the EVB-KSZ8563 and SAMA5D3-EDS Board provide a highly-flexible platform to allow evaluation of basic KSZ8563 PHY/Switch features using static control-status registers (CSRs) to develop firmware of advanced KSZ8563 MAC/Switch features, such as IEEE1588 PTP, AVB, and RSTP/MSTP that require interaction with upper network layers.

The scope of this document is meant to describe the EVB-KSZ8563 evaluation board setup and its user interface features. A simplified block diagram of the board is shown in [Figure 1-1](#).

FIGURE 1-1: EVB-KSZ8563 FUNCTIONAL BLOCK DIAGRAM



1.2 REFERENCES

Concepts and materials available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- *KSZ8563 Data Sheet*
- *EVB-KSZ8563 Schematics*
- *SAMA5D3-EDS Schematics*
- *SAMA5D3-EDS Board User's Guide*
- *MIC33153YHJ Data Sheet*
- *DSC1001 Data Sheet*

Chapter 2. Board Details and Configuration

2.1 INTRODUCTION

The EVB-KSZ8563 is designed as a plug-in card to interface directly with a mating Microchip host processor or controller board, such as the SAMA5D3-EDS Board, that supplies full power and provides full register access and configuration via IBA, SPI, or I²C bus management.

2.2 POWER SOURCE

The EVB-KSZ8563 is completely bus-powered from its mating Microchip host processor or controller board. Input power is delivered via the high-speed multi-pin (HS) connector.

Refer to [Figure 2-3](#) and board schematics in [Appendix B. “EVB-KSZ8563 Schematics”](#) for details.

2.2.1 Power Probe Points

The power probe points along with the ground test points are shown in [Figure 2-2](#).

2.2.2 Current Access Rework/Probe Points

The EVB-KSZ8563 design is not intended to perform current measurements on the device. If needed, the current access points to measure the current consumption of the KSZ8563 power rails are across the following series ferrite beads to the board powers.

- DVDDL: FB2
- AVDDL: FB3
- VDDIO: FB6
- AVDDH: FB4 for 3.3V (default populate); FB1 for 2.5V (default not populate)

Note: Populate either FB4 only or FB1 only. If 2.5V AVDDH is desired, FB4 should be 'do not populate' (DNP) and FB1 should be populated.

Remove the above ferrite beads and place the current probes in series across the power probe points ([Section 2.2.1 “Power Probe Points”](#)) that are joined by the ferrite beads. See also [Appendix B. “EVB-KSZ8563 Schematics”](#).

Board LED components are connected to the VDDIO power rail, and thus the measured current is higher than the amount consumed by only the KSZ8563 device.

2.3 CLOCK

The EVB-KSZ8563 utilizes the on-board Microchip DSC1001CI2-025.0000 clock chip, a 25-MHz MEMS oscillator, as the input reference clock to the KSZ8563 device. Refer to [Figure 2-1](#) and board schematics in [Appendix B. “EVB-KSZ8563 Schematics”](#) for details.

2.4 RESET

2.4.1 Power-On Reset

The discrete RC/Diode (R12, C8, D3) circuit provides power-on reset to the KSZ8563 device.

2.4.2 Manual Reset

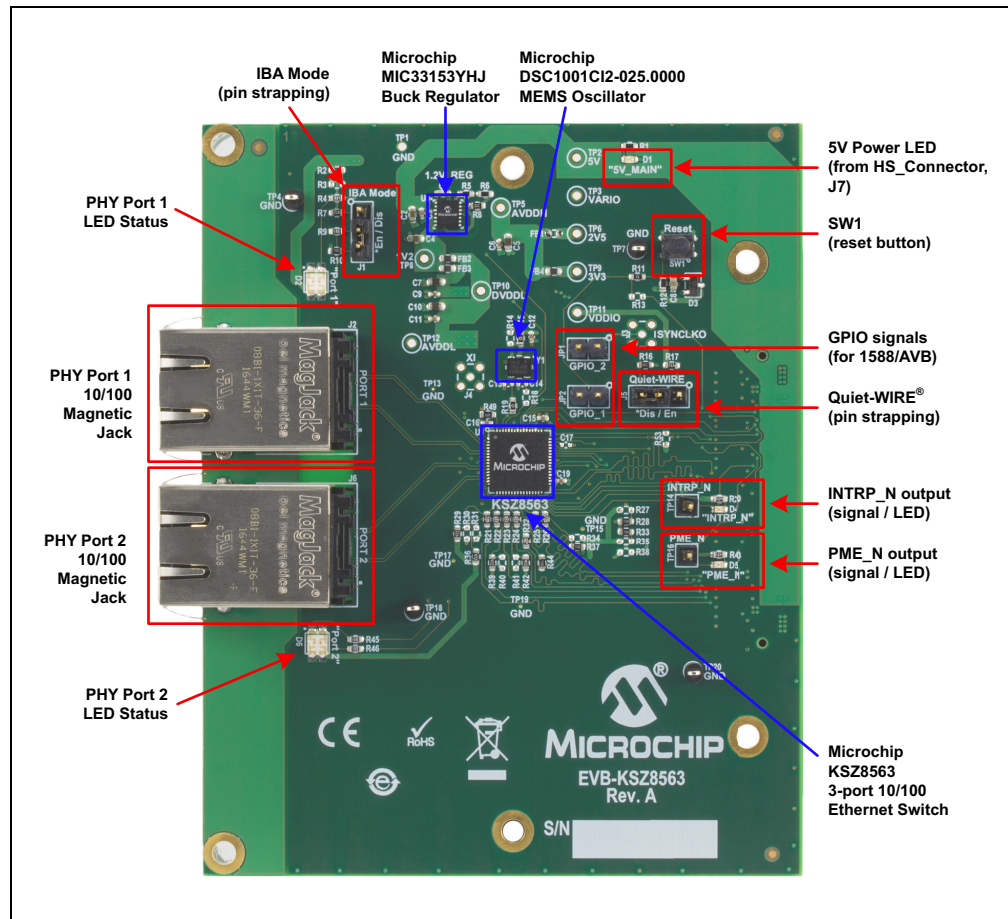
The SW1 reset button can be pressed and released to provide manual reset to the KSZ8563 device after power-up. Refer to [Figure 2-1](#) and board schematics in [Appendix B. "EVB-KSZ8563 Schematics"](#) for details.

2.5 BOARD FEATURES AND CONFIGURATION

The following sub-sections describe the board features and configuration settings.

[Figure 2-1](#) displays the top view of the EVB-KSZ8563 with key features, jumpers, and headers highlighted in red, and with Microchip components highlighted in blue.

FIGURE 2-1: EVB-KSZ8563 TOP VIEW WITH CALLOUTS



Board Details and Configuration

Figure 2-2 displays the power probe points along with the ground test points.

FIGURE 2-2: EVB-KSZ8563 POWER/GROUND CALLOUTS

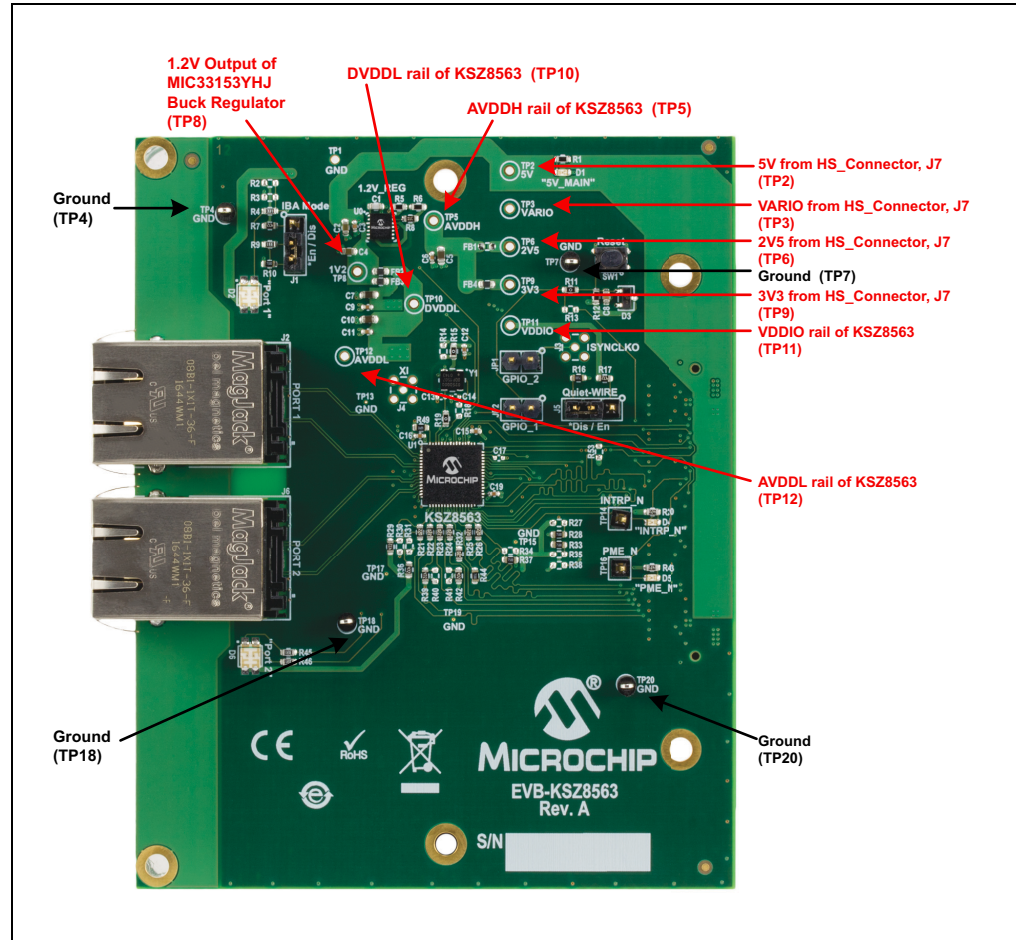
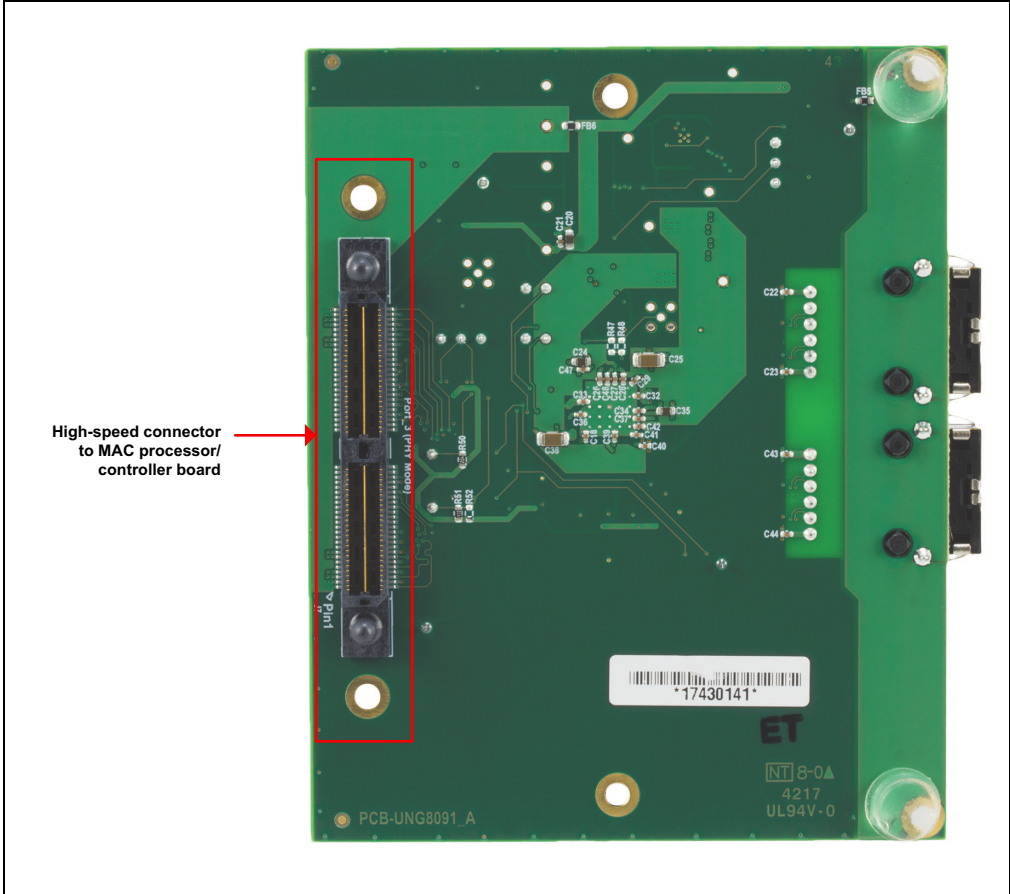


Figure 2-3 displays the bottom view of the EVB-KSZ8563 with the HS connector (J7) (highlighted in red) that plugs directly into a mating Microchip MAC processor or controller board.

FIGURE 2-3: EVB-KSZ8563 BOTTOM VIEW WITH CALLOUT



Board Details and Configuration

2.5.1 PHY Ports - Integrated Magnetic Jacks

PHY ports 1 and 2 (J2 and J6) support 10BASE-T/100BASE-TX with both Auto-Negotiation and Auto MDI/MDI-X enabled as the power-up defaults.

2.5.2 PHY Ports - LEDs

Two Dual-LEDs (D2 and D6) provide the link status for PHY ports 1 and 2, respectively. The LED descriptions are listed in [Table 2-1](#).

TABLE 2-1: PHY PORTS - LED DESCRIPTION

LED	LED Color	Description
D2, D6	Red	Solid Color: 100-Mbps Link Blinking: Activity (RX, TX)
	Orange	Solid Color: 10-Mbps Link Blinking: Activity (RX, TX)
	Off	Link off

2.5.3 Pin Strapping Configuration

As the power-up or reset defaults, the KSZ8563 device is configured via internal or external pull-up/down resistors to the following settings:

- **PHY Ports 1 and 2:** Auto-Negotiation enabled and Energy-Efficient Ethernet (EEE) enabled
- **MAC Port 3:** RGMII Mode at 1000-Mbps speed
- **Start Switch:** The switch forwards the packets immediately after hardware reset.
- **Management:** SPI Slave mode

The In-band Management Access (IBA) Mode and Quiet-Wire[®] pin strappings can be enabled or disabled using the 3-pin jumpers in [Table 2-2](#). Set the desired jumper settings prior to board power-up, hardware reset, or both.

TABLE 2-2: PIN STRAPPING JUMPERS

Jumper	Label	Description	Close Pins 1-2	Close Pins 2-3
J1	IBA Mode	IBA provides full register read and write access via any one of the three data ports. When enabled by pin strapping, IBA defaults to PHY port 1. SPI or I ² C management access is required to enable IBA for MAC port 3 or PHY port 2.	Disable	Enable (default)
J5	Quiet-Wire	Quiet-Wire filtering is implemented on-chip to enhance 100BASE-TX EMC performance by reducing both conducted and radiated emissions from the TXP/M signal differential pair.	Enable	Disable (default)

Refer to the board schematics in [Appendix B. “EVB-KSZ8563 Schematics”](#) and the *KSZ8563 Data Sheet* for further details on the pin strappings.

2.5.4 GPIO Signal Headers

[Table 2-3](#) shows the GPIO signals that support the IEEE 1588 Precision Time Protocol (PTP).

TABLE 2-3: GPIO SIGNAL HEADERS

Header	Label	Description	Pin 1	Pin 2
JP1	GPIO_2	The GPIO_2 pin is configurable to implement IEEE1588 event trigger outputs and time stamp capture inputs to support real-time application requirements.	No Connect	GPIO_2 (KSZ8563 pin 41)
JP2	GPIO_1	The GPIO_1 pin is configurable to implement IEEE1588 event trigger outputs and time stamp capture inputs to support real-time application requirements.	Ground	GPIO_1 (KSZ8563 pin 40)

Refer to the board schematics in [Appendix B. “EVB-KSZ8563 Schematics”](#) and the *KSZ8563 Data Sheet* for further details and usage on the GPIO signal pins.

2.5.5 INTRP_N Output

The INTRP_N output at test point TP14 provides the interrupt output from the KSZ8563 device. By default, it is active low and drives low to turn on D4 when asserted.

Refer to board schematics in [Appendix B. “EVB-KSZ8563 Schematics”](#) and *KSZ8563 Data Sheet* for further details and usage on the INTRP_N signal.

2.5.6 PME_N Output

The PME_N output at test point TP16 provides the Power Management Event (PME) interrupt output for Wake-on-LAN (WoL) from the KSZ8563 device. By default, it is active low and drives low to turn on D5 when asserted.

Refer to the board schematics in [Appendix B. “EVB-KSZ8563 Schematics”](#) and the *KSZ8563 Data Sheet* for further details and usage on the PME_N signal.

2.6 USING THE EVB-KSZ8563

The EVB-KSZ8563 plugs in directly to a mating Microchip host controller or processor board, such as the SAMA5D3-EDS Board, that delivers full power and provides full register access and configuration via IBA, SPI, or I²C bus management.

Together, the EVB-KSZ8563 and the SAMA5D3-EDS enable Ethernet traffic switching across all three data ports of the KSZ8563 device with RGMII MAC port 3 connecting to the SAMA5D3 processor and PHY ports 1 and 2 connecting via copper Ethernet cable (CAT-5 UTP or better) to external Ethernet devices.

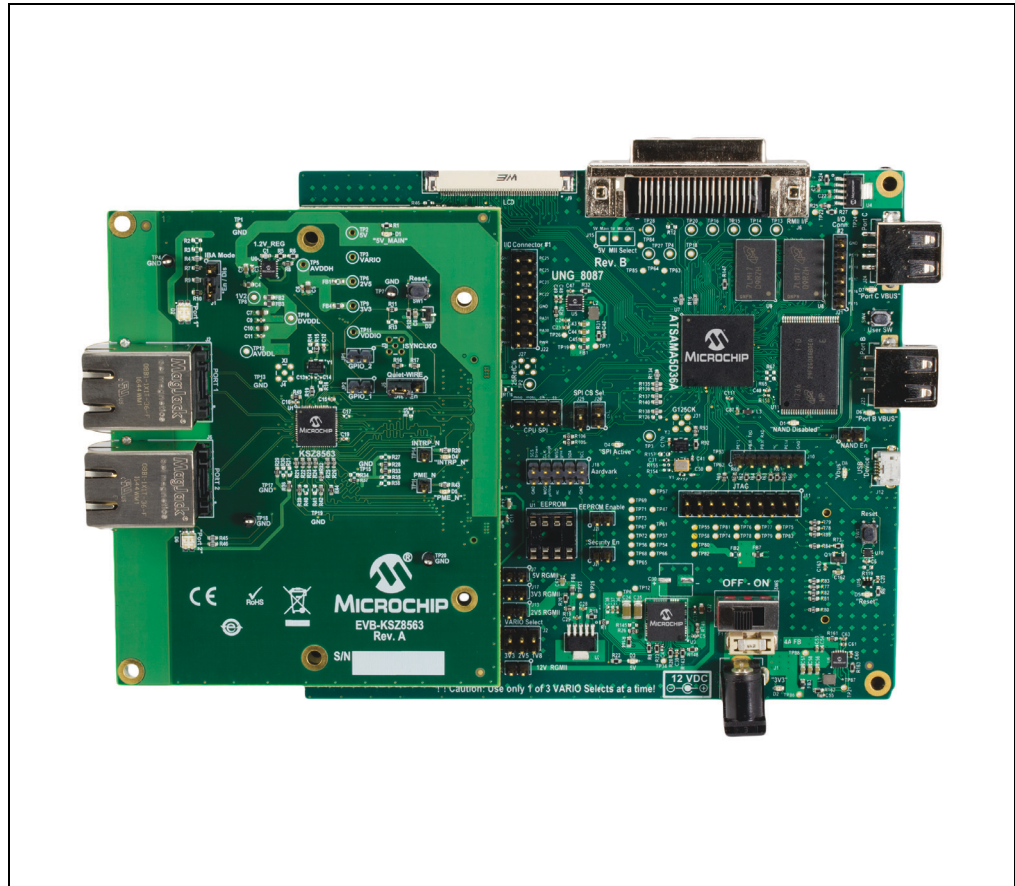
All KSZ8563 registers are accessible via IBA, SPI, or I²C bus management from the SAMA5D3-EDS Board, enabling full evaluation and firmware development for all KSZ8563 MAC/Switch features and interaction with upper network layers.

Refer to SAMA5D3-EDS Board documentation on its usage.

[Figure 2-4](#) shows the EVB-KSZ8563 connected to the SAMA5D3-EDS Board.

Board Details and Configuration

FIGURE 2-4: EVB-KSZ8563/SAMA5D3-EDS EVALUATION AND FIRMWARE DEVELOPMENT PLATFORM



NOTES:

Appendix A. EVB-KSZ8563 Evaluation Board

A.1 INTRODUCTION

This appendix shows the EVB-KSZ8563 evaluation board.

FIGURE A-1: EVB-KSZ8563 EVALUATION BOARD (TOP VIEW)

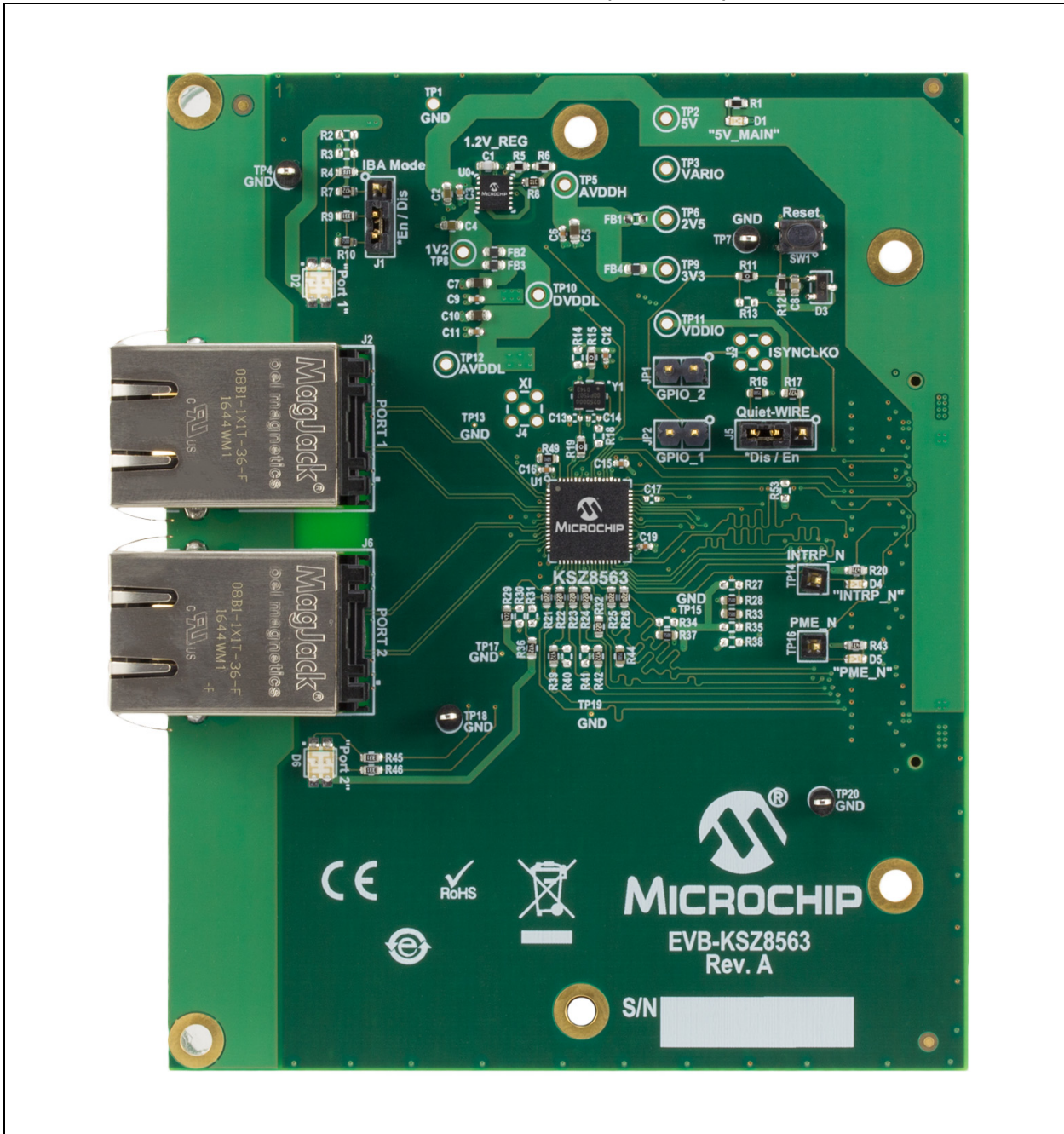
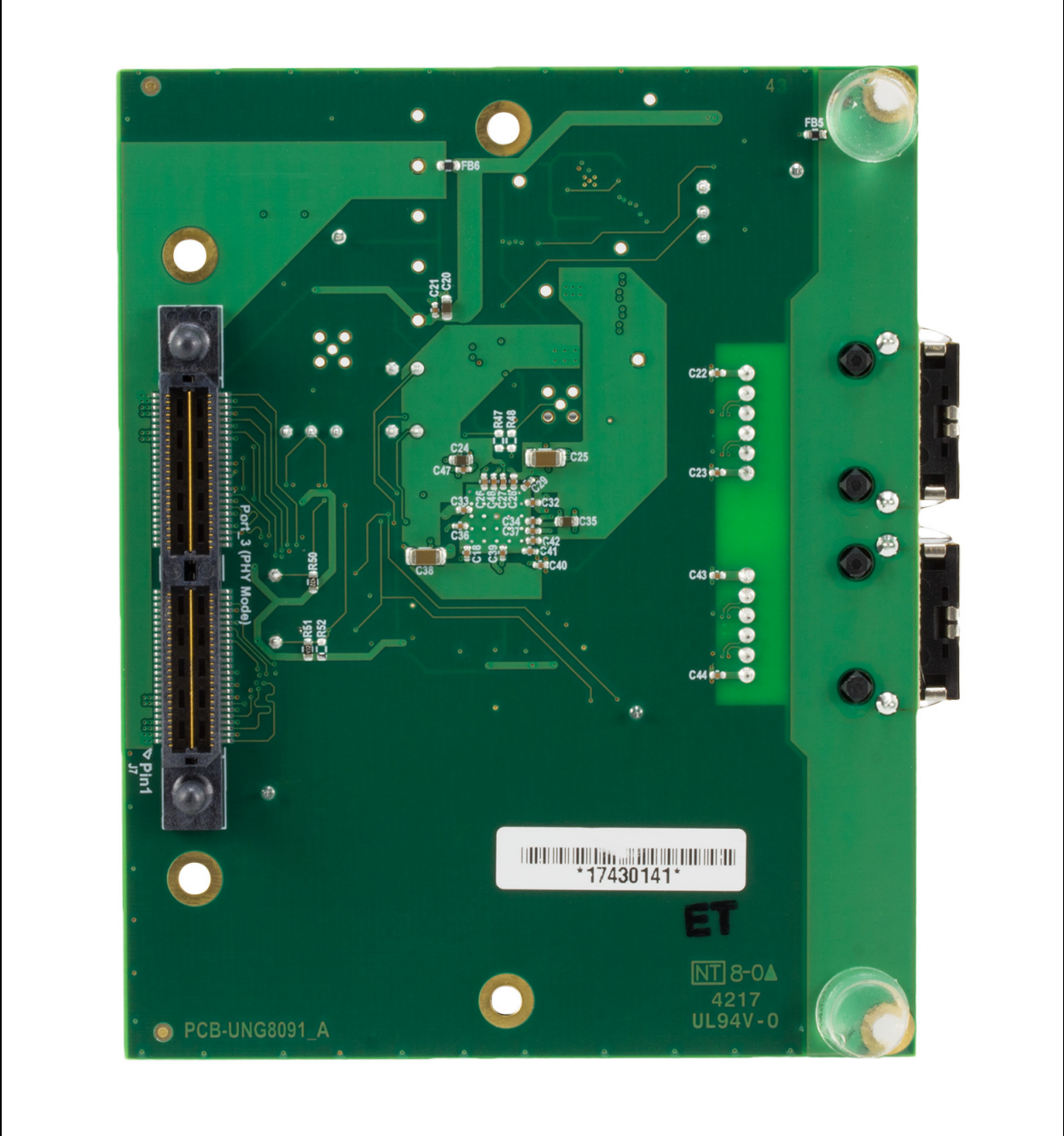


FIGURE A-2: EVB-KSZ8563 EVALUATION BOARD (BOTTOM VIEW)



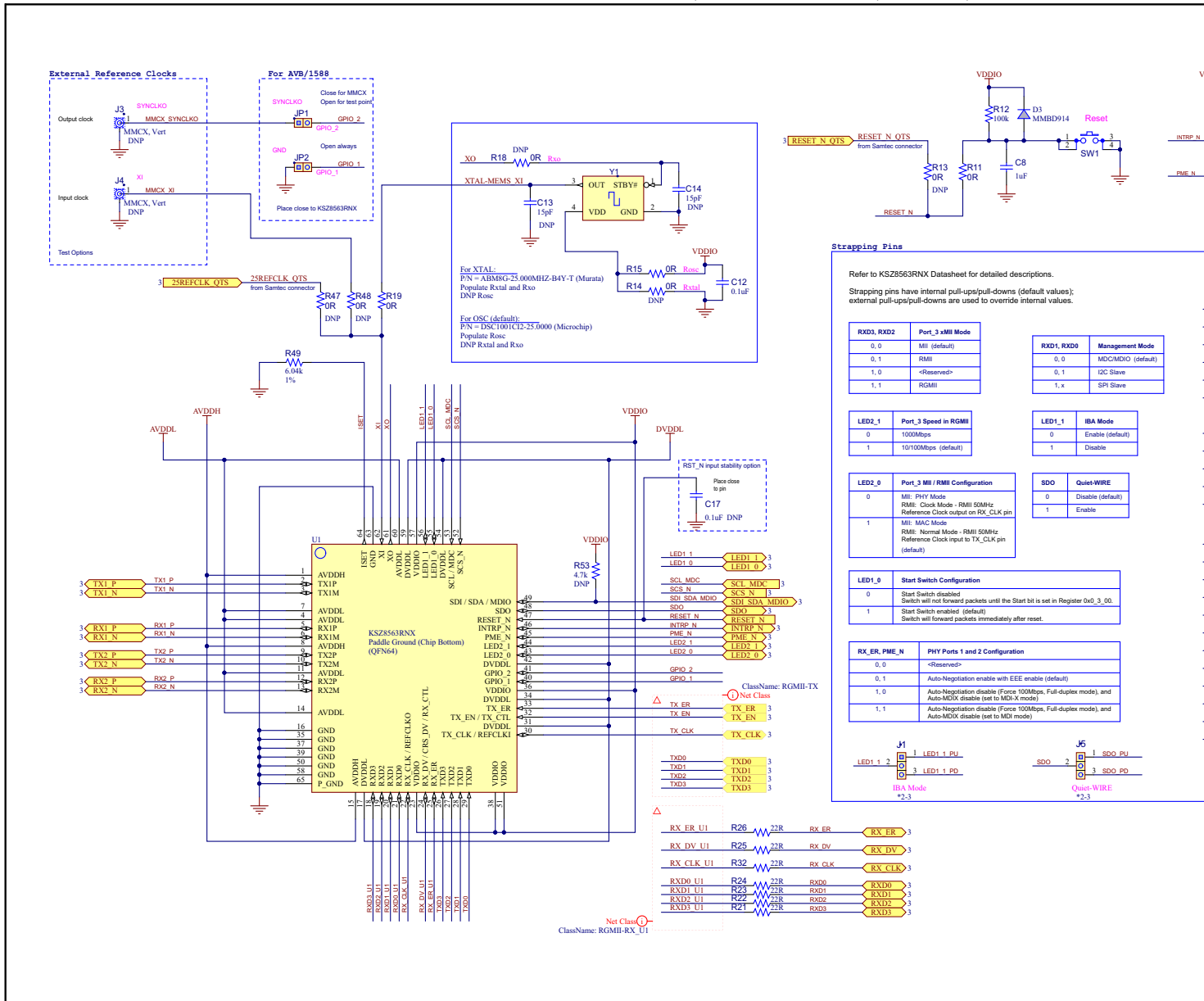


Appendix B. EVB-KSZ8563 Schematics

B.1 INTRODUCTION

This appendix includes the EVB-KSZ8563 schematics.

FIGURE B-1: EVB-KS28563 SCHEMATICS - KS28563 DEVICE, PIN STRAPPING, CLOCK, AND RESET



Strapping Pins

Refer to KS28563RNX Datasheet for detailed descriptions. Strapping pins have internal pull-ups/pull-downs (default values); external pull-ups/pull-downs are used to override internal values.

RXD1, RXD2	Port_3 xMI Mode	RXD1, RXD0	Management Mode
0, 0	MII (default)	0, 0	MDC/Mdio (default)
0, 1	RMI	0, 1	1GC Slave
1, 0	<Reserved>	1, x	SPI Slave
1, 1	RGMI		

LED2_1	Port_3 Speed in RGMII	LED1_1	1BA Mode
0	1000Mbps	0	Enable (default)
1	10/100Mbps (default)	1	Disable

LED2_0	Port_3 MII /RMI Configuration	SDO	Quiet-WIRE
0	MII: PHY Mode RMI: Clock Mode - RMI 50MHz Reference Clock output on RX_CLK pin	0	Disable (default)
1	MII: MAC Mode RMI: Normal Mode - RMI 50MHz Reference Clock input to TX_CLK pin (default)	1	Enable

LED1_0	Start Switch Configuration
0	Start Switch disabled Switch will not forward packets until the Start bit is set in Register 0x0_3_00.
1	Start Switch enabled (default) Switch will forward packets immediately after reset.

RX_ER, PME_N	PHY Ports 1 and 2 Configuration
0, 0	<Reserved>
0, 1	Auto-Negotiation enable with EEE enable (default)
1, 0	Auto-Negotiation disable (Force 100Mbps, Full-duplex mode), and Auto-MDIX disable (set to MDI-x mode)
1, 1	Auto-Negotiation disable (Force 100Mbps, Full-duplex mode), and Auto-MDIX disable (set to MDI mode)

J1 LED1_1 PU
J2 LED1_1 PD
J3 LED1_1 PD
J4 LED1_1 PU
J5 SDO PU
J6 SDO PD
 IBA Mode *+3
 Quiet-WIRE *+3

FIGURE B-2: EVB-KS28563 SCHEMATICS - PORTS 1, 2 PHYS; PORT 3 MAC - MII/RMII/RGMII CONNECTOR

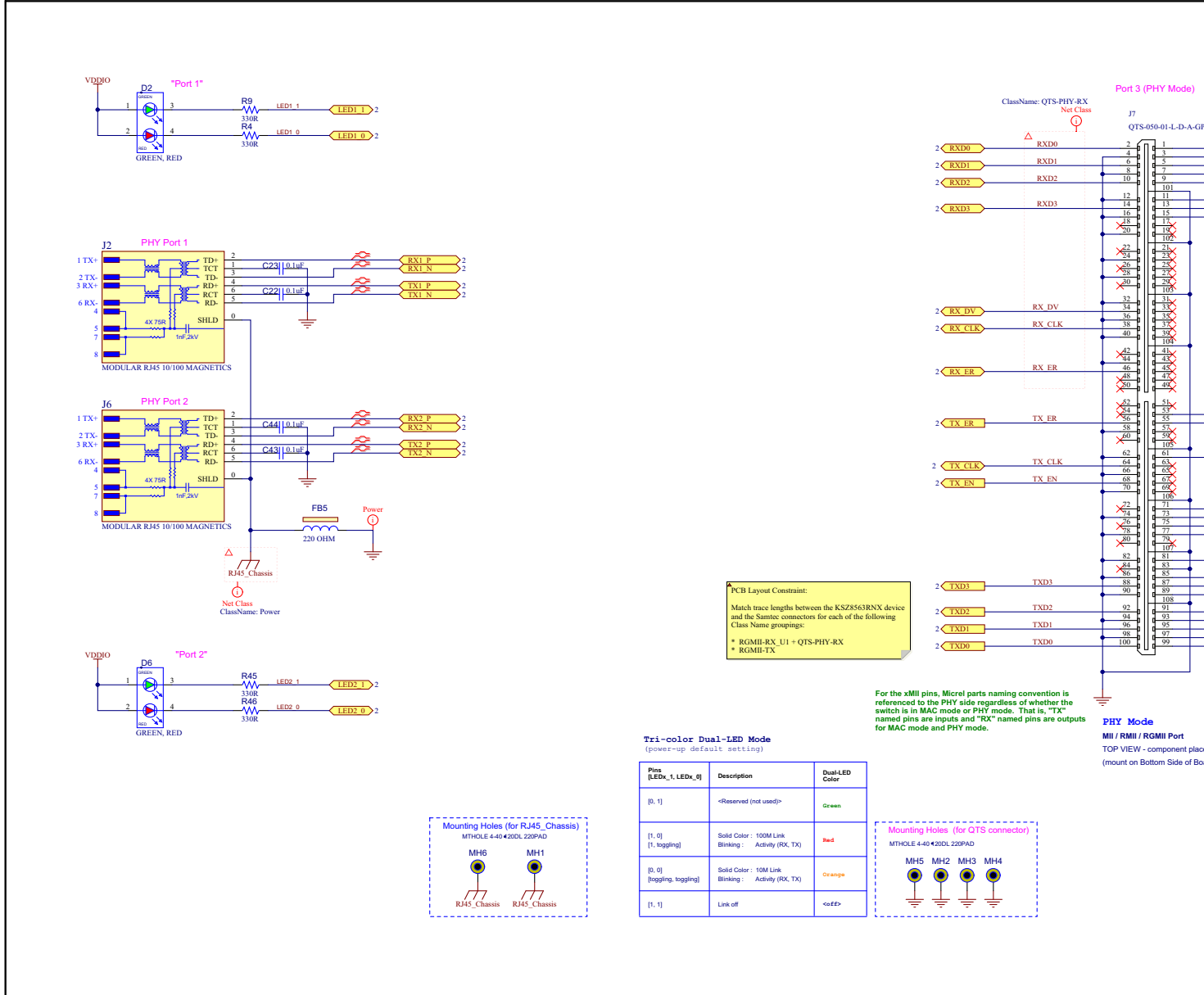
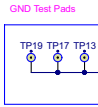
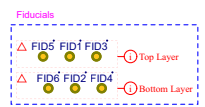
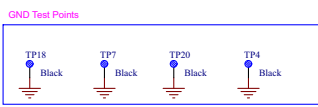
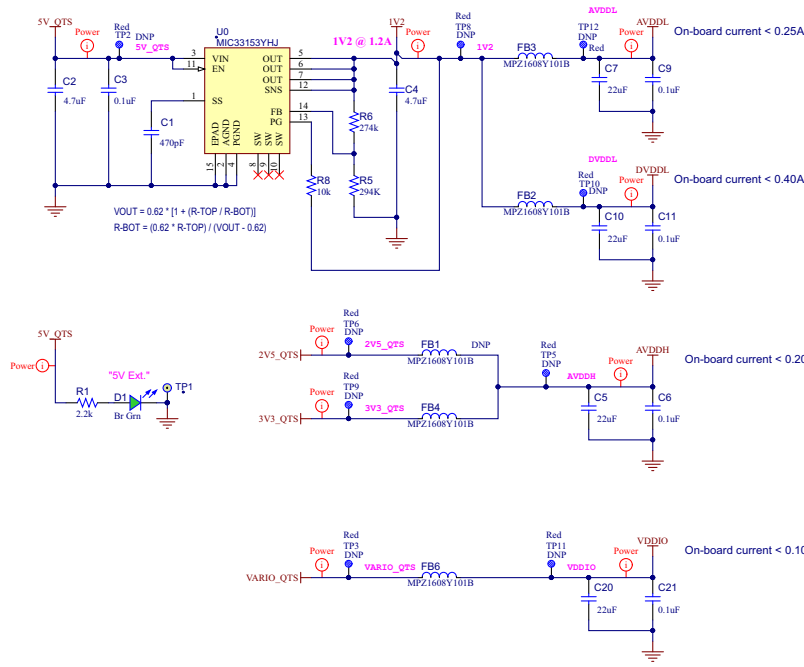


FIGURE B-3: EVB-KSZ8563 SCHEMATICS - BOARD POWER I/O AND REGULATORS





Appendix C. EVB-KSZ8563 Bill of Materials (BOM)

C.1 INTRODUCTION

This appendix includes the EVB-KSZ8563 Bill of Materials (BOM).

FIGURE C-1: BILL OF MATERIALS

Item	Qty	Reference	Description	Populated	Manufacturer	
1	2	C13, C14	CAP CER 15 pF 50V 5% NP0 SMD 0402	YES	Murata	GRN
2	1	C1	CAP CER 470 pF 25V 5% NP0 SMD 0603	YES	AVX	060
3	2	C2, C4	CAP CER 4.7 uF 10V 10% X5R SMD 0603	YES	KEMET	C06
4	22	C3, C6, C9, C11, C15, C16, C18, C19, C21, C26, C27, C28, C29, C32, C33, C34, C36, C37, C39, C40, C41, C42	CAP CER 0.1 uF 50V 10% X7R SMD 0402	YES	TDK Corporation	C10
5	6	C5, C7, C10, C20, C24, C35	CAP CER 22 uF 10V 20% X5R SMD 0603	YES	TDK Corporation	C16
6	1	C8	CAP CER 1 uF 16V 10% X5R SMD 0603	YES	AVX	060
7	7	C12, C22, C23, C43, C44, C47, C48	CAP CER 0.1 uF 50V 10% X7R SMD 0402	YES	TDK Corporation	C10
8	2	C25, C38	CAP CER 22 uF 10V 20% X5R SMD 1206	YES	Taiyo Yuden	LMP
9	3	D1, D4, D5	LED, Bright Green, 0603	YES	Lite-On	LTS
10	2	D2, D6	DIO LED BI GREEN, RED 2V 30 mA 1210	YES	Lite-On	LTS
11	1	D3	DIO RECT MMBD914LT1G 1V 10 mA 100V SMD SOT-23-3	YES	ON Semiconductor	MM
12	4	FB2, FB3, FB4, FB6	FERRITE CHIP 100 OHM 2A 0603	YES	TDK Corporation	MP2
13	1	FB5	FERRITE 500 mA 220R SMD 0603	YES	Murata Electronics North America	BLM
14	2	J1, J5	HDR 3POS 100" SGL GOLD	YES	Samtec Inc.	TSV
15	2	J2, J6	CON MODULAR RJ45 MAGJACK TH R/A, NO LED	YES	Bel Fuse Inc.	08B
16	2	JP1, JP2	CON HDR-2.54 MALE 1x2 GOLD 5.84 MH TH VERT	YES	FCI	680
17	1	R1	RES TKF 2.2k 1% 1/10W SMD 0603	YES	Panasonic	ERJ
18	4	R4, R9, R45, R46	RES TKF 330R 5% 1/10W SMD 0603	YES	Panasonic Electronic Components	ERJ
19	1	R5	RES TKF 294K 1% 1/10W SMD 0603	YES	Panasonic Electronic Components	ERJ
20	1	R6	RES TKF 274K 1% 1/10W SMD 0603	YES	Panasonic Electronic Components	ERJ
21	8	R7, R17, R29, R36, R39, R42, R50, R51	RES TKF 4.7k 5% 1/10W SMD 0603	YES	Yageo	RCC
22	1	R8	RES TKF 10k 5% 1/10W SMD 0603	YES	Panasonic	ERJ
23	6	R10, R16, R28, R33, R37, R44	RES TKF 750R 1% 1/10W SMD 0603	YES	Vishay	CR0
24	4	R11, R14, R18, R19	RES TKF 0R 1/10W SMD 0603	YES	NIC Components	NR0
25	1	R12	RES TKF 100k 1% 1/10W SMD 0603	YES	Panasonic	ERJ
26	2	R20, R43	RES TKF 470R 5% 1/10W SMD 0603	YES	Panasonic	ERJ
27	7	R21, R22, R23, R24, R25, R26, R32	RES TKF 22R 1% 1/10W SMD 0603	YES	Yageo	RCC
28	1	R49	RES TKF 6.04k 1% 1/10W SMD 0603	YES	Yageo	9T0
29	1	SW1	Switch, Tactile, SPST, 50 mA, 16VDC, J-lead, 4.2 x 3.2 mm, PTS810, NO	YES	C&K	PTS
30	4	TP4, TP7, TP18, TP20	TEST POINT PC MINI 0.040"D BLACK	YES	Keystone Electronics	500
31	2	TP14, TP16	CON HDR-2.54 MALE 1x1 GOLD 5.84 MH TH VERT	YES	Samtec	TSV

Item	Qty	Reference	Description	Populated	Manufacturer	
32	1	U1	KSZ8563RNX 3-Port 10/100 Ethernet Switch with AVB/1588	YES	Microchip Technology	KSZ
33	1	U0	IC, 2.7V to 5.5V input, 1.2A, Synchronous 4MHz Buck Regulator with adjustable output	YES	Microchip Technology	MIC
34	1	J7	SAMTEC - QTS-050-01-L-D-A-GP -0.635 mm DOUBLE ROW HS SOCKET ASSEMBLY	YES	SAMTEC	QTS
35	1	Y1	CRYSTAL 25 MHz 10 pF SMD ABM8G	YES	Abracon LLC	ABM
36	0	C13, C14	CAP CER 15 pF 50V 5% NP0 SMD 0402	NO	Murata	GR
37	0	C17	CAP CER 0.1 uF 50V 10% X7R SMD 0402	NO	TDK Corporation	C10
38	0	FB1	FERRITE CHIP 100 OHM 2A 0603	NO	TDK Corporation	MP2
39	0	J3, J4	CONN MMCX JACK STR 50 OHM PCB	NO	Cinch Connectivity Solutions Johnson	135
40	0	R2, R27, R34, R35, R52, R53	RES TKF 4.7k 5% 1/10W SMD 0603	NO	Yageo	RC
41	0	R3, R30, R31, R38, R40, R41	RES TKF 750R 1% 1/10W SMD 0603	NO	Vishay	CR
42	0	R13, R15, R47, R48	RES TKF 0R 1/10W SMD 0603	NO	NIC Components	NR
43	0	TP2, TP3, TP5, TP6, TP8, TP9, TP10, TP11, TP12	TEST POINT PC MINI 0.040"D RED	NO	Keystone Electronics	500

NOTES:

Appendix D. EVB-KSZ8563 Silk Screen

D.1 INTRODUCTION

This appendix shows the EVB-KSZ8563 top and bottom silk screen images.

FIGURE D-1: EVB-KSZ8563 TOP SILK SCREEN

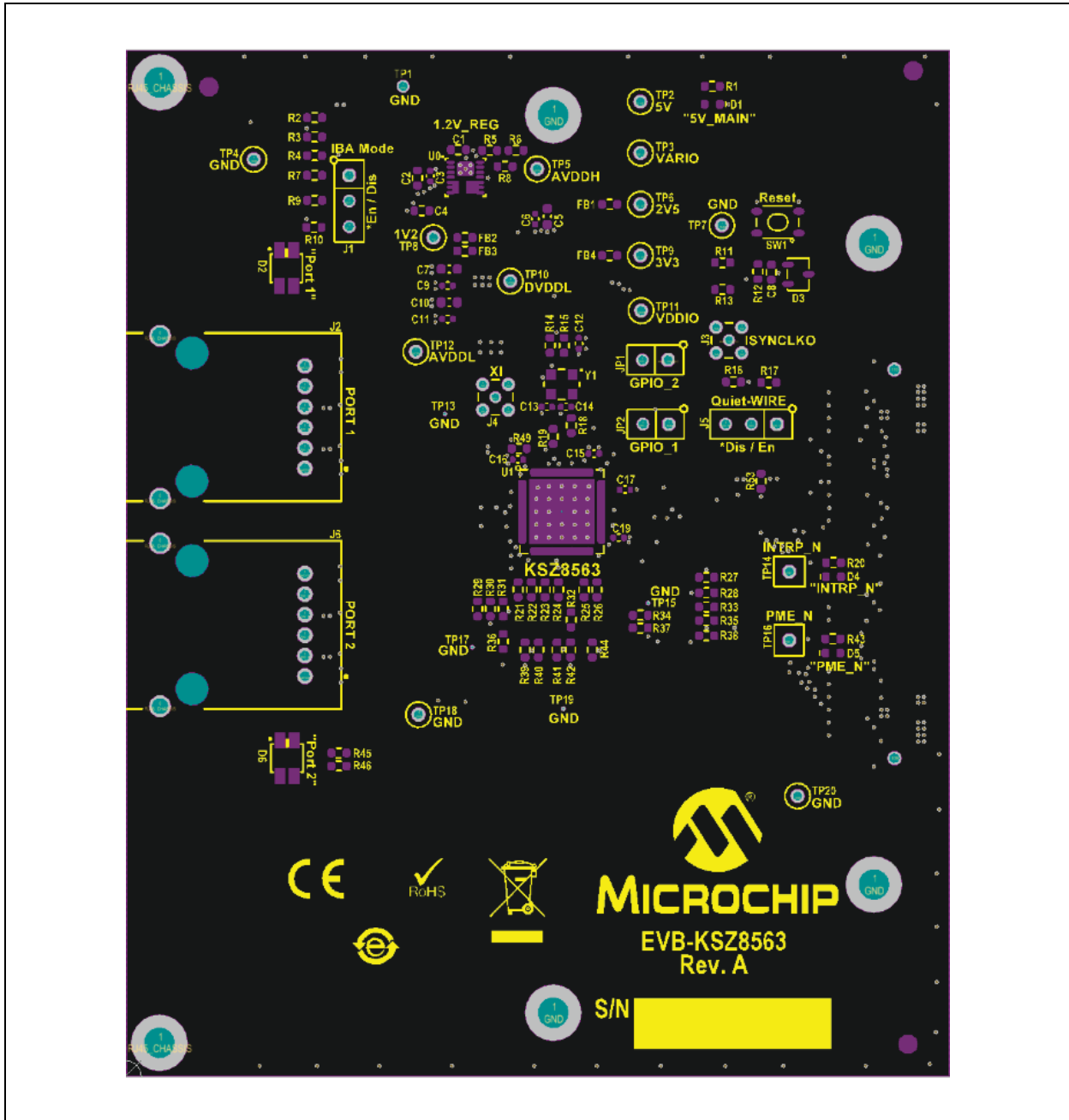
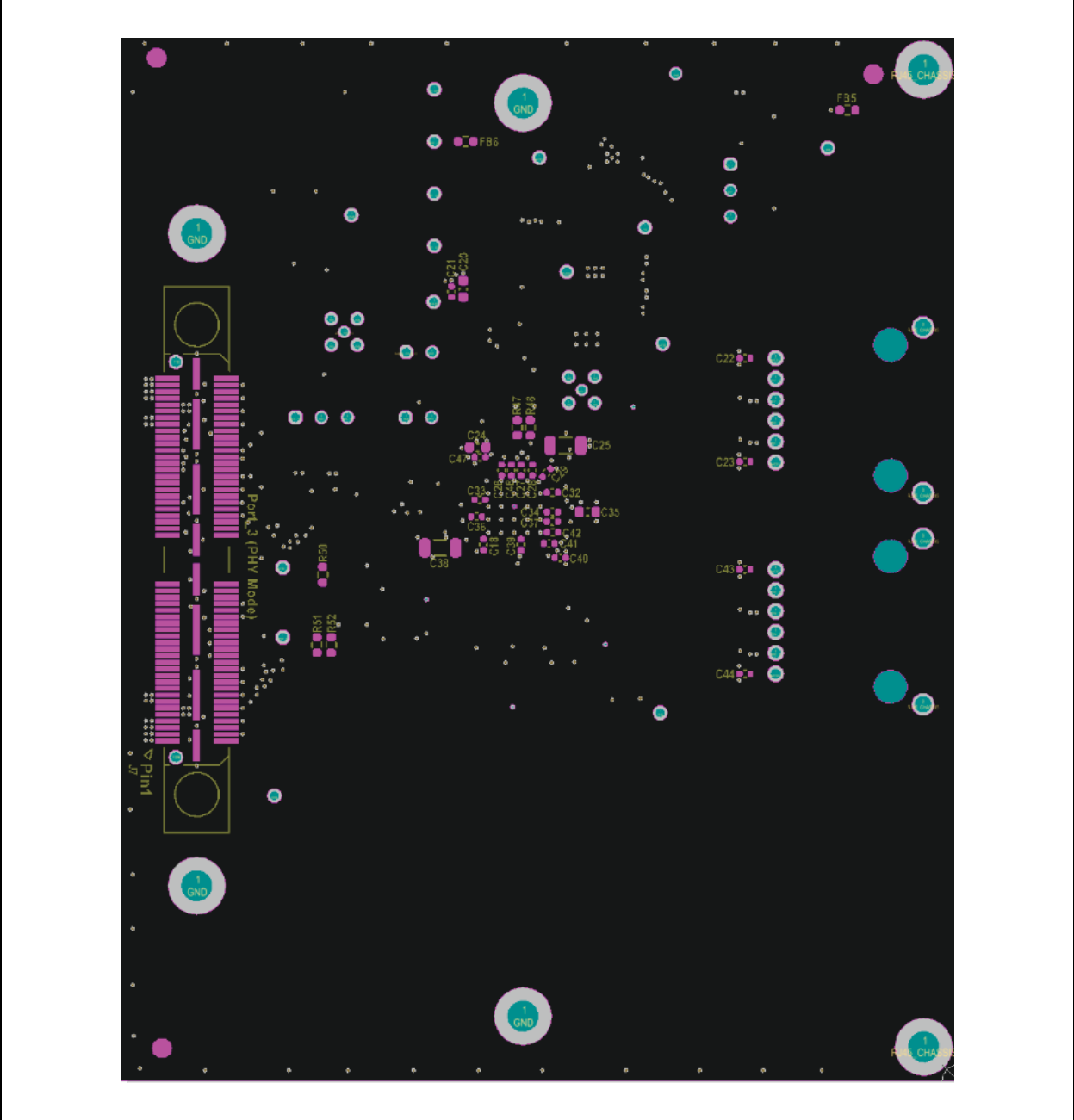


FIGURE D-2: EVB-KSZ8563 BOTTOM SILK SCREEN



NOTES:



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