HCS200

KEELOQ® Code Hopping Encoder

FEATURES

Security

- Programmable 28-bit serial number
- Programmable 64-bit crypt key
- Each transmission is unique
- 66-bit transmission code length
- 32-bit hopping code
- 28-bit serial number, 4-bit button status, low battery indicator transmitted
- Crypt keys are read protected

Operating

- 3.5–13.0V operation
- Three button inputs - seven functions available
- Selectable baud rate
- Automatic code word completion
- Low battery signal transmitted to receiver
- Non-volatile synchronization data

Other

- Easy to use programming interface
- On-chip EEPROM
- On-chip oscillator and timing components
- Button inputs have internal pull-down resistors
- Low external component cost

Typical Applications

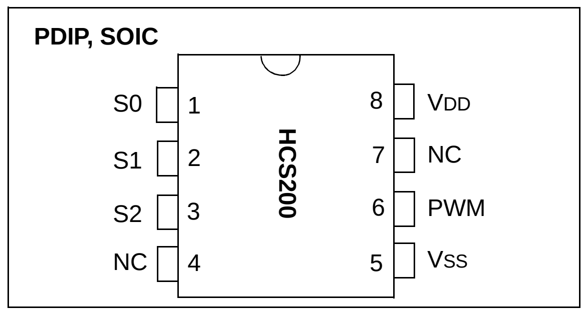
The HCS200 is ideal for Remote Keyless Entry (RKE) applications. These applications include:

- Fixed code replacement
- Automotive RKE systems
- Automotive alarm systems
- Automotive immobilizers
- Gate and garage door openers
- Identity tokens
- Burglar alarm systems

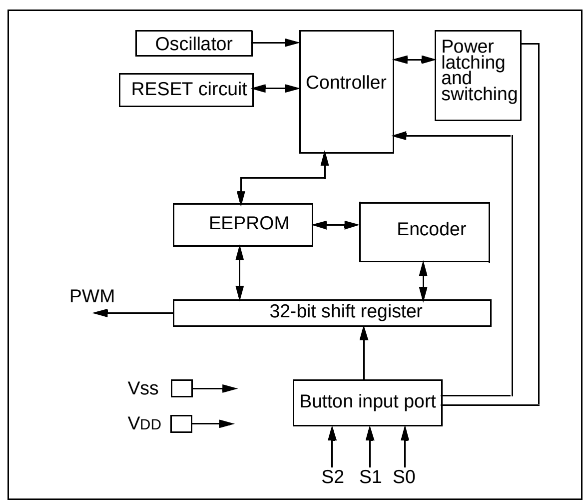
DESCRIPTION

The HCS200 from Microchip Technology Inc. is a code hopping encoder designed primarily for Remote Keyless Entry (RKE) systems. The device utilizes the KEELOQ® code hopping technology, incorporating high security, a small package outline and low cost. The HCS200 is a perfect replacement of fixed code devices in unidirectional remote keyless entry systems and access control systems.

PACKAGE TYPES



BLOCK DIAGRAM



The HCS200 operates over a wide voltage range of 3.5 volts to 13.0 volts and has three button inputs in an 8-pin configuration. This allows the system designer the freedom to implement up to seven functions. The only components required for device operation are the buttons and RF circuitry, allowing a very low system cost.

The HCS200 combines a 32-bit hopping code, generated by a non-linear encryption algorithm, with a 28-bit serial number and 6 information bits to create a 66-bit code word. The code word length eliminates the threat of code scanning and the code hopping mechanism makes each transmission unique, thus rendering code capture and resend schemes useless.

The crypt key, serial number and configuration data are stored in an EEPROM array which is not accessible via any external connection. The EEPROM data is programmable but read-protected. The data can be verified only after an automatic erase and programming operation. This protects against attempts to gain access to keys or manipulate synchronization values. The HCS200 provides an easy to use serial interface for programming the necessary keys, system parameters and configuration data.

1.0 SYSTEM OVERVIEW

Key Terms

The following is a list of key terms used throughout this data sheet. For additional information on KEELOQ and Code Hopping, refer to Technical Brief 3 (TB003).

- **RKE** - Remote Keyless Entry
- **Button Status** - Indicates what button input(s) activated the transmission. Encompasses the 4 button status bits S3, S2, S1 and S0 (Figure 4-2).
- **Code Hopping** - A method by which a code, viewed externally to the system, appears to change unpredictably each time it is transmitted.
- **Code word** - A block of data that is repeatedly transmitted upon button activation (Figure 4-1).
- **Transmission** - A data stream consisting of repeating code words (Figure 8-2).
- **Crypt key** - A unique and secret 64-bit number used to encrypt and decrypt data. In a symmetrical block cipher such as the KEELOQ algorithm, the encryption and decryption keys are equal and will therefore be referred to generally as the crypt key.
- **Encoder** - A device that generates and encodes data.
- **Encryption Algorithm** - A recipe whereby data is scrambled using a crypt key. The data can only be interpreted by the respective decryption algorithm using the same crypt key.
- **Decoder** - A device that decodes data received from an encoder.
- **Decryption algorithm** - A recipe whereby data scrambled by an encryption algorithm can be unscrambled using the same crypt key.
- **Learn** – Learning involves the receiver calculating the transmitter's appropriate crypt key, decrypting the received hopping code and storing the serial number, synchronization counter value and crypt key in EEPROM. The KEELOQ product family facilitates several learning strategies to be implemented on the decoder. The following are examples of what can be done.
  - **Simple Learning**
    The receiver uses a fixed crypt key, common to all components of all systems by the same manufacturer, to decrypt the received code word's encrypted portion.
  - **Normal Learning**
    The receiver uses information transmitted during normal operation to derive the crypt key and decrypt the received code word's encrypted portion.
  - **Secure Learn**
    The transmitter is activated through a special button combination to transmit a stored 60-bit seed value used to generate the transmitter's crypt key. The receiver uses this seed value to derive the same crypt key and decrypt the received code word's encrypted portion.
- **Manufacturer's code** – A unique and secret 64-bit number used to generate unique encoder crypt keys. Each encoder is programmed with a crypt key that is a function of the manufacturer's code. Each decoder is programmed with the manufacturer code itself.

The HCS200 code hopping encoder is designed specifically for keyless entry systems; primarily vehicles and home garage door openers. The encoder portion of a keyless entry system is integrated into a transmitter, carried by the user and operated to gain access to a vehicle or restricted area. The HCS200 is meant to be a cost-effective yet secure solution to such systems, requiring very few external components (Figure 2-1).

Most low-end keyless entry transmitters are given a fixed identification code that is transmitted every time a button is pushed. The number of unique identification codes in a low-end system is usually a relatively small number. These shortcomings provide an opportunity for a sophisticated thief to create a device that 'grabs' a transmission and retransmits it later, or a device that quickly 'scans' all possible identification codes until the correct one is found.

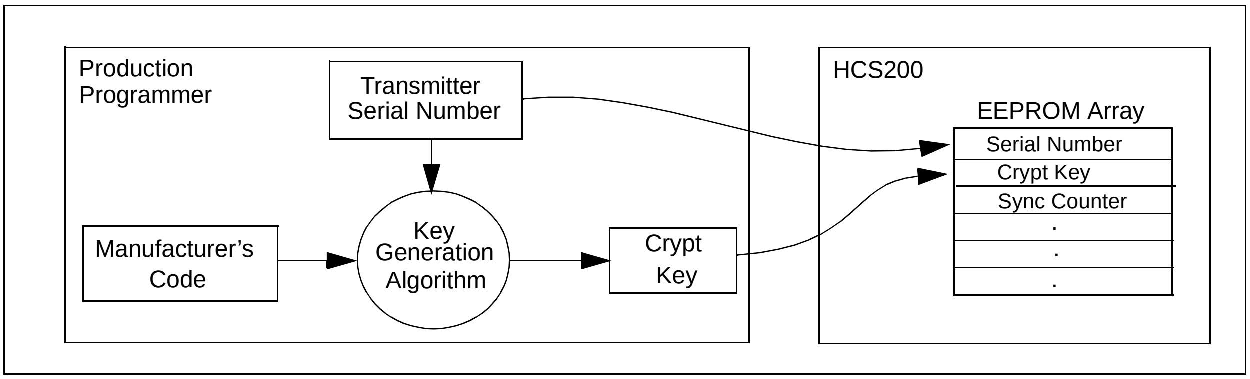
The HCS200, on the other hand, employs the KEELOQ code hopping technology coupled with a transmission length of 66 bits to virtually eliminate the use of code 'grabbing' or code 'scanning'. The high security level of the HCS200 is based on the patented KEELOQ technology. A block cipher based on a block length of 32 bits and a key length of 64 bits is used. The algorithm obscures the information in such a way that even if the transmission information (before coding) differs by only one bit from that of the previous transmission, the next coded transmission will be completely different. Statistically, if only one bit in the 32-bit string of information changes, greater than 50 percent of the coded transmission bits will change.

As indicated in the block diagram on page one, the HCS200 has a small EEPROM array which must be loaded with several parameters before use; most often programmed by the manufacturer at the time of production. The most important of these are:

- A 28-bit serial number, typically unique for every encoder
- A crypt key
- An initial 16-bit synchronization value
- A 16-bit configuration value

The crypt key generation typically inputs the transmitter serial number and 64-bit manufacturer's code into the key generation algorithm (Figure 1-1). The manufacturer's code is chosen by the system manufacturer and must be carefully controlled as it is a pivotal part of the overall system security.

FIGURE 1-1: CREATION AND STORAGE OF CRYPT KEY DURING PRODUCTION



The 16-bit synchronization counter is the basis behind the transmitted code word changing for each transmission; it increments each time a button is pressed. Due to the code hopping algorithm's complexity, each increment of the synchronization value results in greater than 50% of the bits changing in the transmitted code word.

Figure 1-2 shows how the key values in EEPROM are used in the encoder. Once the encoder detects a button press, it reads the button inputs and updates the synchronization counter. The synchronization counter and crypt key are input to the encryption algorithm and the output is 32 bits of encrypted information. This data will change with every button press, its value appearing externally to 'randomly hop around', hence it is referred to as the hopping portion of the code word. The 32-bit hopping code is combined with the button information and serial number to form the code word transmitted to the receiver. The code word format is explained in greater detail in Section 4.0.

A receiver may use any type of controller as a decoder, but it is typically a microcontroller with compatible firmware that allows the decoder to operate in conjunction with an HCS200 based transmitter. Section 7.0 provides detail on integrating the HCS200 into a system.

A transmitter must first be 'learned' by the receiver before its use is allowed in the system. Learning includes calculating the transmitter's appropriate crypt key, decrypting the received hopping code and storing the serial number, synchronization counter value and crypt key in EEPROM.

In normal operation, each received message of valid format is evaluated. The serial number is used to determine if it is from a learned transmitter. If from a learned transmitter, the message is decrypted and the synchronization counter is verified. Finally, the button status is checked to see what operation is requested. Figure 1-3 shows the relationship between some of the values stored by the receiver and the values received from the transmitter.

FIGURE 1-2: BUILDING THE TRANSMITTED CODE WORD (ENCODER)

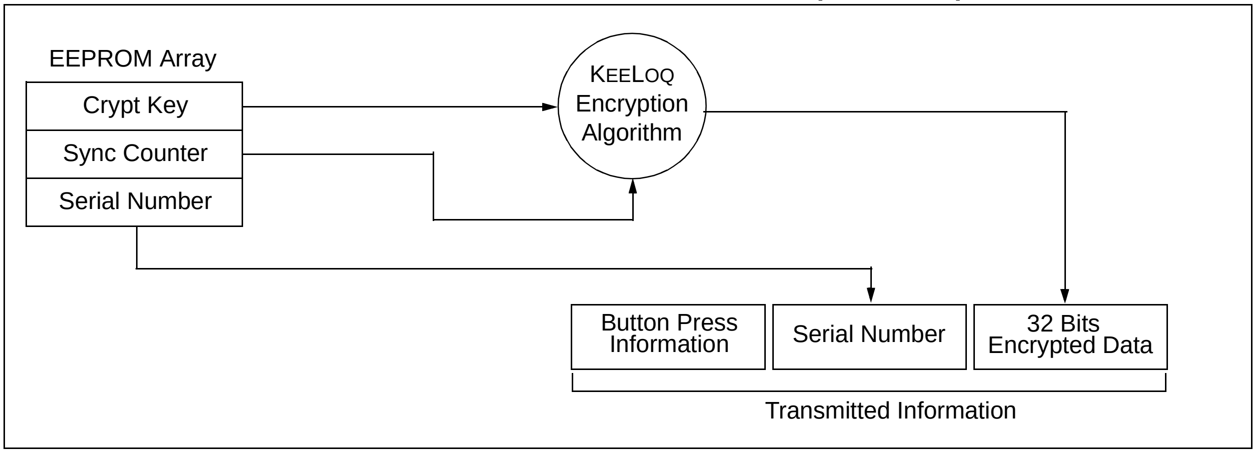
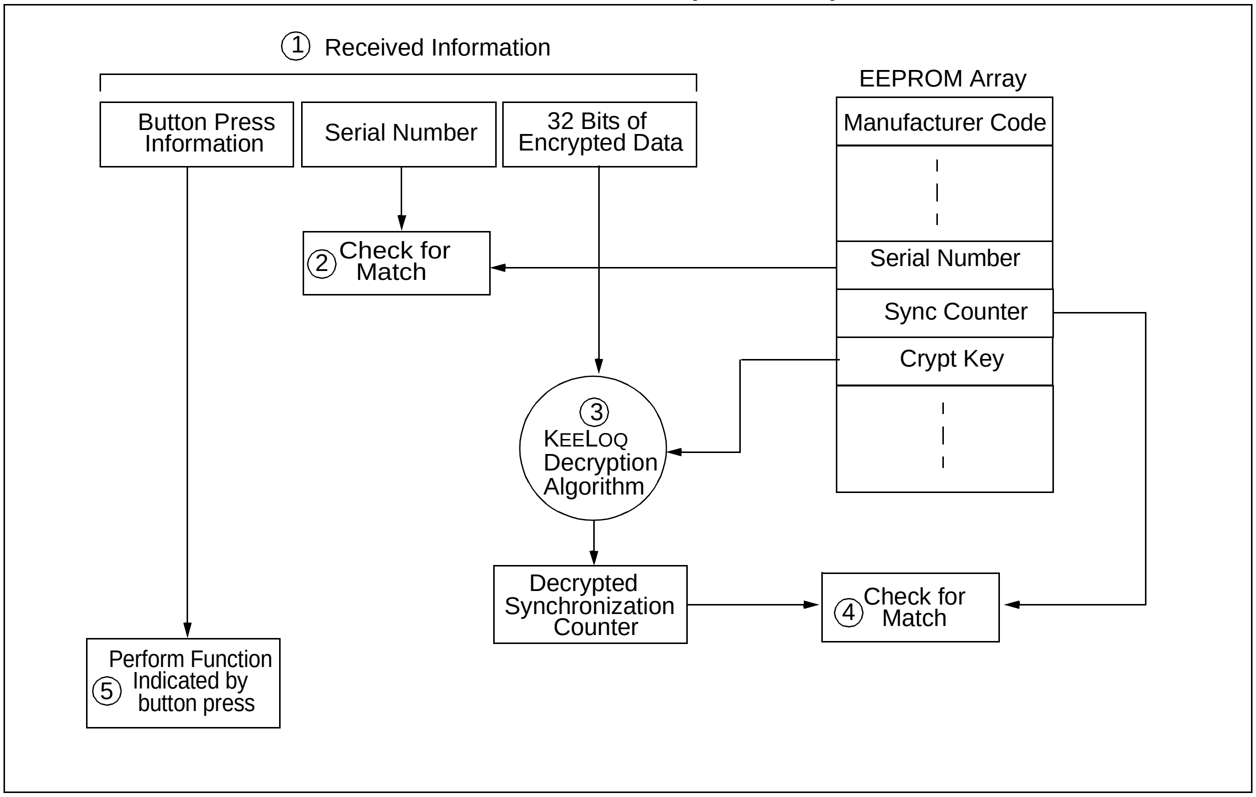


FIGURE 1-3: BASIC OPERATION OF RECEIVER (DECODER)



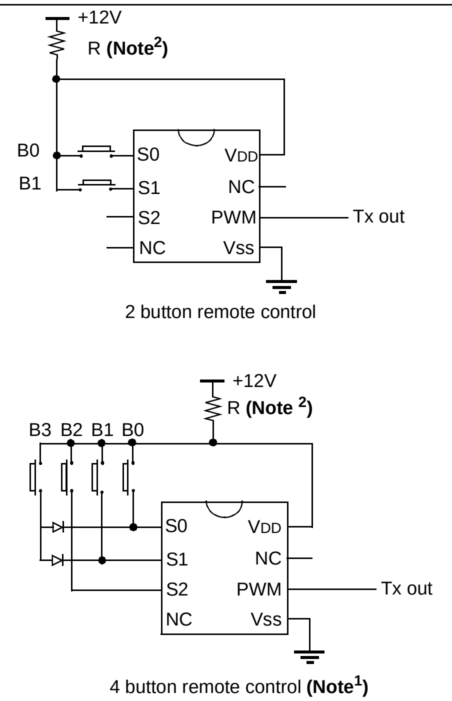
NOTE: Circled numbers indicate the order of execution.

2.0 ENCODER OPERATION

As shown in Figure 2-1, the HCS200 is a simple device to use. It requires only the addition of buttons and RF circuitry for use as the transmitter in your security application. A description of each pin is described in Table 2-1.

Note:	When VDD > 9.0V and driving low capacitive loads, a resistor with a minimum value of 50Ω should be used in line with VDD. This prevents clamping of PWM at 9.0V in the event of PWM overshoot.

FIGURE 2-1: TYPICAL CIRCUITS



Note 1: Up to 7 functions can be implemented by pressing more than one button simultaneously or by using a suitable diode array.

2: Resistor (R) is recommended for current limiting.

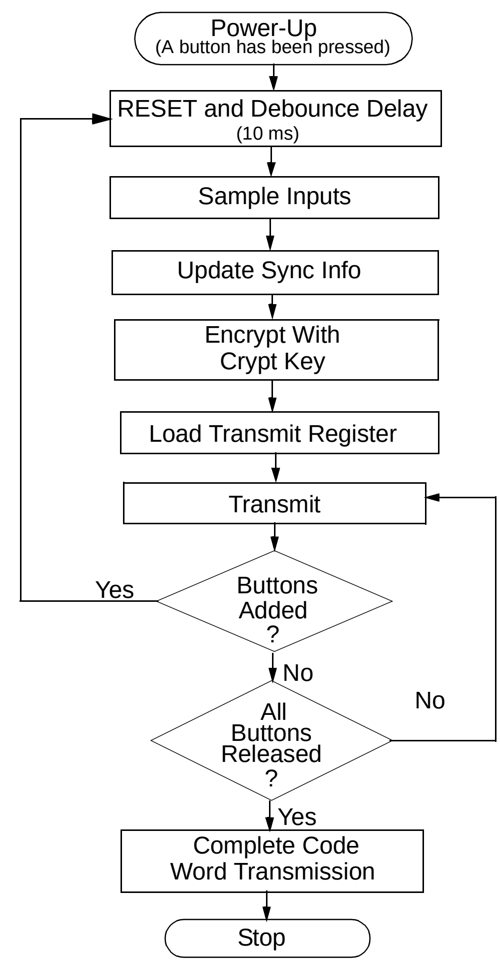
TABLE 2-1: PIN DESCRIPTIONS

Name	Pin Number	Description
S0	1	Switch input 0
S1	2	Switch input 1
S2	3	Switch input 2/Clock pin when in Programming mode
VSS	5	Ground reference
PWM	6	Pulse Width Modulation (PWM) output pin/Data pin for Programming mode
VDD	8	Positive supply voltage

The HCS200 will wake-up upon detecting a button press and delay approximately 10 ms for button debounce (Figure 2-2). The synchronization counter, discrimination value and button information will be encrypted to form the hopping code. The hopping code portion will change every transmission, even if the same button is pushed again. A code word that has been transmitted will not repeat for more than 64K transmissions. This provides more than 18 years of use before a code is repeated; based on 10 operations per day. Overflow information sent from the encoder can be used to extend the number of unique transmissions to more than 192K.

If in the transmit process it is detected that a new button(s) has been pressed, a RESET will immediately occur and the current code word will not be completed. Please note that buttons removed will not have any effect on the code word unless no buttons remain pressed; in which case the code word will be completed and the power-down will occur.

FIGURE 2-2: ENCODER OPERATION



3.0 EEPROM MEMORY ORGANIZATION

The HCS200 contains 192 bits (12 x 16-bit words) of EEPROM memory (Table 3-1). This EEPROM array is used to store the crypt key information, synchronization value, etc. Further descriptions of the memory array is given in the following sections.

TABLE 3-1: EEPROM MEMORY MAP

WORD ADDRESS	MNEMONIC	DESCRIPTION
0	KEY_0	64-bit crypt key (word 0) LSb's
1	KEY_1	64-bit crypt key (word 1)
2	KEY_2	64-bit crypt key (word 2)
3	KEY_3	64-bit crypt key (word 3) MSb's
4	SYNC	16-bit synchronization value
5	Reserved	Set to 0000H
6	SER_0	Device Serial Number (word 0) LSb's
7	SER_1	Device Serial Number (word 1) MSb's
8	SEED_0	Seed Value (word 0)
9	SEED_1	Seed Value (word 1)
10	Reserved	Set to 0000H
11	CONFIG	Configuration Word

3.1 Key_0 - Key_3 (64-Bit Crypt Key)

The 64-bit crypt key is used to create the encrypted message transmitted to the receiver. This key is calculated and programmed during production using a key generation algorithm. The key generation algorithm may be different from the KEELOQ algorithm. Inputs to the key generation algorithm are typically the transmitter's serial number and the 64-bit manufacturer's code. While the key generation algorithm supplied from Microchip is the typical method used, a user may elect to create their own method of key generation. This may be done providing that the decoder is programmed with the same means of creating the key for decryption purposes.

3.2 SYNC (Synchronization Counter)

This is the 16-bit synchronization value that is used to create the hopping code for transmission. This value will increment after every transmission.

3.3 Reserved

Must be initialized to 0000H.

3.4 SER_0, SER_1 (Encoder Serial Number)

SER_0 and SER_1 are the lower and upper words of the device serial number, respectively. Although there are 32 bits allocated for the serial number, only the lower order 28 bits are transmitted. The serial number is meant to be unique for every transmitter.

3.5 SEED_0, SEED_1 (Seed Word)

The 2-word (32-bit) seed code will be transmitted when all three buttons are pressed at the same time (see Figure 4-2). This allows the system designer to implement the secure learn feature or use this fixed code word as part of a different key generation/tracking process.

3.6 Configuration Word

The 16-bit Configuration Word stored in the EEPROM array contains information required to form the encrypted portion of the transmission, as well as the device option configurations. The following sections further explain these bits.

TABLE 3-2: CONFIGURATION WORD

Bit Number	Bit Description
0	Discrimination Bit 0
1	Discrimination Bit 1
2	Discrimination Bit 2
3	Discrimination Bit 3
4	Discrimination Bit 4
5	Discrimination Bit 5
6	Discrimination Bit 6
7	Discrimination Bit 7
8	Discrimination Bit 8
9	Discrimination Bit 9
10	Discrimination Bit 10
11	Discrimination Bit 11
12	Low Voltage Trip Point Select (VLOW SEL)
13	Baudrate Select Bit 0 (BSL0)
14	Reserved, set to 0
15	Reserved, set to 0

3.6.1 DISCRIMINATION VALUE (DISC0 TO DISC11)

The discrimination value aids the post-decryption check on the decoder end. It may be any value, but in a typical system it will be programmed as the 12 Least Significant bits of the serial number. Values other than this must be separately stored by the receiver when a transmitter is learned. The discrimination bits are part of the information that form the encrypted portion of the transmission (Figure 4-2). After the receiver has decrypted a transmission, the discrimination bits are checked against the receiver's stored value to verify that the decryption process was valid. If the discrimination value was programmed as the 12 LSb's of the serial number then it may merely be compared to the respective bits of the received serial number; saving EEPROM space.

3.6.2 BAUD RATE SELECT BIT (BSL0)

BSL0 selects the speed of transmission and the code word blanking. Table 3-3 shows how the bit is used to select the different baud rates and Section 5.2 provides detailed explanation in code word blanking.

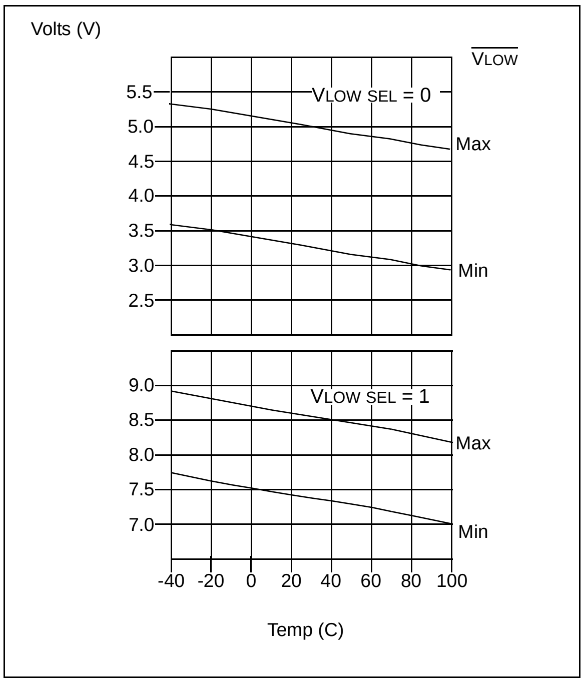
TABLE 3-3: BAUD RATE SELECT

BSL0	Basic Pulse Element	Code Words Transmitted
0	400 µs	All
1	200 µs	1 out of 2

3.6.3 LOW VOLTAGE TRIP POINT SELECT (VLOW SEL)

The low voltage trip point select bit tells the HCS200 what VDD level is being used. This information will be used by the device to determine when to send the voltage low signal to the receiver. When this bit is set to a one, the VDD level is assumed to be operating from a 9.0 volt or 12.0 volt VDD level. If the bit is set to zero, the VDD level is assumed to be 6.0 volts. Refer to Figure 3-1 for voltage trip point.

FIGURE 3-1: VOLTAGE TRIP POINTS BY CHARACTERIZATION



4.0 TRANSMITTED WORD

4.1 Code Word Format

The HCS200 code word is made up of several parts (Figure 4-1). Each code word contains a 50% duty cycle preamble, a header, 32 bits of encrypted data and 34 bits of fixed data followed by a guard period before another code word can begin. Refer to Table 8-3 for code word timing.

4.2 Code Word Organization

The HCS200 transmits a 66-bit code word when a button is pressed. The 66-bit word is constructed from a Fixed Code portion and an Encrypted Code portion (Figure 4-2).

The 32 bits of **Encrypted Data** are generated from 4 button bits, 12 discrimination bits and the 16-bit sync value. The encrypted portion alone provides up to four billion changing code combinations.

The 34 bits of **Fixed Code Data** are made up of 1 status bit, 1 fixed bit, 4 button bits and the 28-bit serial number. The fixed and encrypted sections combined increase the number of code combinations to 7.38 x 10^{19}.

4.3 Synchronous Transmission Mode

Synchronous Transmission mode can be used to clock the code word out using an external clock.

To enter Synchronous Transmission mode, the Programming mode start-up sequence must be executed as shown in Figure 4-3. If either S1 or S0 is set on the falling edge of S2, the device enters Synchronous Transmission mode. In this mode it functions as a normal transmitter, with the exception that the timing of the PWM data string is controlled externally and that 16 extra reserved bits are transmitted at the end of the code word. The reserved bits can be ignored. The button code will be the S0, S1 value at the falling edge of S2. The timing of the PWM data string is controlled by supplying a clock on S2 and should not exceed 20 kHz. When in Synchronous Transmission mode S2 should not be toggled until all internal processing has been completed as shown in Figure 4-3.

FIGURE 4-1: CODE WORD FORMAT

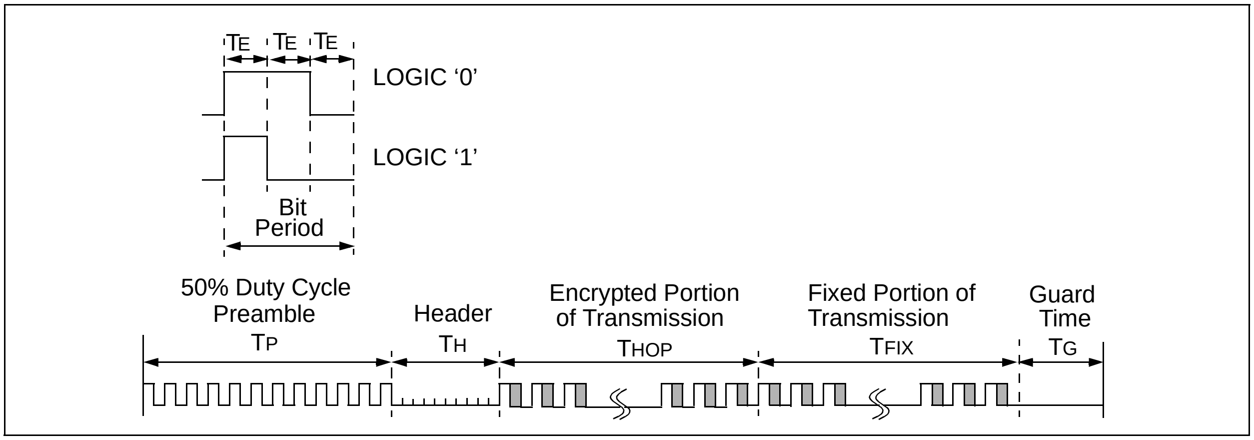


FIGURE 4-2: CODE WORD ORGANIZATION

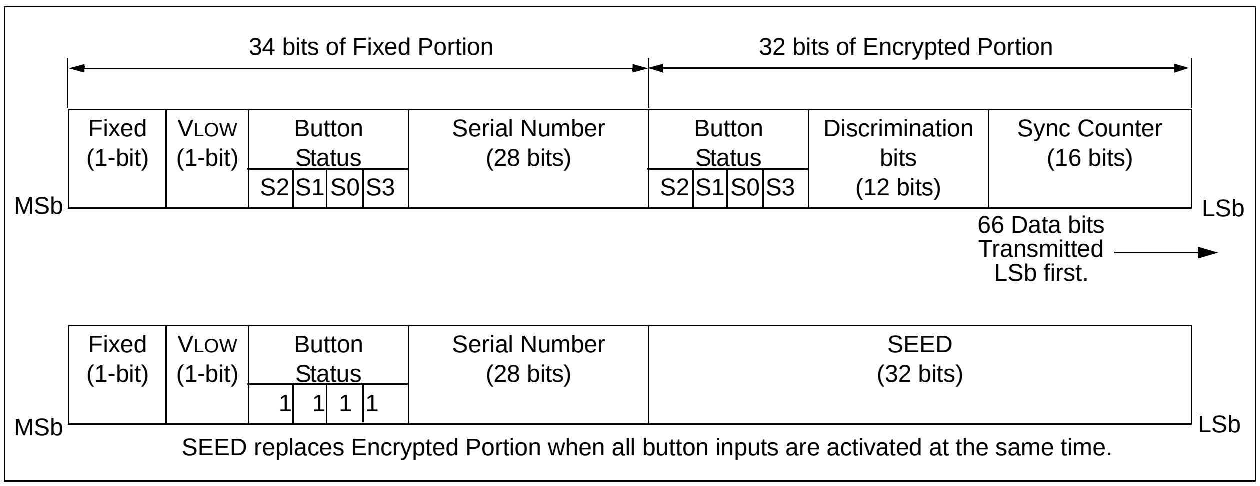


FIGURE 4-3: SYNCHRONOUS TRANSMISSION MODE

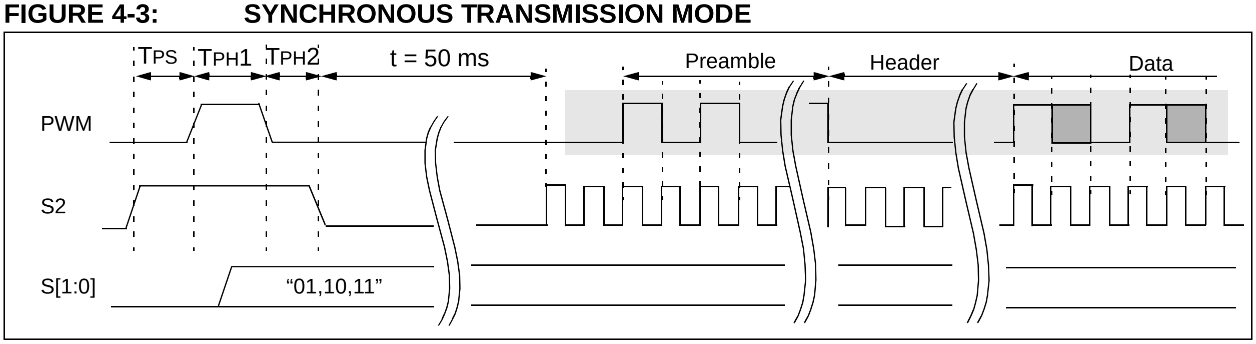
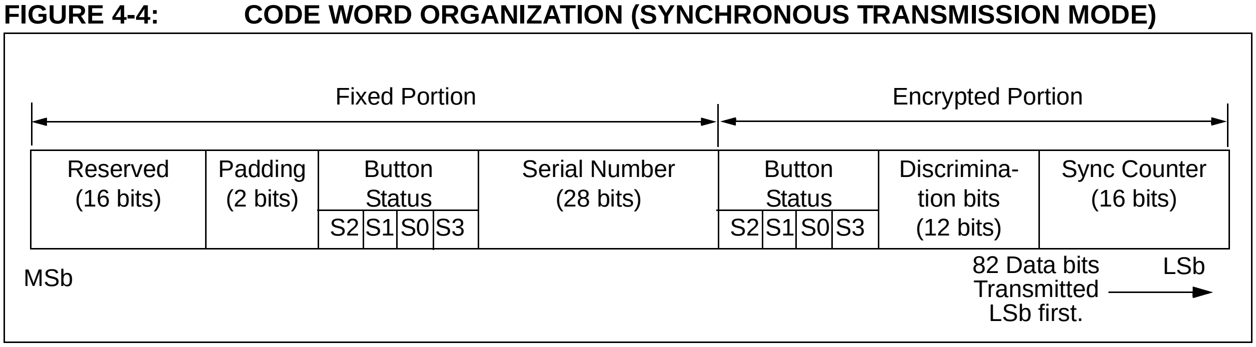


FIGURE 4-4: CODE WORD ORGANIZATION (SYNCHRONOUS TRANSMISSION MODE)



5.0 SPECIAL FEATURES

5.1 Code Word Completion

The code word completion feature ensures that entire code words are transmitted, even if the button is released before the code word is complete. If the button is held down beyond the time for one code word, multiple code words will result. If another button is activated during a transmission, the active transmission will be aborted and a new transmission will begin using the new button information.

5.2 Blank Alternate Code Word

Federal Communications Commission (FCC) part 15 rules specify the limits on worst case average fundamental power and harmonics that can be transmitted in a 100 ms window. For FCC approval purposes, it may therefore be advantageous to minimize the transmission duty cycle. This can be achieved by minimizing the duty cycle of the individual bits as well as by blanking out consecutive code words. Blank Alternate Code Word (BACW) may be used to reduce the average power of a transmission by transmitting only every second code word (Figure 5-1). This is a selectable feature that is determined in conjunction with the baud rate selection bit BSL0.

Enabling the BACW option may likewise allow the user to transmit a higher amplitude transmission as the time averaged power is reduced. BACW effectively halves the RF on time for a given transmission so the RF output power could theoretically be doubled while maintaining the same time averaged output power.

5.3 Seed Transmission

In order to increase the level of security in a system, it is possible for the receiver to implement what is known as a secure learn function. This can be done by utilizing the seed value stored in EEPROM, transmitted only when all three button inputs are pressed at the same time (Table 5-1). Instead of the normal key generation inputs being used to create the crypt key, this seed value is used.

5.4 VLOW: Voltage LOW Indicator

The VLOW signal is transmitted so the receiver can give an indication to the user that the transmitter battery is low. The VLOW bit is included in every transmission (Figure 4-2 and Figure 8-5) and will be transmitted as a zero if the operating voltage is above the low voltage trip point. Refer to Figure 4-2. The trip point is selectable based on the battery voltage being used. See Section 3.6.3 for a description of how the low voltage trip point is configured.

FIGURE 5-1: BLANK ALTERNATE CODE WORD (BACW)

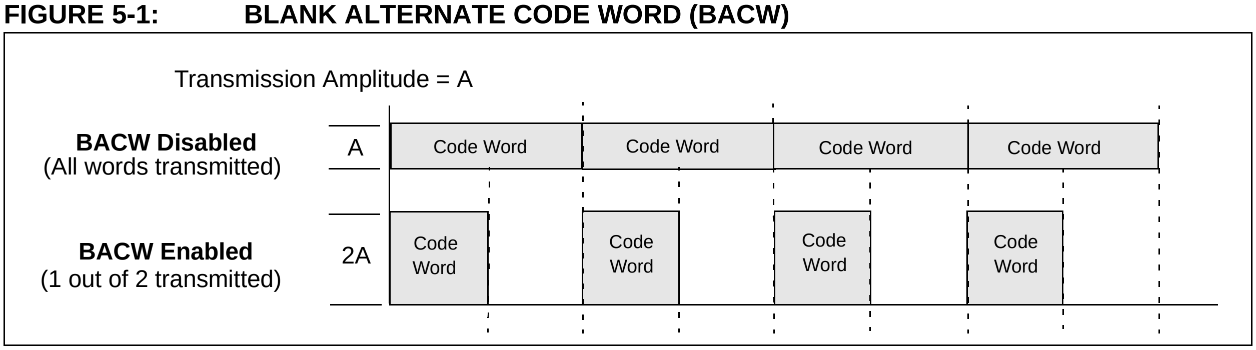


TABLE 5-1: PIN ACTIVATION TABLE

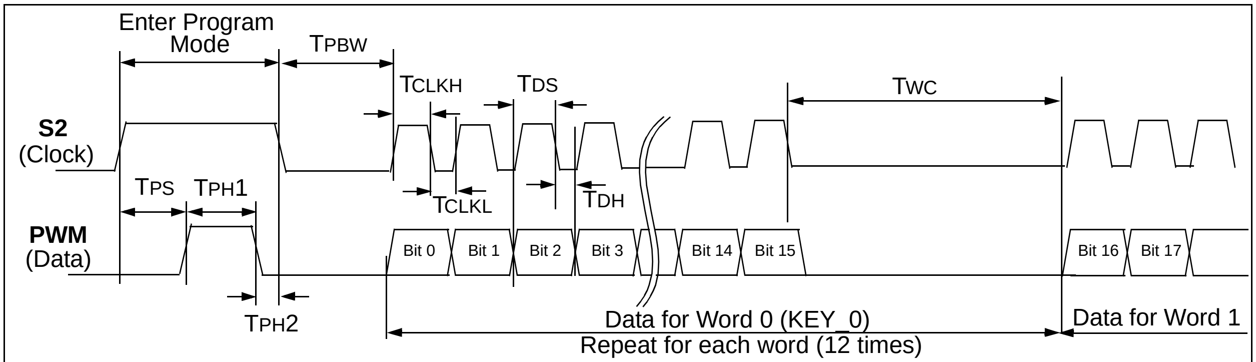
	External			Internal			
	S2	**S1**	**S0**	**S3**	**S2**	**S1**	**S0**
Standby	0	0	0	0	0	0	0
Hopping Code Transmission	0	0	1	0	0	0	1
	0	1	0	0	0	1	0
	0	1	1	0	0	1	1
	1	0	0	1	1	0	0
	1	0	1	1	1	1	0
	1	1	0	1	1	1	0
Seed Transmission	1	1	1	1	1	1	1

6.0 PROGRAMMING THE HCS200

When using the HCS200 in a system, the user will have to program some parameters into the device, such as the serial number and crypt key, before it can be used. The programming cycle allows the user to input all 192 bits in a serial data stream, which are then stored internally in EEPROM. Programming will be initiated by forcing the PWM line high, after the S2 line has been held high for the appropriate length of time (Table 6-1 and Figure 6-1). After the Program mode is entered, a delay must be provided for the automatic bulk write cycle to complete. This will write all locations in the EEPROM to zeros. The device can then be programmed by clocking in 16 bits at a time, using S2 as the clock line and PWM as the data in line; data is clocked in on the falling edge of S2. After each 16-bit word is sent, a programming delay of TWC is required for the internal program cycle to complete. At the end of the programming cycle, the device can be verified (Figure 6-2) by reading back the EEPROM. Reading is done by clocking the S2 line and reading the data bits on PWM. The falling edge of S2 initiates the reading. For security reasons, it is not possible to execute a Verify function without first programming the EEPROM. **A Verify operation can only be done immediately following the Program cycle**.

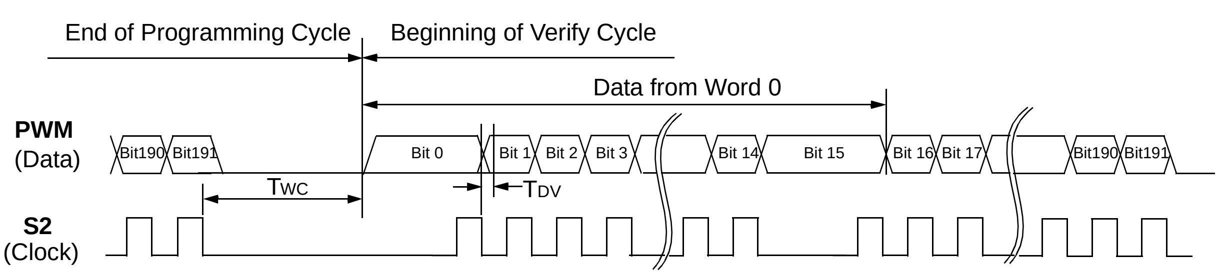
Note:	To ensure that the device does not accidentally enter Programming mode (resulting in a bulk erase), PWM should never be pulled high by the circuit connected to it. Special care should be taken when driving PNP RF transistors.

FIGURE 6-1: PROGRAMMING WAVEFORMS



Note 1: Unused button inputs to be held to ground during the entire programming sequence.
2: The VDD pin must be taken to ground after a Program/Verify cycle.

FIGURE 6-2: VERIFY WAVEFORMS



Note: If a Verify operation is to be done, then it must immediately follow the Program cycle.

TABLE 6-1: PROGRAMMING/VERIFY TIMING REQUIREMENTS

VDD = 5.0V ± 10%, 25°C ± 5 °C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**
Program mode setup time	TPS	3.5	4.5	ms
Hold time 1	TPH1	3.5	—	ms
Hold time 2	TPH2	50	—	µs
Bulk Write time	TPBW	4.0	—	ms
Program delay time	TPROG	4.0	—	ms
Program cycle time	TWC	50	—	ms
Clock low time	TCLKL	50	—	µs
Clock high time	TCLKH	50	—	µs
Data setup time	TDS	0	—	µs (1)
Data hold time	TDH	30	—	µs (1)
Data out valid time	TDV	—	30	µs (1)

Note 1: Typical values - not tested in production.

7.0 INTEGRATING THE HCS200 INTO A SYSTEM

An HCS200 based system requires a compatible decoder. The decoder is typically a microcontroller with compatible firmware. Microchip provides, via a license agreement, firmware routines that will receive and authenticate HCS200 transmissions. These routines provide designers the means to develop their own decoding system.

7.1 Learning a Transmitter to a Receiver

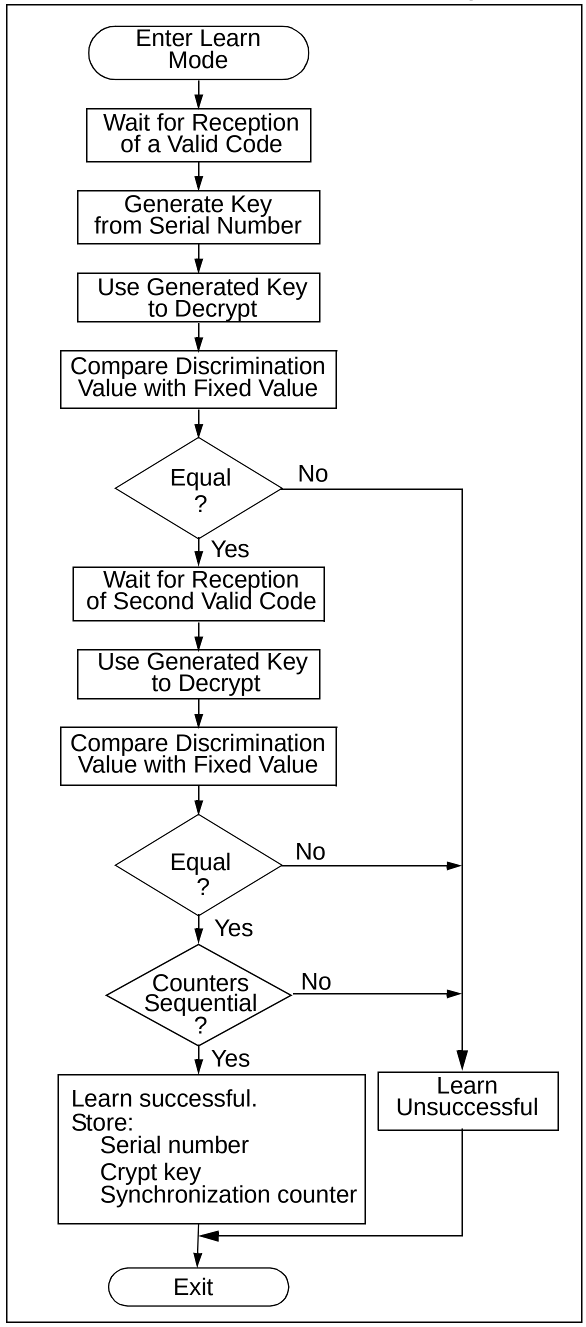
A transmitter must first be ’learned’ by a decoder before its use is allowed in the system. Several learning strategies are possible, Figure 7-1 details a typical learn sequence. Core to each, the decoder must minimally store each learned transmitter’s serial number and current synchronization counter value in EEPROM. Additionally, the decoder typically stores each transmitter’s unique crypt key. The maximum number of learned transmitters will therefore be relative to the available EEPROM.

A transmitter’s serial number is transmitted in the clear but the synchronization counter only exists in the code word’s encrypted portion. The decoder obtains the counter value by decrypting using the same key used to encrypt the information. The KEELOQ algorithm is a symmetrical block cipher so the encryption and decryption keys are identical and referred to generally as the crypt key. The encoder receives its crypt key during manufacturing. The decoder is programmed with the ability to generate a crypt key as well as all but one required input to the key generation routine; typically the transmitter’s serial number.

Figure 7-1 summarizes a typical learn sequence. The decoder receives and authenticates a first transmission; first button press. Authentication involves generating the appropriate crypt key, decrypting, validating the correct key usage via the discrimination bits and buffering the counter value. A second transmission is received and authenticated. A final check verifies the counter values were sequential; consecutive button presses. If the learn sequence is successfully complete, the decoder stores the learned transmitter’s serial number, current synchronization counter value and appropriate crypt key. From now on the crypt key will be retrieved from EEPROM during normal operation instead of recalculating it for each transmission received.

Certain learning strategies have been patented and care must be taken not to infringe.

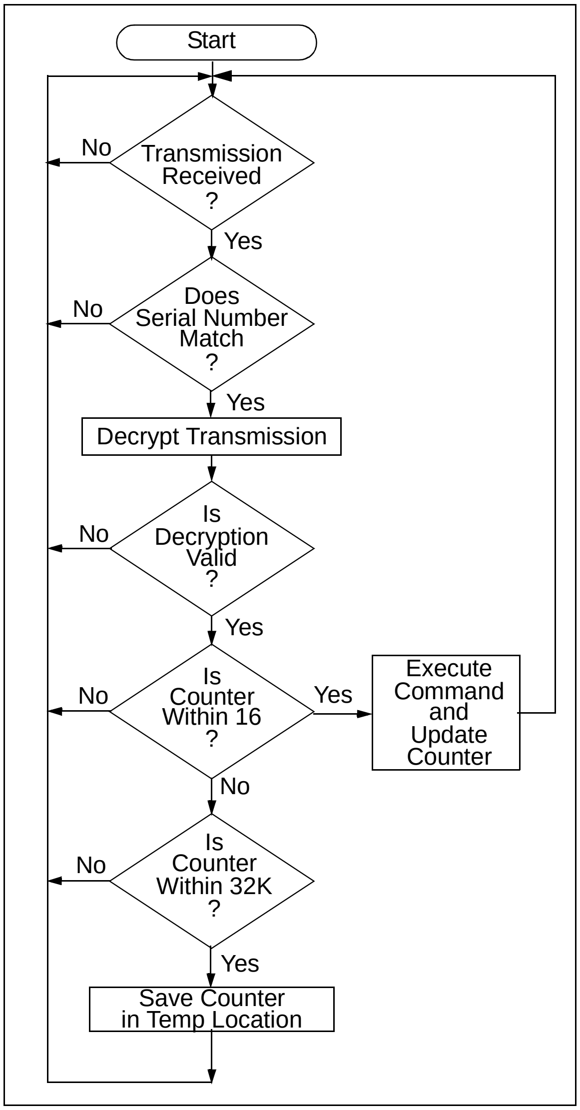
FIGURE 7-1: TYPICAL LEARN SEQUENCE



7.2 Decoder Operation

Figure 7-2 summarizes normal decoder operation. The decoder waits until a transmission is received. The received serial number is compared to the EEPROM table of learned transmitters to first determine if this transmitter's use is allowed in the system. If from a learned transmitter, the transmission is decrypted using the stored crypt key and authenticated via the discrimination bits for appropriate crypt key usage. If the decryption was valid the synchronization value is evaluated.

FIGURE 7-2: TYPICAL DECODER OPERATION



7.3 Synchronization with Decoder (Evaluating the Counter)

The KEELOQ technology patent scope includes a sophisticated synchronization technique that does not require the calculation and storage of future codes. The technique securely blocks invalid transmissions while providing transparent resynchronization to transmitters inadvertently activated away from the receiver.

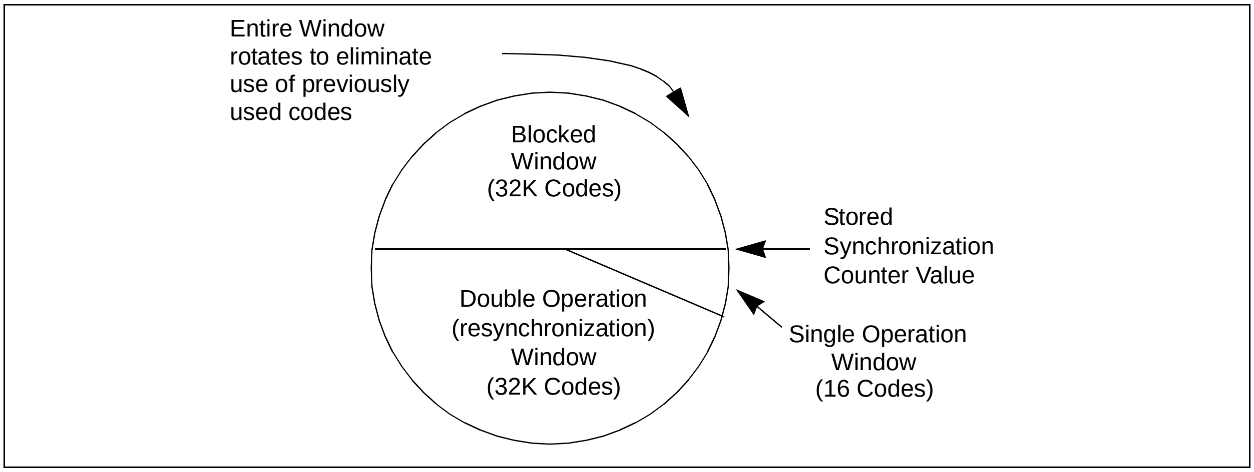
Figure 7-3 shows a 3-partition, rotating synchronization window. The size of each window is optional but the technique is fundamental. Each time a transmission is authenticated, the intended function is executed and the transmission's synchronization counter value is stored in EEPROM. From the currently stored counter value there is an initial "Single Operation" forward window of 16 codes. If the difference between a received synchronization counter and the last stored counter is within 16, the intended function will be executed on the single button press and the new synchronization counter will be stored. Storing the new synchronization counter value effectively rotates the entire synchronization window.

A "Double Operation" (resynchronization) window further exists from the Single Operation window up to 32K codes forward of the currently stored counter value. It is referred to as "Double Operation" because a transmission with synchronization counter value in this window will require an additional, sequential counter transmission prior to executing the intended function. Upon receiving the sequential transmission the decoder executes the intended function and stores the synchronization counter value. This resynchronization occurs transparently to the user as it is human nature to press the button a second time if the first was unsuccessful.

The third window is a "Blocked Window" ranging from the double operation window to the currently stored synchronization counter value. Any transmission with synchronization counter value within this window will be ignored. This window excludes previously used, perhaps code-grabbed transmissions from accessing the system.

Note:	The synchronization method described in this section is only a typical implementation and because it is usually implemented in firmware, it can be altered to fit the needs of a particular system.

FIGURE 7-3: SYNCHRONIZATION WINDOW



8.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

V_{DD} Supply voltage .... -0.3 to 13.3V
V_{IN} Input voltage .... -0.3 to 13.3
V_{OUT} Output voltage .... -0.3 to V_{DD} + 0.3V
I_{OUT} Max output current .... 25 mA
T_{STG} Storage temperature **(Note)** .... -55 to +125°C
T_{LSOL} Lead soldering temp **(Note)** .... 300°C
V_{ESD} ESD rating 4000V

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 8-1: DC CHARACTERISTICS

Commercial(C):Tamb = 0°C to +70°C Industrial(I):Tamb = -40°C to +85°C						
		3.5V < V_{DD} < 13.0V				
Parameter	**Sym.**	**Min**	**Typ***	**Max**	**Unit**	**Conditions**
Operating Current (avg)	I_{CC}		0.6 1.5 8.0	1.0 3.0 12.0	mA	V_{DD} = 3.5V V_{DD} = 6.6V V_{DD} = 13.0V
Standby Current	I_{CCS}		1	10	µA	
High Level Input Voltage	V_{IH}	0.4 V_{DD}		V_{DD}+ 0.3	V	
Low Level Input Voltage	V_{IL}	-0.3		0.15 V_{DD}	V	
High Level Output Voltage	V_{OH}	0.5 V_{DD}			V	I_{OH} = -2.0 mA
Low Level Output Voltage	V_{OL}			0.08 V_{DD}	V	I_{OL} = 2.0 mA
Pull-Down Resistance; S0-S2	R_{S0-2}	40	60	80	KΩ	V_{IN} = 4.0V
Pull-Down Resistance; PWM	R_{PWM}	80	120	160	KΩ	V_{IN} = 4.0V

Note: Typical values are at 25°C.

FIGURE 8-1: TYPICAL ICC CURVE OF HCS200 WITH EXTERNAL RESISTORS

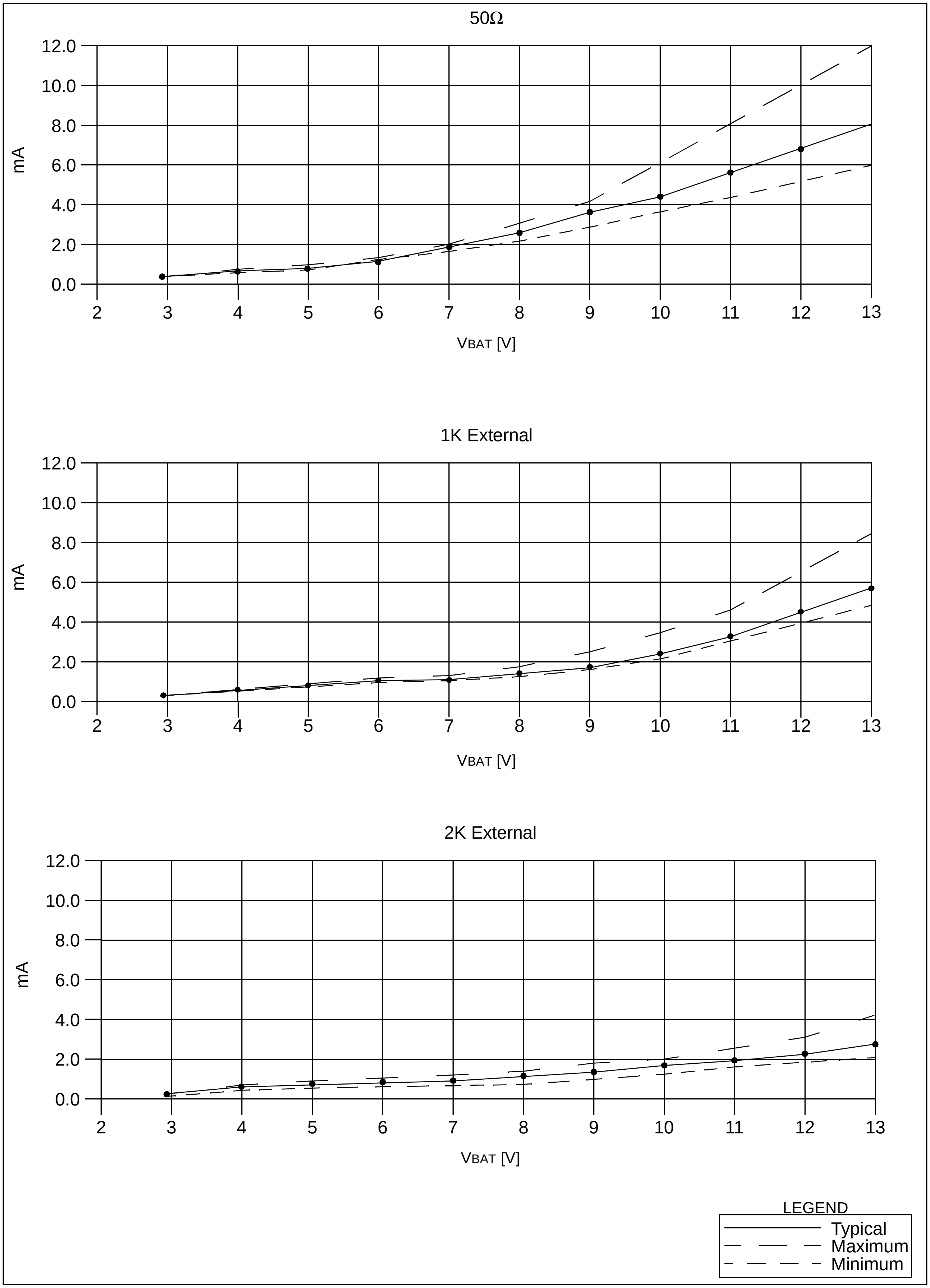


FIGURE 8-2: POWER-UP AND TRANSMIT TIMING

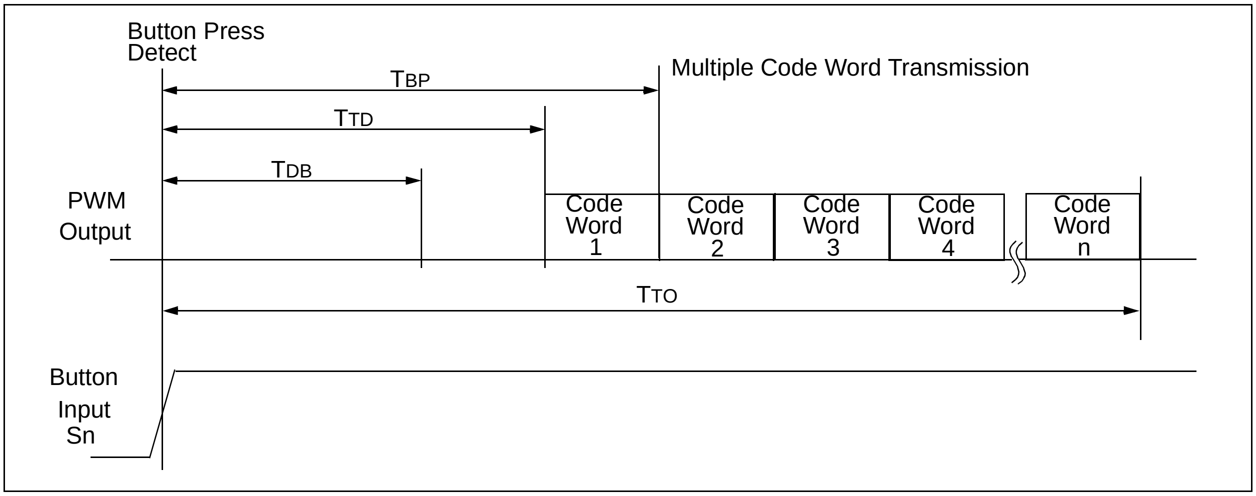


TABLE 8-2: POWER-UP AND TRANSMIT TIMING(2)

VDD = +3.5 to 13.0V
Commercial(C): Tamb = 0°C to +70°C
Industrial(I): Tamb = -40°C to +85°C

Symbol	Parameter	Min	Max	Unit	Remarks
TBP	Time to second button press	10 + Code Word	26 + Code Word	ms	**(Note 1)**
TTD	Transmit delay from button detect	10	26	ms	
TDB	Debounce Delay	6	15	ms	
TTO	Auto-shutoff time-out period	20	120	s	

Note 1: TBP is the time in which a second button can be pressed without completion of the first code word and the intention was to press the combination of buttons.

2: Typical values - not tested in production.

FIGURE 8-3: CODE WORD FORMAT

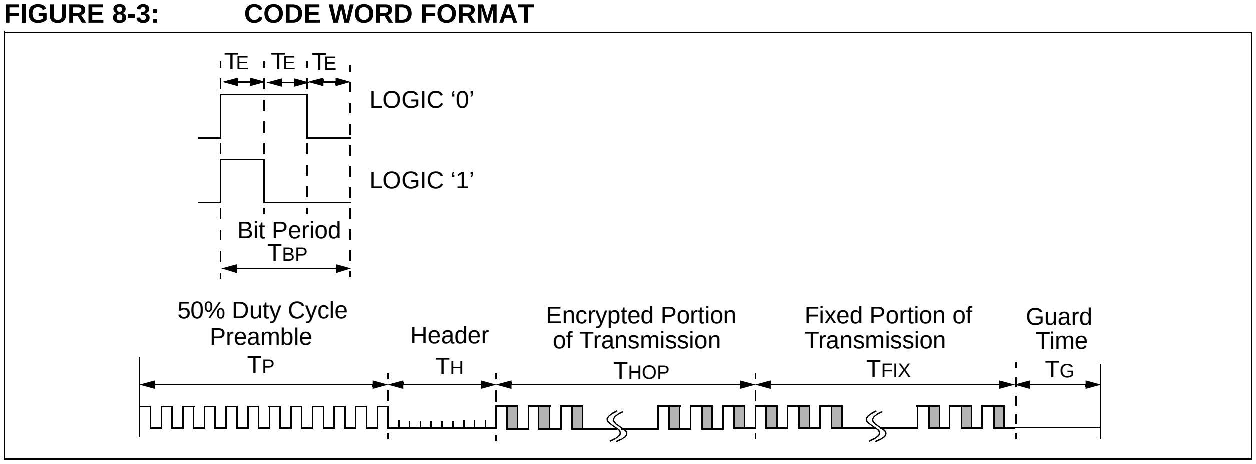


FIGURE 8-4: CODE WORD FORMAT: PREAMBLE/HEADER PORTION

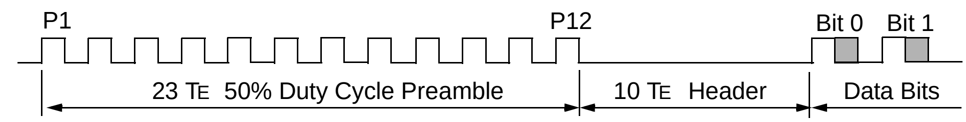


FIGURE 8-5: CODE WORD FORMAT: DATA PORTION

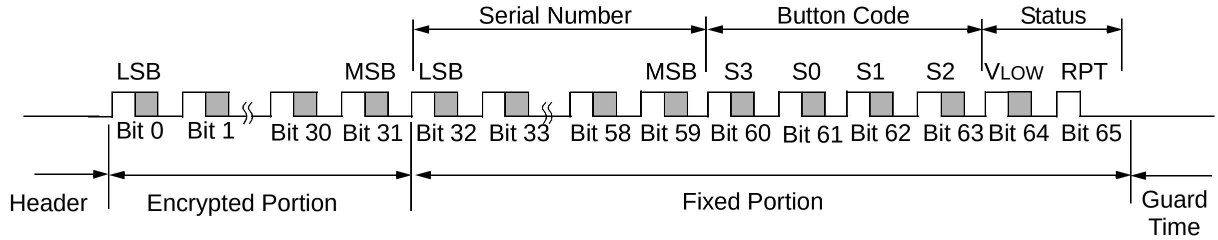
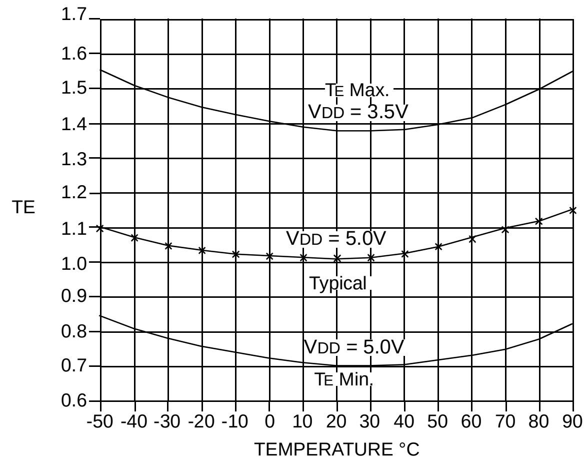


TABLE 8-3: CODE WORD TIMING

V_{DD} = +3.5 to 13.0V Commercial(C):Tamb = 0°C to +70°C Industrial(I):Tamb = -40°C to +85°C			Code Words Transmitted						
			All			1 out of 2			
Symbol	**Characteristic**	**Number of T_E**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
T_E	Basic pulse element	1	280	400	620	140	200	310	µs
T_{BP}	PWM bit pulse width	3	840	1200	1860	420	600	930	µs
T_P	Preamble duration	23	6.4	9.2	14.3	3.2	4.6	7.1	ms
T_H	Header duration	10	2.8	4.0	6.2	1.4	2.0	3.1	ms
T_{HOP}	Hopping code duration	96	26.9	38.4	59.5	13.4	19.2	29.8	ms
T_{FIX}	Fixed code duration	102	28.6	40.8	63.2	14.3	20.4	31.6	ms
T_G	Guard Time	39	10.9	15.6	24.2	5.5	7.8	12.1	ms
—	Total Transmit Time	270	75.6	108.0	167.4	37.8	54.0	83.7	ms
—	PWM data rate	—	1190	833	538	2381	1667	1075	bps

Note: The timing parameters are not tested but derived from the oscillator clock.

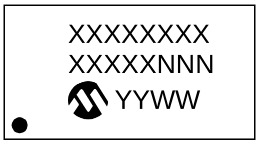
FIGURE 8-6: HCS200 TE VS. TEMP (BY CHARACTERIZATION)



9.0 PACKAGING INFORMATION

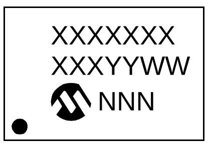
9.1 Package Marking Information

8-Lead PDIP (300 mil)



Example

8-Lead SOIC (150 mil)



Example

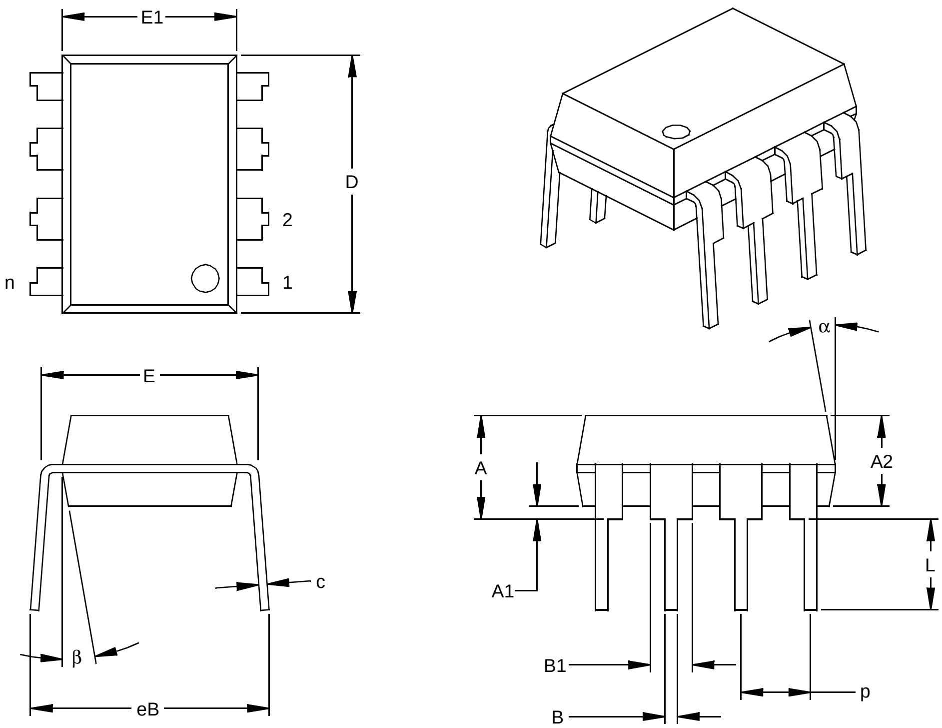
Legend:	XX...X	Customer specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

9.2 Package Details

8-Lead Plastic Dual In-line (P) - 300 mil (PDIP)

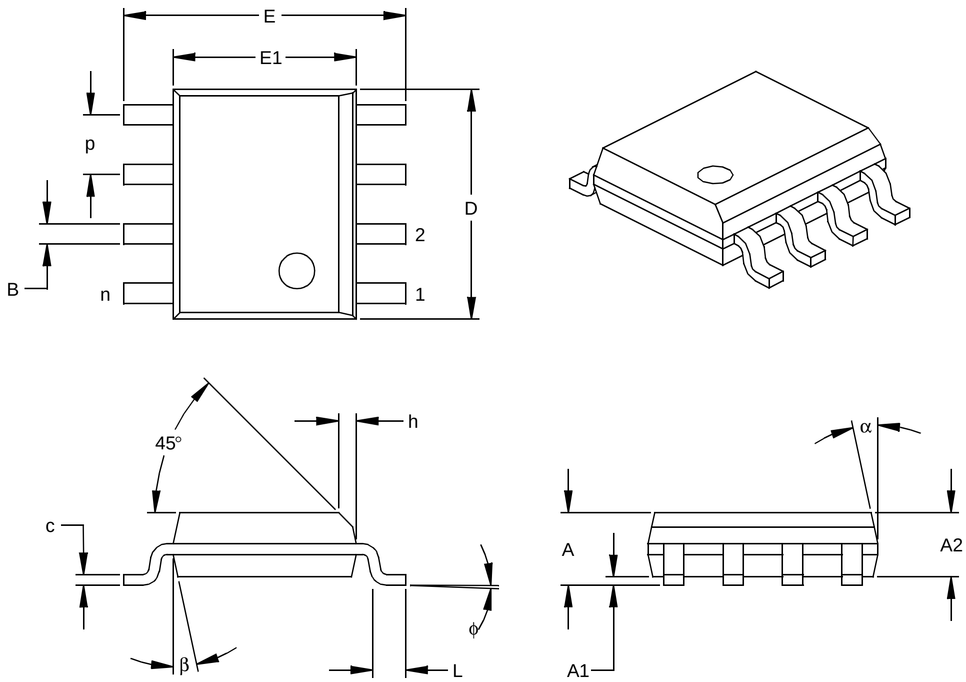


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) - Narrow, 150 mil (SOIC)



	Units	INCHES*			MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
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HCS200 PRODUCT IDENTIFICATION SYSTEM

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HCS200 - __ _ /P

Package:	P	=	Plastic DIP (300 mil Body), 8-lead)
	SN	=	Plastic SOIC (150 mil Body), 8-lead
Temperature Range:	Blank	=	0°C to +70°C
	I	=	–40°C to +85°C
Device:	HCS200	=	Code Hopping Encoder
	HCS200T	=	Code Hopping Encoder (Tape and Reel)

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