

## Low Charge Injection, 8-Channel, High Voltage Analog Switches

### Features

- ▶ HVCMOS® technology for high performance
- ▶ Very low quiescent power dissipation (-10µA)
- ▶ Output on-resistance typically 22Ω
- ▶ Low parasitic capacitances
- ▶ DC to 50MHz small signal frequency response
- ▶ -60dB typical output off isolation at 5.0MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ On-chip shift register, latch and clear logic circuitry
- ▶ Flexible high voltage supplies

### Applications

- ▶ Medical ultrasound imaging
- ▶ Piezoelectric transducer drivers

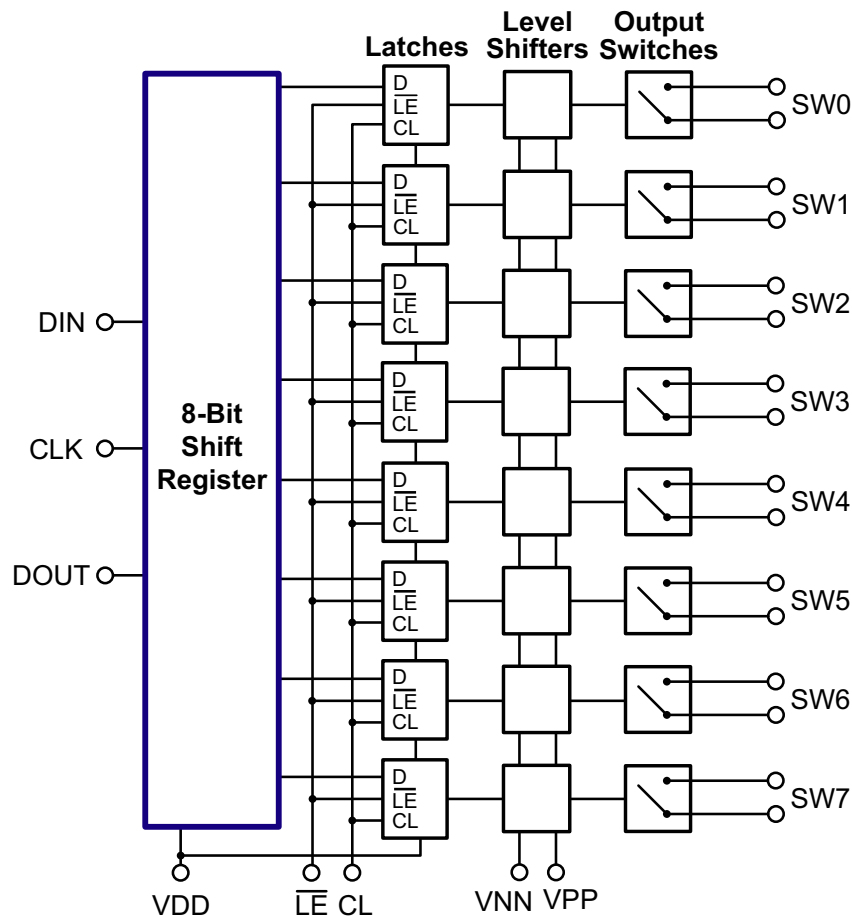
### General Description

This device is a low charge injection, 8-channel, high-voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers.

Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feed-through noise, Latch Enable Bar ( $\overline{LE}$ ) should be left high until all bits are clocked in. Using HVCMOS® technology, this switch combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

These ICs are suitable for various combinations of high voltage supplies, e.g.,  $V_{PP}/V_{NN}$  : +50V/-150V, or +100V/-100V.

### Block Diagram



## Ordering Information

Device	Package Options	
	48-Lead LQFP 7.00x7.00mm body 1.60mm height (max) 0.50mm pitch	28-Lead PLCC .453x.453in body .180in height (max) .050in pitch
HV20220	HV20220FG-G	HV20220PJ-G



-G indicates the part is RoHS compliant (Green)

## Absolute Maximum Ratings

Parameter	Value
V <sub>DD</sub> logic power supply voltage	-0.5V to +15V
V <sub>PP</sub> - V <sub>NN</sub> supply voltage	220V
V <sub>PP</sub> positive high voltage supply	-0.5V to V <sub>NN</sub> +200V
V <sub>NN</sub> negative high voltage supply	+0.5V to -200V
Logic input voltages	-0.5V to V <sub>DD</sub> +0.3V
Analog signal range	V <sub>NN</sub> to V <sub>PP</sub>
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation:	
48-Lead LQFP	1.0W
28-JLead PLCC	1.2W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

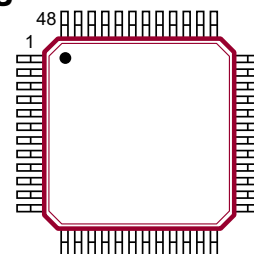
## Operating Conditions

Sym	Parameter	Value
V <sub>DD</sub>	Logic power supply voltage <sup>1,3</sup>	4.5V to 13.2V
V <sub>PP</sub>	Positive high voltage supply <sup>1,3</sup>	40V to V <sub>NN</sub> +200V
V <sub>NN</sub>	Negative high voltage supply <sup>1,3</sup>	-40V to -160V
V <sub>IH</sub>	High level input voltage	V <sub>DD</sub> -1.5V to V <sub>DD</sub>
V <sub>IL</sub>	Low-level input voltage	0V to 1.5V
V <sub>SIG</sub>	Analog signal voltage peak-to-peak	V <sub>NN</sub> +10V to V <sub>PP</sub> -10V <sup>2</sup>
T <sub>A</sub>	Operating free air temperature	0°C to 70°C

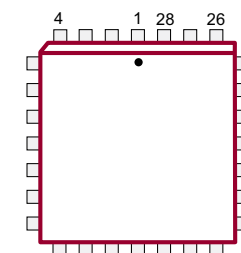
### Notes:

1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V<sub>SIG</sub> must be V<sub>NN</sub> ≤ V<sub>SIG</sub> ≤ V<sub>PP</sub> or floating during power-up/down transition.
3. Rise and fall times of power supplies V<sub>DD</sub>, V<sub>PP</sub> and V<sub>NN</sub> should not be less than 1.0msec.

## Pin Configurations



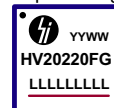
48-Lead LQFP (FG)



28-Lead PLCC (PJ)

## Product Marking

Top Marking



Bottom Marking

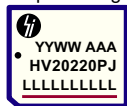


YY = Year Sealed  
WW = Week Sealed  
L = Lot Number  
C = Country of Origin\*  
A = Assembler ID\*  
— = "Green" Packaging  
\*May be part of top marking

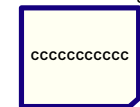
Package may or may not include the following marks: Si or

48-Lead LQFP (FG)

Top Marking



Bottom Marking



YY = Year Sealed  
WW = Week Sealed  
L = Lot Number  
A = Assembler ID  
C = Country of Origin\*  
— = "Green" Packaging  
\*May be part of top marking

Package may or may not include the following marks: Si or

28-Lead PLCC (PJ)

## DC Electrical Characteristics

(Over operating conditions unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R <sub>ONS</sub>	Small signal switch on-resistance	-	30	-	26	38	-	48	Ω	I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +40V
		-	25	-	22	27	-	32		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -160V
		-	25	-	22	27	-	30		I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +100V
		-	18	-	18	24	-	27		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -100V
		-	23	-	20	25	-	30		I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +160V
		-	22	-	16	25	-	27		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -40V
ΔR <sub>ONS</sub>	Small signal switch on-resistance matching	-	20	-	5.0	20	-	20	%	I <sub>SIG</sub> = 5.0mA, V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V	
R <sub>ONL</sub>	Large signal switch on-resistance	-	-	-	15	-	-	-	Ω	V <sub>SIG</sub> = V <sub>PP</sub> -10V, I <sub>SIG</sub> = 1.0A	
I <sub>SOL</sub>	Switch off leakage per switch	-	5.0	-	1.0	10	-	15	μA	V <sub>SIG</sub> = V <sub>PP</sub> -10V, V <sub>NN</sub> +10V	
V <sub>OS</sub>	DC offset switch off	-	300	-	100	300	-	300	mV	R <sub>L</sub> = 100kΩ	
	DC offset switch on	-	500	-	100	500	-	500	mV	R <sub>L</sub> = 100kΩ	
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current	-	-	-	10	50	-	-	μA	All switches off	
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current	-	-	-	-10	-50	-	-	μA	All switches off	
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current	-	-	-	10	50	-	-	μA	All switches on, I <sub>SW</sub> = 5.0mA	
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current	-	-	-	-10	-50	-	-	μA	All switches on, I <sub>SW</sub> = 5.0mA	
I <sub>SW</sub>	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V <sub>SIG</sub> duty cycle < 0.1%	
f <sub>SW</sub>	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I <sub>PP</sub>	Supply current	-	6.5	-	-	7.0	-	8.0	mA	V <sub>PP</sub> = +40V	All output switches are turning On and Off at 50kHz with no load
		-	4.0	-	-	5.0	-	5.5		V <sub>NN</sub> = -160V	
		-	4.0	-	-	5.0	-	5.5		V <sub>PP</sub> = +100V V <sub>NN</sub> = -100V	
I <sub>NN</sub>	Supply current	-	6.5	-	-	7.0	-	8.0	mA	V <sub>PP</sub> = +160V	All output switches are turning On and Off at 50kHz with no load
		-	4.0	-	-	5.0	-	5.5		V <sub>NN</sub> = -40V	
		-	4.0	-	-	5.0	-	5.5		V <sub>PP</sub> = +100V V <sub>NN</sub> = -100V	
I <sub>DD</sub>	Logic supply average current	-	4.0	-	-	4.0	-	4.0	mA	f <sub>CLK</sub> = 5.0MHz, V <sub>DD</sub> = 5.0V	
I <sub>DDQ</sub>	Logic supply quiescent current	-	10	-	-	10	-	10	μA	---	
I <sub>SOR</sub>	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V <sub>OUT</sub> = V <sub>DD</sub> -0.7V	
I <sub>SINK</sub>	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V <sub>OUT</sub> = 0.7V	
C <sub>IN</sub>	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

## AC Electrical Characteristics

(Over recommended operating conditions:  $V_{DD} = 5.0V$ , unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
$t_{SD}$	Set up time before $\overline{LE}$ rises	150	-	150	-	-	150	-	ns	---
$t_{WLE}$	Time width of $\overline{LE}$	150	-	150	-	-	150	-	ns	---
$t_{DO}$	Clock delay time to data out	-	150	-	-	150	-	150	ns	---
$t_{WCL}$	Time width of CL	150	-	150	-	-	150	-	ns	---
$t_{SU}$	Set up time data to clock	15	-	15	8.0	-	20	-	ns	---
$t_H$	Hold time data from clock	35	-	35	-	-	35	-	ns	---
$f_{CLK}$	Clock frequency	-	5.0	-	-	5.0	-	5.0	MHz	50% Duty cycle, $f_{DATA} = f_{CLK}/2$
$t_R, t_F$	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
$t_{ON}$	Turn on time	-	5.0	-	-	5.0	-	5.0	$\mu s$	$V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10k\Omega$
$t_{OFF}$	Turn off time	-	5.0	-	-	5.0	-	5.0	$\mu s$	$V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10k\Omega$
dv/dt	Maximun $V_{SIG}$ slew rate	-	20	-	-	20	-	20	V/ns	$V_{PP} = +160V, V_{NN} = -40V$
		-	20	-	-	20	-	20		$V_{PP} = +100V, V_{NN} = -100V$
		-	20	-	-	20	-	20		$V_{PP} = +40V, V_{NN} = -160V$
$K_O$	Off isolation	-30	-	-30	-33	-	-30	-	dB	$f = 5.0MHz, 1.0k\Omega/15pF$ load
		-58	-	-58	-	-	-58	-		$f = 5.0MHz, 50\Omega$ load
$K_{CR}$	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	$f = 5.0MHz, 50\Omega$ load
$I_{ID}$	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, $f = 1.0MHz$
$C_{SG(ON)}$	On capacitance SW to GND	25	50	25	38	50	25	50	pF	0V, $f = 1.0MHz$
$+V_{SPK}$	Output voltage spike	-	-	-	-	150	-	-	mV	$V_{PP} = +40V, V_{NN} = -160V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	150	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +100V, V_{NN} = -100V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	150	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	150	-	-		
QC	Charge injection	-	-	-	820	-	-	-	pC	$V_{PP} = +40V, V_{NN} = -160V, V_{SIG} = 0V$
		-	-	-	600	-	-	-		$V_{PP} = +100V, V_{NN} = -100V, V_{SIG} = 0V$
		-	-	-	350	-	-	-		$V_{PP} = +160V, V_{NN} = -40V, V_{SIG} = 0V$

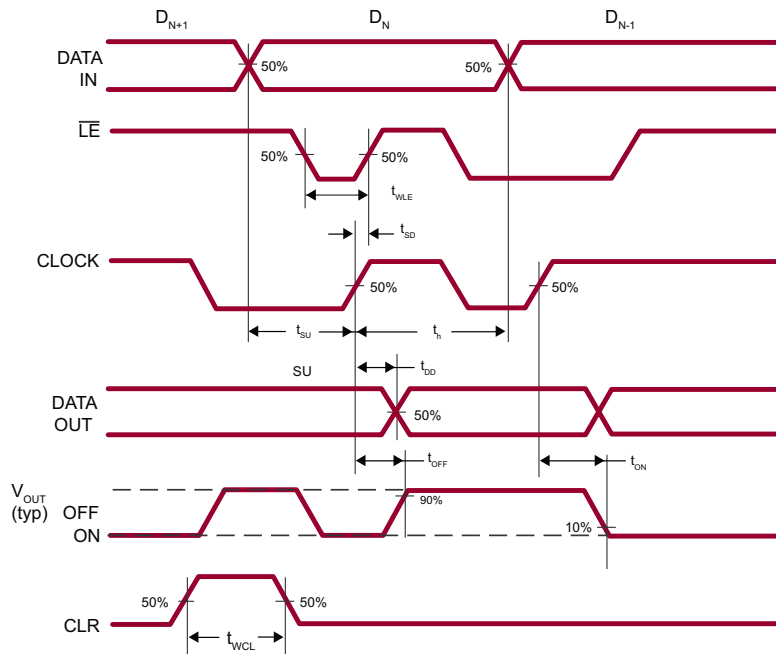
Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7	
L								L	L	Off								
H								L	L	On								
	L							L	L		Off							
	H							L	L		On							
		L						L	L			Off						
		H						L	L			On						
			L					L	L				Off					
			H					L	L				On					
				L				L	L					Off				
				H				L	L					On				
					L			L	L						Off			
					H			L	L						On			
						L		L	L								Off	
						H		L	L								On	
							L	L	L									Off
							H	L	L									On
X	X	X	X	X	X	X	X	H	L	Hold Previous State								
X	X	X	X	X	X	X	X	X	H	All Switches Off								

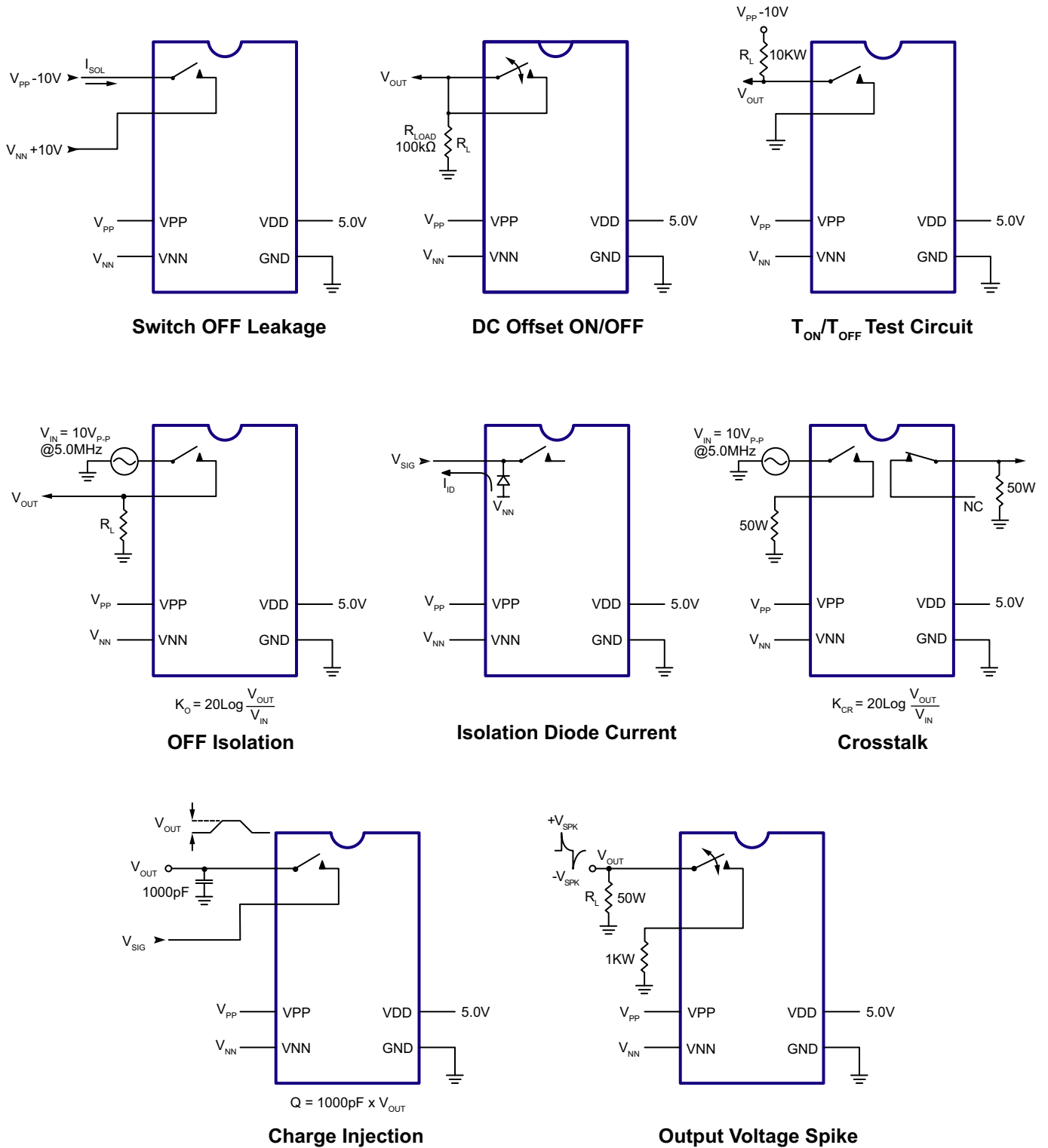
Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. The switches go to a state retaining their present condition at the rising edge of  $\overline{LE}$ . When  $\overline{LE}$  is low the shift register data flow through the latch.
4.  $D_{OUT}$  is high when data in the shift register 7 is high.
5. Shift register clocking has no effect on the switch states if  $\overline{LE}$  is high.
6. The CLR clear input overrides all other inputs.

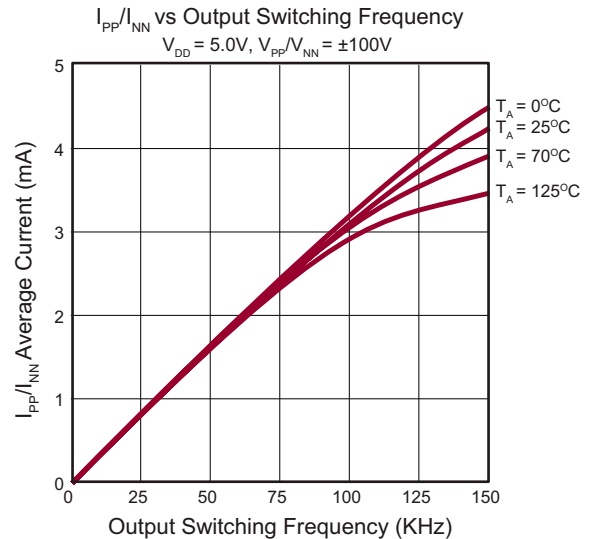
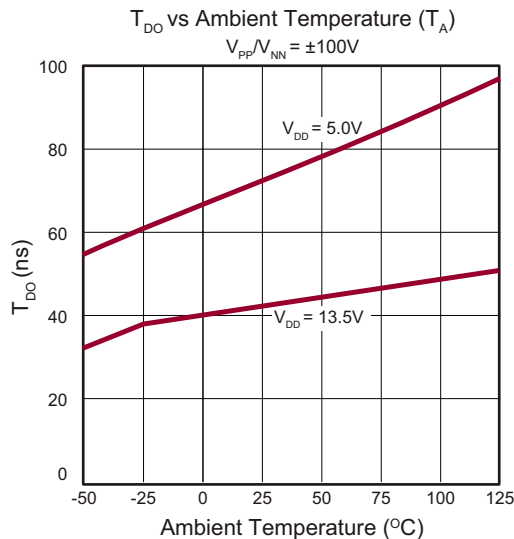
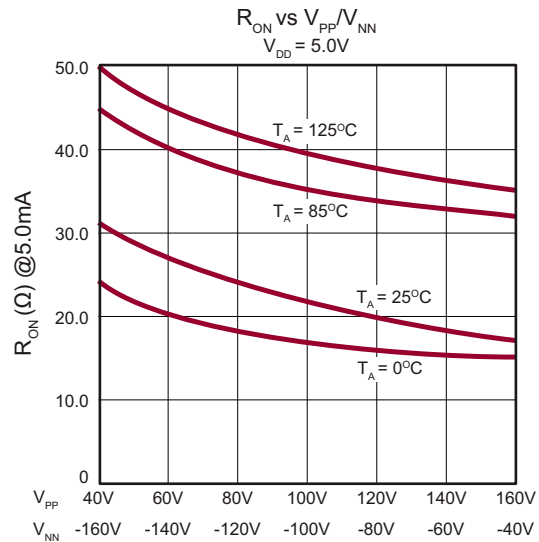
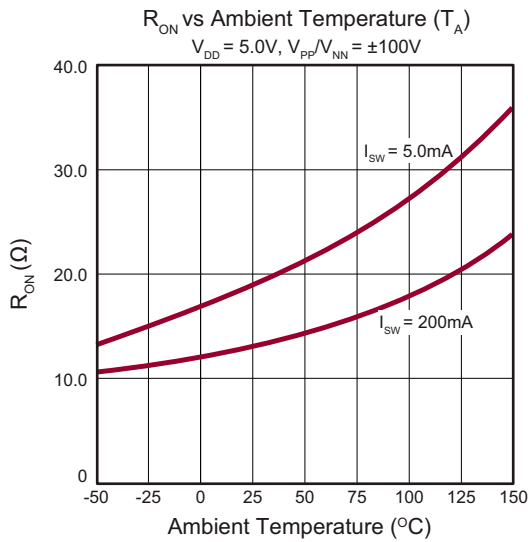
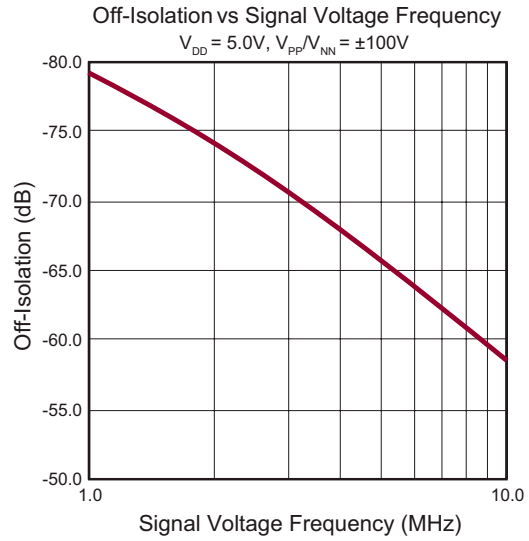
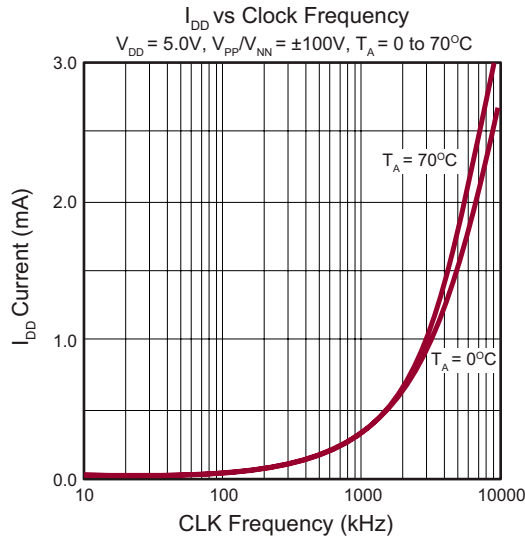
Logic Timing Waveforms



Test Circuits



### Typical Performance Curves



## Pin Description - 48-Lead LQFP (FG)

Pin	Name	Pin	Name
1	SW5	25	VNN
2	N/C	26	N/C
3	SW4	27	N/C
4	N/C	28	GND
5	SW4	29	VDD
6	N/C	30	N/C
7	N/C	31	N/C
8	SW3	32	N/C
9	N/C	33	DIN
10	SW3	34	CLK
11	N/C	35	$\overline{\text{LE}}$
12	SW2	36	CLR
13	N/C	37	DOUT
14	SW2	38	N/C
15	N/C	39	SW7
16	SW1	40	N/C
17	N/C	41	SW7
18	SW1	42	N/C
19	N/C	43	SW6
20	SW0	44	N/C
21	N/C	45	SW6
22	SW0	46	N/C
23	N/C	47	SW5
24	VPP	48	N/C

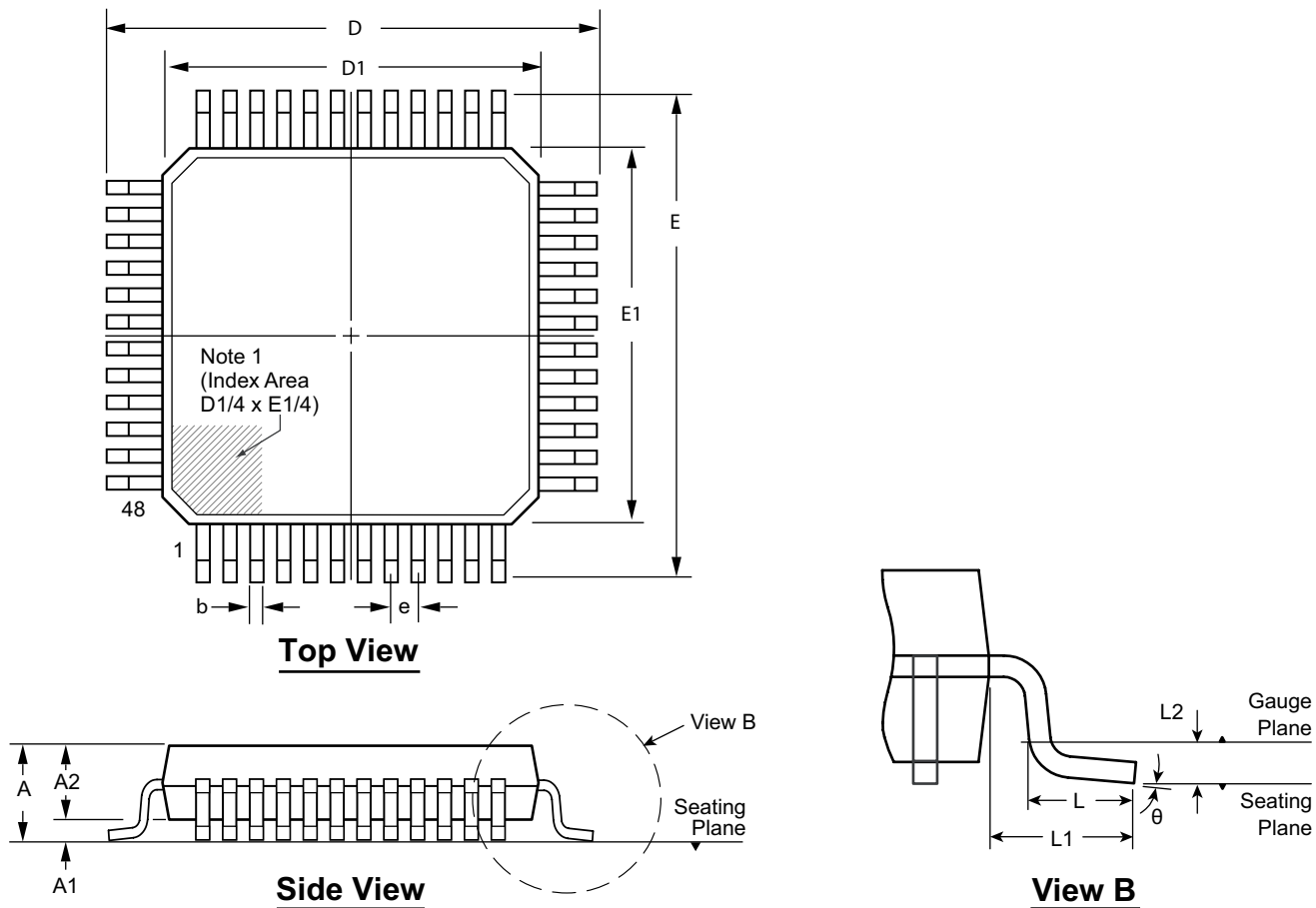
## Pin Description - 28-Lead PLCC (PJ)

Pin	Name	Pin	Name
1	SW3	15	N/C
2	SW3	16	DIN
3	SW2	17	CLK
4	SW2	18	$\overline{\text{LE}}$
5	SW1	19	CL
6	SW1	20	DOUT
7	SW0	21	SW7
8	SW0	22	SW7
9	N/C	23	SW6
10	VPP	24	SW6
11	N/C	25	SW5
12	VNN	26	SW5
13	GND	27	SW4
14	VDD	28	SW4



# 48-Lead LQFP Package Outline (FG)

7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



**Note:**  
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75			7°

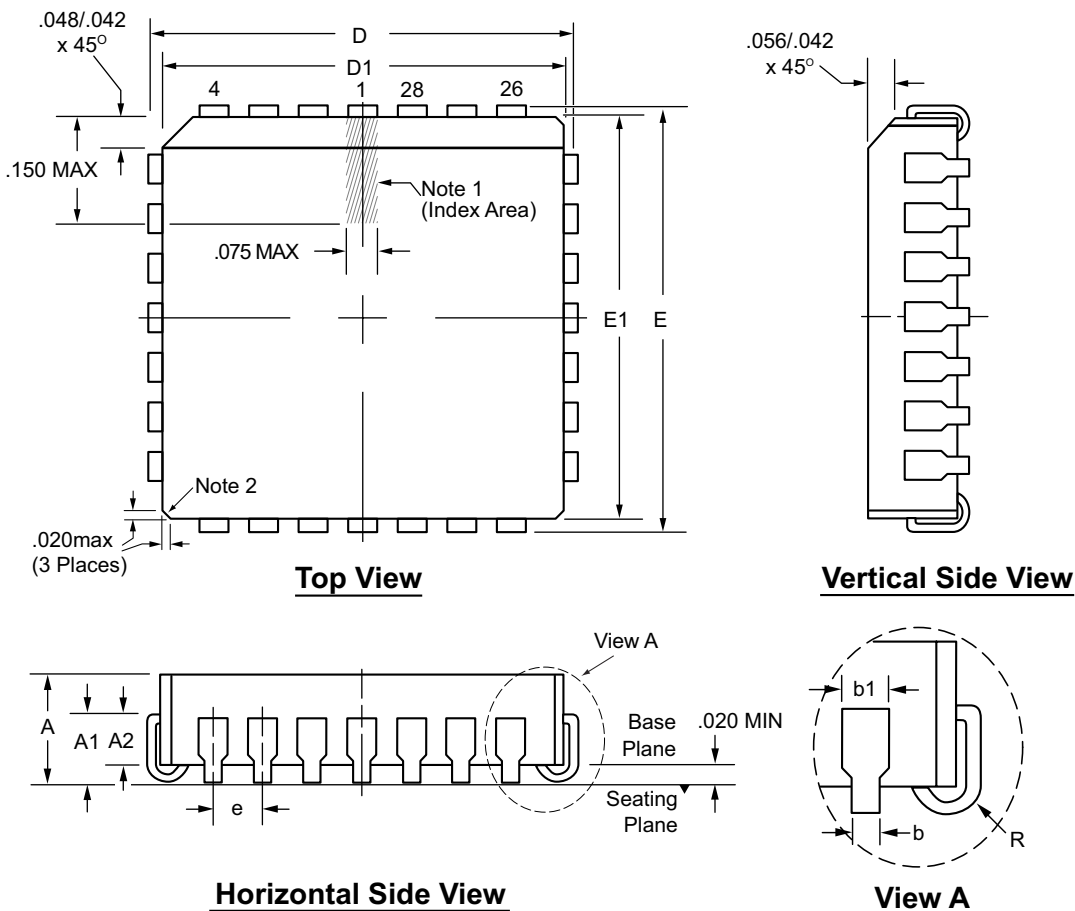
JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.  
\* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-48LQFPFG Version, D041309.

# 28-Lead PLCC Package Outline (PJ)

.453x.453in. body, .180in. height (max), .050in. pitch



**Notes:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.485	.450	.485	.450	.050 BSC	.025
	NOM	.172	.105	-	-	-	.490	.453	.490	.453		.035
	MAX	.180	.120	.083	.021	.032	.495	.456	.495	.456		.045

JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.

Drawings not to scale.

Supertex Doc. #: DSPD-28PLCCPJ, Version B031111.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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[74HC2G66DC.125](#) [DG3257DN-T1-GE4](#) [ADG1611BRUZ-REEL7](#) [DG2535EDQ-T1-GE3](#) [LTC201ACN#PBF](#) [74LV4066DB,118](#)