

250V Low Charge Injection, 8-Channel, High Voltage Analog Switch

Features

- ▶ HVCMOS® technology for high performance
- ▶ Very low quiescent power dissipation (-10µA)
- ▶ Low parasitic capacitances
- ▶ DC to 50MHz small signal frequency response
- ▶ -60dB typical output off isolation at 5.0MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ On-chip shift register, latch and clear logic circuitry
- ▶ Flexible high voltage supplies
- ▶ Surface mount packages

Applications

- ▶ Medical ultrasound imaging
- ▶ Non-destructive evaluation
- ▶ Inkjet printer heads
- ▶ Optical MEMS modules

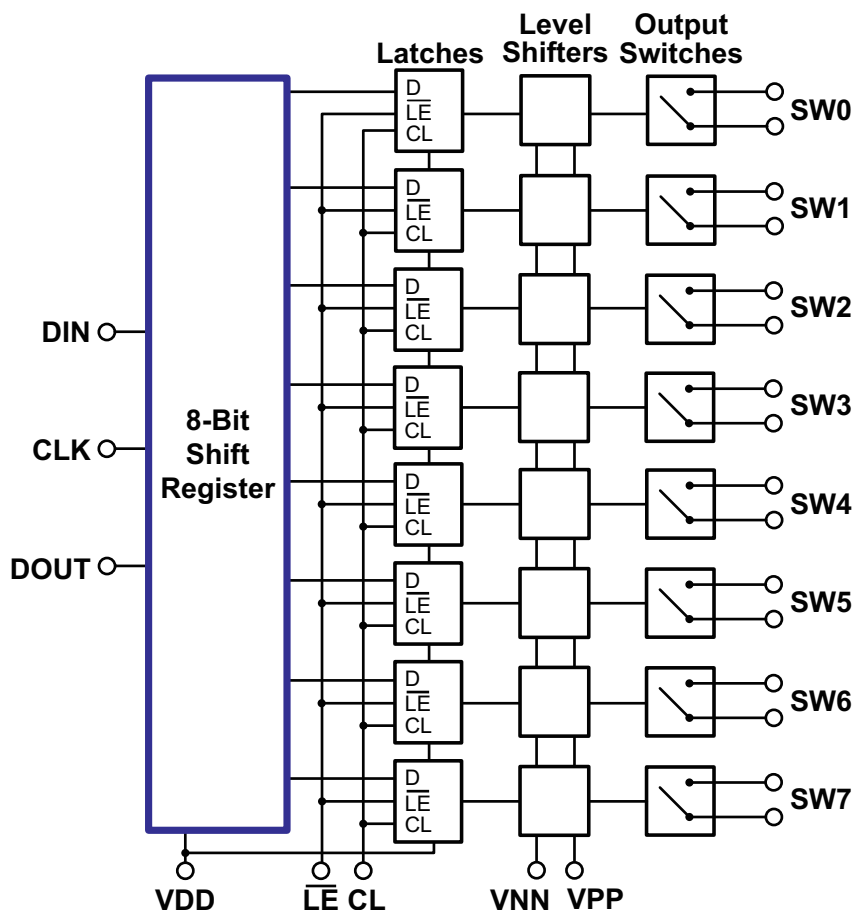
General Description

The Supertex HV214 is a low charge injection, 8-channel, high voltage, analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging, piezoelectric transducer drivers, inkjet printer heads and optical MEMS modules.

Input data is shifted into an 8-bit shift register that can then be retained in an 8-bit latch. To reduce any possible clock feedthrough noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS® technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +40V/-210V, +125V/-125V, +210V/-40V.

Block Diagram



Ordering Information

Part Number	Package Option	Packing
HV214FG-G	48-Lead LQFP	250/Tray
HV214FG-G M931		1000/Reel
HV214PJ-G	28-Lead PLCC	38/Tube
HV214PJ-G M904		500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

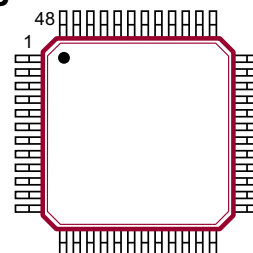
Parameter	Value
V_{DD} logic power supply voltage	-0.5V to +15V
$V_{PP} - V_{NN}$ supply voltage	260V
V_{PP} positive high voltage supply	-0.5V to $V_{NN} + 250V$
V_{NN} negative high voltage supply	+0.5V to -260V
Logic input voltages	-0.5V to $V_{DD} + 0.3V$
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	2.5A
Storage temperature	-65°C to +150°C
Power dissipation:	
48-Lead LQFP	1.0W
28-Lead PLCC	1.2W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

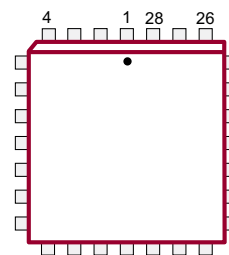
Operating Conditions

Sym	Parameter	Value
V_{DD}	Logic power supply voltage	4.5V to 13.2V
V_{PP}	Positive high voltage supply	40V to $V_{NN} + 250V$
V_{NN}	Negative high voltage supply	-40V to -210V
V_{IH}	High level input logic voltage	$V_{DD} - 1.5V$ to V_{DD}
V_{IL}	Low-level input logic voltage	0V to 1.5V
V_{SIG}	Analog signal voltage peak-to-peak	$V_{NN} + 10V$ to $V_{PP} - 10V$
T_A	Operating free air temperature	0°C to 70°C

Pin Configuration



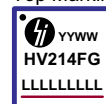
48-Lead LQFP
(top view)



28-Lead PLCC
(top view)

Product Marking

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
— = "Green" Packaging
*May be part of top marking

Bottom Marking



Package may or may not include the following marks: Si or

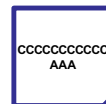
48-Lead LQFP

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
— = "Green" Packaging
*May be part of top marking

Bottom Marking



Package may or may not include the following marks: Si or

28-Lead PLCC

Typical Thermal Resistance

Package	θ_{ja}
48-Lead LQFP	52°C/W
28-Lead PLCC	48°C/W

DC Electrical Characteristics ($T_A = 25^\circ\text{C}$, over recommended operating conditions unless otherwise noted)

Sym	Parameter	Min	Typ	Max	Units	Conditions
R_{ONS}	Small signal switch on-resistance	-	-	55	Ω	$I_{SIG} = 5.0\text{mA}$ $V_{PP} = +40\text{V}$ $V_{NN} = -210\text{V}$
		-	-	49		$I_{SIG} = 200\text{mA}$
		-	-	42		$I_{SIG} = 5.0\text{mA}$ $V_{PP} = +125\text{V}$ $V_{NN} = -125\text{V}$
		-	-	36		$I_{SIG} = 200\text{mA}$
		-	-	38		$I_{SIG} = 5.0\text{mA}$ $V_{PP} = +210\text{V}$ $V_{NN} = -40\text{V}$
		-	-	32		$I_{SIG} = 200\text{mA}$
ΔR_{ONS}	Small signal switch on-resistance matching	-	-	20	%	$I_{SIG} = 5.0\text{mA}$, $V_{PP} = +125\text{V}$, $V_{NN} = -125\text{V}$
R_{ONL}	Large signal switch on-resistance	-	23	-	Ω	$V_{SIG} = V_{PP} - 10\text{V}$, $I_{SIG} = 1.0\text{A}$
I_{SOL}	Switch off leakage per switch	-	-	10	μA	$V_{SIG} = V_{PP} - 10\text{V}$ & $V_{NN} + 10\text{V}$
V_{OS}	DC offset switch off	-	-	300	mV	$R_{LOAD} = 100\text{k}\Omega$
	DC offset switch on	-	-	500	mV	$R_{LOAD} = 100\text{k}\Omega$
I_{PPQ}	Quiescent V_{PP} supply current	-	-	50	μA	All switches off
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-50	μA	All switches off
I_{PPQ}	Quiescent V_{PP} supply current	-	-	50	μA	All switches on, $I_{SW} = 5.0\text{mA}$
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-50	μA	All switches on, $I_{SW} = 5.0\text{mA}$
I_{SW}	Switch output peak current	-	-	2.0	A	V_{SIG} duty cycle 0.1%
f_{SW}	Output switch frequency	-	-	50	kHz	Duty cycle = 50%
I_{PP}	Average V_{PP} supply current	-	-	7.0	mA	$V_{PP} = +40\text{V}$ $V_{NN} = -210\text{V}$
		-	-	5.0		$V_{PP} = +125\text{V}$ $V_{NN} = -125\text{V}$
		-	-	5.0		$V_{PP} = +210\text{V}$ $V_{NN} = -40\text{V}$
I_{NN}	Average V_{NN} supply current	-	-	-7.0	mA	$V_{PP} = +40\text{V}$ $V_{NN} = -210\text{V}$
		-	-	-5.0		$V_{PP} = +125\text{V}$ $V_{NN} = -125\text{V}$
		-	-	-5.0		$V_{PP} = +210\text{V}$ $V_{NN} = -40\text{V}$
I_{DD}	Average V_{DD} supply current	-	-	10	mA	$f_{CLK} = 5.0\text{MHz}$, $V_{DD} = 5.0\text{V}$
I_{DDQ}	Quiescent V_{DD} supply current	-	-	4.0	μA	---
I_{SOR}	Data out source current	45	-	-	mA	$V_{OUT} = V_{DD} - 0.7\text{V}$
I_{SINK}	Data out sink current	45	-	-	mA	$V_{OUT} = 0.7\text{V}$
C_{IN}	Large input capacitance	-	-	10	pF	---
T_A	Ambient temperature range	0	-	70	$^\circ\text{C}$	---

AC Electrical Characteristics ($V_{DD} = 5.0V$, $T_A = 25^\circ C$, over recommended operating conditions unless otherwise noted)

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_{SD}	Set-up time before \overline{LE} rises	150	-	-	ns	---
t_{WLE}	Time width of \overline{LE}	150	-	-	ns	---
t_{DO}	Clock delay time to data out	-	-	150	ns	---
t_{WCL}	Time width of CL	150	-	-	ns	---
t_{SU}	Set-up time data to clock	15	8.0	-	ns	---
t_H	Hold time data from clock	35	-	-	ns	---
f_{CLK}	Clock frequency	-	-	5.0	MHz	50% duty cycle, $f_{DATA} = f_{CLK}/2$
t_R, t_F	Clock rise and fall times	-	-	50	ns	---
T_{ON}	Turn-on time	-	-	5.0	μs	$V_{SIG} = V_{PP} - 10V$, $R_{LOAD} = 10k\Omega$
T_{OFF}	Turn-off time	-	-	5.0	μs	$V_{SIG} = V_{PP} - 10V$, $R_{LOAD} = 10k\Omega$
dv/dt	Maximum V_{SIG} slew rate	-	-	20	V/ns	$V_{PP} = +40V$, $V_{NN} = -160V$
		-	-	20		$V_{PP} = +125V$, $V_{NN} = -100V$
		-	-	20		$V_{PP} = +210V$, $V_{NN} = -40V$
K_O	Off isolation	-30	-	-	dB	$f = 5.0MHz$, $1k\Omega/15pF$ load
		-58	-	-		$f = 5.0MHz$, 50Ω load
K_{CR}	Switch crosstalk	-60	-	-	dB	$f = 5.0MHz$, 50Ω load
I_{ID}	Output switch isolation diode current	-	-	300	mA	300ns pulse width, 2% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	5.0	12	17	pF	0V, $f = 1.0MHz$
$C_{SG(ON)}$	On capacitance SW to GND	25	38	50	pF	0V, $f = 1.0MHz$
$+V_{SPK}$	Output voltage spike	-	-	200	mV	$V_{PP} = +40V$, $V_{NN} = -210V$, $R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	200		
$+V_{SPK}$		-	-	200		$V_{PP} = +125V$, $V_{NN} = -125V$, $R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	200		
$+V_{SPK}$		-	-	200		$V_{PP} = +210V$, $V_{NN} = -40V$, $R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	200		

Power Up/Down Sequence:

1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.
3. Rise and fall times of power supplies V_{DD} , V_{PP} , and V_{NN} should not be less than 1.0msec.

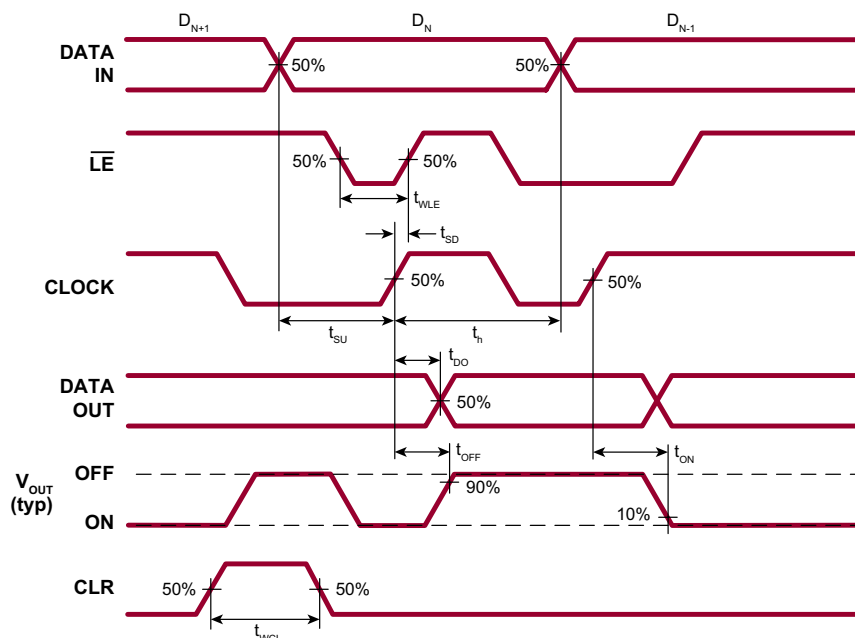
Truth Table

Data in 8-Bit Shift Register								\overline{LE}	CL	Output Switch State							
D0	D1	D2	D3	D4	D5	D6	D7			SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	Hold Previous State							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

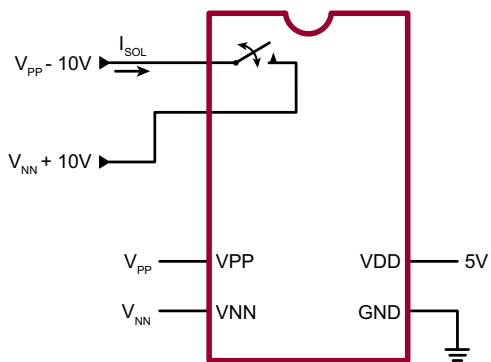
Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L→H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of \overline{LE} . When \overline{LE} is low the shift register data flows through the latch.
4. D_{OUT} is high when data in the shift register 7 is high.
5. Shift register clocking has no effect on the switch states if \overline{LE} is H.
6. The clear input overrides all other inputs.

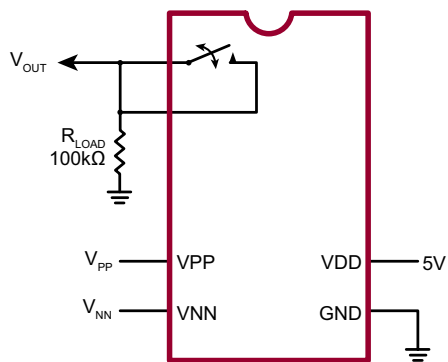
Logic Timing Waveforms



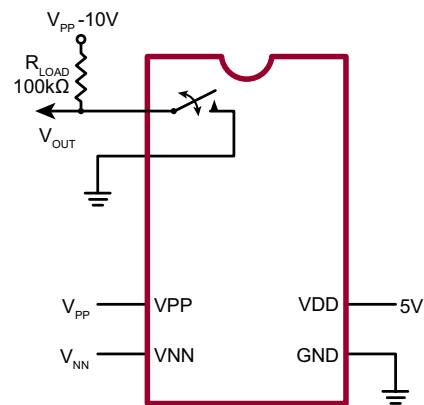
Test Circuits



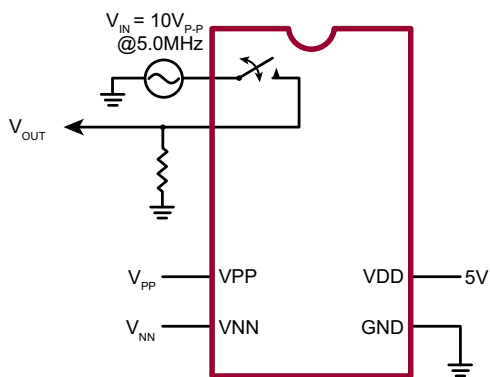
Switch OFF Leakage



DC Offset ON/OFF

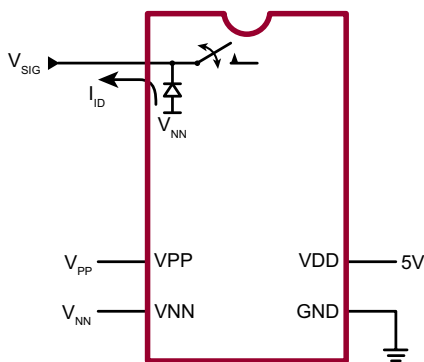


T_{ON}/T_{OFF} Test Circuit

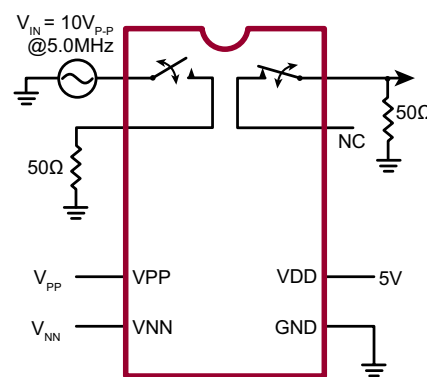


$$K_O = 20 \text{ Log } \frac{V_{OUT}}{V_{IN}}$$

OFF Isolation

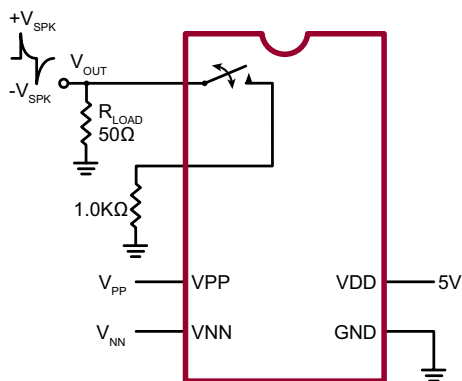


Isolation Diode Current



$$K_{CR} = 20 \text{ Log } \frac{V_{OUT}}{V_{IN}}$$

Crosstalk



Output Voltage Spike

48-Lead LQFP Pin Description

Pin	Function
1	SW5
2	NC
3	SW4
4	NC
5	SW4
6	NC
7	NC
8	SW3
9	NC
10	SW3
11	NC
12	SW2

Pin	Function
13	NC
14	SW2
15	NC
16	SW1
17	NC
18	SW1
19	NC
20	SW0
21	NC
22	SW0
23	NC
24	VPP

Pin	Function
25	VNN
26	NC
27	NC
28	GND
29	VDD
30	NC
31	NC
32	NC
33	DIN
34	CLK
35	\overline{LE}
36	CLR

Pin	Function
37	DOUT
38	NC
39	SW7
40	NC
41	SW7
42	NC
43	SW6
44	NC
45	SW6
46	NC
47	SW5
48	NC

28-Lead PLCC Pin Description

Pin	Function
1	SW3
2	SW3
3	SW2
4	SW2
5	SW1
6	SW1
7	SW0

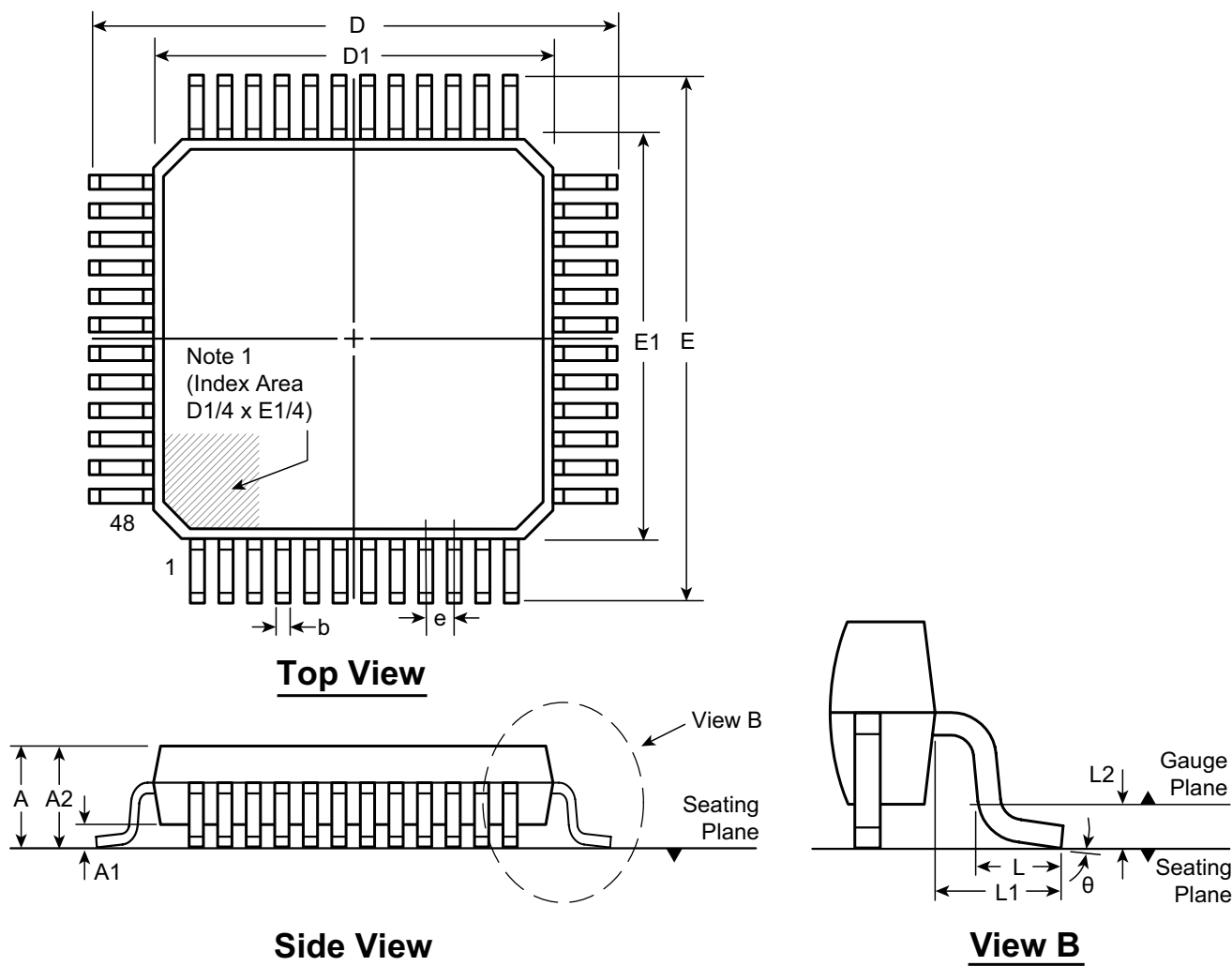
Pin	Function
8	SW0
9	NC
10	VPP
11	NC
12	VNN
13	GND
14	VDD

Pin	Function
15	NC
16	DIN
17	CLK
18	\overline{LE}
19	CL
20	DOUT
21	SW7

Pin	Function
22	SW7
23	SW6
24	SW6
25	SW5
26	SW5
27	SW4
28	SW4

48-Lead LQFP Package Outline (FG)

7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60		3.5°	
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75		7°	

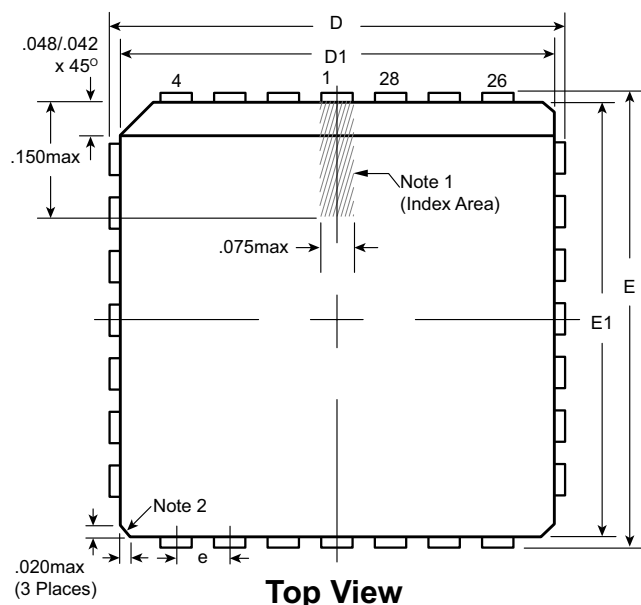
JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.
 * This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

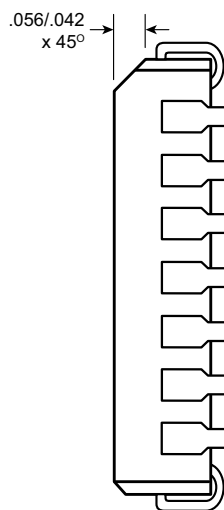
Supertex Doc. #: DSPD-48LQFPFG Version, D041309.

28-Lead PLCC Package Outline (PJ)

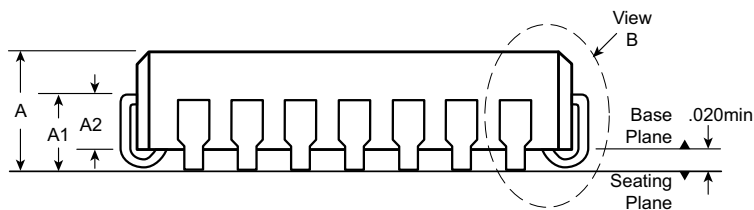
.453x.453in. body, .180in. height (max), .050in. pitch



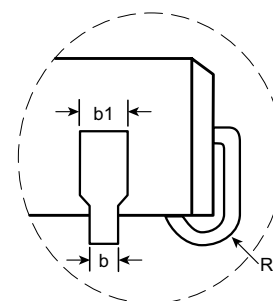
Top View



Vertical Side View



Horizontal Side View



View B

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.485	.450	.485	.450	.050 BSC	.025
	NOM	.172	.105	-	-	-	.490	.453	.490	.453		.035
	MAX	.180	.120	.083	.021	.032	.495	.456	.495	.456		.045

JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.

Drawings not to scale.

Supertex Doc. #: DSPD-28PLCCPJ, Version B031111.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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