HV2621/HV2721/HV2722

300V, Low-Charge Injection, 16-Channel, High-Voltage Analog Switch

Features

- 300V,16-Channel High-Voltage Analog Switch
- 3.3V or 5.0V CMOS Input Logic Level
- 33 MHz Data Shift Clock Frequency
- Very Low Quiescent Current (10 µA)
- Low Parasitic Capacitance
- DC to 50 MHz Analog Small-Signal Frequency
- -60 dB Typical Off Isolation at 5.0 MHz
- Excellent Noise Immunity
- Cascadable Serial Data Register with Latches
- Flexible Operating Supply Voltage
- Integrated Bleed Resistors on the Outputs (both sides for HV2721, one side only for HV2722)

Applications

- Medical Ultrasound Imaging
- Nondestructive Testing (NDT) Metal Flaw Detection
- Multi-Layer Printed Circuit Board (PCB) Tester
- Piezoelectric Transducer Drivers
- Inkjet Printer Head
- Optical MEMS Module

General Description

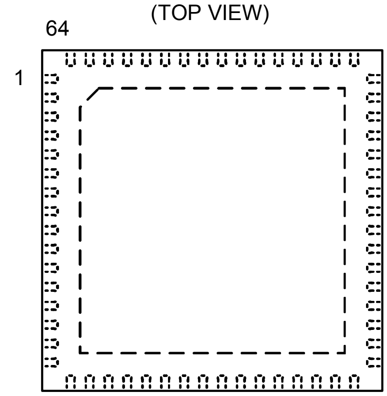
The HV2621/HV2721/HV2722 devices are 300V, low-charge injection, 16-channel, high-voltage analog switches. These devices are designed for use in applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging, piezoelectric transducer drivers. HV2621/HV2721 are almost identical to HV2601/2701 but have larger signal range. If V_{PP}/V_{NN} = ±150V, HV2621/HV2721/HV2722 can pass the analog signal up to ±135V.

The HV2721 has integrated bleed resistors on both sides of the switches. HV2722 has integrated bleed resistors on one side, SWxA only. HV2621 has no bleed resistors. The bleed resistor eliminates voltage build-up on capacitive loads such as piezoelectric transducers.

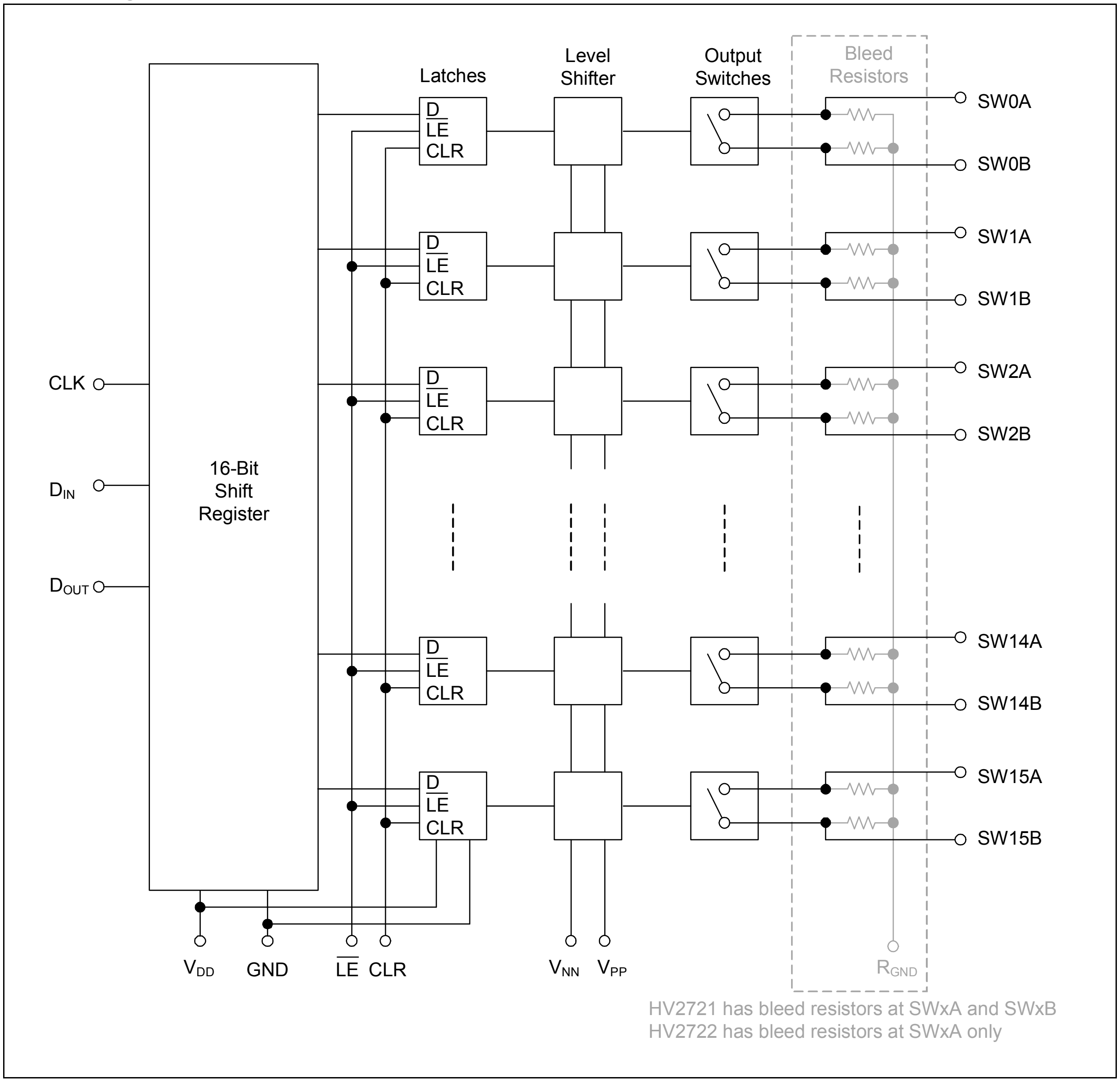
Input data are shifted into a 16-bit shift register that can then be retained in a 16-bit latch. To change all the switch state at the same time, the latch enable bar should be left high until all bits are clocked in. The input data are clocked in at the rising edge of the clock. After all bits are clocked in to the shift register, a negative pulse of the latch enable bar changes all the switch ON/OFF states defined by input data at the same time. Using the HVCMOS technology, these devices combine 300V high-voltage bilateral DMOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals.

These devices are suitable for various combinations of high-voltage supplies, e.g., V_{PP}/V_{NN}: +60V/-240V, +150V/-150V, and +260V/-40V.

Package Types



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Logic Supply Voltage (V_{DD}) .... -0.5V to 6.5V
Differential Supply Voltage (V_{PP}-V_{NN}) 330V
Positive Supply Voltage (V_{PP}) .... -0.5V to V_{NN}+300V
Negative Supply Voltage (V_{NN}) .... -300V to +0.5V
Logic Input Voltage (V_{IN}) .... -0.5V to V_{DD} +0.3V
Analog Signal Range (V_{SIG}) .... V_{NN} to V_{PP}
Peak Analog Signal Current/Channel (I_{PK}) 3A

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES 1, 2, 3)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Logic Supply Voltage	V_{DD}	3	—	5.5	V	
Differential Supply Voltage	V_{PP}-V_{NN}	60	—	300	V	
Positive Supply Voltage	V_{PP}	60	—	260	V	
Negative Supply Voltage	V_{NN}	-240	—	0	V	
High-Level Input Voltage	V_{IH}	0.9V_{DD}	—	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.1V_{DD}	V	
Analog Signal Voltage Peak-to-Peak	V_{SIG}	V_{NN}+15	—	V_{PP}-15	V	

Note 1: Recommended power up sequence is V_{DD}, V_{PP} and V_{NN}. Power down is in reverse order.
2: V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.
3: Rise and fall times of power supplies, V_{DD}, V_{PP} and V_{NN} should be greater than 1.0 ms.

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{PP} = +150V, V_{NN} = -150V, V_{DD} = 5.0V, T_A = 25°C. **Boldface** specifications apply over the full operating temperature range.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions/Comments	
Small Signal Switch On-Resistance	R_{ONS}	—	26	**48**	Ω	I_{SIG} = 5 mA	V_{PP} = +60V, V_{NN} = -240V
		—	22	**32**	Ω	I_{SIG} = 150 mA	
		—	22	**30**	Ω	I_{SIG} = 5 mA	V_{PP} = +150V, V_{NN} = -150V
		—	18	**27**	Ω	I_{SIG} = 150 mA	
		—	20	**30**	Ω	I_{SIG} = 5 mA	V_{PP} = +260V, V_{NN} = -40V
		—	16	**27**	Ω	I_{SIG} = 150 mA	
Small Signal Switch On-Resistance Matching	ΔR_{ONS}	—	5	**20**	%	I_{SIG} = 5 mA, V_{PP} = +150V, V_{NN} = -150V	
Large Signal Switch On-Resistance	R_{ONL}	—	17	—	Ω	V_{SIG} = V_{PP}-15V, I_{SIG} =1A	
Value of Output Bleed Resistor (HV2721/HV2722 Only)	R_{INT}	30	50	70	kΩ	Output switch to RGND, I_{RINT} = 0.5 mA	
Switch Off Leakage per Switch	I_{SOL}	—	1	**15**	µA	V_{SIG} = V_{PP}-15V, V_{NN}+15V. See Figure 3-1	
DC Offset Switch Off	V_{OS}	—	1	**10**	mV	R_{LOAD} = 35 kΩ (HV2621), 70 kΩ (HV2722), No load (HV2721), see Figure 3-2	
DC Offset Switch On		—	1	**10**			

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, V_{PP} = +150V, V_{NN} = -150V, V_{DD} = 5.0V, T_A = 25°C. **Boldface** specifications apply over the full operating temperature range.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions/Comments	
Quiescent V_{PP} Supply Current	I_{PPQ}	—	10	**50**	µA	All switches off	
Quiescent V_{NN} Supply Current	I_{NNQ}	—	10	**50**	µA		
Quiescent V_{PP} Supply Current	I_{PPQ}	—	10	**50**	µA	All switches on, I_{SW} = 5.0 mA	
Quiescent V_{NN} Supply Current	I_{NNQ}	—	10	**50**	µA		
Switch Output Peak Current	I_{SW}	2.0	3.0	—	A	V_{SIG} duty cycle <0.1% (**Note 1**)	
Output Switching Frequency	f_{SW}	—	—	50	kHz	Duty cycle = 50% (**Note 1**)	
Average V_{PP} Supply Current	I_{PP}	—	—	**3**	mA	V_{PP} = +60V, V_{NN} = -240V	All output switches are turning on and off at 10 kHz with no load
		—	—	**4**	mA	V_{PP} = +150V, V_{NN} = -150V	
		— —	—	**6**	mA	V_{PP} = +260V, V_{NN} = -40V	
Average V_{NN} Supply Current	I_{NN}	—	—	**3**	mA	V_{PP} = +60V, V_{NN} = -240V	All output switches are turning on and off at 10 kHz with no load
		—	—	**4**	mA	V_{PP} = +150V, V_{NN} = -150V	
		— —	—	**6**	mA	V_{PP} = +260V, V_{NN} = -40V	
Average V_{DD} Supply Current	I_{DD}	—	—	**4**	mA	f_{CLK} = 5 MHz, f_{DIN}= 2.5 MHz	
Quiescent V_{DD} Supply Current	I_{DDQ}	—	—	**10**	µA	All logic inputs are static	
Data Out Source Current	I_{SOR}	**8**	—	—	mA	V_{OUT} = V_{DD} -0.7V	
Data Out Sink Current	I_{SINK}	**12**	—	—	mA	V_{OUT} = 0.7V	
Logic Input Capacitance	C_{IN}	—	—	10	pF	**Note 2**	

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Design guidance only.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{PP} = +150V, V_{NN} = -150V, V_{DD} = 5.0V, $t_R = t_F \leq$ 5.0 ns, 50% duty cycle, C_{LOAD} = 20 pF, T_A = 25°C, **Boldface** specifications apply over the full operating temperature range.

Sym.	Sym.	Min.	Typ.	Max.	Units	Conditions/Comments
Setup Time before $\overline{LE}$ rises	t_{SD}	**25**	—	—	ns	**Note 1**
Time Width of $\overline{LE}$	t_{WLE}	**56**	—	—	ns	V_{DD} = 3.3V (**Note 1**)
		12	—	—	ns	V_{DD} = 5.0V (**Note 1**)
Clock Delay Time to Data Out	t_{DO}	-	—	**45**	ns	V_{DD} = 3.3V
		-	—	**25**	ns	V_{DD} = 5.0V
Time Width of CLR	t_{WCLR}	**55**	—	—	ns	**Note 1**
Setup Time Data to Clock	t_{SU}	**7**	—	—	ns	V_{DD} = 3.3V (**Note 1**)
		7	—	—	ns	V_{DD} = 5.0V (**Note 1**)
Hold Time Data from Clock	t_H	**4**	—	—	ns	V_{DD} = 3.3V (**Note 1**)
		3.5			ns	V_{DD} = 5.0V (**Note 1**)

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, V_{PP} = +150V, V_{NN} = -150V, V_{DD} = 5.0V, t_R = t_F ≤ 5.0 ns, 50% duty cycle, C_{LOAD} = 20 pF, T_A = 25°C, **Boldface** specifications apply over the full operating temperature range.

Sym.	Sym.	Min.	Typ.	Max.	Units	Conditions/Comments
Clock Frequency	f_{CLK}	—	—	**16**	MHz	V_{DD} = 3.3V (**Note 1**)
		—	—	**33**	MHz	V_{DD} = 5.0V (**Note 1**)
Clock Rise and Fall Time	t_R, t_F	—	—	**50**	ns	**Note 1**
Turn-On Time	t_{ON}	—	—	**6**	µs	V_{SIG} = V_{PP}-15V, R_{LOAD} = 20 kΩ See Figure 3-3
Turn-Off Time	t_{OFF}	—	—	**6**		
Maximum V_{SIG} Slew Rate	dV/dt	—	—	20	V/ns	V_{PP} = +60V, V_{NN} = -240V (**Note 1**)
		—	—	20		V_{PP} = +150V, V_{NN} = -150V (**Note 1**)
		—	—	20		V_{PP} = +260V, V_{NN} = -40V (**Note 1**)
Off Isolation	K_O	—	-55	-50	dB	f = 5.0 MHz,1.0 kΩ//15 pF load See Figure 3-4 (**Note 1**)
		—	-60	-58		f = 5.0 MHz, 50Ω load See Figure 3-4 (**Note 1**)
Switch Crosstalk	K_{CR}	—	-70	-60	dB	f = 5.0 MHz, 50Ω load See Figure 3-5 (**Note 1**)
Output Switch Isolation Diode Current	I_{ID}	—	—	200	mA	300 ns pulse width, 2.0% duty cycle, See Figure 3-6 (**Note 1**)
Off Capacitance SW to GND	$C_{SG(OFF)}$	—	10	—	pF	V_{SIG} = 50 mV@1MHz, no load (**Note 1**)
On Capacitance SW to GND	$C_{SG(ON)}$	—	18	—		
Output Voltage Spike at SWA, SWB	$+V_{SPK}$	—	—	250	mV	V_{PP} = +60V, V_{NN} = -240V, R_{LOAD} = 50Ω, see Figure 3-7 (**Note 1**)
	$-V_{SPK}$	-250	—	—		
	$+V_{SPK}$	—	—	250		V_{PP} = +150V, V_{NN} = -150V, R_{LOAD} = 50Ω, see Figure 3-7 (**Note 1**)
	$-V_{SPK}$	-250	—	—		
	$+V_{SPK}$	—	—	250		V_{PP} = +260V, V_{NN} = -40V, R_{LOAD} = 50Ω, see Figure 3-7 (**Note 1**)
	$-V_{SPK}$	-250	—	—		
Charge Injection	QC	—	1000	—	pC	V_{PP} = +60V, V_{NN} = -240V, V_{SIG} = 0V, see Figure 3-8 (**Note 1**)
		—	770	—		V_{PP} = +150V, V_{NN} = -150V, V_{SIG} = 0V, see Figure 3-8 (**Note 1**)
		—	360	—		V_{PP} = +260V, V_{NN} = -40V, V_{SIG}=0V, see Figure 3-8 (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATION

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Range						
Operating Temperature Range	T_A	0	—	+70	°C	
Storage Temperature Range	T_S	-65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+125	°C	
Package Thermal Resistance						
Thermal Resistance, 64L QFN	Θ_{JA}	—	21	—	°C/W	

TABLE 1-1: TRUTH TABLE (NOTES 1, 2, 3, 4, 5, 6)

D0	D1	...	D7	D8	...	D15	$\overline{LE}$	CLR	SW0	SW1	...	SW7	SW8	...	SW15
L	—		—	—		—	L	L	OFF	—		—	—		—
H	—		—	—		—	L	L	ON	—		—	—		—
—	L		—	—		—	L	L	—	OFF		—	—		—
—	H		—	—		—	L	L	—	ON		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—	...	L	—	...	—	L	L	—	—	...	OFF	—	...	—
—	—		H	—		—	L	L	—	—		ON	—		—
—	—		—	L		—	L	L	—	—		—	OFF		—
—	—		—	H		—	L	L	—	—		—	ON		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		L	L	L	—	—		—	—		OFF
—	—		—	—		H	L	L	—	—		—	—		ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Note 1: The 16 switches operate independently.
2: Serial data is clocked in on the L to H transition of the CLK.
3: All 16 switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the shift registers data flow through the latch.
4: DOUT is high when data in the register 15 is high.
5: Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.
6: The CLR clear input overrides all the inputs.

1.1 Typical Timing Diagrams

Figure 1-1 shows the timing of the AC characteristic parameters graphically.

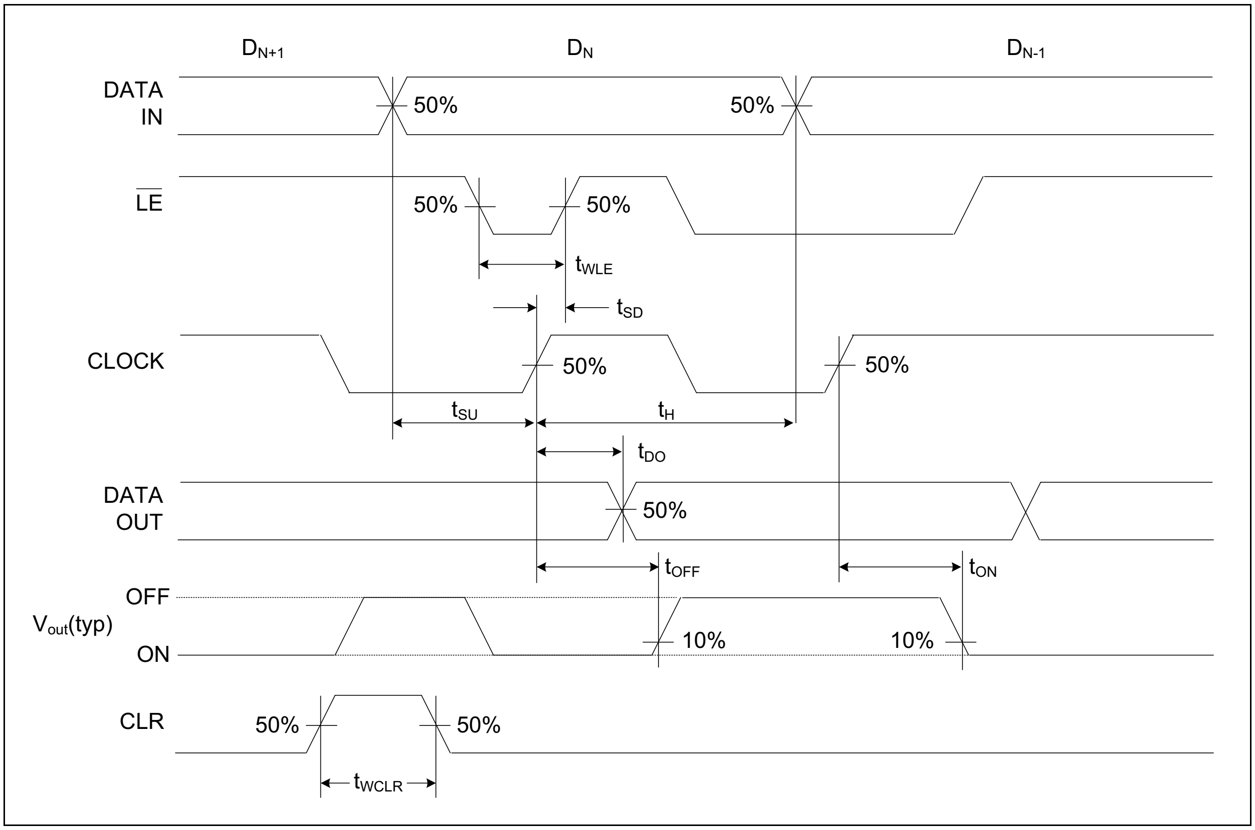


FIGURE 1-1: *Logic Input Timing Diagram.*

2.0 PIN DESCRIPTION

This section details the pin description for 64-lead QFN package (Figure 2-1).The descriptions of the pins are listed in Table 2-1.

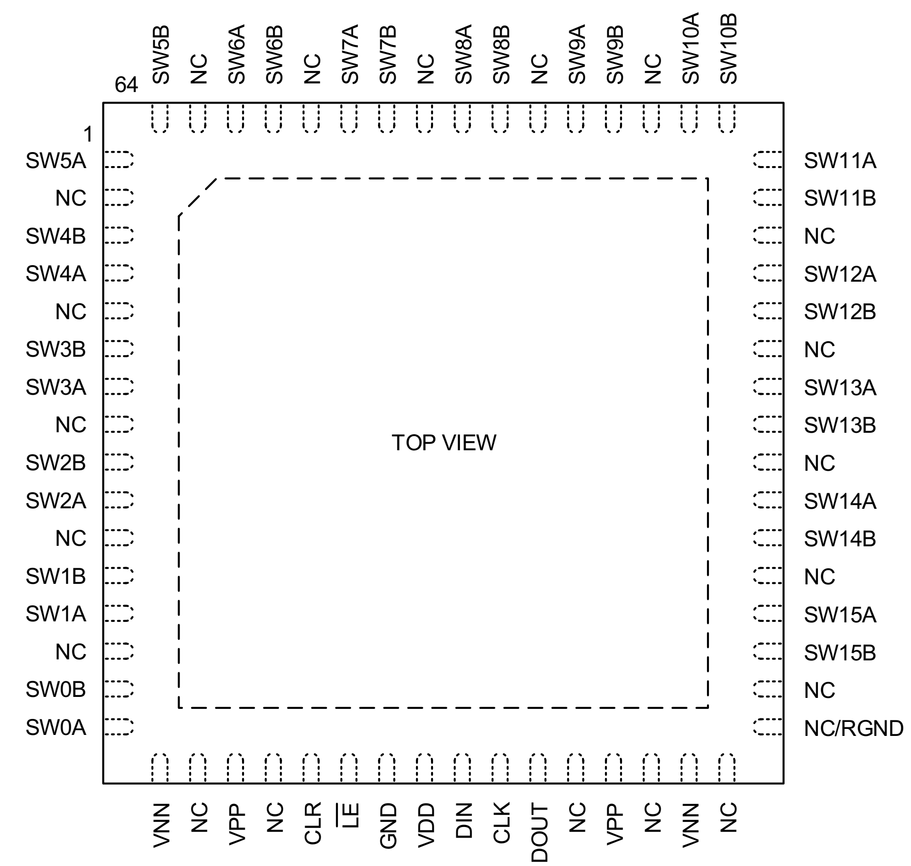


FIGURE 2-1: *64-Lead QFN Package - Top View.*

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol		Description
	HV2621	HV2721/ HV2722	
1	SW5A	SW5A	Analog Switch 5 Terminal A
2	NC	NC	No Connection
3	SW4B	SW4B	Analog Switch 4 Terminal B
4	SW4A	SW4A	Analog Switch 4 Terminal A
5	NC	NC	No Connection
6	SW3B	SW3B	Analog Switch 3 Terminal B
7	SW3A	SW3A	Analog Switch 3 Terminal A
8	NC	NC	No Connection
9	SW2B	SW2B	Analog Switch 2 Terminal B
10	SW2A	SW2A	Analog Switch 2 Terminal A
11	NC	NC	No Connection

Pin Number	Symbol		Description
	HV2621	HV2721/ HV2722	
12	SW1B	SW1B	Analog Switch 1 Terminal B
13	SW1A	SW1A	Analog Switch 1 Terminal A
14	NC	NC	No Connection
15	SW0B	SW0B	Analog Switch 0 Terminal B
16	SW0A	SW0A	Analog Switch 0 Terminal A
17	V_{NN}	V_{NN}	Negative Supply Voltage
18	NC	NC	No Connection
19	V_{PP}	V_{PP}	Positive Supply Voltage
20	NC	NC	No Connection
21	CLR	CLR	Latch Clear Logic Input
22	$\overline{LE}$	$\overline{LE}$	Latch Enable Logic Input
23	GND	GND	Ground
24	V_{DD}	V_{DD}	Logic Supply Voltage
25	D_{IN}	D_{IN}	Data In Logic Input
26	CLK	CLK	Clock Logic Input for Shift Register
27	D_{OUT}	D_{OUT}	Data Out Logic Output
28	NC	NC	No Connection
29	V_{PP}	V_{PP}	Positive Supply Voltage
30	NC	NC	No Connection
31	V_{NN}	V_{NN}	Negative Supply Voltage
32	NC	NC	No Connection
33	NC	RGND	No Connection/Ground for Bleed Resistor
34	NC	NC	No Connection
35	SW15B	SW15B	Analog Switch 15 Terminal B
36	SW15A	SW15A	Analog switch 15 Terminal A
37	NC	NC	No Connection
38	SW14B	SW14B	Analog Switch 14 Terminal B
39	SW14A	SW14A	Analog Switch 14 Terminal A
40	NC	NC	No Connection
41	SW13B	SW13B	Analog Switch 13 Terminal B
42	SW13A	SW13A	Analog switch 13 Terminal A
43	NC	NC	No Connection
44	SW12B	SW12B	Analog Switch 12 Terminal B
45	SW12A	SW12A	Analog Switch 12 Terminal A
46	NC	NC	No Connection
47	SW11B	SW11B	Analog Switch 11 Terminal B
48	SW11A	SW11A	Analog Switch 11 Terminal A
49	SW10B	SW10B	Analog Switch 10 Terminal B
50	SW10A	SW10A	Analog Switch 10 Terminal A
51	NC	NC	No Connection
52	SW9B	SW9B	Analog Switch 9 Terminal B
53	SW9A	SW9A	Analog Switch 9 Terminal A
54	NC	NC	No Connection

Pin Number	Symbol		Description
	HV2621	HV2721/ HV2722	
55	SW8B	SW8B	Analog Switch 8 Terminal B
56	SW8A	SW8A	Analog Switch 8 Terminal A
57	NC	NC	No Connection
58	SW7B	SW7B	Analog Switch 7 Terminal B
59	SW7A	SW7A	Analog Switch 7 terminal A
60	NC	NC	No Connection
61	SW6B	SW6B	Analog Switch 6 Terminal B
62	SW6A	SW6A	Analog Switch 6 Terminal A
63	NC	NC	No Connection
64	SW5B	SW5B	Analog Switch 5 Terminal B
VSUB (Thermal Pad)			The central thermal pad on the bottom of package must be connected to VNN externally

3.0 TEST CIRCUIT EXAMPLES

This section details a few example of test circuits.

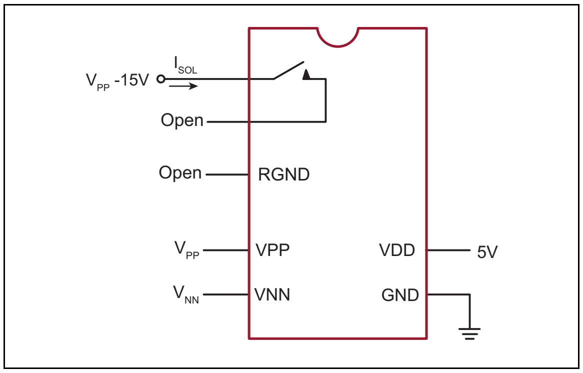


FIGURE 3-1: *Switch Off Leakage per Switch.*

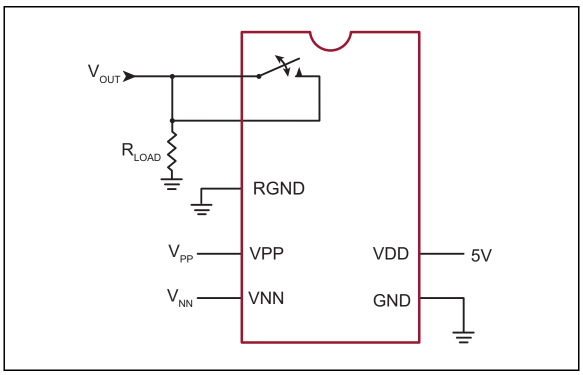


FIGURE 3-2: *DC Offset Switch On/Off.*

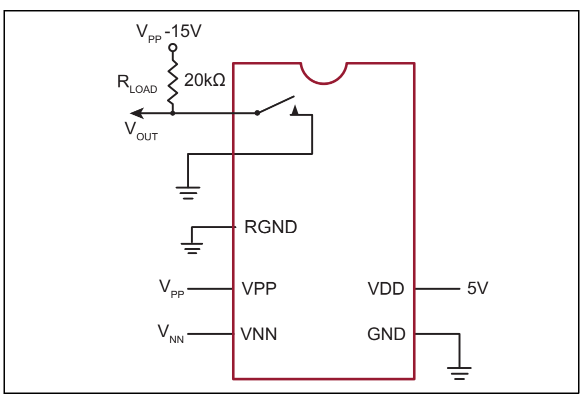


FIGURE 3-3: *T_{ON}/T_{OFF} Test Circuit.*

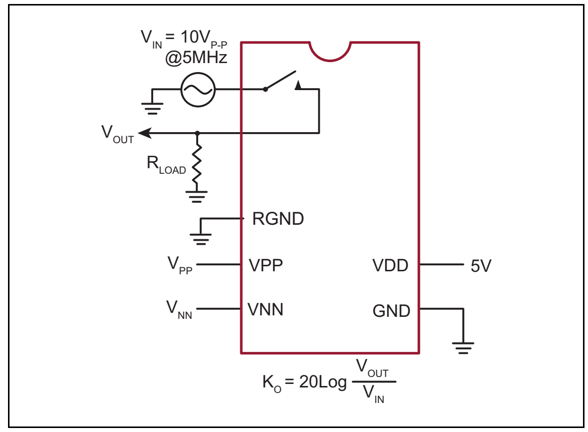


FIGURE 3-4: *Off Isolation.*

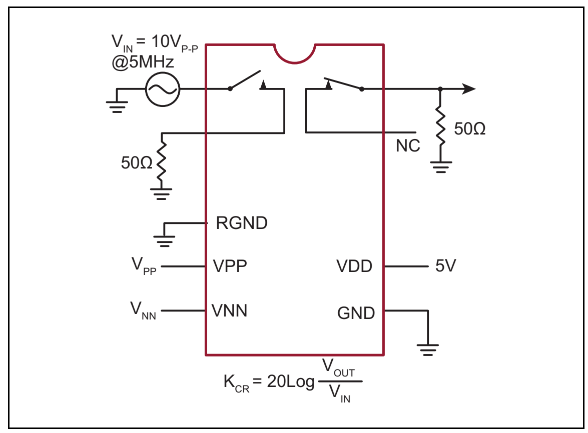


FIGURE 3-5: *Switch Crosstalk.*

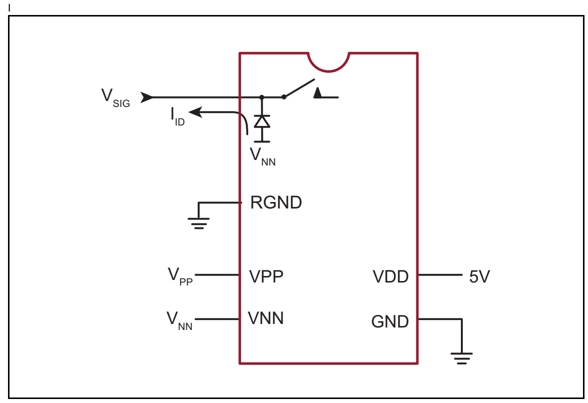


FIGURE 3-6: *Isolation Diode Current.*

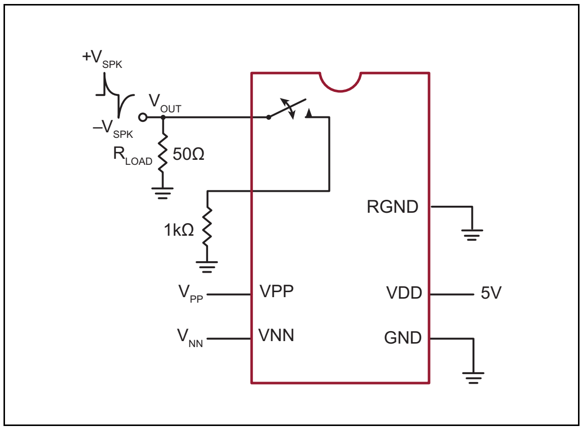


FIGURE 3-7: *Output Voltage Spike.*

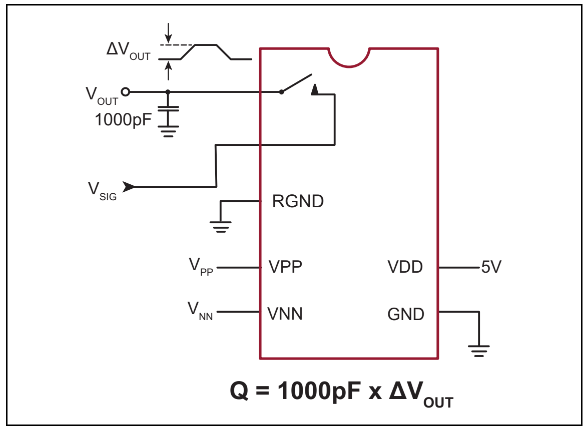


FIGURE 3-8: *Charge Injection.*

4.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{PP} = +150V, V_{NN} = -150V, V_{DD} = 5.0V, T_A = 25°C.

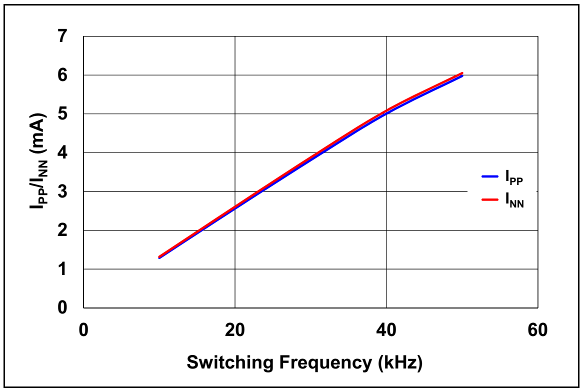


FIGURE 4-1: *I_{PP}/I_{NN} vs. Switching Frequency.*

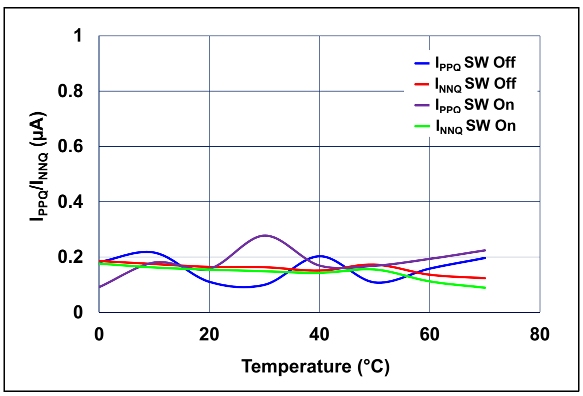


FIGURE 4-2: *I_{PPQ}/I_{NNQ} vs. Temperature.*

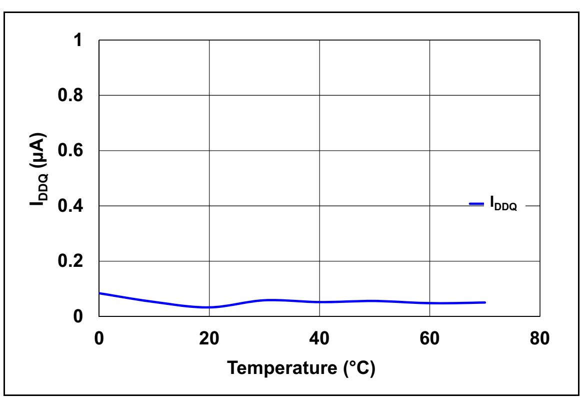


FIGURE 4-3: *I_{DDQ} vs. Temperature.*

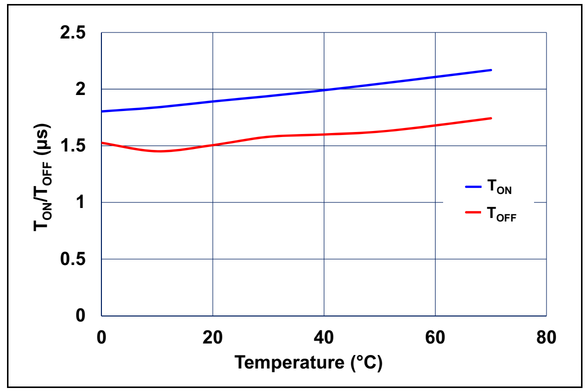


FIGURE 4-4: *T_{ON}/T_{OFF} vs. Temperature.*

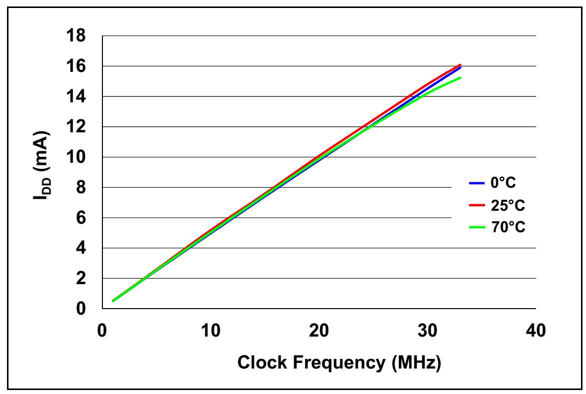


FIGURE 4-5: *I_{DD} vs. CLK Frequency.*

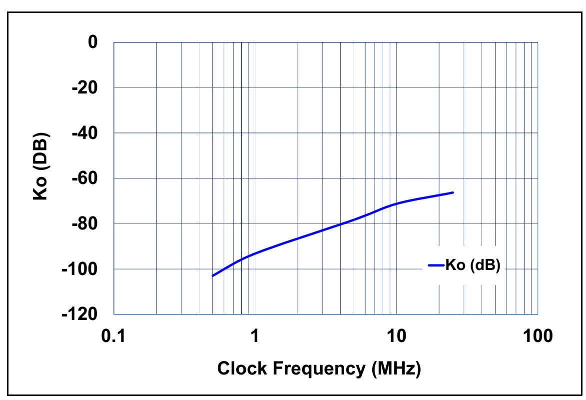


FIGURE 4-6: *K_O vs. Frequency with 50Ω Load.*

5.0 DETAILED DESCRIPTION AND APPLICATION INFORMATION

5.1 Device Overview

The HV2621/HV2721/HV2722 are 300V, low-charge injection, 16-channel, high-voltage analog switches. The high-voltage analog switches are used for multiplexing a piezoelectric transducer array in a probe to multiple channel transmitters (Tx) arrays in a medical ultrasound system.

The HV2621/HV2721/HV2722 are distinguished by bleed resistors that eliminate voltage build-up in capacitance load such as piezoelectric transducers. These devices can pass ±135V high-voltage large signal with V_{PP}/V_{NN} = ±150V. These devices have typical 18Ω on-resistance and 50 MHz bandwidth for small-signals.

Figure 5-1 shows a typical medical ultrasound image system consisting 64-channels of transmit pulsers, 64-channels of receivers (LNA and ADC) and 64-channels of T/R switches connecting to 192 elements of an ultrasound probe via a HV2XXX high-voltage analog switch array.

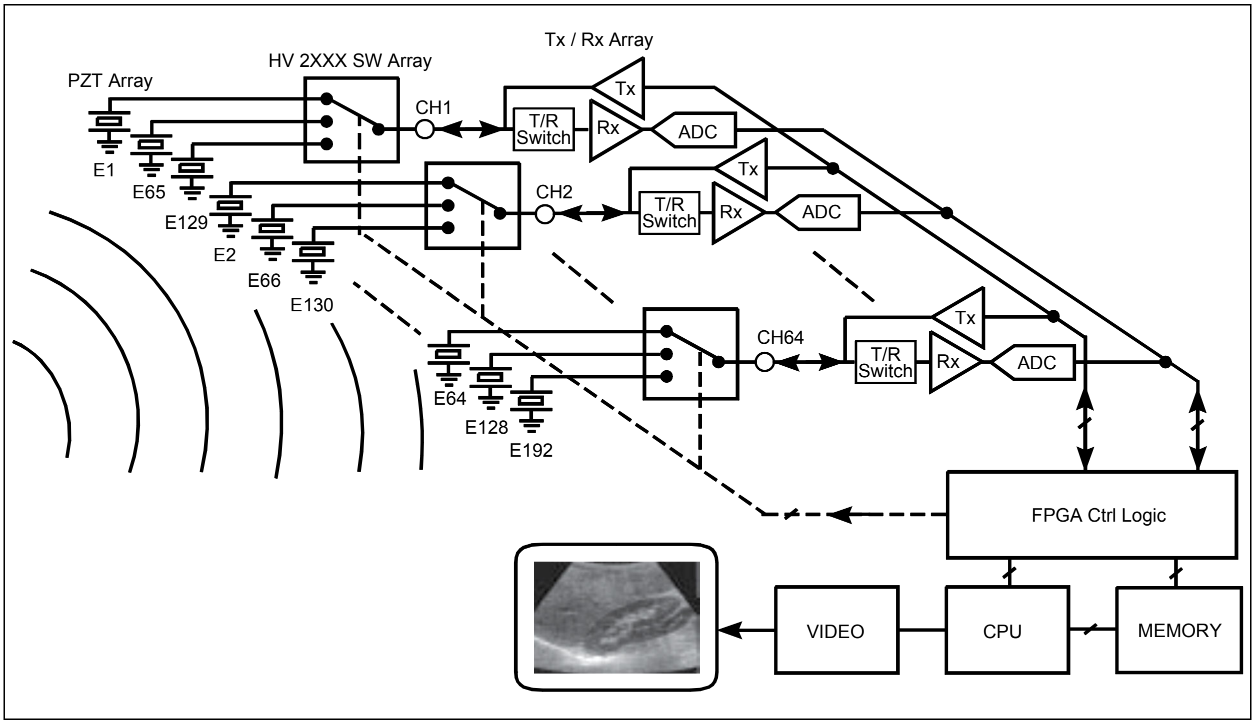


FIGURE 5-1: *Typical Medical Ultrasound Imaging System.*

5.2 Logic Input Timing

The HV2621/HV2721/HV2722 have digital serial interface consisting of Data In (D_{IN}), Clock (CLK), Data Out (D_{OUT}), Latch Enable ($\overline{LE}$), and Clear (CLR) to control 16 switches individually. The digital circuits are supplied by V_{DD}. The serial clock frequency is up to 33 MHz.

The switch state configuration data is shifted into the shift registers at the rising edge (low-to-high transition) of the clock. The switch configuration bit of SW15 is shifted in first and the configuration bit of SW0 is shifted in last. To change all the switch states at the same time, the Latch Enable Input ($\overline{LE}$) should remain high while the 16-bit Data In signal is shifted into the 16-bit register. After the valid 16-bit data completes shifting into the shift registers, the high-to-low transition of the $\overline{LE}$ signal transfers the contents of the shift registers into the latches. Finally, setting the $\overline{LE}$ high again, allows all the latches to keep the current state while new data can now be shifted into the shift registers without disturbing the latches.

It is recommended to change all the latch states at the same time through this method to avoid possible clock feed through noise (see Figure 5-2 for details).

When the CLR input is set high, it resets the data of all 16 latches to low. Consequently, all the high-voltage switches are set to OFF state. However, the CLR signal does not affect the contents of the shift register, so the shift register can operate regardless of the CLR signal. Therefore, when the CLR input is low, the shift register still retains the previous data.

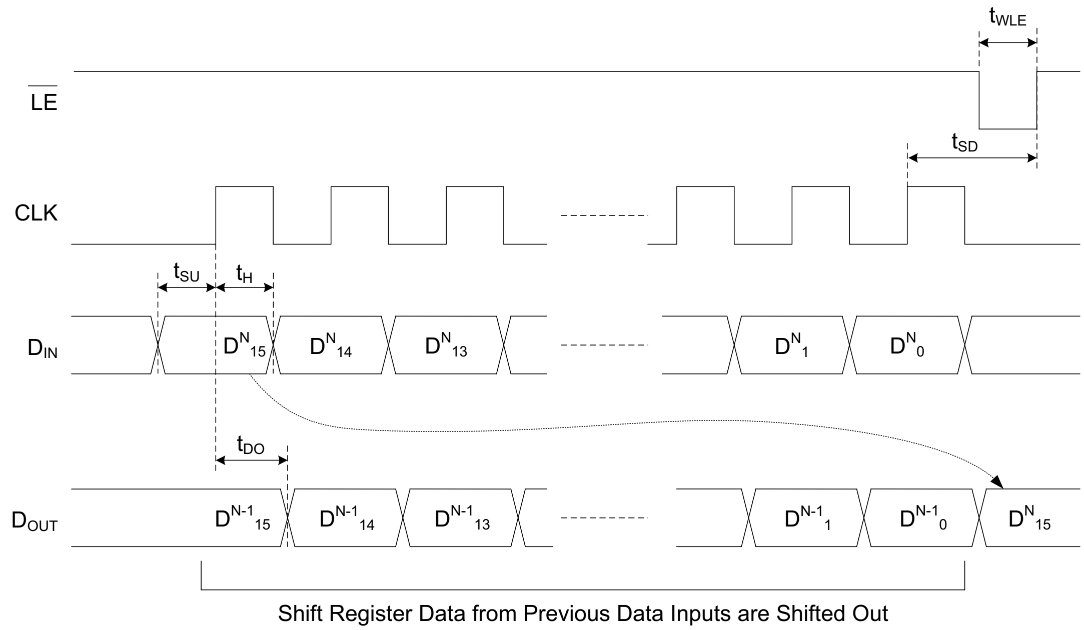


FIGURE 5-2: *Latch Enable Timing Diagram.*

5.3 Multiple Devices Connection

The digital serial interface of the HV2621/HV2721/HV2722 allows multiple devices to make a daisy-chain together. In this configuration, D_{OUT} of a device is connected to the D_{IN} of the subsequent device, and so forth. The last D_{OUT} of the daisy-chained HV2621/HV2721/HV2722 can be either floating or fed back to an FPGA to check the previously stored data in the shift registers.

To control all the high-voltage analog switch states in daisy-chained N devices, N-times 16 clocks and N-times 16 bits of data are shifted into shift registers, while $\overline{LE}$ remains high and CLR remains low. After all the data finishes shifting in, one single negative pulse of $\overline{LE}$ transfers the data from all the shift registers to all the latches simultaneously. Consequently, all N-times 16 high-voltage analog switches change states simultaneously.

5.4 Power Up/Down Sequence and Decoupling Capacitor

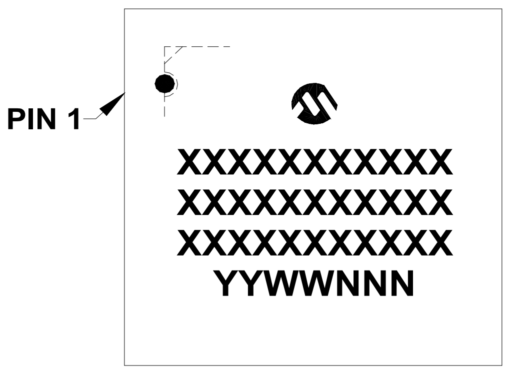
The recommended power up sequence is V_{DD}, V_{PP} and V_{NN}. The power down sequence is in reverse order. We also recommend the rise time and fall time of power supplies are greater than 1 msec. During the power up/down period, all the analog switch inputs should be within between V_{PP} and V_{NN} or floating.

It is recommended that 0.1 µF or larger ceramic decoupling capacitors, with the appropriate voltage ratings, be connected between GND and other supplies (V_{PP}, V_{NN} and V_{DD}). These decoupling capacitors should be placed as close as possible to the device.

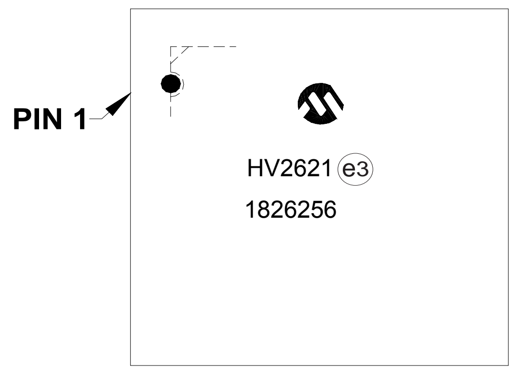
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

64-Pin QFN (9 x 9 mm)



Example

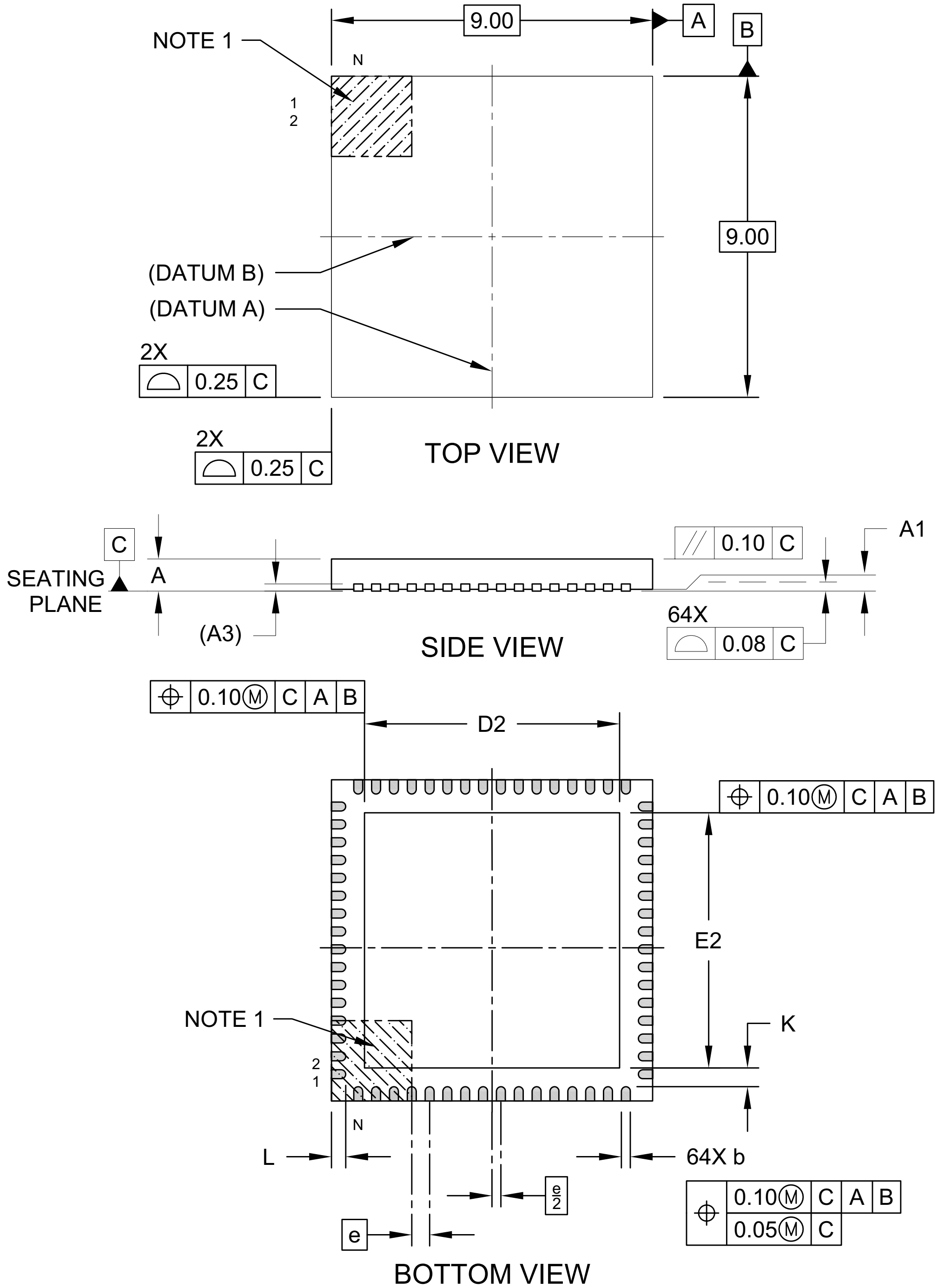


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

64-Lead Very Thin Plastic Quad Flat, No Lead Package (R4X) – 9x9x0.9 mm Body [VQFN]
With 7.15 x 7.15 Exposed Pad [Also called QFN]

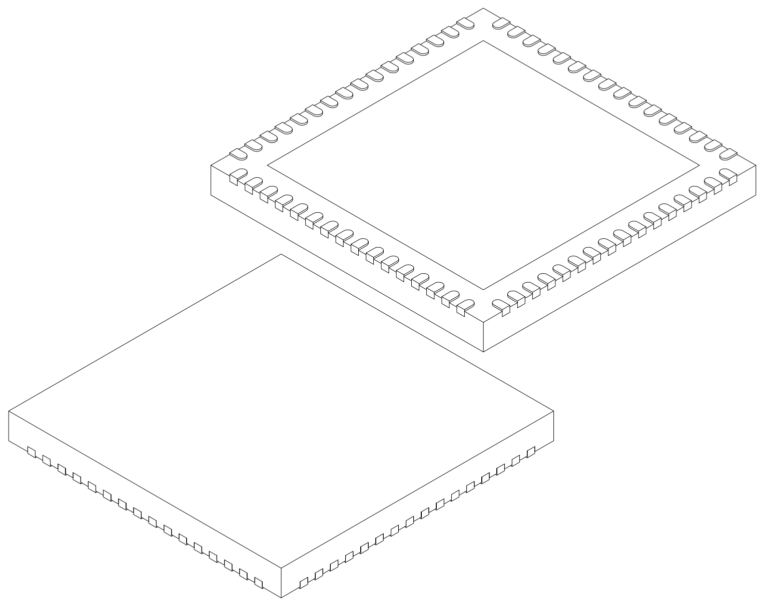
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-149D [R4X] Sheet 1 of 2

64-Lead Very Thin Plastic Quad Flat, No Lead Package (R4X) – 9x9x0.9 mm Body [VQFN]
With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.05	7.15	7.25
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.05	7.15	7.25
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

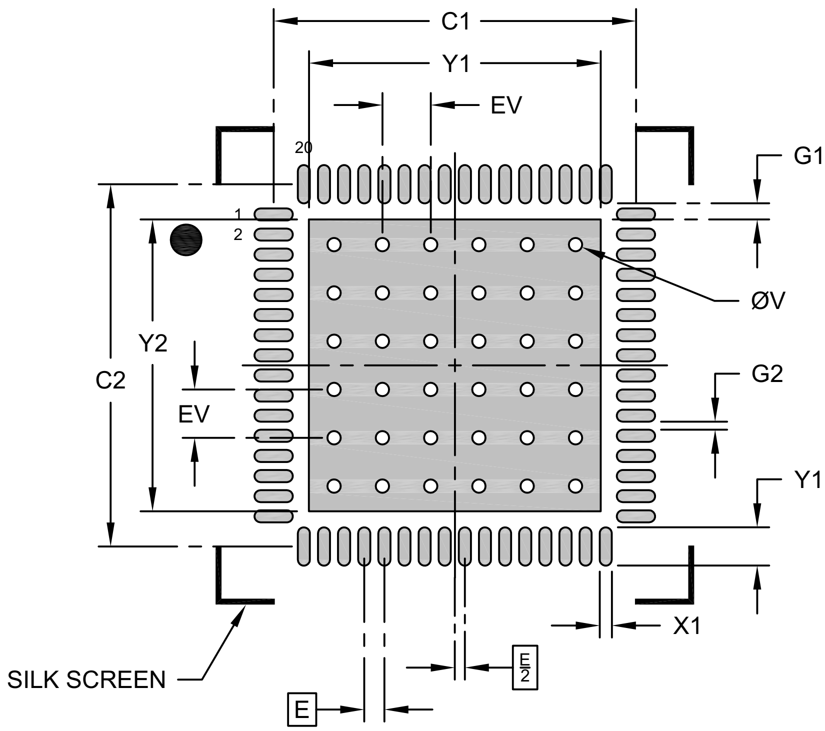
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149D [R4X] Sheet 2 of 2

64-Lead Very Thin Plastic Quad Flat, No Lead Package (R4X) – 9x9x0.9 mm Body [VQFN] With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			7.25
Optional Center Pad Length	Y2			7.25
Contact Pad Spacing	C1		9.00	
Contact Pad Spacing	C2		9.00	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.95
Contact Pad to Center Pad (X64)	G1	0.40		
Spacing Between Contact Pads (X60)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-149C [R4X]

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2019)

- Original release of this document

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	/XX
Device	Package

Device:	HV2621:	300V, Low-Charge Injection 16-Channel High-Voltage Analog Switch
	HV2721:	300V, Low-Charge Injection 16-Channel High-Voltage Analog Switch with Bleed Resistor at Both Sides of Switch
	HV2722:	300V, Low-Charge Injection 16-Channel High-Voltage Analog Switch with Bleed Resistor at One Side of Switch
Package:	R4X=	Very Thin Plastic Quad Flat Pack, No Lead Package – 9x9x0.9 mm Body, 64-Lead (QFN)

Examples:

a) HV2621/R4X: 16-Channel High-Voltage Analog Switch, 64-lead QFN

NOTES:

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