

Low Charge Injection 32-Channel High Voltage Analog Switch with Bleed Resistors

Features

- ▶ 32-channel high voltage analog switch
- ▶ Integrated bleed resistors on the outputs
- ▶ 2:1 Multiplexer / Demultiplexer
- ▶ 3.3V or 5.0V CMOS input logic level
- ▶ 20MHz data shift clock frequency
- ▶ HVCMOS technology for high performance
- ▶ Very low quiescent power dissipation -10 μ A
- ▶ Low parasitic capacitance
- ▶ DC to 50MHz analog signal frequency
- ▶ -60dB typical OFF-isolation at 5.0MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ Cascadable serial data register with latches
- ▶ Flexible operating supply voltages

Applications

- ▶ Medical ultrasound imaging
- ▶ NDT metal flaw detection
- ▶ Piezoelectric transducer drivers
- ▶ Inkjet printer heads
- ▶ Optical MEMS modules

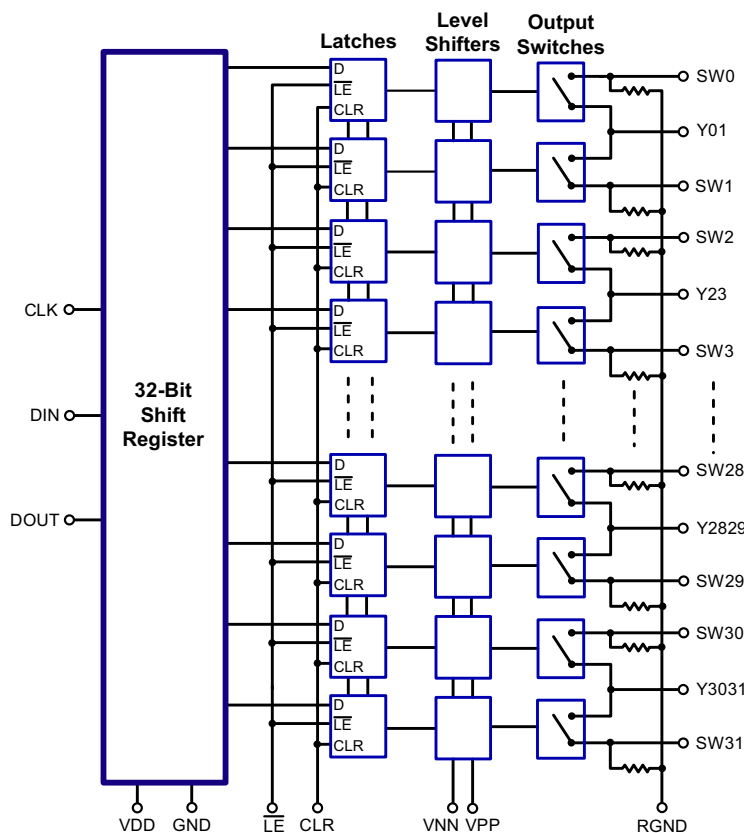
General Description

The Supertex HV2901 is a low charge injection 32-channel high voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging, piezoelectric transducer driver, and printers. The bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers.

Input data are shifted into a 32-bit shift registers that can then be retained in a 32-bit latch. To reduce any possible clock feed through noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +40V/-160V, +100V/-100V, and +160V/-40V.

Block Diagram



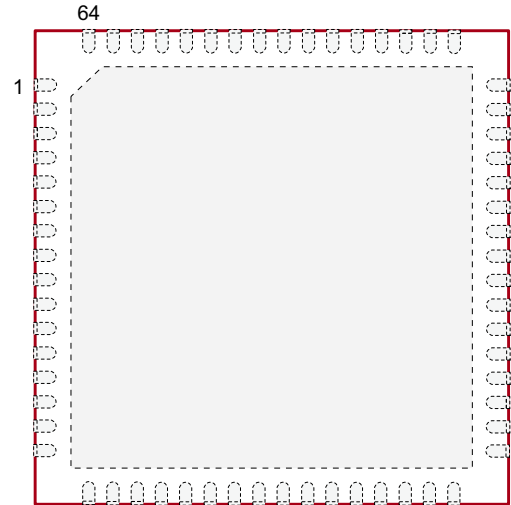
Ordering Information

Part Number	Package Option	Packing
HV2901K6-G	64-Lead QFN (9x9)	260/Tray

-G indicates package is RoHS compliant ('Green')



Pin Configuration



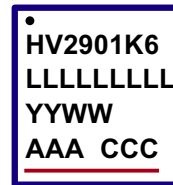
64-Lead QFN (K6)
(top view)

Absolute Maximum Ratings

Parameter	Value
V _{DD} logic supply	-0.5V to +6.5V
V _{PP} -V _{NN} differential supply	220V
V _{PP} positive supply	-0.5V to V _{NN} +200V
V _{NN} negative supply	+0.5V to -200V
Logic input voltage	-0.5V to V _{DD} +0.3V
Analog signal range	V _{NN} to V _{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C
Power dissipation	1.5W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking



L = Lot Number
 YY = Year Sealed
 WW = Week Sealed
 A = Assembler ID
 C = Country of Origin
 — = "Green" Packaging

Package may or may not include the following marks: Si or

64-Lead QFN (K6)

Typical Thermal Resistance

Package	θ_{ja}
64-Lead QFN	21°C/W

Recommended Operating Conditions

Sym	Parameter	Value
V _{DD}	Logic power supply voltage	3.0V to 5.5V
V _{PP}	Positive high voltage supply	+40V to V _{NN} +200V
V _{NN}	Negative high voltage supply	-40V to -160V
V _{IH}	High level input voltage	0.9V _{DD} to V _{DD}
V _{IL}	Low level input voltage	0V to 0.1V _{DD}
V _{SIG}	Analog signal voltage peak-to-peak	V _{NN} +10V to V _{PP} -10V
T _A	Operating free air temperature	0°C to 70°C

Notes:

- Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
- V_{SIG} must be V_{NN} ≤ V_{SIG} ≤ V_{PP} or floating during power up/down transition.
- Rise and fall times of power supplies V_{DD}, V_{PP} and V_{NN} should not be less than 1.0msec.

DC Electrical Characteristics (Over recommended operating conditions unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R _{ONS}	Small signal switch ON-resistance	-	30	-	26	38	-	48	Ω	I _{SIG} = 5.0mA	V _{PP} = +40V, V _{NN} = -160V
		-	25	-	22	27	-	32		I _{SIG} = 200mA	V _{NN} = -160V
		-	25	-	22	27	-	30		I _{SIG} = 5.0mA	V _{PP} = +100V, V _{NN} = -100V
		-	18	-	18	24	-	27		I _{SIG} = 200mA	V _{NN} = -100V
		-	23	-	20	25	-	30		I _{SIG} = 5.0mA	V _{PP} = +160V, V _{NN} = -40V
		-	22	-	16	25	-	27		I _{SIG} = 200mA	V _{NN} = -40V
ΔR _{ONS}	Small signal switch ON-resistance matching	-	20	-	5.0	20	-	20	%	I _{SIG} = 5.0mA, V _{PP} = +100V, V _{NN} = -100V	
R _{ONL}	Large signal switch ON-resistance	-	-	-	15	-	-	-	Ω	V _{SIG} = V _{PP} -10V, I _{SIG} = 1A	
R _{INT}	Value of output bleed resistor	-	-	20	35	50	-	-	KΩ	Output switch to R _{GND} I _{RINT} = 0.5mA	
I _{SOL}	Switch OFF-leakage per switch	-	5.0	-	1.0	10	-	15	μA	V _{SIG} = V _{PP} -10V, V _{NN} +10V	
V _{OS}	DC offset switch OFF	-	300	-	100	300	-	300	mV	No load	
	DC offset switch ON	-	500	-	100	500	-	500			
I _{PPQ}	Quiescent V _{PP} supply current	-	-	-	10	50	-	-	μA	All switches OFF	
I _{NNQ}	Quiescent V _{NN} supply current	-	-	-	-10	-50	-	-			
I _{PPQ}	Quiescent V _{PP} supply current	-	-	-	10	50	-	-	μA	All switches ON, I _{SW} = 5.0mA	
I _{NNQ}	Quiescent V _{NN} supply current	-	-	-	-10	-50	-	-			
I _{SW}	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V _{SIG} duty cycle < 0.1%	
f _{SW}	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I _{PP}	Average V _{PP} supply current	-	16	-	-	20	-	22	mA	V _{PP} = +40V, V _{NN} = -160V	All output switches are turning ON and OFF at 50kHz with no load
		-	14	-	-	14	-	14		V _{PP} = +100V, V _{NN} = -100V	
		-	14	-	-	14	-	14		V _{PP} = +160V, V _{NN} = -40V	
I _{NN}	Average V _{NN} supply current	-	16	-	-	20	-	22	mA	V _{PP} = +40V, V _{NN} = -160V	All output switches are turning ON and OFF at 50kHz with no load
		-	14	-	-	14	-	14		V _{PP} = +100V, V _{NN} = -100V	
		-	14	-	-	14	-	14		V _{PP} = +160V, V _{NN} = -40V	
I _{DD}	Average V _{DD} supply current	-	8.0	-	-	8.0	-	8.0	mA	f _{CLK} = 5.0MHz, V _{DD} = 5.0V	
I _{DDQ}	Quiescent V _{DD} supply current	-	10	-	-	10	-	10	μA	All logic inputs are static	
I _{SOR}	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V _{OUT} = V _{DD} -0.7V	
I _{SINK}	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V _{OUT} = 0.7V	
C _{IN}	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

* See Test Circuits on page 5

AC Electrical Characteristics (Over recommended operating conditions unless otherwise specified)

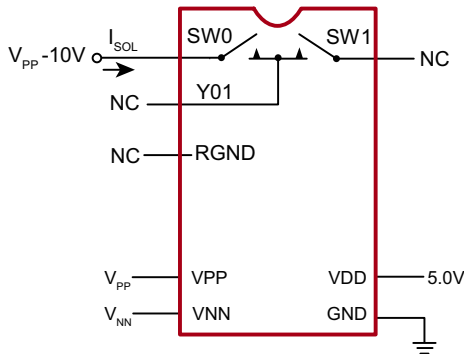
Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{SD}	Set up time before \overline{LE} rises	25	-	25	-	-	25	-	ns	---
t_{WLE}	Time width of \overline{LE}	56	-	-	56	-	56	-	ns	$V_{DD} = 3.0V$
		12	-	-	12	-	12	-		$V_{DD} = 5.0V$
t_{DO}	Clock delay time to data out	8.0	40	8.0	19	40	8.0	40	ns	$V_{DD} = 3.0V$
		8.0	30	8.0	15	30	8.0	30		$V_{DD} = 5.0V$
t_{WCLR}	Time width of CLR	55	-	55	-	-	55	-	ns	---
t_{SU}	Set up time data to clock	21	-	21	-	-	21	-	ns	$V_{DD} = 3.0V$
		7.0	-	7.0	-	-	7.0	-		$V_{DD} = 5.0V$
t_H	Hold time data from clock	5.0	-	5.0	-	-	5.0	-	ns	$V_{DD} = 3.0V$
		7.0	-	7.0	-	-	7.0	-		$V_{DD} = 5.0V$
f_{CLK}	Clock frequency	-	8	-	-	8	-	8	MHz	$V_{DD} = 3.0V$
		-	20	-	-	20	-	20		$V_{DD} = 5.0V$
t_R, t_F	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
t_{ON}	Turn ON time	-	5.0	-	-	5.0	-	5.0	μs	$V_{SIG} = V_{PP} - 10V,$ $R_{LOAD} = 10k\Omega$
t_{OFF}	Turn OFF time	-	5.0	-	-	5.0	-	5.0		
dv/dt	Maximum V_{SIG} slew rate	-	20	-	-	20	-	20	V/ns	$V_{PP} = +40V, V_{NN} = -160V$
		-	20	-	-	20	-	20		$V_{PP} = +100V, V_{NN} = -100V$
		-	20	-	-	20	-	20		$V_{PP} = +160V, V_{NN} = -40V$
K_O	OFF isolation	-30	-	-30	-33	-	-30	-	dB	$f = 5.0MHz,$ $1.0k\Omega/15pF$ load
		-58	-	-58	-60	-	-58	-		$f = 5.0MHz, 50\Omega$ load
K_{CR}	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	$f = 5.0MHz, 50\Omega$ load
I_{ID}	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	OFF capacitance SW to GND	-	14	-	9.0	14	-	14	pF	$V_{SIG} = 0, f = 1.0MHz,$ both SW OFF
	OFF capacitance Y to GND	-	28	-	18	28	-	28		
$C_{SG(ON)}$	ON capacitance SW to GND	-	33	-	23	33	-	33	pF	$V_{SIG} = 0, f = 1.0MHz,$ one SW ON, one SW OFF
	ON capacitance Y to GND	-	33	-	23	33	-	33		
$+V_{SPK}$	Output voltage spike SW	-	-	-	-	+150	-	-	mV	$V_{PP} = +40V, V_{NN} = -160V$ $R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	-150	-	-		
$+V_{SPK}$		-	-	-	-	+150	-	-		$V_{PP} = +100V, V_{NN} = -100V$ $R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	-150	-	-		
$+V_{SPK}$		-	-	-	-	+150	-	-		$V_{PP} = +160V, V_{NN} = -40V$ $R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	-150	-	-		

* See Test Circuits on page 5

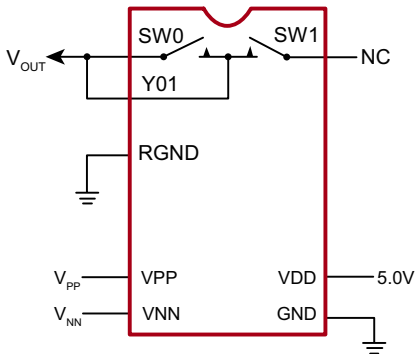
AC Electrical Characteristics (cont.)

Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
+V _{SPK}	Output voltage spike Y	-	-	-	-	+150	-	-	mV	V _{PP} = +40V, V _{NN} = -160V R _{LOAD} = 50Ω
-V _{SPK}		-	-	-	-	-150	-	-		
+V _{SPK}		-	-	-	-	+150	-	-		
-V _{SPK}		-	-	-	-	-150	-	-	mV	V _{PP} = +100V, V _{NN} = -100V R _{LOAD} = 50Ω
+V _{SPK}		-	-	-	-	+150	-	-		
-V _{SPK}		-	-	-	-	-150	-	-		
QC	Charge injection (per switch)	-	-	-	820	-	-	-	pC	V _{PP} = +40V, V _{NN} = -160V V _{PP} = +100V, V _{NN} = -100V V _{PP} = +160V, V _{NN} = -40V
		-	-	-	600	-	-	-		
		-	-	-	350	-	-	-		

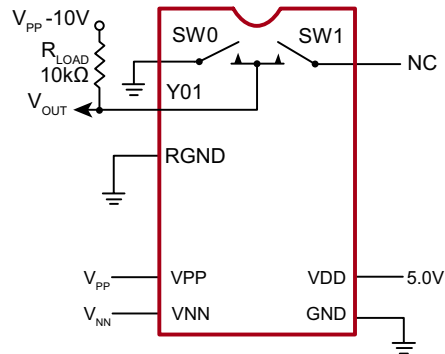
Test Circuits



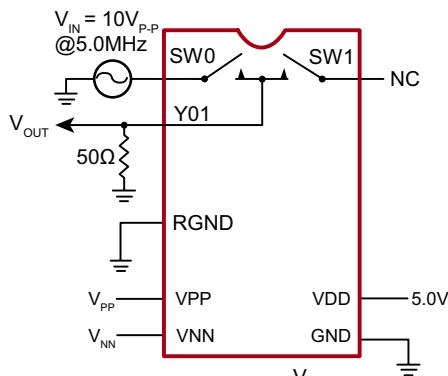
Switch OFF Leakage



DC Offset ON/OFF

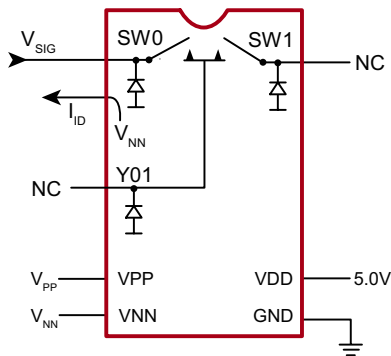


T_{ON}/T_{OFF} Test Circuit

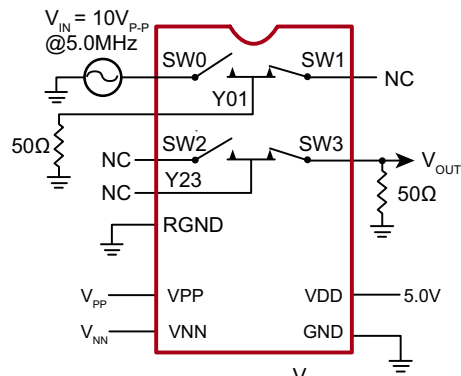


$$K_o = 20 \log \frac{V_{OUT}}{V_{IN}}$$

OFF Isolation

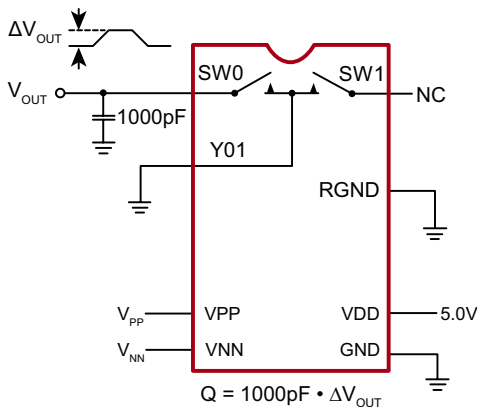


Isolation Diode Current



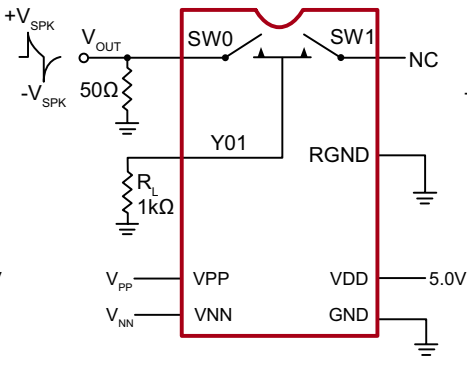
$$K_{CR} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Crosstalk

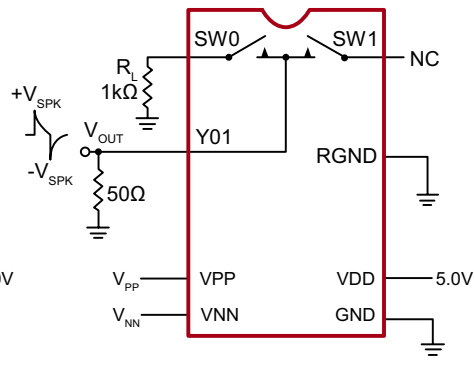


$$Q = 1000pF \cdot \Delta V_{OUT}$$

Charge Injection



Output Voltage Spike SW



Output Voltage Spike Y

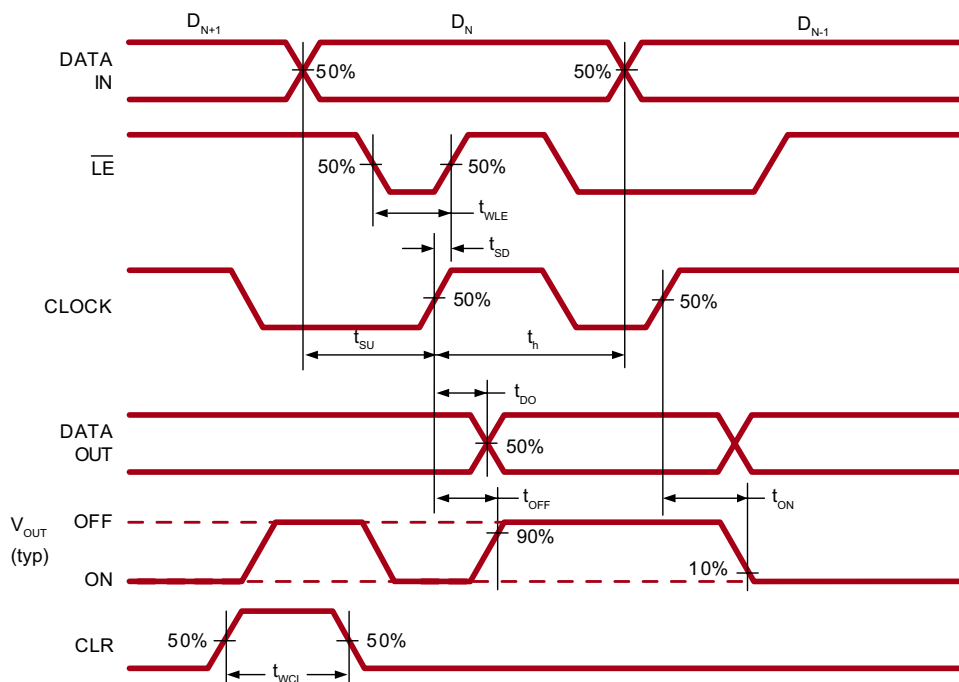
Truth Table

D0	D1	...	D15	D16	...	D31	\overline{LE}	CLR	SW0	SW1	...	SW15	SW16	...	SW31
L	-		-	-		-	L	L	OFF	-		-	-		-
H	-		-	-		-	L	L	ON	-		-	-		-
-	L		-	-		-	L	L	-	OFF		-	-		-
-	H		-	-		-	L	L	-	ON		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		L	-		-	L	L	-	-		OFF	-		-
-	-		H	-		-	L	L	-	-		ON	-		-
-	-	...	-	L	...	-	L	L	-	-	...	-	OFF	...	-
-	-		-	H		-	L	L	-	-		-	ON		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		L	L	L	-	-		-	-		OFF
-	-		-	-		H	L	L	-	-		-	-		ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Notes:

1. The 32 switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. All 32 switches go to a state retaining their latched condition at the rising edge of \overline{LE} . When \overline{LE} is low the shift registers data flow through the latch.
4. D_{OUT} is high when data in the register 31 is high.
5. Shift registers clocking has no effect on the switch states if \overline{LE} is high.
6. The CLR clear input overrides all other inputs.

Logic Timing Waveforms



Pin Function

Pin	Function
1	SW30
2	Y3031
3	SW31
4	NC
5	CLR
6	NC
7	\overline{LE}
8	CLK
9	VDD
10	DIN
11	GND
12	DOUT
13	NC
14	SW0
15	Y01
16	SW1

Pin	Function
17	SW2
18	Y23
19	SW3
20	SW4
21	Y45
22	SW5
23	SW6
24	Y67
25	SW7
26	SW8
27	Y89
28	SW9
29	SW10
30	Y1011
31	SW11
32	SW12

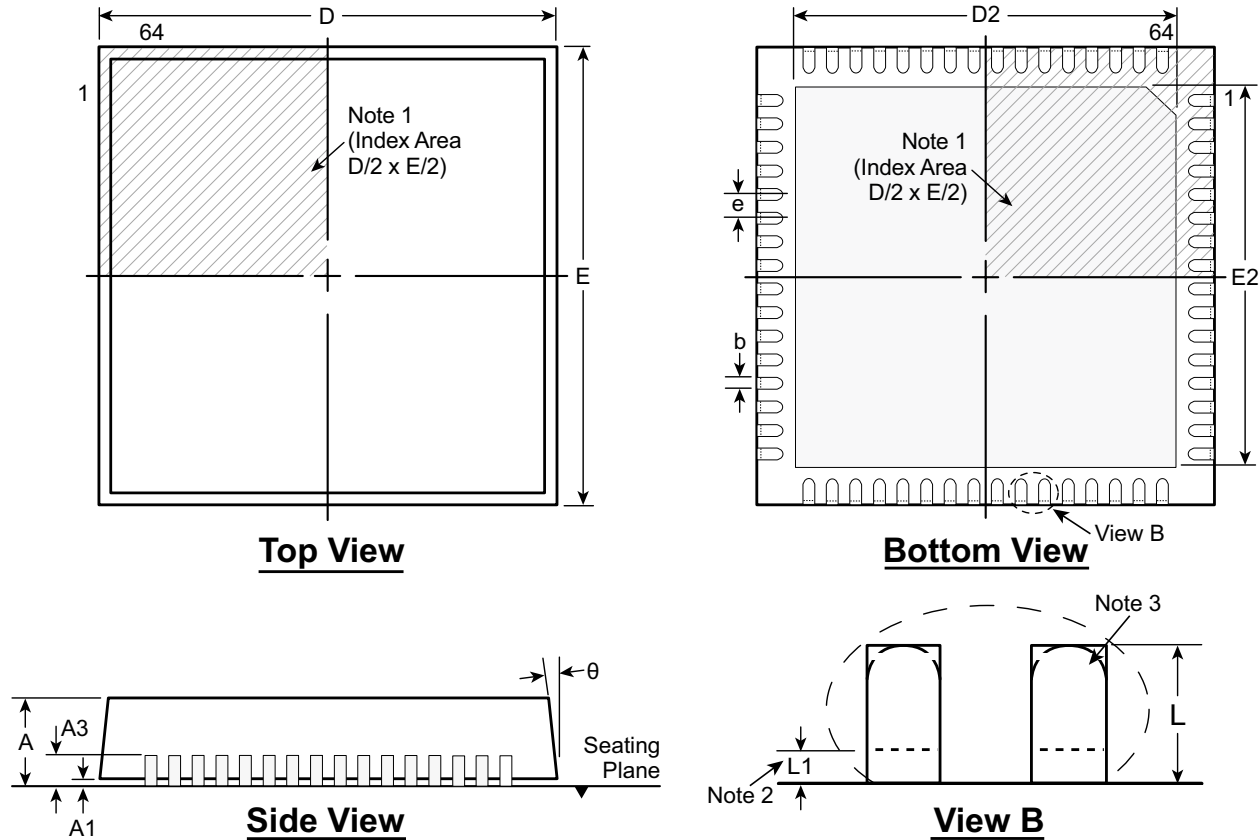
Pin	Function
33	Y1213
34	SW13
35	VPP
36	RGND
37	VNN
38	SW14
39	Y1415
40	SW15
41	SW16
42	Y1617
43	SW17
44	VNN
45	RGND
46	VPP
47	SW18
48	Y1819

Pin	Function
49	SW19
50	SW20
51	Y2021
52	SW21
53	SW22
54	Y2223
55	SW23
56	SW24
57	Y2425
58	SW25
59	SW26
60	Y2627
61	SW27
62	SW28
63	Y2829
64	SW29

VSUB (Thermal Pad)	The central thermal pad on the bottom of package must be connected to VNN externally
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64-Lead QFN Package Outline (K6)

9.00x9.00mm body, 1.00mm height (max), 0.50mm pitch



Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.20	8.90	7.60	8.90	7.60	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	9.00	7.70	9.00	7.70		0.40	-	-
	MAX	1.00	0.05		0.30	9.10	7.80	9.10	7.80		0.50	0.15	14°

Drawings are not to scale.

Supertex Doc.#: DSPD-64QFNK69X9P050, Version B020112

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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