HV53001

16-Channel, ±135V Push-Pull Driver with RTZ, Current Sensor and Built-in Boost Converter

Features

- 16-Channel Push-Pull Output
- Return-To-Zero (RTZ) and High-Impedance (Hi-Z) Function
- Up to ±135V Output Voltage
- 24 mA Minimum Source Sink Output Current
- 250 pF Maximum Output Load
- Current Sensor Output
- SPI Interface with Quad-Latched 2-bit per Channel Architecture
- Power-on Reset Function
- DC/DC Boost Converter with Power MOSFET
- 2.7 to 5.5V Converter Input Voltage
- Short Circuit Protection
- Overtemperature Monitor
- Power ON/OFF Sequence Control
- Shutdown Function
- 105-ball 9 x 9 mm TFBGA Package

Application

- Surface Haptic Application
- MEMS Driver
- Piezo Driver

General Description

The HV53001 device is an integrated driver solution for various applications, which consists of three main functional blocks (1) high-voltage driver, (2) SPI interface and (3) DC/DC boost controller with power MOSFET.

The high-voltage driver block includes 16 push-pull drivers capable of ±135V output swing with Return-To-Zero (RTZ) function. Each output driver is capable of sourcing and sinking at least 24 mA. Each high-voltage output is capable of driving up to 250 pF capacitive load. A global current sensor function is also integrated into this device to monitor the charge and discharge currents. The measured current is mapped to a low-voltage analog output with a scale factor of 3.1 V/V via a current sensing resistor.

The SPI interface is used to communicate between the host processor and the high-voltage drivers. This interface accepts a 3.3V logic I/O signal up to clock speed of 32 MHz. Five digital LATCH control signals manage the data flow and the firing pattern. It establishes the output to one of four possible states: V_{PP}, V_{NN}, 0V or high impedance.

This IC also includes an integrated DC/DC controller with power MOSFET. The controller is used in a flyback configuration to generate four high-voltage rails, ±135V and ±123V, for the high-voltage driver block. The ±123V rails are created from two 12V floating supplies referenced to the ±135V supply rails.

The converter accepts input voltage from a single 2.7V-5.5V input voltage rail. A built-in positive charge pump and a simple external negative charge pump convert the input supply to +6.5V and -6.0V supplies to power the high-voltage driver block.

A proper power on and off sequence is critical to ensure the operation of the high-voltage driver. A power sequence control circuit is included for the user to control the power supplies to power up or down the high-voltage driver. It is used in conjunction with the external high-voltage FET transistors.

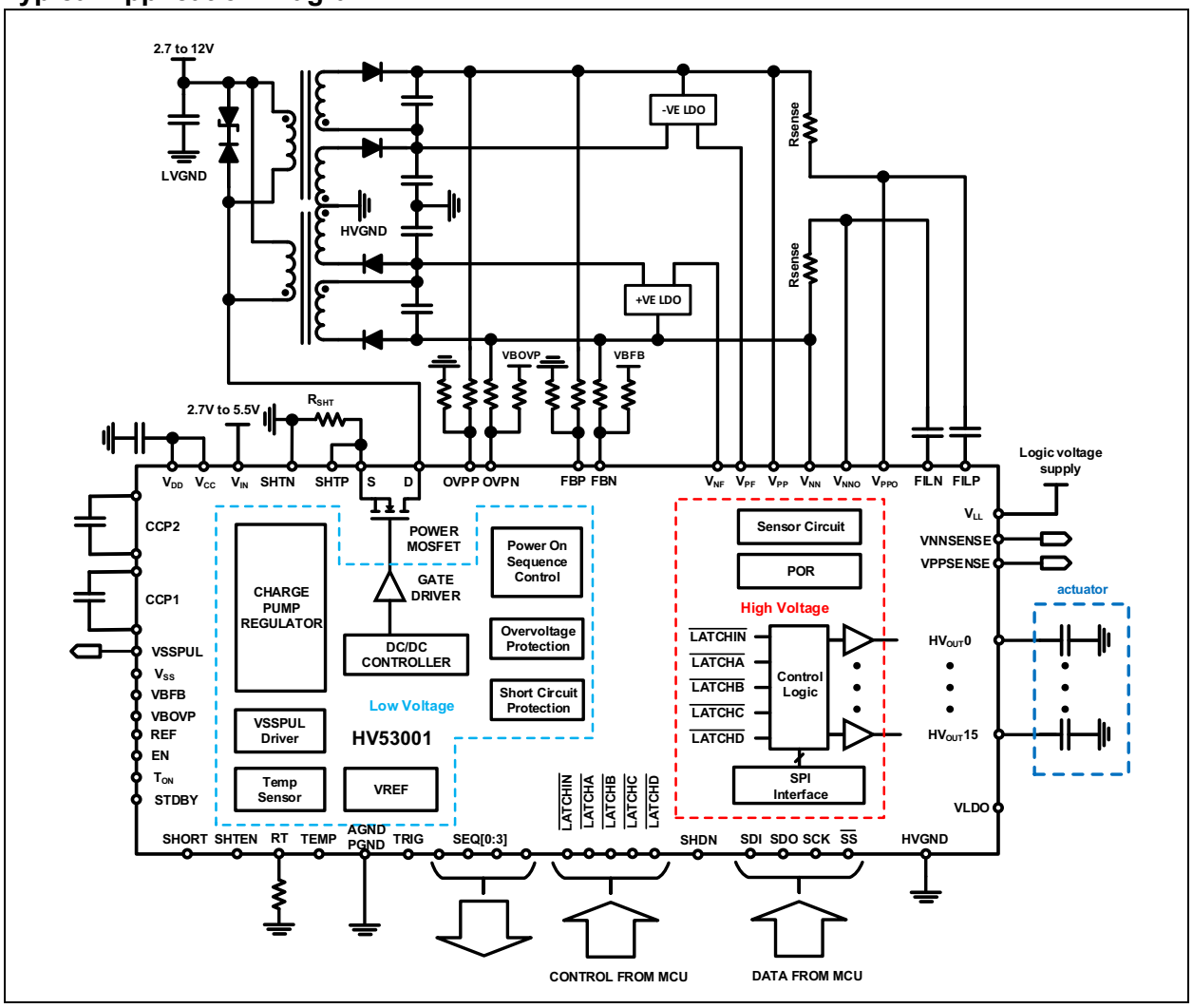
Safety features are added to the DC/DC converter. The overvoltage protection monitors both high-voltage rails to protect the driver against an overvoltage condition. Short circuit protection detects any short circuit event at the high-voltage rails by monitoring the current flow

through the power FET transistor. When a short circuit is detected, the DC/DC controller will shut down the converter and send a fault signal at the SHORT pin.

An overtemperature monitor function is also added in the converter IC. It sends a fault signal at the TEMP pin when it detects a temperature over the threshold temperature.

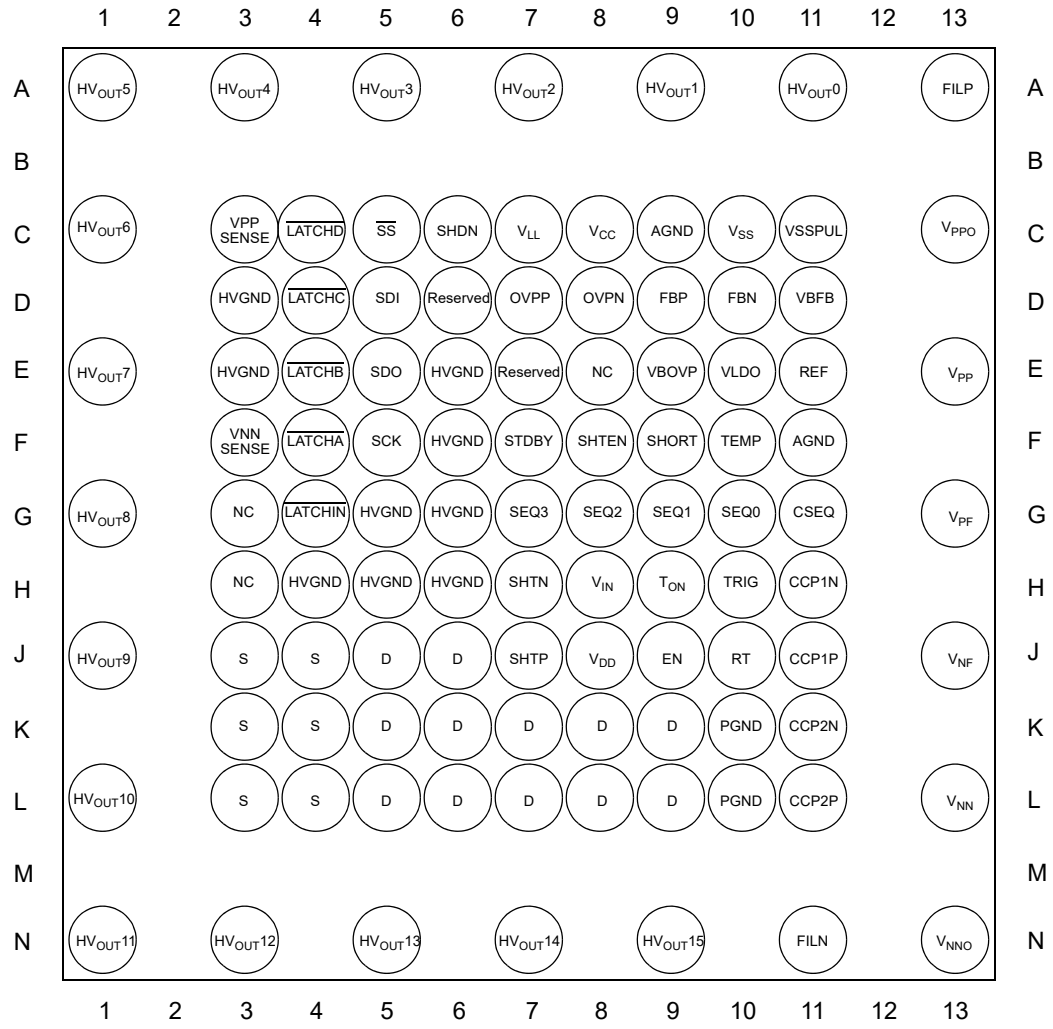
The HV53001 device is packaged in a 9x9mm 105 ball TFBGA package. All high-voltage I/Os are arranged to have sufficient clearance for safety.

Typical Application Diagram



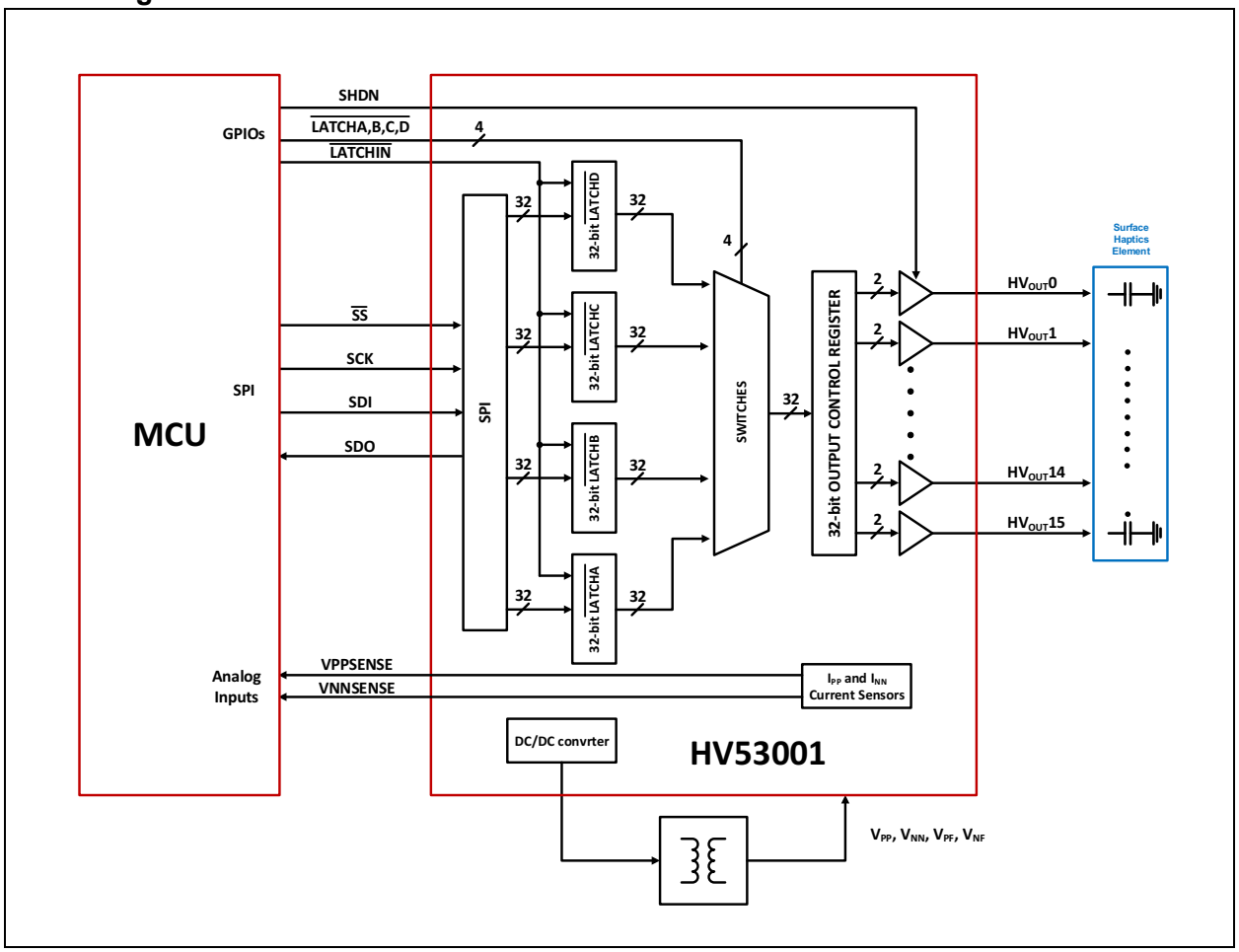
Package Types (Top View)

HV53001
9 x 9 TFBGA*



* see Table 2-1.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Converter Input Supply Voltage (V_{IN}) ..... -0.3V to +6.0V
Enable Pin Input Voltage (EN) ..... -0.3V to V_{IN}
Power FET Drain-Source Voltage (V_{DS}) ..... -0.3V to +80V
Low Positive Voltage Supply (V_{DD}) ..... -0.3V to +8.0V
High Positive Supply Voltage (V_{PP}) ..... -0.3V to +140V
High Negative Supply Voltage (V_{NN}) ..... -140V to +0.3V
High Positive Floating Supply Voltage (V_{PF}) ..... V_{PP} - 14V to V_{PP}
High Negative Floating Supply Voltage (V_{NF}) ..... V_{NN} to V_{NN} + 14V
Analog Low Positive Voltage Supply (V_{CC}) ..... -0.3V to +8.0V
Analog Low Negative Voltage Supply (V_{SS}) ..... -8.0V to +0.3V
Logic Voltage Supply (V_{LL}) ..... -0.3V to +4.0V
Logic Input Levels (Hi-V Driver, SPI Interface, $\overline{\text{LATCHX}}$ and SHDN) ..... -0.3V to V_{LL} +0.3V
Logic Input Levels (DC/DC Converter Controls) ..... -0.3V to V_{LDO} +0.3V
Maximum Junction Temperature ($T_{J(MAX)}$) ..... +125°C
Storage Temperature ..... -65°C to +150°C
ESD Rating on Low-Voltage Pins (Human Body Model) ..... 2 kV
ESD Rating on Low-Voltage Pins (Charged Device Model) ..... 500 V
ESD Rating on High-Voltage Pins (Human Body Model) ..... 500 V
ESD Rating on High-Voltage Pins (Charged Device Model) ..... 500 V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: OPERATING SUPPLY VOLTAGES

Electrical Specifications: Unless otherwise specified: $T_A = T_J$ = +25°C. **Boldface** specifications apply over the $T_A = T_J$ = range of -40°C to +125°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Supply Voltage	V_{IN}	**2.7**	**-**	**5.5**	V	Note 1
High Positive Supply Voltage	V_{PP}	**48**		**135**	V	
High Negative Supply Voltage	V_{NN}	**-135**		**-48**	V	
Low Positive Supply Voltage (High-Voltage Driver)	V_{CC}	**6.0**	**6.5**	**7.0**	V	
Low Negative Supply Voltage (High-Voltage Driver)	V_{SS}	**-6.5**	**-6.0**	**-5.5**	V	
Logic Input Supply Voltage (SPI Interface)	V_{LL}	**3.0**	**3.3**	**3.6**	V	
Negative Floating Supply Voltage	V_{NF}	**V_{NN} + 9V**	**-**	**V_{NN}+13.2V**	V	
Positive Floating Supply Voltage	V_{PF}	**V_{PP}-13.2V**	**-**	**V_{PP} - 9V**	V	
High-Level Input Logic Voltage (DC/DC Controls)	V_{IH}	**2.0**			V	
High-Level Input Logic Voltage (High-Voltage Driver Controls)		**0.8V_{LL}**				
Low-Level Input Logic Voltage (DC/DC Controls)	V_{IL}	**0**		**0.8**	V	
Low-Level Input Logic Voltage (High-Voltage Driver Controls)		**0**		**0.2V_{LL}**		

Note 1: Specification is obtained by characterization and is not 100% tested.

TABLE 1-2: ELECTRICAL CHARACTERISTICS

Electrical Specifications: unless otherwise specified, all limits apply for $T_A = T_J = 25°C$; **Boldface** specifications apply over the full operating temperature range of $T_A = T_J = -40°C$ to 125°C. Typical values are at +25°C. RT = 200kΩ, EN = 3.3V, V_{PP}= +135V, V_{NN}= -135V, V_{PF}= +123V, V_{NF}= -123V, V_{CC}= +6.5V, V_{SS}= -6.0V, V_{LL}= +3.3V, V_{IN} = +3.3V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Low Current Standby Mode						
Low Threshold for EN Pin	V_{IL}	**0**		**0.8**	V	
High Threshold for EN Pin	V_{IH}	**2.0**		**V_{IN}**	V	
Pull Down Resistor at EN Pin			500		kΩ	EN = 3.3V
Quiescent Current Draw from V_{IN} Pin	$I_{IN}Q$			5	μA	EN = open
Charge Pump Converter						
Output Voltage	V_{DD}	**6.0**	**6.5**	**6.75**	V	2.7V ≤ V_{IN} ≤ 5.5V Io = 10mA
Output I_{DD} Load Current	I_{DD}	10			mA	
Output Ripple Voltage	V_{RIPPLE}			150	mV	V_{IN} = 3.3V, Io = 10mA, CV_{DD} = 10μF (Note 3)
V_{DD} Under Voltage Lockout (Rising Edge)	VDD_{UVLO}	**4.25**		**4.75**	V	(Note 2)
V_{DD} Hysteresis (Falling)			0.25		V	(Note 2)
Low Dropout Linear Regulator						
Internal LDO Output Voltage	V_{LDO}	**5.0**	**5.25**	**5.5**	V	
Clock Generation						
Minimum Switching Frequency	$f_{s,min}$	**160**	**200**	**240**	kHz	RT = 400kΩ
Maximum Switching Frequency	$f_{s,max}$	**320**	**400**	**480**	kHz	RT = 200kΩ
Clock Ramp Maximum	V_{TS}		**3.75**		V	(Note 2)
Clock Ramp Minimum	V_{RST}		**0.2**		V	(Note 2)
Output Voltage Reference						
Internally Set Reference	$VREF_{INT}$	**-3%**	**1.19**	**+3%**	V	(Note 2) V_{IN} = 3.7V
Internal Reference to Select External Reference	REF_S	**-5.5%**	**0.6**	**+5.5%**	V	
External Reference Range	REF	**0.6**		**2.4**	V	(Note 2)
Output Current Feedback						
OCP Threshold	VREF2	40		60	mV	(Note 2)
Ton Generation						
T_{ON} Voltage Range	VT_{ON}	0		3	V	
T_{ON} Ceiling Voltage	$LIMIT_{CL}$	$0.8V_{TS}$		3	V	
T_{ON} Floor Range	$LIMIT_{FL}$		$0.25V_{TS}$	3	V	
Minimum T_{ON} Time	T_{ON}(min)	250			ns	(Note 2)
Internal Gain in T_{ON} Generation	K_{TON}		40		μs/V	(Note 2)

Note 1: Recommended Operating Conditions: V_{IN}=3.3V, V_{CC}=+6.5V, V_{SS}=-6.0V, V_{PP}=+135V, V_{NN}= -135V all input pins =0V unless noted. T_J=25°C

2: Design guidance only.

3: Specification is obtained by characterization and is not 100% tested.

TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: unless otherwise specified, all limits apply for $T_A = T_J = 25°C$; **Boldface** specifications apply over the full operating temperature range of $T_A = T_J = -40°C$ to 125°C. Typical values are at +25°C. RT = 200kΩ, EN = 3.3V, V_{PP}= +135V, V_{NN}= -135V, V_{PF}= +123V, V_{NF}= -123V, V_{CC}= +6.5V, V_{SS}= -6.0V, V_{LL}= +3.3V, V_{IN} = +3.3V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Over Voltage Protection						
OVPP Set Point	$OVPP_R$	**-3%**	**1.19**	**+3%**	V	V_{IN} = 3.7V
OVPN Set Point	$OVPN_R$	**-3%**	**1.07**	**+3%**	V	V_{IN} = 3.7V
OVP Hysteresis	OVP_{HYS}		0.12		V	
OVP Comparator Delay Time	OVP_{DLY}		50		ns	100 mV overdrive (Note 2)
VSSPUL DRIVER						
VSSPUL Switching Frequency	f_{PUL}		500		kHz	
VSSPUL High Level Output	V_{OH}	5.75			V	V_{DD} = 6.5V, I_O = 5 mA
VSSPUL Low Level Output	V_{OL}			0.25	V	V_{DD} = 6.5V, I_O = 5 mA
Pull Up Resistance	$R_{ON(UP)}$			10	Ω	V_{DD} = 5.75V (Note 2)
Pull Down Resistance	$R_{ON(DN)}$			5	Ω	V_{DD} = 5.75V (Note 2)
Source and Sink Current	I_{PUL}	**11**			mA	I_L = 5mA at -6.0V output (Note 2)
Temp Sensor						
Threshold Temperature	T_{TH}	135			°C	Note 2
Power FET						
Drain to Source Breakdown voltage	BV_{DSS}	80			V	V_{GS} = 0V, I_D = 250 μA.
Drain to Source ON-Resistance	$R_{DS}(ON)$			60	mΩ	V_{GS} = 5V, V_{DS}=12V. (Note 2)
High-Voltage Driver						
Quiescent V_{PP} Supply Current (Sum of Current at V_{PP} and V_{PPO} Pins)	$I_{PP}Q$		**3.7**	**5.6**	mA	
Quiescent V_{NN} Supply Current (Sum of Current at V_{NN} and V_{NNO} Pins)	$I_{NN}Q$	**-5.8**	**-3.8**		mA	
Quiescent V_{PF} Supply Current (Source)	$I_{PF}Q$	**-5.2**	**-3.6**		mA	
Quiescent V_{NF} Supply Current (Source)	$I_{NF}Q$		**3.7**	**5.4**	mA	
Quiescent High-Voltage Positive Supply Resultant Current, $I_{PP}Q + I_{PF}Q$	$I_{PPR}Q$			**0.4**	mA	
Quiescent High-Voltage Negative Supply Resultant Current, $I_{NN}Q + I_{NF}Q$	$I_{NNR}Q$	**-0.4**			mA	

Note 1: Recommended Operating Conditions: V_{IN}=3.3V, V_{CC}=+6.5V, V_{SS}=-6.0V, V_{PP}=+135V, V_{NN}= -135V all input pins =0V unless noted. T_J=25°C

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TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: unless otherwise specified, all limits apply for $T_A = T_J = 25°C$; **Boldface** specifications apply over the full operating temperature range of $T_A = T_J = -40°C$ to 125°C. Typical values are at +25°C. RT = 200kΩ, EN = 3.3V, V_{PP}= +135V, V_{NN}= -135V, V_{PF}= +123V, V_{NF}= -123V, V_{CC}= +6.5V, V_{SS}= -6.0V, V_{LL}= +3.3V, V_{IN} = +3.3V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
V_{PP} Supply Current (Sum of current at V_{PP} and V_{PPO} pins)	I_{PP}			**7.5**	mA	V_{PP}=+90V, V_{NN}=-90V, V_{PF}=+78V, V_{NF}=-78V, f_{HVOUT} = 20kHz,C_L= 250 pF, Running two channels. Test pattern = Figure 1-3 with 12.5µs pulse width
V_{NN} Supply Current (Sum of current at V_{NN} and V_{NNO} pins)	I_{NN}	**-7.5**			mA	
High-Voltage Positive Supply Resultant Current, I_{PP} + I_{PF}	I_{PPR}			**2**	mA	V_{PP}=+90V, V_{NN}=-90V, V_{PF}=+78V, V_{NF}=-78V, f_{HVOUT} = 20kHz,C_L= 250 pF, Running two channels. Test pattern = Figure 1-3 with 12.5µs pulse width
High-Voltage Negative Supply Resultant Current, I_{NN} + I_{NF}	I_{NNR}	**-2**			mA	
V_{CC} Operating Supply Current	I_{CC}			**0.2**	mA	V_{PP}=+90V, V_{NN}=-90V, V_{PF}=+78V, V_{NF}=-78V, Test pattern = Figure 1-3 with 12.5µs pulse width
V_{SS} Operating Supply Current	I_{SS}	**-0.2**			mA	
V_{LL} Operating Supply Current	I_{LL}			**25**	mA	V_{LL} = +3.3V SCK = 32MHz, SDI = 16 MHz pulse train
V_{PF} Operating Supply Current	I_{PF}	**-5.5**			mA	V_{PP}=+90V, V_{NN}=-90V, V_{PF}=+78V, V_{NF}=-78V, f_{HVOUT} = 20kHz,C_L= 250 pF, Running two channels. Test pattern = Figure 1-3 with 12.5 µs pulse width
V_{NF} Operating Supply Current	I_{NF}			**5.5**	mA	
V_{NF} Negative Floating Supply Voltage	V_{NF}	**V_{NN}+9V**	**-**	**V_{NN}+13.2V**	V	
V_{PF} Positive Floating Supply Voltage	V_{PF}	**V_{PP}-13.2V**	**-**	**V_{PP}-9V**	V	

Note 1: Recommended Operating Conditions: V_{IN}=3.3V, V_{CC}=+6.5V, V_{SS}=-6.0V, V_{PP}=+135V, V_{NN}= -135V all input pins =0V unless noted. T_J=25°C

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TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: unless otherwise specified, all limits apply for $T_A = T_J = 25°C$; **Boldface** specifications apply over the full operating temperature range of $T_A = T_J = -40°C$ to 125°C. Typical values are at +25°C. RT = 200kΩ, EN = 3.3V, V_{PP}= +135V, V_{NN}= -135V, V_{PF}= +123V, V_{NF}= -123V, V_{CC}= +6.5V, V_{SS}= -6.0V, V_{LL}= +3.3V, V_{IN} = +3.3V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
HV_{OUT} Switching Frequency	f_{HVOUT}	**0**		**25**	kHz	V_{PP}=+90V, V_{NN}=-90V, V_{PF}=+78V, V_{NF}=-78V, C_L=250pF, Test pattern = Figure 1-3 with 12.5µs pulse width
HV_{OUT} Output Source and Sink urrent	I_{HVOUT}	**24**			mA	V_{PP}=+90V, V_{NN}=-90V, V_{PF}=+78V, V_{NF}=-78V
Return-To-Zero Slew Rate 90% to 10% (i) from V_{PP} to 0V (ii) from V_{NN} to 0V	SR	**40**	**100**	**200**	V/µs	V_{PP}=+90V,V_{NN}=-90V, V_{PF}=+78V,V_{NF}=-78V, V_{CC}=+6.5V,V_{SS}=-6.0V C_L = 250 pF
Delay time for output to start rise/fall (from $\overline{LATCHA}$, $\overline{B}$, $\overline{C}$, $\overline{D}$ to 1V of HV_{OUT})	$t_{d(ON/OFF)}$			100	ns	V_{PP} = +135 V, V_{NN} = -135 V, V_{CC}= 6.5V, V_{SS} = -6.0V No load. (Note 3)
Variation of delay time (channel to channel)	Δt_d			40	ns	(Note 3)
Shutdown pin input enable voltage	$V_{IH(SHDN)}$	2.5			V	
VPPSENSE and VNNSENSE Current Sensor						
VPPSENSE/VNNSENSE Output Voltage	V_{out} (VPPSENSE/ VNNSENSE)	**0**		**3.6**	V	V_{PP} = +135V, V_{NN} = -135V, V_{CC} = +6.5V, V_{SS} = -6.0V
Voltage Gain of Current Sensor	AV_{SENSE} (-40°C to 125°C)	**-14%**	**3.1**	**+14%**	V/V	V_{PP} = +135V, V_{NN} = -135V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{PP}-V_{PPO} and V_{NNO}-V_{NN}: from 0.1V to 1.0V
Sensing Amplifier Output Offset	V_{OS}	**-280**		**+280**	mV	V_{PP} = +135V, V_{NN} = -135V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{PP}-V_{PPO} and V_{NNO}-V_{NN}: from 0.1V to 1.0V

Note 1: Recommended Operating Conditions: V_{IN}=3.3V, V_{CC}=+6.5V, V_{SS}=-6.0V, V_{PP}=+135V, V_{NN}= -135V all input pins =0V unless noted. T_J=25°C

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TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: unless otherwise specified, all limits apply for $T_A = T_J = 25°C$; **Boldface** specifications apply over the full operating temperature range of $T_A = T_J = -40°C$ to 125°C. Typical values are at +25°C. RT = 200kΩ, EN = 3.3V, V_{PP}= +135V, V_{NN}= -135V, V_{PF}= +123V, V_{NF}= -123V, V_{CC}= +6.5V, V_{SS}= -6.0V, V_{LL}= +3.3V, V_{IN} = +3.3V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Rise Time (Time from 10% to 90% of targeted value)	t_R			300	ns	(Note 3) V_{PP} = +90V, V_{NN} = -90V, V_{CC} = +6.5V, V_{SS} = -6.0V, C_L=3pF, Test pulse: 1V, 1µs pulse width 1. V_{PP} and V_{PPO} 2. V_{NN} and V_{NNO}
Rise Time (Time from 10% to 90% of targeted value)	t_R			740	ns	V_{PP} = +90V, V_{NN} = -90V, V_{CC} = +6.5V, V_{SS} = -6.0V, C_L=20pF, Test pulse: 1V, 1µs pulse width 1. V_{PP} and V_{PPO} 2. V_{NN} and V_{NNO}
VPPSENSE/VNNSENSE Output Load	R_{LOAD}	10			MΩ	(Note 2)
	C_{LOAD}			3	pF	(Note 2)
SPI Interface						
Digital Input Clock frequency	f_{CLK}			**32**	MHz	Note: 3.3V logic input
High-level input logic voltage	V_{IH}	**$0.8V_{LL}$**			V	
Low-level input logic voltage	V_{IL}	**0**		**$0.2V_{LL}$**	V	
Logic I/O pin rise and fall time	t_R, t_F			5	ns	(Note 3) C_L=15pF
Sourced by any standard I/O pin	Isource	**10**			mA	(Note 2)
Sunk by any standard I/O pin	Isink	**10**			mA	(Note 2)
SPI Quiescent current of low-voltage supplies with Shut-down asserted	$I_{LL}Q$			100	µA	In shutdown mode. All logic input = 0V. $V_{(SHDN)} = V_{LL}$
Time to enter and exit shut-down	t_{SHDN}			1	ms	SCK=32MHz and SDI = 16MHz pulse train.
Time from chip select and SPI data	t_{WAIT}	20	50	-	ns	Refer to **Figure 1-1** **(Note 2)**
Time to transfer 128-bits of data	t_{PKT}	4	-	-	µs	Refer to **Figure 1-1** **(Note 2)**
Time from last clock pulse to $\overline{\text{LATCHIN}}$	$t_{H(LAT)}$	20	50	-	ns	Refer to **Figure 1-1** **(Note 2)**
Digital Interface						
Time SPI latch held low	t_{ab}	20	50	-	ns	Refer to **Figure 1-2** **(Note 2)**
Time between SPI latches	t_{ac}	10	12	-	µs	Refer to **Figure 1-2** **(Note 2)**

Note 1: Recommended Operating Conditions: V_{IN}=3.3V, V_{CC}=+6.5V, V_{SS}=-6.0V, V_{PP}=+135V, V_{NN}= -135V all input pins =0V unless noted. T_J=25°C

2: Design guidance only.

3: Specification is obtained by characterization and is not 100% tested.

TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: unless otherwise specified, all limits apply for $T_A = T_J = 25°C$; **Boldface** specifications apply over the full operating temperature range of $T_A = T_J = -40°C$ to 125°C. Typical values are at +25°C. RT = 200kΩ, EN = 3.3V, V_{PP}= +135V, V_{NN}= -135V, V_{PF}= +123V, V_{NF}= -123V, V_{CC}= +6.5V, V_{SS}= -6.0V, V_{LL}= +3.3V, V_{IN} = +3.3V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Time from SPI latch assert to data valid	t_{ae}	-	10	20	ns	Refer to **Figure 1-2** (**Note 2**)
Time from SPI latch to data latch	t_{ak}	20	50	-	ns	Refer to **Figure 1-2** (**Note 2**)
Time latch signal held high	t_{gk}	20	50	-	ns	Refer to **Figure 1-2** (**Note 2**)
Time latch signal held low	t_{mn}	20	50	-	ns	Refer to **Figure 1-2** (**Note 2**)
Time between two data latch events	t_{rs}	80	100	-	ns	Refer to **Figure 1-2** (**Note 2**)
Propagation delay from data register to output register	t_{kv}	-	10	20	ns	Refer to **Figure 1-2** (**Note 2**)

Note 1: Recommended Operating Conditions: V_{IN}=3.3V, V_{CC}=+6.5V, V_{SS}=-6.0V, V_{PP}=+135V, V_{NN}= -135V all input pins =0V unless noted. T_J=25°C

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistance						
Thermal Resistance, 105B-9x9 TFBGA	θ_{JA}	—	38.1	—	°C/W	

1.1 Timing Diagrams

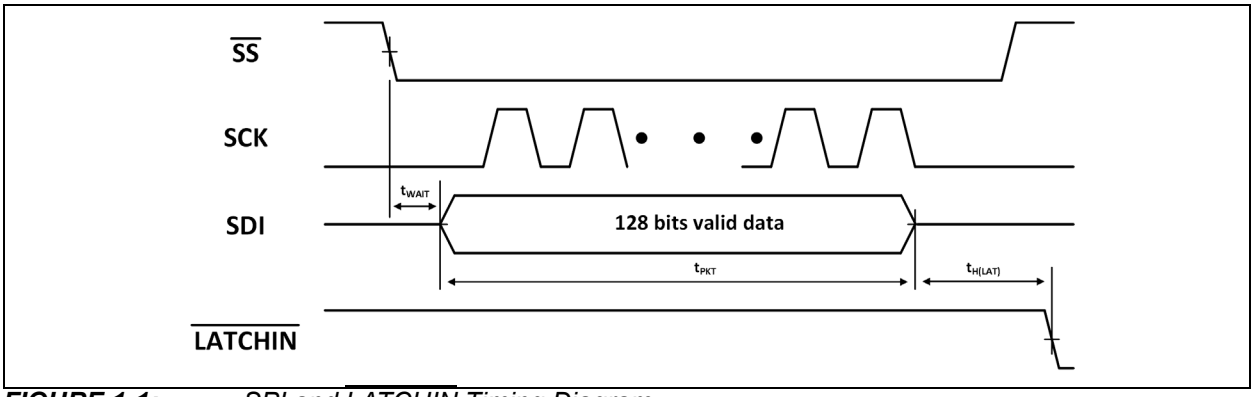

FIGURE 1-1: *SPI and LATCHIN Timing Diagram*

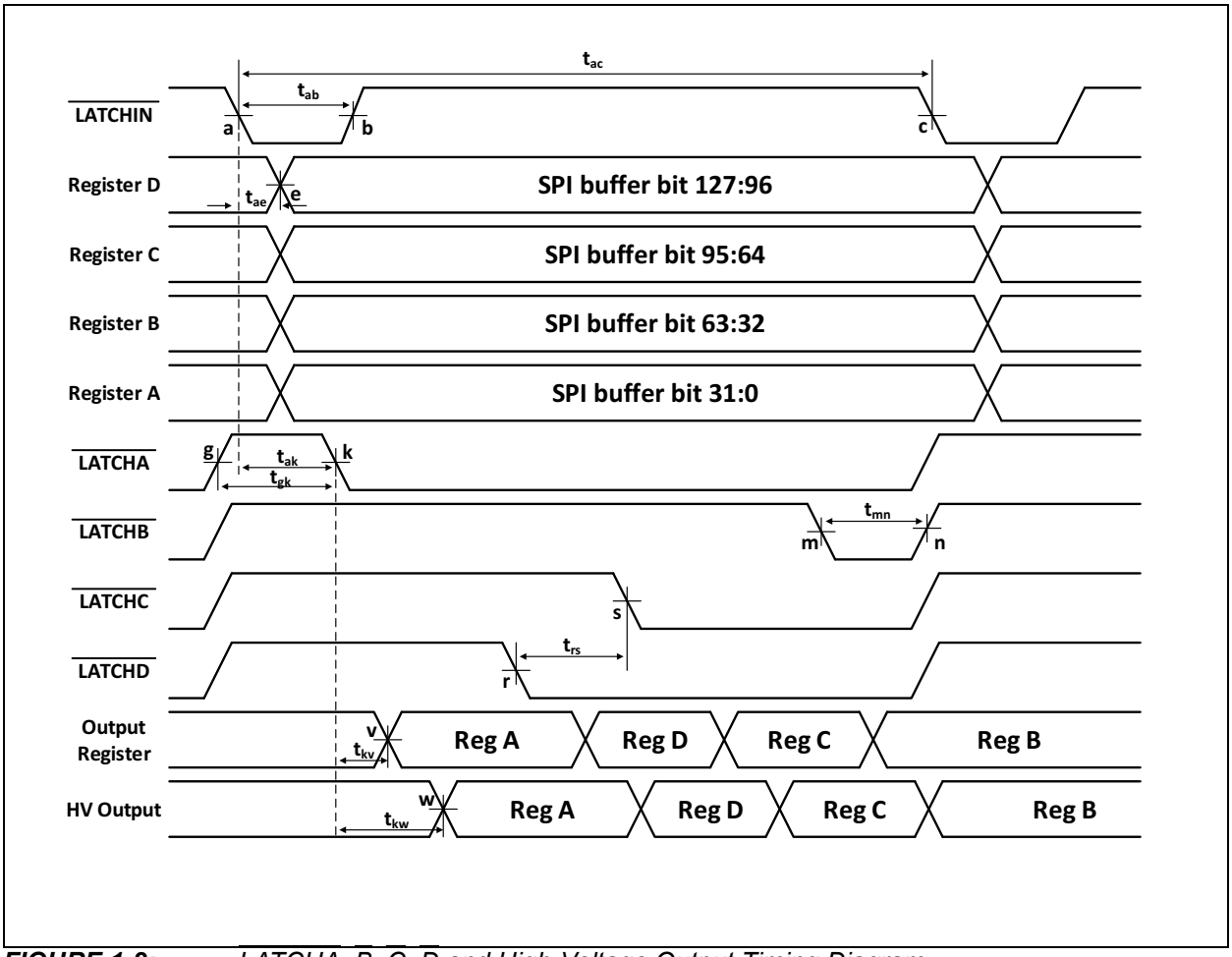

FIGURE 1-2: *LATCHA, B, C, D and High-Voltage Output Timing Diagram*

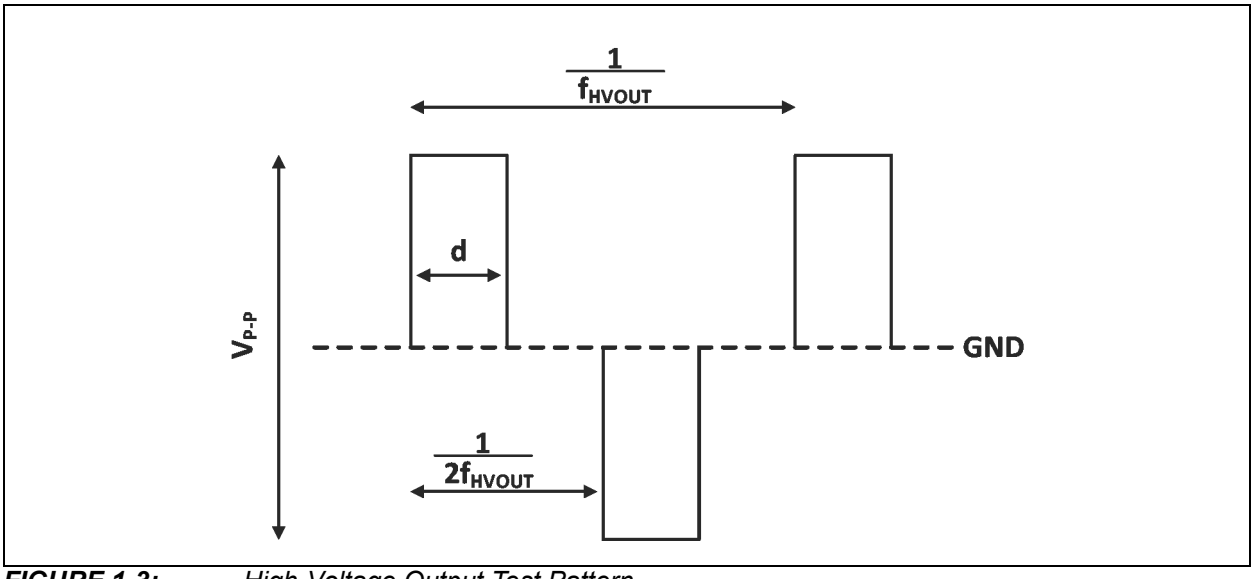

FIGURE 1-3: *High-Voltage Output Test Pattern*

1.2 Typical Performance Curves

Note: The graphs and tables provided below are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

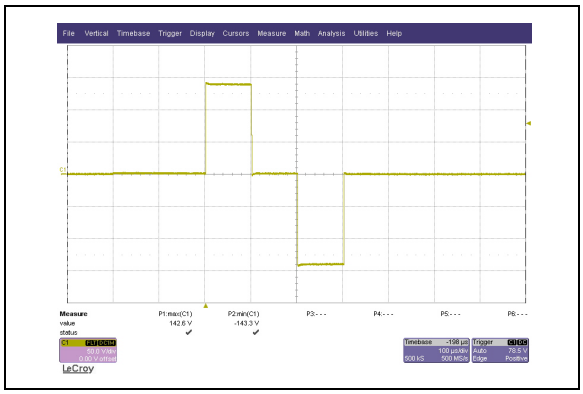

FIGURE 1-4: *Typical HV_{OUT} output waveform V_{PP}=135V V_{NN}=-135V, Load = 100pF*

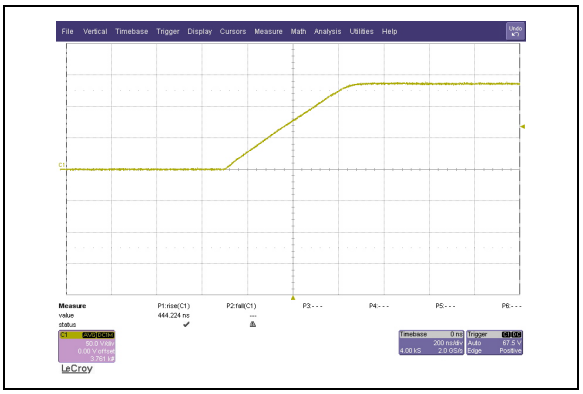

FIGURE 1-7: *Typical HV_{OUT} from 0V to 135V, Load = 100pF*

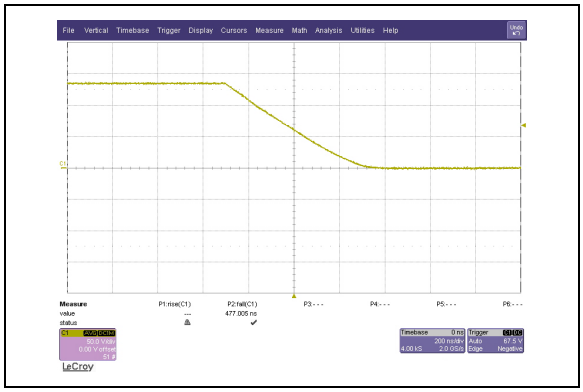

FIGURE 1-5: *Typical HV_{OUT} from 135V to 0V, Load = 100pF*

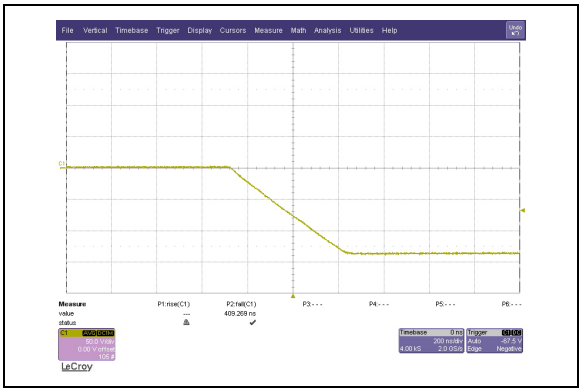

FIGURE 1-8: *Typical HV_{OUT} from 0V to -135V, Load = 100pF*

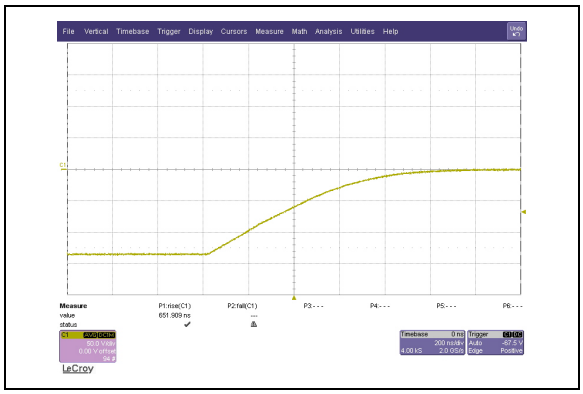

FIGURE 1-6: *Typical HV_{OUT} from -135V to 0V, Load = 100pF*

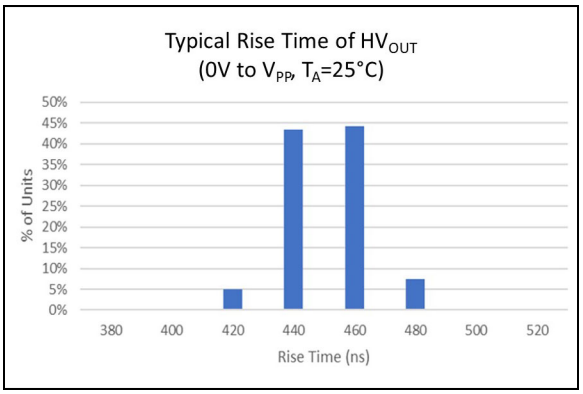

FIGURE 1-9: *Typ. HV_{OUT} Rise Time Distribution, HV_{OUT} from 0V to 90V, Load = 250pF*

Note: The graphs and tables provided below are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

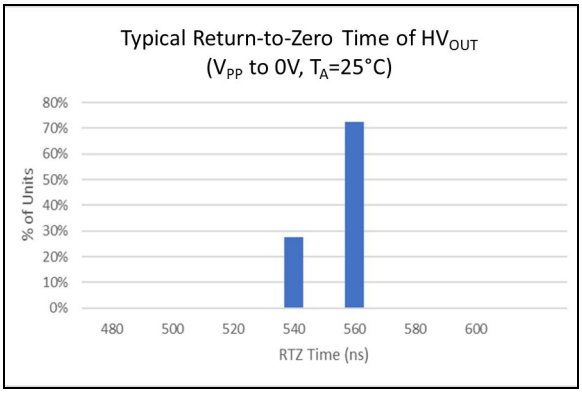

FIGURE 1-10: *Typ. HV_{OUT} Fall Time Distribution, from 90V to 0V, Load = 250pF*

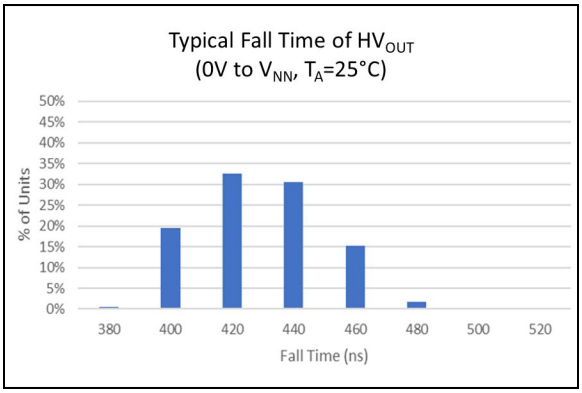

FIGURE 1-13: *Typ. HV_{OUT} Fall Time Distribution, from 0V to -90V, Load = 250pF*

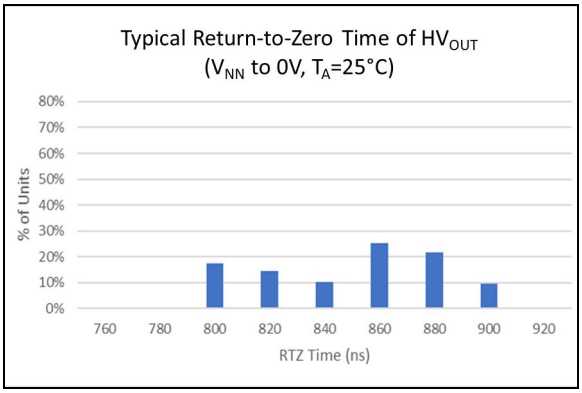

FIGURE 1-11: *Typ. HV_{OUT} Rise Time Distribution, from -90V to 0V, Load = 250pF*

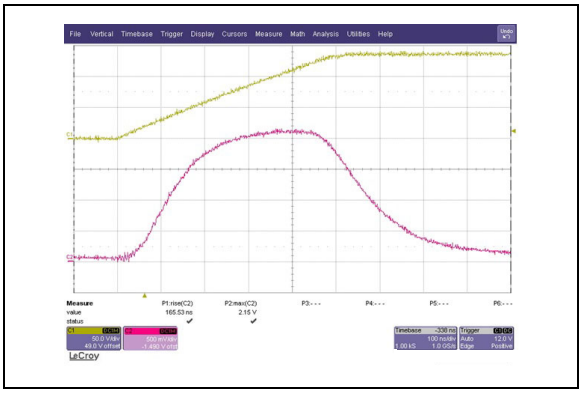

FIGURE 1-14: *Typical VPPSENSE Buffered Output, V_{PP}=135V, V_{NN}=-135V, Load=100pF, 6.04ohm Sense Resistor, Four Channels Active*

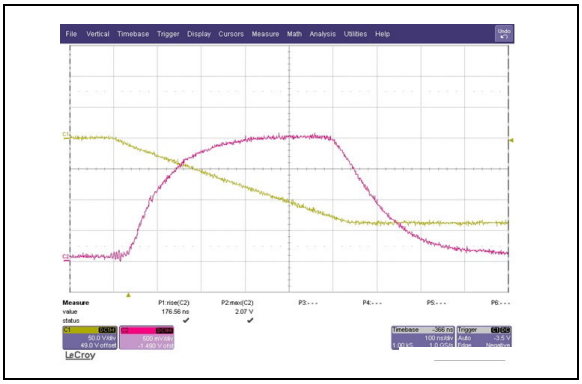

FIGURE 1-12: *Typical VNNSENSE buffered output, V_{PP}=135V, V_{NN}=-135V, Load=100pF, 6.04ohm sense resistor, four channels active*

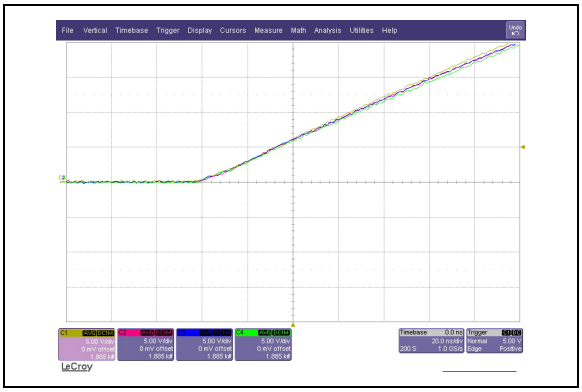

FIGURE 1-15: *Typical HV_{OUT} Channel-to-Channel Delay*

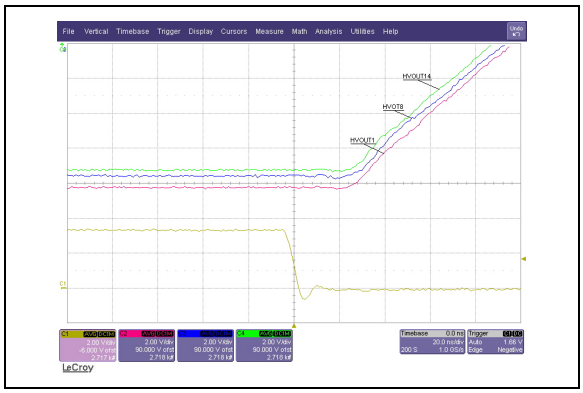

FIGURE 1-16: *Typical $\overline{LATCHA}$ to HV_{OUT} Propagation Delay.*

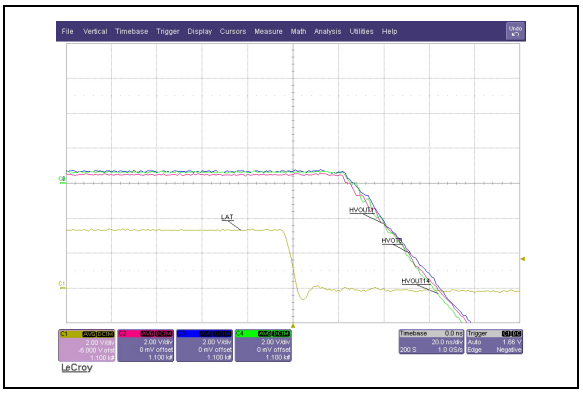

FIGURE 1-19: *Typical $\overline{LATCHB}$ to HV_{OUT} Propagation Delay.*

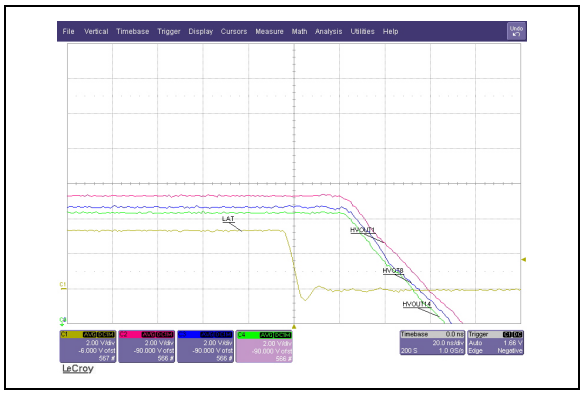

FIGURE 1-17: *Typical $\overline{LATCHC}$ to HV_{OUT} Propagation Delay.*

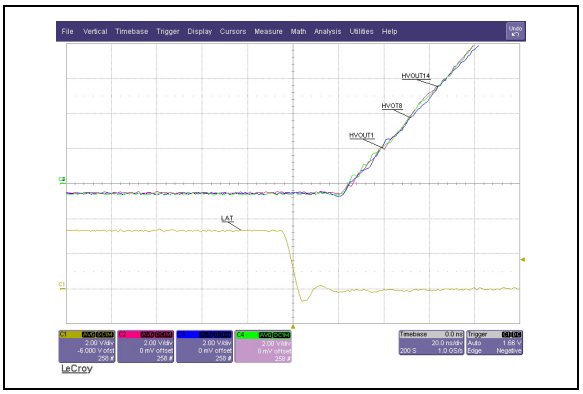

FIGURE 1-20: *Typical $\overline{LATCHD}$ to HV_{OUT} Propagation Delay.*

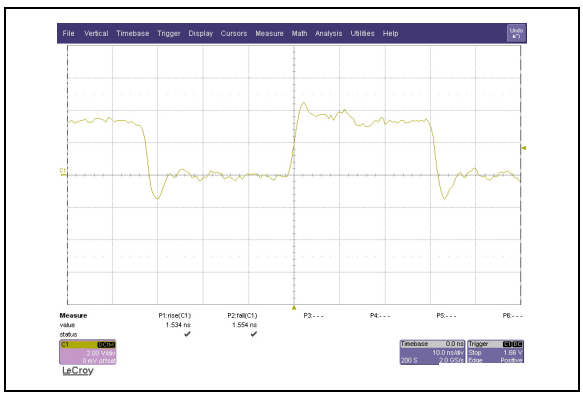

FIGURE 1-18: *Typical SDO output Rise Time and Fall Time.*

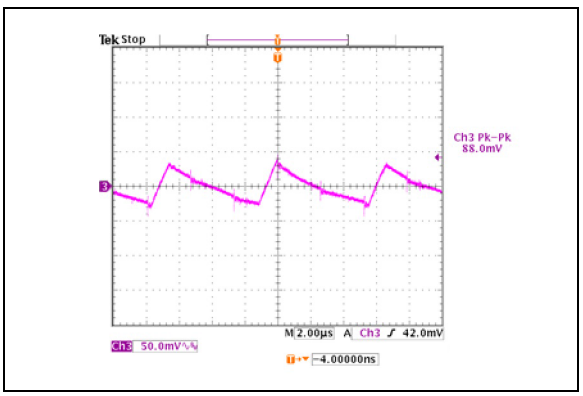

FIGURE 1-21: *Typical Charge Pump Output Noise Ripple.*

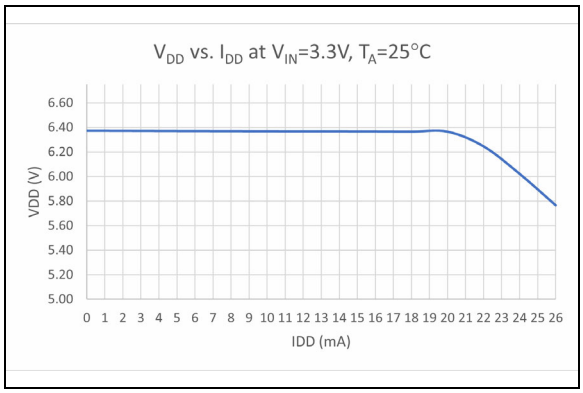

FIGURE 1-22: *Typical Charge Pump Output Voltage vs Output current V_{IN}=3.3V.*

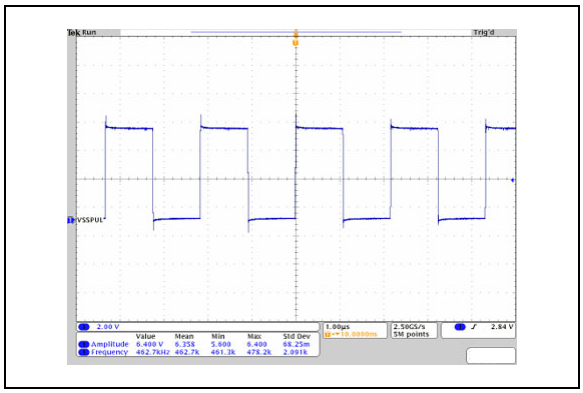

FIGURE 1-23: *Typical VSSPUL output waveform Io = -5mA.*

2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin	Symbol	Description
E13	V_{PP}	Positive High-Voltage Supply
C13	V_{PPO}	Positive High-Voltage Current Sense
L13	V_{NN}	Negative High-Voltage Supply
N13	V_{NNO}	Negative High-Voltage Current Sense
C8	V_{CC}	Positive Low-Voltage Supply
C10	V_{SS}	Negative Low-Voltage Supply
C7	V_{LL}	VLL Logic Voltage
D3, E3, H4-6, G5-6.E6, F6	HVGND	High-Voltage Ground
G13	V_{PF}	Positive floating voltage supply reference to V_{PP} level
J13	V_{NF}	Negative floating voltage supply reference to V_{NN} level
N11	FILN	0.1uF cap across FILN and VNNO
A13	FILP	0.1uF cap across FILP and VPPO
C3	VPPSENSE	Positive High-Voltage Sense Analog Output
F3	VNNSENSE	Negative High-Voltage Sense Analog Output
E10	VLDO	LDO output pin
G3	NC	No Connection. (Do not connect. Keep the pin floating)
H3	NC	No Connection. (Do not connect. Keep the pin floating)
A11	$HV_{OUT}0$	High-Voltage Output 0
A9	$HV_{OUT}1$	High-Voltage Output 1
A7	$HV_{OUT}2$	High-Voltage Output 2
A5	$HV_{OUT}3$	High-Voltage Output 3
A3	$HV_{OUT}4$	High-Voltage Output 4
A1	$HV_{OUT}5$	High-Voltage Output 5
C1	$HV_{OUT}6$	High-Voltage Output 6
E1	$HV_{OUT}7$	High-Voltage Output 7
G1	$HV_{OUT}8$	High-Voltage Output 8
J1	$HV_{OUT}9$	High-Voltage Output 9
L1	$HV_{OUT}10$	High-Voltage Output 10
N1	$HV_{OUT}11$	High-Voltage Output 11
N3	$HV_{OUT}12$	High-Voltage Output 12
N5	$HV_{OUT}13$	High-Voltage Output 13
N7	$HV_{OUT}14$	High-Voltage Output 14
N9	$HV_{OUT}15$	High-Voltage Output 15
C5	$\overline{SS}$	SPI Chip Select
D5	SDI	SPI Data In

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin	Symbol	Description
E5	SDO	SPI Data Out (for daisy chain)
F5	SCK	SPI Clock
G4	$\overline{\text{LATCHIN}}$	Latch SPI Data (SPI -> Latch A, B, C, D)
F4	$\overline{\text{LATCHA}}$	Latch A -> Output Register
E4	$\overline{\text{LATCHB}}$	Latch B -> Output Register
D4	$\overline{\text{LATCHC}}$	Latch C -> Output Register
C4	$\overline{\text{LATCHD}}$	Latch D -> Output Register
H8	V_{IN}	Input Voltage
J8	V_{DD}	Positive Low-Voltage Supply
K10,L10	PGND	Power Ground
C9,F11	AGND	Analog Ground
K11	CCP2N	Charge Pump 2 NEG
L11	CCP2P	Charge Pump 2 POS
H11	CCP1N	Charge Pump 1 NEG
J11	CCP1P	Charge Pump 1 POS
H9	T_{ON}	T_{ON} pin
J10	RT	RT pin
D11	VBFB	FB Bias
E9	VBOVP	OVP Bias
E11	REF	Controller Voltage Reference
C11	VSSPUL	VSS Pulse Train
F10	TEMP	Temp Sensor Output
F9	SHORT	Short circuit indicator
F8	SHTEN	Short circuit protection enable
C6	SHDN	Shutdown Mode
F7	STDBY	Standby Mode
J9	EN	DC/DC Enable
G7	SEQ3	Power Sequence Channel 3
G8	SEQ2	Power Sequence Channel 2
G9	SEQ1	Power Sequence Channel 1
G10	SEQ0	Power Sequence Channel 0
H10	TRIG	Power ON/OFF Sequence Trigger
G11	CSEQ	Sequence timer. External capacitor to ground
J7	SHTP	Short Sense POS
H7	SHTN	Short Sense NEG
D7	OVPP	Over-voltage POS
D8	OVPN	Over-voltage NEG
D9	FBP	Feedback POS
D10	FBN	Feedback NEG

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin	Symbol	Description
E8	NC	No Connection (Do not connect. Keep the pin floating)
E7	Reserved	Reserved pin. Connect to Ground.
D6	Reserved	Reserved pin. Connect to Ground.
J3-4, K3-4,L3-4	S	Source of Power FET
J5-6, K5-9,L5-9	D	Drain of Power FET

3.0 DEVICE DESCRIPTION

3.1 Serial Peripheral Interface

The SPI interface is used to transfer data of the channel settings from the host controller to the high-voltage driver. The HV53001 operates as an SPI slave device and receives 128 bits of data from the master device (host controller). The HV53001 SPI interface is designed to be compatible with all Microchip 8-bit, 16-bit and 32-bit SPI data transmission formats. This SPI interface has a 128-bit shift register buffer to store 128 bits of data.

The $\overline{SS}$ pin is a chip select function which is similar to the enable function to guard the clock and data input signal. The SCK contains the bus clock signal from the host processor. The SDI and SDO are the data input and data output pins of the SPI shift register buffer.

SDI and SDO can be used to cascade multiple HV53001 or HV53011 drivers together if only a single SPI port is available. This SPI interface is compatible with 3.3V logic input voltage with its maximum clock frequency of 32 MHz.

The SPI shift register captures the data at the SDI input in the rising edge of the SCK clock and pushes out the data from the buffer to the SDO output in the falling edge of the SCK clock. When the SPI bus is at idle status, the $\overline{SS}$ pin stays in logic "1" and the SCK clock is expected to stay at "0".

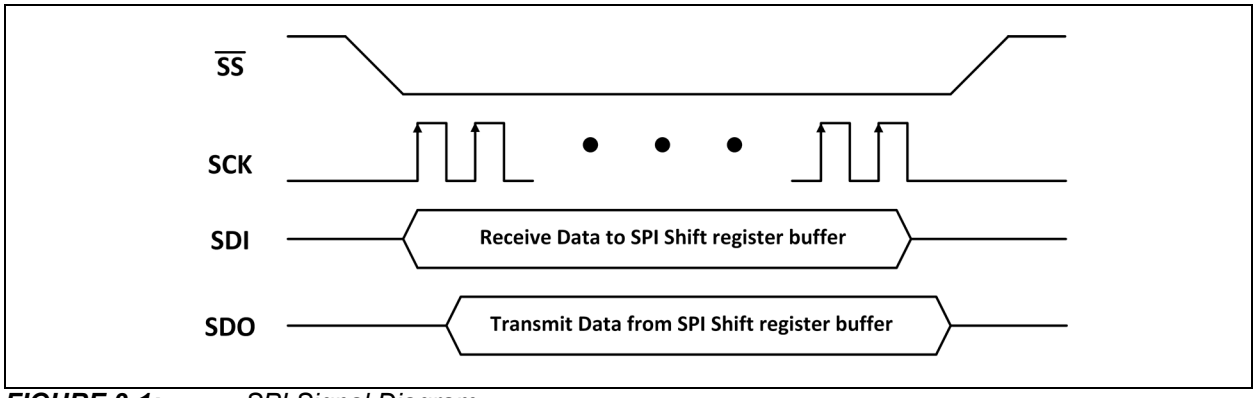

FIGURE 3-1: *SPI Signal Diagram.*

The bit order of the SDI data input is defined in the following. The first and second data bits represent bit 1 and bit 0 of channel 15 in register D, respectively. The third and fourth bits represent bit 1 and bit 0 of channel 14 in register D. This pattern is extended all the way to channel 0. Hence, there are 32 data bits to control register D to cover all sixteen channels.

The next 32 data bits are arranged in the same fashion for register C. Similarly, the exact pattern repeats itself for register B and A. Since each register (A, B, C and D) contains 32 bits of data, the SPI shift register buffer is 128 bits long.

Bit 1 of channel 15 in register D is defined as the MSb (Most Significant bit) and bit 0 of channel 0 in register A as the LSb (Least Significant bit) in this SPI shift register buffer definition.

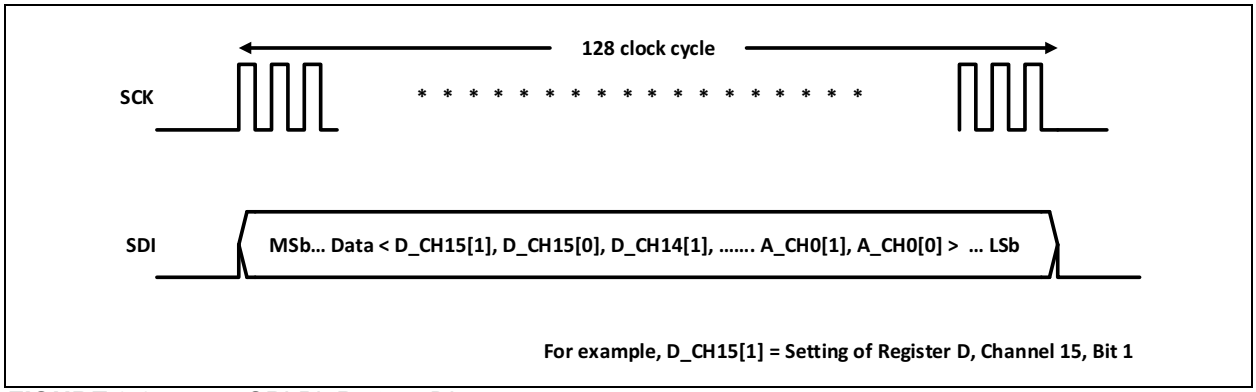

FIGURE 3-2: *SPI Bit Pattern Diagram.*

The following table shows the summary of the SPI shift register buffer.

TABLE 3-1: REGISTER LEGEND

Sym	Description	Sym	Description
R	Readable bit	HC	Cleared by Hardware only
W	Writable bit	HS	Set by Hardware only
U	Unimplemented bit, read as '0'	1	Bit is set at Reset
P	Programmable bit	0	Bit is cleared at Reset
S	Settable bit	x	Bit is unknown at Reset
C	Clearable bit		
Example: R/W - 0 indicates the bit is both readable or writable, and reads '0' after a Reset.			

TABLE 3-2: SPI_SR 128-BIT BUFFER SUMMARY

Register Name	Bit Range	Bit 127/119/111/103	Bit 126/118/110/102	Bit 125/117/109/101	Bit 124/116/108/100	Bit 123/115/107/99	Bit 122/114/106/98	Bit 121/113/105/97	Bit 120/112/104/96
$\overline{\text{LATCHD}}$	<127:120>	CH15<1:0>		CH14<1:0>		CH13<1:0>		CH12<1:0>	
	<119:112>	CH11<1:0>		CH10<1:0>		CH9<1:0>		CH8<1:0>	
	<111:104>	CH7<1:0>		CH6<1:0>		CH5<1:0>		CH4<1:0>	
	<103:96>	CH3<1:0>		CH2<1:0>		CH1<1:0>		CH0<1:0>	
Register Name	Bit Range	Bit 95/87/79/71	Bit 94/86/78/70	Bit 93/85/77/69	Bit 92/84/76/68	Bit 91/83/75/67	Bit 90/82/74/66	Bit 89/81/73/65	Bit 88/80/72/64
$\overline{\text{LATCHC}}$	<95:88>	CH15<1:0>		CH14<1:0>		CH13<1:0>		CH12<1:0>	
	<87:80>	CH11<1:0>		CH10<1:0>		CH9<1:0>		CH8<1:0>	
	<79:72>	CH7<1:0>		CH6<1:0>		CH5<1:0>		CH4<1:0>	
	<71:64>	CH3<1:0>		CH2<1:0>		CH1<1:0>		CH0<1:0>	
Register Name	Bit Range	Bit 63/55/47/39	Bit 62/54/46/38	Bit 61/53/45/37	Bit 60/52/44/36	Bit 59/51/43/35	Bit 58/50/42/34	Bit 57/49/41/33	Bit 56/48/40/32
$\overline{\text{LATCHB}}$	<63:56>	CH15<1:0>		CH14<1:0>		CH13<1:0>		CH12<1:0>	
	<55:48>	CH11<1:0>		CH10<1:0>		CH9<1:0>		CH8<1:0>	
	<47:40>	CH7<1:0>		CH6<1:0>		CH5<1:0>		CH4<1:0>	
	<39:32>	CH3<1:0>		CH2<1:0>		CH1<1:0>		CH0<1:0>	
Register Name	Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
$\overline{\text{LATCHA}}$	<31:24>	CH15<1:0>		CH14<1:0>		CH13<1:0>		CH12<1:0>	
	<23:16>	CH11<1:0>		CH10<1:0>		CH9<1:0>		CH8<1:0>	
	<15:8>	CH7<1:0>		CH6<1:0>		CH5<1:0>		CH4<1:0>	
	<7:0>	CH3<1:0>		CH2<1:0>		CH1<1:0>		CH0<1:0>	

3.2 Quad-Latched Two-Bit per Channel Architecture

In the Quad-Latched 2-bit per channel architecture, each channel is controlled by a 2-bit encoding for each of the four possible states: "00" = (Hi-Z) high impedance, "01" = pull-down to V_{NN}, "10" = pull-up to V_{PP}, "11" = driven to ground. Since there are 16 channels on each HV53001 device, a 32-bit output control register is required.

Four separate latched arrays (A, B, C and D) hold four possible 32-bit output configurations. The data is loaded from the arrays into the output control register by four separate external control signals ($\overline{\text{LATCHA, B, C, D}}$). When the output control register is being updated using one of the latch signals, the output will go to a not driven state temporarily to avoid shoot-through.

The data in these four latched arrays can be updated by the SPI shift register buffer. The 128 bits of data is first transmitted from the host process to this device via the SPI interface. The data format has been discussed in the previous section. After the 128 bits transaction completes, the data will stay in the SPI shift register buffer. The user then sends an activation signal at the $\overline{\text{LATCHIN}}$ pin to initiate the transfer of the data from the SPI shift register to the four 32-bit registers (A, B, C and D).

When the application requires more output channels, the user can cascade more driver devices in a daisy chain configuration. The SDO pin is used to pass the data from the SPI shift register buffer to the cascaded driver.

The SPI signal pins (SCK, $\overline{SS}$, SDI and SDO) are used to control the data flow of the SPI shift register buffer. The five latch control signals ($\overline{LATCHIN}$, $\overline{LATCHA}$, $\overline{LATCHB}$, $\overline{LATCHC}$ and $\overline{LATCHD}$) are used to control the data selection of the high-voltage output from the four 32-bit registers. The SPI interface and latch functions are two independent operation blocks.

To achieve some power savings when idling for a period of time, a shutdown pin is available to reduce the quiescent current draw as much as possible.

TABLE 3-1: 2-BIT CONTROL AND OUTPUT VOLTAGE LOGIC TABLE

CONTROL BITS		HVOUT OUTPUT
Bit 1	Bit 0	
0	0	High impedance (Hi-Z)
0	1	Driven Low (V_{NN})
1	0	Driven High (V_{PP})
1	1	Driven to Ground (0V)

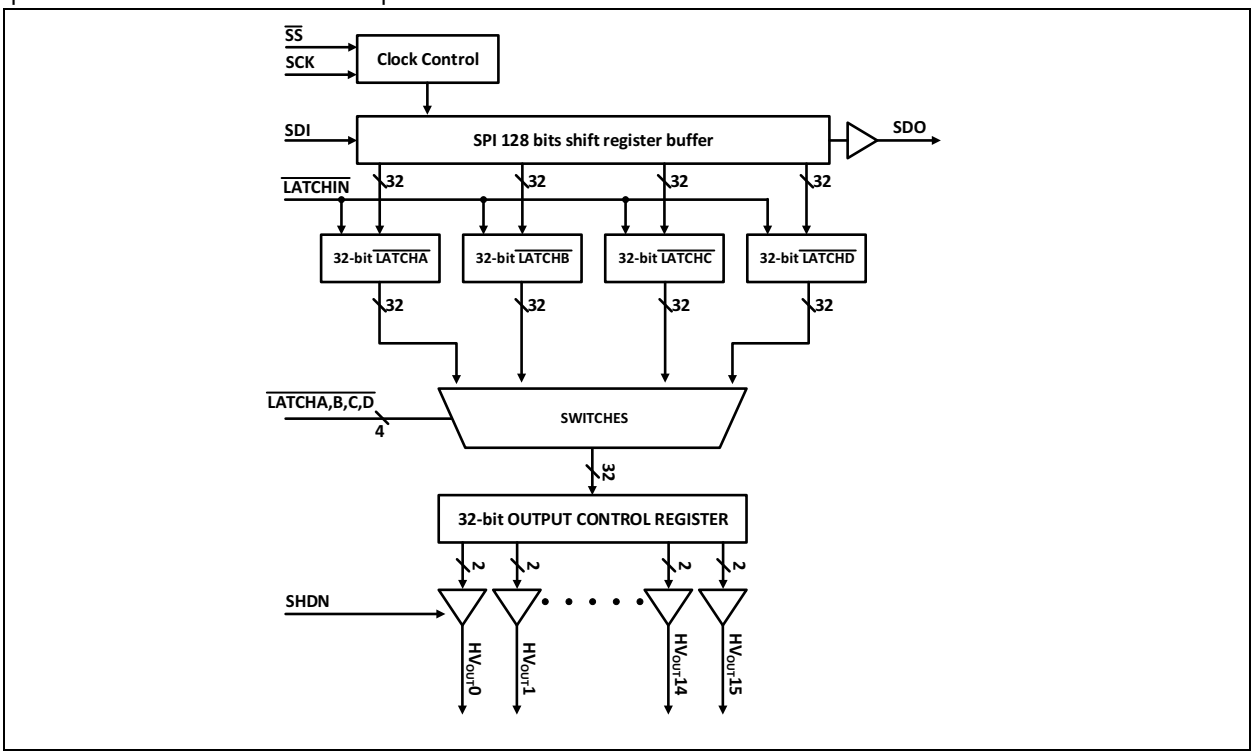

FIGURE 3-3: *Quad-Latched Two-Bit per Channel Architecture.*

TABLE 3-3: QUAD-LATCHED TWO-BIT LOGIC STATE TABLE

$\overline{LATCHIN}$	$\overline{LATCHA}$	$\overline{LATCHB}$	$\overline{LATCHC}$	$\overline{LATCHD}$	Description
↓	X	X	X	X	SPI bit[127:96] into Latch Register D SPI bit[95:64] into Latch Register C SPI bit[63:32] into Latch Register B SPI bit[31:0] into Latch Register A
X*	↓	X	X	X	Register A to output
X*	X	↓	X	X	Register B to output
X*	X	X	↓	X	Register C to output
X*	X	X	X	↓	Register D to output

Note: * = $\overline{LATCHX}$ should be delayed appropriately if a register update from $\overline{LATCHIN}$ is still in progress.
↓ = Negative edge-triggered
X = Don't care

3.3 Driver Shutdown Mode

When the shutdown (SHDN) pin is at logic "1", any unnecessary circuit in the line driver is disabled to minimize the power consumption. It includes the level translator, bias current, voltage reference, driver output, SPI interface and combinational logic. During shutdown, the I_{LL} quiescent current is less than 100 μA. The system response time is less than 1 ms to switch between shutdown and active states when a new signal is asserted at the shutdown pin.

3.4 Driver Power On Reset

The Power-on Reset function resets all high-voltage HV_{OUT} output to high impedance when the device is initially powered on. It also resets and clears the SPI buffer registers, registers A, B, C and D, to logic "0".

3.5 Positive Charge Pump Regulator

The device is targeted to operate with a standard battery voltage range of 2.7V to 5.5V. An internal 3X charge pump converter is integrated to generate a regulated output at high-voltage level. This regulated output supply rail powers the gate driver to drive the power MOSFET transistor.

It is recommended to use 1 μF 16V X7R 0603 ceramic capacitors for the two CCP capacitors and a 10 μF 25V X5R 0805 ceramic capacitor for the output storage capacitor.

Note: Please consider the operating temperature for component selection.

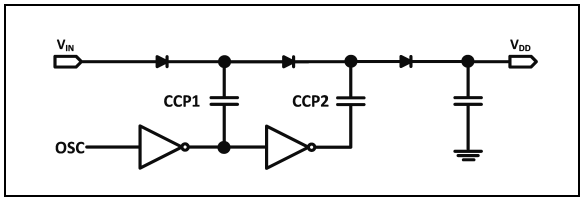

FIGURE 3-4: *Positive Charge Pump Converter Conceptual Diagram*

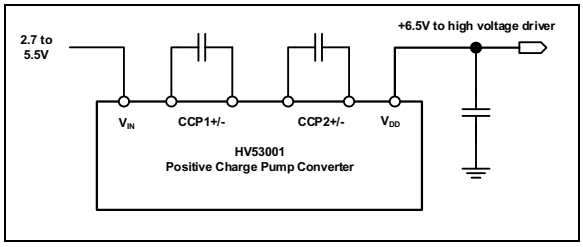

FIGURE 3-5: *HV53001 Positive Charge Pump Connections*

3.6 Negative Charge Pump

A continuous pulse train is created at the VSSPUL output and is used in conjunction with a few external components to create a negative charge pump circuit. The pulse train is a 0 to 6.5V square wave with a fixed oscillation frequency. This -6.0V negative low supply voltage is generated at the output of the external circuity and is capable of supplying a minimum of 5 mA. This negative supply provides enough power to operate the high-voltage driver device.

It is recommended to use 10 μF 25V X5R 0805 ceramic capacitors and B0530WS 400 mV 500 mA 30V Schottky diodes for this circuit.

Note: Please consider the operating temperature for component selection.

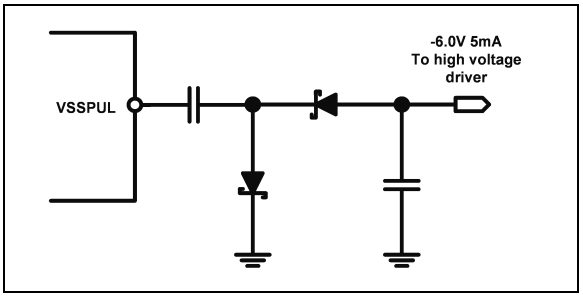

FIGURE 3-6: *Negative Charge Pump Converter*

3.7 Standby Mode

Standby mode is used to guard the PWM pulses from the DC/DC controller to the power FET. It momentarily disables the gate driver of the power FET to minimize the noise level so that the output current sensor can measure the output current precisely. While the device is in Standby mode, all other circuits are expected to be in their operating condition.

3.8 Enable Function

The enable function is used to switch the DC/DC controller on/off completely. When it is set to Off mode, all internal circuits of the DC/DC converter are turned off and minimum current is drawn. When the DC/DC converter is disabled, the boost converter, charge pump converter and linear regulator shut off.

The SHDN and EN are two separate controls. SHDN is for the high-voltage driver, and EN is for the DC/DC converter.

3.9 Power-On/Off Sequence Control

The HV53001 DC/DC converter generates multiple rails to power the high-voltage driver IC. The power-on sequence is important to the high-voltage IC because any incorrect power-on/off sequence may cause damage to the high-voltage driver IC.

A sequence control block is included in this device to avoid an incorrect sequence caused by user error which could damage the driver IC.

When a single pulse is asserted at the TRIG pin, the four sequence control outputs generate a logic "1" in sequential order. First, a logic "1" will appear in SEQ0, and then in SEQ1, SEQ2 and SEQ3. When a second pulse is asserted at the TRIG pin, a logic "0" appears in SEQ3, SEQ2, SEQ1 and SEQ0 sequentially in reverse order. The timing between each is controlled by an external capacitor connected at the CSEQ pin. The sequence switch time period is calculated in the following equation.

Tseq = 2 x ln(2) x R x CSEQ where R = 100 kΩ

The four sequence logic output signals, SEQ[3:0], can be used to control the enable function of the power module or external analog power switches to control the supply voltage rails.

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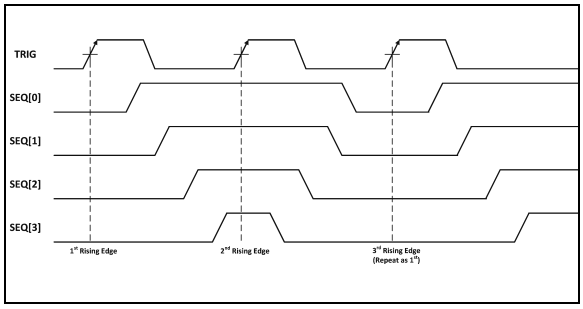


FIGURE 3-7: *Power-On/Off Sequence Control*

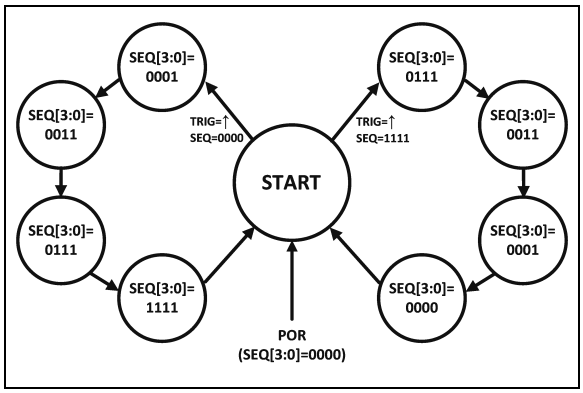


FIGURE 3-8: *Sequence On/Off Control State Diagram.*

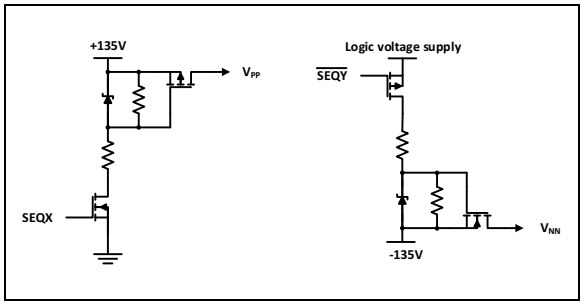


FIGURE 3-9: *Example of Power Switch Circuit*

TABLE 3-2: ACCEPTABLE POWER-ON SEQUENCES

Steps	Description
1	Connect ground.
2	Keep shutdown pin to low.
3	Set all driver inputs to low.
4	Apply V_{IN}.
5	Set all converter inputs to a known state.
6	The power-on sequence will enable supplies in this sequence: V_{LL}, V_{NN}, V_{NF}, V_{SS}, V_{CC}, V_{PF} and V_{PP}.
7	Set all inputs to a known state.

TABLE 3-3: ACCEPTABLE POWER-OFF SEQUENCES

Steps	Description
1	Set all inputs and shutdown pin to low.
2	The power-off sequence will disable supplies in this sequence: V_{PP}, V_{PF}, V_{CC}, V_{SS}, V_{NF}, V_{NN} and V_{LL}.
3	Disconnect V_{IN}.
4	Disconnect ground

3.10 Built-in DC/DC Converter

A hysteretic step-up DC/DC converter is integrated in this driver IC to generate two high-voltage rails, one positive and one negative. In normal operation, this converter operates at a fixed duty cycle and frequency. The controller monitors both positive and negative voltage rails alternately to regulate the output voltage.

The positive supply feedback input is a typical DC/DC feedback which monitors the feedback voltage from a resistor divider referenced to ground. When the sensing voltage is higher than the internal reference voltage, it deactivates the pulse in the next cycle. When the sensing voltage is lower, it activates the pulse.

For the negative supply feedback input, the controller provides a low DC bias voltage to map the feedback voltage above ground because the controller is powered by a low-voltage positive power rail. Hence, the negative supply feedback voltage is referenced to the bias voltage VBFB pin via the resistor divider network. The negative supply feedback path works differently from the positive supply feedback path since it senses the negative voltage. When the sensing voltage is higher than the internal reference voltage, it activates the pulse in the next cycle. When the sensing voltage is lower, it deactivates the pulse.

Based on the operation described above, the controller basically regulates the mid-point of the V_{PP} and V_{NN} voltage rails. As long as the two transformers are closely matched, the two high-voltage outputs can be coupled within a few percentage of each other. For matching the transformers, their absolute values are not important. The important factor is the difference between the two transformers. Since both transformers are built the same way, their secondary effects are very similar. The major factor is their primary parameter, magnetizing inductance.

In addition to the two extreme high-voltage rails, the driver requires two floating voltage rails. Both floating supplies are referenced to one of the extreme high-voltage outputs. These two floating supply rails are created using the multi-winding transformer and two 12V regulators. The positive voltage rail requires a negative 12V regulator referenced to V_{PP}. The negative voltage rail uses a positive 12V regulator reference to V_{NN}.

The following schematic diagram shows how this DC/DC converter can be configured. V_{PP}, V_{PF}, V_{NN} and V_{NF} represent all output rails. V_{IN} is the main supply rail to the DC/DC converter.

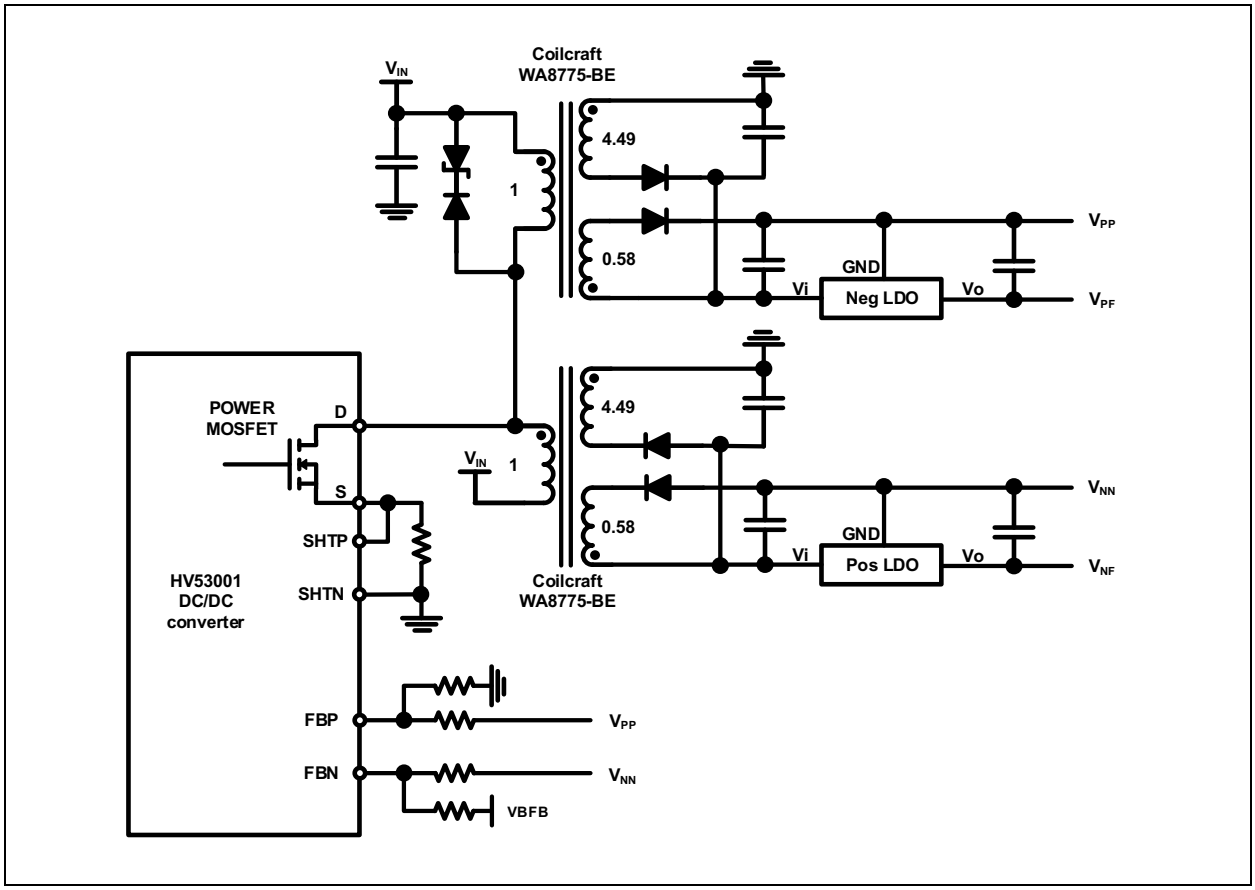


FIGURE 3-10: *HV53001 DC-DC converter configuration*

3.10.1 T_{ON} SETTING

The T_{ON} pin is used to set the duty cycle of the DC-DC converter. An internal ramp generator in the DC-DC converter creates a ramp between 0 and 3.75V. A low-to-high transition starts at 0V. When this ramp voltage reaches the same voltage level presented at the T_{ON} pin, it triggers the internal comparator and sets the pulse high-to-low transition. The voltage present at the T_{ON} pin sets the duty cycle of the pulses.

An internal lower bound and upper bound of the duty cycle are set to avoid any malfunction. The user can select any T_{ON} voltage between 0 and 3V.

For example, the duty cycle is set to 80% for VT_{ON} = 3V.

$$DutyCycle = \frac{VT_{ON}}{3.75}$$

3.10.2 CONVERTER SWITCHING FREQUENCY

The converter switching frequency is set by an external resistor RT. The frequency is set by the following equation.

f_{SW} = 1/ (C * RT) where C = 12pF

3.10.3 OVERVOLTAGE PROTECTION

Overvoltage protection is to monitor the output voltage of the boost converter. If the output voltage of the DC/DC converter reaches above the threshold voltage, it will pause the DC/DC converter operation for safety purpose.

The DC/DC stays in Standby mode until the monitored voltage drops below the threshold. Then, the DC/DC controller exits Standby mode and resumes normal operation.

The overvoltage protection is intended to guard any momentarily overvoltage condition for a short period of time and does not require any user interaction. The threshold voltage can be set by the external resistor network.

The OVPP and OVPN pins are used to monitor the feedback voltage from the V_{PP} and V_{NN} supplies via two sets of voltage divider networks. The sampled voltage from V_{PP} and V_{NN} are compared with the inter-

nal reference voltage. If the sampled V_{PP} or V_{NN} voltage is above the threshold, the controller will turn off the pulses until V_{PP} and V_{NN} drop below the threshold.

3.10.4 SHORT CIRCUIT PROTECTION

A short circuit at the flyback transformer output may cause damage to the power supply circuit and generate a lot of heat. This may create a hazardous situation for the end user. A short circuit protection scheme is implemented in the DC/DC controller by monitoring the current of the power FET transistor.

This DC/DC controller is running in Discontinuous Conduction mode (DCM). When a short circuit situation happens, the converter goes into Continuous Conduction mode (CCM). This causes the FET current at turn on to be non-zero. The controller detects this and shuts down the pulse to the power FET and sets a logic '1' at the SHORT pin. The user toggles the EN signal to restart the converter.

The short circuit protection function can be bypassed by inserting a logic "0" to the short circuit enable pin (SHTEN).

3.11 Driver Output Current Sensing

Some system designs require a load sensing function to determine the size or change of the capacitive load. One simple scheme is to place a series current sensing resistor on the power supply rail and measure the voltage drop across this resistor. This solution is very effective if the voltage drop is small enough not to affect the operation of the system.

The HV53001 driver IC provides this function and the user can monitor the supply current flowing through both high-voltage positive and negative supplies. Two external current sensing resistors are connected to the V_{PP} and V_{NN} supply rails, respectively, as high side current sensing. The voltage drop across these resistors are connected to two pin pairs, V_{PP}-V_{PPO} and V_{NN}-V_{NNO}. Since these voltage drops are referenced to V_{PP} and V_{NN} supply rails, it is not practical for a low-voltage ADC to measure these voltages. Hence, two internal difference amplifiers in the driver IC convert these voltage drops to near ground potential.

The difference amplifier accepts a maximum input voltage of 1V. The amplifier gain of 3.1 amplifies this input and sends the output to the VPPSENSE and VNNSENSE pins. These amplifiers are designed using high-voltage and high value resistors to minimize its power consumption. These amplifier outputs are high impedance in nature, so an external high bandwidth (200MHz) unity gain buffer is highly recommended. The high bandwidth is needed to capture the fast current pulse during the transition.

The user selects the value of the sensing resistor to fit the system requirement. The speed of difference amplifier is a high priority parameter because the charge or discharge current appears for a short period of time. The amplifier output accuracy is less important. Both VPPSENSE and VNNSENSE outputs have a tolerance of ±14%.

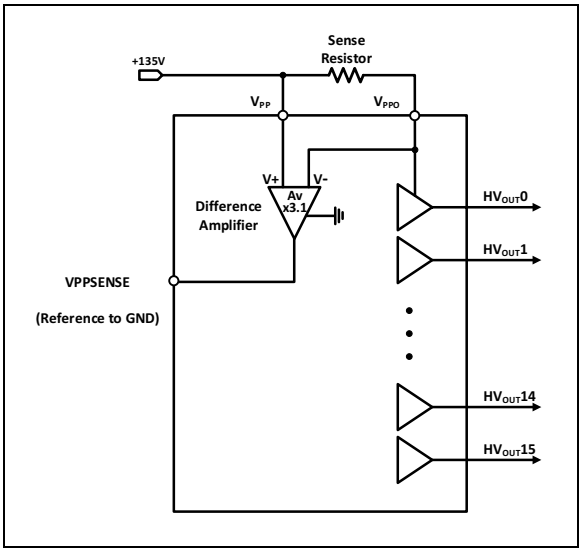
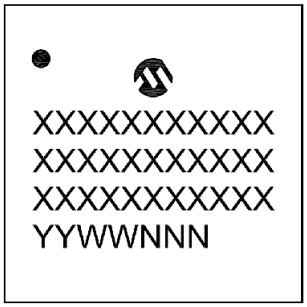


FIGURE 3-11: *Current Sensing Topology.*

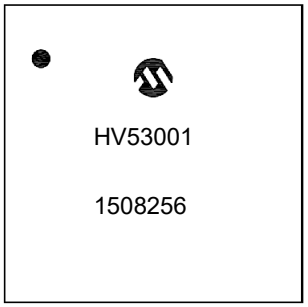
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

105-Ball TFBGA(9x9x1.2 mm)



Example

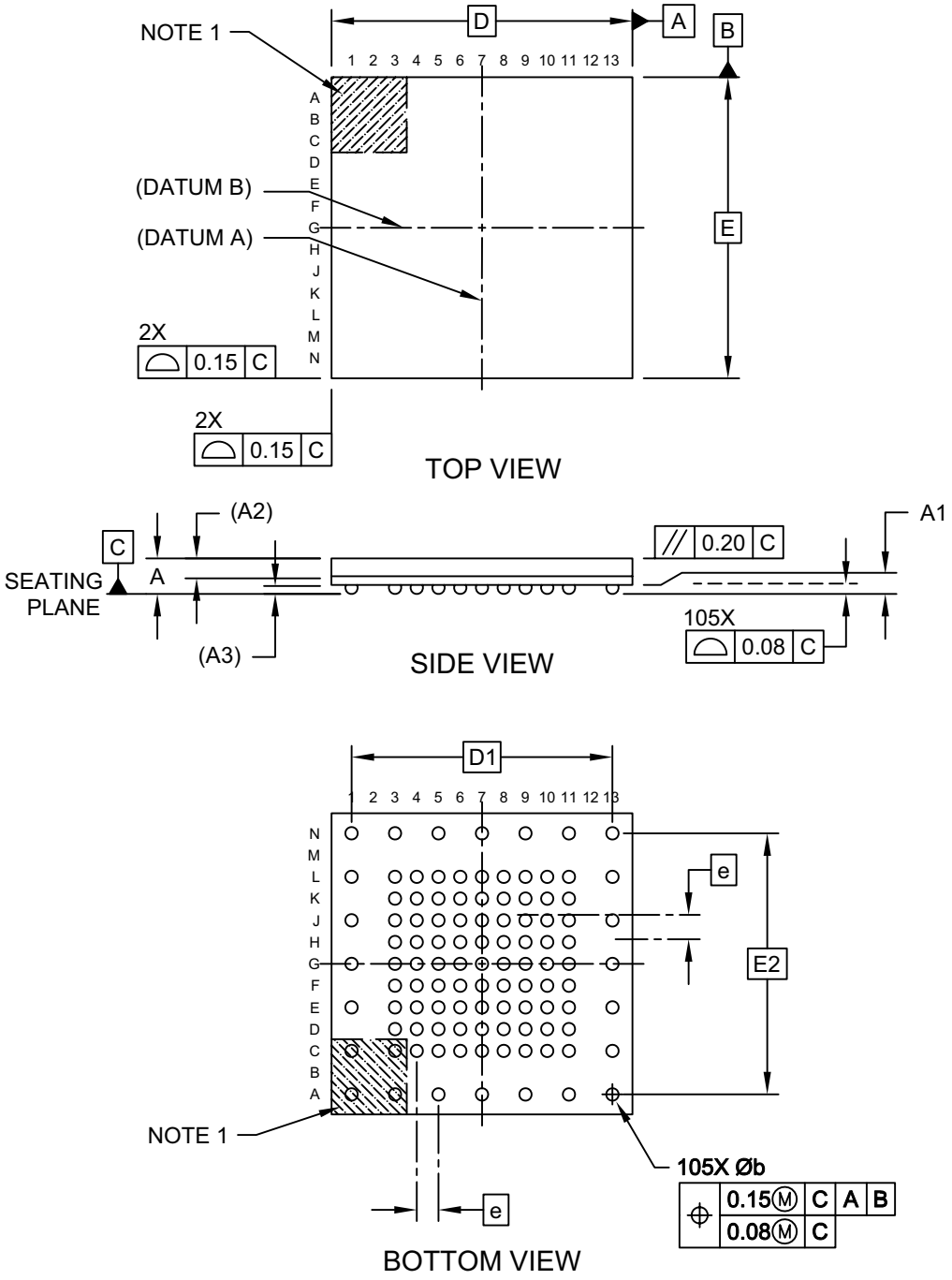


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e8	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e8) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

105-Ball Thin Fine Pitch Ball Grid Array (KWX) - 9x9 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-469 Rev. A Sheet 1 of 2

105-Ball Thin Fine Pitch Ball Grid Array (KWX) - 9x9 mm Body [TFBGA]

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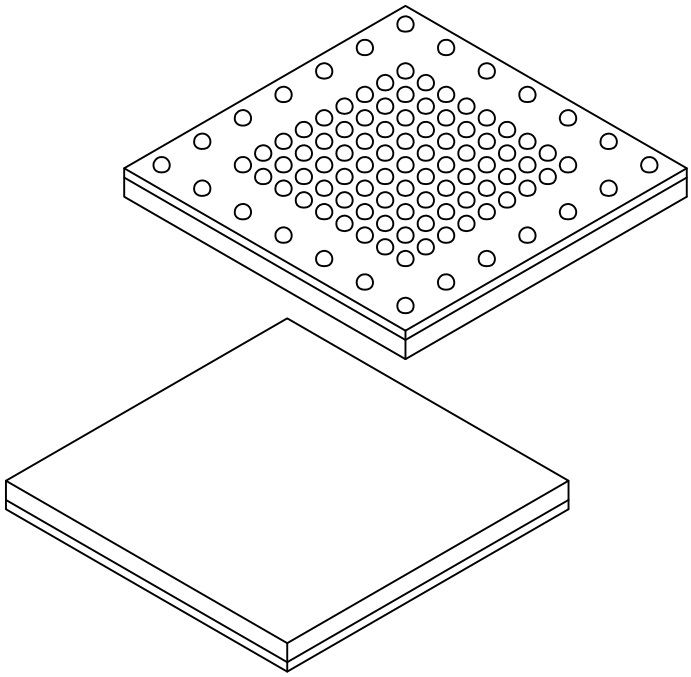


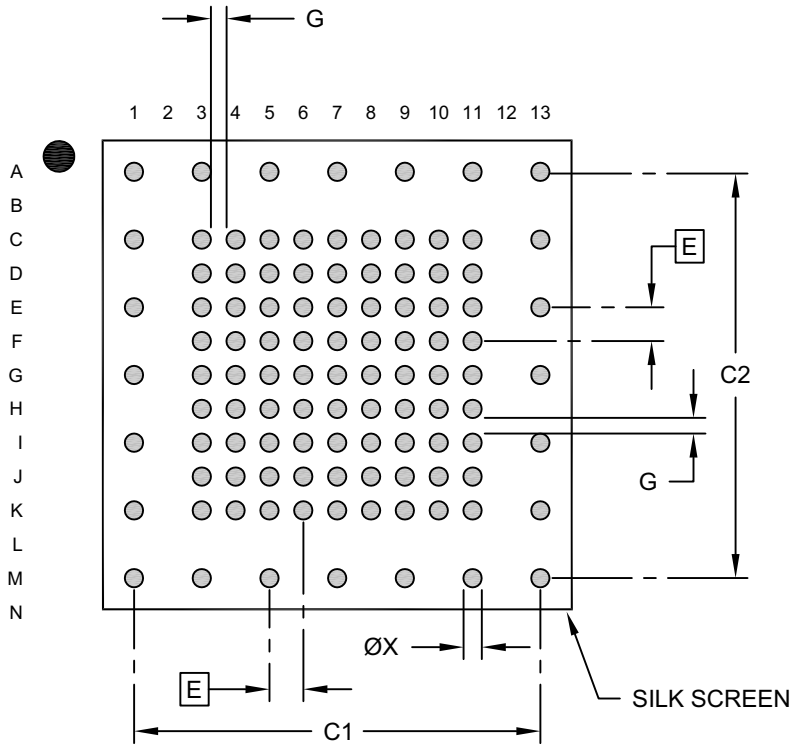
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		105	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.22	0.27	0.32
Mold Thickness	A2		0.53 REF	
Substrate Thickness	A3		0.26 REF	
Overall Length	D		9.00 BSC	
Overall Terminal Spacing	D1		7.80 BSC	
Overall Width	E		9.00 BSC	
Overall Terminal Spacing	E1		7.80 BSC	
Terminal Diameter	b	0.32	0.37	0.42

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-469 Rev. A Sheet 2 of 2

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Overall Contact Pad Spacing	C1		7.80	
Overall Contact Pad Spacing	C2		7.80	
Contact Pad Width (X105)	X			0.35
Contact Pad to Contact Pad	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2469 Rev. A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2021)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X-	X	/XXX
Device	Media Type Tape and Reel	Temperature Range	Package

Device:	HV53001: 16-Channel, +/-135V Push-Pull Driver with RTZ, Current Sensor and Built-in Boost Converter
Media Type:	blank = 260/Tray for KWX Package T = 1000/Reel for KWX Package
Temperature Range:	E =-40°C to +125°C (Extended) RoHS Compliant
Package:	KWX =Thin Fine Pitch Ball Grid Array 105-Ball TFBGA (9 x 9 x 1.2 mm)

Examples:

a) HV53001-E/KWX:16-Channel, ±135V Push-Pull Driver with RTZ, Current Sensor and Built-in Boost Converter. Thin Fine Pitch Ball Grid Array, 105-Ball TFBGA (9 x 9 x 1.2mm) Package, 260/Tray

b) HV53001T-E/KWX:16-Channel, ±135V Push-Pull Driver with RTZ, Current Sensor and Built-in Boost Converter. Thin Fine Pitch Ball Grid Array, 105-Ball TFBGA (9 x 9 x 1.2mm) Package, 1000/Tape & Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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