HV53011

16-Channel ±135V Push-Pull Driver with RTZ

Features

- 16-Channel Push-Pull Output
- Return-To-Zero (RTZ) and High Impedance (Hi-Z) Function
- Up to ±135V Output Voltage
- 24 mA Minimum Source Sink Output Current
- 250 pF Maximum Output Load
- Current Sensor Output
- SPI Interface with Quad-Latched 2-Bit per Channel Architecture
- Power-On Reset Function
- Shutdown Function
- 59-Ball 8 x 8 mm TFBGA Package

Application

- Surface Haptic Application
- MEMS Driver
- Piezo Driver

General Description

HV53011 is a high-voltage driver solution for surface haptic applications. It consists of 16 push-pull drivers capable of ±135V output swing with Return-To-Zero (RTZ) function. Each output driver is capable of sourcing and sinking at least 24 mA. Each high-voltage output is capable of driving up to 250 pF capacitive load. A global current sensor function is also integrated into this device to monitor the charge and discharge currents. The measured current is mapped to a low voltage analog output with a scale factor of 3.1 V/V via a current-sensing resistor.

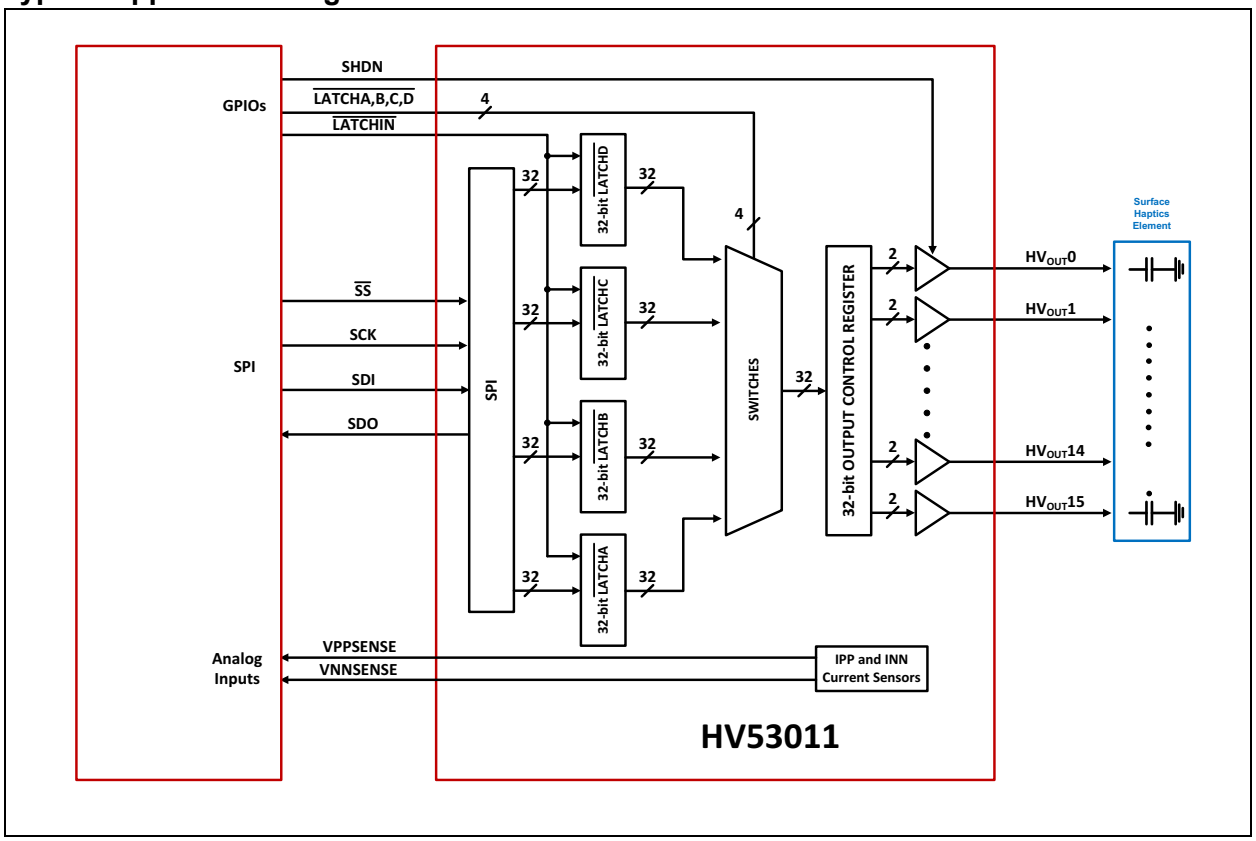
An SPI interface is used to communicate between the microcontroller/processor and the high-voltage drivers. This interface accepts 3.3V logic I/O signals up to clock speeds of 32 MHz. Five digital LATCH control signals manage the data flow and the firing pattern. It establishes the output to one of four possible states: V_{PP}, V_{NN}, 0V or high impedance.

A proper power on and off sequence is critical to ensure the operation of the high-voltage driver. This driver requires four high-voltage power rails, V_{PP}, V_{PF}, V_{NN}, V_{NF}, and three low-voltage power rails, V_{CC}, V_{SS} and V_{LL}. A companion integrated driver IC, HV53001, has a built-in power on/off sequence control circuits to maintain the proper orders.

A shutdown function is available to disable the driver and set it to consume minimum power when the driver is not used.

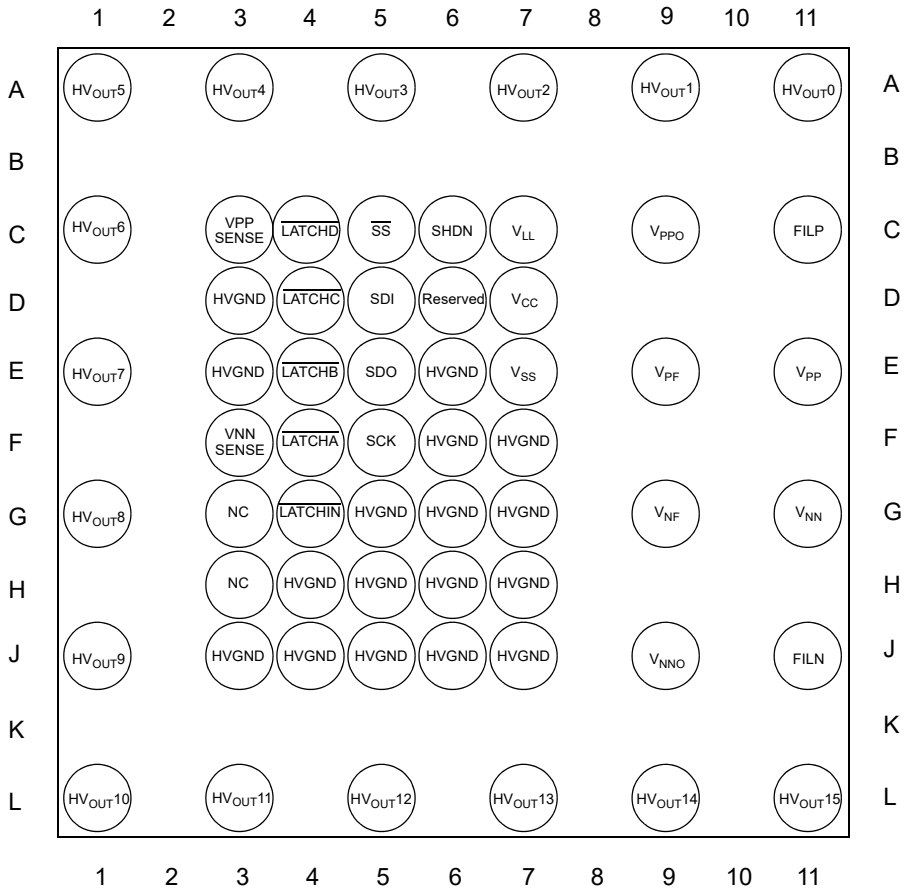
The HV53011 device is packaged in a 8 x 8 mm 59-ball TFBGA package. All high-voltage I/Os are assigned to have sufficient clearance for safety purposes.

Typical Application Diagram



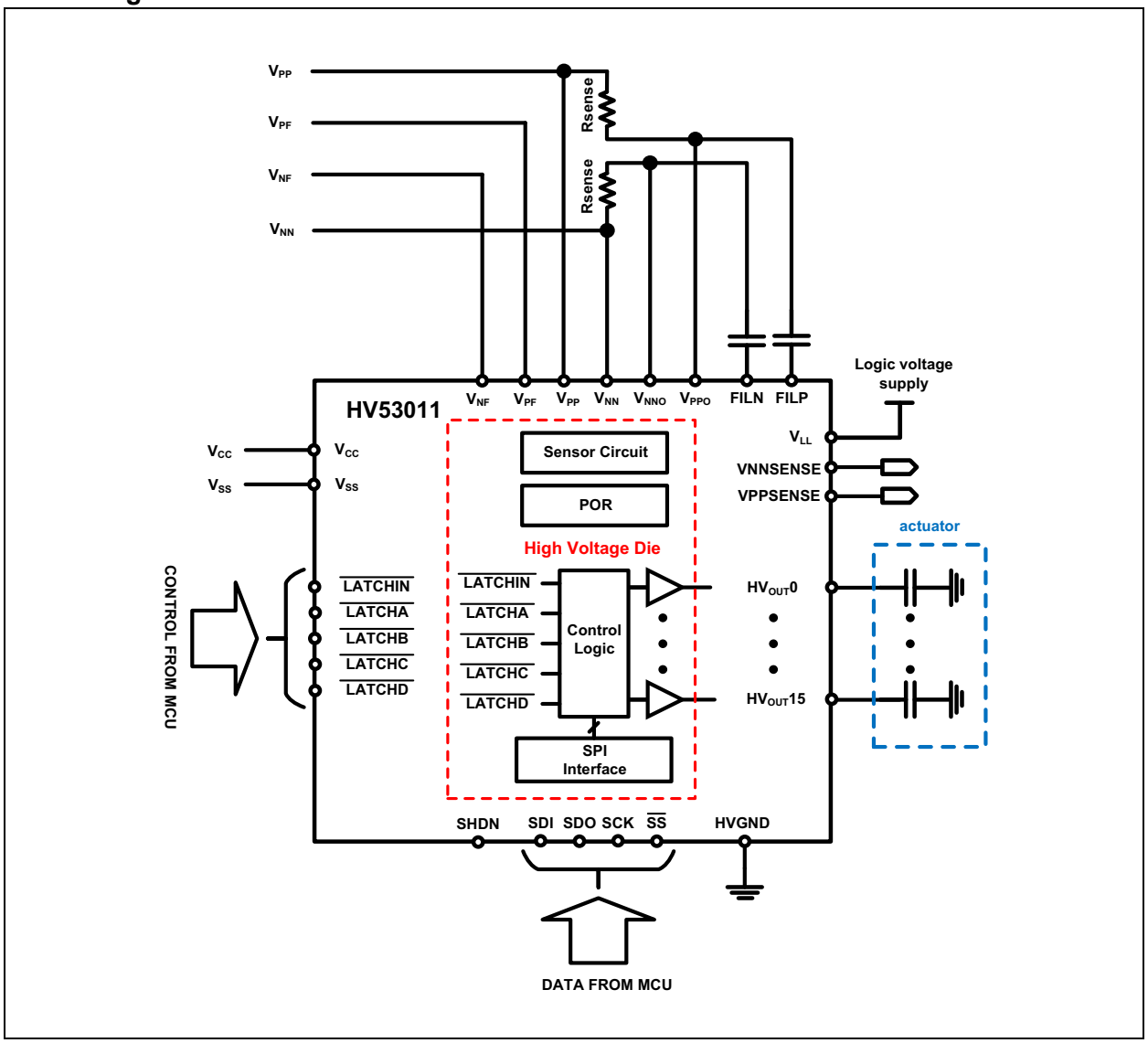
Package Types (Top View)

HV53011
8 x 8 TFBGA*



* see Table 2-1.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

High Positive Supply Voltage (V_{PP}) ..... -0.3V to +140V
High Negative Supply Voltage (V_{NN}) ..... -140V to +0.3V
High Positive Floating Supply Voltage (V_{PF}) ..... V_{PP} - 14V to V_{PP}
High Negative Floating Supply Voltage (V_{NF}) ..... V_{NN} to V_{NN} + 14V
Analog Low Positive Voltage Supply (V_{CC}) ..... -0.3V to +8.0V
Analog Low Negative Voltage Supply (V_{SS}) ..... -8.0V to +0.3V
Logic Voltage Supply (V_{LL}) ..... -0.3V to +4.0V
Logic Input Levels (Hi-V Driver, SPI interface, $\overline{\text{LATCHx}}$ and SHDN) ..... -0.3V to V_{LL} +0.3V
Maximum Junction Temperature ($T_{J(MAX)}$) ..... +125°C
Storage Temperature ..... -65°C to +150°C
ESD Rating on Low Voltage Pins (Human Body Model) ..... 2 kV
ESD Rating on Low Voltage Pins (Charged Device Model) ..... 500 V
ESD Rating on High Voltage Pins (Human Body Model) ..... 500 V
ESD Rating on High Voltage Pins (Charged Device Model) ..... 500 V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: OPERATING SUPPLY VOLTAGES

Electrical Specifications: Unless otherwise specified: $T_A = T_J$ = +25°C. **Boldface** specifications apply over the $T_A = T_J$ = range of -40°C to +125°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
High Positive Supply Voltage	V_{PP}	**48**		**135**	V	**Note 1**
High Negative Supply Voltage	V_{NN}	**-135**		**-48**	V	
Low Positive Supply Voltage (High Voltage Driver)	V_{CC}	**6.0**	**6.5**	**7.0**	V	
Low Negative Supply Voltage (High Voltage Driver)	V_{SS}	**-6.5**	**-6.0**	**-5.5**	V	
Logic Input Supply Voltage (SPI Interface)	V_{LL}	**3.0**	**3.3**	**3.6**	V	
Negative Floating Supply Voltage	V_{NF}	**V_{NN} + 9V**	**-**	**V_{NN}+13.2V**	V	
Positive Floating Supply Voltage	V_{PF}	**V_{PP}-13.2V**	**-**	**V_{PP} - 9V**	V	
High-Level Input Logic Voltage	V_{IH}	**0.8 V_{LL}**			V	
Low-Level Input Logic Voltage	V_{IL}	**0**		**0.2 V_{LL}**	V	

Note 1: Specification is obtained by characterization and is not 100% tested.

TABLE 1-2: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all limits apply for $T_A = T_J = 25°C$; **Boldface** specifications apply over the full operating temperature range of $T_A = T_J = -40°C$ to 125°C. Typical values are at +25°C. V_{PP} = +135V, V_{NN} = -135V, V_{PF} = +123V, V_{NF} = -123V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{LL} = +3.3V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
High Voltage Driver						
Quiescent V_{PP} Supply Current (Sum of Current at V_{PP} and V_{PPO} pins)	$I_{PP}Q$		**3.7**	**5.6**	mA	
Quiescent V_{NN} Supply Current (Sum of Current at V_{NN} and V_{NNO} pins)	$I_{NN}Q$	**-5.8**	**-3.8**		mA	
Quiescent V_{PF} Supply Current (Source)	$I_{PF}Q$	**-5.2**	**-3.6**		mA	
Quiescent V_{NF} Supply Current (Source)	$I_{NF}Q$		**3.7**	**5.4**	mA	
Quiescent High Voltage Positive Supply Resultant Current, $I_{PP}Q + I_{PF}Q$	$I_{PPR}Q$			**0.4**	mA	
Quiescent High Voltage Negative Supply Resultant Current, $I_{NN}Q + I_{NF}Q$	$I_{NNR}Q$	**-0.4**			mA	
V_{PP} Supply Current (Sum of current at V_{PP} and V_{PPO} pins)	I_{PP}			**7.5**	mA	V_{PP}=+90V, V_{NN}=-90V, V_{PF}=+78V, V_{NF}=-78V, f_{HVOUT} = 20 kHz,CL= 250 pF, Running two channels. Test pattern = Figure 1-3 with 12.5 µs pulse width
V_{NN} Supply Current (Sum of current at V_{NN} and V_{NNO} pins)	I_{NN}	**-7.5**			mA	
High Voltage Positive Supply Resultant Current, $I_{PP} + I_{PF}$	I_{PPR}			**2**	mA	V_{PP}=+90V, V_{NN}=-90V, V_{PF}=+78V, V_{NF}=-78V, f_{HVOUT} = 20 kHz,C_L= 250 pF, Running two channels. Test pattern = Figure 1-3 with 12.5 µs pulse width
High Voltage Negative Supply Resultant Current, $I_{NN} + I_{NF}$	I_{NNR}	**-2**			mA	
V_{PF} Operating Supply Current	I_{PF}	**-5.5**			mA	V_{PP} = +90V, V_{NN}= -90V, V_{PF}= + 78V, V_{NF}= -78V, f_{HVOUT} = 20 kHz, C_L= 250 pF, Running two channels. Test pattern = Figure 1-3 with 12.5 µs pulse width
V_{NF} Operating Supply Current	I_{NF}			**5.5**	mA	

Note 1: Recommended operating conditions: V_{LL} = +3.3V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{PP} = +135V, V_{NN} = -135V all input pins = 0V unless noted. T_J = 25°.C

2: Design guidance only.

3: Specification is obtained by characterization and is not 100% tested.

TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits apply for $T_A = T_J = 25°C$; **Boldface** specifications apply over the full operating temperature range of $T_A = T_J = -40°C$ to 125°C. Typical values are at +25°C. V_{PP} = +135V, V_{NN} = -135V, V_{PF} = +123V, V_{NF} = -123V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{LL} = +3.3V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
V_{CC} Operating Supply Current	I_{CC}			**0.2**	mA	V_{PP}=+90V, V_{NN}=-90V, V_{PF}=+78V, V_{NF}=-78V, Test pattern = Figure 1-3 with 12.5 µs pulse width
V_{SS} Operating Supply Current	I_{SS}	**-0.2**			mA	
V_{LL} Operating Supply Current	I_{LL}			**25**	mA	V_{LL} = +3.3V SCK = 32 MHz, SDI = 16 MHz pulse train
V_{NF} Negative Floating Supply Voltage	V_{NF}	**V_{NN}+9V**	-	**V_{NN}+13.2V**	V	
V_{PF} Positive Floating Supply Voltage	V_{PF}	**V_{PP}-13.2V**	-	**V_{PP}-9V**	V	
HV_{OUT} Switching Frequency	f_{HVOUT}	**0**		**25**	kHz	V_{PP} = +90V, V_{NN}= -90V, V_{PF} = +78V, V_{NF}= -78V, C_L= 250 pF, Test pattern = Figure 1-3 with 12.5 µs pulse width
HV_{OUT} Output Source and Sink Current	I_{HVOUT}	**24**			mA	V_{PP} = +90V, V_{NN} = -90V, V_{PF}= +78V, V_{NF} = -78V
Return-To-Zero Slew Rate 90% to 10% (i) from V_{PP} to 0V (ii) from V_{NN} to 0V	SR	**40**	**100**	**200**	V/µs	V_{PP} = +90V,V_{NN} = -90V, V_{PF}= +78V,V_{NF} = -78V, V_{CC}= +6.5V,V_{SS}= -6.0V C_L = 250 pF
Delay Time for Output to Start Rise/Fall (from $\overline{LATCH}$A, B, C, D to 1V HV_{OUT})	$t_{d(ON/OFF)}$			100	ns	V_{PP} = +135 V, V_{NN} = -135 V, V_{CC}= 6.5V, V_{SS} = -6.0V No load (**Note 3**)
Variation of Delay Time (Channel to Channel)	Δt_d			40	ns	**Note 3**
Shutdown Pin Input Enable Voltage	$V_{IH(SHDN)}$	2.5			V	
VPPSENSE and VNNSENSE Current Sensor						

Note 1: Recommended operating conditions: V_{LL} = +3.3V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{PP} = +135V, V_{NN} = -135V all input pins = 0V unless noted. T_J = 25°.C

2: Design guidance only.

3: Specification is obtained by characterization and is not 100% tested.

TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits apply for $T_A = T_J = 25°C$; **Boldface** specifications apply over the full operating temperature range of $T_A = T_J = -40°C$ to 125°C. Typical values are at +25°C. V_{PP} = +135V, V_{NN} = -135V, V_{PF} = +123V, V_{NF} = -123V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{LL} = +3.3V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
VPPSENSE/VNNSENSE Output Voltage	V_{out} (VPPSENSE/ VNNSENSE)	**0**		**3.6**	V	V_{PP} = +135V, V_{NN} = -135V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{PP} - V_{PPO} = 1.0V, V_{NNO} - V_{NN} = 1.0V
Voltage Gain of Current Sensor	AV_{SENSE}	**-14%**	**3.1**	**+14%**	V/V	V_{PP} = +135V, V_{NN} = -135V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{PP}-V_{PPO} and V_{NNO}-V_{NN}: from 0.1 to 1.0V
Sensing Amplifier Output Offset	V_{OS}	**-280**		**+280**	mV	V_{PP} = +135V, V_{NN} = -135V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{PP}-V_{PPO} and V_{NNO}-V_{NN}: from 0.1 to 1.0V
Rise Time (Time from 10% to 90% of targeted value)	t_R			300	ns	(**Note 3**) V_{PP} = +90V, V_{NN} = -90V, V_{CC} = +6.5V, V_{SS} = -6.0V, C_L = 3 pF, Test pulse: 1V, 1 µs pulse width 1. V_{PP} and V_{PPO} 2. V_{NN} and V_{NNO}
				740	ns	V_{PP} = +90V, V_{NN} = -90V, V_{CC} = +6.5V, V_{SS} = -6.0V, C_L = 20 pF, Test pulse: 1V, 1 µs pulse width 1. V_{PP} and V_{PPO} 2. V_{NN} and V_{NNO}
VPPSENSE/VNNSENSE Output Load	R_{LOAD}	10			MΩ	**Note 2**
	C_{LOAD}			3	pF	**Note 2**
SPI Interface						
Digital Input Clock Frequency	f_{CLK}			**32**	MHz	3.3V logic input
High-Level Input Logic Voltage	V_{IH}	**0.8V_{LL}**			V	
Low-Level Input Logic Voltage	V_{IL}	**0**		**0.2V_{LL}**	V	
Logic I/O Pin Rise and Fall Time	t_R, t_F			5	ns	C_L = 15 pF (**Note 3**)

Note 1: Recommended operating conditions: V_{LL} = +3.3V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{PP} = +135V, V_{NN} = -135V all input pins = 0V unless noted. T_J = 25°.C

2: Design guidance only.

3: Specification is obtained by characterization and is not 100% tested.

TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits apply for $T_A = T_J = 25°C$; **Boldface** specifications apply over the full operating temperature range of $T_A = T_J = -40°C$ to 125°C. Typical values are at +25°C. V_{PP} = +135V, V_{NN} = -135V, V_{PF} = +123V, V_{NF} = -123V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{LL} = +3.3V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Sourced by any standard I/O pin	Isource	**10**			mA	**Note 2**
Sunk by any standard I/O pin	Isink	**10**			mA	**Note 2**
SPI Quiescent Current of Low Voltage Supplies with Shut-down asserted	$I_{LL}Q$			100	µA	In shutdown mode. All logic input = 0V. $V_{(SHDN)} = V_{LL}$
Time to Enter and Exit Shutdown	t_{SHDN}			1	ms	SCK = 32 MHz and SDI = 16 MHz pulse train.
Time from Chip Select and SPI data	t_{WAIT}	20	50	-	ns	Refer to **Figure 1-1** **(Note 2)**
Time to Transfer 128 Bits of Data	t_{PKT}	4	-	-	µs	Refer to **Figure 1-1** **(Note 2)**
Time from Last Clock Pulse to $\overline{\text{LATCHIN}}$	$t_{H(LAT)}$	20	50	-	ns	Refer to **Figure 1-1** **(Note 2)**
Digital Interface						
Time SPI Latch Held Low	t_{ab}	20	50	-	ns	Refer to **Figure 1-2** **(Note 2)**
Time Between SPI Latches	t_{ac}	10	12	-	µs	Refer to **Figure 1-2** **(Note 2)**
Time from SPI Latch Assert to Data Valid	t_{ae}	-	10	20	ns	Refer to **Figure 1-2** **(Note 2)**
Time from SPI Latch to Data Latch	t_{ak}	20	50	-	ns	Refer to **Figure 1-2** **(Note 2)**
Time Latch Signal Held High	t_{gk}	20	50	-	ns	Refer to **Figure 1-2** **(Note 2)**
Time Latch Signal Held Low	t_{mn}	20	50	-	ns	Refer to **Figure 1-2** **(Note 2)**
Time Between Two Data Latch Events	t_{rs}	80	100	-	ns	Refer to **Figure 1-2** **(Note 2)**
Propagation Delay from Data Register to Output Register	t_{kv}	-	10	20	ns	Refer to **Figure 1-2** **(Note 2)**

Note 1: Recommended operating conditions: V_{LL} = +3.3V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{PP} = +135V, V_{NN} = -135V all input pins = 0V unless noted. $T_J = 25°.C$

2: Design guidance only.

3: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: V_{PP} = +135V, V_{NN} = -135V, V_{PF} = +123V, V_{NF} = -123V, V_{CC} = +6.5V, V_{SS} = -6.0V, V_{LL} = +3.3V unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistance						
Thermal Resistance, 59B 8x8 TFBGA	θ_{JA}	—	33.7	—	°C/W	

1.1 Timing Diagrams

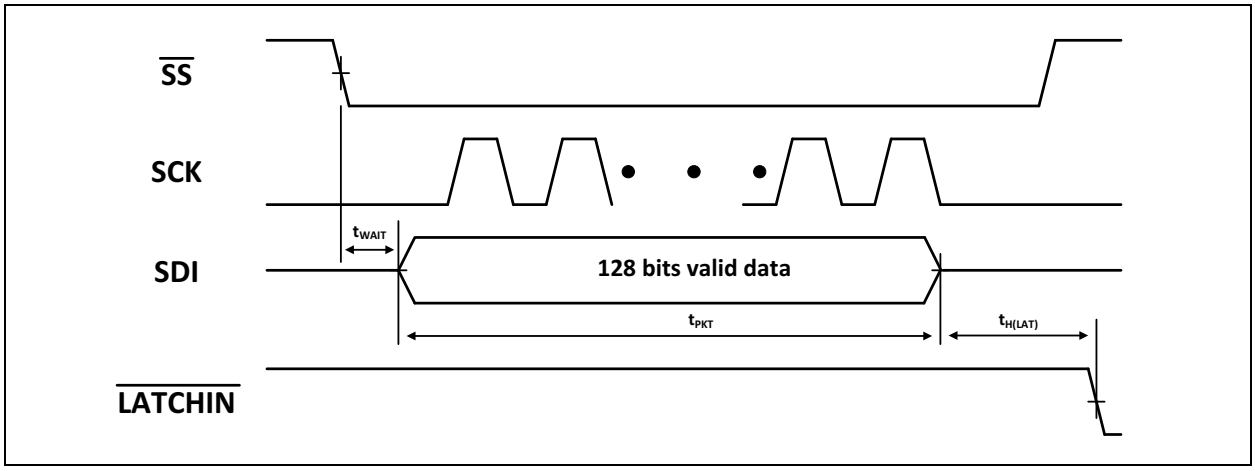


FIGURE 1-1: *SPI and LATCHIN Timing Diagram.*

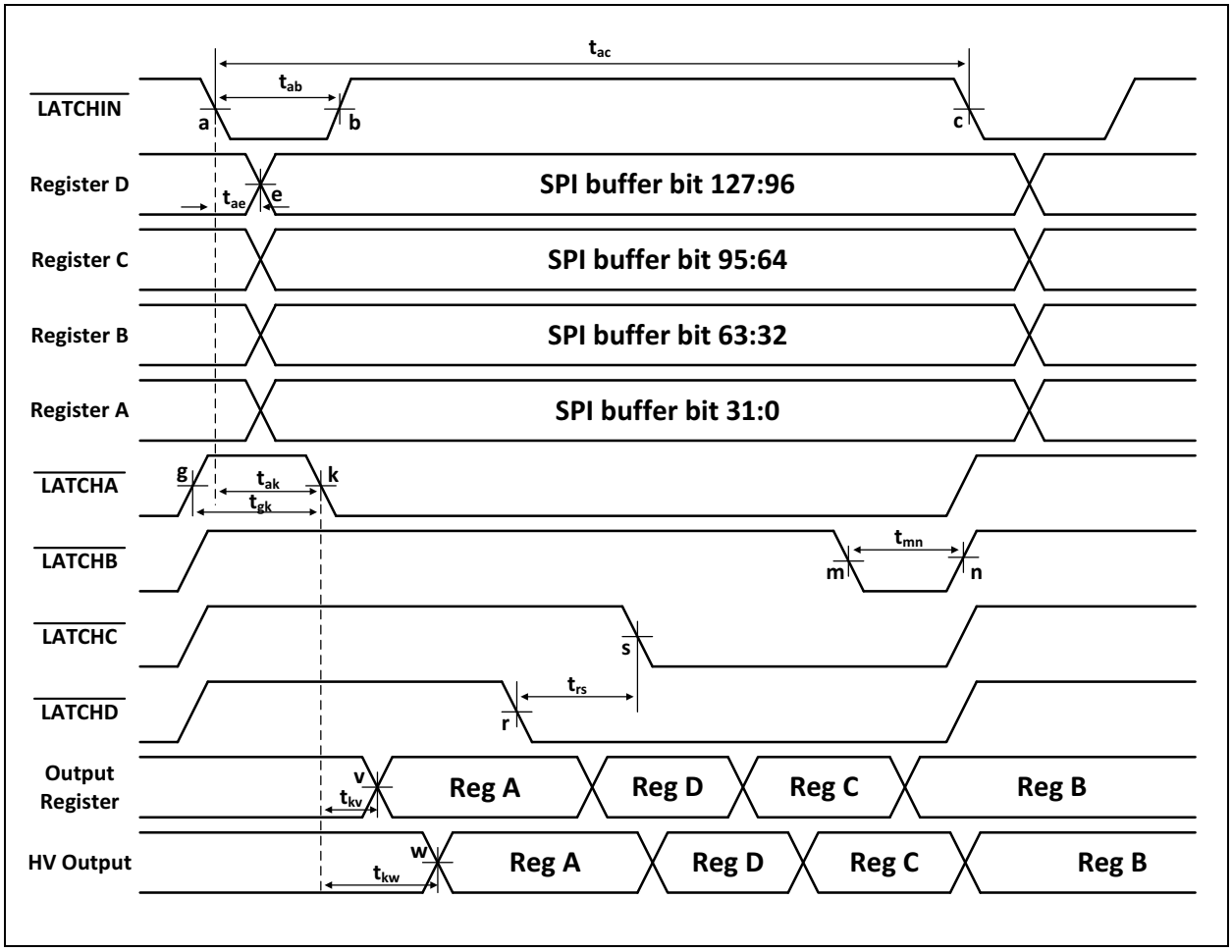


FIGURE 1-2: *LATCHA, B, C, D and High Voltage Output Timing Diagram.*

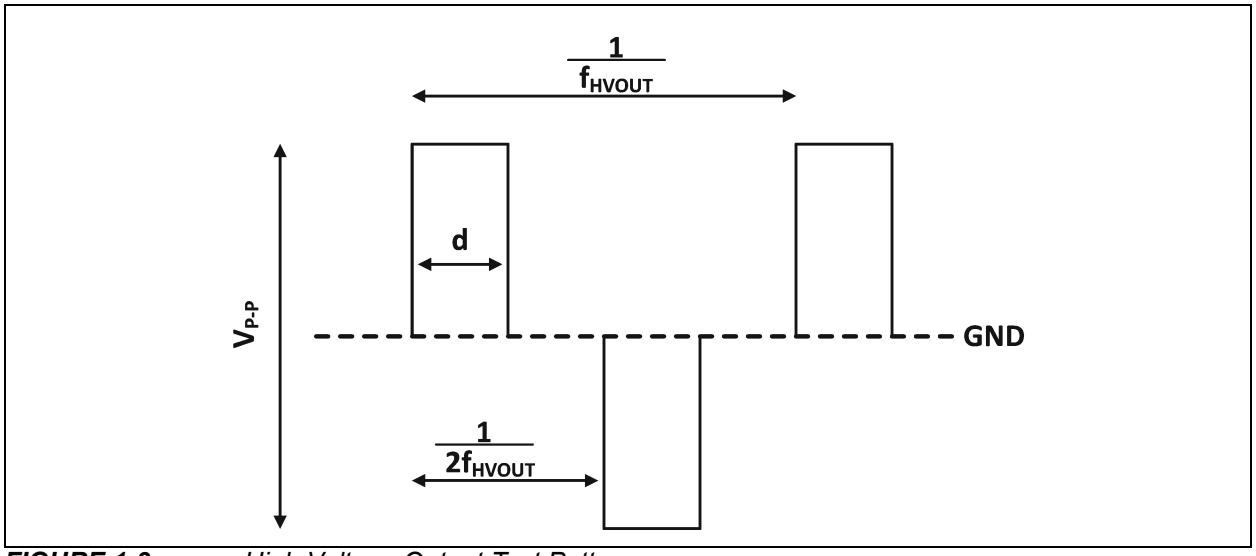


FIGURE 1-3: *High Voltage Output Test Pattern.*

1.2 Typical Performance Curves

Note: The graphs and tables provided below are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

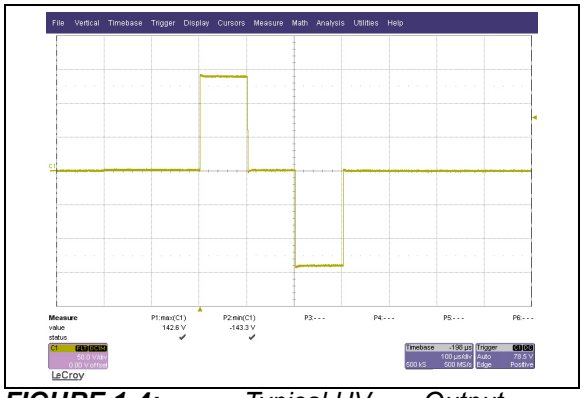


FIGURE 1-4: *Typical HV_{OUT} Output Waveform V_{PP}=135V, V_{NN}=-135V, Load = 100 pF.*

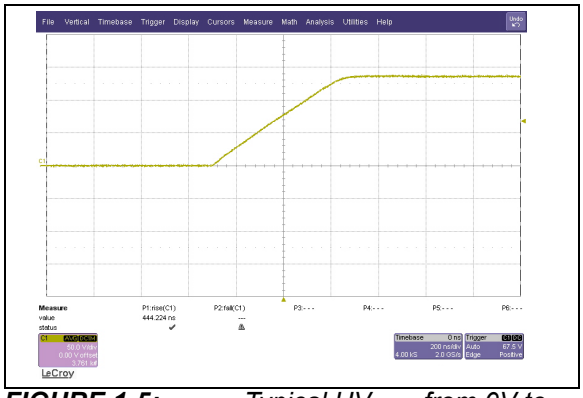


FIGURE 1-5: *Typical HV_{OUT} from 0V to 135V, Load = 100 pF*

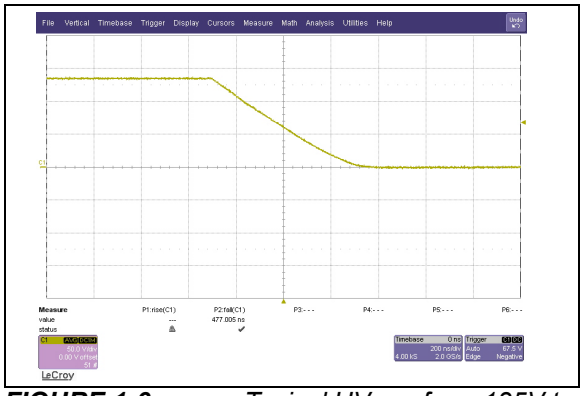


FIGURE 1-6: *Typical HV_{OUT} from 135V to 0V, Load = 100 pF.*

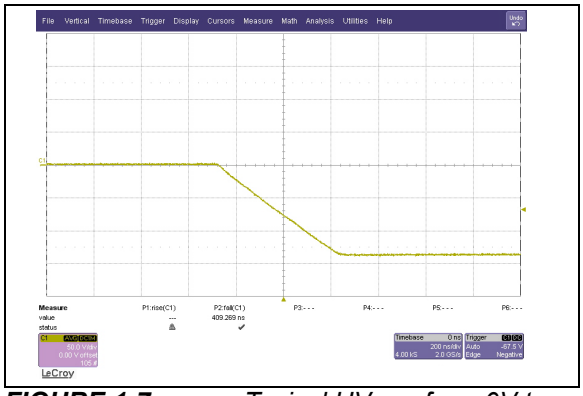


FIGURE 1-7: *Typical HV_{OUT} from 0V to -135V, Load = 100 pF.*

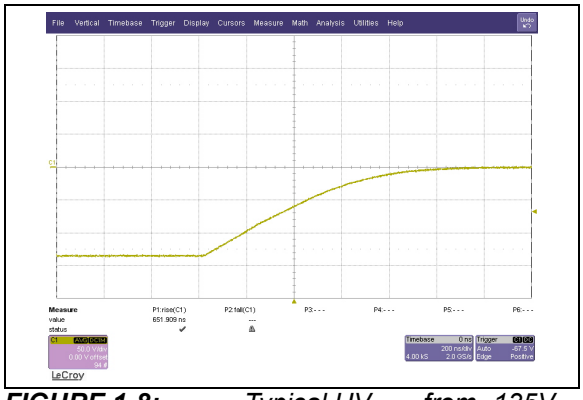


FIGURE 1-8: *Typical HV_{OUT} from -135V to 0V, Load = 100 pF.*

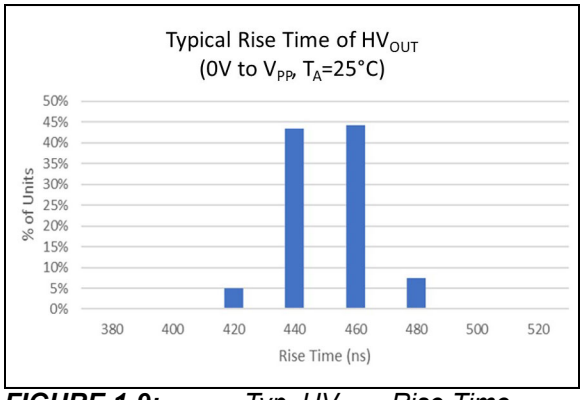


FIGURE 1-9: *Typ. HV_{OUT} Rise Time Distribution, from 0V to 90V, Load = 250 pF.*

Note: The graphs and tables provided below are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

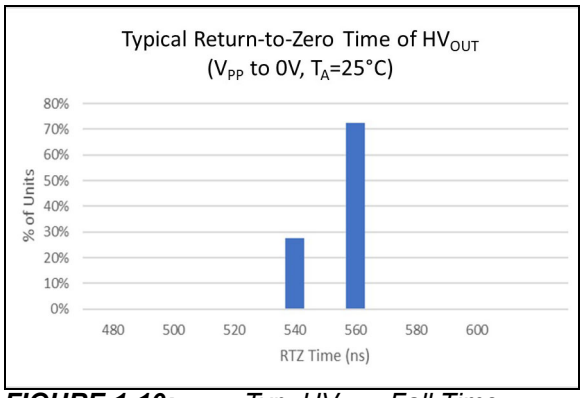


FIGURE 1-10: *Typ. HV_{OUT} Fall Time Distribution, from 90V to 0V, Load = 250 pF.*

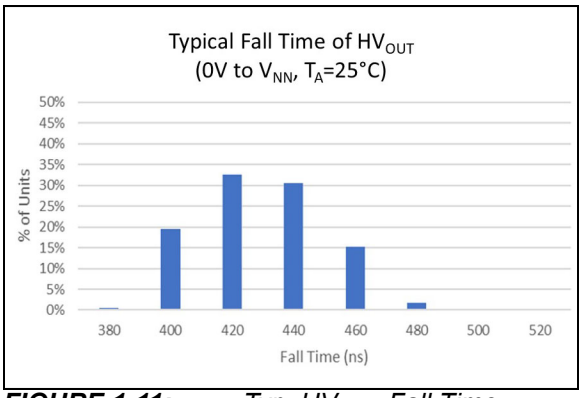


FIGURE 1-11: *Typ. HV_{OUT} Fall Time Distribution, from 0V to -90V, Load = 250 pF.*

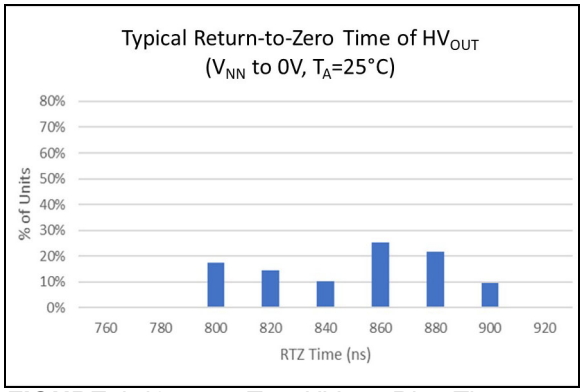


FIGURE 1-12: *Typ. HV_{OUT} Rise Time Distribution, from -90V to 0V, Load = 250 pF.*

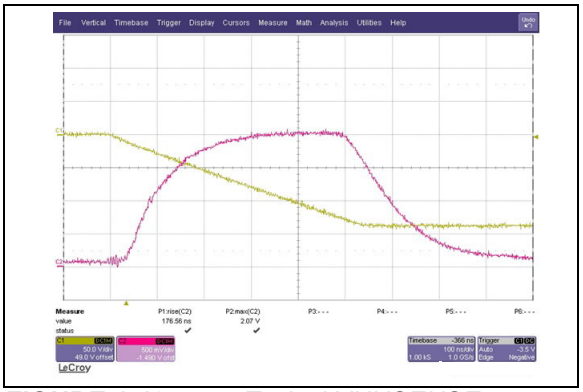


FIGURE 1-13: *Typical VNNSENSE Buffered Output, V_{PP}=135V, V_{NN}=-135V, Load=100pF, 6.04 ohm sense resistor, four channels active.*

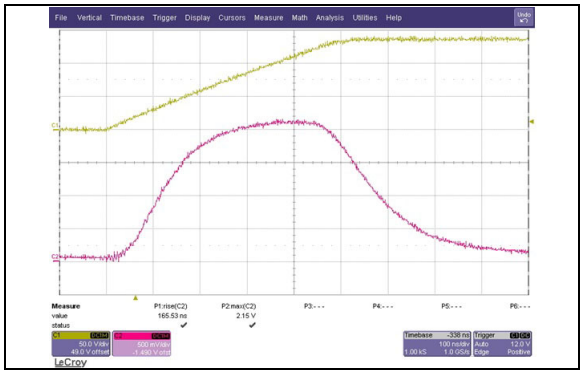


FIGURE 1-14: *Typical VPPSENSE buffered output, V_{PP} = 135V, V_{NN} = -135V, Load=100 pF, 6.04 ohm sense resistor, four channels active.*

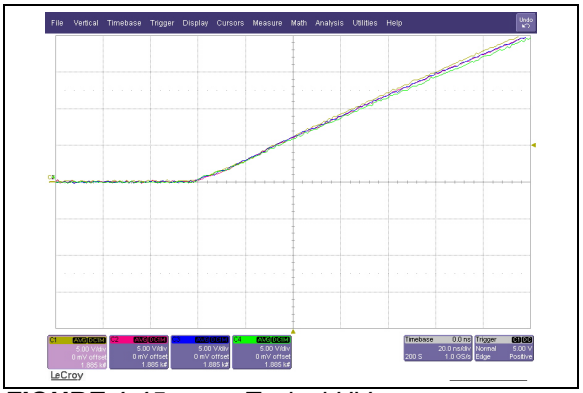


FIGURE 1-15: *Typical HV_{OUT} Channel-to-Channel Delay.*

Note: The graphs and tables provided below are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

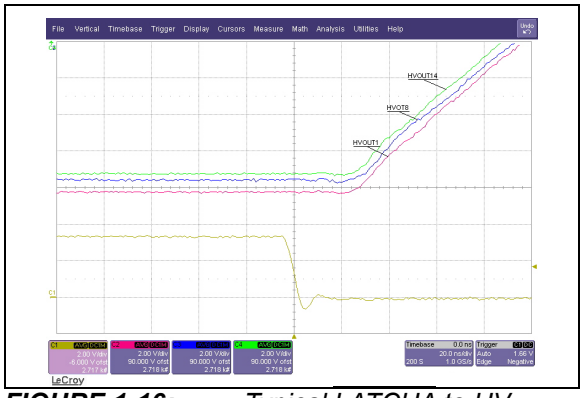


FIGURE 1-16: *Typical LATCHA to HV_{OUT} Propagation Delay*

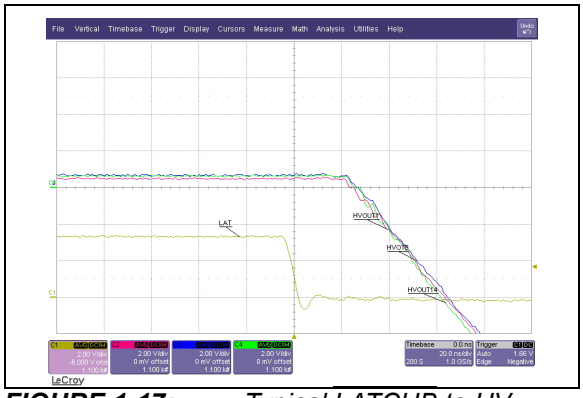


FIGURE 1-17: *Typical LATCHB to HV_{OUT} Propagation Delay*

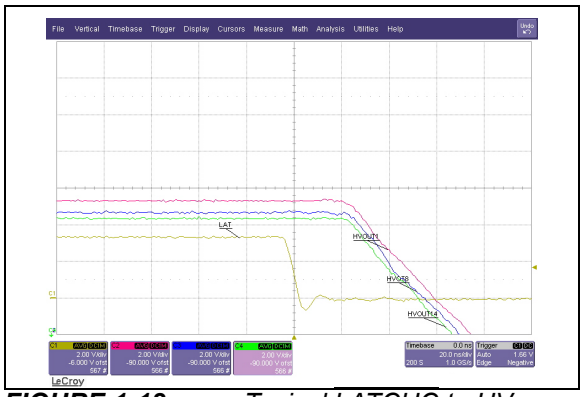


FIGURE 1-18: *Typical LATCHC to HV_{OUT} Propagation Delay*

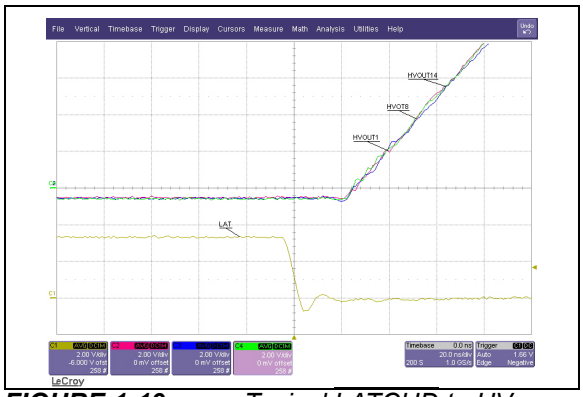


FIGURE 1-19: *Typical LATCHD to HV_{OUT} Propagation Delay*

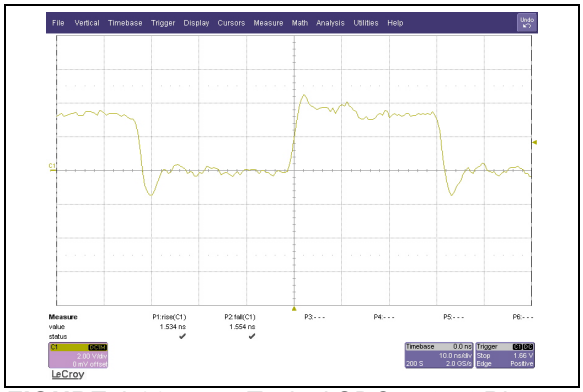


FIGURE 1-20: *Typical SDO output Rise Time and Fall Time*

2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin	Symbol	Description
E11	V_{PP}	Positive High-Voltage Supply
C9	V_{PPO}	Positive High-Voltage Current Sense
G11	V_{NN}	Negative High-Voltage Supply
J9	V_{NNO}	Negative High-Voltage Current Sense
D7	V_{CC}	Positive Low-Voltage Supply
E7	V_{SS}	Negative Low-Voltage Supply
C7	V_{LL}	VLL Logic Voltage
J3-7, H4-7,G5-7, F6-7, E6, D3, E3	HVGND	High-Voltage Ground
E9	V_{PF}	Positive floating voltage supply reference to V_{PP} level
G9	V_{NF}	Negative floating voltage supply reference to V_{NN} level
J11	FILN	0.1 µF Capacitor across FILN and VNNO
C11	FILP	0.1 µF Capacitor across FILP and VPPO
C3	VPPSENSE	Positive High-Voltage Sense Analog Output
F3	VNNSENSE	Negative High-Voltage Sense Analog Output
G3	NC	No connection (Do not connect. Keep the pin floating.)
H3	NC	No connection (Do not connect. Keep the pin floating.)
A11	$HV_{OUT}0$	High-Voltage Output 0
A9	$HV_{OUT}1$	High-Voltage Output 1
A7	$HV_{OUT}2$	High-Voltage Output 2
A5	$HV_{OUT}3$	High-Voltage Output 3
A3	$HV_{OUT}4$	High-Voltage Output 4
A1	$HV_{OUT}5$	High-Voltage Output 5
C1	$HV_{OUT}6$	High-Voltage Output 6
E1	$HV_{OUT}7$	High-Voltage Output 7
G1	$HV_{OUT}8$	High-Voltage Output 8
J1	$HV_{OUT}9$	High-Voltage Output 9
L1	$HV_{OUT}10$	High-Voltage Output 10
L3	$HV_{OUT}11$	High-Voltage Output 11
L5	$HV_{OUT}12$	High-Voltage Output 12
L7	$HV_{OUT}13$	High-Voltage Output 13
L9	$HV_{OUT}14$	High-Voltage Output 14
L11	$HV_{OUT}15$	High-Voltage Output 15
C5	$\overline{SS}$	SPI Chip Select
D5	SDI	SPI Data In
E5	SDO	SPI Data Out (for daisy chain)
F5	SCK	SPI Clock
G4	$\overline{LATCHIN}$	Latch SPI Data (SPI -> Latch A, B, C, D)
F4	$\overline{LATCHA}$	Latch A -> Output Register
E4	$\overline{LATCHB}$	Latch B -> Output Register
D4	$\overline{LATCHC}$	Latch C -> Output Register
C4	$\overline{LATCHD}$	Latch D -> Output Register

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin	Symbol	Description
C6	SHDN	Shutdown Mode
D6	Reserved	Reserved Pin. Connect to Ground.

3.0 DEVICE DESCRIPTION

3.1 Serial Peripheral Interface

The SPI interface is used to transfer data of the channel settings from the microcontroller to the high-voltage driver. The HV53011 operates as an SPI slave device and receives 128 bits of data from the master device (microcontroller). The HV53011 SPI interface is designed to be compatible with all Microchip 8-bit, 16-bit and 32-bit SPI data transmission formats. This SPI interface has a 128-bit shift register buffer to store 128 bits of data.

The $\overline{SS}$ pin is a chip select function which is similar to the enable function to guard the clock and data input signal. The SCK contains the bus clock signal from the microcontroller or host processor. The SDI and SDO are the data input and data output pins of the SPI shift register buffer.

The SDI and SDO can be used to cascade multiple HV53011 or HV53011 drivers together if only a single SPI port is available. This SPI interface is compatible with 3.3V logic input voltage with a maximum clock frequency of 32 MHz.

The SPI shift register captures the data at the SDI input in the rising edge of the SCK clock and pushes out the data from the buffer to the SDO output in the falling edge of the SCK clock. When the SPI bus is at idle status, the $\overline{SS}$ pin stays in logic "1" and the SCK clock is expected to stay at "0".

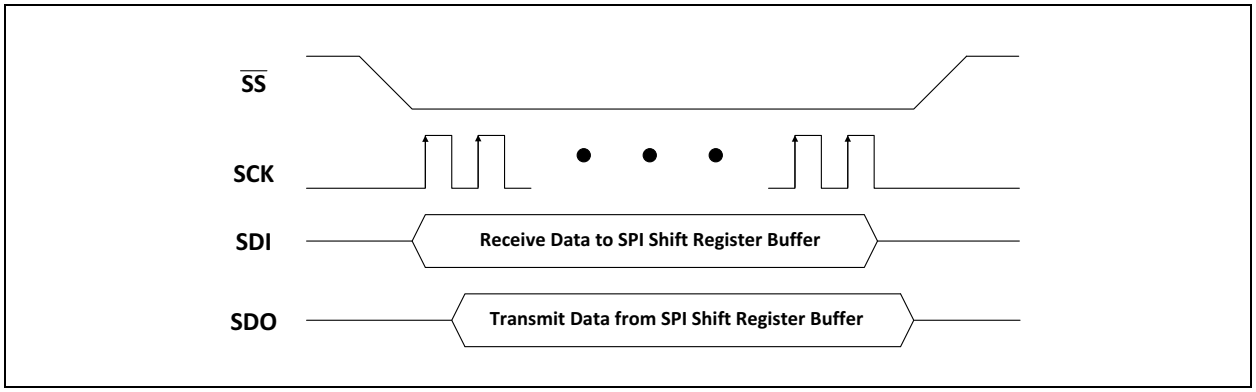


FIGURE 3-1: *SPI Signal Diagram.*

The bit order of the SDI data input is defined as follows. The first and second data bits represent bit 1 and bit 0 of channel 15 in register D, respectively. The third and fourth bits represent bit 1 and bit 0 of channel 14 in register D. The similar pattern is extended all the way to channel 0. Hence, there are 32 data bits to control register D to cover all sixteen channels.

The next 32 data bits are arranged in the same fashion for register C. Similarly, the exact pattern repeats itself for register B and A. Since each register (A, B, C and D) contains 32 bits of data, the SPI shift register buffer is 128 bits long.

Bit 1 of channel 15 in register D is defined as the MSb (Most Significant bit) and bit 0 of channel 0 in register A as the LSb (Least Significant bit) in this SPI shift register buffer definition.

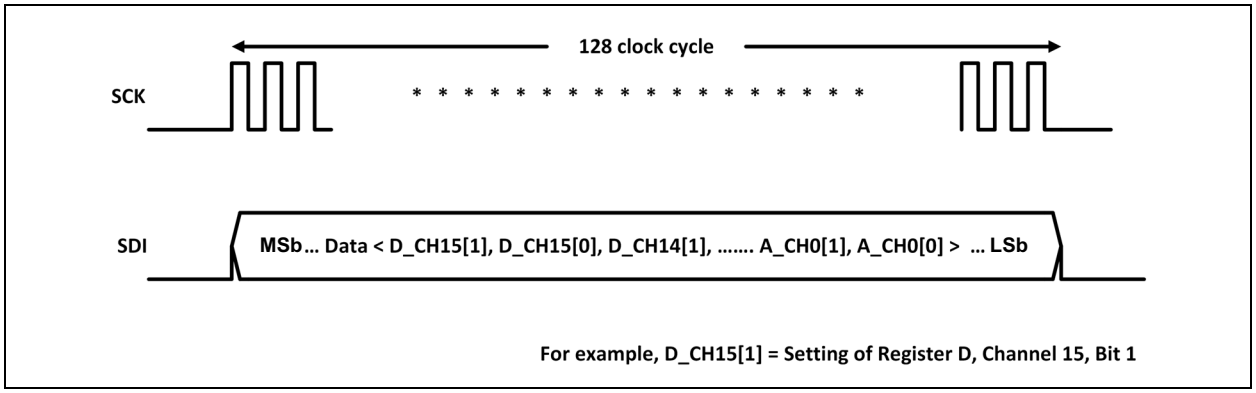


FIGURE 3-2: *SPI Bit Pattern Diagram.*

The following table shows the summary of the SPI shift register buffer.

TABLE 3-1: REGISTER LEGEND

Sym	Description	Sym	Description
R	Readable bit	HC	Cleared by Hardware only
W	Writable bit	HS	Set by Hardware only
U	Unimplemented bit, read as '0'	1	Bit is set at Reset
P	Programmable bit	0	Bit is cleared at Reset
S	Settable bit	x	Bit is unknown at Reset
C	Clearable bit		

Example: R/W - 0 indicates the bit is both readable or writable, and reads '0' after a Reset.

TABLE 3-2: SPI_SR 128-BIT BUFFER SUMMARY

Register Name	Bit Range	Bit 127/119/111/103	Bit 126/118/110/102	Bit 125/117/109/101	Bit 124/116/108/100	Bit 123/115/107/99	Bit 122/114/106/98	Bit 121/113/105/97	Bit 120/112/104/96
$\overline{\text{LATCHD}}$	<127:120>	CH15<1:0>		CH14<1:0>		CH13<1:0>		CH12<1:0>	
	<119:112>	CH11<1:0>		CH10<1:0>		CH9<1:0>		CH8<1:0>	
	<111:104>	CH7<1:0>		CH6<1:0>		CH5<1:0>		CH4<1:0>	
	<103:96>	CH3<1:0>		CH2<1:0>		CH1<1:0>		CH0<1:0>	
Register Name	Bit Range	Bit 95/87/79/71	Bit 94/86/78/70	Bit 93/85/77/69	Bit 92/84/76/68	Bit 91/83/75/67	Bit 90/82/74/66	Bit 89/81/73/65	Bit 88/80/72/64
$\overline{\text{LATCHC}}$	<95:88>	CH15<1:0>		CH14<1:0>		CH13<1:0>		CH12<1:0>	
	<87:80>	CH11<1:0>		CH10<1:0>		CH9<1:0>		CH8<1:0>	
	<79:72>	CH7<1:0>		CH6<1:0>		CH5<1:0>		CH4<1:0>	
	<71:64>	CH3<1:0>		CH2<1:0>		CH1<1:0>		CH0<1:0>	
Register Name	Bit Range	Bit 63/55/47/39	Bit 62/54/46/38	Bit 61/53/45/37	Bit 60/52/44/36	Bit 59/51/43/35	Bit 58/50/42/34	Bit 57/49/41/33	Bit 56/48/40/32
$\overline{\text{LATCHB}}$	<63:56>	CH15<1:0>		CH14<1:0>		CH13<1:0>		CH12<1:0>	
	<55:48>	CH11<1:0>		CH10<1:0>		CH9<1:0>		CH8<1:0>	
	<47:40>	CH7<1:0>		CH6<1:0>		CH5<1:0>		CH4<1:0>	
	<39:32>	CH3<1:0>		CH2<1:0>		CH1<1:0>		CH0<1:0>	
Register Name	Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
$\overline{\text{LATCHA}}$	<31:24>	CH15<1:0>		CH14<1:0>		CH13<1:0>		CH12<1:0>	
	<23:16>	CH11<1:0>		CH10<1:0>		CH9<1:0>		CH8<1:0>	
	<15:8>	CH7<1:0>		CH6<1:0>		CH5<1:0>		CH4<1:0>	
	<7:0>	CH3<1:0>		CH2<1:0>		CH1<1:0>		CH0<1:0>	

3.2 Quad-Latched Two-Bit per Channel Architecture

In the Quad-Latched 2-bit per channel architecture, each channel is controlled by a 2-bit encoding for each of the four possible states: "00" = (Hi-Z) high impedance, "01" = Pull-down to V_{NN}, "10" = Pull-up to V_{PP}, "11" = Driven to Ground. Since there are 16 channels on each HV53011 device, a 32-bit output control register is required.

Four separate latched arrays (A, B, C, & D) hold four possible 32-bit output configurations. The data is loaded from the arrays into the output control register by four separate external control signals ($\overline{\text{LATCHA}}$, $\overline{\text{B}}$, $\overline{\text{C}}$, $\overline{\text{D}}$). When the output control register is being

updated using one of the latch signals, the output will go to a not driven state temporarily to avoid shoot-through.

The data in these four latched arrays can be updated using the SPI shift register buffer. The 128 bits of data is first transmitted from the host processor to this device via the SPI interface. The data format has been discussed in the previous section. After this 128 bits transaction has completed, the data will stay in the SPI shift register buffer. Then the user sends an activation signal at the LATCHIN pin to initiate the transfer of the data from the SPI shift register to the four 32-bit registers (A, B, C and D).

When the application requires more output channels, the user can cascade more driver devices in a daisy chain configuration. The SDO pin is used to pass the data from the SPI shift register buffer to the cascaded driver IC.

The SPI signal pins (SCK, $\overline{SS}$, SDI and SDO) are used to control the data flow of the SPI shift register buffer. The five latch control signals ($\overline{LATCHIN}$, $\overline{LATCHA}$, $\overline{LATCHB}$, $\overline{LATCHC}$ and $\overline{LATCHD}$) are used to control the data selection of the high-voltage output from the four 32-bit registers. The SPI interface and latch functions are two independent operation blocks.

To achieve some power savings when idling for a period of time, a shutdown pin is available to reduce the quiescent current draw as much as possible.

TABLE 3-3: 2-BIT CONTROL AND OUTPUT VOLTAGE LOGIC TABLE

CONTROL BITS		HVOUT OUTPUT
Bit 1	Bit 0	
0	0	High Impedance (Hi-Z)
0	1	Driven Low (V_{NN})
1	0	Driven High (V_{PP})
1	1	Driven to Ground (0V)

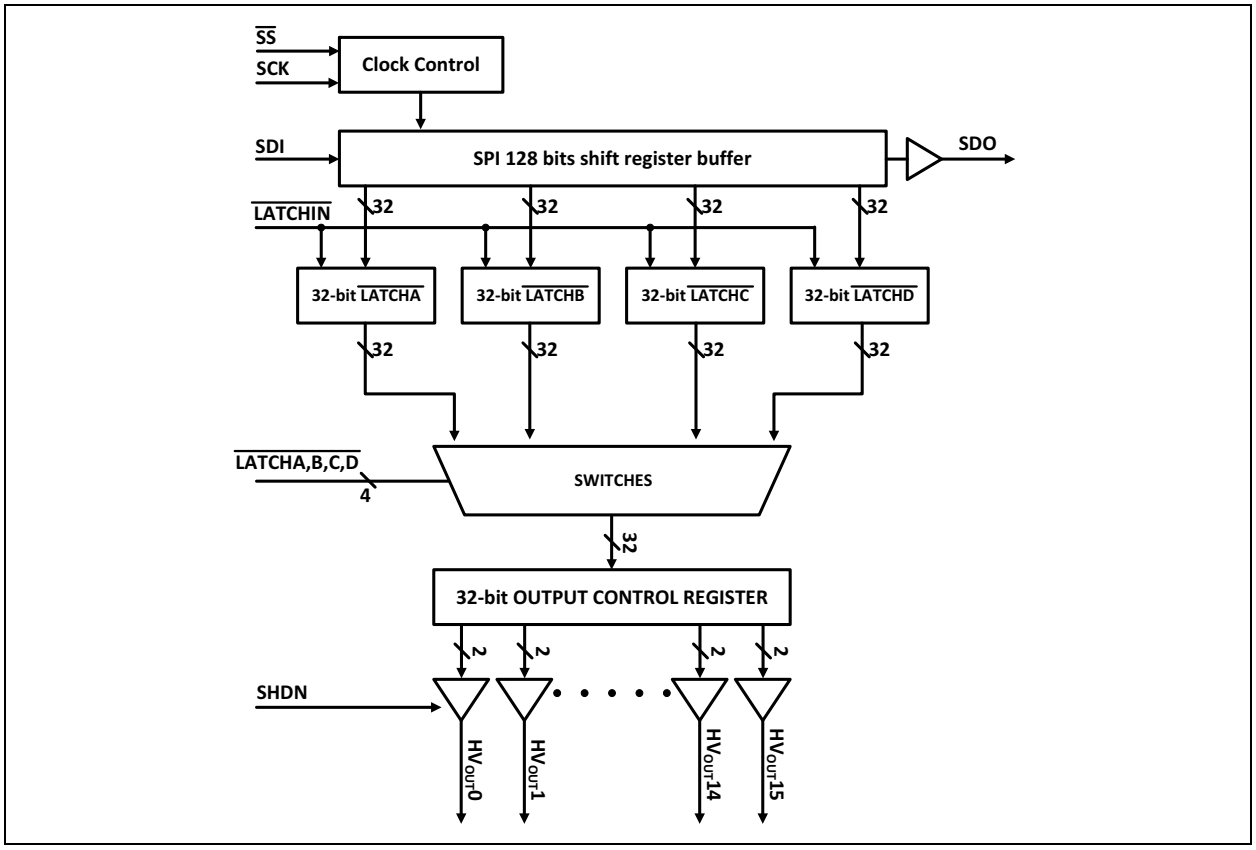


FIGURE 3-3: *Quad-Latched Two Bits per Channel Architecture.*

TABLE 3-4: QUAD-LATCHED TWO-BIT LOGIC STATE TABLE

$\overline{\text{LATCHIN}}$	$\overline{\text{LATCHA}}$	$\overline{\text{LATCHB}}$	$\overline{\text{LATCHC}}$	$\overline{\text{LATCHD}}$	Description
↓	X	X	X	X	SPI bit[127:96] into Latch Register D SPI bit[95:64] into Latch Register C SPI bit[63:32] into Latch Register B SPI bit[31:0] into Latch Register A
X*	↓	X	X	X	Register A to output
X*	X	↓	X	X	Register B to output
X*	X	X	↓	X	Register C to output
X*	X	X	X	↓	Register D to output

Note: * = Delay $\overline{\text{LATCHX}}$ appropriately if a register update from $\overline{\text{LATCHIN}}$ is still in progress.

↓ = Negative edge-triggered.

X = Don't care.

3.3 Driver Shutdown Mode

When the shutdown (SHDN) pin is at logic "1", any unnecessary circuit in the line driver will be disabled to minimize power consumption. It includes the level translator, bias current, voltage reference, driver output, SPI interface, and combinational logic. During shutdown, the quiescent current will be less than 100 µA. The system response time is less than 1 ms to switch between shutdown and active modes when a new signal is asserted at the shutdown pin.

3.4 Driver Power On Reset

The Power-on Reset function resets all high-voltage HV_{OUT} output to high impedance when the device is initially powered on. It also resets and clears the SPI buffer registers, registers A, B, C and D to logic "0".

3.5 Driver Output Current Sensing

Some system designs require a load sensing function to determine the size or any change of the capacitive load. One simple scheme is to place a series current sensing resistor on the power supply rail and measure the voltage drop across this resistor. This solution is very effective as long as the voltage drop is small enough not to affect the operation of the system.

The HV53011 driver IC provides this function by which users can monitor the supply current flowing through both high-voltage positive and negative supplies. Two external current sensing resistors are connected to V_{PP} and V_{NN} supply rails, respectively, as high side current sensing. The voltage drop across these resistors are fed to two pin pairs, V_{PP}-V_{PPO} and V_{NN}-V_{NNO}. Since this voltage drop is referenced to the V_{PP} and V_{NN} supply rails, it is not practical for any low-voltage ADC to measure this voltage. Hence, two internal difference amplifiers in the driver IC convert these voltage drops to ground reference.

The difference amplifier accepts maximum input voltage of 1V. The amplifier gain of 3.1 amplifies this input and send the output to the VPPSENSE and VNNSENSE pins. These amplifiers are designed using high-voltage and high value resistors to minimize its power consumption. These amplifier outputs are high impedance in nature, so an external high bandwidth (200 MHz) unity gain buffer is recommended. The high bandwidth is needed to capture the fast current pulse during the transition.

The user selects the value of the sensing resistor to fit the system requirement. The speed of the difference amplifier is its highest priority because the charge or discharge current appear in a short period of time. The amplifier output accuracy is less important. Both VPPSENSE and VNNSENSE outputs have a tolerance of ±14%.

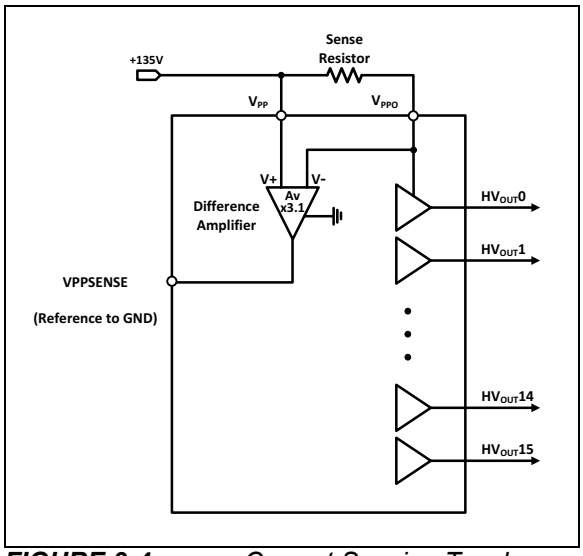


FIGURE 3-4: *Current Sensing Topology.*

TABLE 3-5: ACCEPTABLE POWER-ON SEQUENCES

Steps	Description
1	Connect ground.
2	Keep shutdown pin to low.
3	Set all driver inputs to low.
4	Power-on supplies in this sequence: V_{LL}, V_{NN}, V_{NF}, V_{SS}, V_{CC}, V_{PF} and then V_{PP}
5	Set all inputs to a known state.

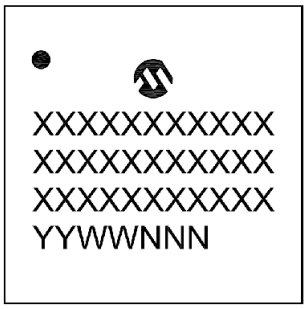
TABLE 3-6: ACCEPTABLE POWER-OFF SEQUENCES

Steps	Description
1	Set all inputs and shutdown pin to low.
2	Power-off supplies in this sequence: $V_{PP,}$ V_{PF}, V_{CC}, V_{SS}, V_{NF}, V_{NN} and then V_{LL}.
3	Disconnect ground

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

59-Ball TFBGA (8x8x1.2 mm)



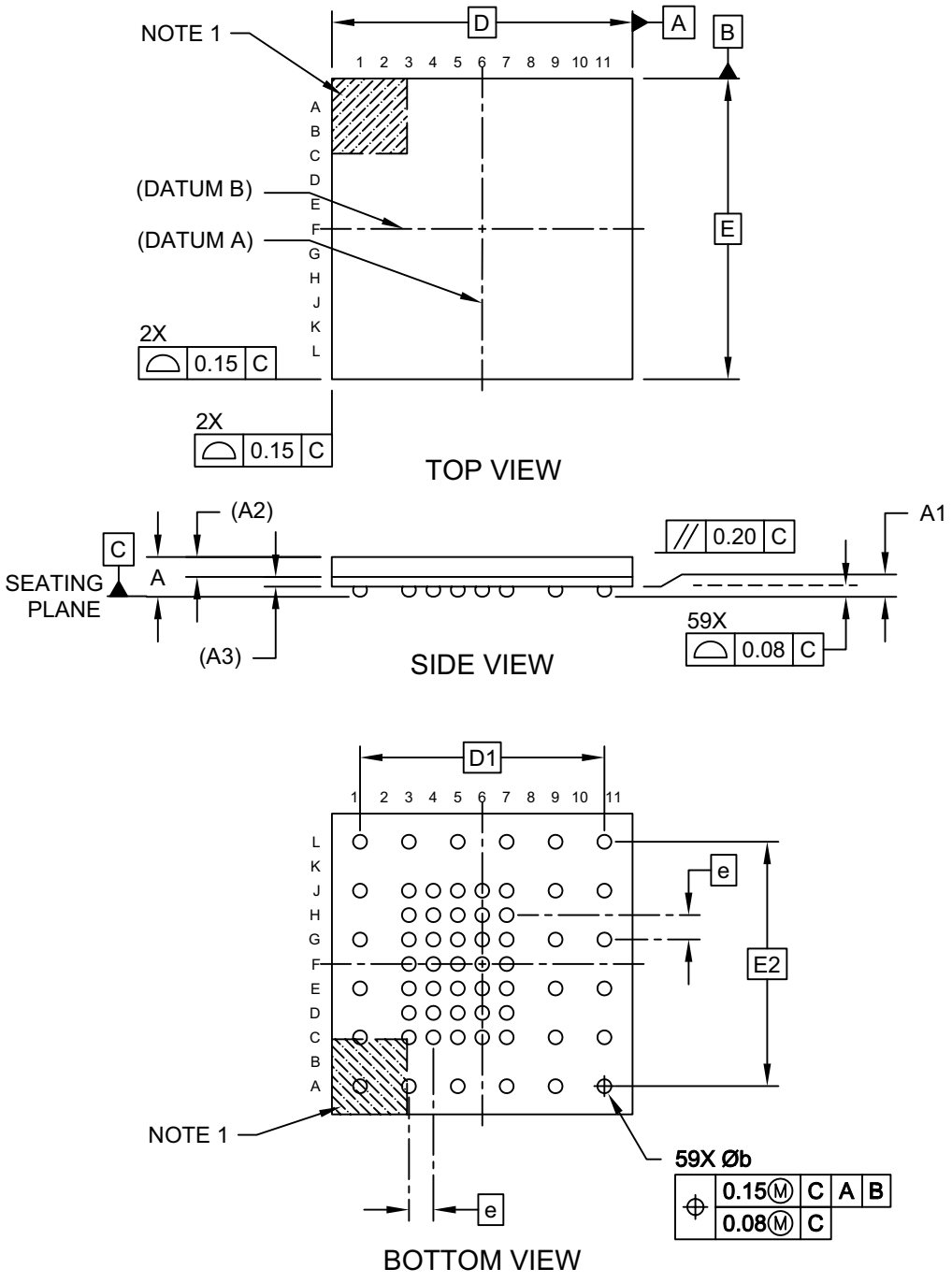
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e8	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e8) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

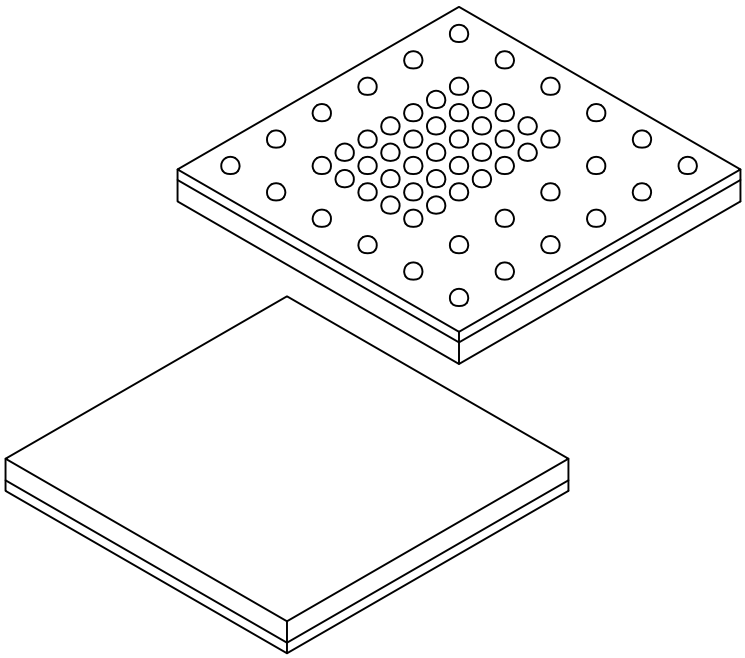
59-Ball Thin Fine Pitch Ball Grid Array (KVX) - 8x8 mm Body [TFBGA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



59-Ball Thin Fine Pitch Ball Grid Array (KVX) - 8x8 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



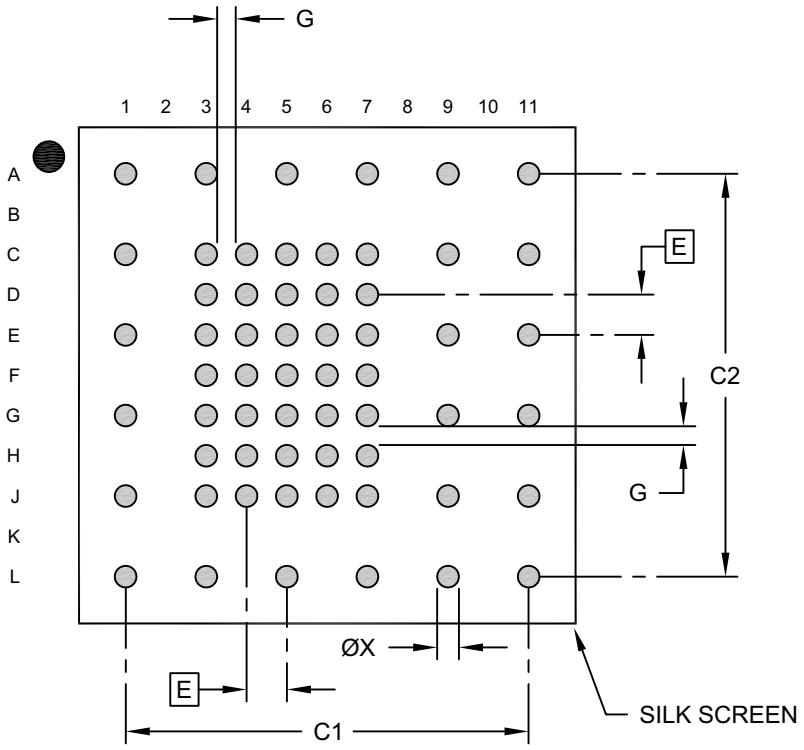
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		59	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.22	0.27	0.32
Mold Thickness	A2		0.53 REF	
Substrate Thickness	A3		0.26 REF	
Overall Length	D		8.00 BSC	
Overall Terminal Spacing	D1		6.50 BSC	
Overall Width	E		8.00 BSC	
Overall Terminal Spacing	E1		6.50 BSC	
Terminal Diameter	b	0.32	0.37	0.42

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

59-Ball Thin Fine Pitch Ball Grid Array (KVX) - 8x8 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Overall Contact Pad Spacing	C1		6.50	
Overall Contact Pad Spacing	C2		6.50	
Contact Pad Width (X59)	X			0.35
Contact Pad to Contact Pad	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

APPENDIX A: REVISION HISTORY

Revision A (March 2021)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X-	X	/XXX
Device	Media Type Tape and Reel	Temperature Range	Package

Device:	HV53011: 16-Channel, ±135V Push-Pull Driver with RTZ
Media Type:	blank = 260/Tray for KVX Package T = 1000/Reel for KVX Package
Temperature Range:	E =-40°C to +125°C (Extended) RoHS Compliant
Package:	KVX = Thin Fine Pitch Ball Grid Array 59-Ball TFBGA (8 x 8 x 1.2 mm)

Examples:

a) HV53011-E/KVX: 16-Channel, ±135V Push-Pull Driver with RTZ. Thin Fine Pitch Ball Grid Array, 59-Ball TFBGA (8 x 8 x 1.2mm) Package, 260/Tray

b) HV53011T-E/KVX:16-Channel, ±135V Push-Pull Driver with RTZ. Thin Fine Pitch Ball Grid Array, 59-Ball TFBGA (8x 8 x 1.2mm) Package, 1000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
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