

8-Channel High-Speed $\pm 60V$ $\pm 1A$ Ultrasound RTZ Pulser

Features

- HVCMOS[®] Technology for High Performance
- High-density Integrated Ultrasound Transmitter
- 0V to $\pm 60V$ Output Voltage
- $\pm 1A$ Source and Sink Current in Pulse Mode
- $\pm 1A$ Source and Sink Current in Return-to-Zero (RTZ) Mode
- Up to 20 MHz Operating Frequency
- Matched Delay Times
- Optional Clock Realignment
- 3.3V CMOS Logic Interface and Reference
- +3.3V Low-voltage Supply for V_{DD}
- Built-in Linear Regulators for Floating Gate Drivers
- Built-in Output Drain Diodes and Bleed Resistors

Applications

- Portable Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Pulse Waveform Generator

General Description

The HV7350 is an 8-channel monolithic high-voltage high-speed pulse generator with built-in fast return to zero-damping FETs. This high-voltage and high-speed integrated circuit is designed for portable medical ultrasound imaging system.

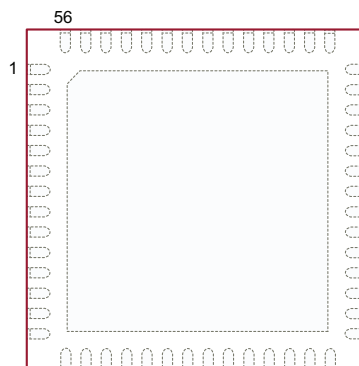
The HV7350 consists of a controller logic interface circuit, level translators, MOSFET gate drives, and high-current power P-channel and N-channel MOSFETs as the output stage for each channel.

The output peak currents of each channel are guaranteed to be over $\pm 1A$ with up to $\pm 60V$ pulse swings as well as Return-to-Zero mode. The gate drivers for the output MOSFETs are powered by built-in linear 5V regulators referenced to V_{PP} and V_{NN} . This direct coupling topology of the gate drivers not only saves four floating voltage supplies or AC coupling capacitors per channel but also makes the PCB layout smaller and easier.

An input clock pin is available to realign all the logic input control lines to a master clock. Precise logic timing is always essential in any ultrasound systems.

Package Type

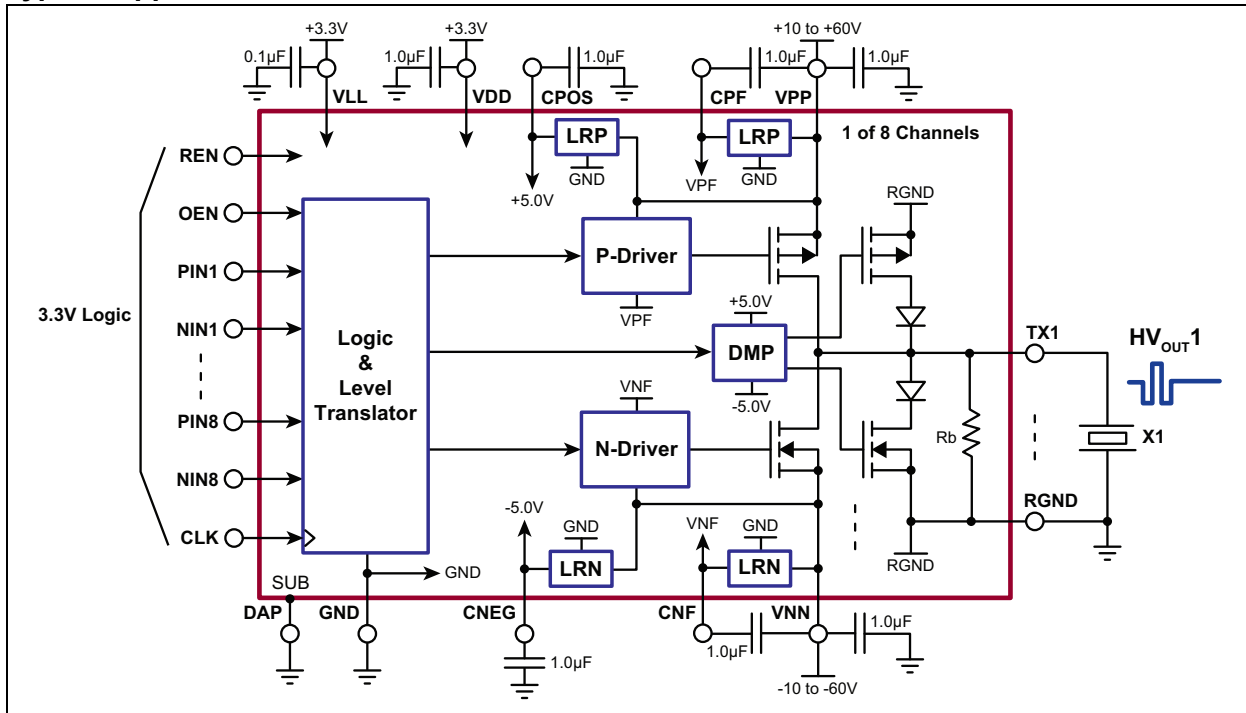
56-lead (8 X 8) QFN
(Top view)



See [Table 2-1](#) for pin information.

HV7350

Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

GND and Substrate Voltage, V _{SUB}	0V
Positive Logic Supply, V _{LL}	-0.5V to +5.5V
Positive Logic and Level Translator Supply, V _{DD}	-0.5V to +5.5V
Positive Level Translator Decoupling Pin, C _{POS} to GND	-0.5V to +5.5V
Negative Level Translator Decoupling Pin, C _{NEG} to GND	+0.5V to -5.5V
Positive Floating Gate Driver Decoupling Pin, V _{PP} -C _{PF}	-0.5V to +5.5V
Floating Gate Driver Decoupling Pin, C _{NF} -V _{NN}	-0.5V to +5.5V
Differential High-voltage Supply, V _{PP} -V _{NN}	+130V
High-voltage Positive Supply, V _{PP}	-0.5V to +65V
High-voltage Negative Supply, V _{NN}	+0.5V to -65V
All Logic Input CLK, PIN _X , NIN _X , OEN and REN Voltages	-0.5V to +5.5V
Operating Junction Temperature, T _J	-40°C to +125°C
Storage Temperature, T _S	-65°C to +150°C
ESD Rating (Note 1).....	ESD Sensitive

† **Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD sensitive. Handling precautions are recommended.

OPERATING SUPPLY VOLTAGES AND CURRENT (EIGHT ACTIVE CHANNELS)

Electrical Specifications: V_{LL} = +3.3V, V_{DD} = +3.3V, V_{PP} = +60V, V_{NN} = -60V, V_{CLK} = +3.3V, T_A = 25°C unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
V _{DD} Voltage Supply	V _{DD}	2.97	3.3	5.2	V	
V _{DD} UVLO	UVLO _{DD}	2.3	2.6	2.8	V	
Logic Voltage Reference	V _{LL}	2.5	3.3	5	V	
V _{LL} UVLO	UVLO _{LL}	1.3	1.55	1.7	V	
Positive High-voltage Supply	V _{PP}	+10	—	+60	V	
Negative High-voltage Supply	V _{NN}	-60	—	-10	V	
V _{LL} Current	I _{LLQ}	—	8	—	μA	OEN = REN = 0
V _{DD} Current	I _{DDQ}	—	1	—		
V _{PP} Current	I _{PPQ}	—	5	10		
V _{NN} Current	I _{NNQ}	—	5	10		
V _{LL} Current	I _{LLEN}	—	13	20	μA	OEN = REN = 1 5 ms after f = 0 MHz
V _{DD} Current	I _{DDEN}	—	480	700		
V _{PP} Current	I _{PPEN}	—	220	350		
V _{NN} Current	I _{NNEN}	—	300	400	mA	f = 5 MHz, continuous, no loads, for calculation reference only
V _{DD} Current	I _{DCCW}	—	2.3	—		
V _{PP} Current	I _{PPCW}	—	80	—		
V _{NN} Current	I _{NNCW}	—	80	—	μA	f _{CLK} = 10 MHz, PIN = NIN = 0
V _{LL} Current	I _{LL,CLK}	—	33	—		

HV7350

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $V_{LL} = +3.3V$, $V_{DD} = +3.3V$, $V_{PP} = +60V$, $V_{NN} = -60V$, $V_{CLK} = +3.3V$, $T_A = 25^\circ C$ unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
PULSER P-CHANNEL MOSFET						
Output Saturation Current	I_{OUT}	1	1.5	—	A	
Channel Resistance	R_{ON}	—	13.2	—	Ω	$I_{SD} = 100\text{ mA}$
PULSER P-CHANNEL MOSFET						
Output Saturation Current	I_{OUT}	1	1.5	—	A	
Channel Resistance	R_{ON}	—	8	—	Ω	$I_{SD} = 100\text{ mA}$
DAMPING P-CHANNEL MOSFET						
Output Saturation Current	I_{OUT}	1	1.5	—	A	
Channel Resistance	R_{ON}	—	13	—	Ω	$I_{SD} = 100\text{ mA}$
DAMPING N-CHANNEL MOSFET						
Output Saturation Current	I_{OUT}	1	1.5	—	A	
Channel Resistance	R_{ON}	—	9	—	Ω	$I_{SD} = 100\text{ mA}$
LOGIC INPUT						
Input Logic High Voltage	V_{IH}	$0.7 \cdot V_{LL}$	—	V_{LL}	V	$V_{LL} = 2.5V$ to $3.3V$ $V_{LL} = 5V$
		$0.8 \cdot V_{LL}$	—			
Input Logic Low Voltage	V_{IL}	0	—	$0.3 \cdot V_{LL}$	V	$V_{LL} = 2.5V$ to $3.3V$ $V_{LL} = 5V$
			—	$0.2 \cdot V_{LL}$		
Input Logic High Current	I_{IH}	—	—	10	μA	
Input Logic Low Current	I_{IL}	-10	—	—	μA	
Input Logic Capacitance	C_{IN}	—	—	5	pF	
MOSFET DRAIN BLEED RESISTOR						
Output Bleed Resistance	R_{B1-8}	12	17	25	k Ω	
Bleed Resistors Power Limit	P_{RB1-8}	—	—	50	mW	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $V_{LL} = +3.3V$, $V_{DD} = +3.3V$, $V_{PP} = +60V$, $V_{NN} = -60V$, $V_{CLK} = +3.3V$, $T_A = 25^\circ C$ unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Output Rise Time	t_r	—	30	—	ns	330 pF//2.5 k Ω load
Output Fall Time	t_f	—	30	—	ns	10%–90%
Enable Time	t_{EN}	—	300	500	μs	Cap value (See Typical Application Circuit.), OEN = REN
Disable Time	t_{DIS}	—	2.8	10	μs	
Delay Time on PIN _X Rise	t_{d1}	—	12	—	ns	1 Ω resistor load, D% < 1% (See Timing Waveforms.) 50% inputs to 50% T_X current
Delay Time on NIN _X Rise	t_{d2}	—	12	—		
Delay Time on Damping Rise	t_{d3}	—	12	—		
Delay Time on Damping Fall	t_{d4}	—	12	—		
Delay Time on CLK Rise	t_{dc}	—	9	—		
Delay Time Matching	Δt_{DELAY}	—	± 3	—	ns	P to N, channel to channel
Delay Jitter on Rise or Fall	t_j	—	30	—	ps	$V_{PP}/V_{NN} = +/-25V$, input t_r 50% to HV _{OUT} t_r or t_f 50%, with 330 pF//2.5 k Ω load
RTZ FETs Drain Diode t_{rr}	t_{rr}	—	25	—	ns	$I_F = 1A$, $I_R = 1A$, $R_L = 10\Omega$

AC ELECTRICAL CHARACTERISTICS (CONTINUED)





Electrical Specifications: $V_{LL} = +3.3V$, $V_{DD} = +3.3V$, $V_{PP} = +60V$, $V_{NN} = -60V$, $V_{CLK} = +3.3V$, $T_A = 25^\circ C$ unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Retiming Clock Frequency	f_{CLK}	10	220	—	MHz	
Retiming Clock Rise and Fall Times	t_{rc} , t_{fc}	—	0.5	5	ns	
Set-up Time, PIN/NIN to CLK	t_{SU}	2	—	—	ns	
Hold time, CLK to PIN/NIN	t_H	1	—	—	ns	
Clock Time Low	t_{CLK_LO}	2	—	100	ns	CLK input must have at least one pulse before PIN and NIN inputs are not zero. Be sure to return inputs to zero before stopping clock.
Clock Time High	t_{CLK_HI}	2	—	100	ns	
Clock Recognition Time	t_{CLK_REC}	—	2	—	ns	
Clock Release Time	t_{CLK_RLS}	150	300	800	ns	
Output Frequency Range	f_{OUT}	—	—	20	MHz	100 Ω resistor load
Second Harmonic Distortion	HD2	—	-40	—	dB	
Output Capacitance	C_{OSS}	—	50	—	pF	$V_{DS} = 25V$, $f = 1$ MHz of T_X pin total

TEMPERATURE SPECIFICATIONS

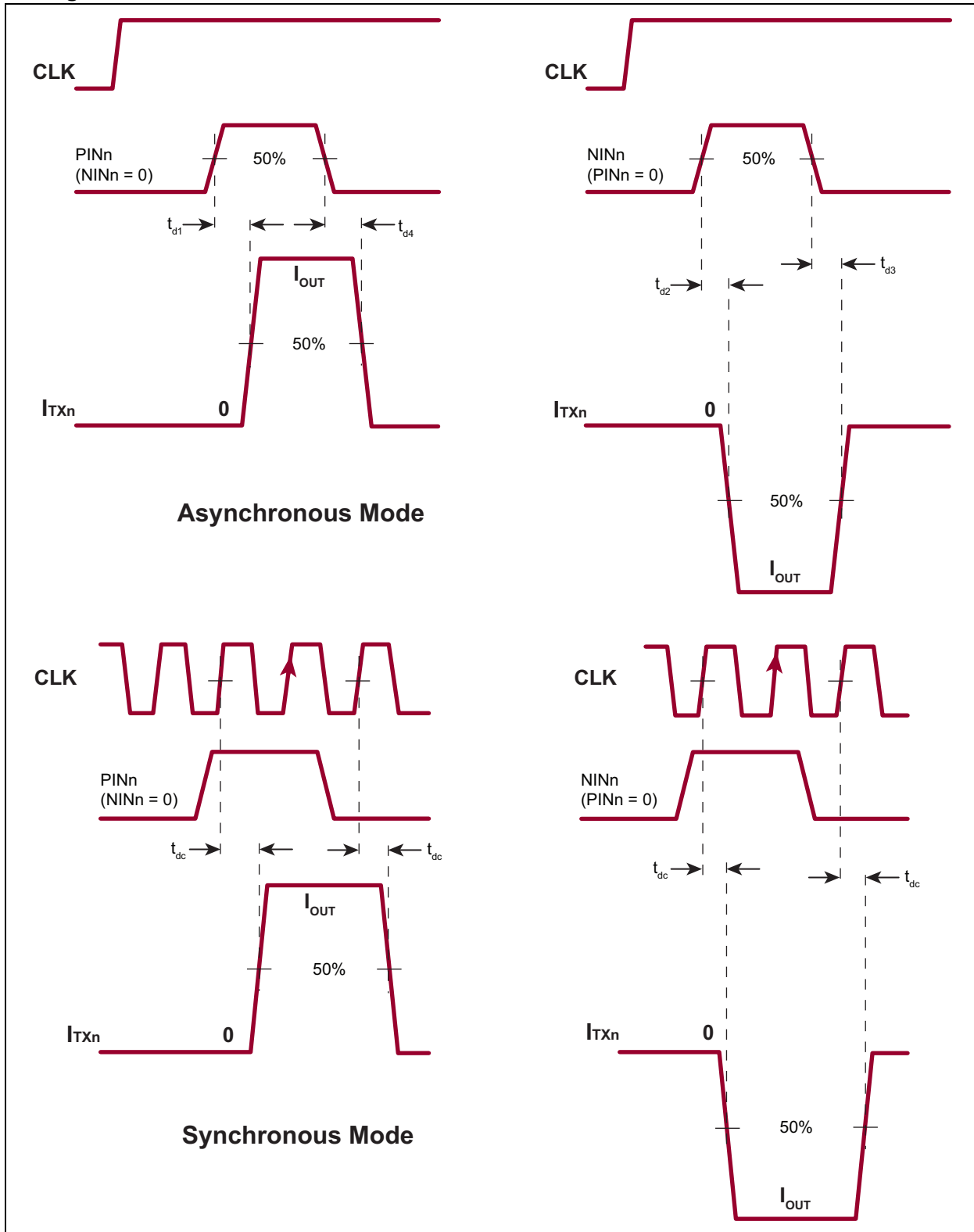
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	-40	—	+125	$^\circ C$	
Storage Temperature	T_S	-65	—	+150	$^\circ C$	
PACKAGE THERMAL RESISTANCE						
56-lead (8 X 8) QFN	θ_{JA}	—	21	—	$^\circ C/W$	

LOGIC CONTROL TABLE

MODE	LOGIC INPUTS				TX_N OUTPUT		
	OEN	CLK	PIN_X	NINX	VPP	VNN	RGND
Asynchronous Mode Output Change on PIN/NIN	1	VLL	0	0	OFF	OFF	ON
	1	VLL	1	0	ON	OFF	OFF
	1	VLL	0	1	OFF	ON	OFF
	1	VLL	1	1	OFF	OFF	OFF
Synchronous Mode Output Change at Retim- ing Clock (CLK) Rising Edge, registered by PIN/NIN	1		0	0	OFF	OFF	ON
	1		1	0	ON	OFF	OFF
	1		0	1	OFF	ON	OFF
	1		1	1	OFF	OFF	OFF
Disabled	0	X	X	X	OFF	OFF	OFF

HV7350

Timing Waveforms



2.0 PAD DESCRIPTION

Table 2-1 details the description of pads in HV7350.

Refer to [Package Type](#) for the location of pins.

TABLE 2-1: PAD FUNCTION TABLE

Pin Number	Pin Name	Description
1	PIN2	Input logic control of high-voltage output P-FET for Channel 2; High = on; Low = off (See Logic Control Table .)
2	NIN2	Input logic control of high-voltage output N-FET for Channel 2; High = on; Low = off (See Logic Control Table .)
3	PIN3	Input logic control of high-voltage output P-FET for Channel 3; High = on; Low = off (See Logic Control Table .)
4	NIN3	Input logic control of high-voltage output N-FET for Channel 3; High = on; Low = off (See Logic Control Table .)
5	PIN4	Input logic control of high-voltage output P-FET for Channel 4; High = on; Low = off (See Logic Control Table .)
6	NIN4	Input logic control of high-voltage output N-FET for Channel 4; High = on; Low = off (See Logic Control Table .)
7	OEN	Output enable; High = on; Low = off (See Logic Control Table .)
8	REN	Built-in positive and negative 5V voltage regulators enable; High = on; Low = off If REN = 0, four isolated 5V power supplies may provide, as external supplies, for the VPP to CPF, CNF to VNN, CPOS to GND and GND to CNEG pins. Note that between VPP to CPF and CNF to VNN, two must be floating supplies. (See Logic Control Table .)
9	PIN5	Input logic control of high-voltage output P-FET for Channel 5; High = on; Low = off (See Logic Control Table .)
10	NIN5	Input logic control of high-voltage output N-FET for Channel 5; High = on; Low = off (See Logic Control Table .)
11	PIN6	Input logic control of high-voltage output P-FET for Channel 6; High = on; Low = off (See Logic Control Table .)
12	NIN6	Input logic control of high-voltage output N-FET for Channel 6; High = on; Low = off (See Logic Control Table .)
13	PIN7	Input logic control of high-voltage output P-FET for Channel 7; High = on; Low = off (See Logic Control Table .)
14	NIN7	Input logic control of high-voltage output N-FET for Channel 7; High = on; Low = off (See Logic Control Table .)
15	PIN8	Input logic control of high-voltage output P-FET for Channel 8; High = on; Low = off (See Logic Control Table .)
16	NIN8	Input logic control of high-voltage output N-FET for Channel 8; High = on; Low = off (See Logic Control Table .)
17	VLL	Logic supply voltage and reference input (+3.3V)
18	GND	Logic and circuit return ground (0V)
19	VDD	Positive voltage power supply (+3.3V)
20	VPP	Positive high-voltage power supply (+10V to +60V)
21	VPP	
22	VPP	
23	CPF	Built-in linear voltage VPF regulator output decoupling capacitor pin, 1 uF from VPP to CPF for every CPF pin
24	CNF	Built-in linear voltage VNF regulator output decoupling capacitor pin, 1 uF from CNF to VNN for every CNF pin
25	VNN	Negative high-voltage power supply (-10V to -60V)
26	VNN	
27	VNN	
28	TX8	T _X pulser Channel 8 output
29	RGND	Damping ground and bleed resistors common return ground

HV7350

TABLE 2-1: PAD FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
30	TX7	T _X pulser Channel 7 output
31	RGND	Damping ground and bleed resistors common return ground
32	TX6	T _X pulser Channel 6 output
33	RGND	Damping ground and bleed resistors common return ground
34	TX5	T _X pulser Channel 5 output
35	CNEG	Built-in linear voltage -5V regulator output decoupling capacitor pin, 1 uF from CNEG to GND
36	CPOS	Built-in linear voltage +5V regulator output decoupling capacitor pin, 1 uF from CPOS to GND
37	TX4	T _X pulser Channel 4 output
38	RGND	Damping ground and bleed resistors common return ground
39	TX3	T _X pulser Channel 3 output
40	RGND	Damping ground and bleed resistors common return ground
41	TX2	T _X pulser Channel 2 output
42	RGND	Damping ground and bleed resistors common return ground
43	TX1	T _X pulser Channel 1 output
44	VNN	Negative high-voltage power supply (-10V to -60V)
45	VNN	
46	VNN	
47	CNF	Built-in linear voltage VNF regulator output decoupling capacitor pin, 1 uF from CNF to VNN for every CNF pin
48	CPF	Built-in linear voltage VPF regulator output decoupling capacitor pin, 1 uF from VPP to CPF for every CPF pin
49	VPP	Positive high-voltage power supply (+10V to +60V)
50	VPP	
51	VPP	
52	VDD	Positive voltage power supply (+3.3V)
53	GND	Logic and circuit return ground (0V)
54	CLK	Retiming register clock input. Connect to VLL to disable the retiming function.
55	PIN1	Input logic control of high-voltage output P-FET for Channel 1; High = on; Low = off (See Logic Control Table .)
56	NIN1	Input logic control of high-voltage output N-FET for Channel 1; High = on; Low = off (See Logic Control Table .)
VSUB (Thermal Pad)		Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to GND (0V) externally.

3.0 FUNCTIONAL DESCRIPTION

Follow the steps below to power up and power down the HV7350:

POWER-UP AND POWER-DOWN SEQUENCE (Note 1)

Power-Up		Power-Down	
Step	Description	Step	Description
1	V_{LL} with logic signal low	1	All logic signals go to low
2	V_{DD}	2	V_{PP} and V_{NN}
3	REN = 1 (external supplies on)	3	REN = 0 (external supplies off)
4	V_{PP} and V_{NN}	4	V_{DD}
5	Logic control signals active	5	V_{LL}

Note 1: Powering up or down in any arbitrary sequence will not damage the device. The power-up sequence and power-down sequence are only recommended to minimize possible inrush current.

OUTPUT CURRENT AND R_{ON} (Note 1, Note 4)

I_{SC} ²	R_{onP}	R_{onN}	I_{DMP} ³	R_{onDP}	R_{onDN}
1.5A	13 Ω	6.5 Ω	1.5A	13 Ω	8 Ω

Note 1: $V_{PP}/V_{NN} = +/-60V$; $V_{DD} = +3.3V$; REN = 1

2: I_{SC} is current into 1 Ω to GND.

3: I_{DMP} is current from +/-30V connected to T_X pin.

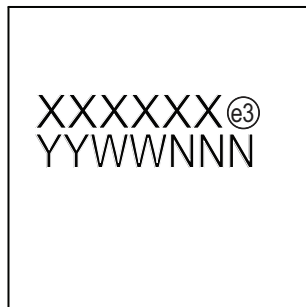
4: Maximum pulse width for current measurement on T_X pin is 20 ns.

HV7350

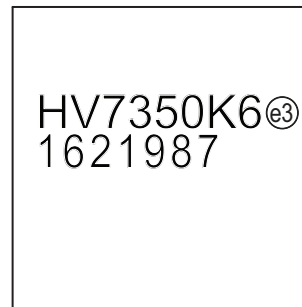
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

56-lead QFN

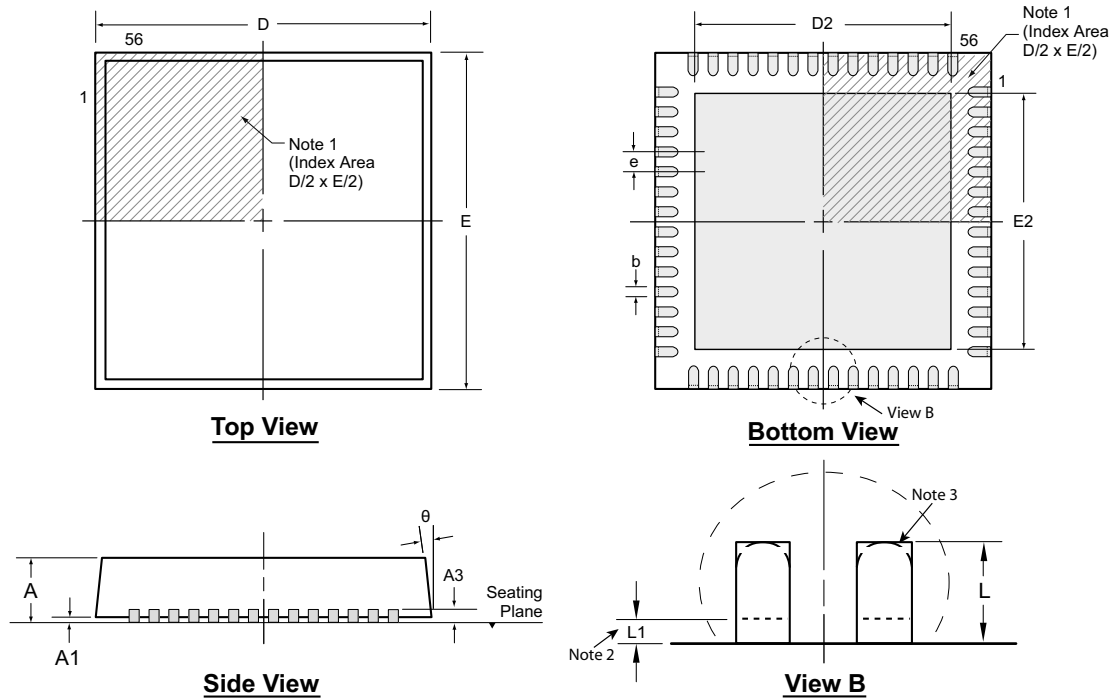


Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	^{ⓔ3}	Pb-free JEDEC [®] designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (^{ⓔ3}) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

56-Lead QFN Package Outline (K6) 8.00x8.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol	A	A1	A3	b	D	D2	E	E2	e	L	L1	θ	
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	7.85*	2.75	7.85*	2.75	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	8.00	5.70	8.00	5.70		0.40	-	-
	MAX	1.00	0.05		0.30	8.15*	6.70†	8.15*	6.70†		0.50	0.15	14°

JEDEC Registration MO-220, Variation VLLD-2, Issue K, June 2006.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings are not to scale.

HV7350

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2016)

- Converted Supertex Doc# DSFP-HV7350 to Microchip DS20005627A
- Changed the packaging quantity of 56-lead QFN M937 from 2000/Reel to 3000/Reel
- Made minor text changes throughout the document

HV7350

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	HV7350	=	8-Channel High-Speed $\pm 60V \pm 1A$ Ultrasound RTZ Pulser		
Package:	K6	=	56-lead VQFN		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	250/Tray for a K6 Package		
	M937	=	3000/Reel for a K6 Package		

Examples:

a) HV7350K6-G: 8-Channel High-Speed $\pm 60V \pm 1A$ Ultrasound RTZ Pulser, 56-lead VQFN, 250/Tray

b) HV7350K6-G-M937: 8-Channel High-Speed $\pm 60V \pm 1A$ Ultrasound RTZ Pulser, 56-lead VQFN, 3000/Reel

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =**

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, KeeLoq logo, Klear, LANCheck, LINK MD, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC32 logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, ETHERSYNCH, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and QUIET-WIRE are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, RightTouch logo, REAL ICE, Ripple Blocker, Serial Quad I/O, SQL, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2016, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-0997-7



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199

Tel: 480-792-7200

Fax: 480-792-7277

Technical Support:

[http://www.microchip.com/
support](http://www.microchip.com/support)

Web Address:

www.microchip.com

Atlanta

Duluth, GA

Tel: 678-957-9614

Fax: 678-957-1455

Austin, TX

Tel: 512-257-3370

Boston

Westborough, MA

Tel: 774-760-0087

Fax: 774-760-0088

Chicago

Itasca, IL

Tel: 630-285-0071

Fax: 630-285-0075

Cleveland

Independence, OH

Tel: 216-447-0464

Fax: 216-447-0643

Dallas

Addison, TX

Tel: 972-818-7423

Fax: 972-818-2924

Detroit

Novi, MI

Tel: 248-848-4000

Houston, TX

Tel: 281-894-5983

Indianapolis

Noblesville, IN

Tel: 317-773-8323

Fax: 317-773-5453

Los Angeles

Mission Viejo, CA

Tel: 949-462-9523

Fax: 949-462-9608

New York, NY

Tel: 631-435-6000

San Jose, CA

Tel: 408-735-9110

Canada - Toronto

Tel: 905-695-1980

Fax: 905-695-2078

ASIA/PACIFIC

Asia Pacific Office

Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong

Tel: 852-2943-5100

Fax: 852-2401-3431

Australia - Sydney

Tel: 61-2-9868-6733

Fax: 61-2-9868-6755

China - Beijing

Tel: 86-10-8569-7000

Fax: 86-10-8528-2104

China - Chengdu

Tel: 86-28-8665-5511

Fax: 86-28-8665-7889

China - Chongqing

Tel: 86-23-8980-9588

Fax: 86-23-8980-9500

China - Dongguan

Tel: 86-769-8702-9880

China - Guangzhou

Tel: 86-20-8755-8029

China - Hangzhou

Tel: 86-571-8792-8115

Fax: 86-571-8792-8116

China - Hong Kong SAR

Tel: 852-2943-5100

Fax: 852-2401-3431

China - Nanjing

Tel: 86-25-8473-2460

Fax: 86-25-8473-2470

China - Qingdao

Tel: 86-532-8502-7355

Fax: 86-532-8502-7205

China - Shanghai

Tel: 86-21-5407-5533

Fax: 86-21-5407-5066

China - Shenyang

Tel: 86-24-2334-2829

Fax: 86-24-2334-2393

China - Shenzhen

Tel: 86-755-8864-2200

Fax: 86-755-8203-1760

China - Wuhan

Tel: 86-27-5980-5300

Fax: 86-27-5980-5118

China - Xian

Tel: 86-29-8833-7252

Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen

Tel: 86-592-2388138

Fax: 86-592-2388130

China - Zhuhai

Tel: 86-756-3210040

Fax: 86-756-3210049

India - Bangalore

Tel: 91-80-3090-4444

Fax: 91-80-3090-4123

India - New Delhi

Tel: 91-11-4160-8631

Fax: 91-11-4160-8632

India - Pune

Tel: 91-20-3019-1500

Japan - Osaka

Tel: 81-6-6152-7160

Fax: 81-6-6152-9310

Japan - Tokyo

Tel: 81-3-6880-3770

Fax: 81-3-6880-3771

Korea - Daegu

Tel: 82-53-744-4301

Fax: 82-53-744-4302

Korea - Seoul

Tel: 82-2-554-7200

Fax: 82-2-558-5932 or

82-2-558-5934

Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857

Fax: 60-3-6201-9859

Malaysia - Penang

Tel: 60-4-227-8870

Fax: 60-4-227-4068

Philippines - Manila

Tel: 63-2-634-9065

Fax: 63-2-634-9069

Singapore

Tel: 65-6334-8870

Fax: 65-6334-8850

Taiwan - Hsin Chu

Tel: 886-3-5778-366

Fax: 886-3-5770-955

Taiwan - Kaohsiung

Tel: 886-7-213-7828

Taiwan - Taipei

Tel: 886-2-2508-8600

Fax: 886-2-2508-0102

Thailand - Bangkok

Tel: 66-2-694-1351

Fax: 66-2-694-1350

EUROPE

Austria - Wels

Tel: 43-7242-2244-39

Fax: 43-7242-2244-393

Denmark - Copenhagen

Tel: 45-4450-2828

Fax: 45-4485-2829

France - Paris

Tel: 33-1-69-53-63-20

Fax: 33-1-69-30-90-79

Germany - Dusseldorf

Tel: 49-2129-3766400

Germany - Karlsruhe

Tel: 49-721-625370

Germany - Munich

Tel: 49-89-627-144-0

Fax: 49-89-627-144-44

Italy - Milan

Tel: 39-0331-742611

Fax: 39-0331-466781

Italy - Venice

Tel: 39-049-7625286

Netherlands - Drunen

Tel: 31-416-690399

Fax: 31-416-690340

Poland - Warsaw

Tel: 48-22-3325737

Spain - Madrid

Tel: 34-91-708-08-90

Fax: 34-91-708-08-91

Sweden - Stockholm

Tel: 46-8-5090-4654

UK - Wokingham

Tel: 44-118-921-5800

Fax: 44-118-921-5820

06/23/16

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [RF Front End](#) category:

Click to view products by [Microchip](#) manufacturer:

Other Similar products are found below :

[SE2622L-R](#) [BGM1032N7E6327XUSA1](#) [LX5586LL](#) [LX5586HLL](#) [LX5586ALL](#) [SKY66111-21](#) [SKY65728-11](#) [SKY68000-31](#) [SKY85308-11](#)
[SKY85302-11](#) [SKY85300-21](#) [ADTR1107ACCZ](#) [LMP91051MTX/NOPB](#) [SE5501L-R](#) [SE5503A-R](#) [ADA8282WBCPZ](#) [ADRF5545ABCPZN](#)
[ADRF5545ABCPZN-R7](#) [AD8283WBCPZ](#) [AD8284WCSVZ](#) [ADRF5547BCPZN](#) [ADRF5547BCPZN-R7](#) [ADRF5549BCPZN](#)
[ADRF5549BCPZN-R7](#) [HV7350K6-G](#) [SE5516A-R](#) [MCP2030-I/SL](#) [MAX2335ETI+](#) [MD2131K7-G](#) [MD2134K7-G](#) [RFFM4554SR](#)
[RFFM4554TR7](#) [RFFM8504SR](#) [RFFM8511SR](#) [RFFM4552TR7](#) [RFFM4503TR7](#) [RFFM6903TR13](#) [HV7351K6-G](#) [MCP2035-I/ST](#)
[SE2614BT-R](#) [SE2438T-R](#) [SST12LF02-QXCE](#) [SST12LF09-Q3CE](#) [PN5180A0HN/C3E](#) [RFX2401C](#) [RFX2402E](#) [SKY85201-11](#)
[RFFM4591FTR7](#) [RFFM8211TR7](#) [RFFM4293TR7](#)