HV98100/HV98101

Non-Dimmable, Off-Line, LED Driver with Low Total Harmonic Distortions

Features

- Good LED Current Regulation
  - Better than 5% accuracy
- Valley Switching Buck-Boost Converter with Power Factor Correction (PFC)
  - 0.97 Power Factor (typical)
  - 5% Total Harmonic Distortion (THD) (typical)
- Uses a Standard Off-the-Shelf Inductor
  - No auxiliary winding required
- Single Input Voltage Range
  - HV98100: 110 V_{AC} ±15%
  - HV98101: 230 V_{AC} ±15%
- Supports 5W-15W Output Power
- Space-saving SOT-23-6L Package

Applications

- LED Lamps
- LED Lighting Fixtures

Description

The HV98100/HV98101 LED driver integrated circuit (IC) is an off-line, high-power factor, buck-boost controller targeted at general LED lighting products, such as LED lamps and LED lighting fixtures with a maximum power rating of about 15W.

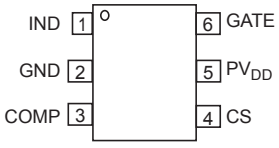
Valley-switching buck-boost converters are preferred in off-line applications since they reduce switching losses. A typical solution is to pair a constant on-time control scheme with valley switching to achieve both a high-power factor and good efficiency. However, this control scheme results in a higher total harmonic distortion, and the actual value is dependent on the input and output voltages. The HV98100/HV98101 uses a unique control scheme to achieve a high-power factor and low THD simultaneously under all line and load conditions, while maximizing efficiency utilizing valley switching. The average LED current is also controlled in a closed-loop manner to achieve high LED accuracy.

Other unique features of the ICs are the bootstrap of the IC supply voltage from the output, as well as the unique valley-sensing scheme that allows the use of a standard off-the-shelf inductor to minimize the overall system cost.

Applications with low-output voltage can be accommodated using a coupled inductor.

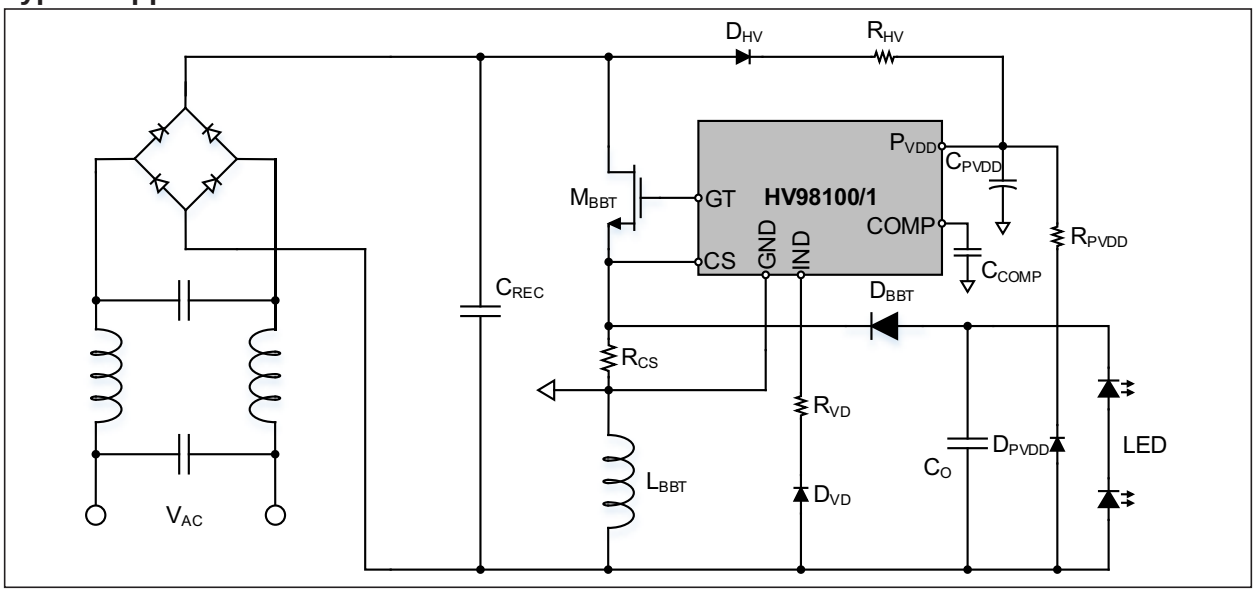
Package Types

HV98100/HV98101
6-Lead SOT-23

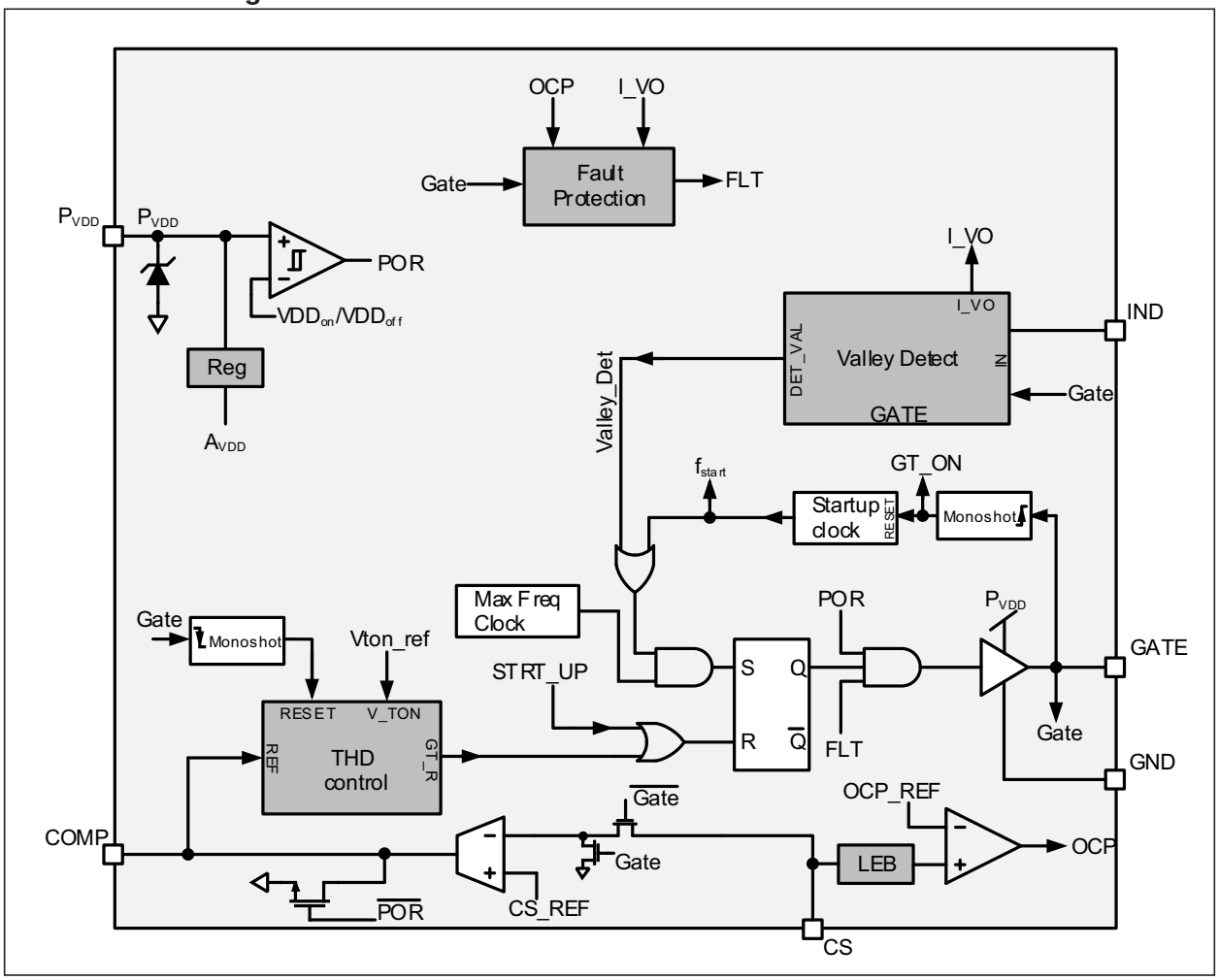


See Table 3-1 for pin description.

Typical Application Circuit



Internal Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage PV_{DD} to GND ..... -0.3V to +20V
GATE to GND ..... -0.3V to (PV_{DD} +0.5V)
CS, COMP, IND to GND ..... -0.3V to 4.5V
Operating Junction Temperature ..... -40°C to +125°C
Storage Temperature ..... -65°C to +150°C
Power Dissipation at +25°C for 6L-SOT-23 ..... 800 mW
ESD Protection on all pins (HBM) ..... 2 kV
ESD Protection on all pins (MM) 175V

* Based on JEDEC JESD51 testing and reporting standards

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all specifications are for $T_A = T_J = +25°C$, PV_{DD} = 12V. Boldface specifications apply over the full temperature range $T_A = T_J = -40°C$ to +125°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply (PV_{DD})						
PV_{DD} Clamp Voltage	$PV_{DD,clamp}$	**15.5**	**17**	**18.5**	V	Current into PV_{DD} = 4.0 mA; C_{GATE} = 500 pF; f_{sw} = 100 kHz;
V_{DD} Start Voltage	$V_{DD,ON}$	**14.5**	**16**	**17.5**	V	GATE starts switching
V_{DD} Stop Voltage	$V_{DD,OFF}$	**6.5**	**8**	**9.5**	V	GATE stops switching
Current into clamp	$I_{DD,max}$	—	—	5	mA	**Note 1**
Current drawn by IC before start	$I_{DD,Q}$	—	—	200	µA	Measured at PV_{DD} = 12V after PV_{DD} rises from 0V to 12V
Current drawn by IC during operation	$I_{DD,OP}$	—	—	4.3	mA	C_{GATE} = 500 pF; f_{sw} = 100 kHz; COMP = 3V; I_IND_{SINK} = 200 µA; I_IND_{SOURCE} = 250 µA
Gate Driver						
GATE Driver Sourcing Current	I_{SOURCE}	0.3	—	—	A	**Note 2**
Gate Driver Sinking Current	I_{SINK}	0.6	—	—	A	**Note 2**
Gate Rise Time (10%-90%)	T_{RISE}	—	—	45	ns	C_{GATE} = 500 pF
Gate Fall Time (10%-90%)	T_{FALL}	—	—	23	ns	C_{GATE} = 500 pF
Output Current Control						
Internal Reference Voltage	CS_{REF}	194	204	214	mV	**Note 2**
OTA Offset Voltage	V_{OFFSET}	-7.5	—	7.5	mV	**Note 2**
Open Loop DC Gain	A_V	55	—	—	dB	1V ≤ COMP ≤ 4V; Output open **Note 1**
Small Signal Transconductance	g_m	160	230	300	µA/V	1V ≤ COMP ≤ 4V; **Note 1**
Gain Bandwidth Product	GBW	0.16	0.24	—	MHz	CCOMP = 150 pF **(Note 2)**

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all specifications are for $T_A = T_J = +25°C$, $PV_{DD} = 12V$. Boldface specifications apply over the full temperature range $T_A = T_J = -40°C$ to $+125°C$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
R_{ON} of COMP Reset FET	R_{COMP}	300	400	500	Ω	
Internal Clocks						
Start-up Clock	F_{start}	6.25	10	15	kHz	
Maximum Frequency Limit	F_{max}	217	320	480	kHz	**Note 1**
Valley Detect						
Current into IND pin	I_{IND}	—	—	600	µA	**Note 2**
Voltage at IND pin	V_{IND}	3.87	4.3	4.73	V	I_{IND} = 250 µA
Comparator Delay Time	T_{delay}	—	—	50	ns	**Note 2**
Control Circuit						
Internal Timing Constant	K_T	—	1.25	—	µs	
Internal Voltage for Timing	V_{Tref}	—	2	—	V	HV98100
		—	2.5	—	V	HV98101
GATE On-time	T_{ON}	6.83	7.35	7.89	µs	HV98100 Ext Clk = 50 kHz COMP = 2V
	T_{ON}	6.11	6.7	7.05	µs	HV98101 Ext CSlk = 50 kHz COMP = 2V
Protection						
Over Voltage Protection Current Threshold	I_{OVP}	350	450	550	µA	GATE = LOW
Over Current Protection Reference	OCP_{REF}	2.2	2.35	2.5	V	
Over Current Protection Blanking Time	$T_{BLNKOCP}$	150	—	250	ns	**Note 2**
Detect time for Over Current Protection	T_{DETOCP}	150	—	250	ns	After TBLNKOCP (**Note 2**)
Over Current Comparator Delay	OCP_{DLY}	—	50	100	ns	100 mV overdrive (**Note 2**)

Note 1: Obtained by Design and Characterization; not 100% tested in production.

2: Design Guidance only.

TABLE 1-1: TEMPERATURE SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature	T_A	-65	—	+150	°C	
Operating Junction Temperature	T_J	-40	—	+125	°C	
Thermal Package Resistance						
Thermal Resistance, 6L-SOT-23	θJA	—	**124**	—	°C/W	
	θJC	—	**74**	—	°C/W	

2.0 TYPICAL OPERATING CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = T_J = +25°C$, $PV_{DD} = 12V$. Boldface specifications apply over the full temperature range $T_A = T_J = -40°C$ to $+125°C$.

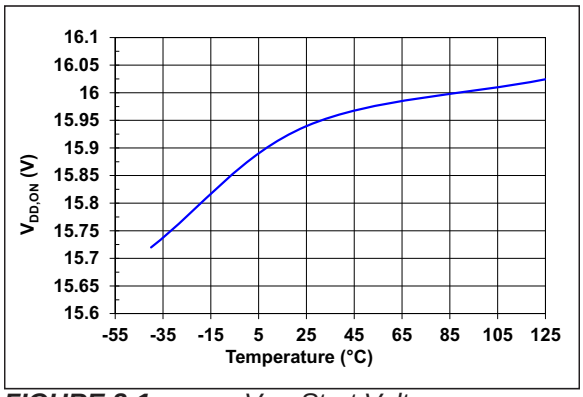


FIGURE 2-1: *V_{DD} Start Voltage vs. Junction Temperature.*

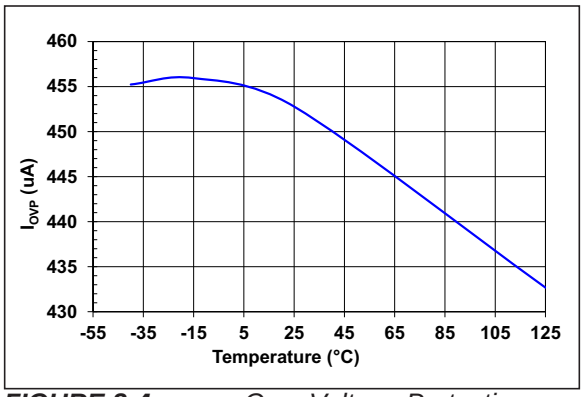


FIGURE 2-4: *Over Voltage Protection Current Threshold vs. Junction Temperature.*

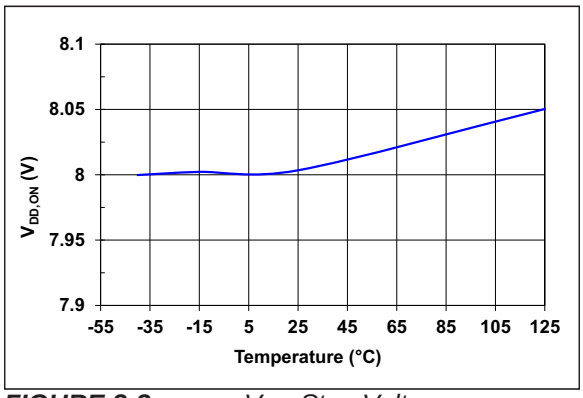


FIGURE 2-2: *V_{DD} Stop Voltage vs. Junction Temperature.*

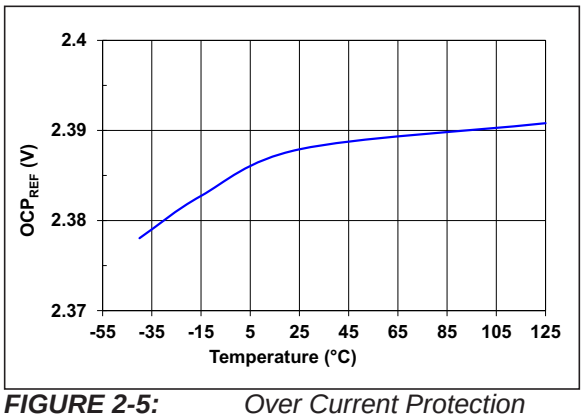


FIGURE 2-5: *Over Current Protection Reference vs. Junction Temperature.*

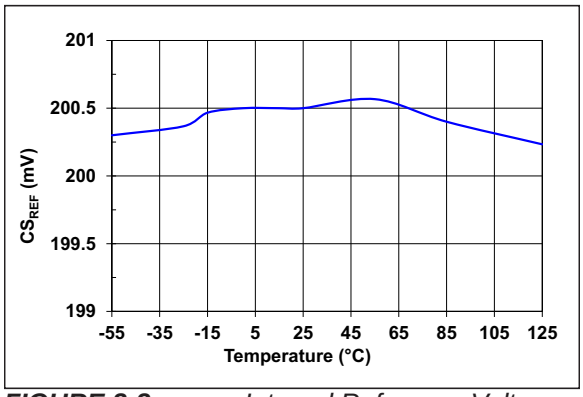


FIGURE 2-3: *Internal Reference Voltage vs. Junction Temperature.*

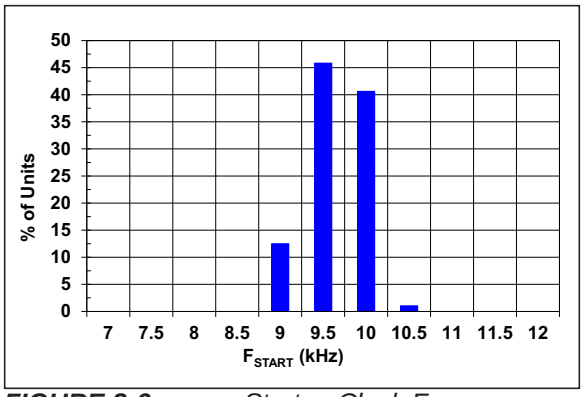


FIGURE 2-6: *Startup Clock Frequency Histogram.*

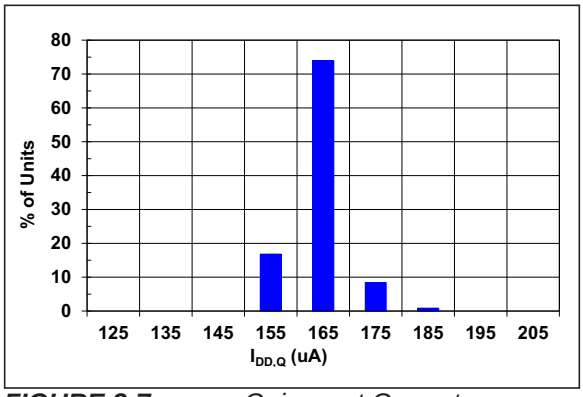


FIGURE 2-7: *Quiescent Current Histogram.*

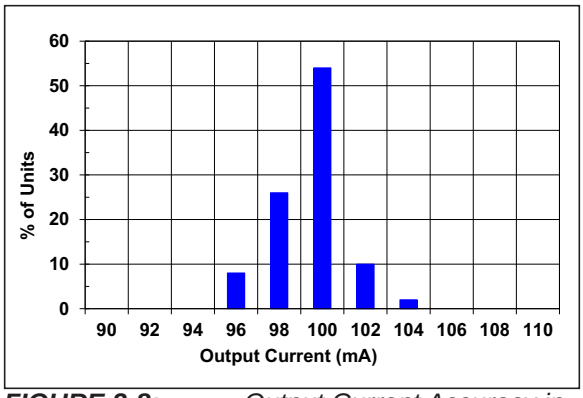


FIGURE 2-8: *Output Current Accuracy in Application.*

3.0 PIN DESCRIPTION

The description of the pins are listed in Table 3-1.

TABLE 3-1: PIN DESCRIPTION

HV98100/HV98101 SOT-23	Symbol	Description
1	IND	Input from LED String Anode for both valley detection and over-voltage protection Pin
2	GND	Common connection for all circuits Pin
3	COMP	Loop compensation for stable response Pin
4	CS	Current sense input for sensing inductor current Pin
5	PV_{DD}	Supply Voltage for the IC Pin
6	GATE	Gate driver for driving the external MOSFET Pin

3.1 IND

This pin is used for detecting the valley, as well as for over-voltage protection. The voltage at pin is maintained at approximately 4.3V. When the switching FET is off, current is sourced out of this pin. If this current exceeds 450 µA, then over voltage is detected and the IC shuts down. This current sourced out of the pin is also used to detect the valley, using a patented method.

For proper operation, the IND pin should be shielded to prevent mis-triggering due to the large voltage slew rates present in application. A recommended layout is shown in Figure 3-1.

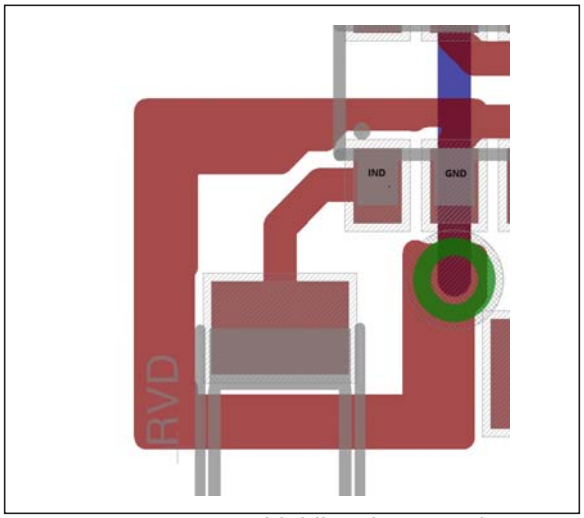


FIGURE 3-1: *Shielding the IND Pin.*

3.2 Power Ground Pin (GND)

This is the ground pin of the IC. The V_{DD} capacitor and COMP network should be connected to this pin and the GND pin should be connected to the sense resistor, as shown in the Typical Application Circuit for proper functioning of the IC. Figure 3-2 shows a recommended layout. Red traces in the layout are on the top layer, whereas blue traces on the layout are on the bottom layer.

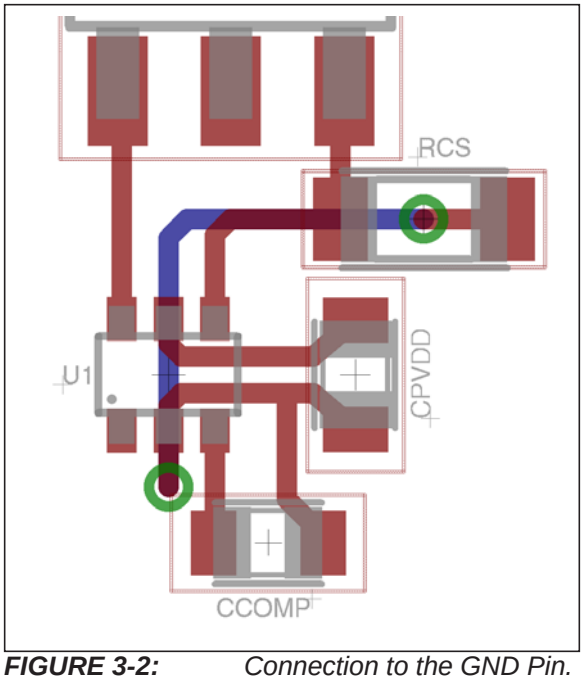


FIGURE 3-2: *Connection to the GND Pin.*

3.3 COMP

This pin is the output of the internal transconductance amplifier. A compensation network connected between COMP and GND pins is used to stabilize the closed loop control of the LED current.

3.4 CS

This pin is used to sense the inductor current. The inductor current information is used to derive the output LED current, as well as to protect the inductor from saturation.

3.5 PV_{DD}

This pin is the power supply pin for the IC. A minimum of 4.7 µF capacitor needs to be connected between PV_{DD} and GND for stability of the internal shunt regulator. The C_{PVDD} capacitor needs to be placed physically close to the IC to minimize the trace length between the PV_{DD} pin and the capacitor.

3.6 GATE

This pin is the gate drive output of the IC and is used to control the switching of the external FET.

4.0 FUNCTIONAL DESCRIPTION

4.1 Introduction

The HV98100/HV98101 control ICs provide constant average LED current for LED lamps and fixtures with a single-stage, valley-switching, buck-boost power-supply topology.

The IC is targeted at designs at a single-line voltage, such as 110 V_{AC} (HV98100) or 230 V_{AC} (HV98101) and does not support designs for universal input voltage range.

4.2 Principle of Operation

The IC adopts a novel control mechanism to vary both on-time and switching period at the same instant over the line cycle in a way that forces the average input current to be proportional to the input voltage, realizing high-power factor and low THD which is independent of the load voltage (V_O) (unlike a constant on-time control where the THD is dependent on the LED string voltage).

In order to determine the LED current regulation, power balancing is used to maintain the mean programmable LED current (I_O) in a closed-loop manner by means of the adaptive V_{COMP} swing upon the defined input/output voltage variation, as shown in Equation 4-1.

EQUATION 4-1:

$$I_O = \frac{V_{in,rms}^2 \cdot K_T \cdot V_{COMP}}{V_O}$$

Assume a V_{COMP} variation from 1.2V to 3.8V, an input voltage ($V_{IN,rms}$) variation of ±15% and the internal timing constant (K_T) variation of ±12%. With these assumptions, the maximum variation in the LED string voltage (to maintain constant LED current) cannot exceed ±18% approximately.

5.0 APPLICATION INFORMATION

5.1 Introduction

This section describes the operation of the various blocks in the IC. Detailed design information, along with a design example, is provided in **Section 6.0 "Design Example"**.

5.2 PV_{DD} Regulator

The supply current is initially fed from the rectified AC input directly via an external start-up resistor (R_{HV}) to peak charge a hold-up capacitor (C_{PVDD}) connected at this pin. Note that a switching diode (D_{HV}) is required in series to prevent the capacitor from discharging when the buck-boost converter FET (M_{BBT}) turns on. As the voltage on the V_{DD} capacitor increases, the IC is held in a Stand-by mode and draws minimum current (200 µA max.). Once the voltage at V_{DD} reaches $V_{DD,ON}$, the IC turns on and starts switching at an internally fixed switching frequency of 10 kHz, until the valley can be detected. Once the valley is detected, the converter starts working in the normal Valley-Switching mode and tries to regulate the LED current. In this mode, the current drawn by the IC from V_{DD} increases causing the voltage across the V_{DD} capacitor to start dropping (since the current supplied by the external start-up resistor is not sufficient).

If the V_{DD} voltage drops below $V_{DD,OFF}$, the IC enters into Stand-by mode and the process starts again. If the bootstrap from the output capacitor (C_O) is available to prevent the V_{DD} voltage from going below $V_{DD,OFF}$, then the LED driver operates normally. In this way, as shown in Figure 5-1, the PV_{DD} voltage bounces between $V_{DD,ON}$ and $V_{DD,OFF}$ within a hysteresis band for the IC to start GATE switching, until the energy stored in the output capacitor can be partially delivered to PV_{DD} through the bootstrapping resistor-diode network (R_{PVDD}-D_{PVDD}).

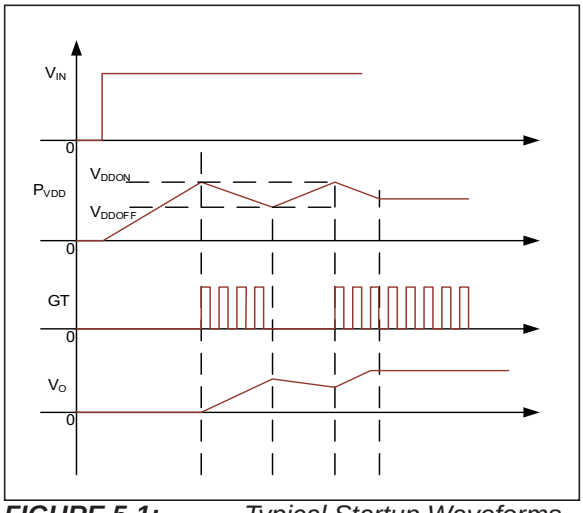


FIGURE 5-1: *Typical Startup Waveforms.*

The IC includes an internal V_{DD} clamp circuit. The clamp limits the voltage on the V_{DD} supply pin to the maximum value ($PV_{DD,clamp}$). If the maximum current supplied through the external resistors minus the current consumption of the IC is lower than the maximum value that the Zener clamp can sustain ($I_{DD,MAX}$), no external Zener diode is required.

5.3 LED Current Regulator

The LED current (I_O) is sensed directly using an external sense resistor R_{CS} and compared to an internal fixed reference (CS_{REF}). An internal transconductance amplifier is used to close the loop on the LED current with an external compensation capacitor. The LED current can be programmed as in Equation 5-1.

EQUATION 5-1:

$$I_{LED} = \frac{CS_{REF}}{R_{CS}}$$

5.4 Valley Switching

The driver incorporates valley switching (quasi-resonant switching), a technique for reducing switching loss at the turn-on event of the buck-boost converter FET. Valley detect is accomplished by sensing the current sunk into the IND pin when the GATE is low. The operation is illustrated in Figure 5-2. When the inductor current I_L has decreased to zero at t_2, the positive LED voltage V_L starts to oscillate around the 0V level (with respect to the IC GND), with an amplitude V_O. The GATE turns on again when the first lowest level (valley) is detected.

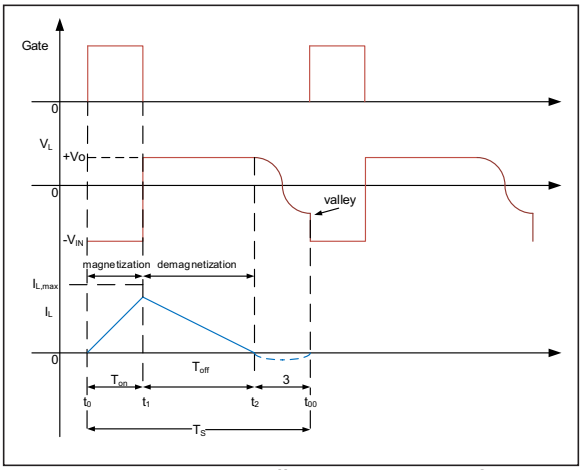


FIGURE 5-2: *Valley Detect Waveforms.*

However, in case the valley is not detected (during startup, output short circuit and input voltage zero crossings), a 10 kHz internal clock is used to start the next cycle.

5.5 Over-Voltage and Short-Circuit Protection

5.5.1 OVER-VOLTAGE PROTECTION

Apart from the valley detect, measuring the current sunk into the IND pin when the GATE is low can be used to sense an output over voltage or open circuit. The IND triggering level is I_{OVP}.

When the current into the IND pin exceeds I_{OVP}, the gate driver shuts down. The PV_{DD} capacitor starts discharging (since there is no bootstrap and the current through the input start-up resistor is insufficient to charge the capacitor). Once the voltage at PV_{DD} drops to $V_{DD,OFF}$, the IC goes into a low-current mode and the start-up procedure starts. This process keeps repeating until the over-voltage condition disappears.

5.5.2 SHORT-CIRCUIT PROTECTION

Output short circuit (or input under voltage) causes the converter to go into Continuous Conduction mode (CCM) by sensing the inductor current when M_{BBT} is on.

When the GATE turns on, a leading edge blanking circuit is activated within the IC. The blanking circuit has two functions:

1. Blank the first $T_{BLNKOCP}$ of the GATE on-time. During this time, R_{CS} will detect the leading edge spike, and the edge spike is not allowed to propagate to the comparator since it might cause false triggering of the OCP comparator.
2. Allow the OCP comparator to see the next T_{DETOCP} of the inductor current. Since the converter is assumed to be in Boundary Conduction mode during normal operation, when the GATE turns on, the inductor current will start at zero and start ramping up. The IC compares the second voltage across R_{CS} in the detect window after the GATE turns on and determines if the converter is operating in CCM.

If the IC detects four consecutive cycles of CCM, the GATE is turned off and the IC goes through a POR.

Typical waveforms are shown in Figures 5-3 and 5-4.

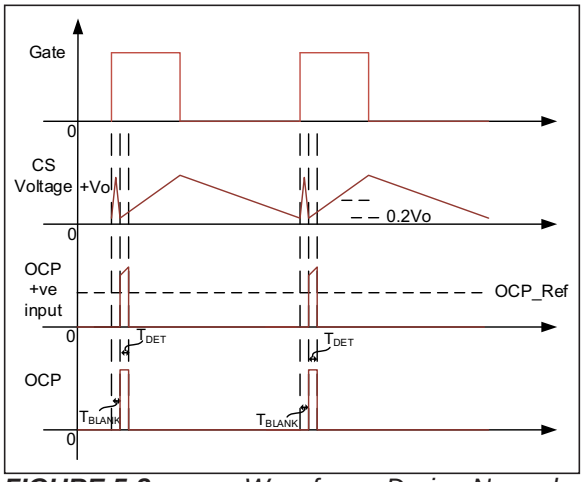


FIGURE 5-3: *Waveforms During Normal Operation.*

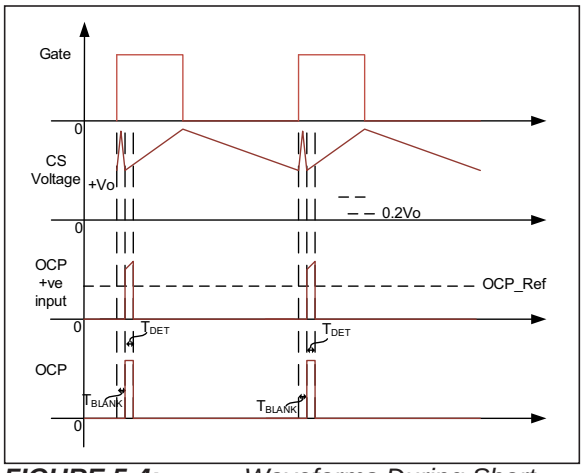


FIGURE 5-4: *Waveforms During Short Circuit.*

6.0 DESIGN EXAMPLE

This section describes the procedure to design an HV98100/HV98101 LED driver. The specifications used for this example are:

- **Input:** 230 V_{AC} r.m.s ±15%, 50 Hz
- **Output Current:** 150 mA
- **LED String Voltage:** 88V - 122V

6.1 Power stage design

6.1.1 CALCULATING INPUT CURRENT

The maximum output power (P_{Omax}) can be computed as:

EQUATION 6-1:

$$P_{O,max} = V_{O,max} \cdot I_O = 122V \cdot 150\ mA = 18.3W$$

Assuming a sinusoidal input current wave-shape, the peak input current at the minimum input voltage and maximum output power can be computed to be:

EQUATION 6-2:

$$I_{IN,max,pk} = \frac{\sqrt{2} \cdot P_{O,max}}{V_{IN,min,rms} \cdot \eta} = \frac{\sqrt{2} \cdot 18.3W}{195.5V \cdot 0.85} = 156\ mA$$

where:

η = the assumed efficiency of the converter

6.1.2 SELECTING THE INDUCTOR

The typical inductor current waveform for a Boundary Conduction mode buck-boost converter is shown in Figure 5-2. Ignoring the dead-time, the peak input current can be expressed as a function of the peak inductor current.

EQUATION 6-3:

$$I_{IN,max,peak} = \frac{1}{2} \cdot I_{L,max,pk} \cdot \frac{T_{ON,max}}{T_{S,max}}$$

Since a Boundary Conduction mode converter has the same DC transfer function as a Continuous Conduction mode (CCM) converter, the ratio of the on-time to the switching frequency can be expressed as:

EQUATION 6-4:

$$\frac{T_{ON,max}}{T_{S,max}} = \frac{1}{1 + \frac{\sqrt{2} \cdot V_{IN,min,rms}}{V_{O,max}}} = \frac{1}{1 + \frac{\sqrt{2} \cdot 195.5V}{122V}} = 0.31$$

Combining Equations 6-2, 6-3 and 6-4:

EQUATION 6-5:

$$I_{L,max,pk} = 2 \cdot I_{IN,max,peak} \cdot \frac{T_{S,max}}{T_{ON,max}}$$

$$= 2 \cdot 156\ mA \cdot \frac{1}{0.31} = 1A$$

Assuming a minimum switching frequency of 30 kHz, the inductor value can be computed as:

EQUATION 6-6:

$$T_{ON,max} = \frac{T_{S,max}}{1 + \frac{\sqrt{2} \cdot V_{IN,min,rms}}{V_{O,max}}} = \frac{33.33\ \mu s}{1 + \frac{\sqrt{2} \cdot 195.5V}{122V}} = 10.2\ \mu s$$

EQUATION 6-7:

$$L_{BBT} = \frac{\sqrt{2} \cdot V_{IN,min,rms} \cdot T_{ON,max}}{I_{L,max,pk}}$$

$$= \frac{\sqrt{2} \cdot 195.5V \cdot 10.2\ \mu s}{1A} = 2.79\ mH$$

The inductor peak current has already been computed in Equation 6-5. The r.m.s current can be computed using:

EQUATION 6-8:

$$K_{IL} = \sqrt{\frac{(\sqrt{2} \cdot V_{IN,min,rms})^2}{8 \cdot V_{O,max}^2} + \frac{8 \cdot \sqrt{2} \cdot V_{IN,min,rms}}{9 \cdot \pi \cdot V_{O,max}} + \frac{1}{6}}$$

$$= \sqrt{\frac{(\sqrt{2} \cdot 195.5V)^2}{8 \cdot 122V^2} + \frac{8 \cdot \sqrt{2} \cdot 195.5V}{9 \cdot \pi \cdot 122V} + \frac{1}{6}}$$

$$= 1.204$$

EQUATION 6-9:

$$I_{L,rms} = K_{IL} \cdot \frac{4 \cdot V_{O,max} \cdot I_O}{n \cdot \sqrt{2} \cdot V_{IN,min,rms}}$$

$$= 1.204 \cdot \frac{4 \cdot 122V \cdot 0.15A}{0.85 \cdot (\sqrt{2} \cdot 195.5V)}$$

$$= 0.375A$$

6.1.3 SELECTING THE SWITCHING FET

The voltage rating of the switching FET should be:

EQUATION 6-10:

$$BV_{DSS,min} = 1.3 \cdot (\sqrt{2} \cdot V_{IN,max,rms} + V_{O,max})$$
$$= 1.3 \cdot (\sqrt{2} \cdot 264.5V + 122V) = 645V$$

A 650V rated switching FET should be chosen for this application.

The r.m.s current through the FET is:

EQUATION 6-11:

$$I_{Q,rms,max} =$$

$$\frac{4 \cdot V_{O,max} \cdot I_O}{n \cdot (\sqrt{2} \cdot V_{IN,min,rms})} \cdot \sqrt{\frac{1}{3} \cdot \left(\frac{4 \cdot (\sqrt{2} \cdot V_{IN,min,rms})}{3 \cdot \pi \cdot V_{O,max}} + \frac{1}{2} \right)} =$$

$$\frac{4 \cdot 122V \cdot 0.15A}{0.85 \cdot (\sqrt{2} \cdot 195.5)} \cdot \sqrt{\frac{1}{3} \cdot \left(\frac{4 \cdot (\sqrt{2} \cdot 195.5V)}{3 \cdot \pi \cdot 122V} + \frac{1}{2} \right)}$$

$$= 217.48\ mA$$

The Rds_{on} of the FET can be computed assuming a 3% power loss at maximum output power and minimum input voltage.

EQUATION 6-12:

$$Rds_{on,25C} = \frac{0.03 \cdot P_{O,max}}{1.5 \cdot I_{Q,rms}^2} = \frac{0.03 \cdot 18.3W}{1.5 \cdot 0.217^2} = 7.77\Omega$$

The 1.5 factor in the denominator is used to account for the higher FET resistance in actual operation due to higher junction temperature.

6.1.4 SELECTING THE SWITCHING DIODE

The voltage rating of the switching diode should match or exceed the voltage rating of the switching FET. A high-speed diode with reverse recovery time in the order of 50 ns should be chosen for this application. The peak, r.m.s and average current through the diode can be computed using the following equations:

EQUATION 6-13:

$$I_{DBBT,avg} = I_O = 0.15A$$

EQUATION 6-14:

$$K_{ID} = \sqrt{\frac{\sqrt{2} \cdot V_{IN,min,rms}}{3 \cdot V_{O,max}} \cdot \left(\frac{3 \cdot \sqrt{2} \cdot V_{IN,min,rms}}{8 \cdot V_{O,max}} + \frac{4}{3 \cdot \pi} \right)}$$

$$= \sqrt{\frac{\sqrt{2} \cdot 195.5V}{3 \cdot 122V} \cdot \left(\frac{3 \cdot (\sqrt{2} \cdot 195.5V)}{8 \cdot 122V} + \frac{4}{3 \cdot \pi} \right)}$$

$$= 0.981$$

EQUATION 6-15:

$$I_{DBBT,max,rms} = \frac{4 \cdot V_{O,max} \cdot I_O}{n \cdot \sqrt{2} \cdot V_{IN,min,rms}} \cdot K_{ID}$$

$$= \frac{4 \cdot 122V \cdot 0.15A}{0.85 \cdot \sqrt{2} \cdot 195.5V} \cdot 0.981 = 0.306A$$

EQUATION 6-16:

$$I_{DBBT,peak} = I_{L,max,pk} = 1.0A$$

6.1.5 CHOOSING THE OUTPUT CAPACITOR

The output capacitor is chosen based on the maximum allowable line frequency ripple in the LED current. This can be computed if the desired flicker index is known.

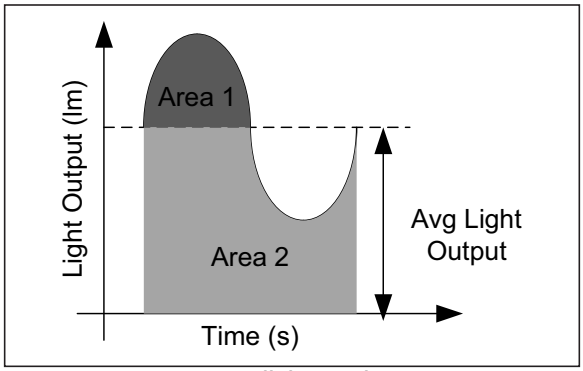


FIGURE 6-1: *Flicker Index.*

For a given instantaneous light output waveform (shown in Figure 6-1), the flicker index can be computed to be:

EQUATION 6-17:

$$FI = \frac{Area1}{(Area1) + (Area2)}$$

where:

Area1 = the area of the curve above the average

Area2 = the area of the curve below the average

Assuming that the instantaneous light output is directly proportional to the instantaneous LED current, the flicker index can be computed from the instantaneous LED current waveform shown in Figure 6-1.

EQUATION 6-18:

$$FI = \frac{\Delta I_O}{2 \cdot \pi \cdot I_O}$$

$$\Rightarrow \Delta I_O = 2 \cdot FI \cdot \pi \cdot I_O = 2 \cdot 0.15 \cdot \pi \cdot 0.15A = 0.14A$$

The typical LED string dynamic resistance can be computed as:

EQUATION 6-19:

$$R_{LED} = 0.05 \cdot \frac{V_{O,max}}{I_O} = 0.05 \cdot \frac{122V}{0.15A} = 40.67\Omega$$

The corresponding line frequency peak-to-peak ripple in the output voltage is:

EQUATION 6-20:

$$\Delta V_O = \Delta I_O \cdot R_{LED} = 0.14A \cdot 40.67\Omega = 5.69V$$

The output capacitor is usually dominated by the low-frequency ripple component. It can be computed using the following equation:

EQUATION 6-21:

$$C_O = \frac{I_O}{4 \cdot \pi \cdot f_L \cdot \Delta V_O} = \frac{0.15A}{4 \cdot \pi \cdot 50\,Hz \cdot 5.69V} = 42\mu F$$

Voltage rating of the output capacitor should be about 20% higher than the maximum output voltage.

EQUATION 6-22:

$$V_{CO} = 1.2 \cdot V_{O,max} = 1.2 \cdot 122V = 146V$$

The r.m.s current through the output capacitor is:

EQUATION 6-23:

$$I_{Co,rms} = \sqrt{I^2_{DBBT,max,rms} - I^2_O} = \sqrt{0.305A^2 - 0.15A^2} = 0.265A$$

6.1.6 SELECTING THE INPUT CAPACITOR

The input capacitor is selected to reduce the input ripple voltage. A simple first-pass selection can be computed as:

EQUATION 6-24:

$$C_{REC} = \frac{0.5 \cdot I_{L,max,pk} \cdot T_{ON,max}}{0.1 \cdot \sqrt{2} \cdot V_{IN,min,rms}} = \frac{0.5 \cdot 1A \cdot 10.2\mu s}{0.1 \cdot (\sqrt{2} \cdot 195.5V)} = 0.185\mu F$$

This capacitor will need to be adjusted in once a prototype is built. A large value will increase the THD where as a low value will affect the EMI performance.

6.2 Control Stage Design

6.2.1 SELECTING THE CURRENT SENSE RESISTOR

The current sense resistor value is set by the output current. The resistor's power rating is set by the inductor current.

EQUATION 6-25:

$$R_{CS} = \frac{CS_{REF}}{I_O} = \frac{0.2V}{0.15A} = 1.33\Omega$$

$$P_{Rcs} = I^2_{L,rms} \cdot R_{CS} = 0.375A^2 \cdot 1.33\Omega = 0.187W$$

6.2.2 SELECTING THE VALLEY SENSE COMPONENTS

The resistor used for detecting the valley is also used for over-voltage protection. Hence, the resistor should be chosen based on the over-voltage setting desired.

Assume a 10% headroom over the maximum output voltage to set the minimum over-voltage threshold. Then, the resistor is:

EQUATION 6-26:

$$R_{VD} = \frac{1.1 \cdot V_{O,max} - V_{IND}}{I_{OCP,min}} = \frac{1.1 \cdot 122V - 4.3V}{350\mu A} = 371k\Omega$$

Then maximum output voltage that can occur during over-voltage conditions is:

EQUATION 6-27:

$$OVP_{max} = I_{OCP,max} \cdot R_{VD} + V_{IND} = 550\mu A \cdot 371k\Omega + 4.3V = 208V$$

Note that since this is not a continuous operation, the voltage rating of the output capacitor should be chosen to withstand this voltage, but not to operate at this voltage continuously.

The diode in series with this resistor should be a 500 µA switching diode with a breakdown voltage of at least 400V (250V for a HV98100 design).

6.2.3 SELECTING THE START-UP NETWORK

The start-up resistor should be chosen based on the maximum start-up time that is allowable before the GATE starts switching. Note that selecting a shorter start-up time will cause higher losses in the resistor during operation. The start-up time and power loss should be iterated until a reasonable compromise is achieved for both parameters.

The minimum capacitor at PV_{DD} required is 4.7 µF. In most cases this capacitor value is sufficient for hold-up.

Assuming a 100 ms start-up time (T_{STRT}), the start-up resistor can be computed as shown in Equation 6-28.

EQUATION 6-28:

$$R_{HV} = \frac{\sqrt{2} \cdot V_{in,min,rms} - V_{DD,ON}}{\frac{C_{PVDD} \cdot V_{DD,ON}}{T_{STRT}} + 200\mu A} = \frac{\sqrt{2} \cdot 195.5V - 16V}{\frac{4.7\mu F \cdot 16V}{100ms} + 200\mu A} = 273k\Omega$$

The maximum power loss in the resistor occurs at high line and is shown in Equation 6-29.

EQUATION 6-29:

$$P_{RHV,max} = \frac{\sqrt{2} \cdot V_{in,max,rms} \cdot (4 \cdot V_{O,max} + \pi \cdot \sqrt{2} \cdot V_{in,max,rms})}{2 \cdot \pi \cdot R_{HV}}$$

$$= \frac{\sqrt{2} \cdot 264.5V \cdot (4 \cdot 122V + \pi \cdot \sqrt{2} \cdot 264.5V)}{2 \cdot \pi \cdot 273k\Omega} = 0.363W$$

The minimum average current supplied by RHV during operation is shown in Equation 6-30.

EQUATION 6-30:

$$I_{RHV,min,avg} = \frac{2 \cdot \sqrt{2} \cdot V_{in,min,rms}}{\pi \cdot R_{HV}} = \frac{2 \cdot \sqrt{2} \cdot 195.5V}{\pi \cdot 273k\Omega} = 645\mu A$$

The diode in the start-up network (D_{HV}) can be a simple 1N4148.

6.2.4 SELECTING BOOTSTRAP COMPONENTS

The total current required by the IC during normal operation comes from two sources

- Current through R_{HV}
- Current through R_{PVDD}

The current through R_{HV} resistor has been computed in Equation 6-28. The average current supplied through R_{PVDD} is:

EQUATION 6-31:

$$I_{RPVDD,AVG} = \frac{1}{\pi} \cdot \int_0^{\pi} \left(\frac{V_O - PV_{DD}}{R_{PVDD}} \cdot \frac{\hat{V}_{IN} \cdot \sin\theta}{V_O + \hat{V}_{IN} \cdot \sin\theta} \right) d\theta$$

However, the closed form solution for the integral in Equation 6-31 is very complex. The equation can be simplified using a curve fit solution.

EQUATION 6-32:

$$I_{RPVDD_{AVG}} = \frac{V_O - PV_{DD}}{R_{PVDD}} \cdot \left(0.193 \cdot ln\left(\frac{\hat{V}_{IN}}{V_O} \right) + 0.3801 \right)$$

This approximation is valid as long as

$$2 \le \frac{\hat{V}_{IN}}{V_O} \le 10$$

Assuming we need a total current of about 4 mA during normal operation, the R_{PVDD} resistor can be chosen as:

EQUATION 6-33:

$$R_{PVDD} = \frac{V_{O,min} - PV_{DD}}{(I_{PVDD} - I_{RHV})} \cdot \left(0.193 \cdot ln\left(\frac{\hat{V}_{IN}}{V_{O,min}}\right) + 0.3801\right)$$

$$= \frac{88V - 16V}{(4\,mA - 645\,\mu A)} \cdot \left(0.193 \cdot ln\left(\frac{\sqrt{2} \cdot 195.5V}{88V}\right) + 0.3801\right)$$

$$= 12k\Omega$$

The power dissipated in the R_{PVDD} resistor can be computed as:

EQUATION 6-34:

$$I_{RPVDD,rms} = \frac{V_O - PV_{DD}}{R_{PVDD}} \cdot \sqrt{\left(0.193 \cdot ln\left(\frac{\hat{V}_{IN}}{V_o}\right) + 0.3801\right)}$$

$$= \frac{88V - 16V}{12.9k\Omega} \cdot \sqrt{\left(0.193 \cdot ln\left(\frac{\sqrt{2} \cdot 195.5V}{88V}\right) + 0.3801\right)}$$

$$= 4.33\,mA$$

$$P_{RPVDD} = I^2_{RPVDD,rms} \cdot R_{PVDD}$$

$$= 4.33\,mA^2 \cdot 12.9\,k\Omega = 0.242W$$

The average current drawn by the IC is not easy to estimate. It is recommended to start with an assumed higher value for the current consumed by the IC (4 mA-5 mA) and increase R_{PVDD} by trial and error.

The bootstrap diode should have a voltage rating of at least 400V (at least 250V for an HV98100 design) and an average current rating of about 5 mA. This should be a switching diode with a very low-junction capacitance (< 10 pF preferable).

6.2.5 CHOOSING THE COMPENSATION CAPACITOR

The compensation capacitor serves two functions in a power factor correction circuit:

- maintain loop stability
- reduce third harmonic distortion in the input current.

The capacitor can be chosen based on either criteria. For this design example, the capacitor is chosen based on the third harmonic distortion criterion. This criterion leads to a larger compensation capacitor value which also ensures stability in most cases.

The second harmonic component of the COMP voltage causes third harmonic distortion in the input current. The criterion used to design the compensation capacitor is that the second harmonic peak-to-peak voltage in COMP voltage is 2% of the DC component of the COMP voltage.

Equation 6-35 shows the relation between the input current and the DC component of the COMP voltage.

EQUATION 6-35:

$$I_{IN,\,rms,\,max} = \frac{1}{2} \cdot \frac{V_{IN,\,rms,\,min}}{L} \cdot \frac{2 \cdot K_T \cdot COMP}{V_{TREF}}$$

Substituting values in Equation 6-35:

EQUATION 6-36:

$$COMP = \frac{2 \cdot 2.79mH \cdot 110\,mA \cdot 2.5V}{2 \cdot 195.5V \cdot 1.25\,\mu s} = 3.14V$$

The compensation capacitor can be computed as:

EQUATION 6-37:

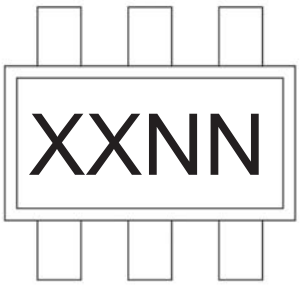
$$C_{COMP} = \frac{\Delta I_O \cdot R_{CS} \cdot g_m}{2 \cdot (2 \cdot \pi \cdot f_L) \cdot \Delta V_{COMP}} = \frac{0.14A \cdot 1.3\Omega \cdot 230\mu\frac{A}{V}}{2 \cdot (2 \cdot \pi \cdot 50\,Hz) \cdot 0.06V} = 1.11\mu F$$

Note: The design of the EMI filter is beyond the scope of this design example. The design example is intended to provide a first pass design that can be further optimized in hardware.

7.0 PACKAGING INFORMATION

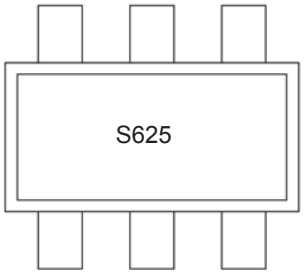
7.1 Package Marking Information

6-Lead, SOT-23
(**HV98100/HV98101**)



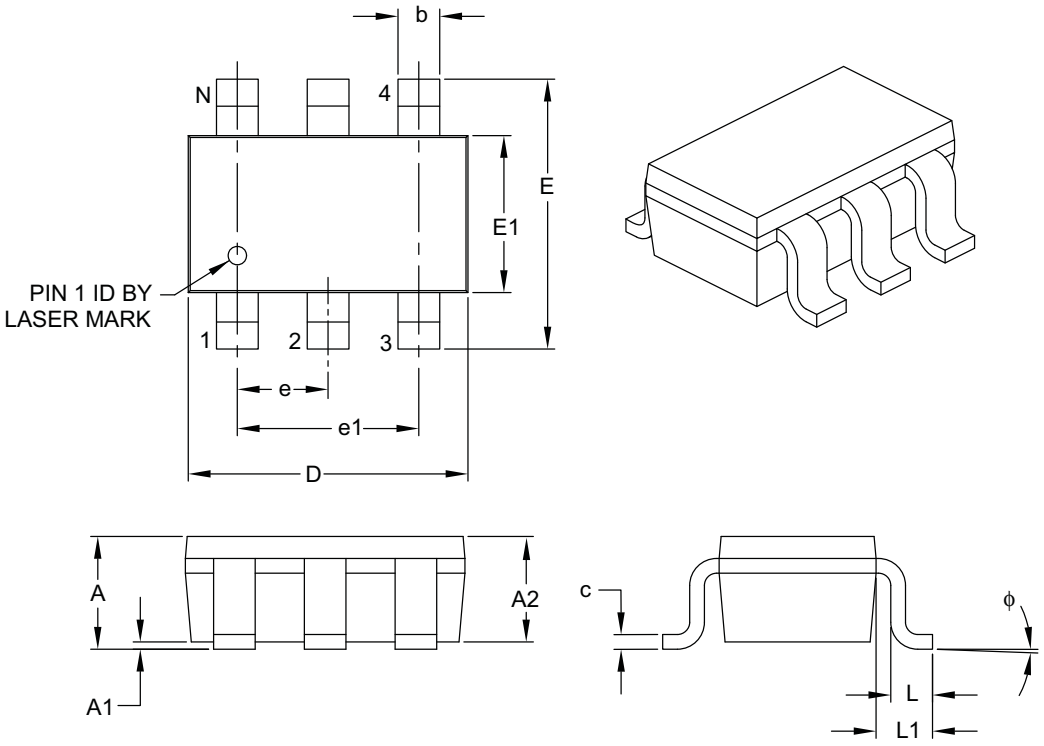
Product Number	Code
HV98100T-E/CH	S6NN
HV98101T-E/CH	S7NN

Example



6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

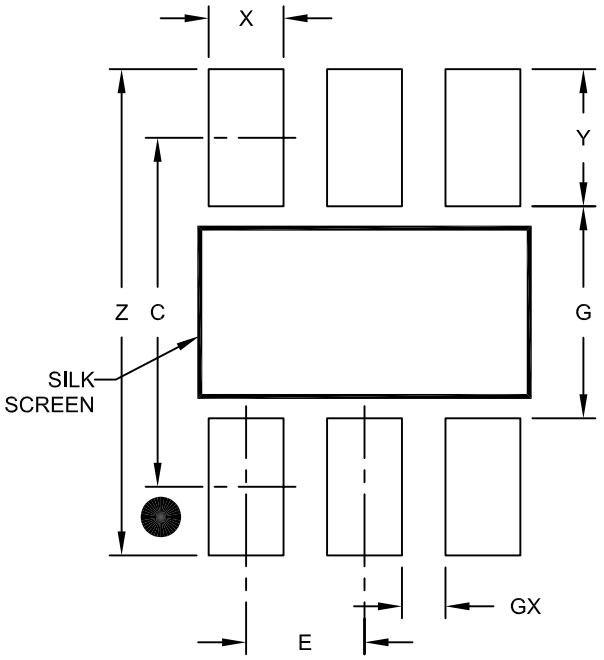
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2016)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	HV98100 =	Off-line, high-power factor, buck-boost controller
	HV98101 =	Off-line, high-power factor, buck-boost controller
Tape and Reel Option:	T =	Tape and Reel(1)
Temperature Range:	E =	-40°C to+125°C(Extended)
Package:	CH =	Plastic Small Outline Transistor

Examples:

a) HV98100T-E/CH: Tape and Reel, Extended Temperature, 6LD SOT-23 package

b) HV98101T-E/CH: Tape and Reel, Extended Temperature, 6LD SOT-23 package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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