KSZ8041TL/FTL

10Base-T/100Base-TX/100Base-FX Physical Layer Transceiver

Evaluation Board User's Guide

Revision 1.1 / May 2007

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Revision History

Revision	Date	Summary of Changes
1.0	4/5/07	Initial Release
1.1	5/24/07	Added 100pF capacitor (C54) to BOM.

Table of Contents

List of Figures

List of Tables

1.0 Introduction

The KSZ8041TL is a 10Base-T/100Base-TX Physical Layer Transceiver with MII, RMII, and SMII MAC interfaces, and Micrel LinkMD® TDR-based cable diagnostics for identification of faulty copper cabling. It utilizes a unique mixed-signal design to extend signaling distance while reducing power consumption, and offers HP Auto MDI/MDI-X for reliable detection of and correction for crossover and straight-through cables, eliminating the need to differentiate between crossover and straight-through cables.

The KSZ8041FTL has all the identical rich features of the KSZ8041TL plus 100Base-FX support for fiber and media converter applications.

The KSZ8041TL/FTL Eval Board (KSZ8041TL/FTL-EVAL) provides a convenient platform to evaluate the KSZ8041TL/FTL features. All KSZ8041TL/FTL configuration pins are accessible either by jumpers, test points or interface connectors.

2.0 Board Features

- Micrel KSZ8041TL/FTL 10Base-T/100Base-TX/100Base-FX Physical Layer Transceiver
- RJ-45 Jack for Fast Ethernet cable interface
- HP Auto-MDIX for automatic detection and correction for straight-through and crossover cables
- 1x9 SIP Socket for 100Base-FX Fiber Module (KSZ8041FTL only)
- MII (Media Independent Interface) Connector to interface with a MAC controller
- RMII (Reduced MII) option using MII Connector
- 2 LED Indicators for status and activity
- Jumpers to configure strapping pins
- Manual Reset Button for quick reboot after re-configuration of strapping pins

3.0 Evaluation Kit Contents

The KSZ8041TL/FTL Evaluation Kit includes the following hardware:

- KSZ8041TL/FTL Evaluation Board

A design package with the following collaterals that can be downloaded from Micrel's website at http://www.micrel.com

- KSZ8041TL/FTL Eval Board Schematic (PDF and OrCAD DSN file)
- KSZ8041NL_TL-FTL Eval Boards Gerber Files (PDF version included)
- KSZ8041TL/FTL Eval Board User's Guide (this document)
- KSZ8041TL IBIS Model
- KSZ8041FTL IBIS Model

and the KSZ8041TL/FTL Datasheet which is also available from Micrel's website.

4.0 Hardware Description

The KSZ8041TL/FTL-EVAL (Figure 1) comes in a compact form factor and plugs directly into industry standard test equipment such as Spirent SmartBits, or other boards with Ethernet MACs that expose the MII interface. Configuration of the KSZ8041TL/FTL is accomplished through on-board jumper selections and/or by PHY register access via the MDC/MDIO management pins of the MII Interface.

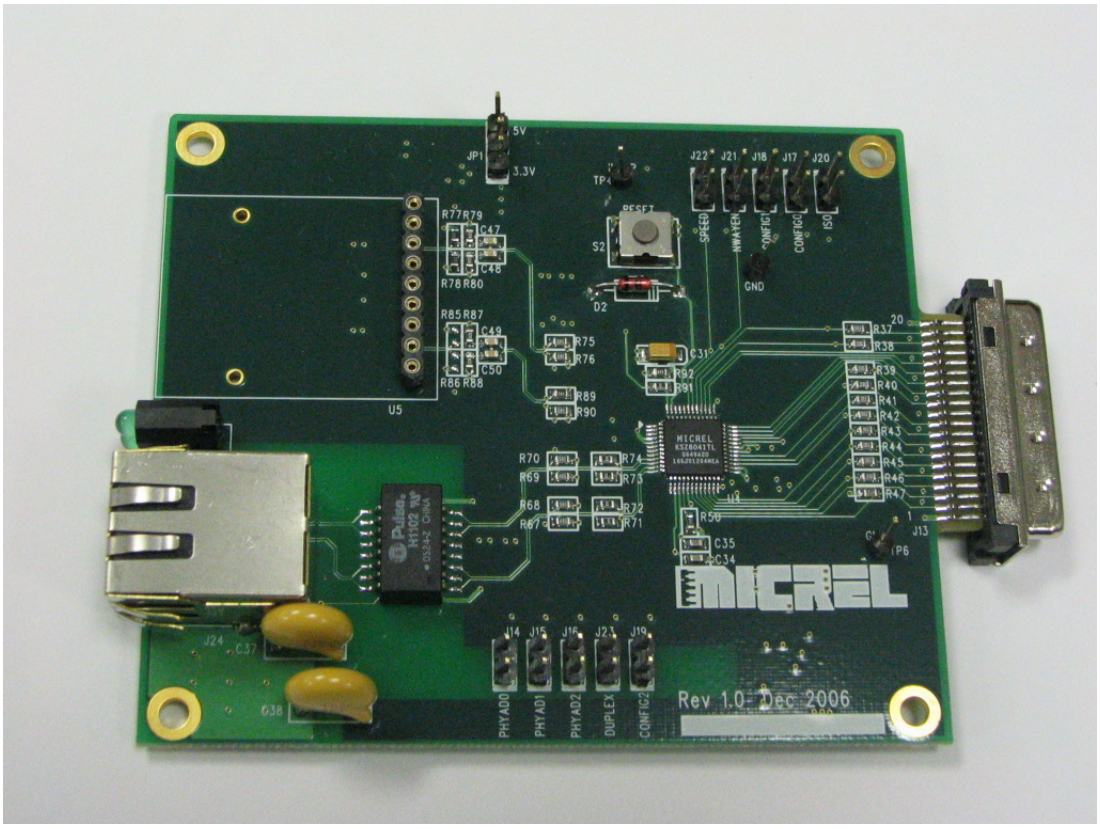

Figure 1. KSZ8041TL/FTL Evaluation Board (copper mode)

Features include a RJ-45 Jack for Fast Ethernet cable connection, programmable LED indicators for reporting link status and activity, and a manual reset button for quick reboot after re-configuration of strapping pins.

The KSZ8041TL/FTL-EVAL receives +5V DC input power through its MII connector.

For 100Base-FX (KSZ8041FTL only), an 1x9 SIP Socket allows the Fiber Module under test to be inserted and removed quickly. Figure 2 shows the KSZ8041TL/FTL-EVAL in fiber mode with an Agilent HFBR-5803 Fiber Module.

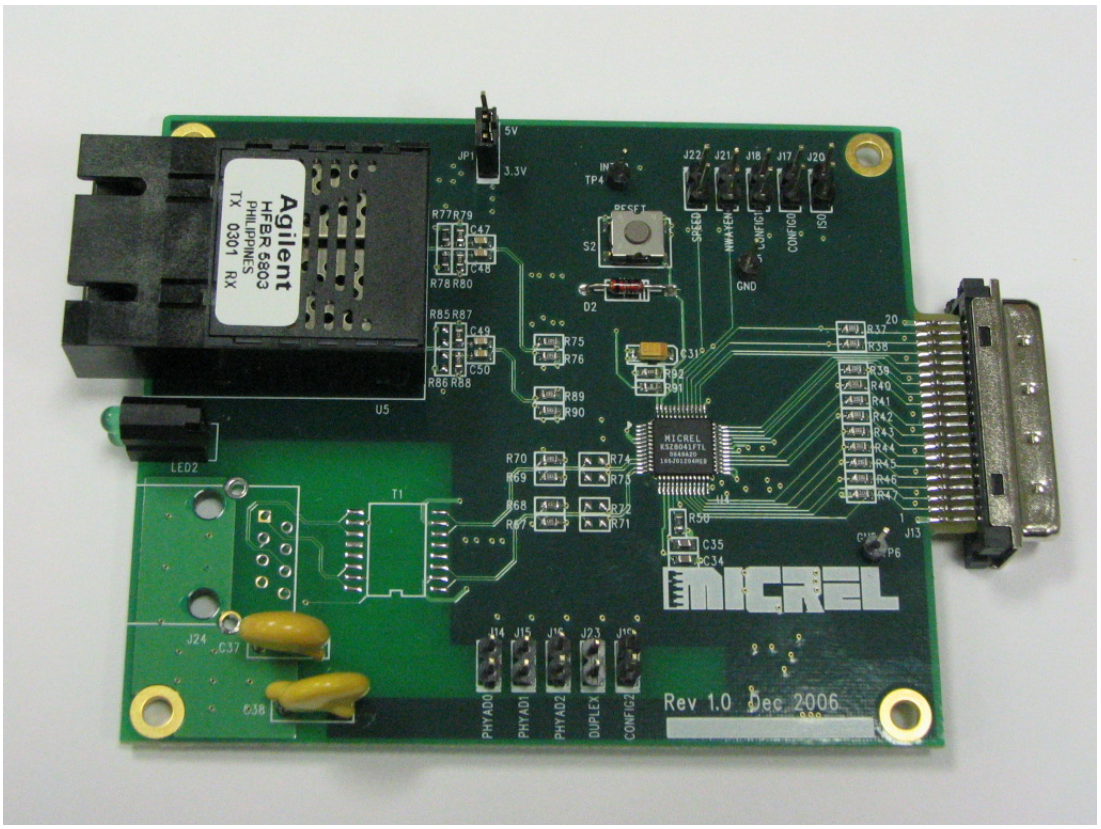

Figure 2. KSZ8041TL/FTL Evaluation Board (fiber mode)

4.1 MII (Media Independent Interface)

The KSZ8041TL/FTL-EVAL receives power and accesses MII data and management information from the MII connector, J13. Figure 3 shows the MII interface connection with Spirent SmartBits.

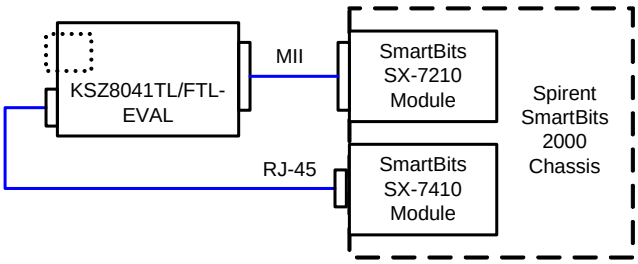

Figure 3. KSZ8041TL/FTL-EVAL MII Interface Connection with Spirent SmartBits

Connections with other boards that also expose the MII interface are possible. Figure 4 shows the KSZ8041TL/FTL-EVAL connected to the Micrel KSZ8893MQL Evaluation Board.

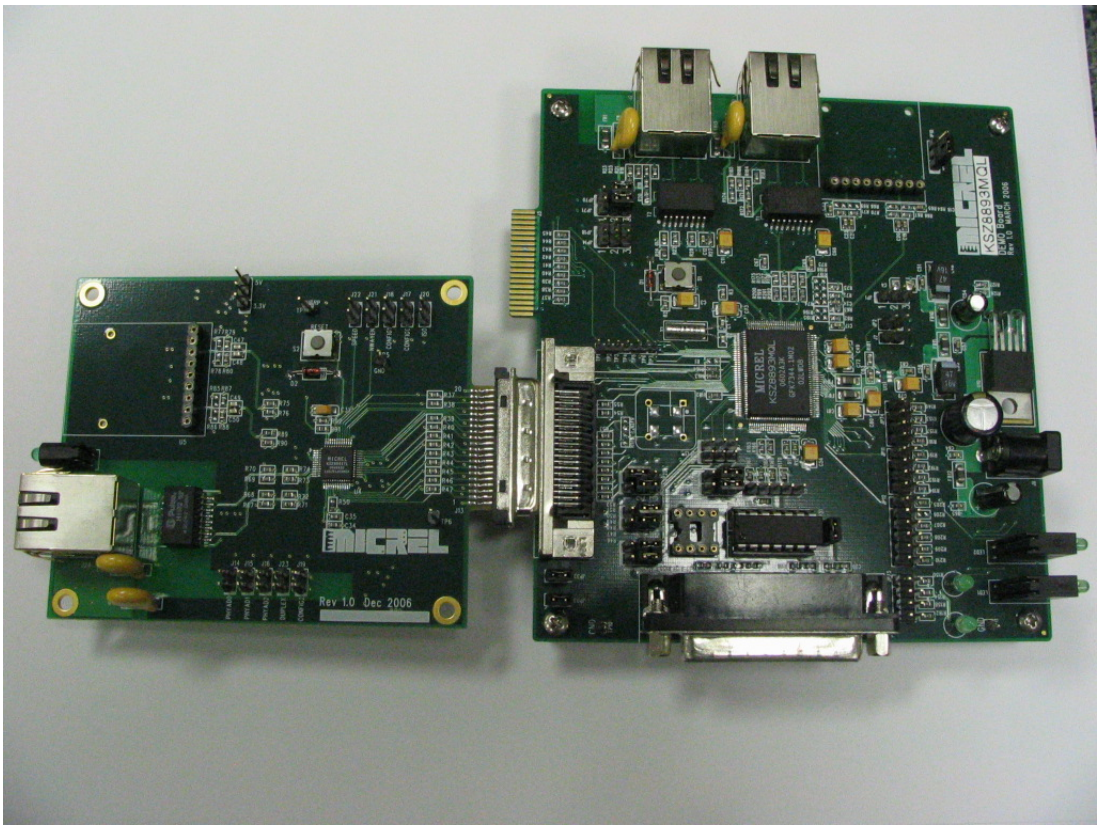

Figure 4. KSZ8041TL/FTL-EVAL interfacing with KSZ8893MQL Evaluation Board

The MII interface is defined by Clause 22 of the IEEE 802.3 Specification. MII Management (MIIM) is conducted thru pins MDC (clock line) and MDIO (data line). MIIM allows upper-layer devices to monitor and control the states of the KSZ8041TL/FTL. An external device with MDC/MDIO capability can be used to read the PHY status or configure the PHY registers. The MIIM frame format and timing information can be found in the KSZ8041TL/FTL Datasheet and in Clause 22 of the IEEE 802.3 Specification.

The KSZ8041TL/FTL-EVAL has a 40-pin male edge connector that interfaces with and plugs directly into the SmartBits SX-7210 Module or other Fast Ethernet MAC boards with the mating AMP 787170-4 (40-pin, right angle, female) connector. Table 1 lists the pin outs for the MII interface on connector J13.

Pin #	Signal	Pin #	Signal
1	+5V	21	+5V
2	MDIO	22	Ground
3	MDC	23	Ground
4	RXD3	24	Ground
5	RXD2	25	Ground
6	RXD1	26	Ground
7	RXD0	27	Ground
8	RXDV	28	Ground
9	RXCLK	29	Ground
10	RXER	30	Ground
11	TXER	31	Ground
12	TXCLK	32	Ground
13	TXEN	33	Ground
14	TXD0	34	Ground
15	TXD1	35	Ground
16	TXD2	36	Ground
17	TXD3	37	Ground
18	COL	38	Ground
19	CRS	39	Ground
20	+5V	40	+5V

Table 1. Connector J13 - MII Pin Definition

4.1.1 RMII (Reduced Media Independent Interface) Option

The KSZ8041TL/FTL-EVAL can use its 40-pin male edge connector (J13) with some minor board population changes to interface with RMII MACs. Like MII mode, the KSZ8041TL/FTL-EVAL receives power and accesses RMII data and management information via connector J13 in RMII mode.

Figure 4 shows the KSZ8041TL/FTL-EVAL interfacing with the KSZ8893MQL Evaluation Board in MII mode. Alternatively, both KSZ8041TL/FTL and KSZ8893MQL devices can be configured to RMII mode and interface with each other using the same J13 connector interface. For this setup, the RMII 50MHz reference clock is sourced from the KSZ8893MQL Evaluation Board side. Refer to KSZ8893MQL Eval Board Schematic for additional population changes on the KSZ8893MQL side. For the KSZ8041TL/FTL-EVAL side, the board changes to support RMII mode are as follows:

1. Remove crystal circuit (Y2, C34, C35) and TXC clock termination (R39).
2. Populate R49 with 0 Ohm and R48 with 33 Ohm to connect RMII 50MHz reference clock (provided by MAC side via J13 pin 12) to U4 pin 15 (XI input).
3. Select RMII mode by setting strapping pins CONFIG[2:0] to '001'.

These board changes can also be found in the KSZ8041TL/FTL Eval Board Schematic.

Table 2 lists the pin outs for the RMII interface on connector J13.

Pin #	Signal	Pin #	Signal
1	+5V	21	+5V
2	MDIO	22	Ground
3	MDC	23	Ground
4	<not used>	24	Ground
5	<not used>	25	Ground
6	RXD[1]	26	Ground
7	RXD[0]	27	Ground
8	CRSDV	28	Ground
9	<not used>	29	Ground
10	RXER	30	Ground
11	<not used>	31	Ground
12	REF_CLK	32	Ground
13	TXEN	33	Ground
14	TXD0	34	Ground
15	TXD1	35	Ground
16	<not used>	36	Ground
17	<not used>	37	Ground
18	<not used>	38	Ground
19	<not used>	39	Ground
20	+5V	40	+5V

Table 2. Connector J13 - RMII Pin Definition

4.2 Jumper Setting & Definition

The KSZ8041TL/FTL-EVAL does not require any jumper for normal operation. At power-up, the KSZ8041TL/FTL is configured using the chip's internal pull-up and pull-down resistors with its default strapping pin values. Jumpers are provided to override the default settings, allowing for quick configuration and re-configuration of the board. To override the default settings, simply select and close the desired jumper setting(s) and toggle the on-board manual reset button (S2) for the new setting(s) to take effect.

The KSZ8041TL/FTL-EVAL jumper settings are defined in Table 3 below.

<table>
<tr><th>Jumper</th><th>Definition</th><th>Open (default)</th><th>Close</th></tr>
<tr><td>J14</td><td>PHYAD0</td><td>1</td><td>0</td></tr>
<tr><td>J15</td><td>PHYAD1</td><td>0</td><td>1</td></tr>
<tr><td>J16</td><td>PHYAD2</td><td>0</td><td>1</td></tr>
<tr><td>J17</td><td>CONFIG0</td><td colspan="2" rowspan="3"><table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>[open, open, open]</td><td>MII (default)</td></tr><tr><td>[open, open, close]</td><td>RMII</td></tr><tr><td>[close, open, open]</td><td>PCS Loopback</td></tr></table>All other CONFIG[2:0] settings not listed are reserved or not used by the KSZ8041TL/FTL-EVAL.</td></tr>
<tr><td>J18</td><td>CONFIG1</td></tr>
<tr><td>J19</td><td>CONFIG2</td></tr>
<tr><td>J20</td><td>Isolate Mode</td><td>Disable</td><td>Enable</td></tr>
<tr><td>J21</td><td>Auto-Negotiation

(see also Table 4 for KSZ8041FTL pin function)</td><td>Enable</td><td>Disable</td></tr>
<tr><td>J22</td><td>Forced Speed

(see also Table 4 for KSZ8041FTL pin function)</td><td>100Base-TX</td><td>10Base-T</td></tr>
<tr><td>J23</td><td>Forced Duplex</td><td>Half</td><td>Full</td></tr>
</table>

Table 3. KSZ8041TL/FTL-EVAL Jumper Definition

Table 4 lists the strapping pin definitions for the KSZ8041TL/FTL-EVAL jumpers.

<table>
<tr><th>Jumper</th><th>Pin</th><th>Pin Name</th><th>Pin Function</th></tr>
<tr><td>J16
J15
J14</td><td>22
21
20</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7.
The default PHY Address is 00001.
PHY Address bits [4:3] are always set to '00'.</td></tr>
<tr><td>J19
J18
J17</td><td>27
41
40</td><td>CONFIG2
CONFIG1
CONFIG0</td><td>The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows:
<table><tr><td>CONFIG[2:0]</td><td>Mode</td></tr><tr><td>000</td><td>MII (default)</td></tr><tr><td>001</td><td>RMII</td></tr><tr><td>100</td><td>PCS Loopback</td></tr></table>All other CONFIG[2:0] settings not listed are reserved or not used by the KSZ8041TL/FTL-EVAL.</td></tr>
<tr><td>J20</td><td>29</td><td>ISO</td><td>ISOLATE mode
Pull-up = Enable
Pull-down (default) = Disable
During power-up / reset, this pin value is latched into register 0h bit 10.</td></tr>
<tr><td>J22

(TL device)</td><td>43</td><td>SPEED</td><td>SPEED mode
Pull-up (default) = 100Mbps
Pull-down = 10Mbps
During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.</td></tr>
<tr><td>J22

(FTL device)</td><td>43</td><td>SPEED

no FEF</td><td>If copper mode (FXEN=0), pin strap-in is SPEED mode.
Pull-up (default) = 100Mbps
Pull-down = 10Mbps
During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.

If fiber mode (FXEN=1), pin strap-in is no FEF.
Pull-up (default) = Enable Far-End Fault
Pull-down = Disable Far-End Fault
This pin value is latched during power-up / reset.</td></tr>
<tr><td>J23</td><td>23</td><td>DUPLEX</td><td>DUPLEX mode
Pull-up (default) = Half Duplex
Pull-down = Full Duplex
During power-up / reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.</td></tr>
</table>

Jumper	Pin	Pin Name	Pin Function
J21 **(TL device)**	42	NWAYEN	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up / reset, this pin value is latched into register 0h bit 12.
J21 **(FTL device)**	42	NWAYEN	If copper mode (FXEN=0), pin strap-in is Nway Auto-Negotiation Enable. Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up / reset, this pin value is latched into register 0h bit 12. If fiber mode (FXEN=1), this pin configuration is always strapped to disable Auto-Negotiation.

Table 4. Strapping Pin Definitions for KSZ8041TL/FTL-EVAL Jumpers

4.3 Test Point Definition

The KSZ8041TL/FTL-EVAL has three test points. They are defined in the following table.

Test Point	Definition
TP4	Interrupt Signal (pin 32) with external pull-up
TP5	Signal Ground
TP6	Signal Ground

Table 5. KSZ8041TL/FTL-EVAL Test Point Definition

4.4 Cable Interface

The KSZ8041TL/FTL-EVAL has the option to interface with either copper cable or fiber cable. Resistors are used to select between the two cable types. Table 6 shows the KSZ8041TL/FTL-EVAL population options to select copper or fiber mode.

Cable Mode	Populate	Do not populate
Copper	R71 : 0 Ohm R72 : 0 Ohm R73 : 0 Ohm R74 : 0 Ohm	R81 R82 R83 R84
Fiber	R81 : 0 Ohm R82 : 0 Ohm R83 : 0 Ohm R84 : 0 Ohm	R71 R72 R73 R74

Table 6. KSZ8041TL/FTL-EVAL Copper/Fiber Mode Selection

These board changes can also be found in the KSZ8041TL/FTL Eval Board Schematic.

4.4.1 Copper Port

The RJ-45 Connector (J24) connects to standard CAT-5 Ethernet cable to interface with 10Base-T/100Base-TX Ethernet devices.

J24 also supports Auto-MDIX and Auto-Negotiation / Forced Modes.

4.4.2 Fiber Port (KSZ8041FTL only)

The industry standard 1x9 SIP socket (U5) connects to 100Base-FX Fiber Modules with the same form factor. The socket allows the Fiber Modules to be inserted and removed quickly.

The KSZ8041FTL device can interface with LVPECL and PECL Fiber Modules. Jumper JP1 is set to 3.3V (pins 1 and 2 closed) for LVPECL, and set to 5V (pins 2 and 3 closed) for PECL. By default, the fiber port termination resistors are populated with LVPECL values. Refer to KSZ8041TL/FTL Eval Board Schematic for termination resistor values to support PECL.

4.5 LED Indicators

A dual LED indicator (LED2) is located between the RJ-45 Connector and Fiber Module. The top LED and bottom LED are connected to LED1 (pin 43) and LED0 (pin 42) of the KSZ8041TL/FTL, respectively.

The two LEDs are programmable to LED mode '00' or '01' via register 1Eh bits [15:14], and are defined in the following table.

<table>
<tr><th>LED Mode</th><th>LED1 (pin 43)</th><th>LED0 (pin 42)</th></tr>
<tr><td>00</td><td>
<table>
<tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>10BT</td><td>H</td><td>OFF</td></tr>
<tr><td>100BT</td><td>L</td><td>ON</td></tr>
</table>
</td><td>
<table>
<tr><th>Link/ Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>
</td></tr>
<tr><td>01</td><td>
<table>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity</td><td>L</td><td>ON</td></tr>
</table>
</td><td>
<table>
<tr><th>Link</th><th>Pin State</th><th>Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
</table>
</td></tr>
<tr><td>10</td><td>Reserved – not used</td><td>Reserved – not used</td></tr>
<tr><td>11</td><td>Reserved – not used</td><td>Reserved – not used</td></tr>
</table>

Table 7. KSZ8041TL/FTL-EVAL LED Definition

5.0 Bill of Materials

KSZ8041TL/FTL Eval Board
Revision 1.0

Item	Quantity	Reference	Description	Package
1	2	C20,C21	47uF / Tantalum	C-size
2	3	C18,C19,C32	22uF / Tantalum	B-size
3	22	C22,C23,C24,C25,C27,C28 C29,C30,C33,C39,C40,C41 C43,C44,C45,C46,C47,C48 C49,C50,C51,C52	0.1uF	0603
4	3	C26,C31,C36	10uF / Tantalum	A-size
5	2	C37,C38	1000pF / 2kV	radial lead
6	2	C34,C35	22pF	0603
7	1	C42	47uF / 16V Tantalum	C-size
8	1	C54	100pF	0603
9	1	D2	1N4148	DO-35 / axial lead
10	5	FB2,FB3,FB4,FB5,FB6	Ferrite Bead	1206
11	1	JP1	Header 3X1	thru hole / 0.1" pitch
12	1	J13	Male MII Connector	
13	10	J14,J15,J16,J17,J18,J19 J20,J21,J22,J23	Header 2X1	thru hole / 0.1" pitch
14	1	J24	RJ-45 Jack	
15	1	LED2	LEDx2 / Green	thru hole / 0.1" pitch
16	1	R34	100K	0603
17	1	R35	10K	0603
18	8	R36,R47,R53,R55,R56,R57, R58,R59	4.7K	0603
19	10	R37,R38,R39,R40,R41,R42, R43,R44,R45,R46	33	0603
20	8	R67,R68,R69,R70,R75,R76, R89,R90	49.9	0603
21	8	R48,R49,R81,R82,R83,R84, R85,R86	NC	0603
22	1	R50	6.49K	0603
23	2	R52,R54	220	0603
24	4	R51,R60,R61,R62	1K	0603
25	4	R63,R64,R65,R66	75	0603
26	5	R71,R72,R73,R74,R91	0	0603
27	2	R77,R78	82	0603

Item	Quantity	Reference	Description	Package
28	5	R79,R80,R87,R88,R92	130	0603
29	1	S2	SW PUSHBUTTON	SMT
30	3	TP4,TP5,TP6	TestPoint	thru hole / 0.1" pitch
31	1	T1	Pulse H1102	
32	1	U3	MIC5216-3.3BM5	SOT-23-5
33	1	U4	KSZ8041TL-FTL	48-pin TQFP
34	1	U5	HFBR-5803	1x9/SC/SIP
35	1	Y2	25MHz +/-50ppm	cylinder

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