KSZ8463ML/RL/FML/FRL

IEEE 1588 Precision Time Protocol-Enabled, Three-Port, 10/100 Managed Switch with MII or RMII

Features

Management Capabilities

- The KSZ8463ML/RL/FML/FRL Includes All the Functions of a 10/100BASE-T/TX/FX Switch System that Combines a Switch Engine, Frame Buffer Management, Address Look-Up Table, Queue Management, MIB Counters, Media Access Controllers (MAC) and PHY Transceivers
- Non-Blocking Store-and-Forward Switch Fabric Ensures Fast Packet Delivery by Utilizing 1024 Entry Forwarding Table
- Port Mirroring/Monitoring/Sniffing: Ingress and/or Egress Traffic to any Port
- MIB Counters for Fully Compliant Statistics Gathering: 34 Counters per Port
- Loopback Modes for Remote Failure Diagnostics
- Rapid Spanning Tree Protocol Support (RSTP) for Topology Management and Ring/Linear Recovery
- Bypass Mode Ensures Continuity Even When a Host is Disabled or Fails

Robust PHY Ports

- Two Integrated IEEE 802.3/802.3u-Compliant Ethernet Transceivers Supporting 10BASE-T and 100BASE-TX
- Copper and 100BASE-FX Fiber Mode Support in the KSZ8463FML and KSZ8463FRL
- Copper Mode Support in the KSZ8463ML and KSZ8463RL
- On-Chip Termination Resistors and Internal Biasing for Differential Pairs to Reduce Power
- HP Auto MDI/MDI-X Crossover Support Eliminates the Need to Differentiate Between Straight or Crossover Cables in Applications

MAC Ports

- Three Internal Media Access Control (MAC) Units
- MII or RMII Interface Support on MAC Port 3
- 2Kbyte Jumbo Packet Support
- Tail Tagging Mode (One byte Added before FCS) Support at Port 3 to Inform The Processor Which Ingress Port Receives the Packet and its Priority
- Supports Reduced Media Independent Interface (RMII) with 50 MHz Reference Clock Input or Output
- Supports Media Independent Interface (MII) in Either PHY Mode or MAC Mode on Port 3
- Programmable MAC Addresses for Port 1 and Port 2 and Source Address Filtering for Implementing Ring Topologies
- MAC Filtering Function to Filter or Forward Unknown Unicast Packets
- Port 1 and Port 2 MACs Programmable as Either E2E or P2P Transparent Clock (TC) Ports for 1588 Support
- Port 3 MAC Programmable as Slave or Master of Ordinary Clock (OC) Port for 1588 Support
- Microchip LinkMD® Cable Diagnostic Capabilities for Determining Cable Opens, Shorts, and Length

Advanced Switch Capabilities

- Non-Blocking Store-and-Forward Switch Fabric Ensures Fast Packet Delivery by Utilizing 1024 Entry Forwarding Table
- IEEE 802.1Q VLAN for Up to 16 Groups with Full Range of VLAN IDs
- IEEE 802.1p/Q Tag Insertion or Removal on a per Port Basis (Egress) and Support Double-Tagging
- VLAN ID Tag/Untag Options on per Port Basis
- Fully Compliant with IEEE 802.3/802.3u Standards
- IEEE 802.3x Full-Duplex with Force-Mode Option and Half-Duplex Backpressure Collision Flow Control
- IEEE 802.1w Rapid Spanning Tree Protocol Support
- IGMP v1/v2/v3 Snooping for Multicast Packet Filtering
- QoS/CoS Packets Prioritization Support: 802.1p, DiffServ-Based and Re-Mapping of 802.1p Priority Field per Port Basis on Four Priority Levels
- IPv4/IPv6 QoS Support
- IPv6 Multicast Listener Discovery (MLD) Snooping Support
- Programmable Rate Limiting at the Ingress and Egress Ports
- Broadcast Storm Protection
- Bypass Mode to Sustain the Switch Function between Port 1 and Port 2 when CPU (Port 3) Goes into Sleep Mode
- 1K Entry Forwarding Table with 32K Frame Buffer
- Four Priority Queues with Dynamic Packet Mapping for IEEE 802.1p, IPv4 TOS (DIFFSERV), IPv6 Traffic Class, etc.

Comprehensive Configuration Registers Access

- High-Speed SPI (4-Wire, Up to 50 MHz) Interface to Access All Internal Registers
- MII Management (MIIM, MDC/MDIO 2-Wire) Interface to Access All PHY Registers per Clause 22.2.4.5 of the IEEE 802.3 Specification
- I/O Pin Strapping Facility to Set Certain Register Bits from I/O Pins at Reset Time
- Control Registers Configurable On-the-Fly

IEEE 1588v2 PTP and Clock Synchronization

- Fully Compliant with the IEEE 1588v2 Precision Time Protocol
- One-Step or Two-Step Transparent Clock (TC) Timing Corrections
- E2E (End-to-End) or P2P (Peer-to-Peer) Transparent Clock (TC)
- Grandmaster, Master, Slave, Ordinary Clock (OC) Support
- IEEE1588v2 PTP Multicast and Unicast Frame Support
- Transports of PTP Over IPv4/IPv6 UDP and IEEE 802.3 Ethernet
- Delay Request-Response and Peer Delay Mechanism
- Ingress/Egress Packet time stamp Capture/Recording and Checksum Update
- Correction Field Update with Residence Time and Link Delay
- IEEE1588v2 PTP Packet Filtering Unit to Reduce Host Processor Overhead
- A 64-bit Adjustable System Precision Clock
- Twelve Trigger Output Units and Twelve time stamp Input Units Available for Flexible IEEE1588v2 Control of Twelve Programmable GPIO[11:0] Pins Synchronized to the Precision Time Clock
- GPIO Pin Usage for 1 PPS Generation, Frequency Generator, Control Bit Streams, Event Monitoring, Precision Pulse Generation, Complex Waveform Generation

Power and Power Management

- Single 3.3V Power Supply with Optional VDD I/O for 1.8V, 2.5V, or 3.3V
- Integrated Low Voltage (~1.3V) Low-Noise Regulator (LDO) Output for Digital and Analog Core Power
- Supports IEEE P802.3az™ Energy Efficient Ethernet (EEE) to Reduce Power Consumption in Transceivers in LPI State
- Full-Chip Hardware or Software Power-Down (All Registers Value are Not Saved and Strap-In Value will Re-Strap After Release the Power-Down)
- Energy Detect Power-Down (EDPD), which Disables the PHY Transceiver when Cables are Removed
- Dynamic Clock Tree Control to Reduce Clocking in Areas Not in Use
- Power Consumption Less than 0.5W

Additional Features

- Single 25 MHz ±50 ppm Reference Clock Requirement for MII Mode
- Selectable 25 MHz or 50 MHz Inputs for RMII Mode
- Comprehensive Programmable Two LED Indicators Support for Link, Activity, Full-/Half-Duplex and 10/100 Speed
- LED Pins Directly Controllable
- Industrial Temperature Range: –40°C to +85°C
- 64-Pin (10 mm x 10 mm) Lead Free (ROHS) LQFP Package

Applications

- Industrial Ethernet Applications that Employ IEEE 802.3-Compliant MACs. (Ethernet/IP, Profinet, MODBUS TCP, etc)
- Real-Time Ethernet Networks Requiring Sub-Microsecond Synchronization over Standard Ethernet
- IEC 61850 Networks Supporting Power Substation Automation
- Networked Measurement and Control Systems
- Industrial Automation and Motion Control Systems
- Test and Measurement Equipment

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Table of Contents

1.0 INTRODUCTION

1.1 General Terms and Conditions

The following is list of the general terms used throughout this document:

BIU - Bus Interface Unit	The host interface function that performs code conversion, buffering, and the like required for communications to and from a network.
BPDU - Bridge Protocol Data Unit	A packet containing ports, addresses, etc. to make sure data being passed through a bridged network arrives at its proper destination.
CMOS - Complementary Metal Oxide Semiconductor	A common semiconductor manufacturing technique in which positive and negative types of transistors are combined to form a current gate that in turn forms an effective means of controlling electrical current through a chip.
CRC - Cyclic Redundancy Check	A common technique for detecting data transmission errors. CRC for Ethernet is 32 bits long.
Cut-Through Switch	A switch typically processes received packets by reading in the full packet (storing), then processing the packet to determine where it needs to go, then forwarding it. A cut-through switch simply reads in the first bit of an incoming packet and forwards the packet. Cut-through switches do not store the packet.
DA - Destination Address	The address to send packets.
EMI - Electro-Magnetic Interference	A naturally occurring phenomena when the electromagnetic field of one device disrupts, impedes or degrades the electromagnetic field of another device by coming into proximity with it. In computer technology, computer devices are susceptible to EMI because electromagnetic fields are a byproduct of passing electricity through a wire. Data lines that have not been properly shielded are susceptible to data corruption by EMI.
FCS - Frame Check Sequence	See CRC.
FID - Frame or Filter ID	Specifies the frame identifier. Alternately is the filter identifier.
GPIO - General Purpose Input/Output	General Purpose Input/Output pins are signal pins that can be controlled or monitored by hardware and software to perform specific tasks.
IGMP - Internet Group Management Protocol	The protocol defined by RFC 1112 for IP multicast transmissions.
IPG - Inter-Packet Gap	A time delay between successive data packets mandated by the network standard for protocol reasons. In Ethernet, the medium has to be "silent" (i.e., no data transfer) for a short period of time before a node can consider the network idle and start to transmit. IPG is used to correct timing differences between a transmitter and receiver. During the IPG, no data is transferred, and information in the gap can be discarded or additions inserted without impact on data integrity.
ISA - Industry Standard Architecture	A bus architecture used in the IBM PC/XT and PC/AT.
ISI - Inter-Symbol Interference	The disruption of transmitted code caused by adjacent pulses affecting or interfering with each other.
Jumbo Packet	A packet larger than the standard Ethernet packet (1500 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc.
MAC - Media Access Controller	A functional block responsible for implementing the media access control layer which is a sub layer of the data link layer.
MDI - Medium Dependent Interface	An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null-modem, or cross-over, cable. MDI provides the standard interface to a particular media (copper or fiber) and is therefore “media dependent”.

BIU - Bus Interface Unit	The host interface function that performs code conversion, buffering, and the like required for communications to and from a network.
MDI-X - Medium Dependent Interface Crossover	An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null-modem, or crossover, cable. For 10/100 full-duplex networks, an end point (such as a computer) and a switch are wired so that each transmitter connects to the far end receiver. When connecting two computers together, a cable that crosses the TX and RX is required to do this. With auto MDI-X, the PHY senses the correct TX and RX roles, eliminating any cable confusion.
MIB - Management Information Base	The MIB comprises the management portion of network devices. This can include things like monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses).
MII - Media Independent Interface	The MII accesses PHY registers as defined in the IEEE 802.3 specification.
NIC - Network Interface Card	An expansion board inserted into a computer to allow it to be connected to a network. Most NICs are designed for a particular type of network, protocol, and media, although some can serve multiple networks.
NPVID - Non-Port VLAN ID	The port VLAN ID value is used as a VLAN reference.
NRZ - Non-Return to Zero	A type of signal data encoding whereby the signal does not return to a zero state in between bits.
PHY	A device or functional block which performs the physical layer interface function in a network.
PLL - Phase-Locked Loop	An electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal. A PLL ensures that a communication signal is locked on a specific frequency and can also be used to generate, modulate, and demodulate a signal and divide a frequency.
PTP - Precision Time Protocol	A protocol, IEEE 1588 as applied to this device, for synchronizing the clocks of devices attached to a specific network.
SA - Source Address	The address from which information has been sent.
TDR - Time Domain Reflectometry	TDR is used to pinpoint flaws and problems in underground and aerial wire, cabling, and fiber optics. They send a signal down the conductor and measure the time it takes for the signal, or part of the signal, to return.
TSU - time stamp Input Unit	The functional block which captures signals on the GPIO pins and assigns a time to the specific event.
TOU - Trigger Output Unit	The functional block which generates user configured waveforms on a specified GPIO pin at a specific trigger time.
UTP - Unshielded Twisted Pair	Commonly a cable containing four twisted pairs of wires. The wires are twisted in such a manner as to cancel electrical interference generated in each wire, therefore shielding is not required.
VLAN - Virtual Local Area Network	A configuration of computers that acts as if all computers are connected by the same physical network but which may be located virtually anywhere.

1.2 General Description

The KSZ8463 EtherSynch® product line consists of IEEE 1588v2 enabled Ethernet switches, providing integrated communications and synchronization for a range of Industrial Ethernet applications.

The KSZ8463 EtherSynch product line enables distributed, daisy-chained or ring topologies preferred for Industrial Ethernet networks. Conventional centralized (i.e., star-wired) topologies are also supported for dual-homed, fault-tolerant arrangements.

A flexible set of standard MAC interfaces is provided to interface to external host processors with embedded Ethernet MACs:

- KSZ8463ML: Media Independent Interface (MII)
- KSZ8463RL: Reduced Media Independent Interface (RMII)
- KSZ8463FML: MII, supports 100BASE-FX fiber in addition to 10/100BASE-TX copper
- KSZ8463FRL: RMII, supports 100BASE-FX fiber in addition to 10/100BASE-TX copper

The KSZ8463 devices incorporate the IEEE 1588v2 protocol. Sub-microsecond synchronization is available via the use of hardware-based time-stamping and transparent clocks making it the ideal solution for time synchronized Layer 2 communication in critical industrial applications.

Extensive general purpose I/O (GPIO) capabilities are available to use with the IEEE 1588v2 PTP to efficiently and accurately interface to locally connected devices.

Complementing the industry's most-integrated IEEE 1588v2 device is a precision timing protocol (PTP) v2 software stack that has been pre-qualified with the KSZ84xx product family. The PTP stack has been optimized around the KSZ84xx chip architecture, and is available in source code format along with Microchip's chip driver.

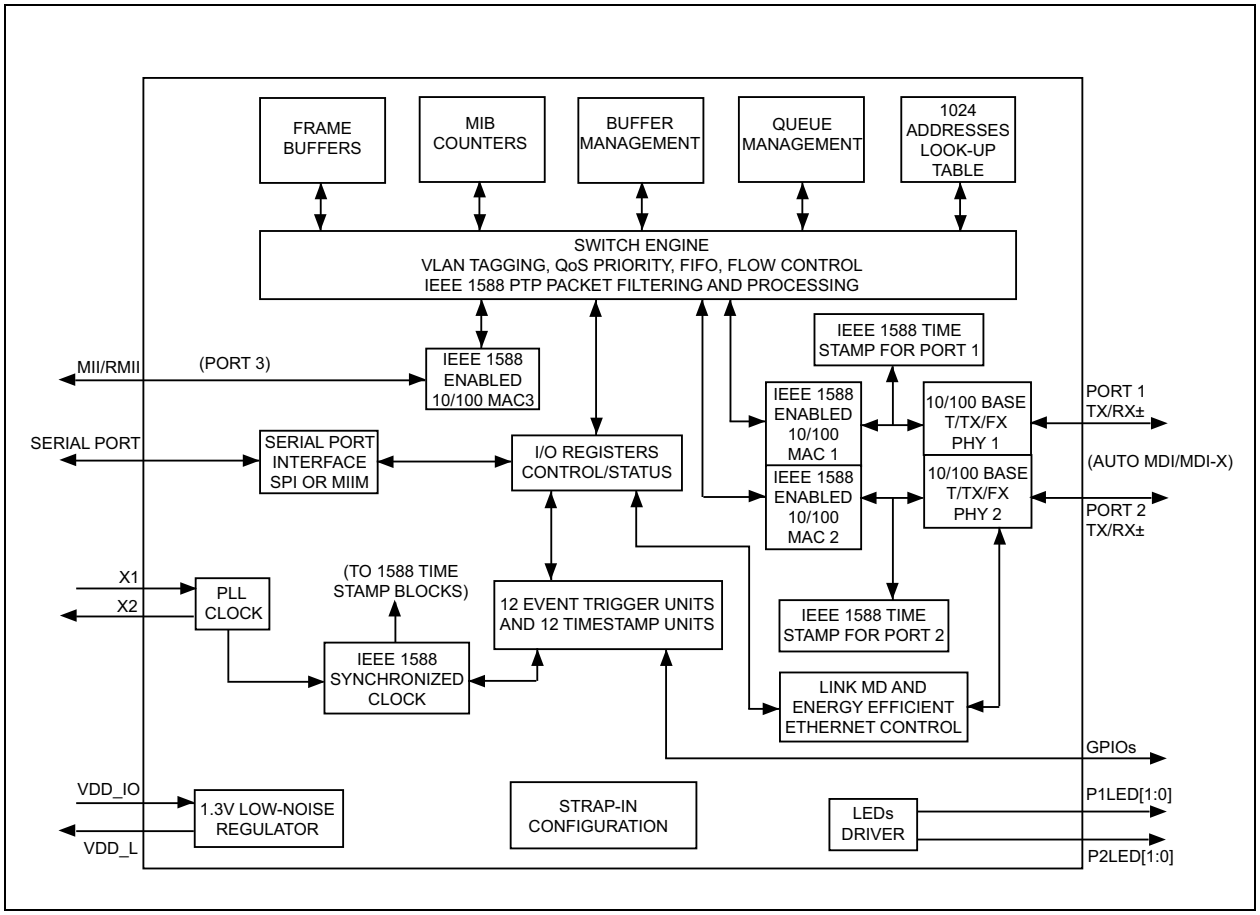
The KSZ8463 product line is built upon Microchip's industry-leading Ethernet technology, with features designed to offload host processing and streamline your overall design.

- Wire-speed Ethernet switching fabric with extensive filtering
- Two integrated 10/100BASE-TX PHY transceivers, featuring the industry's lowest power consumption
- Full-featured quality-of-service (QoS) support
- Flexible management options that support common standard interfaces

The wire-speed, store-and-forward switching fabric provides a full complement of QoS and congestion control features optimized for real-time Ethernet.

A robust assortment of power-management features including Energy Efficient Ethernet (EEE) have been designed in to satisfy energy efficient environments.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM, KSZ8463ML/RL/FML/FRL



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 64-PIN LQFP ASSIGNMENT, (TOP VIEW)

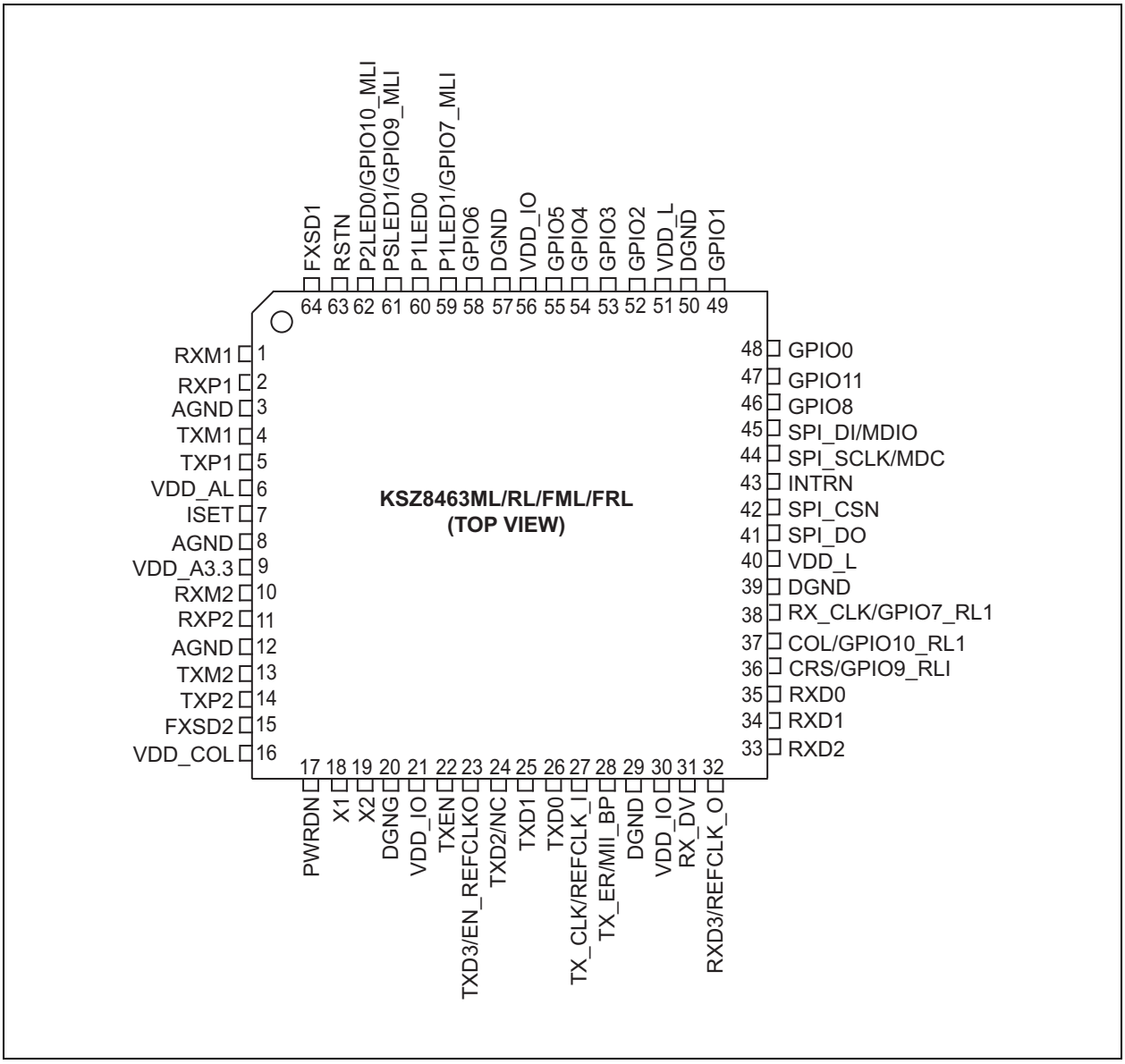


TABLE 2-1: SIGNALS FOR KSZ8463ML/RL/FML/FRL

Pin Number	Pin Name	Type (Note 2-1)	Description
1	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential).
2	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential).
3	AGND	GND	Analog Ground.
4	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential).
5	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential).
6	VDD_AL	P	This pin is used as an input for the low-voltage analog power. Its source should have appropriate filtering with a ferrite bead and capacitors.
7	ISET	O	Set physical transmits output current. Pull-down this pin with a 6.49 kΩ (1%) resistor to ground.
8	AGND	GND	Analog Ground.
9	VDD_A3.3	P	3.3V analog V_{DD} input power supply (Must be well decoupled).
10	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (– differential).
11	RXP2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (+ differential).
12	AGND	GND	Analog Ground.
13	TXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (– differential).
14	TXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential).
15	FXSD2	I	Fiber signal detect input for port 2 in 100BASE-FX fiber mode. When in copper mode, this input is unused and should be pulled to GND. Note: This functionality is available only on the KSZ8463FML/FRL devices.
16	VDD_COL	P	This pin is used as a second input for the low-voltage analog power. Its source should have appropriate filtering with a ferrite bead and capacitors.
17	PWRDN	IPU	**Full-Chip Power-Down** Active-Low (Low = Power-down; High or floating = Normal operation). While this pin is asserted low, all I/O pins will be tri-stated. All registers will be set to their default state. While this pin is asserted, power consumption will be minimal. When the pin is de-asserted, power consumption will climb to nominal and the device will be in the same state as having been reset by the reset pin (RSTN, pin 63).
18	X1	I	**25 MHz Crystal or Oscillator Clock Connection** Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a VDD_IO voltage tolerant oscillator and X2 is a no connect. This clock requirement is ±50 ppm. The KSZ8463RL has the option to use REFCLK_I (50 MHz) as its primary clock input instead of X1 and X2. This is determined by the state of pin 41 (SPI_DO) at power-up/reset time. See Table 2-2 for details. (Applies to the KSZ8463RL/FRL devices only)
19	X2	O	
20	DGND	GND	Digital ground.
21	VDD_IO	P	3.3V, 2.5V, or 1.8V digital V_{DD} input power pin for IO logic and the internal low-voltage regulator.

TABLE 2-1: SIGNALS FOR KSZ8463ML/RL/FML/FRL (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
22	TX_EN	IPD	**(8463ML, 8463FML) – MII Mode:** Transmit Enable. Active high input indicates there is valid transmit data on TXD[3:0]. **(8463RL, 8463FRL) – RMII Mode:** Transmit Enable. Active high indicates there is valid transmit data on TXD[1:0].
23	TXD3/ EN_REF- CLKO	IPD	**(8463ML, 8463FML) – MII Mode:** Transmit data input bit[3]. This data is synchronous to the TX_CLK (2.5 MHz in 10BASE-T mode or 25 MHz in 100BASE-TX mode) **(8463RL, 8463FRL) – RMII Mode:** EN_REFCLKO is used to enable REFCLK_O output on pin 32. If pulled up, the REFCLK_O output is enabled. If pulled down to disable, the REFCLK_O output is disabled.
24	TXD2/NC	IPD	**(8463ML, 8463FML) – MII Mode:** Transmit data input bit[2]. This data is synchronous to TX_CLK (2.5 MHz in 10BASE-T mode or 25 MHz in 100BASE-TX mode). **(8463RL, 8463FRL) – RMII Mode:** No connect. Is not used.
25	TXD1	IPD	**(8463ML, 8463FML) – MII Mode:** Transmit data input bit[1]. This data is synchronous to TX_CLK (2.5 MHz in 10BASE-T mode or 25 MHz in 100BASE-TX mode). **(8463RL, 8463FRL) – RMII Mode:** Transmit data input bit[1]. This data is synchronous to REFCLK (50 MHz).
26	TXD0	IPD	**(8463ML, 8463FML) – MII Mode:** Transmit data input bit[0]. This data is synchronous to TX_CLK (2.5 MHz in 10BASE-T mode or 25 MHz in 100BASE-TX mode). **(8463RL, 8463FRL) – RMII Mode:** Transmit data input bit[0]. This data is synchronous to REFCLK (50 MHz).
27	TX_CLK/ REFCLK_I	I/O (PD)	**(8463ML, 8463FML) – MII Mode:** Transmit clock. This is the output clock in PHY MII mode and input clock in MAC MII mode (2.5 MHz in 10BASE-T mode or 25 MHz in 100BASE-TX mode). **(8463RL, 8463FRL) – RMII Mode:** Reference input clock (50 MHz).
28	TX_ER/ MII_BP	IPD	**(8463ML, 8463FML) – MII Mode:** Transmit error input in MII MAC mode. In MII PHY mode: 1 = Disable the MII PHY mode link and enable the bypass mode. 0 = Set MII PHY mode in normal operation. **(8463RL, 8463FRL) – RMII Mode:** No connect. Not used.
29	DGND	GND	Digital Ground.
30	VDD_IO	P	3.3V, 2.5V, or 1.8V digital V_{DD} input power pin for IO logic and the internal low-voltage regulator.

TABLE 2-1: SIGNALS FOR KSZ8463ML/RL/FML/FRL (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
31	RX_DV	IPU/O	**(8463ML, 8463FML) – MII Mode:** Receive data valid, active high indicates that receive data on RXD[3:0] is valid. **(8463RL, 8463FRL) – RMII Mode:** Receive data valid, active high indicates that receive data on RXD[1:0] is valid. **Config Mode:** This pin is pulled up or down and its value is latched during the power-up / reset to select either PHY MII mode or MAC MII mode. See Table 2-2 for details.
32	RXD3/ REFCLK_O	IPD/O	**(8463ML, 8463FML) – MII Mode:** Receive data output bit[3]. This data is synchronous to RX_CLK (2.5 MHz in 10BASE-T mode or 25 MHz in 100BASE-TX mode) **(8463RL, 8463FRL) – RMII Mode:** REFCLK_O (50 MHz) output when EN_REFCLKO (pin 23) is pulled-up. (16 mA drive)
33	RXD2	IPU/O	**(8463ML, 8463FML) – MII Mode:** Receive data output bit[2]. This data is synchronous to RX_CLK (2.5 MHz in 10BASE-T mode or 25 MHz in 100BASE-TX mode) **(8463RL, 8463FRL) – RMII Mode:** Not used. **Config Mode:** This pin is pulled up or down via an external resistor and its value is latched during power-up/reset to select either high-speed SPI or low-speed SPI mode. See Table 2-2 for details.
34	RXD1	IPU/O	**(8463ML, 8463FML) – MII Mode:** Receive data output bit[1]. This data is synchronous to RX_CLK (2.5 MHz in 10BASE-T mode or 25 MHz in 100BASE-TX mode) **(8463RL, 8463FRL) – RMII Mode:** Receive data output bit[1]. This data is synchronous to REFCLK (50 MHz). **Config Mode:** This pin is pulled up or down via an external resistor and its value is latched during power-up/reset to select serial bus mode. See Table 2-2 for details.
35	RXD0	IPD/O	**(8463ML, 8463FML) – MII Mode:** Receive data output bit[0]. This data is synchronous to RX_CLK (2.5 MHz in 10BASE-T mode or 25 MHz in 100BASE-TX mode) **(8463RL, 8463FRL) – RMII Mode:** Receive data output bit[0]. This data is synchronous to REFCLK (50 MHz). **Config Mode:** This pin is pulled up or down via an external resistor and its value is latched during power-up/reset to select serial bus mode. See Table 2-2 for details.
36	CRS/ GPIO9_RLI	I/O (PD)	**(8463ML, 8463FML) – MII Mode:** Carrier Sense. This is an output signal in PHY MII mode and an input signal in MAC MII mode. **(8463RL, 8463FRL) – RMII Mode:** This is GPIO9 while in RMII mode. (Refer to GPIO0 pin 48 description).

TABLE 2-1: SIGNALS FOR KSZ8463ML/RL/FML/FRL (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
37	COL/ GPIO10_RLI	I/O (PD)	**(8463ML, 8463FML) – MII Mode:** Collision Detect. This is an output signal in PHY MII mode and an input signal in MAC MII mode. **(8463RL, 8463FRL) – RMII Mode:** This is GPIO10 while in RMII Mode. (Refer to GPIO0 pin 48 description).
38	RX_CLK/ GPIO7_RLI	I/O (PD)	**(8463ML, 8463FML) – MII Mode:** Receive Clock. This is an output clock in PHY MII mode and an input clock in MAC MII mode (2.5 MHz in 10BASE-T mode or 25 MHz in 100BASE-TX mode). **(8463RL, 8463FRL) – RMII Mode:** This is GPIO7 while in RMII mode. (Refer to GPIO0 pin 48 description).
39	DGND	GND	Digital Ground
40	VDD_L	P	This pin can be used in two ways: as the pin to input a low voltage to the device if the internal low-voltage regulator is not used, or as the low-voltage output if the internal low-voltage regulator is used.
41	SPI_DO	IPU/O	**Serial Data Output in SPI Slave Mode.** **Config Mode:** This pin pull-up/pull-down value is latched to select clock input either 25 MHz from X1/X2 or 50 MHz from REFCLK_I during power-up/reset. See Strapping Options section for detail. The REFCLK_I (50 MHz) option is available only on the KSZ8463RL and KSZ8463FRL. For the KSZ8463ML and KSZ8463FML, this pin must NOT be pulled down at power-up/reset.
42	SPI_CSN	IPD	**Chip Select (active-low) in SPI Slave Mode.** When SPI_CSN is high, the device is deselected and SPI_DO is held in a high-impedance state. A high-to-low transition is used to initiate the SPI data transfer. Note: An external 4.7 kΩ pull-up is needed on this pin when it is in use.
43	INTRN	OPU	**Interrupt Output.** This is an active-low signal going to the host CPU to indicate an interrupt status bit is set. This pin needs an external 4.7 kΩ pull-up resistor.
44	SPI_SCLK/ MDC	IPU	Serial Clock input in SPI (SPI_SCLK) slave mode. MIIM (MDC) mode is clock input.
45	SPI_DI/ MDIO	I/O (PU)	**Serial Data Input in SPI (SPI_DI) Slave Mode.** Serial Data input/output in MIIM (MDIO) mode. This pin needs an external 4.7 kΩ pull-up resistor.
46	GPIO8	I/O (PD)	This pin is GPIO8 (refer to GPIO0 pin 48 description).
47	GPIO11	I/O (PU)	This pin is GPIO11 (refer to GPIO0 pin 48 description).
48	GPIO0	I/O (PU)	**General Purpose Input/Output [0]** This pin can be used as an input or output pin for use by the IEEE 1588 event trigger or time stamp capture units. It will be synchronized to the internal IEEE 1588 clock. The host processor can also directly drive or read this GPIO pin.

TABLE 2-1: SIGNALS FOR KSZ8463ML/RL/FML/FRL (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
49	GPIO1	I/O (PU)	This pin is GPIO1 (refer to GPIO0 pin 48 description).
50	DGND	GND	Digital Ground.
51	VDD_L	P	This pin can be used in two ways: as the pin to input a low voltage to the device if the internal low-voltage regulator is not used, or as the low-voltage output if the internal low-voltage regulator is used.
52	GPIO2	I/O (PU)	This pin is GPIO2 (refer to GPIO0 pin 48 description).
53	GPIO3	I/O (PD)	This pin is GPIO3 (refer to GPIO0 pin 48 description).
54	GPIO4	I/O (PD)	This pin is GPIO4 (refer to GPIO0 pin 48 description).
55	GPIO5	I/O (PD)	This pin is GPIO5 (refer to GPIO0 pin 48 description).
56	VDD_IO	P	3.3V, 2.5V, or 1.8V digital VDD input power pin for IO logic and the internal low-voltage regulator.
57	DGND	GND	Digital ground.
58	GPIO6	I/O (PU)	This pin is GPIO6 (refer to GPIO0 pin 48 description).

TABLE 2-1: SIGNALS FOR KSZ8463ML/RL/FML/FRL (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (Note 2-1)</th><th>Description</th></tr>
<tr><td>59</td><td>P1LED1/
GPIO7_MLI</td><td>I/O
(PU)</td><td>Programmable LED Output to Indicate Port 1 and Port 2 Activity/Status.
The LED is ON (active) when output is low; the LED is OFF (inactive) when output is high.
The port 1 LED pins outputs are determined by the table below if Reg. 0x06C – 0x06D, bits [14:12] are set to ‘000’. Otherwise, the port 1 LED pins are controlled via the processor by setting Reg. 0x06C – 0x06D, bits [14:12] to a non-zero value.
The port 2 LED pins outputs are determined by the table below if Reg. 0x084 – 0x085, bits [14:12] are set to ‘000’. Otherwise, the port 2 LED pins are controlled via the processor by setting Reg. 0x084 – 0x085, bits [14:12] to a non-zero value.
Automatic port 1 and port 2 indicators are defined as follows:
<table>
<tr><td rowspan="2">—</td><td colspan="4">Two bits [9:8] in SGCR7 Control Register</td></tr>
<tr><td>00
(default)</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Speed</td><td>ACT</td><td>Duplex</td><td>Duplex</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Link/ACT</td><td>Link</td><td>Link/ACT</td><td>Link</td></tr>
</table>
Link = LED ON; ACT = LED Blink; Link/ACT = LED ON/Blink
Speed = LED ON (100BASE-TX); LED OFF (10BASE-T)
Duplex = LED ON (Full-Duplex); LED OFF (Half-Duplex)</td></tr>
<tr><td>60</td><td>P1LED0</td><td>I/O
(PU)</td><td></td></tr>
<tr><td>61</td><td>P2LED1/
GPIO9_MLI</td><td>I/O
(PU)</td><td></td></tr>
<tr><td>62</td><td>P2LED0/
GPIO10_MLI</td><td>I/O
(PU)</td><td>(8463ML, 8463FML) – MII Mode:
Functionality is controlled by IOMXSEL register D6h.
Pin 59 is P1LED1 (default) or GPIO7.
Pin 60 is P1LED0.
Pin 61 is P2LED1 (default) or GPIO9.
Pin 62 is P2LED0 (default) or GPIO10.
(8463RL, 8463FRL) – RMII Mode:
Pin 59 is P1LED1.
Pin 60 is P1LED0.
Pin 61 is P2LED1.
Pin 62 is P2LED0.</td></tr>
<tr><td>63</td><td>RSTN</td><td>IPU</td><td>Hardware reset input (active-low). This reset input is required to be low for a minimum of 10 ms after supply voltages VDD_IO and 3.3V are stable.</td></tr>
<tr><td>64</td><td>FXSD1</td><td>I</td><td>Fiber Signal Detect input for port 1 in 100BASE-FX fiber mode. When in copper mode, this input is unused and should be pulled to GND.
Note: This functionality is available only on the KSZ8463FML/FRL devices.</td></tr>
</table>

Note 2-1 P = power supply; GND = ground
I = input; O = output; I/O = bi-directional
IPU/O = Input with internal pull-up (58 kΩ ±30%) during power-up/reset; output pin otherwise.
IPD/O = Input with internal pull-down (58 kΩ ±30%) during power-up/reset; output pin otherwise.
IPU = Input with internal pull-up. (58 kΩ ±30%)
IPD = Input with internal pull-down. (58 kΩ ±30%)
OPU = Output with internal pull-up. (58 kΩ ±30%)
OPD = Output with internal pull-down. (58 kΩ ±30%)
I/O (PD) = Bi-directional input/output with internal pull-down. (58 kΩ ±30%)
I/O (PU) = Bi-directional input/output with internal pull-up. (58 kΩ ±30%)

TABLE 2-2: STRAPPING OPTIONS

Pin Number	Pin Name	Type Note 2-1	Description
31	RX_DV	IPU/O	**PHY Mode or MAC Mode Select During Power-Up/Reset:** Pull-up (default) or No Connect = PHY MII mode. Pull-down = MAC MII mode. Note: There is no equivalent strapping pin for RMII mode.
33	RXD2	IPU/O	**High-Speed SPI or Low-Speed SPI Select During Power-Up/Reset:** Pull-up (default) or No Connect = High-speed SPI mode (up to 50 MHz). Pull-down = Low-speed SPI mode (up to 12.5 MHz).
34	RXD1	IPU/O	**Serial Bus Mode Selection to Access the KSZ8463 Internal Registers During Power-Up/Reset:** Note: SPI Slave Mode is required for access to all registers, and for implementing the IEEE1588 protocol. **[RXD1, RXD0] = [0, 0] — Reserved** **[RXD1, RXD0] = [0, 1] — Reserved** **[RXD1, RXD0] = [1, 0] — SPI Slave Mode (Default)**
35	RXD0	IPD/O	Interface Signals / Type / Description SPI_DO (pin 41) / O / SPI data out SPI_SCLK (pin 44) / I / SPI clock SPI_DI (pin 45) / I / SPI data in SPI_CSN (pin 42) / I / SPI chip select **[RXD1, RXD0] = [1, 1] – MIIM-Mode** In MIIM mode, the KSZ8463 provides access to its 16-bit MIIM registers through its MDC (pin 44) and MDIO (pin 45).
41	SPI_DO	IPU/O	**25 MHz/50 MHz Input Clock Select for X1/X2 REFCLK_I On Power-Up/Reset:** Pull-up (default) or No Connect = 25 MHz input from X1/X2. (Both RMII and MII mode) Pull-down = 50 MHz input from REFCLK_I (EN_REFCLK = “0”). (Only RMII mode) This option is available only on the KSZ8463RL and KSZ8463FRL. For the KSZ8463ML and KSZ8463FML, this pin must NOT be pulled down at power-up/reset time.

Note 2-1 IPU/O = Input with internal pull-up (58 kΩ ±30%) during power-up/reset; output pin otherwise.
IPD/O = Input with internal pull-down (58 kΩ ±30%) during power-up/reset; output pin otherwise.

All strapping pins are latched at the end of the power-up or reset cycle. They are also latched when powering-up from a hardware or software power-down or hardware reset state.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8463 is a highly-integrated networking device that incorporates a Layer-2 switch, two 10BASE-T/100BASE-TX physical layer transceivers (PHYs) and associated MAC units, one MII/RMII interface on a third accessible MAC unit, and contains key IEEE 1588 precision time protocol (PTP) features.

The KSZ8463 operates in a managed mode. In managed mode, a host processor can access and control all PHY, Switch, MAC, and IEEE 1588 related registers in the KSZ8463 via the high-speed SPI bus, or partial control via the MIIM (MDC/MDIO) interface.

Physical signal transmission and reception are enhanced through the use of analog circuits in the PHY that make the design more efficient and allow for low power consumption. Both power management and Energy Efficient Ethernet (EEE) are designed to save more power while the device is in idle state.

The KSZ8463 is fully compliant to IEEE802.3u standards.

3.1 Physical (PHY) Block

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. An external 6.49 kΩ (1%) resistor for the 1:1 transformer ratio sets the output current.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output driver is also incorporated into the 100BASE-TX driver.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer has to adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to an MII format and provided as the input data to the MAC.

3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander.

Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence. Then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

3.1.4 PLL CLOCK SYNTHESIZER (RECOVERY)

The device incorporates an internal PLL clock synthesizer for data recovery as well as for generating various clocks used in the device. Refer to the Device Clocks section for details of this area.

3.1.5 100BASE-FX OPERATION

Fiber Mode is available only on the KSZ8463FML and KSZ8463FRL devices.

100BASE-FX operation is similar to 100BASE-TX operation except that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In this fiber mode, the auto-negotiation feature is bypassed and auto MDI/MDIX is disabled since there is no standard that supports fiber auto-negotiation and auto MDI/MDIX mode. The fiber port must be forced to either full-duplex or half-duplex mode.

All KSZ8463 devices are in copper mode (10BASE-T/100BASE-TX) when reset or powered on. Fiber mode is enabled by clearing bits [7:6] in the CFGR register (0x0D8-0x0D9). Each port is individually configurable. Bit[13] in the DSP_CNTRL_6 register (0x734-0x735) should also be cleared if either (or both) ports are set to fiber mode.

3.1.6 100BASE-FX SIGNAL DETECTION

In 100BASE-FX operation, the fiber signal detect inputs FXSD1 and FXSD2 are usually connected to the signal detect (SD) output pin of the fiber transceiver. When FXSD is low, no fiber signal is detected and a far-end fault (FEF) is generated. When FXSD is high, the fiber signal is detected. To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver SD output voltage swing to match the FXSD pin's input voltage threshold.

Alternatively, the user may choose not to implement the FEF feature. In this case, the FXSD input pin is tied high to force 100BASE-FX mode.

In copper mode, and on the KSZ8463ML and KSZ8463RL, the FXSD pins are unused and should be pulled low.

3.1.7 100BASE-FX FAR-END FAULT

A Far-End Fault (FEF) occurs when the signal detection is logically false on the receive side of the fiber transceiver. The KSZ8463FML/FRL detects an FEF when its FXSD input is below the fiber signal detect threshold. When an FEF is detected, the KSZ8463FML/FRL signals its fiber link partner that a FEF has occurred by sending 84 1's followed by a zero in the idle period between frames. By default, FEF is enabled. FEF can be disabled through register setting in P1CR4[12] and P2CR4[12].

3.1.8 10BASE-T TRANSMIT

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with typical 2.3V amplitude. The harmonic contents are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.1.9 10BASE-T RECEIVE

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function.

The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP1 or RXM1 input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8463 decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.1.10 MDI/MDI-X AUTO CROSSOVER

To eliminate the need for crossover cables between similar devices, the KSZ8463 supports HP-Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP-Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns the transmit and receive pairs for the KSZ8463. This feature is extremely useful when end users are unaware of cable types in addition to saving on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers. The IEEE 802.3u standard MDI and MDI-X definitions are in Table 3-1.

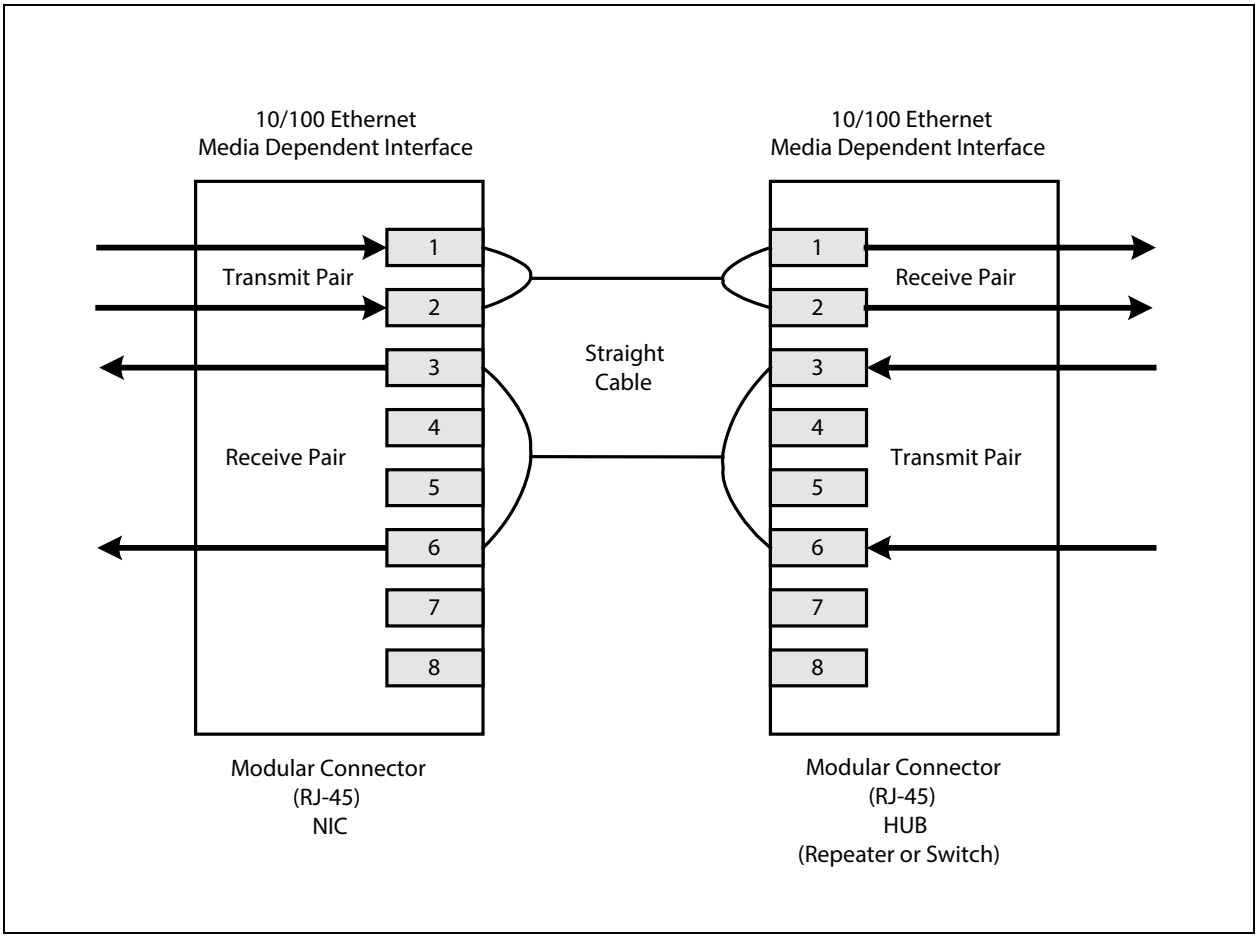
TABLE 3-1: MDI/MDI-X PIN DEFINITION

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.1.11 STRAIGHT CABLE

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-1 depicts a typical straight cable connection between a network interface card (NIC) and a switch, or hub (MDI-X).

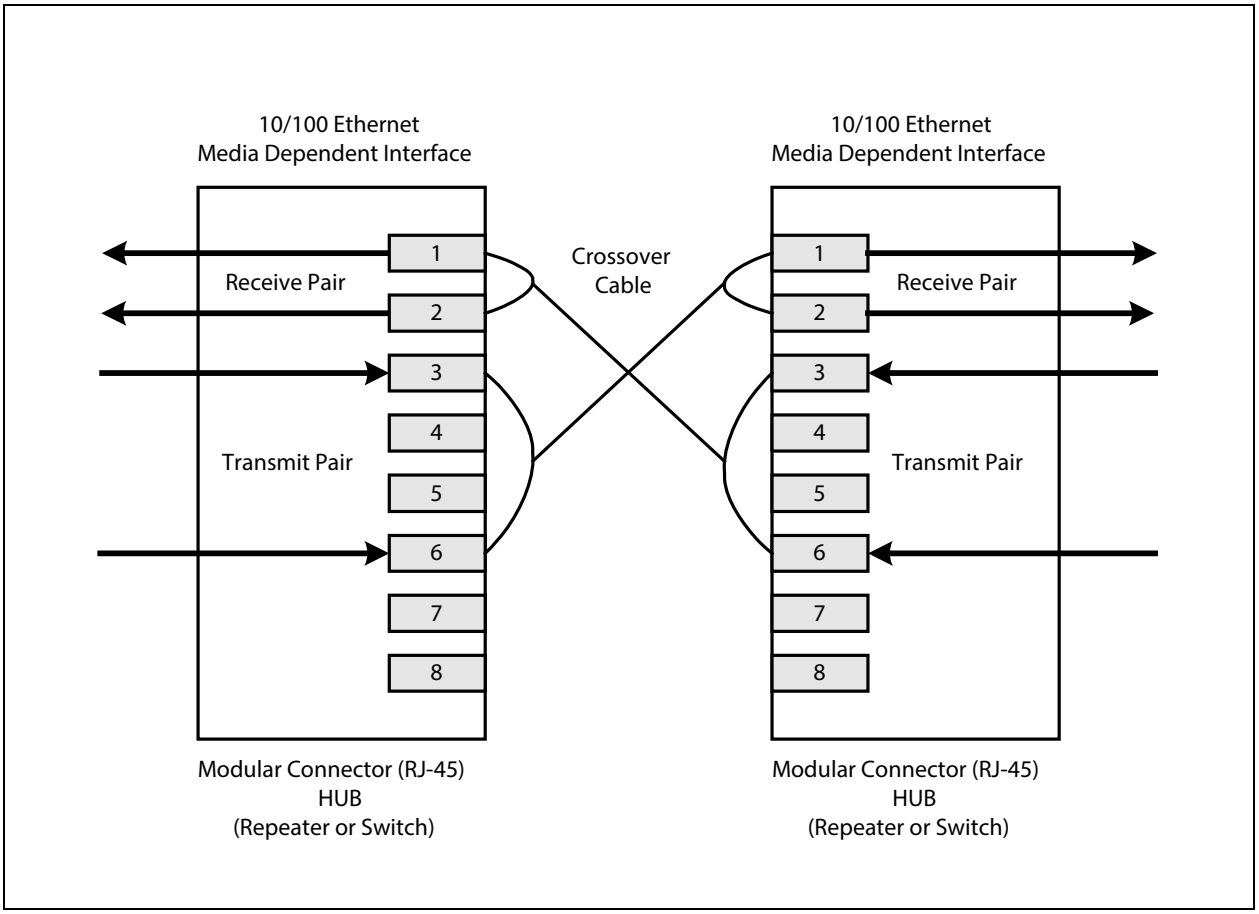
FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION



3.1.12 CROSSOVER CABLE

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-2 shows a typical crossover cable connection between two chips or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION



3.1.13 AUTO-NEGOTIATION

The KSZ8463 conforms to the auto-negotiation protocol as described by IEEE 802.3. It allows each port to operate at either 10BASE-T or 100BASE-TX. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto-negotiation, the link partners advertise capabilities across the link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation. Auto-negotiation is also used to negotiate support for Energy Efficient Ethernet (EEE). Auto-negotiation is only supported on ports in copper mode, not fiber mode.

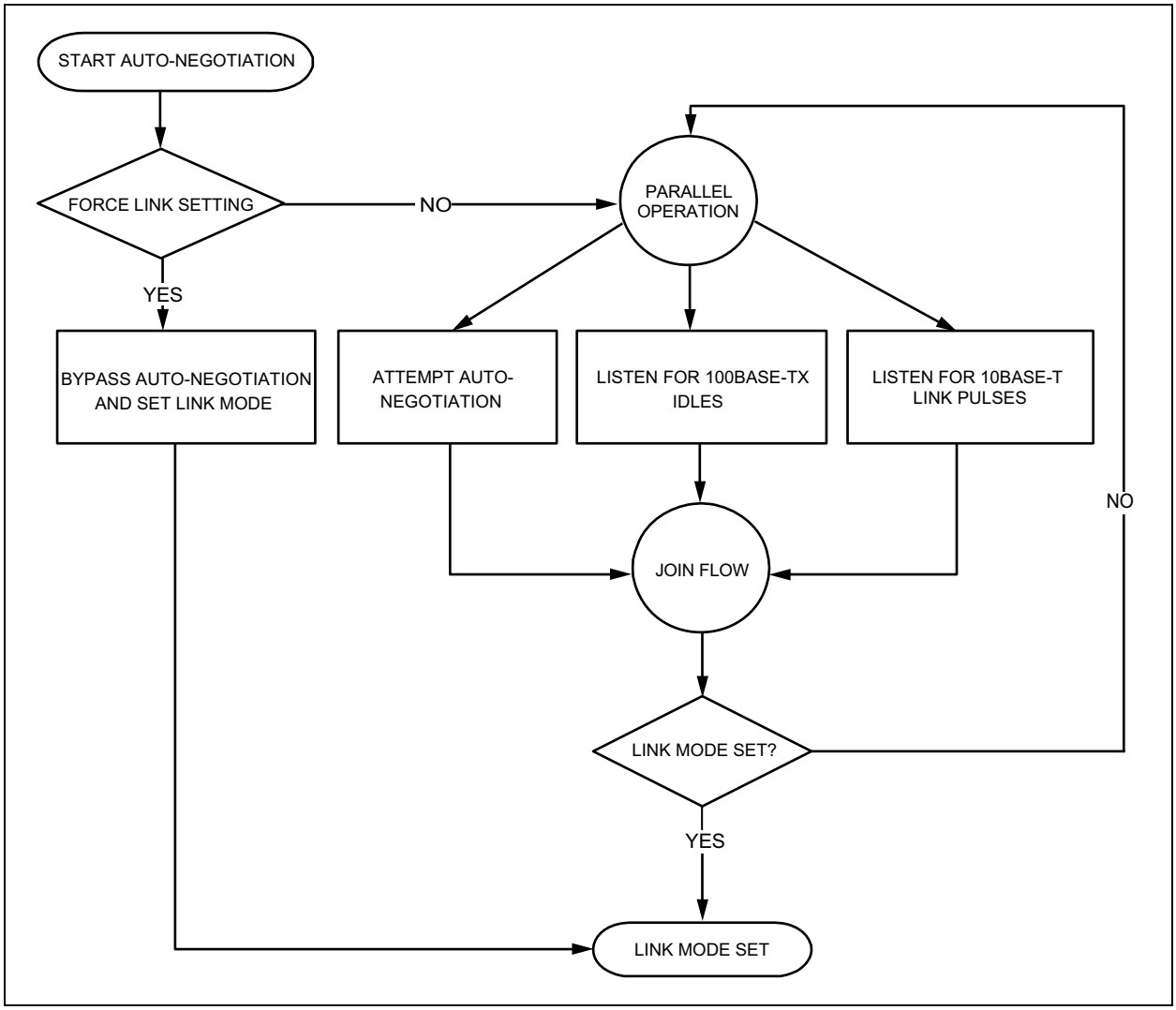
The following list shows the speed and duplex operation mode from highest to lowest.

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

If auto-negotiation is not supported or the link partner to the KSZ8463 is forced to bypass auto-negotiation, the mode is automatically set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto-negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The auto-negotiation link up process is shown in the following flow chart.

FIGURE 3-3: AUTO-NEGOTIATION FLOW CHART



3.1.14 LINKMD® CABLE DIAGNOSTICS

The KSZ8463 LinkMD uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with a maximum distance of 200m and an accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format in register P1SCSLMD[8:0] or P2SCSLMD[8:0].

Cable diagnostics are only valid for copper connections. Fiber-optic operation is not supported.

3.1.14.1 Access

LinkMD is initiated by accessing register P1SCSLMD (0x07C) or P2SCSLMD (0x094), the PHY special control/status and LinkMD register.

3.1.14.2 Usage

Before initiating LinkMD, the value 0x8008 must be written to the ANA_CNTRL_3 Register (0x74C – 0x74D). This needs to be done once (after power-n reset), but does not need to be repeated for each initiation of LinkMD. Auto-MDIX must also be disabled before using LinkMD. To disable Auto-MDIX, write a '1' to P1CR4[10] or P2CR4[10] to enable manual control over the pair used to transmit the LinkMD pulse. The self-clearing cable diagnostic test enable bit, P1SCSLMD[12] or P2SCSLMD[12], is set to '1' to start the test on this pair.

When bit P1SCSLMD[12] or P2SCSLMD[12] returns to '0', the test is completed. The test result is returned in bits P1SCSLMD[14:13] or P2SCSLMD[14:13] and the distance is returned in bits P1SCSLMD[8:0] or P2SCSLMD[8:0]. The cable diagnostic test results are as follows:

- 00 = Valid test, normal condition
- 01 = Valid test, open circuit in cable
- 10 = Valid test, short-circuit in cable
- 11 = Invalid test, LinkMD® failed

If P1SCSLMD[14:13] or P2SCSLMD[14:13] is "11", this indicates an invalid test. This occurs when the KSZ8463 is unable to shut down the link partner. In this instance, the test is not run, because it is not possible for the KSZ8463 to determine if the detected signal is a reflection of the signal generated or a signal from another source.

Cable distance can be approximated by utilizing the following formula:

- P1SCSLMD[8:0] x 0.4m for port 1 cable distance
- P2SCSLMD[8:0] x 0.4m for port 2 cable distance

This constant (0.4m) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

3.1.15 ON-CHIP TERMINATION RESISTORS

Using the KSZ8463 reduces board cost and simplifies board layout by using on-chip termination resistors for the RX/TX differential pairs, eliminating the need for external termination resistors in copper mode. The internal chip termination and biasing provides significant power savings when compared with using external biasing and termination resistors.

3.1.16 LOOPBACK SUPPORT

The KSZ8463 provides two loopback modes. One is near-end (remote) loopback to support remote diagnosing of failures on line side, and the other is far-end loopback to support local diagnosing of failures through all blocks of the device. In loopback mode, the speed of the PHY port will be set to 100BASE-TX full-duplex mode.

3.1.16.1 Far-End Loopback

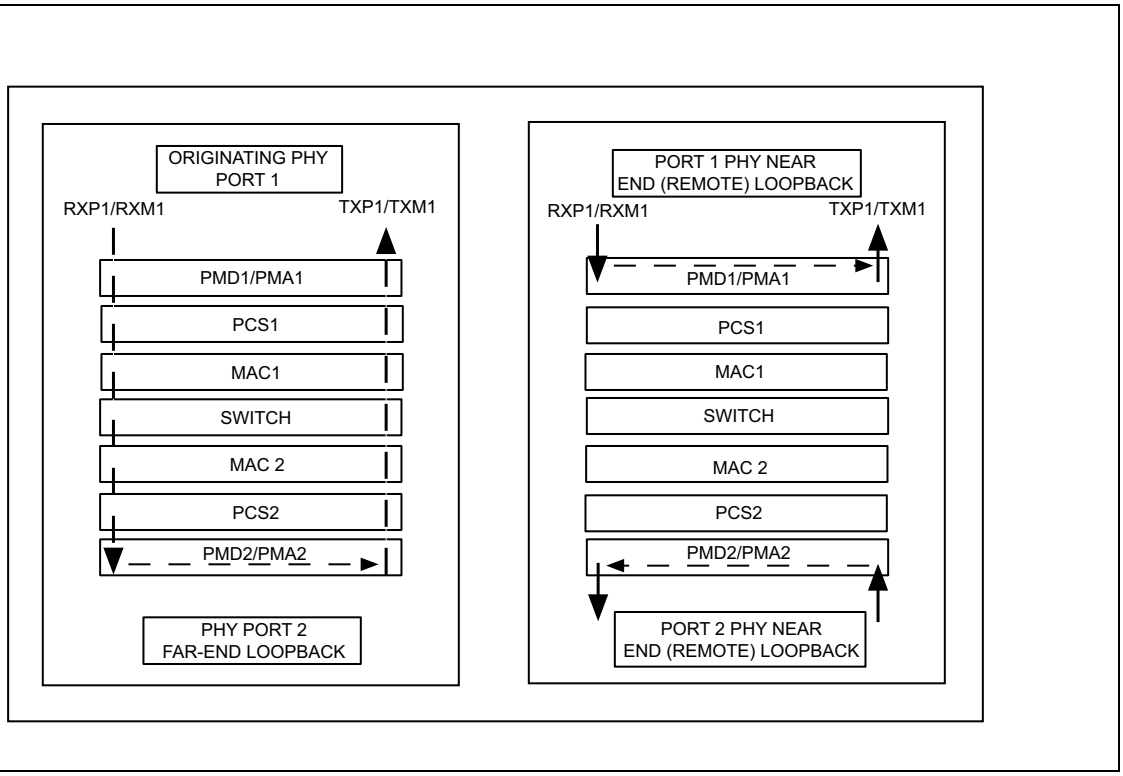
Far-end loopback is conducted between the KSZ8463's two PHY ports. The loopback path starts at the "originating" PHY port's receive inputs (RXP/RXM), wraps around at the "loopback" PHY port's PMD/PMA (Physical Media Dependent/Physical Media Attachment), and ends at the "Originating" PHY port's transmit outputs (TXP/TXM).

Bit[8] of registers P1CR4 and P2CR4 is used to enable far-end loopback for ports 1 and 2, respectively. As an alternative, bit[14] of registers P1MBCR and P2MBCR can be used to enable far-end loopback. The far-end loopback path is illustrated in Figure 3-4.

3.1.16.2 Near-End (Remote) Loopback

Near-end (remote) loopback is conducted at either PHY port 1 or PHY port 2 of the KSZ8463. The loopback path starts at the PHY port's receive inputs (RXPx/RXMx), wraps around at the same PHY port's PMD/PMA, and ends at the same PHY port's transmit outputs (TXPx/TXMx). Bit[1] of registers P1PHYCTRL and P2PHYCTRL is used to enable near-end loopback for ports 1 and 2, respectively. As an alternative, bit[9] of registers P1SCSLMD and P2SCSLMD can be used to enable near-end loopback. The near-end loopback paths for port 1 and port 2 are illustrated in Figure 3-4.

FIGURE 3-4: NEAR-END AND FAR-END LOOPBACK



3.2 Media Access Controller (MAC) Block

3.2.1 MAC OPERATION

The KSZ8463 strictly abides by IEEE 802.3 standards to maximize compatibility. Additionally, there is an added MAC filtering function to filter unicast packets. The MAC filtering function is useful in applications such as VoIP where restricting certain packets reduces congestion and thus improves performance.

3.2.2 ADDRESS LOOKUP

The internal Dynamic MAC Address lookup table stores MAC addresses and their associated information. It contains a 1K entry unicast address learning table plus switching information.

The KSZ8463 is guaranteed to learn 1K addresses and distinguishes itself from hash-based lookup tables, which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses they can learn.

3.2.3 LEARNING

The internal lookup engine updates the Dynamic MAC Address table with a new entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the lookup table.
- The received packet has no receiving errors, and the packet size is of legal length.

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the oldest entry of the table is deleted to make room for the new entry.

3.2.4 MIGRATION

The internal lookup engine also monitors whether a station has moved. If a station has moved, it updates the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet has no receiving errors, and the packet size is of legal length.

The lookup engine updates the existing record in the table with the new source port information.

3.2.5 AGING

The lookup engine updates the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the lookup engine removes the record from the table. The lookup engine constantly performs the aging process and continuously removes aging records. The aging period is about 300 seconds (±75 seconds). This feature can be enabled or disabled through global register SGCR1[10].

3.2.6 FORWARDING

The KSZ8463 forwards packets using the algorithm that is depicted in the following flowcharts. Figure 3-5 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with “port-to-forward 2” (PTF2), as shown in Figure 3-6. The packet is sent to PTF2.

The KSZ8463 will not forward the following packets:

- Error packets: These include framing errors, frame check sequence (FCS) errors, alignment errors, and illegal size packet errors.
- IEEE802.3x PAUSE frames: KSZ8463 intercepts these packets and performs full duplex flow control accordingly.

"Local" packets: Based on destination address (DA) lookup. If the destination port from the lookup table matches the port from which the packet originated, the packet is defined as "local."

FIGURE 3-5: DESTINATION ADDRESS LOOKUP FLOW CHART IN STAGE ONE

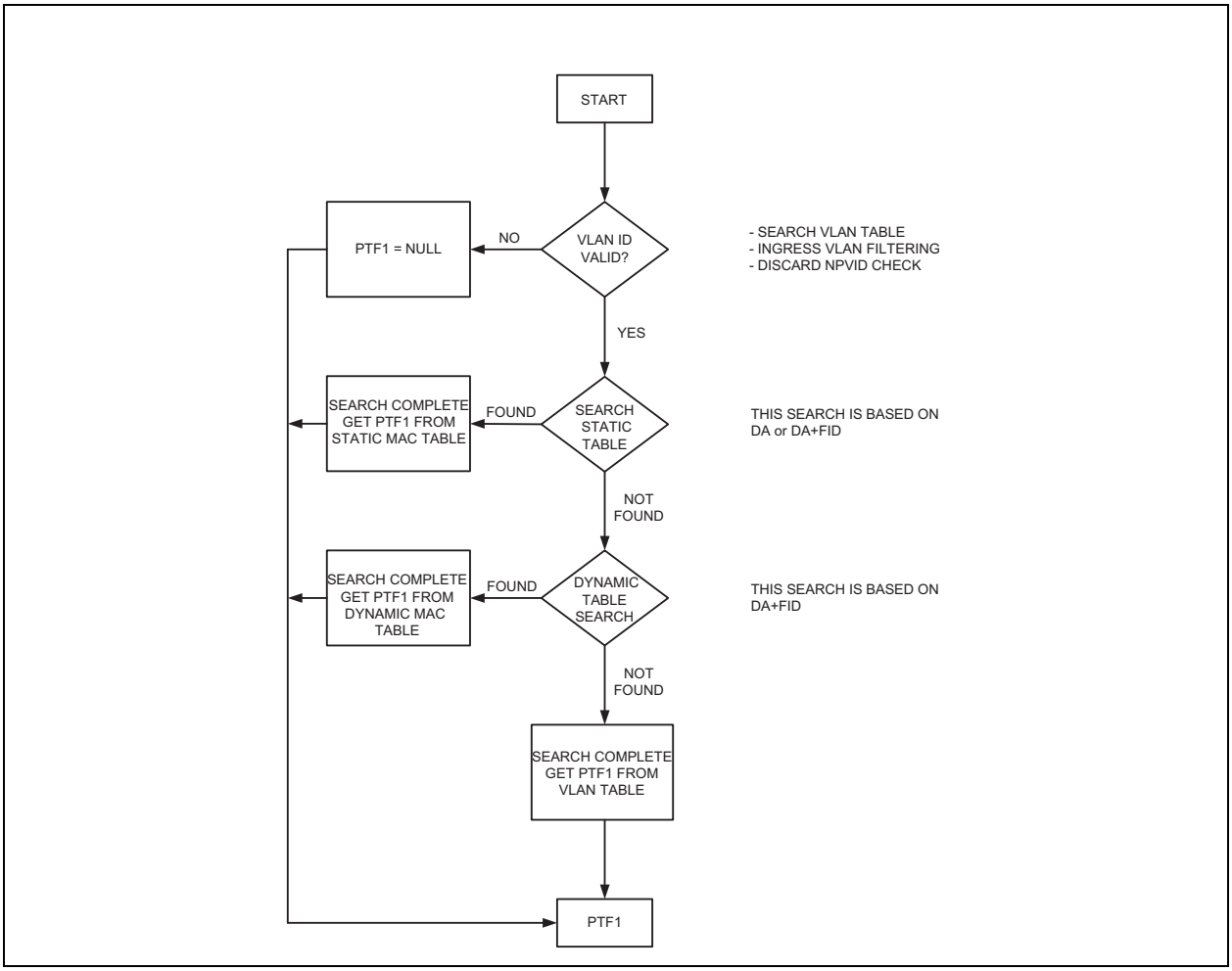
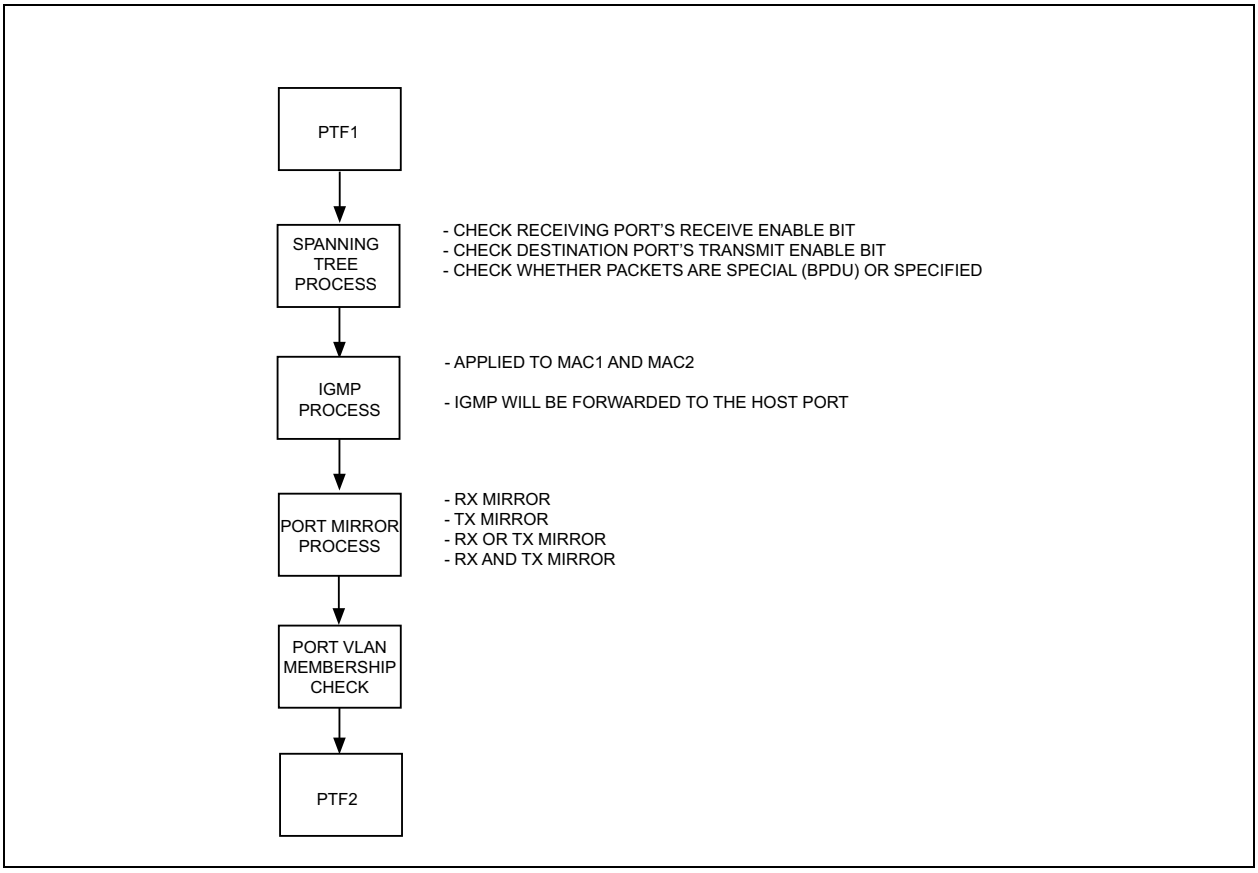


FIGURE 3-6: DESTINATION ADDRESS RESOLUTION FLOW CHART IN STAGE TWO



3.2.7 INTER-PACKET GAP (IPG)

If a frame is successfully transmitted, then the minimum 96-bit time for IPG is measured between two consecutive packets. If the current packet is experiencing collisions, the minimum 96-bit time for IPG is measured from carrier sense (CRS) to the next transmit packet.

3.2.8 BACK-OFF ALGORITHM

The KSZ8463 implements the IEEE standard 802.3 binary exponential back-off algorithm in half-duplex mode. After 16 collisions, the packet is dropped.

3.2.9 LATE COLLISION

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

3.2.10 LEGAL PACKET SIZE

The KSZ8463 discards packets less than 64 bytes and can be programmed to accept packet sizes up to 1536 bytes in SGCR2[1]. The KSZ8463 can also be programmed for special applications to accept packet sizes up to 2000 bytes in SGCR1[4].

3.2.11 FLOW CONTROL

The KSZ8463 supports standard 802.3x flow control frames in both the transmit and receive directions.

In the receive direction, if a PAUSE control frame is received on any port, the KSZ8463 will not transmit the next normal frame on that port until the timer, specified in the PAUSE control frame, expires. If another PAUSE frame is received before the current timer expires, the timer will then update with the new value in the second PAUSE frame. During this period (while it is flow controlled), only flow control packets from the KSZ8463 are transmitted.

In the transmit direction, the KSZ8463 has intelligent and efficient ways to determine when to invoke flow control and send PAUSE frames. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KSZ8463 issues a PAUSE frame containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8463 sends out another flow control frame with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

3.2.12 HALF-DUPLEX BACKPRESSURE

A half-duplex backpressure option (non-IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as in full-duplex mode. If backpressure is required, the KSZ8463 sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8463 discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until chip resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collision and carrier sense is maintained to prevent packet reception.

To ensure no packet loss in 10BASE-T or 100BASE-TX half-duplex mode, the user must enable the following bits:

- Aggressive back-off (bit [8] in SGCR1)
- No excessive collision drop (bit [3] in SGCR2)
- Backpressure flow control enable (bit [11] in P1CR2/P2CR2)

Please note that these bits are not set in default because this is not the IEEE standard.

3.2.13 BROADCAST STORM PROTECTION

The KSZ8463 has an intelligent option to protect the switch system from receiving too many broadcast packets. As the broadcast packets are forwarded to all ports except the source port, an excessive number of switch resources (bandwidth and available space in transmit queues) may be utilized. The KSZ8463 has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis in P1CR1[7] and P2CR1[7]. The rate is based on a 67ms interval for 100BASE-TX and a 670 ms interval for 10BASE-T. At the beginning of each interval, the counter is cleared to zero and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in SGCR3[2:0][15:8]. The default setting is 0x63 (99 decimal). This is equal to a rate of 1%, calculated as follows:

EQUATION 3-1:

$$148,000 \text{ frames/sec} \times 67ms/\text{interval} \times 1\% = 99 \text{ frames/interval (appx.)} = 0x63$$

148,800 frames/sec is based on 64-byte block of packets in 100BASE-T with 12 bytes of IPG and 8 bytes of preamble between two packets.

3.2.14 PORT INDIVIDUAL MAC ADDRESS AND SOURCE PORT FILTERING

The KSZ8463 can provide individual MAC addresses for port 1 and port 2. They can be set at registers 0x0B0h – 0x0B5h and 0x0B6 – 0x0BB. Received packets can be filtered (dropped) if their source address matches the MAC address of port 1 or port 2. This feature can be enabled by setting bits [11:10] in the P1CR1 or P2CR1 registers. One example of usage is that a packet will be dropped after it completes a full round trip within a ring network.

3.3 Switch Block

3.3.1 SWITCHING ENGINE

The KSZ8463 features a high-performance switching engine to move data to and from the MAC's packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency. The switching engine has a 32 KByte internal frame buffer. This resource is shared between all the ports. There are a total of 256 buffers available. Each buffer is sized at 128 Bytes.

3.3.2 SPANNING TREE SUPPORT

To support spanning tree, the host port is the designated port for the processor. The other ports (port 1 and port 2) can be configured in one of the five spanning tree states via "transmit enable", "receive enable", and "learning disable" register settings in registers P1CR2 and P2CR2 for ports 1 and 2, respectively. Table 3-2 shows the setting and software actions taken for each of the five spanning tree states.

TABLE 3-2: SPANNING TREE STATES

Disable State	**Port Setting**	**Software Action**
The port should not forward or receive any packets. Learning is disabled.	transmit enable = "0", receive enable = "0", learning disable = "1"	The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the "Static MAC Table" with "overriding bit" set) and the processor should discard those packets. Address learning is disabled on the port in this state.
Blocking State	**Port Setting**	**Software Action**
Only packets to the processor are forwarded.	transmit enable = "0", receive enable = "0", learning disable = "1"	The processor should not send any packets to the port(s) in this state. The processor should program the "Static MAC Table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.
Listening State	**Port Setting**	**Software Action**
Only packets to and from the processor are forwarded. Learning is disabled.	transmit enable = "0", receive enable = "0", learning disable = "1"	The processor should program the "Static MAC Table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is disabled on the port in this state.
Learning State	**Port Setting**	**Software Action**
Only packets to and from the processor are forwarded. Learning is enabled.	transmit enable = "0", receive enable = "0", learning disable = "0"	The processor should program the "Static MAC Table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is enabled on the port in this state.
Forwarding State	**Port Setting**	**Software Action**
Packets are forwarded and received normally. Learning is enabled.	transmit enable = "1", receive enable = "1", learning disable = "0"	The processor programs the "Static MAC Table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit is set so that the switch forwards those specific packets to the processor. The processor can send packets to the port(s) in this state. Address learning is enabled on the port in this state.

3.3.3 RAPID SPANNING TREE SUPPORT

There are three operational states assigned to each port for RSTP (Discarding, Learning, and Forwarding):

- Discarding ports do not participate in the active topology and do not learn MAC addresses.
- Discarding state: the state includes three states of the disable, blocking and listening of STP.
- Port setting: transmit enable = “0”, receive enable = “0”, learning disable = “1”.

3.3.3.1 Discarding State

Software action: The host processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the static table with “overriding bit” set) and the processor should discard those packets. When the port’s learning capability (learning disable = ‘1’) is disabled, setting bits [10:9] in the SGCR8 register will rapidly flush the port related entries in the dynamic MAC table and static MAC table.

The processor is connected to port 3 via the host interface. Address learning is disabled on the port in this state.

3.3.3.2 Learning State

Ports in “learning states” learn MAC addresses, but do not forward user traffic.

Learning State: Only packets to and from the processor are forwarded. Learning is enabled.

Port setting for Learning State: transmit enable = “0”, receive enable = “0”, learning disable = “0”.

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state (see the Tail Tagging Mode sub-section for details). Address learning is enabled on the port in this state.

Ports in “forwarding states” fully participate in both data forwarding and MAC learning.

3.3.3.3 Forwarding State

Forwarding state: Packets are forwarded and received normally. Learning is enabled.

Port setting: transmit enable = “1”, receive enable = “1”, learning disable = “0”.

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state (see the Tail Tagging Mode sub-section for details). Address learning is enabled on the port in this state.

RSTP uses only one type of BPDU called RSTP BPDUs. They are similar to STP configuration BPDUs with the exception of a type field set to “version 2” for RSTP and “version 0” for STP, and a flag field carrying additional information.

3.3.4 TAIL TAGGING MODE

The tail tag is only seen and used by the port 3 host interface, which should be connected to a processor. It is an effective way to retrieve the ingress port information for spanning tree protocol, IGMP snooping, and other applications. Bits [1:0] in the one byte tail tagging are used to indicate the source/destination port in port 3. Bits[3:2] are used for priority setting of the ingress frame in port 3. Other bits are not used. The tail tag feature is enabled by setting bit[8] in the SGCR8 register.

FIGURE 3-7: TAIL TAG FRAME FORMAT

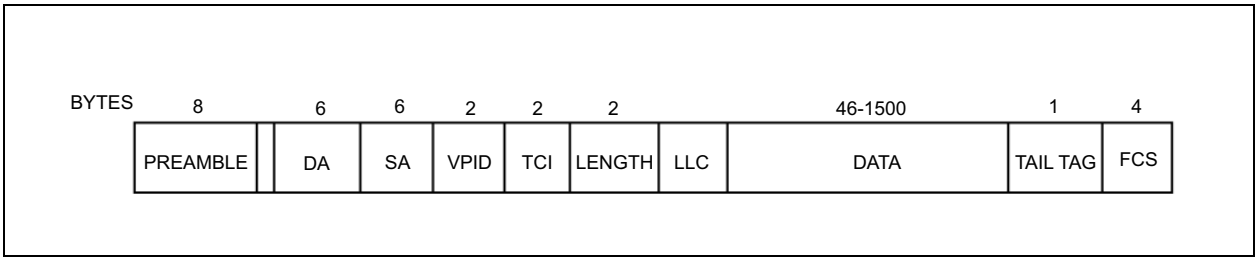


TABLE 3-3: TAIL TAG RULES

Ingress to Port 3 (Host to KSZ8463)	
Bit[1:0]	**Destination Port**
00	Normal (Address Look up)
01	Port 1
10	Port 2
11	Port 1 and Port 2
Bit[3:2]	**Frame Priority**
00	Priority 0
01	Priority 1
10	Priority 2
11	Priority 3
Egress from Port 3 (KSZ8463 to Host)	
Bit[0]	**Source Port**
0	Port 1
1	Port 2

3.3.5 IGMP SUPPORT

For Internet Group Management Protocol (IGMP) support in Layer 2, the KSZ8463 provides two components:

3.3.5.1 IGMP Snooping

The KSZ8463 traps IGMP packets and forwards them only to the processor (host port). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2.

3.3.5.2 Multicast Address Insertion in the Static MAC Table

Once the multicast address is programmed in the Static MAC Address Table, the multicast session is trimmed to the subscribed ports, instead of broadcasting to all ports.

To enable IGMP support, set bit[14] to ‘1’ in the SGCR2 register. Also, Tail Tagging Mode needs to be enabled, so that the processor knows which port the IGMP packet was received on. This is achieved by setting bit [8] to ‘1’ in the SGCR8 register.

3.3.6 IPV6 MLD SNOOPING

The KSZ8463 traps IPv6 Multicast Listener Discovery (MLD) packets and forwards them only to the processor (host port). MLD snooping is controlled by SGCR2, bit[13] (MLD snooping enable) and SGCR2 bit[12] (MLD option).

Setting SGCR2 bit[13] causes the KSZ8463 to trap packets that meet all of the following conditions:

- IPv6 multicast packets
- Hop count limit = “1”
- IPv6 next header = “1”or “58” (or = “0” with hop-by-hop next header = “1” or “58”)
- If SGCR2[12] = “1”, IPv6 next header = “43”, “44”, “50”, “51”, or “60” (or = “0” with hop-by-hop next header = “43”, “44”, “50”, “51”, or “60”)

3.3.7 PORT MIRRORING SUPPORT

KSZ8463 supports port mirroring comprehensively as:

3.3.7.1 “Receive Only” Mirror-on-a-Port

All the packets received on the port are mirrored on the sniffer port. For example, 1 is programmed to be “receive sniff” and the host port is programmed to be the “sniffer”. A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8463 forwards the packet to both port 2 and the host port. The KSZ8463 can optionally even forward “bad” received packets to the “sniffer port”.

3.3.7.2 "Transmit Only" Mirror-on-a-Port

All the packets transmitted on the port are mirrored on the sniffer port. For example, port 1 is programmed to be "transmit sniff" and the host port is programmed to be the "sniffer port". A packet received on port 2 is destined to port 1 after the internal lookup. The KSZ8463 forwards the packet to both port 1 and the host port.

3.3.7.3 "Receive and Transmit" Mirror-on-Two-Ports

All the packets received on port A and transmitted on port B are mirrored on the sniffer port. To turn on the "AND" feature, set register SGCR2, bit 8 to "1". For example, port 1 is programmed to be "receive sniff", port 2 is programmed to be "transmit sniff", and the host port is programmed to be the "sniffer port". A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8463 forwards the packet to both port 2 and the host port.

Multiple ports can be selected as "receive sniff" or "transmit sniff". In addition, any port can be selected as the "sniffer port". All these per port features can be selected through registers P1CR2, P2CR2, and P3CR2 for ports 1, 2, and the host port, respectively.

3.3.7.4 IEEE 802.1Q VLAN Support

The KSZ8463 supports 16 active VLANs out of the 4096 possible VLANs specified in the IEEE 802.1Q specification. KSZ8463 provides a 16-entry VLAN table, which converts the 12-bits VLAN ID (VID) to the 4-bits Filter ID (FID) for address lookup. If a non-tagged or null-VID-tagged packet is received, the ingress port default VID is used for lookup. In VLAN mode, the lookup process starts with VLAN table lookup to determine whether the VID is valid. If the VID is not valid, the packet is dropped and its address is not learned. If the VID is valid, the FID is retrieved for further lookup. The FID + Destination Address (FID+DA) are used to determine the destination port. The FID + Source Address (FID+SA) are used for address learning (see Table 3-4 and Table 5).

Advanced VLAN features are also supported in the KSZ8463, such as "VLAN ingress filtering" and "discard non PVID" defined in bits [14:13] of P1CR2, P2CR2 and P3CR2 registers. These features can be controlled on per port basis.

TABLE 3-4: FID + DA LOOKUP IN VLAN MODE

DA found in Static MAC Table?	Use FID Flag?	FID Match?	DA+FID found in Dynamic MAC Table?	Action
No	Don't Care	Don't Care	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16].
No	Don't Care	Don't Care	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52].
Yes	0	Don't Care	Don't Care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48].
Yes	1	No	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16].
Yes	1	No	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52].
Yes	1	Yes	Don't Care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48].

TABLE 3-5: FID + SA LOOKUP IN VLAN MODE

FID+SA found in Dynamic MAC Address Table?	Action
No	Learn and add FID+SA to the Dynamic MAC Address Table.
Yes	Update time stamp.

3.3.8 QUALITY-OF-SERVICE (QOS) PRIORITY SUPPORT

The KSZ8463 provides quality-of-service (QoS) for applications such as VoIP and video conferencing. The KSZ8463 offer 1, 2, and 4 priority queues option per port. This is controlled by bit[0] and bit[8] in P1CR1, P2CR1 and P3CR1 registers as shown below:

- Bit[0], bit[8] = "00" egress port is a single output queue as default.

- Bit[0], bit[8] = “01” egress port can be split into two priority transmit queues. (Q0 and Q1)
- Bit[0], bit[8] = “10” egress port can be split into four priority transmit queues. (Q0, Q1, Q2 and Q3)

The four priority transmit queues is a new feature in the KSZ8463. Queue 3 is the highest priority queue and Queue 0 is the lowest priority queue. If a port's transmit queue is not split, high priority and low priority packets have equal priority in the transmit queue.

There is an additional option for every port via bits[15,7] in the P1TXQRCR1, P1TXQRCR2, P2TXQRCR1, P2TXQRCR2, P3TXQRCR1, and P3TXQRCR2 Registers to select either always to deliver high priority packets first or use weighted fair queuing for the four priority queues scale by 8:4:2:1.

3.3.9 PORT-BASED PRIORITY

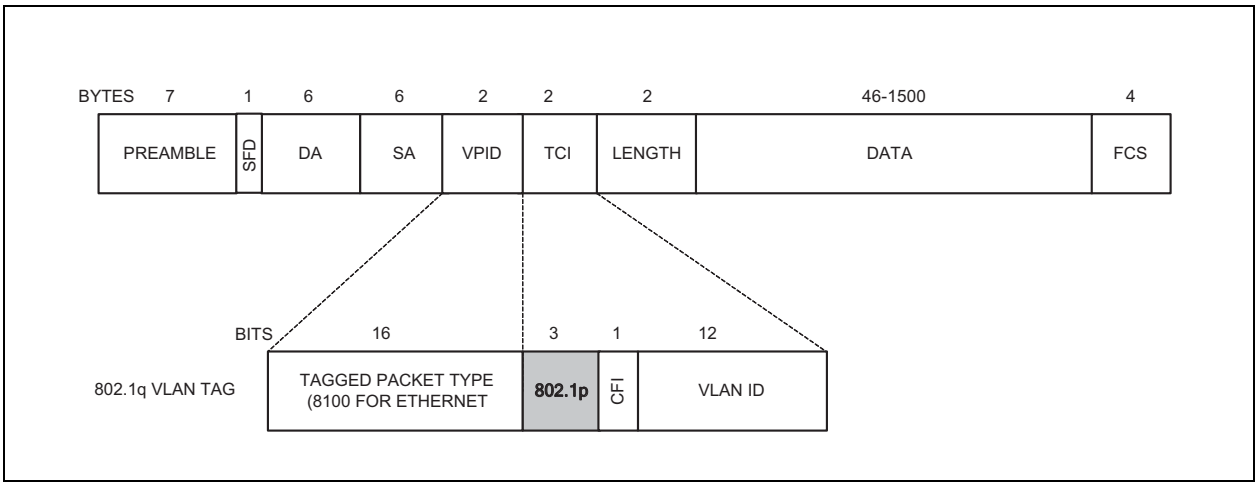
With port-based priority, each ingress port is individually classified as a specific priority level. All packets received at the high-priority receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split. bits[4:3] of registers P1CR1, P2CR1, and P3CR1 are used to enable port-based priority for ports 1, 2, and the host port, respectively.

3.3.10 802.1P-BASED PRIORITY

For 802.1p-based priority, the KSZ8463 examines the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bit priority field in the VLAN tag is retrieved and used to look up the “priority mapping” value, as specified by the register SGCR6. The “priority mapping” value is programmable.

Figure 3-8 illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

FIGURE 3-8: 802.1P PRIORITY FIELD FORMAT



802.1p-based priority is enabled by bit[5] of registers P1CR1, P2CR1, and P3CR1 for ports 1, 2, and the host port, respectively.

The KSZ8463 provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the 2 bytes VLAN protocol ID (VPID) and the 2 bytes tag control information field (TCI), is also referred to as the 802.1Q VLAN tag.

Tag insertion is enabled by bit[2] of registers P1CR1, P2CR1, and P3CR1 for ports 1, 2, and the host port, respectively. At the egress port, untagged packets are tagged with the ingress port’s default tag. The default tags are programmed in register sets P1VIDCR, P2VIDCR, and P3VIDCR for ports 1, 2, and the host port, respectively. The KSZ8463 does not add tags to already tagged packets.

Tag removal is enabled by bit[1] of registers P1CR1, P2CR1, and P3CR1 for ports 1, 2, and the host port, respectively. At the egress port, tagged packets will have their 802.1Q VLAN tags removed. The KSZ8463 will not modify untagged packets.

The CRC is recalculated for both tag insertion and tag removal.

3.3.11 802.1P PRIORITY FIELD RE-MAPPING

This is a QoS feature that allows the KSZ8463 to set the “User Priority Ceiling” at any ingress port. If the ingress packet’s priority field has a higher priority value than the default tag’s priority field of the ingress port, the packet’s priority field is replaced with the default tag’s priority field. The “User Priority Ceiling” is enabled by bit[3] of registers P1CR2, P2CR2, and P3CR2 for ports 1, 2, and the host port, respectively.

3.3.12 DIFFSERV-BASED PRIORITY

DiffServ-based priority uses the ToS registers shown in the TOS Priority Control Registers. The ToS priority control registers implement a fully decoded, 128-bit differentiated services code point (DSCP) register to determine packet priority from the 6-bit ToS field in the IP header. When the most significant 6 bits of the ToS field are fully decoded, the resultant of the 64 possibilities is compared with the corresponding bits in the DSCP register to determine priority.

3.3.13 RATE LIMITING SUPPORT

The KSZ8463 supports hardware rate limiting from 64 Kbps to 99 Mbps (refer to Ingress or Egress Data Rate Limits), independently on the “receive side” and on the “transmit side” as per port basis. For 10BASE-T, a rate setting above 10 Mbps means the rate is not limited. On the receive side, the data receive rate for each priority at each port can be limited by setting up ingress rate control registers. On the transmit side, the data transmit rate for each priority queue at each port can be limited by setting up egress rate control registers. The size of each frame has options to include minimum interframe gap (IFG) or preamble byte, in addition to the data field (from packet DA to FCS).

For ingress rate limiting, KSZ8463 provides options to selectively choose frames from all types, multicast, broadcast, and flooded unicast frames. The KSZ8463 counts the data rate from those selected type of frames. Packets are dropped at the ingress port when the data rate exceeds the specified rate limit.

For egress rate limiting, the leaky bucket algorithm is applied to each output priority queue for shaping output traffic. Inter frame gap is stretched on a per frame base to generate smooth, non-burst egress traffic. The throughput of each output priority queue is limited by the egress rate specified.

If any egress queue receives more traffic than the specified egress rate throughput, packets may be accumulated in the output queue and packet memory. After the memory of the queue or the port is used up, packet dropping or flow control will be triggered. As a result of congestion, the actual egress rate may be dominated by flow control/dropping at the ingress end, and may be therefore slightly less than the specified egress rate.

To reduce congestion, it is a good practice to make sure the egress bandwidth exceeds the ingress bandwidth.

3.3.14 MAC ADDRESS FILTERING FUNCTION

When a packet is received, the destination MAC address is looked up in both the static and dynamic MAC address tables. If the address is not found in either of these tables, then the destination MAC address is “unknown”. By default, an unknown unicast packet is forwarded to all ports except the port at which it was received. An optional feature makes it possible to specify the port or ports to which to forward unknown unicast packets. It is also possible to specify no ports, meaning that unknown unicast packets will be discarded. This feature is enabled by setting bit[7] in SGCR7.

The unicast MAC address filtering function is useful in preventing the broadcast of unicast packets that could degrade the quality of this port in applications such as Voice over Internet Protocol (VoIP).

3.4 IEEE 1588 Precision Time Protocol (PTP) Block

The IEEE 1588 precision time protocol (PTP) provides a method for establishing synchronized time across nodes in an Ethernet networking environment. The KSZ8463 implements V2 (2008) of the IEEE 1588 PTP specification.

The KSZ8463 3-port switch implements the IEEE 1588 PTP Version 2 protocol. Port 1 and port 2 can be programmed as either end-to-end (E2E) or peer-to-peer (P2P) transparent clock (TC) ports. In addition, port 3 can be programmed as either slave or master ordinary clock (OC) port. Ingress time stamp capture, egress time stamp recording, correction field update with residence time and link delay, delay turn-around time insertion, egress time stamp insertion, and checksum update are supported. PTP frame filtering is implemented to enhance overall system performance. Delay adjustments are implemented to fine tune the synchronization. Versatile event trigger outputs and time stamp capture inputs are implemented to meet various real time application requirements through GPIO pins.

The key features of the KSZ8463 implementation are as follows:

- Both one-step and two-step transparent clock (TC) operations are supported
- Implementation of precision time clock per specification
  - Upper 16 bits of the second clock not implemented due to practical values of time

- Both E2E and P2P TC are supported on port 1 and port 2
- Both slave and master OC are supported on port 3
- PTP multicast and unicast frame are supported
- Transports of PTP over IPv4/IPv6 UDP and IEEE 802.3/Ethernet are supported
- Both path delay request-response and peer delay mechanism are supported
- Precision time stamping of input signals on the GPIO pins
- Creation and delivery of clocks, pulses, or other unique serial bit streams on the GPIO pins with respect to the precision time clock time.

IEEE 1588 defines two essential functions: The measurement of link and residence (switching) delays by using the Delay_Req/Resp or Pdelay_Req/Resp messages, and the distribution of time information by using the Sync/Follow_Up messages. The 1588 PTP event messages are periodically sent from the grandmaster in the network to all slave clock devices. Link delays are measured by each slave node to all its link partners to compensate for the delay of PTP messages sent through the network.

The 1588 PTP Announce messages are periodically sent from the grandmaster(s) in the network to all slave clock devices. This information is used by each node to select a master clock using the “best master clock” algorithm.

1588 PTP (Version 2) defines two types of messages: event and general messages. These are summarized below and are supported by the KSZ8463:

Event Messages (an accurate time stamp is generated at egress and ingress):

- Sync (from master to slave)
- Delay_Req (from slave to master)
- Pdelay_Req (between link partners for peer delay measurement)
- Pdelay_Resp (between link partners for peer delay measurement)

General Messages:

- Follow_Up (from Master to Slave)
- Delay_Resp (from Master to Slave)
- Pdelay_Resp_Follow_Up (between link partners for peer delay measurement)
- Announce
- Management
- Signaling

3.4.1 IEEE 1588 PTP CLOCK TYPES

The KSZ8463 supports the following clock types:

- Ordinary Clock (OC) is defined as a PTP clock with a single PTP port in a PTP domain. It may serve as a source of time such as a master clock, or it may be a slave clock which synchronizes to another master clock.
- End-to-End Transparent Clock (E2E TC) is defined as a transparent clock that supports the use of the end-to-end delay measurement mechanism between a slave clock and the master clock. In this method, the E2E TC intermediate devices do not need to be synchronized to the master clock and the end slave node is directly synchronized to the master clock. The E2E TC/SC slave intermediate devices can also be synchronized to the master clock. Note that the transparent clock is not a real clock that can be viewed on an oscilloscope but rather it is a mechanism by which delay are accounted for when transporting information across and through physical network nodes.
- Peer-to-Peer Transparent Clock (P2P TC for Version 2) is defined as a transparent clock, in addition to providing PTP event transit time information. P2P TC also provides corrections for the propagation delay between nodes (link partners) by using Pdelay_Req (Peer Delay Request) and Pdelay_Resp (Peer Delay Response). In this method, the P2P TC intermediate devices can be synchronized to the master clock. A transparent clock (TC) is not part of the master-slave hierarchy. Instead, it measures the resident time which is the time taken for a PTP message to traverse the node. The P2P TC then provides this information to the clock receiving the PTP message. In addition, the P2P TC measures and passes on the link delay of the receiving PTP message. Note that the transparent clock is not a real clock that can be viewed on an oscilloscope but rather it is a mechanism by which delay are accounted for when transporting information across and through physical network nodes.
- Master clock is defined as a clock which is used as the reference clock for the entire system. The KSZ8463 can operate as a master clock if needed. However, the quality of the clock signal will be limited by the quality of the crystal or oscillator used to clock the device.

Note that P2P and E2E TCs cannot be mixed on the same communication path.

3.4.2 IEEE 1588 PTP ONE-STEP OR TWO-STEP CLOCK OPERATION

The KSZ8463 supports either 1-step or 2-step clock operation.

- One-Step Clock Operation: A PTP message (Sync) exchange that provides time information using a single event message which eliminates the need for a Follow_Up message to be sent. This one-step operation will eliminate the need for software to read the time stamp and to send a Follow_Up message.
- Two-Step Clock Operation: A PTP messages (Sync/Follow_Up) that provides time information using the combination of an event message and a subsequent general message. The Follow_Up message carries a precise estimate of the time the sync message was placed on the PTP communication path by the sending node.

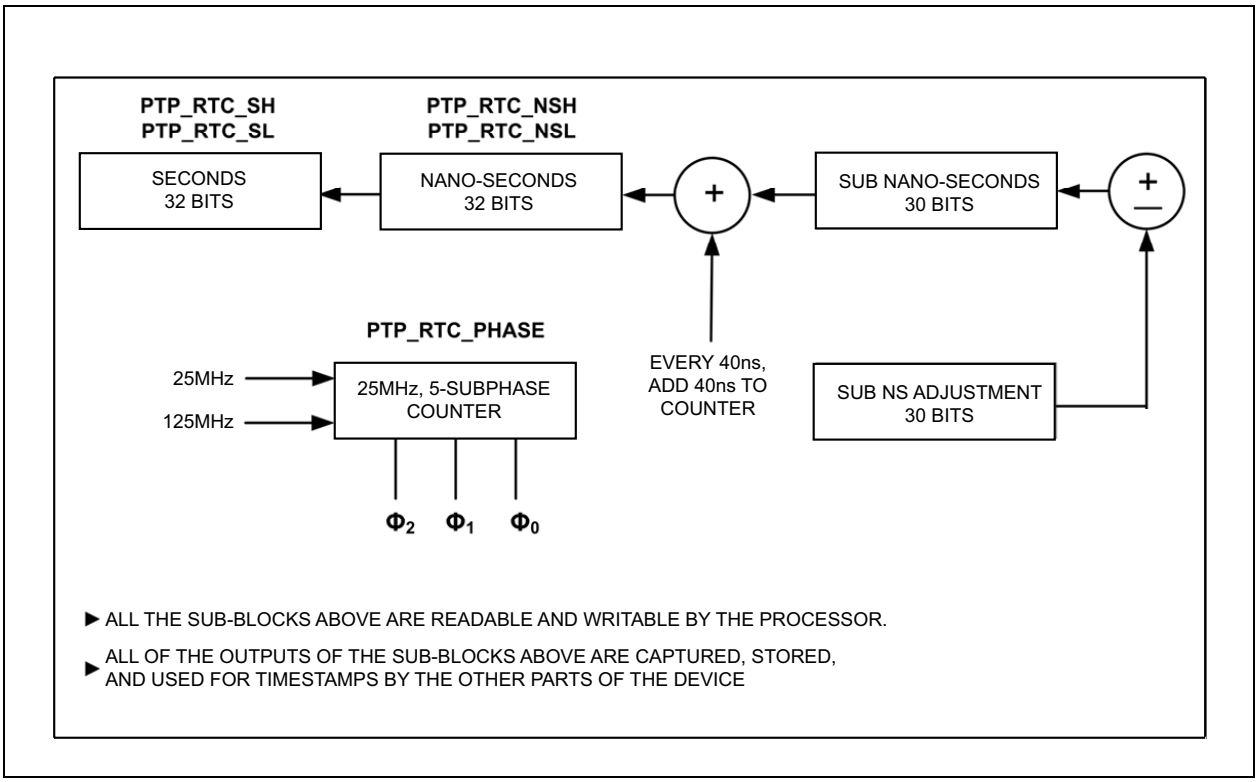
3.4.3 IEEE 1588 PTP BEST MASTER CLOCK SELECTION

The IEEE 1588 PTP specification defines an algorithm based on the characteristics of the clocks and system topology called best master clock (BMC) algorithm. BMC uses announce messages to establish the synchronization hierarchy. The algorithm compares data from two clocks to determine the better clock. Each clock device continuously monitors the announce messages issued by the current master and compares the dataset to itself. The software controls this process.

3.4.4 IEEE 1588 PTP SYSTEM TIME CLOCK

The system time clock (STC) in KSZ8463 is a readable or writable time source for all IEEE 1588 PTP-related functions and contains three counters: a 32-bit counter for seconds, a 30-bit counter for nanoseconds and a 32-bit counter for sub-nanoseconds (units of 2^{-32} ns). Figure 3-9 shows the PTP Clock.

FIGURE 3-9: PTP SYSTEM CLOCK OVERVIEW



The STC is clocked (incremented by 40 ns or updated with sub-nanosecond carry info) every 40 ns by a derivative of the 125 MHz derived clock. The 30-bit nanosecond counter will be numerically incremented by 40 ns every 40 ns. There is another 3-bit phase counter that is designed to indicate one of the five sub-phases (0 ns, 8 ns, 16 ns, 24 ns, or 32 ns) within the 40 ns period. This provides finer resolution for the various messages and time stamps. The overflow for the 30-bit nanosecond counter is 0x3B9ACA00 (109) and the overflow for the 32-bit sub-nanosecond counter is 0xFFFFFFFF.

The system time clock does not support the upper 16-bits of the seconds field as defined by the IEEE 1588 PTP Version 2 which specifies a 48-bit seconds field. If the 32-bit seconds counter overflows, it will have to be handled by software. Note that an overflow of the seconds field only occurs every 136 years.

The seconds value is kept track of in the PTP_RTC_SH and PTP_RTC_SL registers (0x608 – 0x60B). The nanoseconds value is kept track of in the PTP_RTC_NSH and PTP_RTC_NSL registers (0x604 – 0x607).

The PTP_RTC_PHASE clock register (0x60C – 0x60D) is initialized to zero whenever the local processor writes to the PTP_RTC_NSL, PTP_RTC_NSH, PTP_RTC_SL, and PTP_RTC_SH registers.

During normal operation when the STC clock is keeping synchronized real time, and not while it is undergoing any initialization manipulation by the processor to get it close to the real time, the PTP_RTC_PHASE clock register will be reset to zero at the beginning of the current 40 ns STC clock update interval. It will start counting at zero at the beginning of the 40 ns period and every 8 ns it will be incremented. The information provided by the PTP_RTC_PHASE register will increase the accuracy of the various time stamps and STC clock readings.

3.4.5 UPDATING THE SYSTEM TIME CLOCK

The KSZ8463 provides four mechanisms for updating the system time clock:

- Directly Setting or Reading the Time
- Step-Time Adjustment
- Continuous Time Adjustment
- Temporary Time Adjustment

3.4.5.1 Directly Setting or Reading the Time

Directly setting the system time clock to a value is accomplished by setting a new time in the real time clock registers (PTP_RTC_SH/L, PTP_RTC_NSH/L and PTP_RTC_PHASE) and then setting the load PTP 1588 clock bit (PTP_LOAD_CLK).

Directly reading the system time clock is accomplished by setting the read PTP 1588 clock bit (PTP_READ_CLK). To avoid lower bits overflowing during reading the system time clock, a snapshot register technique is used. The value in the system time clock will be saved into a snapshot register by setting the PTP_READ_CLK bit in PTP_CLK_CTL, and then subsequent reads from PTP_RTC_S, PTP_RTC_NS, and PTP_RTC_PHASE will return the system time clock value. The CPU will add the PTP_RTC_PHASE value to PTP_RTC_S and PTP_RTC_NS to get the exact real time.

3.4.5.2 Step-Time Adjustment

The system time clock can be incremented in steps if desired. The nanosecond value (PTP_RTC_NSH/L) can be added or subtracted when the PTP_STEP_ADJ_CLK bit is set. The value will be added to the system time clock if this action occurs while the PTP_STEP_DIR bit = “1”. The value will be subtracted from the system time clock if this action occurs while the PTP_STEP_DIR bit = “0”. The PTP_STEP_ADJ_CLK bit is self-clearing.

3.4.5.3 Continuous Time Adjustment

The system can be set up to perform continuous time adjustment to the 1588 PTP clock. This is the mode that is anticipated to be used the most. This mode is overseen by the local processor and provides a method of periodically adjusting the count of the PTP clock to match the time of the master clock as best as possible. The rate registers (PTP_SNS_RATE_H and PTP_SNS_RATE_L) (0x610 – 0x613) are used to provide a value by which the sub-nanosecond Portion of the clock is adjusted on a periodic basis. While continuous adjustment mode (PTP_CONTINU_ADJ_CLK = “1”) is selected every 40 ns the sub-nanosecond value of the clock will be adjusted in either a positive or negative direction as determined by the PTP_RATE_DIR bit. The value will be positively adjusted if PTP_RATE_DIR = “0” or negatively adjusted if PTP_RATE_DIR = “1”. The rate adjustment allows for correction with resolution of 2^{-32} ns for every 40 ns reference clock cycle, and it will be added to or subtracted from the system time clock on every reference clock cycle right after the write to PTP_SNC_RATE_L is done. To stop the continuous time adjustment, one can either set the PTP_CONTINU_ADJ_CLK = “0” or the PTP_SNS_RATE_H/L value to zero.

3.4.5.4 Temporary Time Adjustment

This mode allows for the continuous time adjustment to take place over a specified period of time only. The period of time is specified in the PTP_ADJ_DURA_H/L registers. This mode is enabled by setting the PTP_TEMP_ADJ_CLK bit to one. Once the duration is reached, the increment or decrement will cease. When the temporary time adjustment is done, the internal duration counter register (PTP_ADJ_DURA_H/L) will stay at zero, which will disable the time adjustment. The local processor needs to set the PTP_TEMP_ADJ_CLK to one again to start another temporary time adjustment with the reloaded value into the internal rate and duration registers. The PTP_ADJ_DURA_L register needs to be

programmed before PTP_ADJ_DURA_H register. The PTP_ADJ_DURA_L, PTP_ADJ_DURA_H and PTP_SNS_RATE_L registers need to be programmed before the PTP_SNS_RATE_H register. The temporary time adjustment will start after the PTP_TEMP_ADJ_CLK bit is set to one. This bit is self-cleared when the adjustment is completed. Software can read this bit to check whether the adjustment is still in progress.

3.4.5.5 PTP Clock Initialization

During software initialization when the device is powering up, the PTP clock needs to be initialized in preparation for synchronizing to the master clock. The suggested order of tasks is to reset the PTP 1588 clock (RESET_PTP_CLK = “0”), load the PTP 1588 clock (PTP_LOAD_CLK = “1”) with a value then enable the PTP 1588 clock (EN_PTP_CLK = “1”). During the initial synchronization attempt, the system time clock may be a little far apart from the PTP master clock, so it most likely will require a step-time adjustment to get it closer. After that, the continuous time adjustment method or temporary time adjustment method may be the best options when the system time clock is close to being synchronized with the master clock.

More details on the 1588 PTP system time clock controls and functions can be found in the register descriptions for registers 0x600 to 0x617.

3.4.6 IEEE 1588 PTP MESSAGE PROCESSING

The KSZ8463 supports IEEE 1588 PTP time synchronization when 1588 PTP mode and message detection are enabled in the PTP_MSG_CFG_1 register (0x620 – 0x621). Different operations will be applied to PTP packet processing based on the setting of P2P or E2E in transparent clock mode for port 1 and port 2, master or slave in ordinary clock mode for port 3 (host port), one-step or two-step clock mode, and if the domain checking is enabled. For the IPv4/UDP egress packet, the checksum can be updated by either re-calculating the two-bytes or by setting it to zero. For the IPv6/UDP egress packet, the checksum is always updated. All these 1588 PTP configuration bits are in the PTP_MSG_CFG_1/2 registers (0x620 – 0x623).

For a more detailed description of the 1588 PTP message processing control and function, please refer to the register descriptions in the register map at locations 0x620 to 0x68F.

3.4.6.1 IEEE 1588 PTP Ingress Packet Processing

The KSZ8463 can detect all IEEE 802.3 Ethernet 1588 PTP packets, IPv4/UDP 1588 PTP packets, and IPv6/UDP 1588 PTP packets by enabling these features in the PTP_MSG_CFG_1 register (0x620 – 0x621). Upon detection of receiving a 1588 PTP packet, the device will capture the receive time stamp at the time when the start-of-frame delimiter (SFD) is detected. Adjusting the receive time stamp with the receive latency or asymmetric delay is the responsibility of the software. The hardware only takes these values into consideration when it updates the correction field in the PTP message header. Likewise, the software needs to adjust the transmit time stamp with the transmit latency. Both the ingress time stamp and the ingress port number will be embedded in the reserved fields of the 1588 PTP header. The embedded information will be used by the host to designate the destination port in the response egress packet, identify the direction of the master port, and to calculate the link delay and offset.

The 1588 PTP packet will be discarded if the 1588 PTP domain field does not match the domain number in the PTP_DOMAIN_VER register (0x624 – 0x625) or if the 1588 PTP version number does not match version number (either 1 or 2) in the PTP_DOMAIN_VER register (0x624 – 0x625). Packets with a version number of one will always be forwarded to port 1 or port 2, and not to port 3.

The 1588 PTP packets that are not associated with packet messages in pairs (Pdelay_ Req with Pdelay_Resp, Sync with Follow_Up, Delay_Req with Delay_Resp) can be filtered and not forwarded to port 3 if the corresponding enable bits are set in the PTP_MSG_CFG_2 register (0x0622 – 0x623). The 1588 PTP version-1 packet will be forwarded without being modified.

3.4.6.2 IEEE 1588 PTP Egress Packet Processing

The ingress time stamp, the transport type of the 1588 PTP packet, the packet type (tagged or untagged), and the type of correction field update on the egress side are in the frame header and are accessible for modification by the egress logic in local switch packet memory. The 1588 PTP packet will be put in the egress queue of highest priority. From the 1588 PTP frame header inside the switch packet memory, the egress logic will get the correction field update instruction. The residence time, link delay in the PTP_P1/2_LINK_DLY registers (0x646 – 0x647 and 0x666 – 0x667) or turn-around time might be added to the correction field depending upon the type of 1588 PTP egress packet. The 1588 PTP packet received from port 3 (host port) has the destination port information to forward as well as the time stamp information that will be used for updating the correction field in one-step clock operation.

This embedded information (in the reserved fields of 1588 PTP frame header) will be zeroed out before the egress packet is sent out to conform to the 1588 PTP standard.

For one-step operation, the original time stamp will be inserted into the sync packet. The egress time stamp of the Sync packet will be latched in the P1/2_SYNC_TS registers (0x64C – 0x64F and 0x66C – 0x66F), the egress time stamps of Delay_Req, Pdelay_Req and Pdelay_Resp will be latched in the P1/2_XDLY_REQ_TS (0x648 – 0x64B and 0x668 – 0x6B) and P1/2_PDLY_RESP_TS registers (0x650 – 0x653 and 0x670 – 0x673). These latched egress time stamps will generate an interrupt to the host CPU and set the interrupt status bits in the PTP_TS_IS register (0x68C – 0x68D) if the interrupt enable is set in the PTP_TS_IE register (0x68E – 0x68F). These captured egress time stamps will be used by the 1588 PTP software for link delay measurement, offset adjustment, and time calculation.

The transmit delay value from the port 1 or port 2 time stamp reference point to the network connection point in the PTP_P1/2_TX_LATENCY registers (0x640 – 0x643) will be added to these value in the P1/2_SYNC_TS, P1/2_XDLY_REQ_TS and P1/2_PDLY_RESP_TS registers to get the egress time stamp with reference point to the network connection point. For transmit Delay_Req or Pdelay_Req packets, the value in the PTP_P1/2_ASYM_COR registers (0x644 – 0x645 and 0x664 – 0x665) will be subtracted from the correction field.

3.4.7 IEEE 1588 PTP EVENT TRIGGERING AND TIME STAMPING

An event trigger output signal can be generated when the target and activation time matches the IEEE 1588 PTP system clock time. Likewise, an event time stamp input can be captured from an external event input signal and the corresponding time on the IEEE 1588 PTP system clock will be captured.

Up to 12 GPIO pins can be configured as either output signal when trigger target time is matching IEEE 1588 PTP system clock time or monitoring input signal for external event time stamp. All event trigger outputs are generated by comparing the system clock time with trigger target time continuously to make sure time synchronization is always on-going.

3.4.7.1 IEEE 1588 PTP Trigger Output

The KSZ8463 supports up to 12 event trigger units which can output to any one of the 12 GPIO pins by setting bits[3:0] in TRIG[1:12]_CFG_1 registers. Multiple trigger units can be assigned to a single GPIO pin at the same time as logical OR'ed function allowing generation of more complex waveforms. Also multiple trigger units can be cascaded (one Unit only at any time) to drive a single GPIO pin to generate a long and repeatable bit sequence. Each trigger unit that is cascaded can be any signal type (edge, pulse, periodic, register-bits, and clock output).

Each trigger unit can be programmed to generate one time rising or falling edge (toggle mode), a single positive or negative pulse of programmable width, a periodic signal of programmable width, cycle time, bit-patterns to shift out from TRIG[1:12]_CFG_[1:8] registers, and each trigger Unit can be programmed to generate interrupt of trigger output Unit done and status in PTP_TRIG_IE/IS registers. For each trigger Unit, the host CPU programs the desired output waveform, GPIO pins, target time in TRIG[1:12]_TGT_NS and TRIG[1:12]_TGT_S registers that the activity is to occur, and enable the trigger output Unit in TRIG_EN register, then the trigger output signal will be generated on the GPIO pin when the internal IEEE 1588 PTP system time matches the desired target time. The device can be programmed to generate a pulse-per-second (PPS) output signal. The maximum trigger output signal frequency is up to 12.5 MHz.

For a more detailed description of the 1588 PTP event trigger output control, configuration and function, please refer to the registers description in the register map from 0x200 to 0x397 locations.

3.4.7.2 IEEE 1588 PTP Event Time Stamp Input

External event inputs on the GPIO pins can be monitored and time stamped with the resolution of 8 ns. The external signal event can be monitored and detected as either rising edge, falling edge, positive pulse, or negative pulse by setting bits[7:6] in TS[1:12]_CFG registers. Multiple time stamp units can be cascaded or chained together to associate with a single GPIO pin to detect a series of events. When event is detected, the time stamp will be captured in three fields: 32-bit second field in TS[1:12]_SMPL1/2_SH/L registers, 30-bit nanosecond field in TS[1:12]_SMPL1/2_NSH/L registers, and 3-bit phase field in TS[1:12]_SMPL1/2_SUB_NS registers. Second and nanosecond fields are updated every 25 MHz clock cycle. The 3-bit phase field is updated every 125 MHz clock cycle and indicates one of the five 8 ns/125 MHz clock cycles. The bit [14] in TS[1:12]_SMPL1/2_NSH registers indicates the event time stamp input is either falling edge or rising edge.

The KSZ8463 supports up to twelve time stamp input units which can input from any one of the twelve GPIO pins by setting bits[11:8] in TS[1:12]_CFG registers. The enable bits [11:0] in TS_EN register are used to enable the time stamp units. The last time stamp unit (Unit 12) can support up to eight time stamps for multiple event detection and up to four pulses can be detected. The rest of the units (units 1 through 11) have two time stamps to support single edge or pulse detection. Pulse width can be measured by the time difference between consecutive time stamps. When an input event is detected, one of the bits [11:0] in TS_RDY register is asserted and will generate a time stamp interrupt if the PTP_TS_IE bit is set. The host CPU is also expected to read the time stamp status in the TS[1:12]_STATUS registers to report the number of detected event (either rising or falling edge) counts and overflow. In single mode, it can detect

up to fifteen events at any single Unit. In cascade mode, it can detect up to two events at units 1 through 11 or up to eight events at Unit 12, and it can detect up to fifteen events for any unit as a tail unit. Pulses or edges can be detected up to 25 MHz.

For more details on 1588 PTP event time stamp input control, configuration and function, please refer to the register descriptions for locations 0x400 to 0x5FD in the register map.

3.4.7.3 IEEE 1588 PTP Event Interrupts

All IEEE 1588 PTP event trigger and time stamp interrupts are located in the PTP_TRIG_IE/PTP_TS_IE enable registers and the PTP_TRIG_IS/PTP_TS_IS status registers. These interrupts are fully maskable via their respective enable bits and shared with other interrupts that use the INTRN interrupt pin.

These twelve event trigger output status interrupts are logical OR'ed together and connected to bit[10] in the ISR register.

These twelve event trigger output enable interrupts are logical OR'ed together and connected to bit[10] in the IER register.

These twelve time stamp status interrupts are logical OR'ed together with the rest of bits in this register and the logical OR'ed output is connected to bit[12] in the ISR register.

These twelve time stamp enable interrupts are logical OR'ed together with the rest of bits in this register and the logical OR'ed output is connected to bit[12] in the IER register.

3.4.7.4 IEEE 1588 GPIO

The KSZ8463 supports twelve GPIO pins that can be used for general I/O or can be configured to utilize the timing of the IEEE 1588 protocol. These GPIO pins can be used for input event monitoring, outputting pulses, outputting clocks, or outputting unique serial bit streams. The GPIO output pins can be configured to initiate their output upon the occurrence of a specific time which is being kept by the onboard precision time clock. Likewise, the specific time of arrival of an input event can be captured and recorded with respect to the precision time clock. Refer to the General Purpose and IEEE 1588 Input/Output (GPIO) section for details on the operation of the GPIO pins.

3.5 General Purpose and IEEE 1588 Input/Output (GPIO)

3.5.1 OVERVIEW

The KSZ8463 devices incorporate a set of general purpose input/output (GPIO) pins that are configurable to meet the needs of many applications. The input and output signals on the GPIO pins can be directly controlled via a local processor or they can be set up to work closely with the IEEE 1588 protocol to create and/or monitor precisely timed signals which are synchronous to the precision time clock. Some GPIO pins are dedicated, while others are dual function pins. Dual function pins are managed by the IOMXSEL register. Table 3-6 provides a convenient summary of available GPIO resources in the KSZ8463 devices.

TABLE 3-6: GPIO PIN REFERENCE

KSZ8463ML and KSZ8463FML			KSZ8463RL and KSZ8463FRL		
GPIO	**Pin Number**	**Function**	**GPIO**	**Pin Number**	**Function**
GPIO_0	48	GPIO0	GPIO_0	48	GPIO0
GPIO_1	49	GPIO1	GPIO_1	49	GPIO1
GPIO_2	52	GPIO2	GPIO_2	52	GPIO2
GPIO_3	53	GPIO3	GPIO_3	53	GPIO3
GPIO_4	54	GPIO4	GPIO_4	54	GPIO4
GPIO_5	55	GPIO5	GPIO_5	55	GPIO5
GPIO_6	58	GPIO6	GPIO_6	58	GPIO6
GPIO_7	59	P1LED1/ GPIO7_MLI	GPIO_7	38	GPIO7_RLI
GPIO_8	46	GPIO8	GPIO_8	46	GPIO8
GPIO_9	61	P2LED1/ GPIO9_MLI	GPIO_9	36	GPIO9_RLI

TABLE 3-6: GPIO PIN REFERENCE (CONTINUED)

KSZ8463ML and KSZ8463FML			KSZ8463RL and KSZ8463FRL		
GPIO	**Pin Number**	**Function**	**GPIO**	**Pin Number**	**Function**
GPIO_10	62	P2LED0/ GPIO10_MLI	GPIO_10	37	GPIO10_RLI
GPIO_11	47	GPIO11	GPIO_11	47	GPIO11

3.5.2 GPIO PIN FUNCTIONALITY CONTROL

The GPIO_OEN register is used to configure each GPIO as an input or an output. Each GPIO pin has a set of registers associated with it that are configured to determine its functionality, and any relationship it has with other GPIO pins or registers. Each GPIO pin can be configured to output a binary signal state or a serial sequence of bits. Each GPIO pin can output a single serial bit pattern or it can be programmed to continuously loop and output the pattern until stopped. The duration of the high and low periods within the sequential bit patterns can be programmed to meet the requirements of the application. The output can be triggered to occur at any time by the local processor writing to the correct register or it can be triggered by the local IEEE precision timing protocol clock being equal to an exact time. The local processor can interrogate any GPIO pin at any time or the value of the IEEE precision time protocol clock can be captured and recorded when the specified event occurs on any of the GPIO pins. The control and output of the GPIO pins can be cascaded to create complex digital output sequences and waveforms. Lastly, the units can be programmed to generate an interrupt on specific conditions.

The control structure for the twelve GPIO pins are organized into two separate units called the trigger output units (TOU) and the time stamp input units (TSU). There are twelve TOUs and twelve TSUs which can be used with any of the GPIO pins. There are 32 control bytes for each of the two units to control the functionality. The depth of control is summarized in Table 3-7.

TABLE 3-7: TRIGGER OUTPUT UNITS AND TIME STAMP INPUT UNITS SUMMARY

Trigger Output Units	Time Stamp Input Units
32 Bytes of Parameters	32 Bytes of Parameters
Trigger Patterns: Negative Edge, Positive Edge, Negative Pulse, Positive Pulse, Negative Period, Positive Period, Register Output Shift	Detection: Negative or Positive Edges Negative or Positive Pulses
Pulse Width: 16-Bit Counter @ 8 ns Each (524288 ns, maximum)	Two Edge/One Pulse (Two Time Stamps) Detection Capability (time stamp Units 10:0)
Cycle Width: 32-Bit Counter @ 1 ns Each (4.29 seconds, maximum)	Eight Edge/Four Pulse (Eight Time Stamps) Detection (time stamp Unit 11)
Cycle Count: 16-Bit Counter (0 = Infinite Loop)	Cascadable to Detect Multiple Edges
Total Cascade Mode Cycle Time: 32-Bit Counter @ 1 ns Each	—
Shift Register: 16-Bits (only for register shift output mode)	—
Cascadable to Generate Complex Waveforms	—

3.5.3 GPIO PIN CONTROL REGISTER LAYOUT

Most of the registers used to control the time stamp units and the trigger output units are duplicated for each GPIO pin.

There are a few registers which are associated with all the overall functionality of all the GPIO pins or only specific GPIO pins. These are summarized in Table 3-8.

TABLE 3-8: GPIO REGISTERS AFFECTING EITHER ALL OR SPECIFIC UNITS

Register Name	Register Location	Related to Which Trigger Output Units or Time Stamping Units
Trigger Error Register – TRIG_ERR	0x200 – 0x201	All trigger output units.
Trigger Active Register – TRIG_ACTIVE	0x202 – 0x203	All trigger output units.

TABLE 3-8: GPIO REGISTERS AFFECTING EITHER ALL OR SPECIFIC UNITS (CONTINUED)

Register Name	Register Location	Related to Which Trigger Output Units or Time Stamping Units
Trigger Done Register – TRIG_DONE	0x204 – 0x205	All trigger output units.
Trigger Enable Register – TRIG_EN	0x206 – 0x207	All trigger output units.
Trigger SW Reset Register – TRIG_SW_RST	0x208 – 0x209	All trigger output units.
Trigger Unit 12 Output PPS Pulse-Width Register – TRIG12_PPS_WIDTH	0x20A – 0x20B	Trigger output Unit 1, 12.
Time Stamp Ready Register – TS_RDY	0x400 – 0x401	All trigger output units.
Time Stamp Enable Register – TS_EN	0x402 – 0x403	All trigger output units.
Time Stamp Software Reset Register – TS_SW_RST	0x404 – 0x405	All trigger output units.

FIGURE 3-10: TRIGGER OUTPUT UNIT ORGANIZATION AND ASSOCIATED REGISTERS

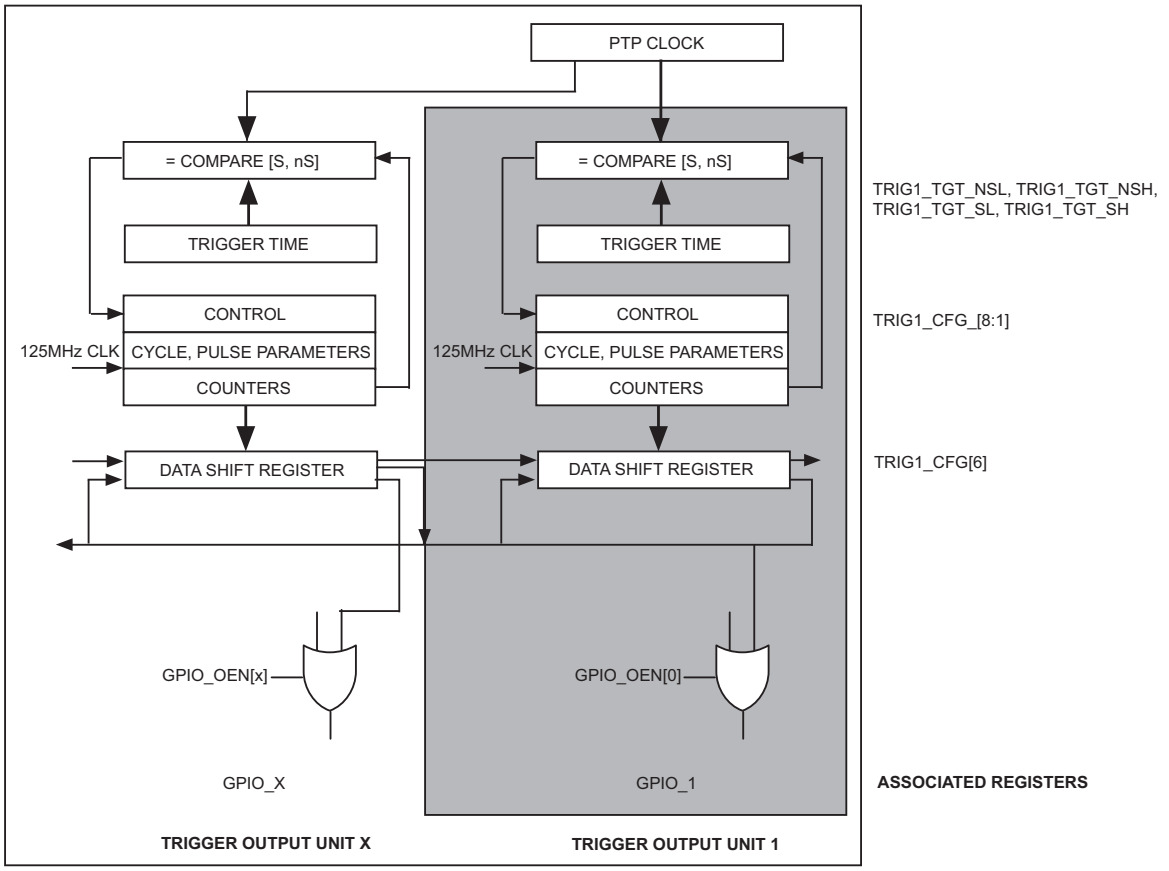
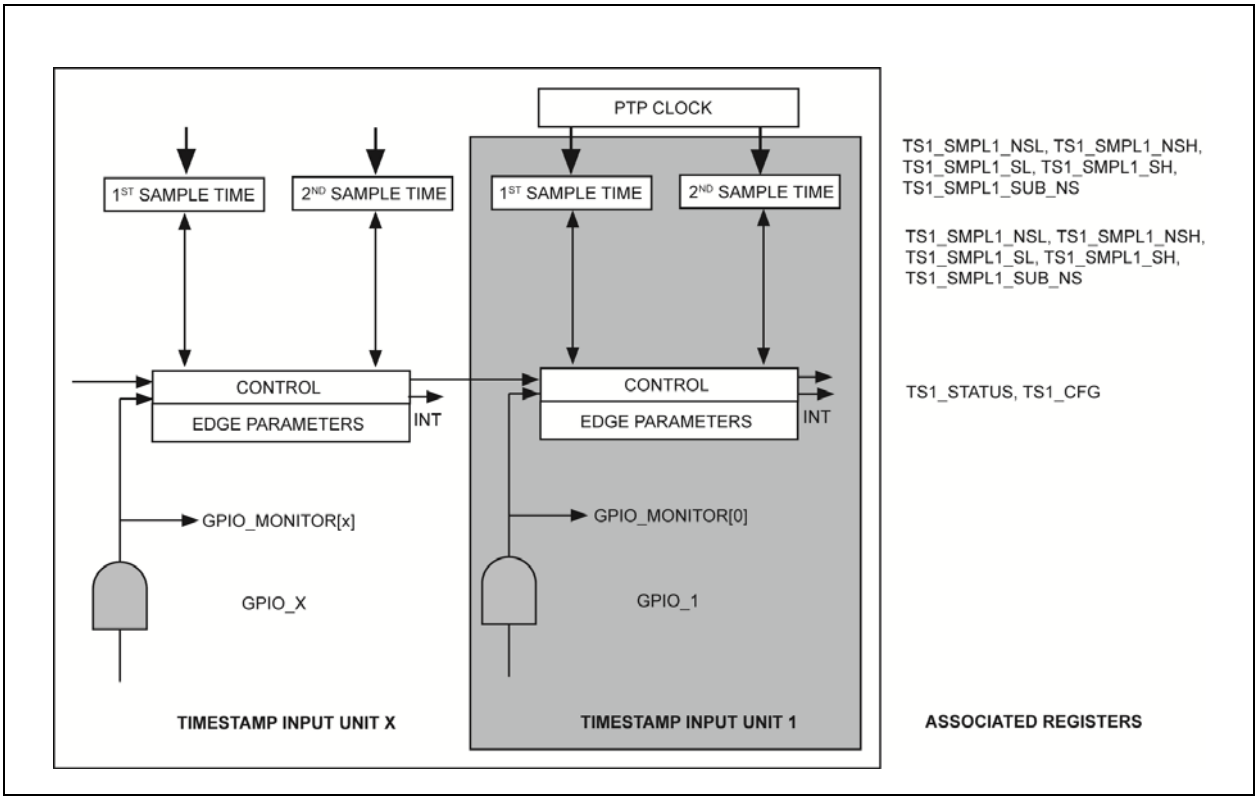


FIGURE 3-11: TIME STAMP INPUT UNIT ORGANIZATION AND ASSOCIATED REGISTERS



3.5.4 GPIO TRIGGER OUTPUT UNIT AND TIME STAMP UNIT INTERRUPTS

The trigger output units and the time stamp units can be programmed to generate interrupts when specified events occur. The interrupt control structure is shown in Figure 3-12 and Figure 3-13.

FIGURE 3-12: TRIGGER UNIT INTERRUPTS

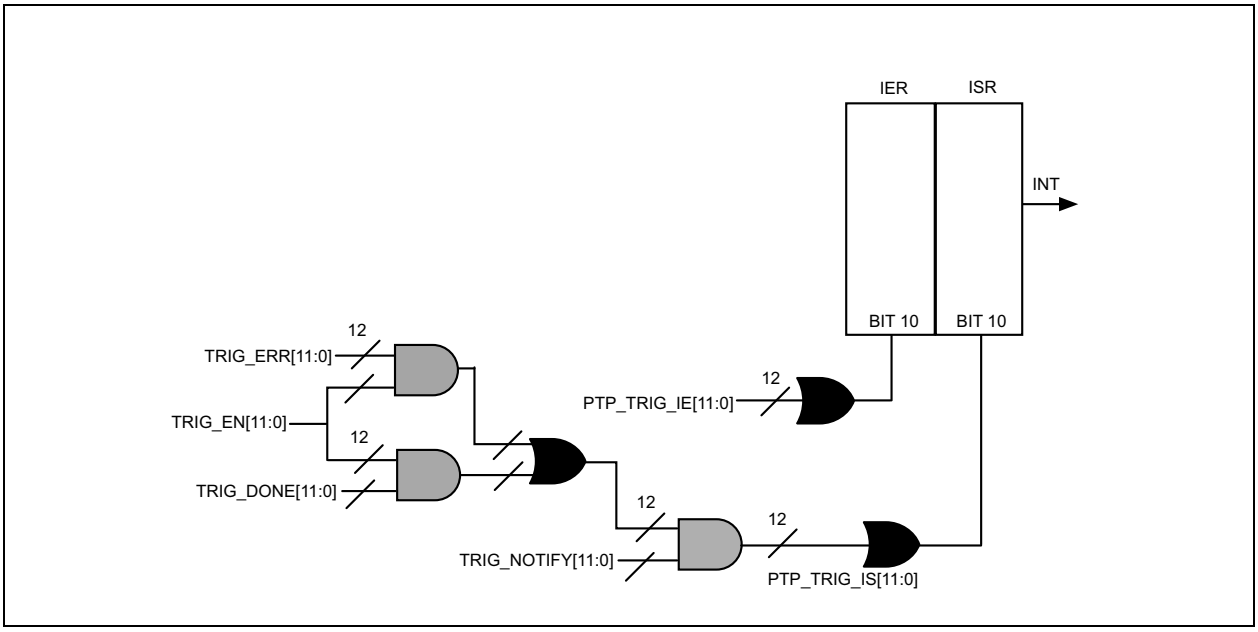
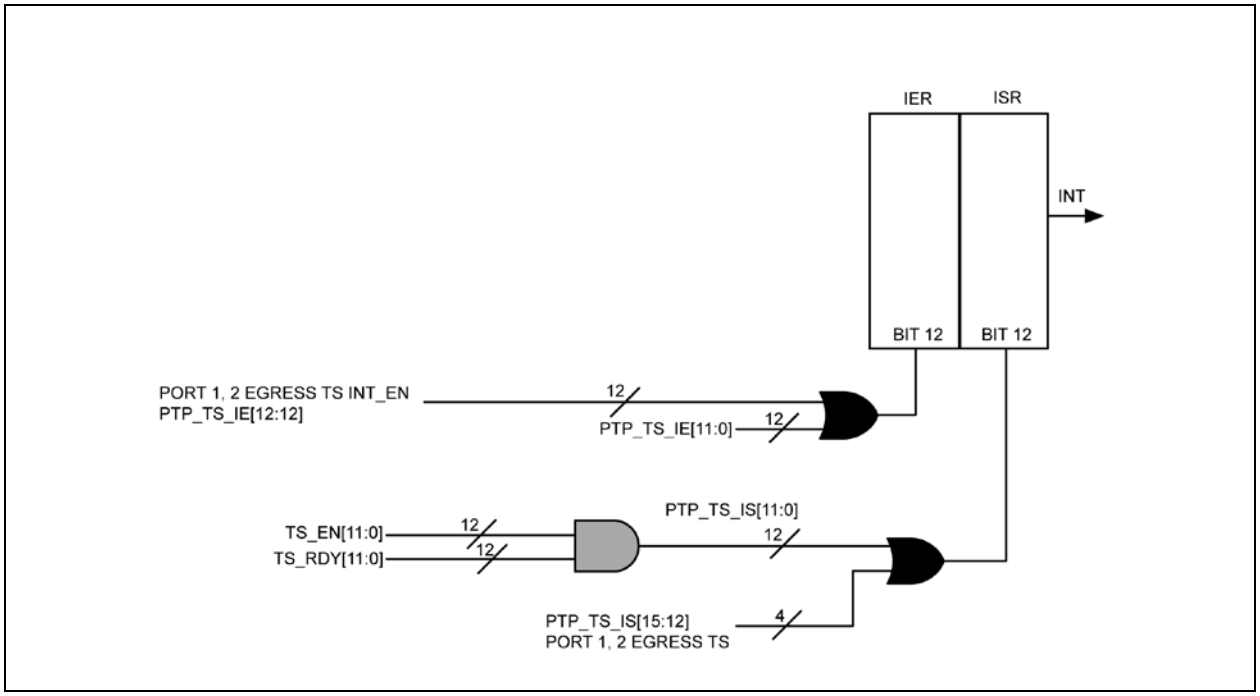


FIGURE 3-13: TIME STAMP UNIT INTERRUPTS



3.6 Using the GPIO Pins with the Trigger Output Units

The twelve trigger output units (TOU) can be used to generate a variety of pulses, clocks, waveforms, and data streams at user-selectable GPIO pins. The TOUs will generate the user-specified output starting at a specific time with respect to the IEEE 1588 precision time clock. This section provides some information on configuring the TOUs to generate specific types of output. In the information below, the value “x” represents one of the twelve TOUs. Because this area of the device is very flexible and powerful, please reference application note ANLAN203, *KSZ84xx GPIO Pin Output Functionality*, for additional information on creating specific types of waveforms and utilizing this feature.

When using a single TOU to control multiple GPIO pins, there are several details of functionality that must be taken into account. When switching between GPIO pins, the output value on those pins can be affected. If a TOU changes the GPIO pin level to a high value, writing to this units configuration register to change the addressed GPIO pin to a different one will cause the hardware to drop the level in the previous GPIO pin and set the new GPIO pin to a high value. To prevent the second GPIO pin from going high immediately, the TOU must be reset prior to programming in a different GPIO pin value.

3.6.1 CREATING A LOW-GOING PULSE AT A SPECIFIC TIME

- Specifying the Time

The desired trigger time will be set in TRIGx_TGT_NSH, TRIGx_TGT_NSL, TRIGx_TGT_SH, and TRIGx_TGT_SL registers.

- Specifying the Pulse Parameters

TRIGx_CFG_1[6:4] = “010” for negative pulse generation.

TRIGx_CFG_2[15:0] = Pulse width where each Unit is 8 ns.

- Associate this Trigger Output Unit to a Specific GPIO Pin

TRIGx_CFG_1[3:0] = Selects GPIO pin to use.

- Set Up Interrupts, if Needed

If it is desired to get notification that the trigger output event occurred set up the following registers.

TRIGx_CFG_1, bit[8] (Trigger Notify) = “1” is one requirement for enabling interrupt on done or error.

Set the corresponding trigger Unit interrupt enable bit in the PTP_TRIG_IE register.

• Enabling the Trigger Output Unit

Set the corresponding trigger Unit enable bit in the TRIG_EN register.

Be aware that for a low-going pulse in non-cascaded mode (single mode), the output will be driven by the unit to a high level when the trigger unit is enabled. In cascade mode, the output will be driven by the unit to the high state 8 ns prior to the programmed trigger time.

3.6.2 CREATING A HIGH-GOING PULSE AT A SPECIFIC TIME

• Specifying the Time

The desired trigger time will be set in TRIGx_TGT_NSH, TRIGx_TGT_NSL, TRIGx_TGT_SH, and TRIGx_TGT_SL registers.

• Specifying the Pulse Parameters

TRIGx_CFG_1[6:4] = “011” for positive pulse generation.

TRIGx_CFG_2[15:0] = Pulse width where each Unit is 8 ns.

• Associate this Trigger Output Unit to a Specific GPIO Pin

TRIGx_CFG_1[3:0] = Selects GPIO pin to use.

• Set Up Interrupts if Needed

If it is desired to get notification that the trigger output event occurred set up the following registers.

TRIGx_CFG_1, bit[8] (Trigger Notify) = “1” is one requirement for enabling interrupt on done or error.

Set the corresponding trigger Unit interrupt enable bit in the PTP_TRIG_IE register.

• Enabling the Trigger Output Unit

Set the corresponding trigger Unit enable bit in the TRIG_EN register.

Be aware that for a high-going pulse in non-cascaded mode (single mode), the output will be driven by the unit to a low level when the trigger unit is enabled. In cascade mode, the output will be driven by the unit to the low state 8 ns prior to the programmed trigger time.

3.6.3 CREATING A FREE RUNNING CLOCK SOURCE

• Specifying the Time

Typically there is no need to set up a desired trigger time with respect to a free running clock. There are two ways that the free running clock can be started.

Set up a desired trigger time in the TRIGx_TGT_NSH, TRIGx_TGT_NSL, TRIGx_TGT_SH, and TRIGx_TGT_SL registers.

After parameters have been set up, start the clock by setting the Trigger Now bit, bit[9], in the TRIGx_CFG_1 register.

• Specifying the Clock Parameters

TRIGx_CFG_1[6:4] = “101” for generating a positive periodic signal.

High part of cycle defined by bits[15:0] in the TRIGx_CFG_2 register. Each Unit is 8 ns.

Cycle width defined by bits[15:0] in TRIGx_CFG_3 and TRIGx_CFG_4 registers. Each Unit is 1 ns.

Continuous clock by setting TRIGx_CFG_5, bits[15:0] = “0”.

• Associate this Trigger Output Unit to a Specific GPIO Pin

TRIGx_CFG_1[3:0] = Selects GPIO pin to use.

• Set Up Interrupts if Needed

If it is desired to get notification that the trigger output event occurred set up the following registers.

TRIGx_CFG_1, bit[8] (Trigger Notify) = “1” is one requirement for enabling interrupt on done or error.

Set the corresponding trigger Unit interrupt enable bit in the PTP_TRIG_IE register.

• Enabling the Trigger Output Unit

Set the corresponding trigger Unit enable bit in the TRIG_EN register.

Because the frequencies to be generated are based on the period of the 125 MHz clock, there are some limitations that the user must be aware of. Certain frequencies can be created with unvarying duty cycles. However, other frequencies may incur some variation in duty cycle. There are methods of utilizing the trigger Unit 2 clock edge output select bit (bit[7] in of Reg. 0x248 – 0x249) and GPIO1 to control and minimize the variances.

3.6.4 CREATING FINITE LENGTH PERIODIC BIT STREAMS AT A SPECIFIC TIME

This example implies that a uniform clock will be generated for a specific number of clock cycles:

- Specifying the Time

The desired trigger time will be set in TRIGx_TGT_NSH, TRIGx_TGT_NSL, TRIGx_TGT_SH, and TRIGx_TGT_SL registers.

- Specifying the Finite Length Periodic Bit Stream Parameters

TRIGx_CFG_1[6:4] = “101” for generating a positive periodic signal.

High part of cycle defined by bits[15:0] in the TRIGx_CFG_2 register. Each Unit is 8 ns.

Cycle width defined by bits[15:0] in TRIGx_CFG_3 and TRIGx_CFG_4 registers. Each Unit is 1 ns.

Finite length count established by setting TRIGx_CFG_5, bits[15:0] = “number of cycles”. Each Unit is one cycle.

- Associate this Trigger Output Unit to a Specific GPIO Pin

TRIGx_CFG_1[3:0] = Selects GPIO pin to use.

- Set Up Interrupts if Needed

If it is desired to get notification that the trigger output event occurred, set up the following registers.

TRIGx_CFG_1, bit[8] (Trigger Notify) = “1” is one requirement for enabling interrupt on done or error.

Set the corresponding trigger Unit interrupt enable bit in the PTP_TRIG_IE register.

- Enabling the Trigger Output Unit

Set the corresponding Trigger Unit Enable bit in the TRIG_EN register.

3.6.5 CREATING FINITE LENGTH NON-UNIFORM BIT STREAMS AT A SPECIFIC TIME

Generation of a finite length non-uniform waveform which is a multiple of the bit pattern stored in the data storage register.

- Specifying the Time

The desired trigger time will be set in TRIGx_TGT_NSH, TRIGx_TGT_NSL, TRIGx_TGT_SH, and TRIGx_TGT_SL registers.

- Specifying the Finite Length Non-Uniform Bit Stream Parameters

TRIGx_CFG_1[6:4] = “110” for generating signal based on contents of data register.

16-bit pattern stored in TRIGx_CFG_6 register.

Bit width defined by bits[15:0] in TRIGx_CFG_3 and TRIGx_CFG_4 registers. Each Unit is 1 ns.

Bit length of finite pattern is established by shifting the data register “N” times. Set TRIGx_CFG_5, bits[15:0] = “N”.

- Associate this Trigger Output Unit to a Specific GPIO Pin

TRIGx_CFG_1[3:0] = Selects GPIO pin to use.

- Set up Interrupts if Needed

If it is desired to get notification that the trigger output event occurred, set up the following registers.

TRIGx_CFG_1, bit[8] (Trigger Notify) = “1” is one requirement for enabling interrupt on done or error.

Set the corresponding trigger unit interrupt enable bit in the PTP_TRIG_IE register.

- Enabling the Trigger Output Unit

Set the corresponding trigger unit enable bit in the TRIG_EN register.

3.6.6 CREATING COMPLEX WAVEFORMS AT A SPECIFIC TIME

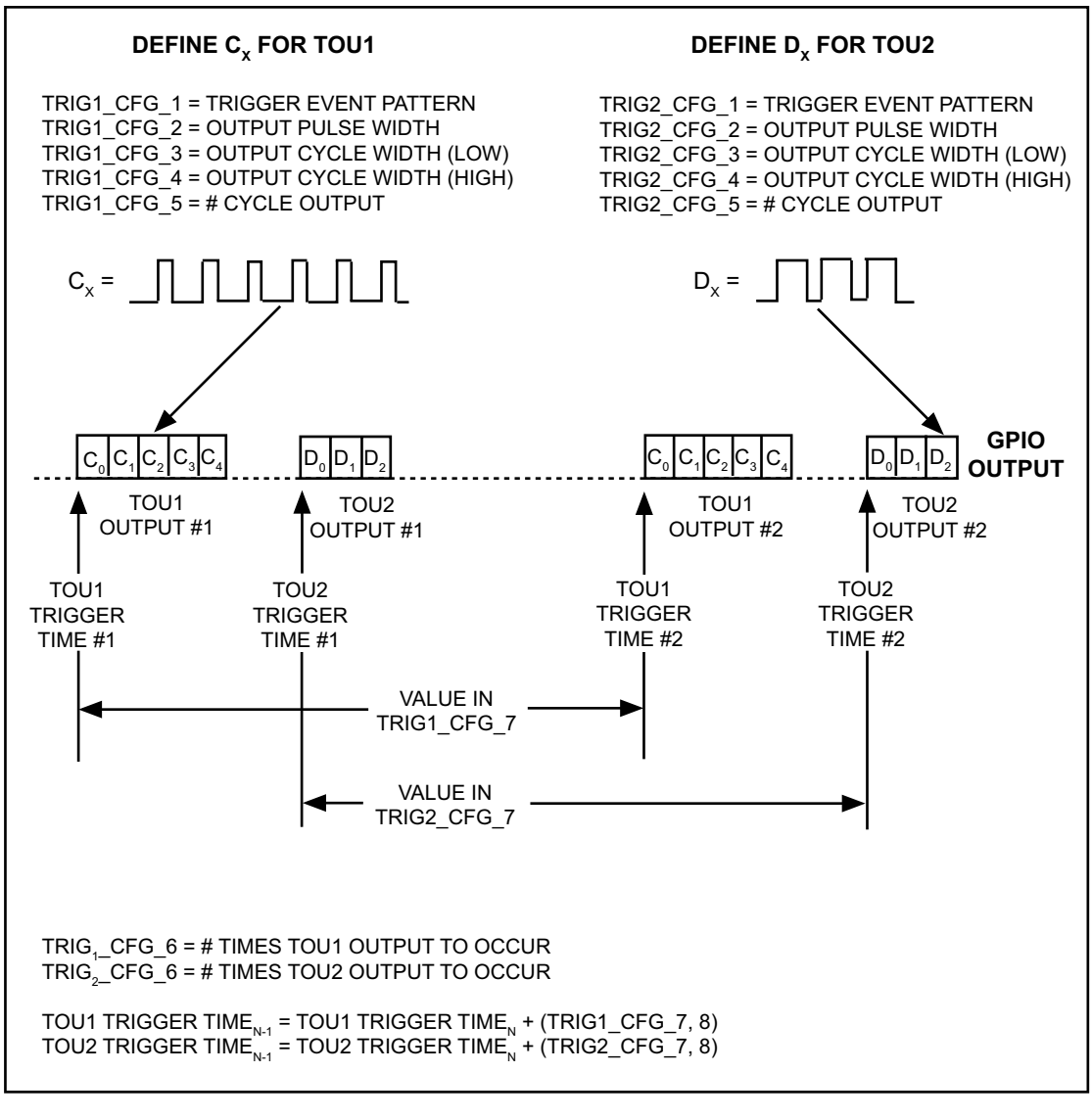
Complex waveforms can be created by combining the various functions available in the trigger output units using a method called “cascading.”

Figure 3-14 illustrates the generation of a complex waveform onto one GPIO pin. Trigger output Unit 1 (TOU1) and trigger output Unit 2 (TOU2) are cascaded to produce the complex waveform. Cascading allows multiple outputs to be sequentially output onto one GPIO pin. In Figure 3-14, the waveform created by TOU1 is output first on the selected GPIO pin when the indicated TOU1 trigger time is reached. The value in TRIG1_CFG7 and TRIG1_CFG8 will be added to the TOU1 trigger time and the next TOU1 output will occur at that time. Meanwhile, TOU2, will operate in the same manner; outputting its waveform at TOU2 trigger time and then outputting again at a time TRIG2_CFG7 and TRIG2_CFG8 later. The TRIGx_CFG7 and 8 register values must be the same for all TOUs that are cascaded together. The number of times TOU1 and TOU2 will be output will depend on the cycle times programmed into the TRIG1_CFG6 and TRIG2_CFG6 registers. Care must be taken to select the correct values so as to avoid erroneous overlap.

Additional steps are required in setting up cascaded TOUs:

- Specifying which trigger output Unit in the cascade is the last Unit called the tail unit.
- The last trigger output Unit in a cascade setup should have its tail bit set to “1”.

FIGURE 3-14: COMPLEX WAVEFORM GENERATION USING CASCADE MODE



3.7 Using the GPIO Pins with the Time Stamp Input Units

The twelve time stamp input units (TSU) can be set up to capture a variety of inputs at user selectable GPIO pins. The current time of the precision time clock time will be captured and stored at the time in which the input event occurs. This section provides some information on configuring the time stamp input units. In the information below, the value “x” represents one of the twelve time stamp input units. Because this area of the device is very flexible and powerful, it is advised that you contact your Microchip representative for additional information on capturing specific types of waveforms and utilizing this feature.

- Time Stamp Value

Each time stamp input nit can capture two sampled values of time stamps. These first two values remain until read, even if more events occur. The time stamp value captured consists of three parts which are latched in three registers.

Sample #1, the seconds value; TSx_SMPL1_SH, TSx_SMPL1_SL

Sample #1, the nanoseconds value; TSx_SMPL1_NSH, TSx_SMPL1_NSL

Sample #1, the sub-nanoseconds value; TSx_SMPL1_SUB_NS

Sample #2, the seconds value; TSx_SMPL2_SH, TSx_SMPL2_SL

Sample #2, the nanoseconds value; TSx_SMPL2_NSH, TSx_SMPL2_NSL

Sample #2, the sub-nanoseconds value; TSx_SMPL2_SUB_NS

The actual value in TSx_SMPL1/2_SUB_NS is a binary value of 0 through 4 which indicates 0 ns, 8 ns, 16 ns, 24 ns, or 32 ns. Note that the processor needs to add this value to the seconds and nanoseconds value to get the closest true value of the time stamp event.

- Number of Time Stamps Available

Each time stamp input unit can capture two events or two time stamps values. Note that the exception to this is TSU12. TSU12 can capture eight events and thus has eight sample time registers (SMPL1 thru SMPL8) allowing for more robust timing acquisition in one TSU. Note that the amount of samples for any given GPIO pin can be increased by cascading time stamp unit. When TSUs are cascaded, the incoming events are routed to a sequentially established order of TSUs for capture. For example, you can cascade TSU12, and TSU 1-4 to be able to capture twelve time stamps off of one GPIO pin. Cascading is set up in the TSx_CFG registers.

- Events that can be Captured

The time stamp input units can capture rising edges and falling edges. In this case, the time stamp of the event will be captured in the Sample #1 time stamp registers. A pulse can be captured if rising edge detection is combined with falling edge detection. In this case, one edge will be captured in the Sample #1 time stamp registers and the other edge will be captured in the Sample #2 time stamp registers. This functionality is programmed in the TSx_CFG register for each time stamp unit.

time stamping an incoming low-going edge:

- Specifying the Edge Parameters

TSx_CFG bit[6] = “1”

- Associate this Time Stamp Unit to a Specific GPIO Pin

TSx_CFG bits[11:8] = Selected GPIO Pin #

- Set Up Interrupts if Needed

Set the corresponding time stamp unit interrupt enable bit in the PTP_TS_IE register.

- Enabling the Time Stamp Unit

Set the corresponding time stamp unit enable bit in the TS_EN register.

Time stamping an incoming high-going edge:

- Specifying the Edge Parameters

TSx_CFG bit[7] = “1”

- Associate this Time Stamp Unit to a Specific GPIO Pin

TSx_CFG bits[11:8] = Selected GPIO Pin #

- Set Up Interrupts if Needed

Set the corresponding time stamp unit interrupt enable bit in the PTP_TS_IE register.

- Enabling the Time Stamp Unit

Set the corresponding time stamp unit enable bit in the TS_EN register.

Time stamping an incoming low-going pulse or high-going pulse

- Specifying the Edge Parameters

TSx_CFG bit[7] = “1”

TSx_CFG bit[6] = “1”

- Associate this Time Stamp Unit to a Specific GPIO Pin

TSx_CFG bits[11:8] = Selected GPIO Pin #

- Set Up Interrupts if Needed

Set the corresponding time stamp unit interrupt enable bit in the PTP_TS_IE register.

- Enabling the Time Stamp Unit

Set the corresponding time stamp unit enable bit in the TS_EN register.

3.8 Device Clocks

A 25 MHz clock source on X1/X2 is required for MII operation. The RMII 50 MHz clock can either be derived from the 25 MHz X1/X2 reference, or is received from an external source. If an external 50 MHz clock is used for RMII, then a local 25 MHz crystal or clock oscillator is not required. There are a number of pins with clock related functions on this device. Table 3-9 summarizes those pins and the area of usage and if they are related to 25 MHz, 50 MHz, RMII, or MII clocking.

TABLE 3-9: DEVICE CLOCKS AND RELATED PINS

Clock Signal Name	Pin Number	Usage	Strapping Option Information
X1, X2	18, 19	The X1 and X2 pins are used to input a clock which is used to clock all of the circuits within the device. MII – Clocking Choices: • 25 MHz crystal connected between X1, X2 • 25 MHz oscillator connected to pin X1 only. X2 shall be unconnected. RMII – Clocking Choices: • Either connection specified above for X1 and X2 with other control bits and pins configured as specified in Table 3-17 to produce the required 50 MHz output on REFCLK_O. REFCLK_O externally connected to REFCLK_I. • 50MHz supplied on REFCLK_I pin from external source. X1 and X2 unconnected. Other control bits and pins configured as specified in Table 3-17. Refer also to X1, X2 pin descriptions.	The SPI_DO pin (pin 41) is used to select if a 25 MHz clock on the X1 and X2 pins or a 50 MHz clock on the REFCLK_I pin will be used as the source of all RMII clocking. Other control bits and control pins are used to determine other attributes of the RMII/MII clocking scheme. Refer to Table 3-17 for more information on the control bits and pins. Refer to Table 2-2.

TABLE 3-9: DEVICE CLOCKS AND RELATED PINS (CONTINUED)

Clock Signal Name	Pin Number	Usage	Strapping Option Information
TX_CLK/ REFCLK_I	27	These four pins are used for the clocking and configuration of the MII and RMII interfaces. MII: • 25MHz clocks are output on TX_CLK and RX_CLK. RMII: • A 50 MHz clock must be received on REFCLK_I. This comes either from an external source or via external connection from REFCLK_O. Refer to Table 3-17 for details on the usage of these signal pins.	The SPI_DO pin (pin 41) is used to select if a 25 MHz clock on the X1 and X2 pins or a 50 MHz clock on the REFCLK_I pin will be used as the source of all RMII clocking. Other control bits and control pins are used to determine other attributes of the RMII/MII clocking scheme. Refer to Table 3-17 for more information on the control bits and pins. Refer to Table 2-2.
TXD3/ EN_REFCLK_O	23		
RXD3/ REFCLK_O	32		
RX_CLK/ GPIO7_RLI	38		
SPI_SCLK/MDC	44	This pin is the clock for the SPI interface.	—
RXD2	33	This pin determines the clocking range of the SPI clock. Refer to the Strapping Options section.	—

Note that the clock tree power-down control register (0x038 – 0x039): CTPDC is used to power down the clocks in various areas of the device. There are no other internal register bits which control the clock generation or usage in the device.

3.8.1 GPIO AND IEEE 1588-RELATED CLOCKING

The GPIO and IEEE 1588-related circuits both utilize the 25 MHz clock and the derived 125 MHz clock. The tolerance and accuracy of the 25 MHz clock source will affect the IEEE 1588 jitter and offset in a system utilizing multiple slave devices. Therefore, the 25 MHz source should be chosen with care towards the performance of the application in mind. Using an oscillator will generally provide better results.

3.9 Power

The KSZ8463 device requires a single 3.3V supply to operate. An internal low-voltage LDO provides the necessary low voltage (nominal ~1.3V) to power the analog and digital logic cores. The various I/Os can be operated at 1.8V, 2.5V, and 3.3V. Table 3-10 illustrates the various voltage options and requirements of the device.

TABLE 3-10: VOLTAGE OPTIONS AND REQUIREMENTS

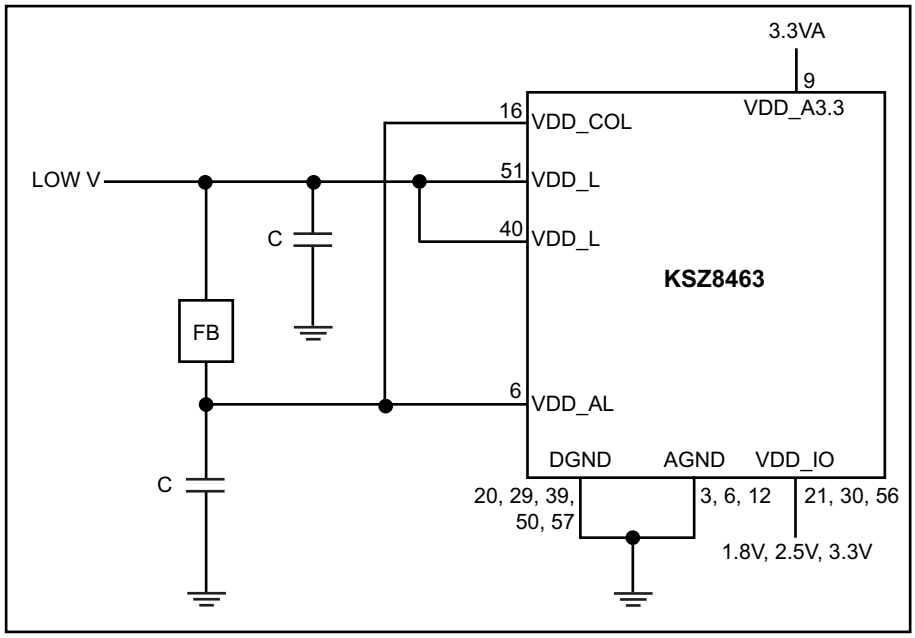
Power Signal Name	Device Pin	Requirement
VDD_A3.3	9	3.3V input power to the analog blocks in the device.
VDD_IO	21, 30, 56	Choice of 1.8V or 2.5V or 3.3V for the I/O circuits. These input power pins power the I/O circuitry of the device. This voltage is also used as the input to the internal low-voltage regulator.
VDD_AL	6	Filtered low-voltage analog input voltage. This is where the filtered low voltage is fed back into the device to power the analog block.
VDD_COL	16	Filtered low-voltage AD input voltage. This pin feeds the low voltage to the digital circuits within the analog block.

TABLE 3-10: VOLTAGE OPTIONS AND REQUIREMENTS (CONTINUED)

Power Signal Name	Device Pin	Requirement
VDD_L	40, 51	Output of internal low-voltage LDO regulator. This voltage is available on these pins to allow connection to external capacitors and ferrite beads for filtering and power integrity. These pins must be externally connected to pins 6 and 16. If the internal LDO regulator is turned off, these pins become power inputs.
AGND	3, 8, 12	Analog Ground.
DGND	20, 29, 39, 50, 57	Digital Ground.

The preferred method of configuring the related low-voltage power pins when using an external low-voltage regulator is illustrated in Figure 3-15. The number of capacitors, values of capacitors, and exact placement of components will depend upon the specific design.

FIGURE 3-15: RECOMMENDED LOW-VOLTAGE POWER CONNECTION USING AN EXTERNAL LOW-VOLTAGE REGULATOR



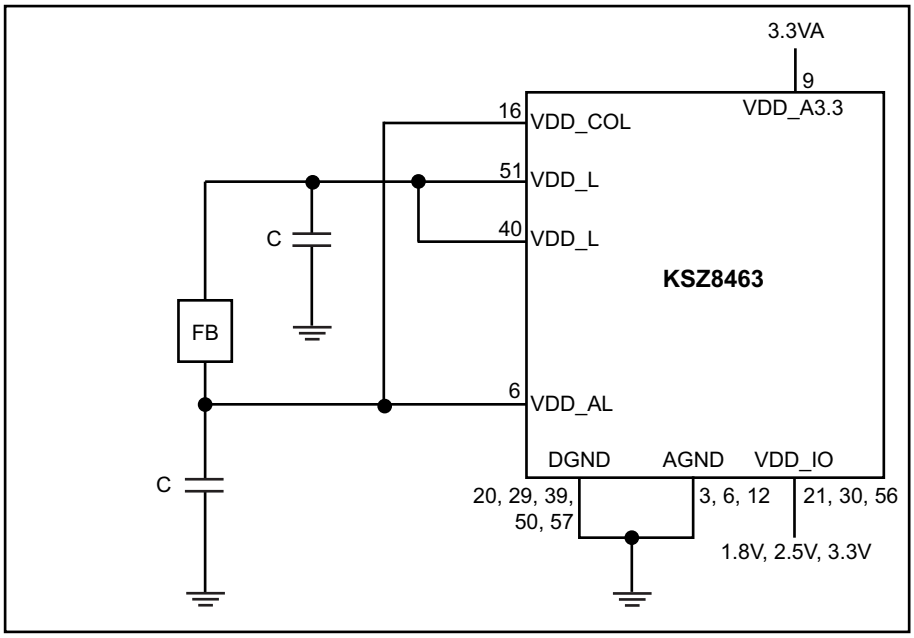
3.9.1 INTERNAL LOW VOLTAGE LDO REGULATOR

The KSZ8463 reduces board cost and simplifies board layout by integrating a low noise internal low-voltage LDO regulator to supply the nominal ~1.3V core power voltage for a single 3.3V power supply solution. If it is desired to take advantage of an external low-voltage supply that is available, the internal low-voltage regulator can be disabled to save power. The LDO_Off bit, bit[7] in Register 0x748 is used to enable or disable the internal low-voltage regulator. The default state of the LDO_Off bit is “0” which enables the internal low-voltage regulator. Turning off the internal low-voltage regulator will require software to write a “1” to that control bit. During the time from power up to setting this bit, both the external voltage supply and the internal regulator will be supplying power. Note that it is not necessary to turn off the internal low-voltage regulator. No damage will occur if it is left on. However, leaving it on will result in less than optimized power consumption.

The internal regulator takes its power from VDD_IO, and functions best when VDD_IO is 3.3V or 2.5V. If VDD_IO is 1.8V, the output voltage will be somewhat decreased. For optimal performance, an external power supply, in place of the internal regulator, is recommended when VDD_IO is 1.8V.

The preferred method of configuring the low-voltage related power pins for using the internal low-voltage regulator is illustrated in Figure 3-16. The output of the internal regulator is available on pins 40 and 51 and is filtered using external capacitors and a ferrite bead to supply power to pins 6 and 16. The number of capacitors, values of capacitors, and exact placement of components will depend upon the specific design.

FIGURE 3-16: RECOMMENDED LOW-VOLTAGE POWER CONNECTION USING THE INTERNAL LOW-VOLTAGE REGULATOR



3.10 Power Management

The KSZ8463 supports enhanced power management features in low-power state with energy detection to ensure low-power dissipation during device idle periods. There are three operation modes under the power management function which is controlled by two bits in the power management control and wake-up event status register (PMCTRL, 0x032 – 0x033) as shown below:

- PMCTRL[1:0] = “00” Normal Operation Mode
- PMCTRL[1:0] = “01” Energy Detect Mode
- PMCTRL[1:0] = “10” Global Soft Power-Down Mode

The Table 3-11 indicates all internal function blocks status under three different power-management operation modes.

TABLE 3-11: POWER MANAGEMENT AND INTERNAL BLOCKS

KSZ8463 Function Blocks	Power Management Operation Modes		
	Normal Mode	Energy Detect Mode	Soft Power-Down Mode
Internal PLL Clock	Enabled	Disabled	Disabled
Tx/Rx PHYs	Enabled	Energy Detect at Rx	Disabled
MACs	Enabled	Disabled	Disabled
Host Interface	Enabled	Disabled	Disabled

3.10.1 NORMAL OPERATION MODE

Normal operation mode is the power management mode entered into after device power-up or after hardware reset pin 63. It is established via bits[1:0] = “00” in the PMCTRL register. When the KSZ8463 is in normal operation mode, all PLL clocks are running, PHYs and MACs are on, and the CPU is ready to read or write the KSZ8463 through these serial interfaces (SPI and MIIM).

During the normal operation mode, the host CPU can change the power management mode bits[1:0] in the PMCTRL register to transition to another desired power management mode

3.10.2 ENERGY-DETECT MODE

Energy-detect mode provides a mechanism to save more power than in normal operation mode when the KSZ8463 is not connected to an active link partner. For example, if the cable is not present or it is connected to a powered down partner, the KSZ8463 can automatically enter the low power state in energy detect mode. Once activity resumes after attaching a cable or by a link partner attempting to establish a link, the KSZ8463 will automatically power-up into the normal power state in energy detect normal power state. The energy-detect mode function is not valid in fiber mode using the KSZ8463FML and KSZ8463FRL devices.

Energy-detect mode consists of two states, normal-power state and low-power state. While in low-power state, the KSZ8463 reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. Energy detect mode is enabled by setting bits[1:0] = “01” in the PMCTRL register. When the KSZ8463 is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than a pre-configured value determined by bits[7:0] (Go-Sleep Time) in the GST register, the device will go into the low-power state. When the KSZ8463 is in low-power state, it will keep monitoring the cable energy. Once energy is detected from the cable and is present for a time longer than 100 ns, the KSZ8463 will enter the normal-power state.

3.10.3 GLOBAL SOFT POWER-DOWN MODE

Soft power-down mode is entered by setting bits[1:0] = “10” in PMCTRL register. When the device is in this mode, all PLL clocks are disabled, the PHYs and the MACs are off, all internal registers value will change to default value, and the CPU serial interface is only used to wake-up this device from the current soft power-down mode to normal operation mode by setting bits[1:0] = “00” in the PMCTRL register.

All strapping pins are sampled to latch any new values when soft power-down is disabled.

3.10.4 ENERGY EFFICIENT ETHERNET (EEE)

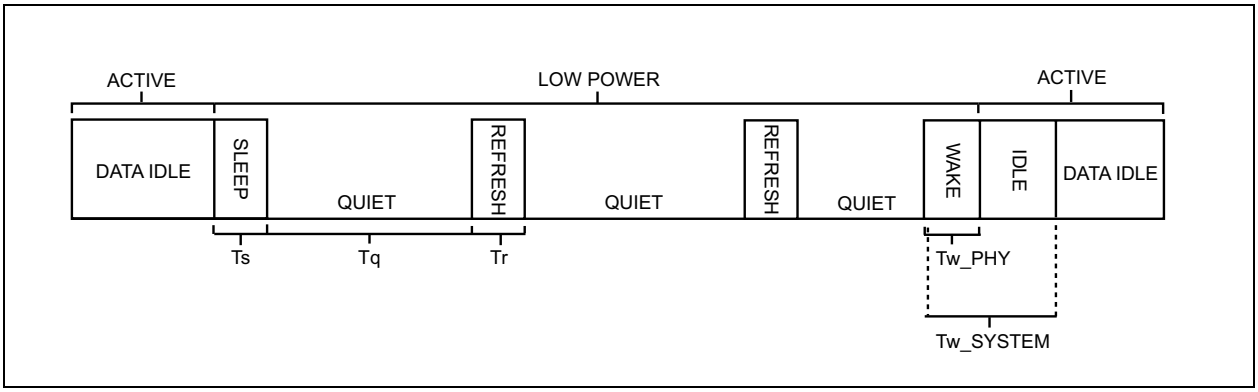
Energy Efficient Ethernet (EEE) is implemented in the KSZ8463ML device as described in the IEEE 802.3AZ specification for MII operations on Port 1 and Port 2. The EEE function is not available for fiber mode Ports using the KSZ8463FML and KSZ8463FRL devices. EEE is not performed at Port 3 since that is a MAC to MAC interface and not a MAC to PHY interface. The internal connection between the MAC and PHY blocks are performed in MII mode. The details of the implementation are provided in the information that follows. The standards are defined around a MAC that supports special signaling associated with EEE. EEE saves power by keeping the voltage on the Ethernet cable at approximately 0V for as often as possible during periods of no traffic activity. This is called low-power idle (LPI) state. However, the link will respond automatically when traffic resumes and do so in such a way as to not cause blocking or dropping of any packets (the wake-up time for 100BASE-TX is specified to be less than 30 µs.). The transmit and receive directions are independently controlled. Note the EEE is not specified or implemented for 10BASE-T. In 10BASE-T, the transmitter is already OFF during idle periods.

The EEE feature is enabled by default. EEE is auto-negotiated independently for each direction on a link, and is enabled only if both nodes on a link support it. To disable EEE, clear the Next Page Enable bit(s) for the desired port(s) in the PCSEEEC register (0x0F3) and restart auto-negotiation.

Based on the EEE specification, the energy savings from EEE occurs at the PHY level. However, the KSZ8463 device reduces the power consumption not only in the PHY block but also in the MAC and switch blocks by shutting down any unused clocks as much as possible when the device is at LPI state. A comprehensive LPI request on/off policy is also built-in at the switch level to determine when to issue LPI requests and when to stop the LPI request. Some software control options are provided in the device to terminate the LPI request in the early phase when certain events occur to reduce the latency impact during LPI recovery. A configurable LPI recovery time register is provided at each port to specify the recovery time (25 µs at default) required for the KSZ8463 and its link partner before they are ready to transmit and receive a packet after going back to the normal state. For details, please refer to the KSZ8463 EEE registers (0x0E0 – 0x0F7) description.

The time during which LPI mode is active is during what is called quiet time. This is shown in Figure 3-17.

FIGURE 3-17: TRAFFIC ACTIVITY AND EEE



3.10.5 TRANSMIT DIRECTION CONTROL FOR MII MODE

For ports 1 and 2, low-power idle (LPI) state for the transmit direction will be entered when the internal EEE MAC signals to its PHY to do so. The PHY will stay in the transmit LPI state as long as indicated by the MAC. The TX_CLK is not stopped.

Even though the PHY is in LPI state, it will periodically leave the LPI state to transmit a refresh signal using specific transmit code bits. This allows the link partner to keep track of the long-term variation of channel characteristics and clock drift between the two partners. Approximately every 20 ms – 22 ms, the PHY will transmit a bit pattern to its link partner of duration 200 µs – 220 µs. The refresh times are listed in Figure 3-17.

3.10.6 RECEIVE DIRECTION CONTROL FOR MII MODE

If enabled for LPI mode, upon receiving a P Code bit pattern (refresh), the PHY will enter the LPI state and signal to the internal MAC. If the PHY receives some non-P Code bit pattern, it will signal to the MAC to return to “normal frame” mode. The PHY can turn off the RX_CLK after nine or more clocks have occurred in the LPI state.

In the EEE-compliant environment, the internal PHYs will be monitoring and expecting the P Code (refresh) bit pattern from its link partner that is generated approximately every 20 ms – 22 ms, with a duration of about 200 µs – 220 µs. This allows the link partner to keep track of the long term variation of channel characteristics and clock drift between the two partners.

3.10.7 REGISTERS ASSOCIATED WITH EEE

The following registers are used to configure or manage the EEE feature:

- Reg. DCh, DDh – P1ANPT – Port 1 Auto-Negotiation Next Page Transmit Register
- Reg. DEh, DFh – P1ALPRNP – Port 1 Auto-Negotiation Link Partner Received Next Page Register
- Reg. E0h, E1h – P1EEEA – Port 1 EEE and Link Partner Advertisement Register
- Reg. E2h, E3h – P1EEEWEC – Port 1 EEE Wake Error Count Register
- Reg. E4h, E5h – P1EEECS – Port 1 EEE Control/Status and Auto-Negotiation Expansion Register
- Reg. E6h – P1LPIRTC – Port 1 LPI Recovery Time Counter Register
- Reg. E7h – BL2LPIC1 – Buffer Load to LPI Control 1 Register
- Reg. E8h, E9h – P2ANPT – Port 2 Auto-Negotiation Next Page Transmit Register
- Reg. EAh, EBh – P2ALPRNP – Port 2 Auto-Negotiation Link Partner Received Next Page Register
- Reg. ECh, EDh – P2EEEA – Port 2 EEE and Link Partner Advertisement Register
- Reg. EEh, EFh – P2EEEWEC – Port 2 EEE Wake Error Count Register
- Reg. F0h, F1h – P2EEECS – Port 2 EEE Control/Status and Auto-Negotiation Expansion Register
- Reg. F2h – P2LPIRTC – Port 2 LPI Recovery Time Counter Register
- Reg. F3h – PCSEEEC – PCS EEE Control Register
- Reg. F4h, F5h – ETLWTC – Empty TXQ to LPI Wait Time Control Register
- Reg. F6h, F7h – BL2LPIC2 – Buffer Load to LPI Control 2 Register

3.11 Interrupt Generation on Power Management-Related Events

The various status bits associated with link change and energy detect situations are found in the PMCTRL Register (0x032 – 0x033) bits[3:2]. The enabling of these signals to generate an interrupt are in IER (0x190 – 0x191) bits[3:2]. The actual interrupt status for these bits are located in ISR (0x192 – 0x193) bits[3:2].

3.12 Interfaces

The KSZ8463 device incorporates a number of interfaces to enable it to be designed into a standard network environment as well as a vendor unique environment. The available interfaces are summarized in Table 3-12. The details of each usage in the table are provided in the sections which follow.

TABLE 3-12: AVAILABLE INTERFACES

Interface	Type	Usage	Registers Accessed
SPI	Configuration and Register Access	[As Slave Serial Bus] – External CPU or controller can R/W all internal registers through this interface.	All
MIIM	Configuration and Register Access	MDC/MDIO-capable CPU or controllers can R/W PHY registers.	PHY Only
MII	Data Flow	Interface to the port 3 MAC using the standard MII timing.	N/A
RMII	Data Flow	Interface to the port 3 MAC using the faster reduced RMII timing.	N/A
PHY	Data Flow	Interface to the two internal PHY devices.	N/A

3.12.1 CONFIGURATION INTERFACE

The KSZ8463 supports a serial configuration interface, which may be either SPI or MIIM. The strapping option on pin 35 (RXD0) and pin 34 (RXD1) is used to select one of these two interfaces. This setting may be read in the serial bus selection bits in the configuration status and serial bus mode register (0x0D8 – 0x0D9): CFGR.

3.12.2 SPI SLAVE SERIAL BUS CONFIGURATION

The KSZ8463 supports a SPI interface in slave mode (see Strapping Options). In this managed mode, an external SPI master device (micro-controller or CPU) supplies the serial clock (SPI_SCLK), chip select (SPI_CSN), and serial input data (SPI_DI). Serial output data (SPI_DO) is driven out by the KSZ8463. SPI operations start with the falling edge of SPI_CSN and end with the rising edge of SPI_CSN. SPI_SCLK is expected to stay low when SPI operation is idle. A SPI master device (external controller/CPU) has complete programming access to all KSZ8463 registers. Table 3-13 shows the SPI interface connection for the KSZ8463.

TABLE 3-13: SPI CONNECTION

Pin Number	SPI Slave Signal Name	External Processor (SPI Master) Signal Description
42	SPI_CSN (input)	SPI Chip Select (Master output)
44	SPI_SCLK (input)	SPI Clock (Master output)
45	SPI_DI (input)	SPI Data Out (Master output)
41	SPI_DO (output)	SPI Data In (Master input)

Input data on SPI_DI (MOSI) is sampled by the KSZ8463 on the rising edge of SPI_SCLK. Timing of the output data on SPI_DO (MISO) is user-selectable by a strapping option on pin 33. The options are high-speed SPI and low-speed SPI:

- High-Speed SPI Mode: SPI_DO is clocked out at the rising edge of SPI_SCLK mode. The master will typically sample MISO data at the falling edge of SPI_SCLK, but depending on the MISO hold time requirements of the master, rising edge sampling may be possible.
- Low-Speed SPI Mode: SPI_DO is clocked out at the falling edge of SPI_SCLK, ½ cycle later than high-speed SPI mode. The master will typically sample MISO data at the rising edge of SPI_SCLK.

The KSZ8463 supports two standard SPI commands:

- Internal I/O registers read (Opcode = “0”)

- Internal I/O registers write (Opcode = “1”)

As shown in Table 3-14 and Figure 3-18, there are two phases in each SPI operation. The first is the command phase, followed by the data phase. The command phase is two bytes long for register access. The data phase is in the range of one to four bytes long depending on the specified byte enable bits B[3:0] in command phase.

TABLE 3-14: REGISTER ACCESS USING THE SPI INTERFACE

SPI Operation	Command Phase (SI Pin)				Data Phase (SO or SI Pins)
	Byte 0 [7:0]		Byte 1 [7:0]		
	Op	Register Address	Byte Enable	TA Bits	
Register Read	0	A10 A9 A8 A7 A6 A5 A4	A3 A2 B3 B2 B1 B0	X X	1 to 4 Bytes (Read Data on SO pin)
Register Write	1	A10 A9 A8 A7 A6 A5 A4	A3 A2 B3 B2 B1 B0	X X	1 to 4 Bytes (Write Data on SI pin)

Note 3-1 In Command phase, Address A[10:2] access register location in double-word and Byte enable B[3:0] to indicate which byte to access during read or write. In Data phase, the byte 0 is first in/out and byte 3 is last in/out during read or write.

Note 3-2 B[3:0] -> 1: enable byte; 0: disable byte. CPU can enable any one of the four bytes, lower or higher two bytes, or all four bytes during the command phase.

Note 3-3 TA bits are “turn around” bits and “don’t care” bits.

3.12.3 SPI REGISTER ACCESS OPERATION TIMING

As shown in Figure 3-10 and Figure 3-11, illustrating the SPI internal I/O registers read and write operation timing, the first two command byte 0/1 contain opcode (0: read command, 1: write command), A[10:2] address bits to access register location in double words and B[3:0] Byte enable bits to indicate which data byte is available in data phase (1: byte enable, 0: byte disable). The following is data phase either 1, 2, or 4 bytes depending on B[3:0] setting.

Figure 3-19 and Figure 3-20 show the details of the SPI bus protocol for read and write operations. Initially the master sends a two-byte command. This command begins with a 1-bit opcode (0: read command, 1: write command). It is followed by address bits A[10] to A[2], then four byte enable bits B[3:0], then finally two zero bits. The byte enable bits are set to indicate which bytes will be transferred in the data phase of the SPI operation. For a two-byte operation, which is the most common, B[3:0] = 0011. For a single byte operation, B[3:0] = 0001, and for a four-byte operation, B[3:0] = 1111.

The sequence for data transfer is least significant byte first. Then within each byte, the most significant bit goes first.

FIGURE 3-18: SPI REGISTER READ OPERATION – LOW-SPEED MODE

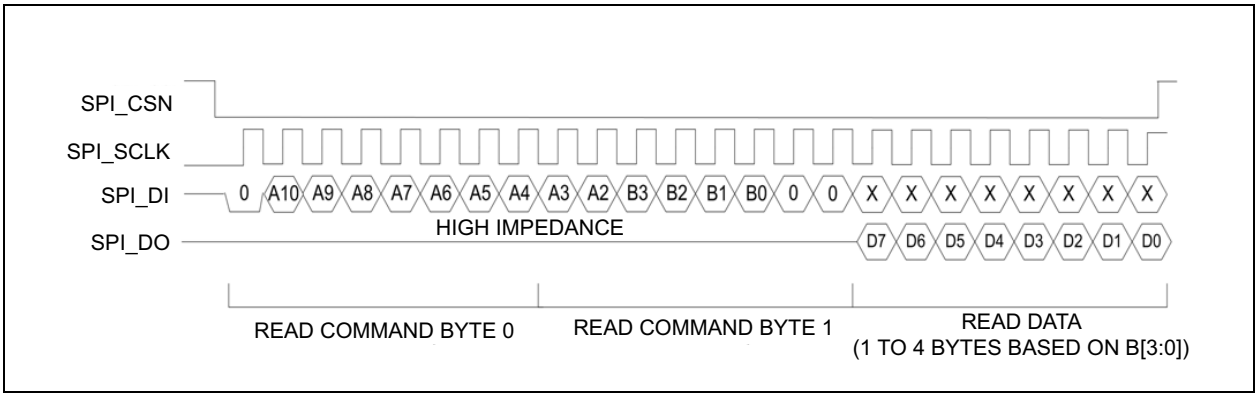


FIGURE 3-19: SPI REGISTER READ OPERATION – HIGH-SPEED MODE

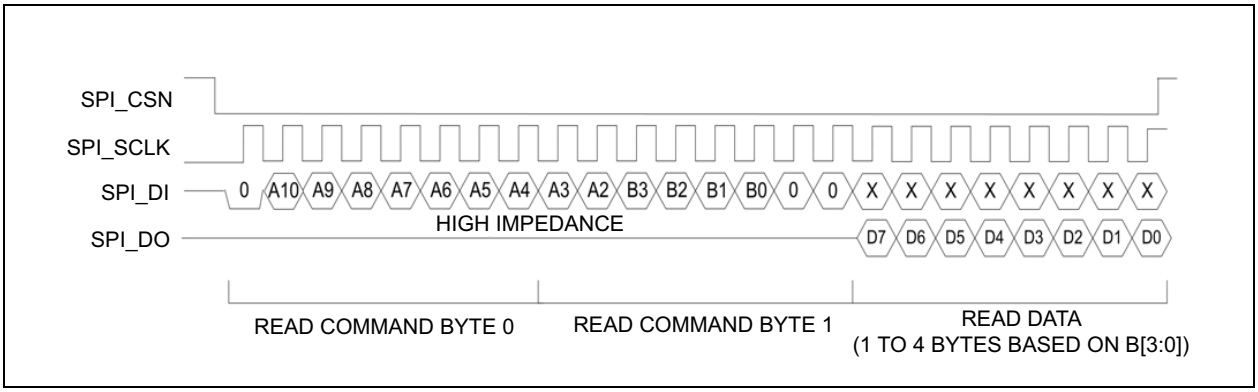
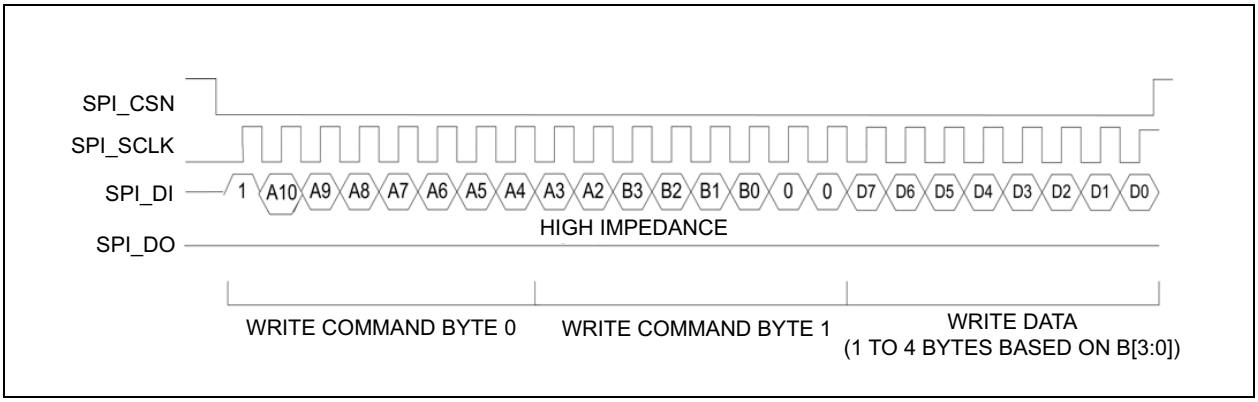


FIGURE 3-20: SPI REGISTER WRITE OPERATION TIMING



3.12.4 MII MANAGEMENT (MIIM) INTERFACE

The KSZ8463 supports the IEEE 802.3 MII management interface, also known as the management data input/output (MDIO) interface. This interface allows upper-layer devices to monitor and control the states of the KSZ8463 PHY block. An external device with MDC/MDIO capability can read the PHY status or configure the PHY settings. Details on the MIIM interface can be found in Clause 22.2.4.5 of the IEEE 802.3u Specification. Timing information can be found in 802.3 section 22.3.4.

The MIIM interface consists of the following:

- A physical connection that uses a data signal (MDIO) and a clock signal (MDC) for communication between an external controller and the KSZ8463 device.
- A specific protocol that operates across the two signal physical connection that allows an external controller to communicate with the internal PHY devices.
- Access to a set of eight 16-bit registers, consisting of six standard MIIM registers (0x0 – 0x5) and two custom MIIM registers (0x1D and 0x1F). Each set of registers is duplicated for each internal PHY device.

The MIIM Interface can operate up to a maximum clock speed of 5 MHz and access is limited to only the registers in the PHY block. Table 3-15 summarizes the MII management interface frame format.

TABLE 3-15: MII MANAGEMENT INTERFACE FRAME FORMAT

Operation Mode	Preamble (32-Bit)	Start of Frame (2-Bit)	Op Code (2-Bit)	PHY Address (5-Bit)	Register Address (5-Bit)	TA (2-Bit)	Register Data (16-Bit)	Idle
Read	All 1s	01	10	A[4:0]	Reg[4:0]	Z0	D[15:0]	Z
Write	All 1s	01	01	A[4:0]	Reg[4:0]	10	D[15:0]	Z

3.12.5 MEDIA INDEPENDENT INTERFACE (MII)

The media independent interface (MII) is specified in Clause 22 of the IEEE 802.3u Standard. It provides a common interface between PHY layer and MAC layer devices. The MII provided by the KSZ8463ML and KSZ8463FML is connected to the device's third MAC on port 3. This interface is operated in PHY Mode or in MAC Mode. This is determined by the strapping option on the RX_DV pin (pin 31) at the time of de-assertion of RSTN. The interface contains two distinct groups of signals, one for transmission and the other for reception. Table 3-16 describes the signals used by the MII interface to connect to an external MAC or an external PHY.

TABLE 3-16: MII INTERFACE SIGNAL AND PIN ASSOCIATIONS

PHY Mode Signals Connection		MII Interface Signals Description	MAC Mode Signals Connection	
KSZ8463ML/FML In PHY Mode Signals	External MAC Controller Signals		External PHY Device Signals	KSZ8463ML/FML In MAC Mode Signals
TX_EN (pin 22, input)	TX_EN	Transmit Enable	TX_EN	RX_DV (pin 31, output)
MII_BP (pin 28, input)	TX_ER	Transmit Error	TX_ER	NA (not used)
TXD3 (pin 23, input)	TXD3	Transmit Data Bit 3	TXD3	RXD3 (pin 32, output)
TXD2 (pin 24, input)	TXD2	Transmit Data Bit 2	TXD2	RXD2 (pin 33, output)
TXD1 (pin 25, input)	TXD1	Transmit Data Bit 1	TXD1	RXD1 (pin 34, output)
TXD0 (pin 26, input)	TXD0	Transmit Data Bit 0	TXD0	RXD0 (pin 35, output)
TX_CLK (pin 27, output)	TX_CLK	Transmit Clock	TX_CLK	RX_CLK (pin 38, output)
COL (pin 37, output)	COL	Collision Detection	COL	COL (pin 37, output)
CRS (pin 36, output)	CRS	Carrier Sense	CRS	CRS (pin 36, output)
RX_DV (pin 31, output)	RX_DV	Receive Data Valid	RX_DV	TX_EN (pin 22, input)
NA (not used)	RX_ER	Receive Error	RX_ER	MII_BP (pin 28, input)
RXD3 (pin 32, output)	RXD3	Receive Data Bit 3	RXD3	TXD3 (pin 23, input)
RXD2 (pin 33, output)	RXD2	Receive Data Bit 2	RXD2	TXD2 (pin 24, input)
RXD1 (pin 34, output)	RXD1	Receive Data Bit 1	RXD1	TXD1 (pin 25, input)
RXD0 (pin 35, output)	RXD0	Receive Data Bit 0	RXD0	TXD0 (pin 26, input)
RX_CLK (pin 38, output)	RX_CLK	Receive Clock	RX_CLK	TX_CLK (pin 27, output)

The MII interface operates in either PHY mode or MAC mode. The data interface is 4-bits wide and runs at one quarter the network bit rate; either 2.5 MHz in 10BASE-T or 25 MHz in 100BASE-TX (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Similarly, the receive side has signals that convey when the data is valid and without physical layer errors. For half duplex operation, the COL signal indicates if a collision has occurred during transmission.

The KSZ8463ML/FML does not provide the RX_ER signal in PHY mode operation or the TX_ER signal in MAC mode operation. Normally, RX_ER indicates a receive error coming from the physical layer device and TX_ER indicates a transmit error from the MAC device. Since the switch filters error frames, these MII error signals are not used by the KSZ8463ML/FML. So, for PHY mode operation, if the device interfacing with the KSZ8463ML/FML has an RX_ER input pin, it needs to be tied low. And, for MAC mode operation, if the device interfacing with the KSZ8463ML/FML has a TX_ER input pin, it also needs to be tied low.

The KSZ8463ML/FML provides a bypass feature in the MII PHY mode. The TX_ER/MII_BP pin (pin 28) is used to enable the MII bypass mode when this pin is tied to high. The MII (port 3) is shut down if TX_ER/MII_BP is set to high in the MII PHY mode. In this case, no new ingress frames from either port 1 or port 2 will be sent out through port 3 and only switching between port 1 and port 2 for all ingress packets will occur, and the frames for port 3 already in packet memory will be flushed out.

3.12.6 REDUCED MEDIA INDEPENDENT INTERFACE (RMII)

The reduced media independent interface (RMII) specifies a low pin count MII. It is available only on port 3 of the KSZ8463RL and KSZ8463FRL devices for communication with the MAC attached to that port. As with MII, RMII provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports network data rates of either 10 Mbps or 100 Mbps.
- Uses a single 50 MHz clock reference (provided internally or externally) for both transmit and receive data.
- Uses independent 2-bit wide transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

The user should select one the two RMII clocking methods shown in Table 3-17. While EN_REFCLK_O (pin 23) is high, the KSZ8463RL/FRL will output a 50 MHz clock on REFCLK_O (pin 32), which is derived from the 25 MHz crystal or oscillator attached to the X1 and X2 inputs. In this mode, REFCLK_O must be externally connected to REFCLK_I (pin 27). While EN_REFCLK_O (pin 23) is low, the KSZ8463RL/FRL will require an external 50 MHz signal to be input to the REFCLK_I input from an external source. In this mode, the X1 and X2 pins are not used.

TABLE 3-17: RMII CLOCK SETTINGS

EN_REFCLK_O (Pin 23)	25/50 MHz Select (Pin 41) at Power-Up/Reset Time	Output on REFCLK_0 (Pin 32)	Clock Source	Note
0 (Disable)	0 (50 MHz)	No	External 50 MHz input to REFCLK_I	X1/X2 are not used. Leave them unconnected.
1 (Enable)	1 (25 MHz)	50 MHz	REFCLK_O output must be externally connected to REFCLK_I	50 MHz output on REFCLK_O pin X1/X2 is connected to a 25 MHz crystal or oscillator
Do not use the remainder of logical inputs		—	N/A	N/A

The RMII interface in KSZ8463RL/FRL is connected to the device's third MAC. It complies with the RMII specification. Table 3-18 describes the signals used by the RMII interface. Refer to the RMII specification for full details on the signal descriptions.

TABLE 3-18: RMII SIGNAL DESCRIPTIONS

RMII Signal Name	Direction (with respect to the PHY)	Direction (with respect to the MAC)	RMII Signal Description	KSZ8463RL/FRL RMII Signal (Direction)
REFCLK	Input	Input or Output	Synchronous 50 MHz clock reference for receive, transmit, and control interface	REFCLK_I (input)
CRS_DV	Output	Input	Carrier Sense/ Receive Data Valid	RX_DV (output)
RXD[1:0]	Output	Input	Receive Data Bit[1:0]	RXD[1:0] (output)
TX_EN	Input	Output	Transmit Enable	TX_EN (input)
TXD[1:0]	Input	Output	Transmit Data Bit[1:0]	TXD[1:0] (input)
RX_ER	Output	Input or not required	Receive Error	(not used)
—	—	—	—	TX_ER (input) Connects to RX_ER signal of RMII PHY device

The KSZ8463RL/FRL filters error frames, and thus does not implement the RX_ER output signal. To detect error frames from RMII PHY devices, the TX_ER input signal of the KSZ8463RL/FRL is connected to the RX_ER output signal of the RMII PHY device. Collision detection is implemented in accordance with the RMII Specification.

In RMII mode, tie the MII signals (TXD[3:2], RXD[3:2] and TX_ER) to ground via a resistor if they are not used.

The KSZ8463RL/FRL can interface to either an RMII PHY or an RMII MAC device. The RMII MAC device allows two KSZ8463RL/FRL devices to be connected back-to-back. Table 3-19 shows the KSZ8463RL/FRL RMII pin connections with an external RMII PHY and an external RMII MAC, such as another KSZ8463RL/FRL device.

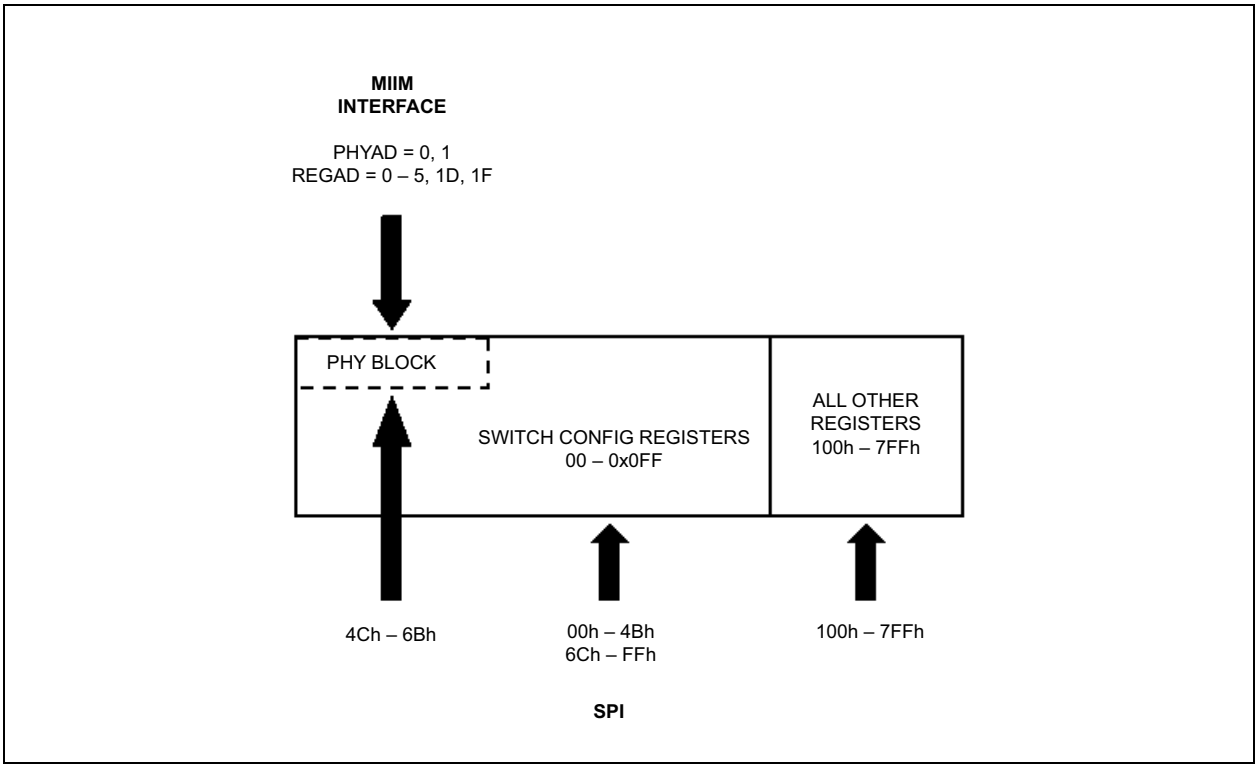
TABLE 3-19: RMII PHY-TO-MAC AND MAC-TO-MAC SIGNAL CONNECTIONS

KSZ8463RL/FRL PHY-MAC Connections		Signal Descriptions	KSZ8463RL/FRL MAC-MAC Connections	
External PHY Signals	KSZ8463RL/FRL MAC Signals		KSZ8463RL/FRL MAC Signals	External MAC Signals
REFCLK	REFCLK_I	Reference Clock	REFCLK_I	REF_CLK
TX_EN	RX_DV	Carrier Sense/ Receive Data Valid	RX_DV	CRS_DV
TXD1	RXD1	Receive Data Bit[1]	RXD1	RXD1
TXD0	RXD0	Receive Data Bit[0]	RXD0	RXD0
CRS_DV	TX_EN	Transmit Enable	TX_EN	TX_EN
RXD1	TXD1	Transmit Data Bit[1]	TXD1	TXD1
RXD0	TXD0	Transmit Data Bit[0]	TXD0	TXD0
RX_ER	TX_ER	Receive Error	(not used)	(not used)

4.0 REGISTER DESCRIPTIONS

The KSZ8463 device has a rich set of registers available to manage the functionality of the device. Access to these registers is via the MIIM or SPI interfaces. All of the registers are not accessible via each interface. Figure 4-1 provides a global picture of accessibility via the various interfaces and addressing ranges from the perspective of each interface.

FIGURE 4-1: INTERFACE AND REGISTER MAPPING



The registers within the linear 0x000 – 0x7FF address space are all accessible via the SPI interface by a microprocessor or CPU attached to that buss. The mapping of the various functions within that linear address space is summarized in Table 4-1.

TABLE 4-1: MAPPING OF FUNCTIONAL AREAS WITHIN THE ADDRESS SPACE

Register Locations	Device Area	Description
0x000 – 0x0FF	Switch Control and Configuration	Registers which control the overall functionality of the Switch, MAC, and PHYs
0x026 – 0x031	Indirect Access Registers	Registers used to indirectly address and access four distinct areas within the device. • Management Information Base (MIB) Counters • Static MAC Address Table • Dynamic MAC Address Table • VLAN Table
0x044 – 0x06B	PHY1 and PHY2 Registers	The same PHY registers as specified in IEEE 802.3 specification
0x100 – 0x1FF	Interrupts and Global Reset	The registers and bits associated with interrupts and global reset
0x200 – 0x3FF	IEEE 1588 PTP Trigger Control and Output Registers	Registers used to configure and use the IEEE 1588 trigger functions

TABLE 4-1: MAPPING OF FUNCTIONAL AREAS WITHIN THE ADDRESS SPACE (CONTINUED)

Register Locations	Device Area	Description
0x400 – 0x5FF	IEEE 1588 PTP Time Stamp Input Units	Registers used for controlling and monitoring the 1588 timestamp units
0x600 – 0x7FF	IEEE 1588 PTP Clock and Global Control	Registers that control and monitor the PTP clock, port ingress/egress, and messaging

4.1 Register Map of CPU Accessible I/O Registers

In managed switch mode, the registers within the KSZ8463 can be accessed using the SPI slave serial bus interface. An external microprocessor communicates with the device through these registers. These registers are used for configuring the device, controlling processes, and reading various statuses.

4.1.1 I/O REGISTERS

The following I/O register space mapping tables apply to 8-bit or 16-bit locations. Depending upon the serial bus mode selected, each I/O access can be performed using the following operations:

- Using 8-bit accesses for all serial bus modes, there are 2048-byte address locations.
- In byte, word, or double word access for SPI serial bus mode only.

TABLE 4-2: INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 – 0X0FF)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x000 – 0x001	0x000 0x001	CIDER	0x8443 (ML, FML) 0x8453 (RL, FRL)	Chip ID and Enable Register [15:0]
0x002 – 0x003	0x002 0x003	SGCR1	0x3450	Switch Global Control Register 1 [15:0]
0x004 – 0x005	0x004 0x005	SGCR2	0x00F0	Switch Global Control Register 2 [15:0]
0x006 – 0x007	0x006 0x007	SGCR3	0x6320	Switch Global Control Register 3 [15:0]
0x008 – 0x00B	0x008 0x00B	Reserved (4-Bytes)	Don’t Care	None
0x00C – 0x00D	0x00C 0x00D	SGCR6	0xFA50	Switch Global Control Register 6 [15:0]
0x00E – 0x00F	0x00E 0x00F	SGCR7	0x0827	Switch Global Control Register 7 [15:0]
0x010 – 0x011	0x010 0x011	MACAR1	0x0010	MAC Address Register 1 [15:0]
0x012 – 0x013	0x012 0x013	MACAR2	0xA1FF	MAC Address Register 2 [15:0]
0x014 – 0x015	0x014 0x015	MACAR3	0xFFFF	MAC Address Register 3 [15:0]
0x016 – 0x017	0x016 0x017	TOSR1	0x0000	TOS Priority Control Register 1 [15:0]
0x018 – 0x019	0x018 0x019	TOSR2	0x0000	TOS Priority Control Register 2 [15:0]
0x01A – 0x01B	0x01A 0x01B	TOSR3	0x0000	TOS Priority Control Register 3 [15:0]
0x01C – 0x01D	0x01C 0x01D	TOSR4	0x0000	TOS Priority Control Register 4 [15:0]

TABLE 4-2: INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 – 0X0FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x01E – 0x01F	0x01E 0x01F	TOSR5	0x0000	TOS Priority Control Register 5 [15:0]
0x020 – 0x021	0x020 0x021	TOSR6	0x0000	TOS Priority Control Register 6 [15:0]
0x022 – 0x023	0x022 0x023	TOSR7	0x0000	TOS Priority Control Register 7 [15:0]
0x024 – 0x025	0x024 0x025	TOSR8	0x0000	TOS Priority Control Register 8 [15:0]
0x026 – 0x027	0x026 0x027	IADR1	0x0000	Indirect Access Data Register 1 [15:0]
0x028 – 0x029	0x028 0x029	IADR2	0x0000	Indirect Access Data Register 2 [15:0]
0x02A – 0x02B	0x02A 0x02B	IADR3	0x0000	Indirect Access Data Register 3 [15:0]
0x02C – 0x02D	0x02C 0x02D	IADR4	0x0000	Indirect Access Data Register 4 [15:0]
0x02E – 0x02F	0x02E 0x02F	IADR5	0x0000	Indirect Access Data Register 5 [15:0]
0x030 – 0x031	0x030 0x031	IACR	0x0000	Indirect Access Control Register [15:0]
0x032 – 0x033	0x032 0x033	PMCTRL	0x0000	Power Management Control and Wake-up Event Status Register [15:0]
0x034 – 0x035	0x034 0x035	Reserved (2-Bytes)	0x0000	None
0x036 – 0x037	0x036 0x037	GST	0x008E	Go Sleep Time Register [15:0]
0x038 – 0x039	0x038 0x039	CTPDC	0x0000	Clock Tree Power Down Control Register [15:0]
0x03A – 0x04B	0x03A 0x04B	Reserved (18-Bytes)	Don’t Care	None
0x04C – 0x04D	0x04C 0x04D	P1MBCR	0x3120	PHY 1 and MII Basic Control Register [15:0]
0x04E – 0x04F	0x04E 0x04F	P1MBSR	0x7808	PHY 1 and MII Basic Status Register [15:0]
0x050 – 0x051	0x050 0x051	PHY1ILR	0x1430	PHY 1 PHYID Low Register [15:0]
0x052 – 0x053	0x052 0x053	PHY1IHR	0x0022	PHY 1 PHYID High Register [15:0]
0x054 – 0x055	0x054 0x055	P1ANAR	0x05E1	PHY 1 Auto-Negotiation Advertisement Register [15:0]
0x056 – 0x057	0x056 0x057	P1ANLPR	0x0001	PHY 1 Auto-Negotiation Link Partner Ability Register [15:0]
0x058 – 0x059	0x058 0x059	P2MBCR	0x3120	PHY 2 and MII Basic Control Register [15:0]
0x05A – 0x05B	0x05A 0x05B	P2MBSR	0x7808	PHY 2 and MII Basic Status Register [15:0]

TABLE 4-2: INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 – 0X0FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x05C – 0x05D	0x05C 0x05D	PHY2ILR	0x1430	PHY 2 PHYID Low Register [15:0]
0x05E – 0x05F	0x05E 0x05F	PHY2IHR	0x0022	PHY 2 PHYID High Register [15:0]
0x060 – 0x061	0x060 0x061	P2ANAR	0x05E1	PHY 2 Auto-Negotiation Advertisement Register [15:0]
0x062 – 0x063	0x062 0x063	P2ANLPR	0x0001	PHY 2 Auto-Negotiation Link Partner Ability Register [15:0]
0x064 – 0x065	0x064 0x065	Reserved (2-Bytes)	Don’t Care	None
0x066 – 0x067	0x066 0x067	P1PHYCTRL	0x0004	PHY 1 Special Control and Status Register [15:0]
0x068 – 0x069	0x068 0x069	Reserved (2-Bytes)	Don’t Care	None
0x06A – 0x06B	0x06A 0x06B	P2PHYCTRL	0x0004	PHY2 Special Control and Status Register [15:0]
0x06C – 0x06D	0x06C 0x06D	P1CR1	0x0000	Port 1 Control Register 1 [15:0]
0x06E – 0x06F	0x06E 0x06F	P1CR2	0x0607	Port 1 Control Register 2 [15:0]
0x070 – 0x071	0x070 0x071	P1VIDCR	0x0001	Port 1 VID Control Register [15:0]
0x072 – 0x073	0x072 0x073	P1CR3	0x0000	Port 1 Control Register 3 [15:0]
0x074 – 0x075	0x074 0x075	P1IRCR0	0x0000	Port 1 Ingress Rate Control Register 0 [15:0]
0x076 – 0x077	0x076 0x077	P1IRCR1	0x0000	Port 1 Ingress Rate Control Register 1 [15:0]
0x078 – 0x079	0x078 0x079	P1ERCR0	0x0000	Port 1 Egress Rate Control Register 0 [15:0]
0x07A – 0x07B	0x07A 0x07B	P1ERCR1	0x0000	Port 1 Egress Rate Control Register 1 [15:0]
0x07C – 0x07D	0x07C 0x07D	P1SCSLMD	0x0400	Port 1 PHY Special Control/Status, LinkMD Register [15:0]
0x07E – 0x07F	0x07E 0x07F	P1CR4	0x00FF	Port 1 Control Register 4 [15:0]
0x080 – 0x081	0x080 0x081	P1SR	0x8000	Port 1 Status Register [15:0]
0x082 – 0x083	0x082 0x083	Reserved (2-Bytes)	Don’t Care	None
0x084 – 0x085	0x084 0x085	P2CR1	0x0000	Port 2 Control Register 1 [15:0]
0x086 – 0x087	0x086 0x087	P2CR2	0x0607	Port 2 Control Register 2 [15:0]
0x088 – 0x089	0x088 0x089	P2VIDCR	0x0001	Port 2 VID Control Register [15:0]

TABLE 4-2: INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 – 0X0FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x08A – 0x08B	0x08A 0x08B	P2CR3	0x0000	Port 2 Control Register 3 [15:0]
0x08C – 0x08D	0x08C 0x08D	P2IRCR0	0x0000	Port 2 Ingress Rate Control Register 0 [15:0]
0x08E – 0x08F	0x08E 0x08F	P2IRCR1	0x0000	Port 2 Ingress Rate Control Register 1 [15:0]
0x090 – 0x091	0x090 0x091	P2ERCR0	0x0000	Port 2 Egress Rate Control Register 0 [15:0]
0x092 – 0x093	0x092 0x093	P2ERCR1	0x0000	Port 2 Egress Rate Control Register 1 [15:0]
0x094 – 0x095	0x094 0x095	P2SCSLMD	0x0400	Port 2 PHY Special Control/Status, LinkMD Register [15:0]
0x096 – 0x097	0x096 0x097	P2CR4	0x00FF	Port 2 Control Register 4 [15:0]
0x098 – 0x099	0x098 0x099	P2SR	0x8000	Port 2 Status Register [15:0]
0x09A – 0x09B	0x09A 0x09B	Reserved (2-Bytes)	Don’t Care	None
0x09C – 0x09D	0x09C 0x09D	P3CR1	0x0000	Port 3 Control Register 1 [15:0]
0x09E – 0x09F	0x09E 0x09F	P3CR2	0x0607	Port 3 Control Register 2 [15:0]
0x0A0 – 0x0A1	0x0A0 0x0A1	P3VIDCR	0x0001	Port 3 VID Control Register [15:0]
0x0A2 – 0x0A3	0x0A2 0x0A3	P3CR3	0x0000	Port 3 Control Register 3 [15:0]
0x0A4 – 0x0A5	0x0A4 0x0A5	P3IRCR0	0x0000	Port 3 Ingress Rate Control Register 0 [15:0]
0x0A6 – 0x0A7	0x0A6 0x0A7	P3IRCR1	0x0000	Port 3 Ingress Rate Control Register 1 [15:0]
0x0A8 – 0x0A9	0x0A8 0x0A9	P3ERCR0	0x0000	Port 3 Egress Rate Control Register 0 [15:0]
0x0AA – 0x0AB	0x0AA 0x0AB	P3ERCR1	0x0000	Port 3 Egress Rate Control Register 1 [15:0]
0x0AC – 0x0AD	0x0AC 0x0AD	SGCR8	0x8000	Switch Global Control Register 8 [15:0]
0x0AE – 0x0AF	0x0AE 0x0AF	SGCR9	0x0000	Switch Global Control Register 9 [15:0]
0x0B0 – 0x0B1	0x0B0 0x0B1	SAFMACA1L	0x0000	Source Address Filtering MAC Address 1 Register Low [15:0]
0x0B2 – 0x0B3	0x0B2 0x0B3	SAFMACA1M	0x0000	Source Address Filtering MAC Address 1 Register Middle [15:0]
0x0B4 – 0x0B5	0x0B4 0x0B5	SAFMACA1H	0x0000	Source Address Filtering MAC Address 1 Register High [15:0]
0x0B6 – 0x0B7	0x0B6 0x0B7	SAFMACA2L	0x0000	Source Address Filtering MAC Address 2 Register Low [15:0]

TABLE 4-2: INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 – 0X0FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x0B8 – 0x0B9	0x0B8 0x0B9	SAFMACA2M	0x0000	Source Address Filtering MAC Address 2 Register Middle [15:0]
0x0BA – 0x0BB	0x0BA 0x0BB	SAFMACA2H	0x0000	Source Address Filtering MAC Address 2 Register High [15:0]
0x0BC – 0x0C7	0x0BC 0x0C7	Reserved (12-Bytes)	Don't Care	None
0x0C8 – 0x0C9	0x0C8 0x0C9	P1TXQRCR1	0x8488	Port 1 TXQ Rate Control Register 1 [15:0]
0x0CA – 0x0CB	0x0CA 0x0CB	P1TXQRCR2	0x8182	Port 1 TXQ Rate Control Register 2 [15:0]
0x0CC – 0x0CD	0x0CC 0x0CD	P2TXQRCR1	0x8488	Port 2 TXQ Rate Control Register 1 [15:0]
0x0CE – 0x0CF	0x0CE 0x0CF	P2TXQRCR2	0x8182	Port 2 TXQ Rate Control Register 2 [15:0]
0x0D0 – 0x0D1	0x0D0 0x0D1	P3TXQRCR1	0x8488	Port 3 TXQ Rate Control Register 1 [15:0]
0x0D2 – 0x0D3	0x0D2 0x0D3	P3TXQRCR2	0x8182	Port 3 TXQ Rate Control Register 2 [15:0]
0x0D4 – 0x0D5	0x0D4 0x0D5	Reserved (2-Bytes)	Don't Care	None
0x0D6 – 0x0D7	0x0D6 0x0D7	IOMXSEL	0x0FFF	Input and Output Multiplex Selection Register [15:0]
0x0D8 – 0x0D9	0x0D8 0x0D9	CFGR	0x00FE	Configuration Status and Serial Bus Mode Register [15:0]
0x0DA – 0x0DB	0x0DA 0x0DB	Reserved (2-Bytes)	Don't Care	None
0x0DC – 0x0DD	0x0DC 0x0DD	P1ANPT	0x2001	Port 1 Auto-Negotiation Next Page Transmit Register [15:0]
0x0DE – 0x0DF	0x0DE 0x0DF	P1ALPRNP	0x0000	Port 1 Auto-Negotiation Link Partner Received Next Page Register [15:0]
0x0E0 – 0x0E1	0x0E0 0x0E1	P1EEEA	0x0002	Port 1 EEE and Link Partner Advertisement Register [15:0]
0x0E2 – 0x0E3	0x0E2 0x0E3	P1EEEWEC	0x0000	Port 1 EEE Wake Error Count Register [15:0]
0x0E4 – 0x0E5	0x0E4 0x0E5	P1EEECS	0x8064	Port 1 EEE Control/Status and Auto-Negotiation Expansion Register [15:0]
0x0E6 – 0x0E7	0x0E6 0x0E7	P1LPIRTC BL2LPIC1	0x27 0x08	Port 1 LPI Recovery Time Counter Register [7:0] Buffer Load to LPI Control 1 Register [7:0]
0x0E8 – 0x0E9	0x0E8 0x0E9	P2ANPT	0x2001	Port 2 Auto-Negotiation Next Page Transmit Register [15:0]
0x0EA – 0x0EB	0x0EA 0x0EB	P2ALPRNP	0x0000	Port 2 Auto-Negotiation Link Partner Received Next Page Register [15:0]
0x0EC – 0x0ED	0x0EC 0x0ED	P2EEEA	0x0002	Port 2 EEE and Link Partner Advertisement Register [15:0]
0x0EE – 0x0EF	0x0EE 0x0EF	P2EEEWEC	0x0000	Port 2 EEE Wake Error Count Register [15:0]

TABLE 4-2: INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 – 0X0FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x0F0 – 0x0F1	0x0F0 0x0F1	P2EEECS	0x8064	Port 2 EEE Control/Status and Auto-Negotiation Expansion Register [15:0]
0x0F2 – 0x0F3	0x0F2 0x0F3	P2LPIRTC PCSEEEC	0x27 0x03	Port 2 LPI Recovery Time Counter Register [7:0] PCS EEE Control Register [7:0]
0x0F4 – 0x0F5	0x0F4 0x0F5	ETLWTC	0x03E8	Empty TXQ to LPI Wait Time Control Register [15:0]
0x0F6 – 0x0F7	0x0F6 0x0F7	BL2LPIC2	0xC040	Buffer Load to LPI Control 2 Register [15:0]
0x0F8 - 0x0FF	0x0F8 0x0FF	Reserved (8-Bytes)	Don’t Care	None

TABLE 4-3: INTERNAL I/O REGISTER SPACE MAPPING FOR INTERRUPTS AND GLOBAL RESET (0X100 – 0X1FF)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x100 – 0x123	0x100 0x123	Reserved (36-Bytes)	Don’t Care	None
0x124 – 0x125	0x124 0x125	MBIR	0x0000	Memory BIST Info Register [15:0]
0x126 – 0x127	0x126 0x127	GRR	0x0000	Global Reset Register [15:0]
0x128 – 0x18F	0x128 0x18F	Reserved (104-Bytes)	Don’t Care	None
0x190 – 0x191	0x190 0x191	IER	0x0000	Interrupt Enable Register [15:0]
0x192 – 0x193	0x192 0x193	ISR	0x0000	Interrupt Status Register [15:0]
0x194 – 0x1FF	0x194 0x1FF	Reserved (108-Bytes)	Don’t Care	None

TABLE 4-4: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TRIGGER OUTPUT (12 UNITS, 0X200 – 0X3FF)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x200 – 0x201	0x200 0x201	TRIG_ERR	0x0000	Trigger Output Unit Error Register [11:0]
0x202 – 0x203	0x202 0x203	TRIG_ACTIVE	0x0000	Trigger Output Unit Active Register [11:0]
0x204 – 0x205	0x204 0x205	TRIG_DONE	0x0000	Trigger Output Unit Done Register [11:0]
0x206 – 0x207	0x206 0x207	TRIG_EN	0x0000	Trigger Output Unit Enable Register [11:0]
0x208 – 0x209	0x208 0x209	TRIG_SW_RST	0x0000	Trigger Output Unit Software Reset Register [11:0]

TABLE 4-4: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TRIGGER OUTPUT (12 UNITS, 0X200 – 0X3FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x20A – 0x20B	0x20A 0x20B	TRIG12_PPS_WIDTH	0x0000	Trigger Output Unit 12 PPS Pulse Width Register
0x20C – 0x21F	0x20C 0x21F	Reserved (20-Bytes)	Don't Care	None
0x220 – 0x221	0x220 0x221	TRIG1_TGT_NSL	0x0000	Trigger Output Unit 1 Target Time in Nanoseconds Low-Word Register [15:0]
0x222 – 0x223	0x222 0x223	TRIG1_TGT_NSH	0x0000	Trigger Output Unit 1 Target Time in Nanoseconds High-Word Register [29:16]
0x224 – 0x225	0x224 0x225	TRIG1_TGT_SL	0x0000	Trigger Output Unit 1 Target Time in Seconds Low-Word Register [15:0]
0x226 – 0x227	0x226 0x227	TRIG1_TGT_SH	0x0000	Trigger Output Unit 1 Target Time in Seconds High-Word Register [31:16]
0x228 – 0x229	0x228 0x229	TRIG1_CFG_1	0x3C00	Trigger Output Unit 1 Configuration/Control Register1
0x22A – 0x22B	0x22A 0x22B	TRIG1_CFG_2	0x0000	Trigger Output Unit 1 Configuration/Control Register2
0x22C – 0x22D	0x22C 0x22D	TRIG1_CFG_3	0x0000	Trigger Output Unit 1 Configuration/Control Register3
0x22E – 0x22F	0x22E 0x22F	TRIG1_CFG_4	0x0000	Trigger Output Unit 1 Configuration/Control Register4
0x230 – 0x231	0x230 0x231	TRIG1_CFG_5	0x0000	Trigger Output Unit 1 Configuration/Control Register5
0x232 – 0x233	0x232 0x233	TRIG1_CFG_6	0x0000	Trigger Output Unit 1 Configuration/Control Register6
0x234 – 0x235	0x234 0x235	TRIG1_CFG_7	0x0000	Trigger Output Unit 1 Configuration/Control Register7
0x236 – 0x237	0x236 0x237	TRIG1_CFG_8	0x0000	Trigger Output Unit 1 Configuration/Control Register8
0x238 – 0x23F	0x238 0x23F	Reserved (8-Bytes)	Don't Care	None
0x240 – 0x241	0x240 0x241	TRIG2_TGT_NSL	0x0000	Trigger Output Unit 2 Target Time in Nanoseconds Low-Word Register [15:0]
0x242 – 0x243	0x242 0x243	TRIG2_TGT_NSH	0x0000	Trigger Output Unit 2 Target Time in Nanoseconds High-Word Register [29:16]
0x244 – 0x245	0x244 0x245	TRIG2_TGT_SL	0x0000	Trigger Output Unit 2 Target Time in Seconds Low-Word Register [15:0]
0x246 – 0x247	0x246 0x247	TRIG2_TGT_SH	0x0000	Trigger Output Unit 2 Target Time in Seconds High-Word Register [31:16]
0x248 – 0x249	0x248 0x249	TRIG2_CFG_1	0x3C00	Trigger Output Unit 2 Configuration/Control Register1
0x24A – 0x24B	0x24A 0x24B	TRIG2_CFG_2	0x0000	Trigger Output Unit 2 Configuration/Control Register2
0x24C – 0x24D	0x24C 0x24D	TRIG2_CFG_3	0x0000	Trigger Output Unit 2 Configuration/Control Register3
0x24E – 0x24F	0x24E 0x24F	TRIG2_CFG_4	0x0000	Trigger Output Unit 2 Configuration/Control Register4

TABLE 4-4: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TRIGGER OUTPUT (12 UNITS, 0X200 – 0X3FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x250 – 0x251	0x250 0x251	TRIG2_CFG_5	0x0000	Trigger Output Unit 2 Configuration/Control Register5
0x252 – 0x253	0x252 0x253	TRIG2_CFG_6	0x0000	Trigger Output Unit 2 Configuration/Control Register6
0x254 – 0x255	0x254 0x255	TRIG2_CFG_7	0x0000	Trigger Output Unit 2 Configuration/Control Register7
0x256 – 0x257	0x256 0x257	TRIG2_CFG_8	0x0000	Trigger Output Unit 2 Configuration/Control Register8
0x258 – 0x25F	0x258 0x25F	Reserved (8-Bytes)	Don't Care	None
0x260 – 0x261	0x260 0x261	TRIG3_T-GT_NSL	0x0000	Trigger Output Unit 3 Target Time in Nanoseconds Low-Word Register [15:0]
0x262 – 0x263	0x262 0x263	TRIG3_T-GT_NSH	0x0000	Trigger Output Unit 3 Target Time in Nanoseconds High-Word Register [29:16]
0x264 – 0x265	0x264 0x265	TRIG3_TGT_SL	0x0000	Trigger Output Unit 3 Target Time in Seconds Low-Word Register [15:0]
0x266 – 0x267	0x266 0x267	TRIG3_T-GT_SH	0x0000	Trigger Output Unit 3 Target Time in Seconds High-Word Register [31:16]
0x268 – 0x269	0x268 0x269	TRIG3_CFG_1	0x3C00	Trigger Output Unit 3 Configuration/Control Register1
0x26A – 0x26B	0x26A 0x26B	TRIG3_CFG_2	0x0000	Trigger Output Unit 3 Configuration/Control Register2
0x26C – 0x26D	0x26C 0x26D	TRIG3_CFG_3	0x0000	Trigger Output Unit 3 Configuration/Control Register3
0x26E – 0x26F	0x26E 0x26F	TRIG3_CFG_4	0x0000	Trigger Output Unit 3 Configuration/Control Register4
0x270 – 0x271	0x270 0x271	TRIG3_CFG_5	0x0000	Trigger Output Unit 3 Configuration/Control Register5
0x272 – 0x273	0x272 0x273	TRIG3_CFG_6	0x0000	Trigger Output Unit 3 Configuration/Control Register6
0x274 – 0x275	0x274 0x275	TRIG3_CFG_7	0x0000	Trigger Output Unit 3 Configuration/Control Register7
0x276 – 0x277	0x276 0x277	TRIG3_CFG_8	0x0000	Trigger Output Unit 3 Configuration/Control Register8
0x278 – 0x27F	0x278 0x27F	Reserved (8-Bytes)	Don't Care	None
0x280 – 0x281	0x280 0x281	TRIG4_T-GT_NSL	0x0000	Trigger Output Unit 4 Target Time in Nanoseconds Low-Word Register [15:0]
0x282 – 0x283	0x282 0x283	TRIG4_T-GT_NSH	0x0000	Trigger Output Unit 4 Target Time in Nanoseconds High-Word Register [29:16]
0x284 – 0x285	0x284 0x285	TRIG4_TGT_SL	0x0000	Trigger Output Unit 4 Target Time in Seconds Low-Word Register [15:0]
0x286 – 0x287	0x286 0x287	TRIG4_T-GT_SH	0x0000	Trigger Output Unit 4 Target Time in Seconds High-Word Register [31:16]
0x288 – 0x289	0x288 0x289	TRIG4_CFG_1	0x3C00	Trigger Output Unit 4 Configuration/Control Register1

TABLE 4-4: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TRIGGER OUTPUT (12 UNITS, 0X200 – 0X3FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x28A – 0x28B	0x28A 0x28B	TRIG4_CFG_2	0x0000	Trigger Output Unit 4 Configuration/Control Register2
0x28C – 0x28D	0x28C 0x28D	TRIG4_CFG_3	0x0000	Trigger Output Unit 4 Configuration/Control Register3
0x28E – 0x28F	0x28E 0x28F	TRIG4_CFG_4	0x0000	Trigger Output Unit 4 Configuration/Control Register4
0x290 – 0x291	0x290 0x291	TRIG4_CFG_5	0x0000	Trigger Output Unit 4 Configuration/Control Register5
0x292 – 0x293	0x292 0x293	TRIG4_CFG_6	0x0000	Trigger Output Unit 4 Configuration/Control Register6
0x294 – 0x295	0x294 0x295	TRIG4_CFG_7	0x0000	Trigger Output Unit 4 Configuration/Control Register7
0x296 – 0x297	0x296 0x297	TRIG4_CFG_8	0x0000	Trigger Output Unit 4 Configuration/Control Register8
0x298 – 0x29F	0x298 0x29F	Reserved (8-Bytes)	Don’t Care	None
0x2A0 – 0x2A1	0x2A0 0x2A1	TRIG5_TGT_NSL	0x0000	Trigger Output Unit 5 Target Time in Nanoseconds Low-Word Register [15:0]
0x2A2 – 0x2A3	0x2A2 0x2A3	TRIG5_TGT_NSH	0x0000	Trigger Output Unit 5 Target Time in Nanoseconds High-Word Register [29:16]
0x2A4 – 0x2A5	0x2A4 0x2A5	TRIG5_TGT_SL	0x0000	Trigger Output Unit 5 Target Time in Seconds Low-Word Register [15:0]
0x2A6 – 0x2A7	0x2A6 0x2A7	TRIG5_TGT_SH	0x0000	Trigger Output Unit 5 Target Time in Seconds High-Word Register [31:16]
0x2A8 – 0x2A9	0x2A8 0x2A9	TRIG5_CFG_1	0x3C00	Trigger Output Unit 5 Configuration/Control Register1
0x2AA – 0x2AB	0x2AA 0x2AB	TRIG5_CFG_2	0x0000	Trigger Output Unit 5 Configuration/Control Register2
0x2AC – 0x2AD	0x2AC 0x2AD	TRIG5_CFG_3	0x0000	Trigger Output Unit 5 Configuration/Control Register3
0x2AE – 0x2AF	0x2AE 0x2AF	TRIG5_CFG_4	0x0000	Trigger Output Unit 5 Configuration/Control Register4
0x2B0 – 0x2B1	0x2B0 0x2B1	TRIG5_CFG_5	0x0000	Trigger Output Unit 5 Configuration/Control Register5
0x2B2 – 0x2B3	0x2B2 0x2B3	TRIG5_CFG_6	0x0000	Trigger Output Unit 5 Configuration/Control Register6
0x2B4 – 0x2B5	0x2B4 0x2B5	TRIG5_CFG_7	0x0000	Trigger Output Unit 5 Configuration/Control Register7
0x2B6 – 0x2B7	0x2B6 0x2B7	TRIG5_CFG_8	0x0000	Trigger Output Unit 5 Configuration/Control Register8
0x2B8 – 0x2BF	0x2B8 0x2BF	Reserved (8-Bytes)	Don’t Care	None
0x2C0 – 0x2C1	0x2C0 0x2C1	TRIG6_TGT_NSL	0x0000	Trigger Output Unit 6 Target Time in Nanoseconds Low-Word Register [15:0]
0x2C2 – 0x2C3	0x2C2 0x2C3	TRIG6_TGT_NSH	0x0000	Trigger Output Unit 6 Target Time in Nanoseconds High-Word Register [29:16]

TABLE 4-4: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TRIGGER OUTPUT (12 UNITS, 0X200 – 0X3FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x2C4 – 0x2C5	0x2C4 0x2C5	TRIG6_TGT_SL	0x0000	Trigger Output Unit 6 Target Time in Seconds Low-Word Register [15:0]
0x2C6 – 0x2C7	0x2C6 0x2C7	TRIG6_TGT_SH	0x0000	Trigger Output Unit 6 Target Time in Seconds High-Word Register [31:16]
0x2C8 – 0x2C9	0x2C8 0x2C9	TRIG6_CFG_1	0x3C00	Trigger Output Unit 6 Configuration/Control Register1
0x2CA – 0x2CB	0x2CA 0x2CB	TRIG6_CFG_2	0x0000	Trigger Output Unit 6 Configuration/Control Register2
0x2CC – 0x2CD	0x2CC 0x2CD	TRIG6_CFG_3	0x0000	Trigger Output Unit 6 Configuration/Control Register3
0x2CE – 0x2CF	0x2CE 0x2CF	TRIG6_CFG_4	0x0000	Trigger Output Unit 6 Configuration/Control Register4
0x2D0 – 0x2D1	0x2D0 0x2D1	TRIG6_CFG_5	0x0000	Trigger Output Unit 6 Configuration/Control Register5
0x2D2 – 0x2D3	0x2D2 0x2D3	TRIG6_CFG_6	0x0000	Trigger Output Unit 6 Configuration/Control Register6
0x2D4 – 0x2D5	0x2D4 0x2D5	TRIG6_CFG_7	0x0000	Trigger Output Unit 6 Configuration/Control Register7
0x2D6 – 0x2D7	0x2D6 0x2D7	TRIG6_CFG_8	0x0000	Trigger Output Unit 6 Configuration/Control Register8
0x2D8 – 0x2DF	0x2D8 0x2DF	Reserved (8-Bytes)	Don’t Care	None
0x2E0 – 0x2E1	0x2E0 0x2E1	TRIG7_TGT_NSL	0x0000	Trigger Output Unit 7 Target Time in Nanoseconds Low-Word Register [15:0]
0x2E2 – 0x2E3	0x2E2 0x2E3	TRIG7_TGT_NSH	0x0000	Trigger Output Unit 7 Target Time in Nanoseconds High-Word Register [29:16]
0x2E4 – 0x2E5	0x2E4 0x2E5	TRIG7_TGT_SL	0x0000	Trigger Output Unit 7 Target Time in Seconds Low-Word Register [15:0]
0x2E6 – 0x2E7	0x2E6 0x2E7	TRIG7_TGT_SH	0x0000	Trigger Output Unit 7 Target Time in Seconds High-Word Register [31:16]
0x2E8 – 0x2E9	0x2E8 0x2E9	TRIG7_CFG_1	0x3C00	Trigger Output Unit 7 Configuration/Control Register1
0x2EA – 0x2EB	0x2EA 0x2EB	TRIG7_CFG_2	0x0000	Trigger Output Unit 7 Configuration/Control Register2
0x2EC – 0x2ED	0x2EC 0x2ED	TRIG7_CFG_3	0x0000	Trigger Output Unit 7 Configuration/Control Register3
0x2EE – 0x2EF	0x2EE 0x2EF	TRIG7_CFG_4	0x0000	Trigger Output Unit 7 Configuration/Control Register4
0x2F0 – 0x2F1	0x2F0 0x2F1	TRIG7_CFG_5	0x0000	Trigger Output Unit 7 Configuration/Control Register5
0x2F2 – 0x2F3	0x2F2 0x2F3	TRIG7_CFG_6	0x0000	Trigger Output Unit 7 Configuration/Control Register6
0x2F4 – 0x2F5	0x2F4 0x2F5	TRIG7_CFG_7	0x0000	Trigger Output Unit 7 Configuration/Control Register7
0x2F6 – 0x2F7	0x2F6 0x2F7	TRIG7_CFG_8	0x0000	Trigger Output Unit 7 Configuration/Control Register8

TABLE 4-4: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TRIGGER OUTPUT (12 UNITS, 0X200 – 0X3FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x2F8 – 0x2FF	0x2F8 0x2FF	Reserved (8-Bytes)	Don't Care	None
0x300 – 0x301	0x300 0x301	TRIG8_TGT_NSL	0x0000	Trigger Output Unit 8 Target Time in Nanoseconds Low-Word Register [15:0]
0x302 – 0x303	0x302 0x303	TRIG8_TGT_NSH	0x0000	Trigger Output Unit 8 Target Time in Nanoseconds High-Word Register [29:16]
0x304 – 0x305	0x304 0x305	TRIG8_TGT_SL	0x0000	Trigger Output Unit 8 Target Time in Seconds Low-Word Register [15:0]
0x306 – 0x307	0x306 0x307	TRIG8_TGT_SH	0x0000	Trigger Output Unit 8 Target Time in Seconds High-Word Register [31:16]
0x308 – 0x309	0x308 0x309	TRIG8_CFG_1	0x3C00	Trigger Output Unit 8 Configuration/Control Register1
0x30A – 0x30B	0x30A 0x30B	TRIG8_CFG_2	0x0000	Trigger Output Unit 8 Configuration/Control Register2
0x30C – 0x30D	0x30C 0x30D	TRIG8_CFG_3	0x0000	Trigger Output Unit 8 Configuration/Control Register3
0x30E – 0x30F	0x30E 0x30F	TRIG8_CFG_4	0x0000	Trigger Output Unit 8 Configuration/Control Register4
0x310 – 0x311	0x310 0x311	TRIG8_CFG_5	0x0000	Trigger Output Unit 8 Configuration/Control Register5
0x312 – 0x313	0x312 0x313	TRIG8_CFG_6	0x0000	Trigger Output Unit 8 Configuration/Control Register6
0x314 – 0x315	0x314 0x315	TRIG8_CFG_7	0x0000	Trigger Output Unit 8 Configuration/Control Register7
0x316 – 0x317	0x316 0x317	TRIG8_CFG_8	0x0000	Trigger Output Unit 8 Configuration/Control Register8
0x318 – 0x31F	0x318 0x31F	Reserved (8-Bytes)	Don't Care	None
0x320 – 0x321	0x320 0x321	TRIG9_TGT_NSL	0x0000	Trigger Output Unit 9 Target Time in Nanoseconds Low-Word Register [15:0]
0x322 – 0x323	0x322 0x323	TRIG9_TGT_NSH	0x0000	Trigger Output Unit 9 Target Time in Nanoseconds High-Word Register [29:16]
0x324 – 0x325	0x324 0x325	TRIG9_TGT_SL	0x0000	Trigger Output Unit 9 Target Time in Seconds Low-Word Register [15:0]
0x326 – 0x327	0x326 0x327	TRIG9_TGT_SH	0x0000	Trigger Output Unit 9 Target Time in Seconds High-Word Register [31:16]
0x328 – 0x329	0x328 0x329	TRIG9_CFG_1	0x3C00	Trigger Output Unit 9 Configuration/Control Register1
0x32A – 0x32B	0x32A 0x32B	TRIG9_CFG_2	0x0000	Trigger Output Unit 9 Configuration/Control Register2
0x32C – 0x32D	0x32C 0x32D	TRIG9_CFG_3	0x0000	Trigger Output Unit 9 Configuration/Control Register3
0x32E – 0x32F	0x32E 0x32F	TRIG9_CFG_4	0x0000	Trigger Output Unit 9 Configuration/Control Register4
0x330 – 0x331	0x330 0x331	TRIG9_CFG_5	0x0000	Trigger Output Unit 9 Configuration/Control Register5

TABLE 4-4: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TRIGGER OUTPUT (12 UNITS, 0X200 – 0X3FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x332 – 0x333	0x332 0x333	TRIG9_CFG_6	0x0000	Trigger Output Unit 9 Configuration/Control Register6
0x334 – 0x335	0x334 0x335	TRIG9_CFG_7	0x0000	Trigger Output Unit 9 Configuration/Control Register7
0x336 – 0x337	0x336 0x337	TRIG9_CFG_8	0x0000	Trigger Output Unit 9 Configuration/Control Register8
0x338 – 0x33F	0x338 0x33F	Reserved (8-Bytes)	Don't Care	None
0x340 – 0x341	0x340 0x341	TRIG10_T-GT_NSL	0x0000	Trigger Output Unit 10 Target Time in Nanoseconds Low-Word Register [15:0]
0x342 – 0x343	0x342 0x343	TRIG10_T-GT_NSH	0x0000	Trigger Output Unit 10 Target Time in Nanoseconds High-Word Register [29:16]
0x344 – 0x345	0x344 0x345	TRIG10_T-GT_SL	0x0000	Trigger Output Unit 10 Target Time in Seconds Low-Word Register [15:0]
0x346 – 0x347	0x346 0x347	TRIG10_T-GT_SH	0x0000	Trigger Output Unit 10 Target Time in Seconds High-Word Register [31:16]
0x348 – 0x349	0x348 0x349	TRIG10_CFG_1	0x3C00	Trigger Output Unit 10 Configuration/Control Register1
0x34A – 0x34B	0x34A 0x34B	TRIG10_CFG_2	0x0000	Trigger Output Unit 10 Configuration/Control Register2
0x34C – 0x34D	0x34C 0x34D	TRIG10_CFG_3	0x0000	Trigger Output Unit 10 Configuration/Control Register3
0x34E – 0x34F	0x34E 0x34F	TRIG10_CFG_4	0x0000	Trigger Output Unit 10 Configuration/Control Register4
0x350 – 0x351	0x350 0x351	TRIG10_CFG_5	0x0000	Trigger Output Unit 10 Configuration/Control Register5
0x352 – 0x353	0x352 0x353	TRIG10_CFG_6	0x0000	Trigger Output Unit 10 Configuration/Control Register6
0x354 – 0x355	0x354 0x355	TRIG10_CFG_7	0x0000	Trigger Output Unit 10 Configuration/Control Register7
0x356 – 0x357	0x356 0x357	TRIG10_CFG_8	0x0000	Trigger Output Unit 10 Configuration/Control Register8
0x358 – 0x35F	0x358 0x35F	Reserved (8-Bytes)	Don't Care	None
0x360 – 0x361	0x360 0x361	TRIG11_T-GT_NSL	0x0000	Trigger Output Unit 11 Target Time in Nanoseconds Low-Word Register [15:0]
0x362 – 0x363	0x362 0x363	TRIG11_T-GT_NSH	0x0000	Trigger Output Unit 11 Target Time in Nanoseconds High-Word Register [29:16]
0x364 – 0x365	0x364 0x365	TRIG11_T-GT_SL	0x0000	Trigger Output Unit 11 Target Time in Seconds Low-Word Register [15:0]
0x366 – 0x367	0x366 0x367	TRIG11_T-GT_SH	0x0000	Trigger Output Unit 11 Target Time in Seconds High-Word Register [31:16]
0x368 – 0x369	0x368 0x369	TRIG11_CFG_1	0x3C00	Trigger Output Unit 11 Configuration/Control Register1
0x36A – 0x36B	0x36A 0x36B	TRIG11_CFG_2	0x0000	Trigger Output Unit 11 Configuration/Control Register2

TABLE 4-4: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TRIGGER OUTPUT (12 UNITS, 0X200 – 0X3FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x36C – 0x36D	0x36C 0x36D	TRIG11_CFG_3	0x0000	Trigger Output Unit 11 Configuration/Control Register3
0x36E – 0x36F	0x36E 0x36F	TRIG11_CFG_4	0x0000	Trigger Output Unit 11 Configuration/Control Register4
0x370 – 0x371	0x370 0x371	TRIG11_CFG_5	0x0000	Trigger Output Unit 11 Configuration/Control Register5
0x372 – 0x373	0x372 0x373	TRIG11_CFG_6	0x0000	Trigger Output Unit 11 Configuration/Control Register6
0x374 – 0x375	0x374 0x375	TRIG11_CFG_7	0x0000	Trigger Output Unit 11 Configuration/Control Register7
0x376 – 0x377	0x376 0x377	TRIG11_CFG_8	0x0000	Trigger Output Unit 11 Configuration/Control Register8
0x378 – 0x37F	0x378 0x37F	Reserved (8-Bytes)	Don’t Care	None
0x380 – 0x381	0x380 0x381	TRIG12_TGT_NSL	0x0000	Trigger Output Unit 12 Target Time in Nanoseconds Low-Word Register [15:0]
0x382 – 0x383	0x382 0x383	TRIG12_TGT_NSH	0x0000	Trigger Output Unit 12 Target Time in Nanoseconds High-Word Register [29:16]
0x384 – 0x385	0x384 0x385	TRIG12_TGT_SL	0x0000	Trigger Output Unit 12 Target Time in Seconds Low-Word Register [15:0]
0x386 – 0x387	0x386 0x387	TRIG12_TGT_SH	0x0000	Trigger Output Unit 12 Target Time in Seconds High-Word Register [31:16]
0x388 – 0x389	0x388 0x389	TRIG12_CFG_1	0x3C00	Trigger Output Unit 12 Configuration/Control Register1
0x38A – 0x38B	0x38A 0x38B	TRIG12_CFG_2	0x0000	Trigger Output Unit 12 Configuration/Control Register2
0x38C – 0x38D	0x38C 0x38D	TRIG12_CFG_3	0x0000	Trigger Output Unit 12 Configuration/Control Register3
0x38E – 0x38F	0x38E 0x38F	TRIG12_CFG_4	0x0000	Trigger Output Unit 12 Configuration/Control Register4
0x390 – 0x391	0x390 0x391	TRIG12_CFG_5	0x0000	Trigger Output Unit 12 Configuration/Control Register5
0x392 – 0x393	0x392 0x393	TRIG12_CFG_6	0x0000	Trigger Output Unit 12 Configuration/Control Register6
0x394 – 0x395	0x394 0x395	TRIG12_CFG_7	0x0000	Trigger Output Unit 12 Configuration/Control Register7
0x396 – 0x397	0x396 0x397	TRIG12_CFG_8	0x0000	Trigger Output Unit 12 Configuration/Control Register8
0x398 – 0x3FF	0x398 0x3FF	Reserved (104-Bytes)	Don’t Care	None

TABLE 4-5: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TIME STAMP INPUTS (12 UNITS, 0X400 – 0X5FF)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x400 – 0x401	0x400 0x401	TS_RDY	0x0000	Input Unit Ready Register [11:0]
0x402 – 0x403	0x402 0x403	TS_EN	0x0000	Time stamp Input Unit Enable Register [11:0]
0x404 – 0x405	0x404 0x405	TS_SW_RST	0x0000	Time stamp Input Unit Software Reset Register [11:0]
0x406 – 0x41F	0x406 0x41F	Reserved (26-Bytes)	Don't Care	None
0x420 – 0x421	0x420 0x421	TS1_STATUS	0x0000	Time stamp Input Unit 1 Status Register
0x422 – 0x423	0x422 0x423	TS1_CFG	0x0000	Time stamp Input Unit 1 Configuration/Control Register
0x424 – 0x425	0x424 0x425	TS1_SM-PL1_NSL	0x0000	Time stamp Unit 1 Input Sample Time (1st) in Nanoseconds Low-Word Register [15:0]
0x426 – 0x427	0x426 0x427	TS1_SM-PL1_NSH	0x0000	Time stamp Unit 1 Input Sample Time (1st) in Nanoseconds High-Word Register [29:16]
0x428 – 0x429	0x428 0x429	TS1_SM-PL1_SL	0x0000	Time stamp Unit 1 Input Sample Time (1st) in Seconds Low-Word Register [15:0]
0x42A – 0x42B	0x42A 0x42B	TS1_SM-PL1_SH	0x0000	Time stamp Unit 1 Input Sample Time (1st) in Seconds High-Word Register [31:16]
0x42C – 0x42D	0x42C 0x42D	TS1_SMPL1_-SUB_NS	0x0000	Time stamp Unit 1 Input Sample Time (1st) in Sub-Nanoseconds Register [2:0]
0x42E – 0x433	0x42E 0x433	Reserved (6-Bytes)	Don't Care	None
0x434 – 0x435	0x434 0x435	TS1_SM-PL2_NSL	0x0000	Time stamp Unit 1 Input Sample Time (2nd) in Nanoseconds Low-Word Register [15:0]
0x436 – 0x437	0x436 0x437	TS1_SM-PL2_NSH	0x0000	Time stamp Unit 1 Input Sample Time (2nd) in Nanoseconds High-Word Register [29:16]
0x438 – 0x439	0x438 0x439	TS1_SM-PL2_SL	0x0000	Time stamp Unit 1 Input Sample Time (2nd) in Seconds Low-Word Register [15:0]
0x43A – 0x43B	0x43A 0x43B	TS1_SM-PL2_SH	0x0000	Time stamp Unit 1 Input Sample Time (2nd) in Seconds High-Word Register [31:16]
0x43C – 0x43D	0x43C 0x43D	TS1_SMPL2_-SUB_NS	0x0000	Time stamp Unit 1 Input Sample Time (2nd) in Sub-Nanoseconds Register [2:0]
0x43E – 0x43F	0x43E 0x43F	Reserved (2-Bytes)	Don't Care	None
0x440 – 0x441	0x440 0x441	TS2_STATUS	0x0000	Time stamp Input Unit 2 Status Register
0x442 – 0x443	0x442 0x443	TS2_CFG	0x0000	Time stamp Input Unit 2 Configuration/Control Register
0x444 – 0x445	0x444 0x445	TS2_SM-PL1_NSL	0x0000	Time stamp Unit 2 Input Sample Time (1st) in Nanoseconds Low-Word Register [15:0]
0x446 – 0x447	0x446 0x447	TS2_SM-PL1_NSH	0x0000	Time stamp Unit 2 Input Sample Time (1st) in Nanoseconds High-Word Register [29:16]

TABLE 4-5: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TIME STAMP INPUTS (12 UNITS, 0X400 – 0X5FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x448 – 0x449	0x448 0x449	TS2_SM-PL1_SL	0x0000	Time stamp Unit 2 Input Sample Time (1st) in Seconds Low-Word Register [15:0]
0x44A – 0x44B	0x44A 0x44B	TS2_SM-PL1_SH	0x0000	Time stamp Unit 2 Input Sample Time (1st) in Seconds High-Word Register [31:16]
0x44C – 0x44D	0x44C 0x44D	TS2_SMPL1_-SUB_NS	0x0000	Time stamp Unit 2 Input Sample Time (1st) in Sub-Nanoseconds Register [2:0]
0x44E – 0x453	0x44E 0x453	Reserved (6-Bytes)	Don't Care	None
0x454 – 0x455	0x454 0x455	TS2_SM-PL2_NSL	0x0000	Time stamp Unit 2 Input Sample Time (2nd) in Nanoseconds Low-Word Register [15:0]
0x456 – 0x457	0x456 0x457	TS2_SM-PL2_NSH	0x0000	Time stamp Unit 2 Input Sample Time (2nd) in Nanoseconds High-Word Register [29:16]
0x458 – 0x459	0x458 0x459	TS2_SMP2_SL	0x0000	Time stamp Unit 2 Input Sample Time (2nd) in Seconds Low-Word Register [15:0]
0x45A – 0x45B	0x45A 0x45B	TS2_SM-PL2_SH	0x0000	Time stamp Unit 2 Input Sample Time (2nd) in Seconds High-Word Register [31:16]
0x45C – 0x45D	0x45C 0x45D	TS2_SMPL2_-SUB_NS	0x0000	Time stamp Unit 2 Input Sample Time (2nd) in Sub-Nanoseconds Register [2:0]
0x45E – 0x45F	0x45E 0x45F	Reserved (2-Bytes)	Don't Care	None
0x460 – 0x461	0x460 0x461	TS3_STATUS	0x0000	Time stamp Input Unit 3 Status Register
0x462 – 0x463	0x462 0x463	TS3_CFG	0x0000	Time stamp Input Unit 3 Configuration/Control Register
0x464 – 0x465	0x464 0x465	TS3_SM-PL1_NSL	0x0000	Time stamp Unit 3 Input Sample Time (1st) in Nanoseconds Low-Word Register [15:0]
0x466 – 0x467	0x466 0x467	TS3_SM-PL1_NSH	0x0000	Time stamp Unit 3 Input Sample Time (1st) in Nanoseconds High-Word Register [29:16]
0x468 – 0x469	0x468 0x469	TS3_SM-PL1_SL	0x0000	Time stamp Unit 3 Input Sample Time (1st) in Seconds Low-Word Register [15:0]
0x46A – 0x46B	0x46A 0x46B	TS3_SM-PL1_SH	0x0000	Time stamp Unit 3 Input Sample Time (1st) in Seconds High-Word Register [31:16]
0x46C – 0x46D	0x46C 0x46D	TS3_SMPL1_-SUB_NS	0x0000	Time stamp Unit 3 Input Sample Time (1st) in Sub-Nanoseconds Register [2:0]
0x46E – 0x473	0x46E 0x473	Reserved (6-Bytes)	Don't Care	None
0x474 – 0x475	0x474 0x475	TS3_SM-PL2_NSL	0x0000	Time stamp Unit 3 Input Sample Time (2nd) in Nanoseconds Low-Word Register [15:0]
0x476 – 0x477	0x476 0x477	TS3_SM-PL2_NSH	0x0000	Time stamp Unit 3 Input Sample Time (2nd) in Nanoseconds High-Word Register [29:16]
0x478 – 0x479	0x478 0x479	TS3_SMP2_SL	0x0000	Time stamp Unit 3 Input Sample Time (2nd) in Seconds Low-Word Register [15:0]
0x47A – 0x47B	0x47A 0x47B	TS3_SM-PL2_SH	0x0000	Time stamp Unit 3 Input Sample Time (2nd) in Seconds High-Word Register [31:16]

TABLE 4-5: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TIME STAMP INPUTS (12 UNITS, 0X400 – 0X5FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x47C – 0x47D	0x47C 0x47D	TS3_SMPL2_-SUB_NS	0x0000	Time stamp Unit 3 Input Sample Time (2nd) in Sub-Nanoseconds Register [2:0]
0x47E – 0x47F	0x47E 0x47F	Reserved (2-Bytes)	Don't Care	None
0x480 – 0x481	0x480 0x481	TS4_STATUS	0x0000	Time stamp Input Unit 4 Status Register
0x482 – 0x483	0x482 0x483	TS4_CFG	0x0000	Time stamp Input Unit 4 Configuration/Control Register
0x484 – 0x485	0x484 0x485	TS4_SM-PL1_NSL	0x0000	Time stamp Unit 4 Input Sample Time (1st) in Nanoseconds Low-Word Register [15:0]
0x486 – 0x487	0x486 0x487	TS4_SM-PL1_NSH	0x0000	Time stamp Unit 4 Input Sample Time (1st) in Nanoseconds High-Word Register [29:16]
0x488 – 0x489	0x488 0x489	TS4_SM-PL1_SL	0x0000	Time stamp Unit 4 Input Sample Time (1st) in Seconds Low-Word Register [15:0]
0x48A – 0x48B	0x48A 0x48B	TS4_SM-PL1_SH	0x0000	Time stamp Unit 4 Input Sample Time (1st) in Seconds High-Word Register [31:16]
0x48C – 0x48D	0x48C 0x48D	TS4_SMPL1_-SUB_NS	0x0000	Time stamp Unit 4 Input Sample Time (1st) in Sub-Nanoseconds Register [2:0]
0x48E – 0x493	0x48E 0x493	Reserved (6-Bytes)	Don't Care	None
0x494 – 0x495	0x494 0x495	TS4_SM-PL2_NSL	0x0000	Time stamp Unit 4 Input Sample Time (2nd) in Nanoseconds Low-Word Register [15:0]
0x496 – 0x497	0x496 0x497	TS4_SM-PL2_NSH	0x0000	Time stamp Unit 4 Input Sample Time (2nd) in Nanoseconds High-Word Register [29:16]
0x498 – 0x499	0x498 0x499	TS4_SMP2_SL	0x0000	Time stamp Unit 4 Input Sample Time (2nd) in Seconds Low-Word Register [15:0]
0x49A – 0x49B	0x49A 0x49B	TS4_SM-PL2_SH	0x0000	Time stamp Unit 4 Input Sample Time (2nd) in Seconds High-Word Register [31:16]
0x49C – 0x49D	0x49C 0x49D	TS4_SMPL2_-SUB_NS	0x0000	Time stamp Unit 4 Input Sample Time (2nd) in Sub-Nanoseconds Register [2:0]
0x49E – 0x49F	0x49E 0x49F	Reserved (2-Bytes)	Don't Care	None
0x4A0 – 0x4A1	0x4A0 0x4A1	TS5_STATUS	0x0000	Time stamp Input Unit 5 Status Register
0x4A0 – 0x4A1	0x4A0 0x4A1	TS5_STATUS	0x0000	Time stamp Input Unit 5 Status Register
0x4A2 – 0x4A3	0x4A2 0x4A3	TS5_CFG	0x0000	Time stamp Input Unit 5 Configuration/Control Register
0x4A4 – 0x4A5	0x4A4 0x4A5	TS5_SMPL1_NSL	0x0000	Time stamp Unit 5 Input Sample Time (1st) in Nanoseconds Low-Word Register [15:0]
0x4A6 – 0x4A7	0x4A6 0x4A7	TS5_SMPL1_NSH	0x0000	Time stamp Unit 5 Input Sample Time (1st) in Nanoseconds High-Word Register [29:16]
0x4A8 – 0x4A9	0x4A8 0x4A9	TS5_SM-PL1_SL	0x0000	Time stamp Unit 5 Input Sample Time (1st) in Seconds Low-Word Register [15:0]

TABLE 4-5: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TIME STAMP INPUTS (12 UNITS, 0X400 – 0X5FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x4AA – 0x4AB	0x4AA 0x4AB	TS5_SM-PL1_SH	0x0000	Time stamp Unit 5 Input Sample Time (1st) in Seconds High-Word Register [31:16]
0x4AC – 0x4AD	0x4AC 0x4AD	TS5_SMPL1_-SUB_NS	0x0000	Time stamp Unit 5 Input Sample Time (1st) in Sub-Nanoseconds Register [2:0]
0x4AE – 0x4B3	0x4AE 0x4B3	Reserved (6-Bytes)	Don't Care	None
0x4B4 – 0x4B5	0x4B4 0x4B5	TS5_SM-PL2_NSL	0x0000	Time stamp Unit 5 Input Sample Time (2nd) in Nanoseconds Low-Word Register [15:0]
0x4B6 – 0x4B7	0x4B6 0x4B7	TS5_SM-PL2_NSH	0x0000	Time stamp Unit 5 Input Sample Time (2nd) in Nanoseconds High-Word Register [29:16]
0x4B8 – 0x4B9	0x4B8 0x4B9	TS5_SMP2_SL	0x0000	Time stamp Unit 5 Input Sample Time (2nd) in Seconds Low-Word Register [15:0]
0x4BA – 0x4BB	0x4BA 0x4BB	TS5_SM-PL2_SH	0x0000	Time stamp Unit 5 Input Sample Time (2nd) in Seconds High-Word Register [31:16]
0x4BC – 0x4BD	0x4BC 0x4BD	TS5_SMPL2_-SUB_NS	0x0000	Time stamp Unit 5 Input Sample Time (2nd) in Sub-Nanoseconds Register [2:0]
0x4BE – 0x4BF	0x4BE 0x4BF	Reserved (2-Bytes)	Don't Care	None
0x4C0 – 0x4C1	0x4C0 0x4C1	TS6_STATUS	0x0000	Time stamp Input Unit 6 Status Register
0x4C2 – 0x4C3	0x4C2 0x4C3	TS6_CFG	0x0000	Time stamp Input Unit 6 Configuration/Control Register
0x4C4 – 0x4C5	0x4C4 0x4C5	TS6_SM-PL1_NSL	0x0000	Time stamp Unit 6 Input Sample Time (1st) in Nanoseconds Low-Word Register [15:0]
0x4C6 – 0x4C7	0x4C6 0x4C7	TS6_SM-PL1_NSH	0x0000	Time stamp Unit 6 Input Sample Time (1st) in Nanoseconds High-Word Register [29:16]
0x4C8 – 0x4C9	0x4C8 0x4C9	TS6_SM-PL1_SL	0x0000	Time stamp Unit 6 Input Sample Time (1st) in Seconds Low-Word Register [15:0]
0x4CA – 0x4CB	0x4CA 0x4CB	TS6_SM-PL1_SH	0x0000	Time stamp Unit 6 Input Sample Time (1st) in Seconds High-Word Register [31:16]
0x4CC – 0x4CD	0x4CC 0x4CD	TS6_SMPL1_-SUB_NS	0x0000	Time stamp Unit 6 Input Sample Time (1st) in Sub-Nanoseconds Register [2:0]
0x4CE – 0x4D3	0x4CE 0x4D3	Reserved (6-Bytes)	Don't Care	None
0x4D4 – 0x4D5	0x4D4 0x4D5	TS6_SM-PL2_NSL	0x0000	Time stamp Unit 6 Input Sample Time (2nd) in Nanoseconds Low-Word Register [15:0]
0x4D6 – 0x4D7	0x4D6 0x4D7	TS6_SM-PL2_NSH	0x0000	Time stamp Unit 6 Input Sample Time (2nd) in Nanoseconds High-Word Register [29:16]
0x4D8 – 0x4D9	0x4D8 0x4D9	TS6_SMP2_SL	0x0000	Time stamp Unit 6 Input Sample Time (2nd) in Seconds Low-Word Register [15:0]
0x4DA – 0x4DB	0x4DA 0x4DB	TS6_SM-PL2_SH	0x0000	Time stamp Unit 6 Input Sample Time (2nd) in Seconds High-Word Register [31:16]
0x4DC – 0x4DD	0x4DC 0x4DD	TS6_SMPL2_-SUB_NS	0x0000	Time stamp Unit 6 Input Sample Time (2nd) in Sub-Nanoseconds Register [2:0]

TABLE 4-5: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TIME STAMP INPUTS (12 UNITS, 0X400 – 0X5FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x4DE – 0x4DF	0x4DE 0x4DF	Reserved (2-Bytes)	Don't Care	None
0x4E0 – 0x4E1	0x4E0 0x4E1	TS7_STATUS	0x0000	Time stamp Input Unit 7 Status Register
0x4E2 – 0x4E3	0x4E2 0x4E3	TS7_CFG	0x0000	Time stamp Input Unit 7 Configuration/Control Register
0x4E4 – 0x4E5	0x4E4 0x4E5	TS7_SMPL1_NSL	0x0000	Time stamp Unit 7 Input Sample Time (1st) in Nanoseconds Low-Word Register [15:0]
0x4E6 – 0x4E7	0x4E6 0x4E7	TS7_SMPL1_NSH	0x0000	Time stamp Unit 7 Input Sample Time (1st) in Nanoseconds High-Word Register [29:16]
0x4E8 – 0x4E9	0x4E8 0x4E9	TS7_SMPL1_SL	0x0000	Time stamp Unit 7 Input Sample Time (1st) in Seconds Low-Word Register [15:0]
0x4EA – 0x4EB	0x4EA 0x4EB	TS7_SMPL1_SH	0x0000	Time stamp Unit 7 Input Sample Time (1st) in Seconds High-Word Register [31:16]
0x4EC – 0x4ED	0x4EC 0x4ED	TS7_SMPL1_SUB_NS	0x0000	Time stamp Unit 7 Input Sample Time (1st) in Sub-Nanoseconds Register [2:0]
0x4EE – 0x4F3	0x4EE 0x4F3	Reserved (6-Bytes)	Don't Care	None
0x4F4 – 0x4F5	0x4F4 0x4F5	TS7_SMPL2_NSL	0x0000	Time stamp Unit 7 Input Sample Time (2nd) in Nanoseconds Low-Word Register [15:0]
0x4F6 – 0x4F7	0x4F6 0x4F7	TS7_SMPL2_NSH	0x0000	Time stamp Unit 7 Input Sample Time (2nd) in Nanoseconds High-Word Register [29:16]
0x4F8 – 0x4F9	0x4F8 0x4F9	TS7_SMP2_SL	0x0000	Time stamp Unit 7 Input Sample Time (2nd) in Seconds Low-Word Register [15:0]
0x4FA – 0x4FB	0x4FA 0x4FB	TS7_SMPL2_SH	0x0000	Time stamp Unit 7 Input Sample Time (2nd) in Seconds High-Word Register [31:16]
0x4FC – 0x4FD	0x4FC 0x4FD	TS7_SMPL2_SUB_NS	0x0000	Time stamp Unit 7 Input Sample Time (2nd) in Sub-Nanoseconds Register [2:0]
0x4FE – 0x4FF	0x4FE 0x4FF	Reserved (2-Bytes)	Don't Care	None
0x500 – 0x501	0x500 0x501	TS8_STATUS	0x0000	Time stamp Input Unit 8 Status Register
0x502 – 0x503	0x502 0x503	TS8_CFG	0x0000	Time stamp Input Unit 8 Configuration/Control Register
0x504 – 0x505	0x504 0x505	TS8_SMPL1_NSL	0x0000	Time stamp Unit 8 Input Sample Time (1st) in Nanoseconds Low-Word Register [15:0]
0x506 – 0x507	0x506 0x507	TS8_SMPL1_NSH	0x0000	Time stamp Unit 8 Input Sample Time (1st) in Nanoseconds High-Word Register [29:16]
0x508 – 0x509	0x508 0x509	TS8_SMPL1_SL	0x0000	Time stamp Unit 8 Input Sample Time (1st) in Seconds Low-Word Register [15:0]
0x50A – 0x50B	0x50A 0x50B	TS8_SMPL1_SH	0x0000	Time stamp Unit 8 Input Sample Time (1st) in Seconds High-Word Register [31:16]
0x50C – 0x50D	0x50C 0x50D	TS8_SMPL1_SUB_NS	0x0000	Time stamp Unit 8 Input Sample Time (1st) in Sub-Nanoseconds Register [2:0]

TABLE 4-5: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TIME STAMP INPUTS (12 UNITS, 0X400 – 0X5FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x50E – 0x513	0x50E 0x513	Reserved (6-Bytes)	Don't Care	None
0x514 – 0x515	0x514 0x515	TS8_SM- PL2_NSL	0x0000	Time stamp Unit 8 Input Sample Time (2nd) in Nanoseconds Low-Word Register [15:0]
0x516 – 0x517	0x516 0x517	TS8_SM- PL2_NSH	0x0000	Time stamp Unit 8 Input Sample Time (2nd) in Nanoseconds High-Word Register [29:16]
0x518 – 0x519	0x518 0x519	TS8_SMP2_SL	0x0000	Time stamp Unit 8 Input Sample Time (2nd) in Seconds Low-Word Register [15:0]
0x51A – 0x51B	0x51A 0x51B	TS8_SM- PL2_SH	0x0000	Time stamp Unit 8 Input Sample Time (2nd) in Seconds High-Word Register [31:16]
0x51C – 0x51D	0x51C 0x51D	TS8_SMPL2_- SUB_NS	0x0000	Time stamp Unit 8 Input Sample Time (2nd) in Sub-Nanoseconds Register [2:0]
0x51E – 0x51F	0x51E 0x51F	Reserved (2-Bytes)	Don't Care	None
0x520 – 0x521	0x520 0x521	TS9_STATUS	0x0000	Time stamp Input Unit 9 Status Register
0x522 – 0x523	0x522 0x523	TS9_CFG	0x0000	Time stamp Input Unit 9 Configuration/Control Register
0x524 – 0x525	0x524 0x525	TS9_SM- PL1_NSL	0x0000	Time stamp Unit 9 Input Sample Time (1^{st}) in Nanoseconds High-Word Register [15:0]
0x526 – 0x527	0x526 0x527	TS9_SM- PL1_NSH	0x0000	Time stamp Unit 9 Input Sample Time (1^{st}) in Nanoseconds High-Word Register [29:16]
0x528 – 0x529	0x528 0x529	TS9_SM- PL1_SL	0x0000	Time stamp Unit 9 Input Sample Time (1^{st}) in Seconds High-Word Register [15:0]
0x52A – 0x52B	0x52A 0x52B	TS9_SM- PL1_SH	0x0000	Time stamp Unit 9 Input Sample Time (1^{st}) in Seconds High-Word Register [31:16]
0x52C – 0x52D	0x52C 0x52D	TS9_SMPL1_- SUB_NS	0x0000	Time stamp Unit 9 Input Sample Time (1^{st}) in Sub-Nanoseconds Register [2:0]
0x52E – 0x533	0x52E 0x533	Reserved (6-Bytes)	Don't Care	None
0x534 – 0x535	0x534 0x535	TS9_SM- PL2_NSL	0x0000	Time stamp Unit 9 Input Sample Time (2nd) in Nanoseconds Low-Word Register [15:0]
0x536 – 0x537	0x536 0x537	TS9_SM- PL2_NSH	0x0000	Time stamp Unit 9 Input Sample Time (2nd) in Nanoseconds High-Word Register [29:16]
0x538 – 0x539	0x538 0x539	TS9_SMP2_SL	0x0000	Time stamp Unit 9 Input Sample Time (2nd) in Seconds Low-Word Register [15:0]
0x53A – 0x53B	0x53A 0x53B	TS9_SM- PL2_SH	0x0000	Time stamp Unit 9 Input Sample Time (2nd) in Seconds High-Word Register [31:16]
0x53C – 0x53D	0x53C 0x53D	TS9_SMPL2_- SUB_NS	0x0000	Time stamp Unit 9 Input Sample Time (2nd) in Sub-Nanoseconds Register [2:0]
0x53E – 0x53F	0x53E 0x53F	Reserved (2-Bytes)	Don't Care	None
0x540 – 0x541	0x540 0x541	TS10_STATUS	0x0000	Time stamp Input Unit 10 Status Register

TABLE 4-5: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TIME STAMP INPUTS (12 UNITS, 0X400 – 0X5FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x542 – 0x543	0x542 0x543	TS10_CFG	0x0000	Time stamp Input Unit 10 Configuration/ Control Register
0x544 – 0x545	0x544 0x545	TS10_SM-PL1_NSL	0x0000	Time stamp Unit 10 Input Sample Time (1st) in Nanoseconds Low-Word Register [15:0]
0x546 – 0x547	0x546 0x547	TS10_SM-PL1_NSH	0x0000	Time stamp Unit 10 Input Sample Time (1st) in Nanoseconds High-Word Register [29:16]
0x548 – 0x549	0x548 0x549	TS10_SM-PL1_SL	0x0000	Time stamp Unit 10 Input Sample Time (1st) in Seconds Low-Word Register [15:0]
0x54A – 0x54B	0x54A 0x54B	TS10_SM-PL1_SH	0x0000	Time stamp Unit 10 Input Sample Time (1st) in Seconds High-Word Register [31:16]
0x54C – 0x54D	0x54C 0x54D	TS10_SMPL1_-SUB_NS	0x0000	Time stamp Unit 10 Input Sample Time (1st) in Sub-Nanoseconds Register [2:0]
0x54E – 0x553	0x54E 0x553	Reserved (6-Bytes)	Don't Care	None
0x554 – 0x555	0x554 0x555	TS10_SM-PL2_NSL	0x0000	Time stamp Unit 10 Input Sample Time (2nd) in Nanoseconds Low-Word Register [15:0]
0x556 – 0x557	0x556 0x557	TS10_SM-PL2_NSH	0x0000	Time stamp Unit 10 Input Sample Time (2nd) in Nanoseconds High-Word Register [29:16]
0x558 – 0x559	0x558 0x559	TS10_SMP2_SL	0x0000	Time stamp Unit 10 Input Sample Time (2nd) in Seconds Low-Word Register [15:0]
0x55A – 0x55B	0x55A 0x55B	TS10_SM-PL2_SH	0x0000	Time stamp Unit 10 Input Sample Time (2nd) in Seconds High-Word Register [31:16]
0x55C – 0x55D	0x55C 0x55D	TS10_SMPL2_-SUB_NS	0x0000	Time stamp Unit 10 Input Sample Time (2nd) in Sub-Nanoseconds Register [2:0]
0x55E – 0x55F	0x55E 0x55F	Reserved (2-Bytes)	Don't Care	None
0x560 – 0x561	0x560 0x561	TS11_STATUS	0x0000	Time stamp Input Unit 11 Status Register
0x562 – 0x563	0x562 0x563	TS11_CFG	0x0000	Time stamp Input Unit 11 Configuration/ Control Register
0x564 – 0x565	0x564 0x565	TS11_SM-PL1_NSL	0x0000	Time stamp Unit 11 Input Sample Time (1st) in Nanoseconds Low-Word Register [15:0]
0x566 – 0x567	0x566 0x567	TS11_SM-PL1_NSH	0x0000	Time stamp Unit 11 Input Sample Time (1st) in Nanoseconds High-Word Register [29:16]
0x568 – 0x569	0x568 0x569	TS11_SM-PL1_SL	0x0000	Time stamp Unit 11 Input Sample Time (1st) in Seconds Low-Word Register [15:0]
0x56A – 0x56B	0x56A 0x56B	TS11_SM-PL1_SH	0x0000	Time stamp Unit 11 Input Sample Time (1st) in Seconds High-Word Register [31:16]
0x56C – 0x56D	0x56C 0x56D	TS11_SMPL1_-SUB_NS	0x0000	Time stamp Unit 11 Input Sample Time (1st) in Sub-Nanoseconds Register [2:0]
0x56E – 0x573	0x56E 0x573	Reserved (6-Bytes)	Don't Care	None

TABLE 4-5: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TIME STAMP INPUTS (12 UNITS, 0X400 – 0X5FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x574 – 0x575	0x574 0x575	TS11_SM-PL2_NSL	0x0000	Time stamp Unit 11 Input Sample Time (2nd) in Nanoseconds Low-Word Register [15:0]
0x576 – 0x577	0x576 0x577	TS11_SM-PL2_NSH	0x0000	Time stamp Unit 11 Input Sample Time (2nd) in Nanoseconds High-Word Register [29:16]
0x578 – 0x579	0x578 0x579	TS11_SMP2_SL	0x0000	Time stamp Unit 11 Input Sample Time (2nd) in Seconds Low-Word Register [15:0]
0x57A – 0x57B	0x57A 0x57B	TS11_SM-PL2_SH	0x0000	Time stamp Unit 11 Input Sample Time (2nd) in Seconds High-Word Register [31:16]
0x57C – 0x57D	0x57C 0x57D	TS11_SMPL2_-SUB_NS	0x0000	Time stamp Unit 11 Input Sample Time (2nd) in Sub-Nanoseconds Register [2:0]
0x57E – 0x57F	0x57E 0x57F	Reserved (2-Bytes)	Don't Care	None
0x580 – 0x581	0x580 0x581	TS12_STATUS	0x0000	Time stamp Input Unit 12 Status Register
0x582 – 0x583	0x582 0x583	TS12_CFG	0x0000	Time stamp Input Unit 12 Configuration/ Control Register
0x584 – 0x585	0x584 0x585	TS12_SM-PL1_NSL	0x0000	Time stamp Unit 12 Input Sample Time (1st) in Nanoseconds Low-Word Register [15:0]
0x586 – 0x587	0x586 0x587	TS12_SM-PL1_NSH	0x0000	Time stamp Unit 12 Input Sample Time (1st) in Nanoseconds High-Word Register [29:16]
0x588 – 0x589	0x588 0x589	TS12_SM-PL1_SL	0x0000	Time stamp Unit 12 Input Sample Time (1st) in Seconds Low-Word Register [15:0]
0x58A – 0x58B	0x58A 0x58B	TS12_SM-PL1_SH	0x0000	Time stamp Unit 12 Input Sample Time (1st) in Seconds High-Word Register [31:16]
0x58C – 0x58D	0x58C 0x58D	TS12_SMPL1_-SUB_NS	0x0000	Time stamp Unit 12 Input Sample Time (1st) in Sub-Nanoseconds Register [2:0]
0x58E – 0x593	0x58E 0x593	Reserved (6-Bytes)	Don't Care	None
0x594 – 0x595	0x594 0x595	TS12_SM-PL2_NSL	0x0000	Time stamp Unit 12 Input Sample Time (2nd) in Nanoseconds Low-Word Register [15:0]
0x596 – 0x597	0x596 0x597	TS12_SM-PL2_NSH	0x0000	Time stamp Unit 12 Input Sample Time (2nd) in Nanoseconds High-Word Register [29:16]
0x598 – 0x599	0x598 0x599	TS12_SMP2_SL	0x0000	Time stamp Unit 12 Input Sample Time (2nd) in Seconds Low-Word Register [15:0]
0x59A – 0x59B	0x59A 0x59B	TS12_SM-PL2_SH	0x0000	Time stamp Unit 12 Input Sample Time (2nd) in Seconds High-Word Register [31:16]
0x59C – 0x59D	0x59C 0x59D	TS12_SMPL2_-SUB_NS	0x0000	Time stamp Unit 12 Input Sample Time (2nd) in Sub-Nanoseconds Register [2:0]
0x59E – 0x5A3	0x59E 0x5A3	Reserved (6-Bytes)	Don't Care	None

TABLE 4-5: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TIME STAMP INPUTS (12 UNITS, 0X400 – 0X5FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x5A4 – 0x5A5	0x5A4 0x5A5	TS12_SM-PL3_NSL	0x0000	Time stamp Unit 12 Input Sample Time (3rd) in Nanoseconds Low-Word Register [15:0]
0x5A6 – 0x5A7	0x5A6 0x5A7	TS12_SM-PL3_NSH	0x0000	Time stamp Unit 12 Input Sample Time (3rd) in Nanoseconds High-Word Register [29:16]
0x5A8 – 0x5A9	0x5A8 0x5A9	TS12_SM-PL3_SL	0x0000	Time stamp Unit 12 Input Sample Time (3rd) in Seconds Low-Word Register [15:0]
0x5AA – 0x5AB	0x5AA 0x5AB	TS12_SM-PL3_SH	0x0000	Time stamp Unit 12 Input Sample Time (3rd) in Seconds High-Word Register [31:16]
0x5AC – 0x5AD	0x5AC 0x5AD	TS12_SMPL3_-SUB_NS	0x0000	Time stamp Unit 12 Input Sample Time (3rd) in Sub-Nanoseconds Register [2:0]
0x5AE – 0x5B3	0x5AE 0x5B3	Reserved (6-Bytes)	Don't Care	None
0x5B4 – 0x5B5	0x5B4 0x5B5	TS12_SM-PL4_NSL	0x0000	Time stamp Unit 12 Input Sample Time (4th) in Nanoseconds Low-Word Register [15:0]
0x5B6 – 0x5B7	0x5B6 0x5B7	TS12_SM-PL4_NSH	0x0000	Time stamp Unit 12 Input Sample Time (4th) in Nanoseconds High-Word Register [29:16]
0x5B8 – 0x5B9	0x5B8 0x5B9	TS12_SM-PL4_SL	0x0000	Time stamp Unit 12 Input Sample Time (4th) in Seconds Low-Word Register [15:0]
0x5BA – 0x5BB	0x5BA 0x5BB	TS12_SM-PL4_SH	0x0000	Time stamp Unit 12 Input Sample Time (4th) in Seconds High-Word Register [31:16]
0x5BC – 0x5BD	0x5BC 0x5BD	TS12_SMPL4_-SUB_NS	0x0000	Time stamp Unit 12 Input Sample Time (4th) in Sub-Nanoseconds Register [2:0]
0x5BE – 0x5C3	0x5BE 0x5C3	Reserved (6-Bytes)	Don't Care	None
0x5C4 – 0x5C5	0x5C4 0x5C5	TS12_SM-PL5_NSL	0x0000	Time stamp Unit 12 Input Sample Time (5th) in Nanoseconds Low-Word Register [15:0]
0x5C6 – 0x5C7	0x5C6 0x5C7	TS12_SM-PL5_NSH	0x0000	Time stamp Unit 12 Input Sample Time (5th) in Nanoseconds High-Word Register [29:16]
0x5C8 – 0x5C9	0x5C8 0x5C9	TS12_SM-PL5_SL	0x0000	Time stamp Unit 12 Input Sample Time (5th) in Seconds Low-Word Register [15:0]
0x5CA – 0x5CB	0x5CA 0x5CB	TS12_SM-PL5_SH	0x0000	Time stamp Unit 12 Input Sample Time (5th) in Seconds High-Word Register [31:16]
0x5CC – 0x5CD	0x5CC 0x5CD	TS12_SMPL5_-SUB_NS	0x0000	Time stamp Unit 12 Input Sample Time (5th) in Sub-Nanoseconds Register [2:0]
0x5CE – 0x5D3	0x5CE 0x5D3	Reserved (6-Bytes)	Don't Care	None
0x5D4 – 0x5D5	0x5D4 0x5D5	TS12_SM-PL6_NSL	0x0000	Time stamp Unit 12 Input Sample Time (6th) in Nanoseconds Low-Word Register [15:0]

TABLE 4-5: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TIME STAMP INPUTS (12 UNITS, 0X400 – 0X5FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x5D6 – 0x5D7	0x5D6 0x5D7	TS12_SM-PL6_NSH	0x0000	Time stamp Unit 12 Input Sample Time (6th) in Nanoseconds High-Word Register [29:16]
0x5D8 – 0x5D9	0x5D8 0x5D9	TS12_SM-PL6_SL	0x0000	Time stamp Unit 12 Input Sample Time (6th) in Seconds Low-Word Register [15:0]
0x5DA – 0x5DB	0x5DA 0x5DB	TS12_SM-PL6_SH	0x0000	Time stamp Unit 12 Input Sample Time (6th) in Seconds High-Word Register [31:16]
0x5DC – 0x5DD	0x5DC 0x5DD	TS12_SMPL6_-SUB_NS	0x0000	Time stamp Unit 12 Input Sample Time (6th) in Sub-Nanoseconds Register [2:0]
0x5DE – 0x5E3	0x5DE 0x5E3	Reserved (6-Bytes)	Don’t care	None
0x5E4 – 0x5E5	0x5E4 0x5E5	TS12_SM-PL7_NSL	0x0000	Time stamp Unit 12 Input Sample Time (7th) in Nanoseconds Low-Word Register [15:0]
0x5E6 – 0x5E7	0x5E6 0x5E7	TS12_SM-PL7_NSH	0x0000	Time stamp Unit 12 Input Sample Time (7th) in Nanoseconds High-Word Register [29:16]
0x5E8 – 0x5E9	0x5E8 0x5E9	TS12_SM-PL7_SL	0x0000	Time stamp Unit 12 Input Sample Time (7th) in Seconds Low-Word Register [15:0]
0x5EA – 0x5EB	0x5EA 0x5EB	TS12_SM-PL7_SH	0x0000	Time stamp Unit 12 Input Sample Time (7th) in Seconds High-Word Register [31:16]
0x5EC – 0x5ED	0x5EC 0x5ED	TS12_SMPL7_-SUB_NS	0x0000	Time stamp Unit 12 Input Sample Time (7th) in Sub-Nanoseconds Register [2:0]
0x5EE – 0x5F3	0x5EE 0x5F3	Reserved (6-Bytes)	Don’t Care	None
0x5F4 – 0x5F5	0x5F4 0x5F5	TS12_SM-PL8_NSL	0x0000	Time stamp Unit 12 Input Sample Time (8th) in Nanoseconds Low-Word Register [15:0]
0x5F6 – 0x5F7	0x5F6 0x5F7	TS12_SM-PL8_NSH	0x0000	Time stamp Unit 12 Input Sample Time (8th) in Nanoseconds High-Word Register [29:16]
0x5F8 – 0x5F9	0x5F8 0x5F9	TS12_SM-PL8_SL	0x0000	Time stamp Unit 12 Input Sample Time (8th) in Seconds Low-Word Register [15:0]
0x5FA – 0x5FB	0x5FA 0x5FB	TS12_SM-PL8_SH	0x0000	Time stamp Unit 12 Input Sample Time (8th) in Seconds High-Word Register [31:16]
0x5FC – 0x5FD	0x5FC 0x5FD	TS12_SMPL8_-SUB_NS	0x0000	Time stamp Unit 12 Input Sample Time (8th) in Sub-Nanoseconds Register [2:0]
0x5FE – 0x5FF	0x5FE 0x5FF	Reserved (2-Bytes)	Don’t Care	None

TABLE 4-6: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP 1588 CLOCK AND GLOBAL CONTROL (0X600 – 0X7FF)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x600 – 0x601	0x600 0x601	PTP_CLK_CTL	0x0002	PTP Clock Control Register [6:0]
0x602 – 0x603	0x602 0x603	Reserved (2-Bytes)	Don't care	None
0x604 – 0x605	0x604 0x605	PTP_RTC_NSL	0x0000	PTP Real Time Clock in Nanoseconds Low-Word Register [15:0]
0x606 – 0x607	0x606 0x607	PTP_RTC_NSH	0x0000	PTP Real Time Clock in Nanoseconds High-Word Register [31:16]
0x608 – 0x609	0x608 0x609	PTP_RTC_SL	0x0000	PTP Real Time Clock in Seconds Low-Word Register [15:0]
0x60A – 0x60B	0x60A 0x60B	PTP_RTC_SH	0x0000	PTP Real Time Clock in Seconds High-Word Register [31:16]
0x60C – 0x60D	0x60C 0x60D	PTP_RT-C_PHASE	0x0000	PTP Real Time Clock in Phase Register [2:0]
0x60E – 0x60F	0x60E 0x60F	Reserved (2-Bytes)	Don't Care	None
0x610 – 0x611	0x610 0x611	PTP_SNS_RAT-E_L	0x0000	PTP Sub-nanosecond Rate Low-Word Register [15:0]
0x612 – 0x613	0x612 0x613	PTP_SNS_RAT-E_H	0x0000	PTP Sub-nanosecond Rate High-Word [29:16] and Configuration Register
0x614 – 0x615	0x614 0x615	PTP_TEMP_-ADJ_DURA_L	0x0000	PTP Temporary Adjustment Mode Duration Low-Word Register [15:0]
0x616 – 0x617	0x616 0x617	PTP_TEMP_-ADJ_DURA_H	0x0000	PTP Temporary Adjustment Mode Duration High-Word Register [31:16]
0x618 – 0x61F	0x618 0x61F	Reserved (8-Bytes)	Don't Care	None
0x620 – 0x621	0x620 0x621	PTP_MSG_CF-G_1	0x0059	PTP Message Configuration 1 Register [7:0]
0x622 – 0x623	0x622 0x623	PTP_MSG_CF-G_2	0x0404	PTP Message Configuration 2 Register [10:0]
0x624 – 0x625	0x624 0x625	PTP_DO-MAIN_VER	0x0200	PTP Domain and Version Register [11:0]
0x626 – 0x63F	0x626 0x63F	Reserved (26-Bytes)	Don't Care	None
0x640 – 0x641	0x640 0x641	PTP_P1_RX_ LATENCY	0x019F	PTP Port 1 Receive Latency Register [15:0]
0x642 – 0x643	0x642 0x643	PTP_P1_TX_ LATENCY	0x002D	PTP Port 1 Transmit Latency Register [15:0]
0x644 – 0x645	0x644 0x645	PTP_P1_ASYM _COR	0x0000	PTP Port 1 Asymmetry Correction Register [15:0]
0x646 – 0x647	0x646 0x647	PTP_P1_LINK_ DLY	0x0000	PTP Port 1 Link Delay Register [15:0]
0x648 – 0x649	0x648 0x649	P1_XD-LY_REQ_TSL	0x0000	PTP Port 1 Egress Time stamp Low-Word for Pdelay_REQ and Delay_REQ Frames Register [15:0]

TABLE 4-6: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP 1588 CLOCK AND GLOBAL CONTROL (0X600 – 0X7FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x64A – 0x64B	0x64A 0x64B	P1_XD-LY_REQ_TSH	0x0000	PTP Port 1 Egress Time stamp High-Word for Pdelay_REQ and Delay_REQ Frames Register [31:16]
0x64C – 0x64D	0x64C 0x64D	P1_SYNC_TSL	0x0000	PTP Port 1 Egress Time stamp Low-Word for SYNC Frame Register [15:0]
0x64E – 0x64F	0x64E 0x64F	P1_SYNC_TSH	0x0000	PTP Port 1 Egress Time stamp High-Word for SYNC Frame Register [31:16]
0x650 – 0x651	0x650 0x651	P1_PDLY_RE-SP_TSL	0x0000	PTP Port 1 Egress Time stamp Low-Word for Pdelay_resp Frame Register [15:0]
0x652 – 0x653	0x652 0x653	P1_PDLY_RE-SP_TSH	0x0000	PTP Port 1 Egress Time stamp High-Word for Pdelay_resp Frame Register [31:16]
0x654 – 0x65F	0x654 0x65F	Reserved (12-Bytes)	Don't Care	None
0x660 – 0x661	0x660 0x661	PTP_P2_RX-_LATENCY	0x019F	PTP Port 2 Receive Latency Register [15:0]
0x662 – 0x663	0x662 0x663	PTP_P2_TX_LATENCY	0x002D	PTP Port 2 Transmit Latency Register [15:0]
0x664 – 0x665	0x664 0x665	PTP_P2_ASYM_COR	0x0000	PTP Port 2 Asymmetry Correction Register [15:0]
0x666 – 0x667	0x666 0x667	PTP_P2_LINK_DLY	0x0000	PTP Port 2 Link Delay Register [15:0]
0x668 – 0x669	0x668 0x669	P2_XD-LY_REQ_TSL	0x0000	PTP Port 2 Egress Time stamp Low-Word for Pdelay_REQ and Delay_REQ Frames Register [15:0]
0x66A – 0x66B	0x66A 0x66B	P2_XD-LY_REQ_TSH	0x0000	PTP Port 2 Egress Time stamp High-Word for Pdelay_REQ and Delay_REQ Frames Register [31:16]
0x66C – 0x66D	0x66C 0x66D	P2_SYNC_TSL	0x0000	PTP Port 2 Egress Time stamp Low-Word for SYNC Frame Register [15:0]
0x66E – 0x66F	0x66E 0x66F	P2_SYNC_TSH	0x0000	PTP Port 2 Egress Time stamp High-Word for SYNC Frame Register [31:16]
0x670 – 0x671	0x670 0x671	P2_PDLY_RE-SP_TSL	0x0000	PTP Port 2 Egress Time stamp Low-Word for Pdelay_resp Frame Register [15:0]
0x672 – 0x673	0x672 0x673	P2_PDLY_RE-SP_TSH	0x0000	PTP Port 2 Egress Time stamp High-Word for Pdelay_resp Frame Register [31:16]
0x674 – 0x67F	0x674 0x67F	Reserved (12-Bytes)	Don't Care	None
0x680 – 0x681	0x680 0x681	GPIO_MONI-TOR	0x0000	PTP GPIO Monitor Register [11:0]
0x682 – 0x683	0x682 0x683	GPIO_OEN	0x0000	PTP GPIO Output Enable Register [11:0]
0x684 – 0x687	0x684 0x687	Reserved (4-Bytes)	Don't Care	None
0x688 – 0x689	0x688 0x689	PTP_TRIG_IS	0x0000	PTP Trigger Unit Interrupt Status Register
0x68A – 0x68B	0x68A 0x68B	PTP_TRIG_IE	0x0000	PTP Trigger Unit Interrupt Enable Register

TABLE 4-6: INTERNAL I/O REGISTER SPACE MAPPING FOR PTP 1588 CLOCK AND GLOBAL CONTROL (0X600 – 0X7FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x68C – 0x68D	0x68C 0x68D	PTP_TS_IS	0x0000	PTP Time stamp Unit Interrupt Status Register
0x68E – 0x68F	0x68E 0x68F	PTP_TS_IE	0x0000	PTP Time stamp Unit Interrupt Enable Register
0x690 – 0x733	0x690 0x733	Reserved (164-Bytes)	Don't Care	None
0x734 – 0x735	0x734 0x735	DSP_CNTRL_6	0x3020	DSP Control 1 Register
0x736 – 0x747	0x736 0x747	Reserved (18-Bytes)	Don't Care	None
0x748 – 0x749	0x748 0x749	ANA_CNTRL_1	0x0000	Analog Control 1 Register
0x74A – 0x74B	0x74A 0x74B	Reserved (2-Bytes)	Don't Care	None
0x74C – 0x74D	0x74C 0x74D	ANA_CNTRL_3	0x0000	Analog Control 3 Register
0x74E – 0x7FF	0x74E 0x7FF	Reserved (178-Bytes)	Don't Care	None

4.2 Register Bit Definitions

The section provides details of the bit definitions for the registers summarized in the previous section. Writing to a bit or register defined as reserved could cause unpredictable results. If it is necessary to write to registers that contain both writable and reserved bits in the same register, the user should first read back the reserved bits (RO or RW), then "OR" the desired settable bits with the value read and write back the "ORed" value back to the register.

Bit Type Definition:

- RO = Read only.
- WO = Write only.
- RW = Read/Write.
- SC = Self-Clear.
- W1C = Write "1" to Clear (Write a "1" to clear this bit).

4.2.1 INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 – 0X0FF)

4.2.1.1 Chip ID and Enable Register (0x000 – 0x001): CIDER

This register contains the chip ID and switch-enable control.

TABLE 4-7: CHIP ID AND ENABLE REGISTER (0X000 – 0X001): CIDER

Bit	Default	R/W	Description
15 – 8	0x84	RO	**Family ID** Chip family ID.
7 – 4	0x4 or 0x5	RO	**Chip ID** 0x4 is assigned to KSZ8463ML/FML. 0x5 is assigned to KSZ8463RL/FRL.
3 – 1	001	RO	**Revision ID** Chip revision ID.

TABLE 4-7: CHIP ID AND ENABLE REGISTER (0X000 – 0X001): CIDER (CONTINUED)

Bit	Default	R/W	Description
0	1	RW	**Start Switch** 1 = Start the chip. 0 = Switch is disabled.

4.2.1.2 Switch Global Control Register 1 (0x002 – 0x003): SGCR1

This register contains global control bits for the switch function.

TABLE 4-8: SWITCH GLOBAL CONTROL REGISTER 1 (0X002 – 0X003): SGCR1

Bit	Default	R/W	Description
15	0	RW	**Pass All Frames** 1 = Switch all packets including bad ones. Used solely for debugging purposes. Works in conjunction with sniffer mode only. 0 = Do not pass bad frames.
14	0	RW	**Receive 2000 Byte Packet Length Enable** 1 = Enables the receipt of packets up to and including 2000 bytes in length. 0 = Discards the received packets if their length is greater than 2000 bytes.
13	1	RW	**IEEE 802.3x Transmit Direction Flow Control Enable** 1 = Enables transmit direction flow control feature. 0 = Disable transmit direction flow control feature. The switch will not generate any flow control packets.
12	1	RW	**IEEE 802.3x Receive Direction Flow Control Enable** 1 = Enables receive direction flow control feature. 0 = Disable receive direction flow control feature. The switch will not react to any received flow control packets.
11	0	RW	**Frame Length Field Check** 1 = Enable checking frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped (for Length/Type field < 1500). 0 = Disable checking frame length field in the IEEE packets.
10	1	RW	**Aging Enable** 1 = Enable aging function in the chip. 0 = Disable aging function in the chip.
9	0	RW	**Fast Age Enable** 1 = Turn on fast age (800 µs).
8	0	RW	**Aggressive Back-Off Enable** 1 = Enable more aggressive back-off algorithm in half-duplex mode to enhance performance. This is not an IEEE standard.
7 – 6	01	RW	Reserved
5	0	RW	**Enable Flow Control when Exceeding Ingress Limit** 1 = Flow control frame will be sent to link partner when exceeding the ingress rate limit. 0 = Frame will be dropped when exceeding the ingress rate limit.
4	1	RW	**Receive 2K Byte Packets Enable** 1 = Enable packet length up to 2K bytes. While set, SGCR2 bits[2,1] will have no effect. 0 = Discard packet if packet length is greater than 2000 bytes.
3	0	RW	**Pass Flow Control Packet** 1 = Switch will not filter 802.3x “flow control” packets.
2 – 1	00	RW	Reserved

TABLE 4-8: SWITCH GLOBAL CONTROL REGISTER 1 (0X002 – 0X003): SGCR1 (CONTINUED)

Bit	Default	R/W	Description
0	0	RW	**Link Change Age** 1 = Link change from “link” to “no link” will cause fast aging (<800 µs) to age address table faster. After an age cycle is complete, the age logic will return to normal (300 ±75 seconds). This affects ports not linked and not active linked ports. **Note:** If any port is unplugged, all addresses will be automatically aged out.

4.2.1.3 Switch Global Control Register 2 (0x004 – 0x005): SGCR2

This register contains global control bits for the switch function.

TABLE 4-9: SWITCH GLOBAL CONTROL REGISTER 2 (0X004 – 0X005): SGCR2

Bit	Default	R/W	Description
15	0	RW	**802.1Q VLAN Enable** 1 = 802.1Q VLAN mode is turned on. VLAN table must be set up before the operation. 0 = 802.1Q VLAN is disabled.
14	0	RW	**IGMP Snoop Enable** 1 = IGMP snoop is enabled. 0 = IGMP snoop is disabled.
13	0	RW	**IPv6 MLD Snooping Enable** 1 = Enable IPv6 MLD snooping.
12	0	RW	**IPv6 MLD Snooping Option Select** 1 = Enable IPv6 MLD snooping option.
11 – 9	000	RW	Reserved
8	0	RW	**Sniff Mode Select** 1 = Performs RX and TX sniff (both the source port and destination port need to match). 0 = Performs RX or TX sniff (either the source port or destination port needs to match). This is the mode used to implement RX only sniff.
7	1	RW	**Unicast Port-VLAN Mismatch Discard** 1 = No packets can cross the VLAN boundary. 0 = Unicast packets (excluding unknown/multicast/broadcast) can cross the VLAN boundary.
6	1	RW	**Multicast Storm Protection Disable** 1 = “Broadcast Storm Protection” does not include multicast packets. Only DA = FF-FF-FF-FF-FF-FF packets are regulated. 0 = “Broadcast Storm Protection” includes DA = FF-FF-FF-FF-FF-FF and DA[40] = “1” packets.
5	1	RW	**Back Pressure Mode** 1 = Carrier sense-based back pressure is selected. 0 = Collision-based back pressure is selected.
4	1	RW	**Flow Control and Back Pressure Fair Mode** 1 = Fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This prevents the flow control port from being flow controlled for an extended period of time. 0 = In this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port is flow controlled. This may not be “fair” to the flow control port.
3	0	RW	**No Excessive Collision Drop** 1 = The switch does not drop packets when 16 or more collisions occur. 0 = The switch drops packets when 16 or more collisions occur.

TABLE 4-9: SWITCH GLOBAL CONTROL REGISTER 2 (0X004 – 0X005): SGCR2 (CONTINUED)

Bit	Default	R/W	Description
2	0	RW	**Huge Packet Support** 1 = Accepts packet sizes up to 1916 bytes (inclusive). This bit setting overrides setting from bit [1] of the same register. 0 = The max packet size is determined by bit [1] of this register.
1	0	RW	**Legal Maximum Packet Size Check Enable** 1 = 1522 bytes for tagged packets, 1518 bytes for untagged packets. Any packets larger than the specified value are dropped. 0 = Accepts packet sizes up to 1536 bytes (inclusive).
0	0	RW	**Priority Buffer Reserve** 1 = Each port is pre-allocated 48 buffers, used exclusively for high priority (q3, q2, and q1) packets. Effective only when the multiple queue feature is turned on. 0 = Each port is pre-allocated 48 buffers used for all priority packets (q3, q2, q1, and q0).

4.2.1.4 Switch Global Control Register 3 (0x006 – 0x007): SGCR3

This register contains global control bits for the switch function.

TABLE 4-10: SWITCH GLOBAL CONTROL REGISTER 3 (0X006 – 0X007): SGCR3

Bit	Default	R/W	Description
15 – 8	0x63	RW	**Broadcast Storm Protection Rate Bits[7:0]** These bits, along with SGCR3[2:0], determine how many 64-byte blocks of packet data are allowed on an input port in a preset period. The period is 67 ms for 100BASE-TX or 670 ms for 10BASE-T. The default is 1%.
7	0	RO	Reserved
6	0	RW	**Switch Host Port in Half-Duplex Mode** 1 = Enable host port interface half-duplex mode. 0 = Enable host port interface full-duplex mode.
5	1	RW	**Switch Host Port Flow Control Enable** 1 = Enable full-duplex flow control on switch host port. 0 = Disable full-duplex flow control on switch host port
4	0	RW	**Switch MII 10BASE-T** 1 = The switch is in 10 Mbps mode. 0 = The switch is in 100 Mbps mode.
3	0	RW	**Null VID Replacement** 1 = Replaces NULL VID with port VID (12 bits). 0 = No replacement for NULL VID.
2 – 0	000	RW	**Broadcast Storm Protection Rate Bits[10:8]** These bits, along with SGCR3[15:8] determine how many 64-byte blocks of packet data are allowed on an input port in a preset period. The period is 67 ms for 100BASE-TX or 670 ms for 10BASE-T. The default is 1%. Broadcast storm protection rate: 148,800 frames/sec * 67 ms/interval * 1% = 99 frames/interval (approx. 0x63)

4.2.1.5 0x008 – 0x00B: Reserved

4.2.1.6 Switch Global Control Register 6 (0x00C – 0x00D): SGCR6

This register contains global control bits for the switch function.

TABLE 4-11: SWITCH GLOBAL CONTROL REGISTER 6 (0X00C – 0X00D): SGCR6

Bit	Default	R/W	Description
15 – 14	11	RW	**Tag_0x7** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x7.
13 – 12	11	RW	**Tag_0x6** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x6.
11 – 10	10	RW	**Tag_0x5** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x5.
9 – 8	10	RW	**Tag_0x4** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x4.
7 – 6	01	RW	**Tag_0x3** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x3.
5 – 4	01	RW	**Tag_0x2** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x2.
3 – 2	00	RW	**Tag_0x1** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x1.
1 – 0	00	RW	**Tag_0x0** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x0.

4.2.1.7 Switch Global Control Register 7 (0x00E – 0x00F): SGCR7

This register contains global control bits for the switch function.

TABLE 4-12: SWITCH GLOBAL CONTROL REGISTER 7 (0X00E – 0X00F): SGCR7

<table>
<tr><th>Bit</th><th>Default</th><th>R/W</th><th colspan="3">Description</th></tr>
<tr><td>15 – 10</td><td>0x02</td><td>RW</td><td colspan="3">Reserved</td></tr>
<tr><td rowspan="6">9 – 8</td><td rowspan="6">00</td><td rowspan="6">RW</td><td colspan="3">Port LED Mode
When read, these two bits provide the current setting of the LED display mode for P1/2LED1 and P1/2LED0 as defined as below. Reg. 0x06C – 0x06D, bits [14:12] determine if this automatic functionality is utilized or if the port 1 LEDs are controlled by the local processor. Reg. 0x084 – 0x085, bits [14:12] determine if this automatic functionality is utilized or if the port 2 LEDs are controlled by the local processor.</td></tr>
<tr><td>LED Mode</td><td>P1/2LED1</td><td>P1/2LED0</td></tr>
<tr><td>00</td><td>Speed</td><td>Link and Activity</td></tr>
<tr><td>01</td><td>Activity</td><td>Link</td></tr>
<tr><td>10</td><td>Full-Duplex</td><td>Link and Activity</td></tr>
<tr><td>11</td><td>Full-Duplex</td><td>Link</td></tr>
<tr><td>7</td><td>0</td><td>RW</td><td colspan="3">Unknown Default Port Enable
Send packets with unknown destination address to specified ports in bits [2:0].
1 = Enable to send unknown DA packet</td></tr>
</table>

TABLE 4-12: SWITCH GLOBAL CONTROL REGISTER 7 (0X00E – 0X00F): SGCR7 (CONTINUED)

Bit	Default	R/W	Description
6 – 5	01 or 10	RW	**Driver Strength Selection** These two bits determine the drive strength of all I/O pins except for the following category of pins: LED pins, GPIO pins, INTRN, RSTN, and RXD3/REFCLK_0. 00 = 4 mA 01 = 8 mA. (Default when VDD_IO is 3.3V or 2.5V) 10 = 12 mA. (Default when VDD_IO is 1.8V) 11 = 16 mA.
4 – 3	00	RW	Reserved
2 – 0	111	RW	**Unknown Packet Default Port(s)** Specifies which ports to send packets with unknown destination addresses. This applies to both unicast and multicast addresses that are unknown. Feature is enabled by bit[7]. Bit[2] = For Port 3 (MII/RMII Port) Bit[1] = For Port 2 Bit[0] = For Port 1

4.2.2 MAC ADDRESS REGISTERS

4.2.2.1 MAC Address Register 1 (0x010 – 0x011): MACAR1

This register contains the two MSBs of the MAC address for the switch function. This MAC address is used for sending PAUSE frames.

TABLE 4-13: MAC ADDRESS REGISTER 1 (0X010 – 0X011): MACAR1

Bit	Default	R/W	Description
15 – 0	0x0010	RW	**MACA[47:32]** Specifies MAC Address 1 for sending PAUSE frame.

4.2.2.2 MAC Address Register 2 (0x012 – 0x013): MACAR2

This register contains the MAC address for the switch function. This MAC address is used for sending PAUSE frames.

TABLE 4-14: MAC ADDRESS REGISTER 2 (0X012 – 0X013): MACAR2

Bit	Default	R/W	Description
15 – 0	0xA1FF	RW	**MACA[31:16]** Specifies MAC Address 2 for sending PAUSE frame.

4.2.2.3 MAC Address Register 3 (0x014 – 0x015): MACAR3

This register contains the two LSBs of the MAC address for the switch function. This MAC address is used for sending PAUSE frames.

TABLE 4-15: MAC ADDRESS REGISTER 3 (0X014 – 0X015): MACAR3

Bit	Default	R/W	Description
15 – 0	0xFFFF	RW	**MACA[15:0]** Specifies MAC Address 3 for sending PAUSE frame.

4.2.3 TOS PRIORITY CONTROL REGISTERS

4.2.3.1 TOS Priority Control Register 1 (0x016 – 0x017): TOSR1

The IPv4/IPv6 type-of-service (TOS) priority control registers are used to define a 2-bit priority to each of the 64 possible values in the 6-bit differentiated services code point (DSCP) field in the IP header of ingress frames.

This register contains the TOS priority control bits for the switch function.

TABLE 4-16: TOS PRIORITY CONTROL REGISTER 1 (0X016 – 0X017): TOSR1

Bit	Default	R/W	Description
15 – 14	00	RW	**DSCP[15:14]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x1c.
13 – 12	00	RW	**DSCP[13:12]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x18.
11 – 10	00	RW	**DSCP[11:10]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x14.
9 – 8	00	RW	**DSCP[9:8]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x10.
7 – 6	00	RW	**DSCP[7:6]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x0c.
5 – 4	00	RW	**DSCP[5:4]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x08.
3 – 2	00	RW	**DSCP[3:2]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x04.
1 – 0	00	RW	**DSCP[1:0]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x00.

4.2.3.2 TOS Priority Control Register 2 (0x018 – 0x019): TOSR2

This register contains the TOS priority control bits for the switch function.

TABLE 4-17: TOS PRIORITY CONTROL REGISTER 2 (0X018 – 0X019): TOSR2

Bit	Default	R/W	Description
15 – 14	00	RW	**DSCP[31:30]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x3c.
13 – 12	00	RW	**DSCP[29:28]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x38.
11 – 10	00	RW	**DSCP[27:26]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x34.
9 – 8	00	RW	**DSCP[25:24]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x30.
7 – 6	00	RW	**DSCP[23:22]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x2c.
5 – 4	00	RW	**DSCP[21:20]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x28.
3 – 2	00	RW	**DSCP[19:18]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x24.

TABLE 4-17: TOS PRIORITY CONTROL REGISTER 2 (0X018 – 0X019): TOSR2 (CONTINUED)

Bit	Default	R/W	Description
1 – 0	00	RW	**DSCP[17:16]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x20.

4.2.3.3 TOS Priority Control Register 3 (0x01A – 0x01B): TOSR3

This register contains the TOS priority control bits for the switch function.

TABLE 4-18: TOS PRIORITY CONTROL REGISTER 3 (0X01A – 0X01B): TOSR3

Bit	Default	R/W	Description
15 – 14	00	RW	**DSCP[47:46]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x5c.
13 – 12	00	RW	**DSCP[45:44]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x58.
11 – 10	00	RW	**DSCP[43:42]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x54.
9 – 8	00	RW	**DSCP[41:40]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x50.
7 – 6	00	RW	**DSCP[39:38]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x4c.
5 – 4	00	RW	**DSCP[37:36]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x48.
3 – 2	00	RW	**DSCP[35:34]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x44.
1 – 0	00	RW	**DSCP[33:32]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x40.

4.2.3.4 TOS Priority Control Register 4 (0x01C – 0x1D): TOSR4

This register contains the TOS priority control bits for the switch function.

TABLE 4-19: TOS PRIORITY CONTROL REGISTER 4 (0X01C – 0X1D): TOSR4

Bit	Default	R/W	Description
15 – 14	00	RW	**DSCP[63:62]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x7c.
13 – 12	00	RW	**DSCP[61:60]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x78.
11 – 10	00	RW	**DSCP[59:58]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x74.
9 – 8	00	RW	**DSCP[57:56]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x70.

TABLE 4-19: TOS PRIORITY CONTROL REGISTER 4 (0X01C – 0X1D): TOSR4 (CONTINUED)

Bit	Default	R/W	Description
7 – 6	00	RW	**DSCP[55:54]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x6c.
5 – 4	00	RW	**DSCP[53:52]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x68.
3 – 2	00	RW	**DSCP[51:50]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x64.
1 – 0	00	RW	**DSCP[49:48]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x60.

4.2.3.5 TOS Priority Control Register 5 (0x01E – 0x1F): TOSR5

This register contains the TOS priority control bits for the switch function.

TABLE 4-20: TOS PRIORITY CONTROL REGISTER 5 (0X01E – 0X1F): TOSR5

Bit	Default	R/W	Description
15 – 14	00	RW	**DSCP[79:78]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x9c.
13 – 12	00	RW	**DSCP[77:76]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x98.
11 – 10	00	RW	**DSCP[75:74]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x94.
9 – 8	00	RW	**DSCP[73:72]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x90.
7 – 6	00	RW	**DSCP[71:70]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x8c.
5 – 4	00	RW	**DSCP[69:68]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x88.
3 – 2	00	RW	**DSCP[67:66]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x84.
1 – 0	00	RW	**DSCP[65:64]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x80.

4.2.3.6 TOS Priority Control Register 6 (0x020 – 0x021): TOSR6

This register contains the TOS priority control bits for the switch function.

TABLE 4-21: TOS PRIORITY CONTROL REGISTER 6 (0X020 – 0X021): TOSR6

Bit	Default	R/W	Description
15 – 14	00	RW	**DSCP[95:94]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xbc.

TABLE 4-21: TOS PRIORITY CONTROL REGISTER 6 (0X020 – 0X021): TOSR6 (CONTINUED)

Bit	Default	R/W	Description
13 – 12	00	RW	**DSCP[93:92]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xb8.
11 – 10	00	RW	**DSCP[91:90]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xb4.
9 – 8	00	RW	**DSCP[89:88]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xb0.
7 – 6	00	RW	**DSCP[87:86]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xac.
5 – 4	00	RW	**DSCP[85:84]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xa8.
3 – 2	00	RW	**DSCP[83:82]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xa4.
1 – 0	00	RW	**DSCP[81:80]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xa0.

4.2.3.7 TOS Priority Control Register 7 (0x022 – 0x023): TOSR7

This register contains the TOS priority control bits for the switch function.

TABLE 4-22: TOS PRIORITY CONTROL REGISTER 7 (0X022 – 0X023): TOSR7

Bit	Default	R/W	Description
15 – 14	00	RW	**DSCP[111:110]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xdc.
13 – 12	00	RW	**DSCP[109:108]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xd8.
11 – 10	00	RW	**DSCP[107:106]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xd4.
9 – 8	00	RW	**DSCP[105:104]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xd0.
7 – 6	00	RW	**DSCP[103:102]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xcc.
5 – 4	00	RW	**DSCP[101:100]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xc8.
3 – 2	00	RW	**DSCP[99:98]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xc4.
1 – 0	00	RW	**DSCP[97:96]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xc0.

4.2.3.8 TOS Priority Control Register 8 (0x024 – 0x025): TOSR8

This register contains the TOS priority control bits for the switch function.

TABLE 4-23: TOS PRIORITY CONTROL REGISTER 8 (0X024 – 0X025): TOSR8

Bit	Default	R/W	Description
15 – 14	00	RW	**DSCP[127:126]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xfc
13 – 12	00	RW	**DSCP[125:124]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xf8.
11 – 10	00	RW	**DSCP[123:122]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xf4.
9 – 8	00	RW	**DSCP[121:120]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xf0.
7 – 6	00	RW	**DSCP[119:118]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xec.
5 – 4	00	RW	**DSCP[117:116]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xe8.
3 – 2	00	RW	**DSCP[115:114]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xe4.
1 – 0	00	RW	**DSCP[113:112]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xe0.

4.2.4 INDIRECT ACCESS DATA REGISTERS

4.2.4.1 Indirect Access Data Register 1 (0x026 – 0x027): IADR1

This register is used to indirectly read or write the data in the Management Information Base (MIB) Counters, Static MAC Address Table, Dynamic MAC Address Table, or the VLAN Table. Review those sections for detail bit information.

TABLE 4-24: INDIRECT ACCESS DATA REGISTER 1 (0X026 – 0X027): IADR1

Bit	Default	R/W	Description
15 – 8	0x00	RO	Reserved
7	0	RO	**CPU Read Status** Only for dynamic and statistics counter reads. 1 = Read is still in progress. 0 = Read has completed.
6 – 3	0x0	RO	Reserved
2 – 0	000	RO	**Indirect Data [66:64]** Bit[66:64] of indirect data.

4.2.4.2 Indirect Access Data Register 2 (0x028 – 0x029): IADR2

This register is used to indirectly read or write the data in the Management Information Base (MIB) Counters, Static MAC Address Table, Dynamic MAC Address Table, or the VLAN Table. Review those sections for detail bit information.

TABLE 4-25: INDIRECT ACCESS DATA REGISTER 2 (0X028 – 0X029): IADR2

Bit	Default	R/W	Description
15 – 0	0x0000	RW	**Indirect Data [47:32]** Bit[47:32] of indirect data.

4.2.4.3 Indirect Access Data Register 3 (0x02A – 0x02B): IADR3

This register is used to indirectly read or write the data in the Management Information Base (MIB) Counters, Static MAC Address Table, Dynamic MAC Address Table, or the VLAN Table. Review those sections for detail bit information.

TABLE 4-26: INDIRECT ACCESS DATA REGISTER 3 (0X02A – 0X02B): IADR3

Bit	Default	R/W	Description
15 – 0	0x0000	RW	**Indirect Data [63:48]** Bit[63:48] of indirect data.

4.2.4.4 Indirect Access Data Register 4 (0x02C – 0x02D): IADR4

This register is used to indirectly read or write the data in the Management Information Base (MIB) Counters, Static MAC Address Table, Dynamic MAC Address Table, or the VLAN Table. Review those sections for detail bit information.

TABLE 4-27: INDIRECT ACCESS DATA REGISTER 4 (0X02C – 0X02D): IADR4

Bit	Default	R/W	Description
15 – 0	0x0000	RW	**Indirect Data [15:0]** Bit[15:0] of indirect data.

4.2.4.5 Indirect Access Data Register 5 (0x02E – 0x02F): IADR5

This register is used to indirectly read or write the data in the Management Information Base (MIB) Counters, Static MAC Address Table, Dynamic MAC Address Table, or the VLAN Table. Review those sections for detail bit information.

TABLE 4-28: INDIRECT ACCESS DATA REGISTER 5 (0X02E – 0X02F): IADR5

Bit	Default	R/W	Description
15 – 0	0x0000	RW	**Indirect Data [31:16]** Bit[31:16] of indirect data.

4.2.4.6 Indirect Access Control Register (0x030 – 0x031): IACR

This register is used to indirectly read or write the data in the Management Information Base (MIB) Counters, Static MAC Address Table, Dynamic MAC Address Table, or the VLAN Table. Review those sections for detail bit information. Writing to IACR triggers a command. Read or write access is determined by Register bit 12.

TABLE 4-29: INDIRECT ACCESS CONTROL REGISTER (0X030 – 0X031): IACR

Bit	Default	R/W	Description
15 – 13	000	RW	Reserved
12	0	RW	**Read or Write Access Selection** 1 = Read cycle. 0 = Write cycle.
11 – 10	00	RW	**Table Select** 00 = Static MAC address table selected. 01 = VLAN table selected. 10 = Dynamic MAC address table selected. 11 = MIB counter selected.
9 – 0	0x000	RW	**Indirect Address [9:0]** Bit[9:0] of indirect address.

4.2.5 POWER MANAGEMENT CONTROL AND WAKE-UP EVENT STATUS

4.2.5.1 Power Management Control and Wake-Up Event Status (0x032 – 0x033): PMCTRL

This register controls the power management mode and provides wake-up event status.

TABLE 4-30: POWER MANAGEMENT CONTROL AND WAKE-UP EVENT STATUS (0X032 – 0X033): PMCTRL

Bit	Default	R/W	Description
15 – 4	0x000	RO	Reserved.
3	0	RW (W1C)	**Link-Up Detect Status** 1 = A Link Up condition has been detected at either port 1 or port 2 (Write a “1 “to clear). 0 = No Link Up has been detected.
2	0	RW (W1C)	**Energy Detect Status** 1 = Energy is detected at either port 1 or port 2 (Write a “1” to clear). 0 = No energy is detected.
1 – 0	00	RW	**Power Management Mode** These two bits are used to control device power management mode. 00 = Normal Mode. 01 = Energy Detect Mode. 10 = Global Soft Power-Down Mode. 11 = Reserved.

4.2.5.2 (0x034 – 0x035): Reserved

4.2.6 GO SLEEP TIME AND CLOCK TREE POWER-DOWN CONTROL REGISTERS

4.2.6.1 Go Sleep Time Register (0x036 – 0x037): GST

This register contains the value which is used to control the minimum Go-Sleep time period when the device transitions from normal power state to low power state in energy detect mode.

TABLE 4-31: GO SLEEP TIME REGISTER (0X036 – 0X037): GST

Bit	Default	R/W	Description
15 – 8	0x00	RO	Reserved
7 – 0	0x8E	RW	**Go Sleep Time** This value is used to control the minimum period the no energy event has to be detected consecutively before the device enters the low power state during energy-detect mode. The unit is 20 ms. The default go sleep time is around 3.0 seconds.

4.2.6.2 Clock Tree Power-Down Control Register (0x038 – 0x039): CTPDC

This register contains the power-down control bits for all clocks.

TABLE 4-32: CLOCK TREE POWER-DOWN CONTROL REGISTER (0X038 – 0X039): CTPDC

Bit	Default	R/W	Description
15 – 5	0x000	RO	Reserved
4	0	RW	**PLL Auto Power-Down Enable** 1 = When all the following condition are met, the device will automatically shut down the PLL. Any line or host activity will wake up the PLL. • No energy is detected at both port 1 and port 2 in energy-detect mode. • Port 3 is at PHY-MII mode and TX_ER is set at high. 0 = PLL clock is always on.

TABLE 4-32: CLOCK TREE POWER-DOWN CONTROL REGISTER (0X038 – 0X039): CTPDC

Bit	Default	R/W	Description
3	0	RW	**Switch Clock Auto Shut Down Enable** 1 = When no packet transfer is detected on the MII interface of all ports (port 1, port 2, and port 3) longer than the time specified in bit[1:0] of current register, the device will shut down the switch clock automatically. The switch clock will be woken up automatically when the MII interface of any port becomes busy. 0 = Switch clock is always on.
2	0	RW	**CPU Clock Auto Shutdown Enable** 1 = When no packet transfer is detected both on host interface and on MII interface of all ports (port 1, port 2, and port 3) longer than the time specified in bit[1:0] of current register, the device will shut down CPU clock automatically. The CPU clock will be waked up automatically when host activity is detected or MII interface of any port becomes busy. 0 = CPU clock is always on.
1 – 0	00	RW	**Shutdown Wait Period** These two bits specify the time for device to monitor host/MII activity continuously before it could shut down switch or CPU clock. 00 = 5.3s. 01 = 1.6s. 10 = 1 ms. 11 = 3.2 µs.

4.2.6.3 0x03A – 0x04B: Reserved

4.2.7 PHY AND MII BASIC CONTROL REGISTERS

4.2.7.1 PHY 1 and MII Basic Control Register (0x04C – 0x04D): P1MBCR

This register contains media independent interface (MII) control bits for the switch port 1 function as defined in the IEEE 802.3 specification.

TABLE 4-33: PHY 1 AND MII BASIC CONTROL REGISTER (0X04C – 0X04D): P1MBCR

Bit	Default	R/W	Description	Bit is Same As
15	0	RO	Reserved	—
14	0	RW	**Far-End Loopback** 1 = Perform loopback as follows: Start: RXP2/RXM2 (port 2) Loopback: PMD/PMA of port 1's PHY End: TXP2/TXM2 (port 2) 0 = Normal operation.	Bit[8] in P1CR4
13	1	RW	**Force 100BASE-TX** 1 = Force 100 Mbps if auto-negotiation is disabled (bit [12]) 0 = Force 10 Mbps if auto-negotiation is disabled (bit [12])	Bit[6] in P1CR4
12	1	RW	**Auto-Negotiation Enable** 1 = Auto-negotiation enabled. 0 = Auto-negotiation disabled.	Bit[7] in P1CR4
11	0	RW	**Power-Down** 1 = Power-down. 0 = Normal operation.	Bit[11] in P1CR4
10	0	RO	**Isolate** Not supported.	—

TABLE 4-33: PHY 1 AND MII BASIC CONTROL REGISTER (0X04C – 0X04D): P1MBCR

Bit	Default	R/W	Description	Bit is Same As
9	0	RW/SC	**Restart Auto-Negotiation** 1 = Restart auto-negotiation. 0 = Normal operation.	Bit[13] in P1CR4
8	1	RW	**Force Full-Duplex** 1 = Force full-duplex. 0 = Force half-duplex. Applies only when auto-negotiation is disabled (bit [12]). It is always in half duplex if auto-negotiation is enabled but failed.	Bit[5] in P1CR4
7	0	RO	**Collision test** Not supported.	—
6	0	RO	Reserved.	—
5	1	RW	**HP_MDIX** 1 = HP Auto-MDI-X mode. 0 = Microchip Auto-MDI-X mode.	Bit[15] in P1SR
4	0	RW	**Force MDI-X** 1 = Force MDI-X. 0 = Normal operation.	Bit[9] in P1CR4
3	0	RW	**Disable Auto-MDI-X** 1 = Disable Auto-MDI-X. 0 = Normal operation.	Bit[10] in P1CR4
2	0	RW	**Disable Far-End-Fault** 1 = Disable far-end-fault detection. 0 = Normal operation. For 100BASE-FX fiber mode operation.	Bit[12] in P1CR4
1	0	RW	**Disable Transmit** 1 = Disable transmit. 0 = Normal operation.	Bit[14] in P1CR4
0	0	RW	Reserved	—

4.2.7.2 PHY 1 and MII Basic Status Register (0x04E – 0x04F): P1MBSR

This register contains the media independent interface (MII) status bits for the switch port 1 function.

TABLE 4-34: PHY 1 AND MII BASIC STATUS REGISTER (0X04E – 0X04F): P1MBSR

Bit	Default	R/W	Description	Bit is Same As
15	0	RO	**T4 Capable** 1 = 100BASE-T4 capable. 0 = Not 100BASE-T4 capable.	—
14	1	RO	**100BASE-TX Full Capable** 1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable.	—
13	1	RO	**100BASE-TX Half Capable** 1 = 100BASE-TX half-duplex capable. 0 = Not 100BASE-TX half-duplex capable.	—
12	1	RO	**10BASE-T Full Capable** 1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.	—
11	1	RO	**10BASE-T Half Capable** 1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.	—
10 – 7	0x0	RO	Reserved	—

TABLE 4-34: PHY 1 AND MII BASIC STATUS REGISTER (0X04E – 0X04F): P1MBSR (CONTINUED)

Bit	Default	R/W	Description	Bit is Same As
6	0	RO	**Preamble Suppressed** Not supported.	—
5	0	RO	**Auto-Negotiation Complete** 1 = Auto-negotiation complete. 0 = Auto-negotiation not completed.	Bit[6] in P1SR
4	0	RO	**Far-End-Fault** 1 = Far-end-fault detected. 0 = No far-end-fault detected. For 100BASE-FX fiber mode operation.	Bit[8] in P1SR
3	1	RO	**Auto-Negotiation Capable** 1 = Auto-negotiation capable. 0 = Not auto-negotiation capable.	—
2	0	RO	**Link Status** 1 = Link is up. 0 = Link is down.	Bit[5] in P1SR
1	0	RO	**Jabber test** Not supported.	—
0	0	RO	**Extended Capable** 1 = Extended register capable. 0 = Not extended register capable.	—

4.2.7.3 PHY 1 PHYID Low Register (0x050 – 0x051): PHY1ILR

This register contains the PHY ID (low) for the switch port 1 function.

TABLE 4-35: PHY 1 PHYID LOW REGISTER (0X050 – 0X051): PHY1ILR

Bit	Default	R/W	Description
15 – 0	0x1430	RO	**PHY 1 ID Low Word** Low order PHY 1 ID bits.

4.2.7.4 PHY 1 PHYID High Register (0x052 – 0x053): PHY1IHR

This register contains the PHY ID (high) for the switch port 1 function.

TABLE 4-36: PHY 1 PHYID HIGH REGISTER (0X052 – 0X053): PHY1IHR

Bit	Default	R/W	Description
15 – 0	0x0022	RO	**PHY 1 ID High Word** High-order PHY 1 ID bits.

4.2.7.5 PHY 1 Auto-Negotiation Advertisement Register (0x054 – 0x055): P1ANAR

This register contains the auto-negotiation advertisement bits for the switch port 1 function.

TABLE 4-37: PHY 1 AUTO-NEGOTIATION ADVERTISEMENT REGISTER (0X054 – 0X055): P1ANAR

Bit	Default	R/W	Description	Bit is Same As
15	0	RO	**Next page** Not supported.	—
14	0	RO	Reserved	—
13	0	RO	**Remote fault** Not supported.	—
12 – 11	00	RO	Reserved	—

TABLE 4-37: PHY 1 AUTO-NEGOTIATION ADVERTISEMENT REGISTER (0X054 – 0X055): P1ANAR (CONTINUED)

Bit	Default	R/W	Description	Bit is Same As
10	1	RW	**Pause (flow control capability)** 1 = Advertise pause ability. 0 = Do not advertise pause capability.	Bit[4] in P1CR4
9	0	RW	Reserved	—
8	1	RW	**Advertise 100BASE-TX Full-Duplex** 1 = Advertise 100BASE-TX full-duplex capable. 0 = Do not advertise 100BASE-TX full-duplex capability.	Bit[3] in P1CR4
7	1	RW	**Advertise 100BASE-TX Half-Duplex** 1= Advertise 100BASE-TX half-duplex capable. 0 = Do not advertise 100BASE-TX half-duplex capability.	Bit[2] in P1CR4
6	1	RW	**Advertise 10BASE-T Full-Duplex** 1 = Advertise 10BASE-T full-duplex capable. 0 = Do not advertise 10BASE-T full-duplex capability.	Bit[1] in P1CR4
5	1	RW	**Advertise 10BASE-T Half-Duplex** 1 = Advertise 10BASE-T half-duplex capable. 0 = Do not advertise 10BASE-T half-duplex capability.	Bit[0] in P1CR4
4 – 0	0x01	RO	**Selector Field** 802.3	—

4.2.7.6 PHY 1 Auto-Negotiation Link Partner Ability Register (0x056 – 0x057): P1ANLPR

This register contains the auto-negotiation link partner ability bits for the switch port 1 function.

TABLE 4-38: PHY 1 AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER (0X056 – 0X057): P1ANLPR

Bit	Default	R/W	Description	Bit is Same As
15	0	RO	**Next page** Not supported.	—
14	0	RO	**LP ACK** Not supported.	—
13	0	RO	**Remote fault** Not supported.	—
12 - 11	00	RO	Reserved	—
10	0	RO	**Pause** Link partner pause capability.	
9	0	RO	Reserved	—
8	0	RO	**Advertise 100BASE-TX Full-Duplex** Link partner 100BASE-TX full-duplex capability.	
7	0	RO	**Advertise 100BASE-TX Half-Duplex** Link partner 100 half-duplex capability.	
6	0	RO	**Advertise 10BASE-T Full-Duplex** Link partner 10BASE-T full-duplex capability.	
5	0	RO	**Advertise 10BASE-T Half-Duplex** Link partner 10BASE-T half-duplex capability.	
4 - 0	0x01	RO	Reserved	—

4.2.7.7 PHY 2 and MII Basic Control Register (0x058 – 0x059): P2MBCR

This register contains media independent interface (MII) control bits for the switch port 2 function as defined in the IEEE 802.3 specification.

TABLE 4-39: PHY 2 AND MII BASIC CONTROL REGISTER (0X058 – 0X059): P2MBCR

Bit	Default	R/W	Description	Bit is Same As
15	0	RO	Reserved	—
14	0	RW	**Far-End Loopback** 1 = Perform loopback, as follows: Start: RXP1/RXM1 (port 1) Loopback: PMD/PMA of port 2's PHY End: TXP1/TXM1 (port 1) 0 = Normal operation.	Bit[8] in P2CR4
13	1	RW	**Force 100BASE-TX** 1 = Force 100 Mbps if auto-negotiation is disabled (bit [12]) 0 = Force 10 Mbps if auto-negotiation is disabled (bit [12])	Bit[6] in P2CR4
12	1	RW	**Auto-Negotiation Enable** 1 = Auto-negotiation enabled. 0 = Auto-negotiation disabled.	Bit[7] in P2CR4
11	0	RW	**Power Down** 1 = Power down. 0 = Normal operation.	Bit[11] in P2CR4
10	0	RO	**Isolate** Not supported.	—
9	0	RW/SC	**Restart Auto-Negotiation** 1 = Restart auto-negotiation. 0 = Normal operation	Bit[13] in P2CR4
8	1	RW	**Force Full-Duplex** 1 = Force full-duplex. 0 = Force half-duplex. Applies only when auto-negotiation is disabled (bit [12]). It is always in half-duplex if auto-negotiation is enabled but failed.	Bit[5] in P2CR4
7	0	RO	**Collision test** Not supported.	—
6	0	RO	Reserved	—
5	1	RW	**HP_MDIX** 1 = HP Auto-MDI-X mode. 0 = Microchip Auto-MDI-X mode.	Bit[15] in P2SR
4	0	RW	**Force MDI-X** 1 = Force MDI-X. 0 = Normal operation.	Bit[9] in P2CR4
3	0	RW	**Disable Auto- MDI-X** 1 = Disable Auto-MDI-X. 0 = Normal operation.	Bit[10] in P2CR4
2	0	RW	**Disable Far-End-Fault** 1 = Disable far-end-fault detection. 0 = Normal operation. For 100BASE-FX fiber mode operation.	Bit[12] in P2CR4

TABLE 4-39: PHY 2 AND MII BASIC CONTROL REGISTER (0X058 – 0X059): P2MBCR

Bit	Default	R/W	Description	Bit is Same As
1	0	RW	**Disable Transmit** 1 = Disable transmit. 0 = Normal operation.	Bit[14] in P2CR4
0	0	RW	Reserved	—

4.2.7.8 PHY 2 and MII Basic Status Register (0x05A – 0x05B): P2MBSR

This register contains the media independent interface (MII) status bits for the switch port 2 function.

TABLE 4-40: PHY 2 AND MII BASIC STATUS REGISTER (0X05A – 0X05B): P2MBSR

Bit	Default	R/W	Description	Bit is Same As
15	0	RO	**T4 Capable** 1 = 100BASE-T4 capable. 0 = Not 100BASE-T4 capable.	—
14	1	RO	**100BASE-TX Full Capable** 1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable.	—
13	1	RO	**100BASE-TX Half Capable** 1 = 100BASE-TX half-duplex capable. 0 = Not 100BASE-TX half-duplex capable.	—
12	1	RO	**10BASE-T Full Capable** 1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.	—
11	1	RO	**10BASE-T Half Capable** 1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.	—
10 - 7	0x0	RO	Reserved	—
6	0	RO	**Preamble Suppressed** Not supported.	—
5	0	RO	**Auto-Negotiation Complete** 1 = Auto-negotiation complete. 0 = Auto-negotiation not completed.	Bit[6] in P2SR
4	0	RO	**Far-End-Fault** 1 = Far-end-fault detected. 0 = No far-end-fault detected. For 100BASE-FX fiber mode operation.	Bit[8] in P2SR
3	1	RO	**Auto-Negotiation Capable** 1 = Auto-negotiation capable. 0 = Not auto-negotiation capable.	—
2	0	RO	**Link Status** 1 = Link is up. 0 = Link is down.	Bit[5] in P2SR
1	0	RO	**Jabber Test** Not supported.	—
0	0	RO	**Extended Capable** 1 = Extended register capable. 0 = Not extended register capable.	—

4.2.7.9 PHY 2 PHYID Low Register (0x05C – 0x05D): PHY2ILR

This register contains the PHY ID (low) for the switch port 2 function.

TABLE 4-41: PHY 2 PHYID LOW REGISTER (0X05C – 0X05D): PHY2ILR

Bit	Default	R/W	Description
15 - 0	0x1430	RO	**PHY 2 ID Low Word** Low order PHY 2 ID bits.

4.2.7.10 PHY 2 PHYID High Register (0x05E – 0x05F): PHY2IHR

This register contains the PHY ID (high) for the switch port 2 function.

TABLE 4-42: PHY 2 PHYID HIGH REGISTER (0X05E – 0X05F): PHY2IHR

Bit	Default	R/W	Description
15 - 0	0x0022	RO	**PHY 2 ID High Word** High order PHY 2 ID bits.

4.2.7.11 PHY 2 Auto-Negotiation Advertisement Register (0x060 – 0x061): P2ANAR

This register contains the auto-negotiation advertisement bits for the switch port 2 function.

TABLE 4-43: PHY 2 AUTO-NEGOTIATION ADVERTISEMENT REGISTER (0X060 – 0X061): P2ANAR

Bit	Default	R/W	Description	Bit is Same As
15	0	RO	**Next Page** Not supported.	—
14	0	RO	Reserved	—
13	0	RO	**Remote Fault** Not supported.	—
12 - 11	00	RO	Reserved	—
10	1	RW	**Pause (Flow Control Capability)** 1 = Advertise pause ability. 0 = Do not advertise pause capability.	Bit[4] in P2CR4
9	0	RW	Reserved	—
8	1	RW	**Advertise 100BASE-TX Full-Duplex** 1 = Advertise 100BASE-TX full-duplex capable. 0 = Do not advertise 100BASE-TX full-duplex capability.	Bit[3] in P2CR4
7	1	RW	**Advertise 100BASE-TX Half-Duplex** 1 = Advertise 100BASE-TX half-duplex capable. 0 = Do not advertise 100BASE-TX half-duplex capability.	Bit[2] in P2CR4
6	1	RW	**Advertise 10BASE-T Full-Duplex** 1 = Advertise 10BASE-T full-duplex capable. 0 = Do not advertise 10BASE-T full-duplex capability.	Bit[1] in P2CR4
5	1	RW	**Advertise 10BASE-T Half-Duplex** 1 = Advertise 10BASE-T half-duplex capable. 0 = Do not advertise 10BASE-T half-duplex capability.	Bit[0] in P2CR4
4 - 0	0x01	RO	**Selector Field** 802.3	—

4.2.7.12 PHY 2 Auto-Negotiation Link Partner Ability Register (0x062 – 0x063): P2ANLPR

This register contains the auto-negotiation link partner ability bits for the switch port 2 function.

TABLE 4-44: PHY 2 AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER (0X062 – 0X063): P2ANLPR

Bit	Default	R/W	Description	Bit is Same As
15	0	RO	**Next page** Not supported.	—
14	0	RO	**LP ACK** Not supported.	—
13	0	RO	**Remote fault** Not supported.	—
12 - 11	00	RO	Reserved	—
10	0	RO	**Pause** Link partner pause capability.	Bit[4] in P2SR
9	0	RO	Reserved	—
8	0	RO	**Advertise 100BASE-TX Full-Duplex** Link partner 100BASE-TX full-duplex capability.	Bit[3] in P2SR
7	0	RO	**Advertise 100BASE-TX Half-Duplex** Link partner 100 half-duplex capability.	Bit[2] in P2SR
6	0	RO	**Advertise 10BASE-T Full-Duplex** Link partner 10BASE-T full-duplex capability.	Bit[1] in P2SR
5	0	RO	**Advertise 10BASE-T Half-Duplex** Link partner 10BASE-T half-duplex capability.	Bit[0] in P2SR
4 - 0	0x01	RO	Reserved	—

4.2.7.13 0x064 – 0x065: Reserved

4.2.7.14 PHY1 Special Control and Status Register (0x066 – 0x067): P1PHYCTRL

This register contains control and status information of PHY 1.

TABLE 4-45: PHY1 SPECIAL CONTROL AND STATUS REGISTER (0X066 – 0X067): P1PHYCTRL

Bit	Default	R/W	Description	Bit is Same As
15 - 6	0x000	RO	Reserved	—
5	0	RO	**Polarity Reverse** 1 = Polarity is reversed. 0 = Polarity is not reversed.	Bit[13] in P1SR
4	0	RO	**MDI-X Status** 0 = MDI 1 = MDI-X	Bit[7] in P1SR
3	0	RW	**Force Link** 1 = Force link pass. 0 = Normal operation.	Bit[11] in P1SCSLMD
2	1	RW	**Enable Energy Efficient Ethernet (EEE) on 10BASE-Te** 1 = Disable 10BASE-Te. 0 = Enable 10BASE-Te.	—
1	0	RW	**Remote (Near-End) Loopback** 1 = Perform remote loopback at port 1's PHY (RXP1/RXM1 -> TXP1/TXM1) 0 = Normal operation	Bit[9] in P1SCSLMD
0	0	RW	Reserved	—

4.2.7.15 0x068 – 0x069: Reserved

4.2.7.16 PHY 2 Special Control and Status Register (0x06A – 0x06B): P2PHYCTRL

This register contains control and status information of PHY 2.

TABLE 4-46: PHY 2 SPECIAL CONTROL AND STATUS REGISTER (0X06A – 0X06B): P2PHYCTRL

Bit	Default	R/W	Description	Bit is Same As
15 - 6	0x000	RO	Reserved	—
5	0	RO	**Polarity Reverse** 1 = Polarity is reversed. 0 = Polarity is not reversed.	Bit[13] in P2SR
4	0	RO	**MDI-X Status** 0 = MDI 1 = MDI-X	Bit[7] in P2SR
3	0	RW	**Force Link** 1 = Force link pass. 0 = Normal operation.	Bit[11] in P2SCSLMD
2	1	RW	**Enable Energy Efficient Ethernet (EEE) on 10BASE-Te** 1 = Disable 10BASE-Te. 0 = Enable 10BASE-Te.	—
1	0	RW	**Remote (Near-End) Loopback** 1 = Perform remote loopback at port 2's PHY (RXP2/RXM2 -> TXP2/TXM2) 0 = Normal operation	Bit[9] in P2SCSLMD
0	0	RW	Reserved	—

4.2.8 PORT 1 CONTROL REGISTERS

4.2.8.1 Port 1 Control Register 1 (0x06C – 0x06D): P1CR1

This register contains control bits for the switch Port 1 function.

TABLE 4-47: PORT 1 CONTROL REGISTER 1 (0X06C – 0X06D): P1CR1

Bit	Default	R/W	Description
15	0	RO	Reserved
14 - 12	000	RW	**Port 1 LED Direct Control** These bits directly control the port 1 LED pins. 0xx = Normal LED function as set up via Reg. 0x00E – 0x00F, Bits[9:8]. 100 = Both port 1 LEDs off. 101 = Port 1 LED1 off, LED0 on. 110 = Port 1 LED1 on, LED0 off. 111 = Both port 1 LEDs on.
11	0	RW	**Source Address Filtering Enable for MAC Address 2** 1 = Enable the source address filtering function when the SA matches MAC Address 2 in SAFMACA2 (0x0B6 – 0x0BB). 0 = Disable source address filtering function.
10	0	RW	**Source Address Filtering Enable for MAC Address 1** 1 = Enable the source address filtering function when the SA matches MAC Address 1 in SAFMACA1 (0x0B0 – 0x0B5). 0 = Disable source address filtering function.
9	0	RW	**Drop Tagged Packet Enable** 1 = Enable dropping of tagged ingress packets. 0 = Disable dropping of tagged ingress packets.

TABLE 4-47: PORT 1 CONTROL REGISTER 1 (0X06C – 0X06D): P1CR1 (CONTINUED)

Bit	Default	R/W	Description
8	0	RW	**TX Two Queues Select Enable** 1 = The port 1 output queue is split into two priority queues (q0 and q1). 0 = Single output queue on port 1. There is no priority differentiation even though packets are classified into high or low priority. Also see bit 0 in this register. Do not set both bits 0 and 8.
7	0	RW	**Broadcast Storm Protection Enable** 1 = Enable broadcast storm protection for ingress packets on port 1. 0 = Disable broadcast storm protection.
6	0	RW	**Diffserv Priority Classification Enable** 1 = Enable DiffServ priority classification for ingress packets on port 1. 0 = Disable DiffServ function.
5	0	RW	**802.1p Priority Classification Enable** 1 = Enable 802.1p priority classification for ingress packets on port 1. 0 = Disable 802.1p.
4 - 3	00	RW	**Port-Based Priority Classification** 00 = Ingress packets on port 1 are classified as priority 0 queue if “Diff-Serv” or “802.1p” classification is not enabled or fails to classify. 01 = Ingress packets on port 1 are classified as priority 1 queue if “Diff-Serv” or “802.1p” classification is not enabled or fails to classify. 10 = Ingress packets on port 1 are classified as priority 2 queue if “Diff-Serv” or “802.1p” classification is not enabled or fails to classify. 11 = Ingress packets on port 1 are classified as priority 3 queue if “Diff-serv” or “802.1p” classification is not enabled or fails to classify. **Note:** “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	**Tag Insertion** 1 = When packets are output on port 1, the switch adds 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. 0 = Disable tag insertion.
1	0	RW	**Tag Removal** 1 = When packets are output on port 1, the switch removes 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = Disable tag removal.
0	0	RW	**TX Multiple Queues Select Enable** 1 = The port 1 output queue is split into four priority queues (q0, q1, q2 and q3). 0 = Single output queue on the port 1. There is no priority differentiation even though packets are classified into high or low priority. Also see bit 8 in this register. Do not set both bits 0 and 8.

4.2.8.2 Port 1 Control Register 2 (0x06E – 0x06F): P1CR2

This register contains control bits for the switch port 1 function.

TABLE 4-48: PORT 1 CONTROL REGISTER 2 (0X06E – 0X06F): P1CR2

Bit	Default	R/W	Description
15	0	RW	Reserved

TABLE 4-48: PORT 1 CONTROL REGISTER 2 (0X06E – 0X06F): P1CR2 (CONTINUED)

Bit	Default	R/W	Description
14	0	RW	**Ingress VLAN Filtering** 1 = The switch discards packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port VID. 0 = No ingress VLAN filtering.
13	0	RW	**Discard Non PVID Packets** 1 = The switch discards packets whose VID does not match the ingress port default VID. 0 = No packets are discarded.
12	0	RW	**Force Flow Control** 1 = Always enable flow control on the port, regardless of auto-negotiation result. 0 = The flow control is enabled based on auto-negotiation result.
11	0	RW	**Back Pressure Enable** 1 = Enable port's half-duplex back pressure. 0 = Disable port's half-duplex back pressure.
10	1	RW	**Transmit Enable** 1 = Enable packet transmission on the port. 0 = Disable packet transmission on the port.
9	1	RW	**Receive Enable** 1 = Enable packet reception on the port. 0 = Disable packet reception on the port.
8	0	RW	**Learning Disable** 1 = Disable switch address learning capability. 0 = Enable switch address learning.
7	0	RW	**Sniffer Port** 1 = Port is designated as a sniffer port and transmits packets that are monitored. 0 = Port is a normal port.
6	0	RW	**Receive Sniff** 1 = All packets received on the port are marked as "monitored packets" and forwarded to the designated "sniffer port." 0 = No receive monitoring.
5	0	RW	**Transmit Sniff** 1 = All packets transmitted on the port are marked as "monitored packets" and forwarded to the designated "sniffer port." 0 = No transmit monitoring.
4	0	RW	Reserved
3	0	RW	**User Priority Ceiling** 1 = If the packet's "priority field" is greater than the "user priority field" in the port VID control register bit[15:13], replace the packet's "priority field" with the "user priority field" in the port VID control register bit[15:13]. 0 = Do not compare and replace the packet's "priority field."
2 - 0	111	RW	**Port VLAN Membership** Define the port's port VLAN membership. Bit[2] stands for the host port, bit [1] for port 2, and bit [0] for port 1. The port can only communicate within the membership. A '1' includes a port in the membership; a '0' excludes a port from the membership.

4.2.8.3 Port 1 VID Control Register (0x070 – 0x071): P1VIDCR

This register contains control bits for the switch port 1 function. This register has two main uses. It is associated with the ingress of untagged packets and used for egress tagging as well as being used for address lookup and providing a default VID for the ingress of untagged or null-VID-tagged packets.

TABLE 4-49: PORT 1 VID CONTROL REGISTER (0X070 – 0X071): P1VIDCR

Bit	Default	R/W	Description
15 - 13	0x0	RW	**Default Tag[15:13]** Port's default tag, containing "User Priority Field" bits.
12	0	RW	**Default Tag[12]** Port's default tag, containing the CFI bit.
11 - 0	0x001	RW	**Default Tag[11:0]** Port's default tag, containing the VID[11:0].

4.2.8.4 Port 1 Control Register 3 (0x072 – 0x073): P1CR3

This register contains control bits for the switch port 1 function.

TABLE 4-50: PORT 1 CONTROL REGISTER 3 (0X072 – 0X073): P1CR3

Bit	Default	R/W	Description
15 - 5	0x000	RO	Reserved
4	0	RW	Reserved
3 - 2	00	RW	**Ingress Limit Mode** These bits determine what kinds of frames are limited and counted against ingress rate limiting as follows: 00 = Limit and count all frames. 01 = Limit and count Broadcast, Multicast, and flooded Unicast frames. 10 = Limit and count Broadcast and Multicast frames only. 11 = Limit and count Broadcast frames only.
1	0	RW	**Count Inter-Frame Gap** Count IFG Bytes. 1 = Each frame's minimum inter frame gap. IFG bytes (12 per frame) are included in Ingress and Egress rate limiting calculations. 0 = IFG bytes are not counted.
0	0	RW	**Count Preamble** Count preamble Bytes. 1 = Each frame's preamble bytes (8 per frame) are included in Ingress and Egress rate limiting calculations. 0 = Preamble bytes are not counted.

4.2.8.5 Port 1 Ingress Rate Control Register 0 (0x074 – 0x075): P1IRCR0

This register contains the port 1 ingress rate limiting control for priority 1 and priority 0.

TABLE 4-51: PORT 1 INGRESS RATE CONTROL REGISTER 0 (0X074 – 0X075): P1IRCR0

Bit	Default	R/W	Description
15	0	RW	Reserved
14 - 8	0x00	RW	**Ingress Data Rate Limit for Priority 1 Frames** Ingress priority 1 frames will be limited or discarded as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	Reserved
6 - 0	0x00	RW	**Ingress Data Rate Limit for Priority 0 Frames** Ingress priority 0 frames will be limited or discarded as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

TABLE 4-52: INGRESS OR EGRESS DATA RATE LIMITS

Data Rate Limit for Ingress or Egress	100BASE-TX for Priority [3:0] Register Bit[14:8] or Bit[6:0]	10BASE-T for Priority [3:0] Register Bit[14:8] or Bit[6:0]
	0x01 to 0x64 for the rate matches 1 Mbps to 100 Mbps respectively	0x01 to 0x0A for the rate matches 1 Mbps to 10 Mbps respectively
	0x00 (default) for the rate is no limit (full 100 Mbps)	0x00 (default) for the rate is no limit (full 10 Mbps)
64 Kbps	0x65	
128 Kbps	0x66	
192 Kbps	0x67	
256 Kbps	0x68	
320 Kbps	0x69	
384 Kbps	0x6A	
448 Kbps	0x6B	
512 Kbps	0x6C	
576 Kbps	0x6D	
640 Kbps	0x6E	
704 Kbps	0x6F	
768 Kbps	0x70	
832 Kbps	0x71	
896 Kbps	0x72	
960 Kbps	0x73	

4.2.8.6 Port 1 Ingress Rate Control Register 1 (0x076 – 0x077): P1IRCR1

This register contains the port 1 ingress rate limiting control bits for priority 3 and priority 2.

TABLE 4-53: PORT 1 INGRESS RATE CONTROL REGISTER 1 (0X076 – 0X077): P1IRCR1

Bit	Default	R/W	Description
15	0	RW	Reserved
14 - 8	0x00	RW	**Ingress Data Rate Limit for Priority 3 Frames** Ingress priority 3 frames will be limited or discarded as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	Reserved
6 - 0	0x00	RW	**Ingress Data Rate Limit for Priority 2 Frames** Ingress priority 2 frames will be limited or discarded as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

4.2.8.7 Port 1 Egress Rate Control Register 0 (0x078 – 0x079): P1ERCR0

This register contains the port 1 egress rate limiting control bits for priority 1 and priority 0. When this port is configured for 1 egress queue (which is the default), only the Priority 0 rate limit is applied. When it is configured for 2 queues, only the Priority 1 and Priority 0 settings are applied.

TABLE 4-54: PORT 1 EGRESS RATE CONTROL REGISTER 0 (0X078 – 0X079): P1ERCR0

Bit	Default	R/W	Description
15	0	RW	Reserved
14 - 8	0x00	RW	**Egress Data Rate Limit for Priority 1 Frames** Egress priority 1 frames will be limited as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	Reserved
6 - 0	0x00	RW	**Egress Data Rate Limit for Priority 0 Frames** Egress priority 0 frames will be limited as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

4.2.8.8 Port 1 Egress Rate Control Register 1 (0x07A – 0x07B): P1ERCR1

This register contains the port 1 egress rate limiting control bits for priority 3 and priority 2. When this port is configured for 1 egress queue (which is the default), only the Priority 0 rate limit is applied. When it is configured for 2 queues, only the Priority 1 and Priority 0 settings are applied.

TABLE 4-55: PORT 1 EGRESS RATE CONTROL REGISTER 1 (0X07A – 0X07B): P1ERCR1

Bit	Default	R/W	Description
15	0	RW	Reserved
14 - 8	0x00	RW	**Egress Data Rate Limit for Priority 3 Frames** Egress priority 3 frames will be limited as shown in the Ingress or Egress Data Rate Limits table. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	Reserved
6 - 0	0x00	RW	**Egress Data Rate Limit for Priority 2 Frames** Egress priority 2 frames will be limited as shown in the Ingress or Egress Data Rate Limits table. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

4.2.8.9 Port 1 PHY Special Control/Status, LinkMD (0x07C – 0x07D): P1SCSLMD

This register contains the LinkMD control and status information of PHY 1.

TABLE 4-56: PORT 1 PHY SPECIAL CONTROL/STATUS, LINKMD (0X07C – 0X07D): P1SCSLMD

Bit	Default	R/W	Description	Bit is Same As
15	0	RO	**CDT_10m_Short** 1 = Less than 10 meter short.	Bit [12] in MIIM PHYAD1 = 0x1, 0x1D
14 - 13	00	RO	**Cable Diagnostic Test Results** [00] = Normal condition. [01] = Open condition has been detected in cable. [10] = Short condition has been detected in cable. [11] = Cable diagnostic test has failed.	Bits[14:13] in MIIM PHYAD1 = 0x1, 0x1D

TABLE 4-56: PORT 1 PHY SPECIAL CONTROL/STATUS, LINKMD (0X07C – 0X07D): P1SCSLMD

Bit	Default	R/W	Description	Bit is Same As
12	0	RW/SC	**Cable Diagnostic Test Enable** 1 = Cable diagnostic test is enabled. It is self-cleared after the test is done. 0 = Indicates that the cable diagnostic test has completed and the status information is valid for reading.	Bit[15] in MIIM PHYAD1 = 0x1, 0x1D
11	0	RW	**Force_Link** 1 = Force link pass. 0 = Normal operation.	Bit[3] in P1PHYCTRL
10	1	RW	Reserved	—
9	0	RW	**Remote (Near-End) Loopback** 1 = Perform remote loopback at port 1's PHY (RXP1/RXM1 -> TXP1/TXM1) 0 = Normal operation	Bit[1] in P1PHYCTRL
8 - 0	0x000	RO	**CDT_Fault_Count** Distance to the fault. It's approximately 0.4m*CDT_Fault_Count.	Bits[8:0] in MIIM PHYAD1 = 0x1, 0x1D

4.2.8.10 Port 1 Control Register 4 (0x07E – 0x07F): P1CR4

This register contains control bits for the switch port 1 function.

TABLE 4-57: PORT 1 CONTROL REGISTER 4 (0X07E – 0X07F): P1CR4

Bit	Default	R/W	Description	Bit is Same As
15	0	RW	Reserved	—
14	0	RW	**Disable Transmit** 1 = Disable the port's transmitter. 0 = Normal operation.	Bit[1] in P1MBCR
13	0	RW/SC	**Restart Auto-Negotiation** 1 = Restart auto-negotiation. 0 = Normal operation.	Bit[9] in P1MBCR
12	0	RW	**Disable Far-End-Fault** 1 = Disable far-end-fault detection. 0 = Normal operation. For 100BASE-FX fiber mode operation.	Bit[2] in P1MBCR
11	0	RW	**Power Down** 1 = Power down. 0 = Normal operation. No change to registers setting.	Bit[11] in P1MBCR
10	0	RW	**Disable Auto-MDI/MDI-X** 1 = Disable Auto-MDI/MDI-X function. 0 = Enable Auto-MDI/MDI-X function.	Bit[3] in P1MBCR
9	0	RW	**Force MDI-X** 1 = If Auto-MDI/MDI-X is disabled, force PHY into MDI-X mode. 0 = Do not force PHY into MDI-X mode.	Bit[4] in P1MBCR
8	0	RW	**Far-End Loopback** 1 = Perform loopback, as indicated: Start: RXP2/RXM2 (port 2). Loopback: PMD/PMA of port 1's PHY. End: TXP2/TXM2 (port 2). 0 = Normal operation.	Bit[14] in P1MBCR

TABLE 4-57: PORT 1 CONTROL REGISTER 4 (0X07E – 0X07F): P1CR4 (CONTINUED)

Bit	Default	R/W	Description	Bit is Same As
7	1	RW	**Auto-Negotiation Enable** 1 = Auto-negotiation is enabled. 0 = Disable auto-negotiation, speed, and duplex are decided by bits[6:5] of the same register.	Bit[12] in P1MBCR
6	1	RW	**Force Speed** 1 = Force 100BASE-TX if auto-negotiation is disabled (bit[7]). 0 = Force 10BASE-T if auto-negotiation is disabled (bit[7]).	Bit[13] in P1MBCR
5	1	RW	**Force Duplex** 1 = Force full-duplex if auto-negotiation is disabled. 0 = Force half-duplex if auto-negotiation is disabled. It is always in half-duplex if auto-negotiation is enabled but failed.	Bit[8] in P1MBCR
4	1	RW	**Advertised Flow Control Capability** 1 = Advertise flow control (pause) capability. 0 = Suppress flow control (pause) capability from transmission to link partner.	Bit[10] in P1ANAR
3	1	RW	**Advertised 100BASE-TX Full-Duplex Capability** 1 = Advertise 100BASE-TX full-duplex capability. 0 = Suppress 100BASE-TX full-duplex capability from transmission to link partner.	Bit [8] in P1ANAR
2	1	RW	**Advertised 100BASE-TX Half-Duplex Capability** 1 = Advertise 100BASE-TX half-duplex capability. 0 = Suppress 100BASE-TX half-duplex capability from transmission to link partner.	Bit[7] in P1ANAR
1	1	RW	**Advertised 10BASE-T Full-Duplex Capability** 1 = Advertise 10BASE-T full-duplex capability. 0 = Suppress 10BASE-T full-duplex capability from transmission to link partner.	Bit[6] in P1ANAR
0	1	RW	**Advertised 10BASE-T Half-Duplex Capability** 1 = Advertise 10BASE-T half-duplex capability. 0 = Suppress 10BASE-T half-duplex capability from transmission to link partner.	Bit[5] in P1ANAR

4.2.8.11 Port 1 Status Register (0x080 – 0x081): P1SR

This register contains status bits for the switch port 1 function.

TABLE 4-58: PORT 1 STATUS REGISTER (0X080 – 0X081): P1SR

Bit	Default	R/W	Description	Bit is Same As
15	1	RW	**HP_Mdix** 1 = HP Auto-MDI-X mode. 0 = Microchip Auto-MDI-X mode.	Bit[5] in P1MBCR
14	0	RO	Reserved	—
13	0	RO	**Polarity Reverse** 1 = Polarity is reversed. 0 = Polarity is not reversed.	Bit[5] in P1PHYCTRL
12	0	RO	**Transmit Flow Control Enable** 1 = Transmit flow control feature is active. 0 = Transmit flow control feature is inactive.	—

TABLE 4-58: PORT 1 STATUS REGISTER (0X080 – 0X081): P1SR (CONTINUED)

Bit	Default	R/W	Description	Bit is Same As
11	0	RO	**Receive Flow Control Enable** 1 = Receive flow control feature is active. 0 = Receive flow control feature is inactive.	—
10	0	RO	**Operation Speed** 1 = Link speed is 100 Mbps. 0 = Link speed is 10 Mbps.	—
9	0	RO	**Operation Duplex** 1 = Link duplex is full. 0 = Link duplex is half.	—
8	0	RO	**Far-End-Fault** 1 = Far-end-fault detected. 0 = No far-end-fault detected. For 100BASE-FX fiber mode operation.	Bit[4] in P1MBSR
7	0	RO	**MDI-X Status** 0 = MDI. 1 = MDI-X.	Bit[4] in P1PHYCTRL
6	0	RO	**Auto-Negotiation Done** 1 = Auto-negotiation done. 0 = Auto-negotiation not done.	Bit[5] in P1MBSR
5	0	RO	**Link Status** 1 = Link good. 0 = Link not good.	Bit[2] in P1MBSR
4	0	RO	**Partner Flow Control Capability** 1 = Link partner flow control (pause) capable. 0 = Link partner not flow control (pause) capable.	Bit[10] in P1ANLPR
3	0	RO	**Partner 100BASE-TX Full-Duplex Capability** 1 = Link partner 100BASE-TX full-duplex capable. 0 = Link partner not 100BASE-TX full-duplex capable.	Bit[8] in P1ANLPR
2	0	RO	**Partner 100BASE-TX Half-Duplex Capability** 1 = Link partner 100BASE-TX half-duplex capable. 0= Link partner not 100BASE-TX half-duplex capable.	Bit[7] in P1ANLPR
1	0	RO	**Partner 10BASE-T Full-Duplex Capability** 1= Link partner 10BASE-T full-duplex capable. 0 = Link partner not 10BASE-T full-duplex capable.	Bit[6] in P1ANLPR
0	0	RO	**Partner 10BASE-T Half-Duplex Capability** 1 = Link partner 10BASE-T half-duplex capable. 0 = Link partner not 10BASE-T half-duplex capable.	Bit[5] in P1ANLPR

4.2.8.12 0x082 – 0x083: Reserved

4.2.9 PORT 2 CONTROL REGISTERS

4.2.9.1 Port 2 Control Register 1 (0x084 – 0x085): P2CR1

This register contains control bits for the switch port 2 function.

TABLE 4-59: PORT 2 CONTROL REGISTER 1 (0X084 – 0X085): P2CR1

Bit	Default	R/W	Description
15	0	RO	Reserved

TABLE 4-59: PORT 2 CONTROL REGISTER 1 (0X084 – 0X085): P2CR1 (CONTINUED)

Bit	Default	R/W	Description
14 - 12	000	RW	**Port 2 LED Direct Control** These bits directly control the port 2 LED pins. 0xx = Normal LED function as set up via Reg. 0x00E – 0x00F, Bit[9:8]. 100 = Both port 2 LEDs off. 101 = Port 2 LED1 off, LED0 on. 110 = Port 2 LED1 on, LED0 off. 111 = Both port 2 LEDs on.
11	0	RW	**Source Address Filtering Enable for MAC Address 2** 1 = Enable the source address filtering function when the SA matches MAC Address 2 in SAFMACA2 (0x0B6 – 0x0BB). 0 = Disable source address filtering function.
10	0	RW	**Source Address Filtering Enable for MAC Address 1** 1 = Enable the source address filtering function when the SA matches MAC Address 1 in SAFMACA1 (0x0B0 – 0x0B5). 0 = Disable source address filtering function.
9	0	RW	**Drop Tagged Packet Enable** 1 = Enable dropping of tagged ingress packets. 0 = Disable dropping of tagged ingress packets.
8	0	RW	**TX Two Queues Select Enable** 1 = The port 2 output queue is split into two priority queues (q0 and q1) 0 = Single output queue on port 2. There is no priority differentiation even though packets are classified into high or low priority.
7	0	RW	**Broadcast Storm Protection Enable** 1 = Enable broadcast storm protection for ingress packets on port 2. 0 = Disable broadcast storm protection.
6	0	RW	**Diffserv Priority Classification Enable** 1 = Enable DiffServ priority classification for ingress packets on port 2. 0 = Disable DiffServ function.
5	0	RW	**802.1p Priority Classification Enable** 1 = Enable 802.1p priority classification for ingress packets on port 2. 0 = Disable 802.1p.
4 - 3	00	RW	**Port-Based Priority Classification** 00 = Ingress packets on port 2 are classified as priority 0 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 01 = Ingress packets on port 2 are classified as priority 1 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 10 = Ingress packets on port 2 are classified as priority 2 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 11 = Ingress packets on port 2 are classified as priority 3 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. **Note:** “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	**Tag Insertion** 1 = When packets are output on port 2, the switch adds 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. 0 = Disable tag insertion.
1	0	RW	**Tag Removal** 1 = When packets are output on port 2, the switch removes 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = Disable tag removal.

TABLE 4-59: PORT 2 CONTROL REGISTER 1 (0X084 – 0X085): P2CR1 (CONTINUED)

Bit	Default	R/W	Description
0	0	RW	**TX Multiple Queues Select Enable** 1 = The port 2 output queue is split into four priority queues (q0, q1, q2 and q3). 0 = Single output queue on port 2. There is no priority differentiation even though packets are classified into high or low priority.

4.2.9.2 Port 2 Control Register 2 (0x086 – 0x087): P2CR2

This register contains control bits for the switch port 2 function.

TABLE 4-60: PORT 2 CONTROL REGISTER 2 (0X086 – 0X087): P2CR2

Bit	Default	R/W	Description
15	0	RW	Reserved
14	0	RW	**Ingress VLAN Filtering** 1 = The switch discards packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port VID. 0 = No ingress VLAN filtering.
13	0	RW	**Discard Non PVID Packets** 1 = The switch discards packets whose VID does not match the ingress port default VID. 0 = No packets are discarded.
12	0	RW	**Force Flow Control** 1 = Always enable flow control on the port, regardless of auto-negotiation result. 0 = The flow control is enabled based on auto-negotiation result.
11	0	RW	**Back Pressure Enable** 1 = Enable port's half-duplex back pressure. 0 = Disable port's half-duplex back pressure.
10	1	RW	**Transmit Enable** 1 = Enable packet transmission on the port. 0 = Disable packet transmission on the port.
9	1	RW	**Receive Enable** 1 = Enable packet reception on the port. 0 = Disable packet reception on the port.
8	0	RW	**Learning Disable** 1 = Disable switch address learning capability. 0 = Enable switch address learning.
7	0	RW	**Sniffer Port** 1 = Port is designated as a sniffer port and transmits packets that are monitored. 0 = Port is a normal port.
6	0	RW	**Receive Sniff** 1 = All packets received on the port are marked as "monitored packets" and forwarded to the designated "sniffer port." 0 = No receive monitoring.
5	0	RW	**Transmit Sniff** 1 = All packets transmitted on the port are marked as "monitored packets" and forwarded to the designated "sniffer port." 0 = No transmit monitoring.
4	0	RW	Reserved
3	0	RW	**User Priority Ceiling** 1 = If the packet's "priority field" is greater than the "user priority field" in the port VID control register bit[15:13], replace the packet's "priority field" with the "user priority field" in the port VID control register bit[15:13]. 0 = Do not compare and replace the packet's "priority field."
2 - 0	111	RW	**Port VLAN Membership** Define the port's port VLAN membership. Bit[2] stands for the host port, bit[1] for port 2, and bit[0] for port 1. The port can only communicate within the membership. A '1' includes a port in the membership; a '0' excludes a port from the membership.

4.2.9.3 Port 2 VID Control Register (0x088 – 0x089): P2VIDCR

This register contains control bits for the switch port 2 function. This register has two main uses. It is associated with the ingress of untagged packets and used for egress tagging as well as being used for address lookup and providing a default VID for the ingress of untagged or null-VID-tagged packets.

TABLE 4-61: PORT 2 VID CONTROL REGISTER (0X088 – 0X089): P2VIDCR

Bit	Default	R/W	Description
15 - 13	000	RW	**Default Tag[15:13]** Port's default tag, containing "User Priority Field" bits.
12	0	RW	**Default Tag[12]** Port's default tag, containing CFI bit.
11 - 0	0x001	RW	**Default Tag[11:0]** Port's default tag, containing VID[11:0].

4.2.9.4 Port 2 Control Register 3 (0x08A – 0x08B): P2CR3

This register contains the control bits for the switch port 2 function.

TABLE 4-62: PORT 2 CONTROL REGISTER 3 (0X08A – 0X08B): P2CR3

Bit	Default	R/W	Description
15 - 5	0x000	RO	Reserved
4	0	RW	Reserved
3 - 2	00	RW	**Ingress Limit Mode** These bits determine what kinds of frames are limited and counted against ingress rate limiting as follows: 00 = Limit and count all frames. 01 = Limit and count Broadcast, Multicast, and flooded Unicast frames. 10 = Limit and count Broadcast and Multicast frames only. 11 = Limit and count Broadcast frames only.
1	0	RW	**Count Inter-Frame Gap** Count IFG Bytes. 1 = Each frame's minimum inter frame gap. IFG bytes (12 per frame) are included in Ingress and Egress rate limiting calculations. 0 = IFG bytes are not counted.
0	0	RW	**Count Preamble** Count preamble Bytes. 1 = Each frame's preamble bytes (8 per frame) are included in Ingress and Egress rate limiting calculations. 0 = Preamble bytes are not counted.

4.2.9.5 Port 2 Ingress Rate Control Register 0 (0x08C – 0x08D): P2IRCR0

This register contains the port 2 ingress rate limiting control bits for priority 1 and priority 0.

TABLE 4-63: PORT 2 INGRESS RATE CONTROL REGISTER 0 (0X08C – 0X08D): P2IRCR0

Bit	Default	R/W	Description
15	0	RW	Reserved
14 - 8	0x00	RW	**Ingress Data Rate Limit for Priority 1 Frames** Ingress priority 1 frames will be limited or discarded as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	Reserved

TABLE 4-63: PORT 2 INGRESS RATE CONTROL REGISTER 0 (0X08C – 0X08D): P2IRCR0

Bit	Default	R/W	Description
6 - 0	0x00	RW	**Ingress Data Rate Limit for Priority 0 Frames** Ingress priority 0 frames will be limited or discarded as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

4.2.9.6 Port 2 Ingress Rate Control Register 1 (0x08E – 0x08F): P2IRCR1

This register contains the port 2 ingress rate limiting control bits for priority 3 and priority 2.

TABLE 4-64: PORT 2 INGRESS RATE CONTROL REGISTER 1 (0X08E – 0X08F): P2IRCR1

Bit	Default	R/W	Description
15	0	RW	Reserved
14 - 8	0x00	RW	**Ingress Data Rate Limit for Priority 3 Frames** Ingress priority 3 frames will be limited or discarded as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	Reserved
6 - 0	0x00	RW	**Ingress Data Rate Limit for Priority 2 Frames** Ingress priority 2 frames will be limited or discarded as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

4.2.9.7 Port 2 Egress Rate Control Register 0 (0x090 – 0x091): P2ERCR0

This register contains the port 2 egress rate limiting control bits for priority 1 and priority 0. When this port is configured for 1 egress queue (which is the default), only the Priority 0 rate limit is applied. When it is configured for 2 queues, only the Priority 1 and Priority 0 settings are applied.

TABLE 4-65: PORT 2 EGRESS RATE CONTROL REGISTER 0 (0X090 – 0X091): P2ERCR0

Bit	Default	R/W	Description
15	0	RW	Reserved
14 - 8	0x00	RW	**Egress Data Rate Limit for Priority 1 Frames** Egress priority 1 frames will be limited as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	Reserved
6 - 0	0x00	RW	**Egress Data Rate Limit for Priority 0 Frames** Egress priority 0 frames will be limited as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

4.2.9.8 Port 2 Egress Rate Control Register 1 (0x092 – 0x093): P2ERCR1

This register contains the port 2 egress rate limiting control bits for priority 3 and priority 2. When this port is configured for 1 egress queue (which is the default), only the Priority 0 rate limit is applied. When it is configured for 2 queues, only the Priority 1 and Priority 0 settings are applied.

TABLE 4-66: PORT 2 EGRESS RATE CONTROL REGISTER 1 (0X092 – 0X093): P2ERCR1

Bit	Default	R/W	Description
15	0	RW	Reserved

TABLE 4-66: PORT 2 EGRESS RATE CONTROL REGISTER 1 (0X092 – 0X093): P2ERCR1

Bit	Default	R/W	Description
14 - 8	0x00	RW	**Egress Data Rate Limit for Priority 3 Frames** Egress priority 3 frames will be limited as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	Reserved
6 - 0	0x00	RW	**Egress Data Rate Limit for Priority 2 Frames** Egress priority 2 frames will be limited as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

4.2.9.9 Port 2 PHY Special Control/Status, LinkMD® (0x094 – 0x095): P2SCSLMD

This register contains the LinkMD control and status information of PHY 2.

TABLE 4-67: PORT 2 PHY SPECIAL CONTROL/STATUS, LINKMD® (0X094 – 0X095): P2SCSLMD

Bit	Default	R/W	Description	Bit is Same As
15	0	RO	**CDT_10m_Short** 1 = Less than 10 meter short.	Bit[12] in MIIM PHYAD = 0x2, 0x1D
14 - 13	00	RO	**Cable Diagnostic Results** [00] = Normal condition. [01] = Open condition has been detected in cable. [10] = Short condition has been detected in cable. [11] = Cable diagnostic test has failed.	Bits[14:13] in MIIM PHYAD = 0x2, 0x1D
12	0	RW/SC	**Cable Diagnostic Test Enable** 1 = Cable diagnostic test is enabled. It is self-cleared after the test is done. 0 = Indicates that the cable diagnostic test has completed and the status information is valid for reading.	Bit[15] in MIIM PHYAD = 0x2, 0x1D
11	0	RW	**Force_Link** Force link. 1 = Force link pass. 0 = Normal operation.	Bit[3] in P2PHYCTRL
10	1	RW	Reserved	—
9	0	RW	**Remote (Near-End) Loopback** 1 = Perform remote loopback at port 2's PHY (RXP2/RXM2 -> TXP2/TXM2) 0 = Normal operation	Bit[1] in P2PHYCTRL
8 - 0	0x000	RO	**CDT_Fault_Count** Distance to the fault. It's approximately 0.4m*CDT_Fault_Count.	Bits[8:0] in MIIM PHYAD = 0x2, 0x1D

4.2.9.10 Port 2 Control Register 4 (0x096 – 0x097): P2CR4

This register contains the control bits for the switch port 2 function.

TABLE 4-68: PORT 2 CONTROL REGISTER 4 (0X096 – 0X097): P2CR4

Bit	Default	R/W	Description	Bit is Same As
15	0	RW	Reserved	—
14	0	RW	**DisableTransmit** 1 = Disable the port's transmitter. 0 = Normal operation.	Bit[1] in P2MBCR

TABLE 4-68: PORT 2 CONTROL REGISTER 4 (0X096 – 0X097): P2CR4 (CONTINUED)

Bit	Default	R/W	Description	Bit is Same As
13	0	RW/SC	**Restart Auto-Negotiation** 1 = Restart auto-negotiation. 0 = Normal operation.	Bit[9] in P2MBCR
12	0	RW	**Disable Far-End-Fault** 1 = Disable far-end-fault detection. 0 = Normal operation. For 100BASE-FX fiber-mode operation.	Bit[2] in P2MBCR
11	0	RW	**Power Down** 1 = Power down. 0 = Normal operation. No change to registers setting	Bit[11] in P2MBCR
10	0	RW	**Disable Auto-MDI/MDI-X** 1 = Disable Auto-MDI/MDI-X function. 0 = Enable Auto- MDI/MDI-X function.	Bit[3] in P2MBCR
9	0	RW	**Force MDI-X** 1 = If Auto-MDI/MDI-X is disabled, force PHY into MDI-X mode. 0 = Do not force PHY into MDI-X mode.	Bit[4] in P2MBCR
8	0	RW	**Far-End Loopback** 1 = Perform loopback, as indicated: Start: RXP1/RXM1 (port 1). Loopback: PMD/PMA of port 2's PHY. End: TXP1/TXM1 (port 1). 0 = Normal operation.	Bit[14] in P2MBCR
7	1	RW	**Auto-Negotiation Enable** 1 = Auto-negotiation is enabled. 0 = Disable auto-negotiation, speed, and duplex are decided by bits [6:5] of the same register.	Bit[12] in P2MBCR
6	1	RW	**Force Speed** 1 = Force 100BASE-TX if auto-negotiation is disabled (bit[7]). 0 = Force 10BASE-T if auto-negotiation is disabled (bit[7]).	Bit[13] in P2MBCR
5	1	RW	**Force Duplex** 1 = Force full-duplex if auto-negotiation is disabled. 0 = Force half-duplex if auto-negotiation is disabled. It is always in half-duplex if auto-negotiation is enabled but failed.	Bit[8] in P2MBCR
4	1	RW	**Advertised Flow Control Capability** 1 = Advertise flow control (pause) capability. 0 = Suppress flow control (pause) capability from transmission to link partner.	Bit[10] in P2ANAR
3	1	RW	**Advertised 100BASE-TX Full-Duplex Capability** 1 = Advertise 100BASE-TX full-duplex capability. 0 = Suppress 100BASE-TX full-duplex capability from transmission to link partner.	Bit[8] in P2ANAR
2	1	RW	**Advertised 100BASE-TX Half-Duplex Capability** 1 = Advertise 100BASE-TX half-duplex capability. 0 = Suppress 100BASE-TX half-duplex capability from transmission to link partner.	Bit[7] in P2ANAR

TABLE 4-68: PORT 2 CONTROL REGISTER 4 (0X096 – 0X097): P2CR4 (CONTINUED)

Bit	Default	R/W	Description	Bit is Same As
1	1	RW	**Advertised 10BASE-T Full-Duplex Capability** 1 = Advertise 10BASE-T full-duplex capability. 0 = Suppress 10BASE-T full-duplex capability from transmission to link partner.	Bit[6] in P2ANAR
0	1	RW	**Advertised 10BASE-T Half-Duplex Capability** 1 = Advertise 10BASE-T half-duplex capability. 0 = Suppress 10BASE-T half-duplex capability from transmission to link partner.	Bit[5] in P2ANAR

4.2.9.11 Port 2 Status Register (0x098 – 0x099): P2SR

This register contains status bits for the switch port 2 function.

TABLE 4-69: PORT 2 STATUS REGISTER (0X098 – 0X099): P2SR

Bit	Default	R/W	Description	Bit is Same As
15	1	RW	**HP_MDIX** 1 = HP Auto-MDI-X mode. 0 = Microchip Auto-MDI-X mode.	Bit[5] in P2MBCR
14	0	RO	Reserved	—
13	0	RO	**Polarity Reverse** 1 = Polarity is reversed. 0 = Polarity is not reversed.	Bit[5] in P2PHYCTRL
12	0	RO	**Transmit Flow Control Enable** 1 = Transmit flow control feature is active. 0 = Transmit flow control feature is inactive.	—
11	0	RO	**Receive Flow Control Enable** 1 = Receive flow control feature is active. 0 = Receive flow control feature is inactive.	—
10	0	RO	**Operation Speed** 1 = Link speed is 100 Mbps. 0 = Link speed is 10 Mbps.	—
9	0	RO	**Operation Duplex** 1 = Link duplex is full. 0 = Link duplex is half.	—
8	0	RO	**Far-End-Fault** 1 = Far-end-fault detected. 0 = No far-end-fault detected. For 100BASE-FX fiber mode operation.	Bit[4] in P2MBSR
7	0	RO	**MDI-X status** 0 = MDI. 1 = MDI-X.	Bit[4] in P2PHYCTRL
6	0	RO	**Auto-Negotiation Done** 1 = Auto-negotiation done. 0 = Auto-negotiation not done.	Bit[5] in P2MBSR
5	0	RO	**Link Status** 1 = Link good. 0 = Link not good.	Bit[2] in P2MBSR
4	0	RO	**Partner Flow Control Capability** 1 = Link partner flow control (pause) capable. 0 = Link partner not flow control (pause) capable.	Bit[10] in P2ANLPR
3	0	RO	**Partner 100BASE-TX Full-Duplex Capability** 1 = Link partner 100BASE-TX full-duplex capable. 0 = Link partner not 100BASE-TX full-duplex capable.	Bit[8] in P2ANLPR

TABLE 4-69: PORT 2 STATUS REGISTER (0X098 – 0X099): P2SR (CONTINUED)

Bit	Default	R/W	Description	Bit is Same As
2	0	RO	**Partner 100BASE-TX Half-Duplex Capability** 1 = Link partner 100BASE-TX half-duplex capable. 0= Link partner not 100BASE-TX half-duplex capable.	Bit[7] in P2ANLPR
1	0	RO	**Partner 10BASE-T Full-Duplex Capability** 1= Link partner 10BASE-T full-duplex capable. 0 = Link partner not 10BASE-T full-duplex capable.	Bit[6] in P2ANLPR
0	0	RO	**Partner 10BASE-T Half-Duplex Capability** 1 = Link partner 10BASE-T half-duplex capable. 0 = Link partner not 10BASE-T half-duplex capable.	Bit[5] in P2ANLPR

4.2.9.12 0x09A – 0x09B: Reserved

4.2.10 PORT 3 CONTROL REGISTERS

4.2.10.1 Port 3 Control Register 1 (0x09C – 0x09D): P3CR1

This register contains control bits for the switch port 3 function.

TABLE 4-70: PORT 3 CONTROL REGISTER 1 (0X09C – 0X09D): P3CR1

Bit	Default	R/W	Description
15 - 10	0x00	RO	Reserved
9	0	RW	**Drop Tagged Packet Enable** 1 = Enable dropping of tagged ingress packets. 0 = Disable dropping of tagged ingress packets.
8	0	RW	**TX Two Queues Select Enable** 1 = The port 3 output queue is split into two priority queues (q0 and q1). 0 = Single output queue on port 3. There is no priority differentiation even though packets are classified into high or low priority.
7	0	RW	**Broadcast Storm Protection Enable** 1 = Enable broadcast storm protection for ingress packets on port 3. 0 = Disable broadcast storm protection.
6	0	RW	**Diffserv Priority Classification Enable** 1 = Enable DiffServ priority classification for ingress packets on port 3. 0 = Disable DiffServ function.
5	0	RW	**802.1p Priority Classification Enable** 1 = Enable 802.1p priority classification for ingress packets on port 3. 0 = Disable 802.1p.
4 - 3	00	RW	**Port-Based Priority Classification** 00 = Ingress packets on port 3 are classified as priority 0 queue if “Diff-Serv” or “802.1p” classification is not enabled or fails to classify. 01 = Ingress packets on port 3 are classified as priority 1 queue if “Diff-Serv” or “802.1p” classification is not enabled or fails to classify. 10 = Ingress packets on port 3 are classified as priority 2 queue if “Diff-Serv” or “802.1p” classification is not enabled or fails to classify. 11 = Ingress packets on port 3 are classified as priority 3 queue if “Diff-serv” or “802.1p” classification is not enabled or fails to classify. **Note:** “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	**Tag Insertion** 1 = When packets are output on port 3, the switch adds 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. 0 = Disable tag insertion.

TABLE 4-70: PORT 3 CONTROL REGISTER 1 (0X09C – 0X09D): P3CR1 (CONTINUED)

Bit	Default	R/W	Description
1	0	RW	**Tag Removal** 1 = When packets are output on port 3, the switch removes 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = Disable tag removal.
0	0	RW	**TX Multiple Queues Select Enable** 1 = The port 3 output queue is split into four priority queues (q0, q1, q2 and q3). 0 = Single output queue on port 3. There is no priority differentiation even though packets are classified into high or low priority.

4.2.10.2 Port 3 Control Register 2 (0x09E – 0x09F): P3CR2

This register contains control bits for the switch port 3 function.

TABLE 4-71: PORT 3 CONTROL REGISTER 2 (0X09E – 0X09F): P3CR2

Bit	Default	R/W	Description
15	0	RW	Reserved
14	0	RW	**Ingress VLAN Filtering** 1 = The switch discards packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port VID. 0 = No ingress VLAN filtering.
13	0	RW	**Discard Non PVID Packets** 1 = The switch discards packets whose VID does not match the ingress port default VID. 0 = No packets are discarded.
12	0	RW	Reserved
11	0	RW	**Back Pressure Enable** 1 = Enable port's half-duplex back pressure. 0 = Disable port's half-duplex back pressure.
10	1	RW	**Transmit Enable** 1 = Enable packet transmission on the port. 0 = Disable packet transmission on the port.
9	1	RW	**Receive Enable** 1 = Enable packet reception on the port. 0 = Disable packet reception on the port.
8	0	RW	**Learning Disable** 1 = Disable switch address learning capability. 0 = Enable switch address learning.
7	0	RW	**Sniffer Port** 1 = Port is designated as a sniffer port and transmits packets that are monitored. 0 = Port is a normal port.
6	0	RW	**Receive Sniff** 1 = All packets received on the port are marked as "monitored packets" and forwarded to the designated "sniffer port." 0 = No receive monitoring.
5	0	RW	**Transmit Sniff** 1 = All packets transmitted on the port are marked as "monitored packets" and forwarded to the designated "sniffer port." 0 = No transmit monitoring.
4	0	RW	Reserved

TABLE 4-71: PORT 3 CONTROL REGISTER 2 (0X09E – 0X09F): P3CR2 (CONTINUED)

Bit	Default	R/W	Description
3	0	RW	**User Priority Ceiling** 1 = If the packet's "priority field" is greater than the "user priority field" in the port VID control register bit[15:13], replace the packet's "priority field" with the "user priority field" in the port VID control register bit[15:13]. 0 = Do not compare and replace the packet's "priority field."
2 - 0	111	RW	Port VLAN Membership Define the port's port VLAN membership. Bit[2] stands for the host port, bit [1] for port 2, and bit [0] for port 1. The port can only communicate within the membership. A '1' includes a port in the membership; a '0' excludes a port from the membership.

4.2.10.3 Port 3 VID Control Register (0x0A0 – 0x0A1): P3VIDCR

This register contains the control bits for the switch port 3 function. This register has two main uses. It is associated with the ingress of untagged packets and used for egress tagging as well as being used for address lookup and providing a default VID for the ingress of untagged or null-VID-tagged packets.

TABLE 4-72: PORT 3 VID CONTROL REGISTER (0X0A0 – 0X0A1): P3VIDCR

Bit	Default	R/W	Description
15 - 13	0x0	RW	**Default Tag[15:13]** Port's default tag, containing "User Priority Field" bits.
12	0	RW	**Default Tag[12]** Port's default tag, containing CFI bit.
11 - 0	0x001	RW	**Default Tag[11:0]** Port's default tag, containing VID[11:0].

4.2.10.4 Port 3 Control Register 3 (0x0A2 – 0x0A3): P3CR3

This register contains the control bits for the switch port 3 function.

TABLE 4-73: PORT 3 CONTROL REGISTER 3 (0X0A2 – 0X0A3): P3CR3

Bit	Default	R/W	Description
15 - 8	0x00	RO	Reserved
7	—	RW	**Port 3 MAC Mode** The RX_DV (pin 31) value is latched into this bit during power-up/reset. 1 = MAC MII mode. 0 = PHY MII mode.
6 - 4	000	RW	Reserved
3 - 2	00	RW	**Ingress Limit Mode** These bits determine what kinds of frames are limited and counted against ingress rate limiting as follows: 00 = Limit and count all frames. 01 = Limit and count Broadcast, Multicast, and flooded Unicast frames. 10 = Limit and count Broadcast and Multicast frames only. 11 = Limit and count Broadcast frames only.
1	0	RW	**Count Inter-Frame Gap** Count IFG Bytes. 1 = Each frame's minimum inter frame gap. IFG bytes (12 per frame) are included in Ingress and Egress rate limiting calculations. 0 = IFG bytes are not counted.
0	0	RW	**Count Preamble** Count preamble Bytes. 1 = Each frame's preamble bytes (8 per frame) are included in Ingress and Egress rate limiting calculations. 0 = Preamble bytes are not counted.

4.2.10.5 Port 3 Ingress Rate Control Register 0 (0x0A4 – 0x0A5): P3IRCR0

This register contains the port 3 ingress rate limiting control bits for priority 1 and priority 0.

TABLE 4-74: PORT 3 INGRESS RATE CONTROL REGISTER 0 (0X0A4 – 0X0A5): P3IRCR0

Bit	Default	R/W	Description
15	0	RW	Reserved
14 - 8	0x00	RW	**Ingress Data Rate Limit for Priority 1 Frames** Ingress priority 1 frames will be limited or discarded as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	**Sample Edge of REFCLK_I clock in Port 3 RMII Mode** The REFCLK input clock sample edge control. 0 = Use the rising edge of REFCLK clock to sample the input data in RMII mode. 1 = Use the falling edge of REFCLK clock to sample the input data in RMII mode.
6 - 0	0x00	RW	**Ingress Data Rate Limit for Priority 0 Frames** Ingress priority 0 frames will be limited or discarded as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

4.2.10.6 Port 3 Ingress Rate Control Register 1 (0x0A6 – 0x0A7): P3IRCR1

This register contains the port 3 ingress rate limiting control bits for priority 3 and priority 2.

TABLE 4-75: PORT 3 INGRESS RATE CONTROL REGISTER 1 (0X0A6 – 0X0A7): P3IRCR1

Bit	Default	R/W	Description
15	0	RW	Reserved
14 - 8	0x00	RW	**Ingress Data Rate Limit for Priority 3 Frames** Ingress priority 3 frames will be limited or discarded as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	Reserved
6 - 0	0x00	RW	**Ingress Data Rate Limit for Priority 2 Frames** Ingress priority 2 frames will be limited or discarded as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

4.2.10.7 Port 3 Egress Rate Control Register 0 (0x0A8 – 0x0A9): P3ERCR0

This register contains the port 3 egress rate limiting control bits for priority 1 and priority 0. When this port is configured for 1 egress queue (which is the default), only the Priority 0 rate limit is applied. When it is configured for 2 queues, only the Priority 1 and Priority 0 settings are applied.

TABLE 4-76: PORT 3 EGRESS RATE CONTROL REGISTER 0 (0X0A8 – 0X0A9): P3ERCR0

Bit	Default	R/W	Description
15	0	RW	Reserved
14 - 8	0x00	RW	**Egress Data Rate Limit for Priority 1 Frames** Egress priority 1 frames will be limited as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

TABLE 4-76: PORT 3 EGRESS RATE CONTROL REGISTER 0 (0X0A8 – 0X0A9): P3ERCR0

Bit	Default	R/W	Description
7	0	RW	**Egress Rate Limit Control Enable** 1 = Enable egress rate limit control. 0 = Disable egress rate limit control.
6 - 0	0x00	RW	**Egress Data Rate Limit for Priority 0 Frames** Egress priority 0 frames will be limited as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

4.2.10.8 Port 3 Egress Rate Control Register 1 (0x0AA – 0x0AB): P3ERCR1

This register contains the port 3 egress rate limiting control bits for priority 3 and priority 2. When this port is configured for 1 egress queue (which is the default), only the Priority 0 rate limit is applied. When it is configured for 2 queues, only the Priority 1 and Priority 0 settings are applied.

TABLE 4-77: PORT 3 EGRESS RATE CONTROL REGISTER 1 (0X0AA – 0X0AB): P3ERCR1

Bit	Default	R/W	Description
15	0	RW	Reserved
14 - 8	0x00	RW	**Egress Data Rate Limit for Priority 3 Frames** Egress priority 3 frames will be limited as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	Reserved
6 - 0	0x00	RW	**Egress Data Rate Limit for Priority 2 Frames** Egress priority 2 frames will be limited as shown in Table 4-52. **Note:** The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

4.2.11 SWITCH GLOBAL CONTROL REGISTERS

4.2.11.1 Switch Global Control Register 8 (0x0AC – 0x0AD): SGCR8

This register contains the global control bits for the switch function.

TABLE 4-78: SWITCH GLOBAL CONTROL REGISTER 8 (0X0AC – 0X0AD): SGCR8

Bit	Default	R/W	Description
15 - 14	10	RW	**Two Queue Priority Mapping** These bits determine the mapping between the priority of the incoming frames and the destination on-chip queue in a two queue configuration which uses egress queues 0 and 1. ‘00’ = Reserved ‘01’ = Egress Queue 1 receives priority 1, 2, 3 frames Egress Queue 0 receives priority 0 frames ‘10’ = (default) Reserved ‘11’ = Egress Queue 1 receives priority 1, 2, 3 frames Egress Queue 0 receives priority 0 frames
13 - 11	000	RO	Reserved
10	0	RW/SC	**Flush Dynamic MAC Table** Before flushing the dynamic MAC table, switch address learning must be disabled by setting bit[8] in the P1CR2, P2CR2, and P3CR2 registers.
9	0	RW	**Flush Static MAC Table** 1 = Enable flush static MAC table for spanning tree application. 0 = Disable flush static MAC table for spanning tree application.

TABLE 4-78: SWITCH GLOBAL CONTROL REGISTER 8 (0X0AC – 0X0AD): SGCR8 (CONTINUED)

Bit	Default	R/W	Description
8	0	RW	**Port 3 Tail-Tag Mode Enable** 1 = Enable tail tag mode. 0 = Disable tail tag mode.
7 - 0	0x00	RW	**Force PAUSE Off Iteration Limit Time Enable** 0x01 – 0xFF = Enable to force PAUSE off iteration limit time (a unit number is 160 ms). 0x00 = Disable Force PAUSE Off Iteration Limit.

4.2.11.2 Switch Global Control Register 9 (0x0AE – 0x0AF): SGCR9

This register contains the global control bits for the switch function.

TABLE 4-79: SWITCH GLOBAL CONTROL REGISTER 9 (0X0AE – 0X0AF): SGCR9

Bit	Default	R/W	Description
15 - 11	0x00	RO	Reserved
10 - 8	000	RW	**Forwarding Invalid Frame** Define the forwarding port for frame with invalid VID. Bit[10] stands for the host port, bit[9] for port 2, and bit[8] for port 1.
7 - 6	00	RW	Reserved
5	0	RW	**Enable Insert Source Port PVID Tag when Untagged Frame from Port 3 to Port 2** 1 = Enable. 0 = Disable.
4	0	RW	**Enable Insert Source Port PVID Tag when Untagged Frame from Port 3 to Port 1** 1 = Enable. 0 = Disable.
3	0	RW	**Enable Insert Source Port PVID Tag when Untagged Frame from Port 2 to Port 3** 1 = Enable. 0 = Disable.
2	0	RW	**Enable Insert Source Port PVID Tag when Untagged Frame from Port 2 to Port 1** 1 = Enable. 0 = Disable.
1	0	RW	**Enable Insert Source Port PVID Tag when Untagged Frame from Port 1 to Port 3** 1 = Enable. 0 = Disable.
0	0	RW	**Enable Insert Source Port PVID Tag when Untagged Frame from Port 1 to Port 2** 1 = Enable. 0 = Disable.

4.2.12 SOURCE ADDRESS FILTERING MAC ADDRESS REGISTERS

4.2.12.1 Source Address Filtering MAC Address 1 Register Low (0x0B0 – 0x0B1): SAFMACA1L

The following table shows the register bit fields for the low word of MAC Address 1.

TABLE 4-80: SOURCE ADDRESS FILTERING MAC ADDRESS 1 REGISTER LOW (0X0B0 – 0X0B1): SAFMACA1L

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Source Filtering MAC Address 1 Low** The least significant word of MAC Address 1.

4.2.12.2 Source Address Filtering MAC Address 1 Register Middle (0x0B2 – 0x0B3): SAFMACA1M

The following table shows the register bit fields for the middle word of MAC Address 1.

TABLE 4-81: SOURCE ADDRESS FILTERING MAC ADDRESS 1 REGISTER MIDDLE (0X0B2 – 0X0B3): SAFMACA1M

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Source Filtering MAC Address Middle 1** The middle word of MAC Address 1.

4.2.12.3 Source Address Filtering MAC Address 1 Register High (0x0B4 – 0x0B5): SAFMACA1H

The following table shows the register bit fields for the high word of MAC Address 1.

TABLE 4-82: SOURCE ADDRESS FILTERING MAC ADDRESS 1 REGISTER HIGH (0X0B4 – 0X0B5): SAFMACA1H

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Source Filtering MAC Address 1 High** The most significant word of MAC Address 1.

4.2.12.4 Source Address Filtering MAC Address 2 Register Low (0x0B6 – 0x0B7): SAFMACA2L

The following table shows the register bit fields for the low word of MAC Address 2.

TABLE 4-83: SOURCE ADDRESS FILTERING MAC ADDRESS 2 REGISTER LOW (0X0B6 – 0X0B7): SAFMACA2L

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Source Filtering MAC Address Low 2** The least significant word of MAC Address 2.

4.2.12.5 Source Address Filtering MAC Address 2 Register Middle (0x0B8 – 0x0B9): SAFMACA2M

The following table shows the register bit fields for the middle word of MAC Address 2.

TABLE 4-84: SOURCE ADDRESS FILTERING MAC ADDRESS 2 REGISTER MIDDLE (0X0B8 – 0X0B9): SAFMACA2M

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Source Filtering MAC Address Middle 2** The middle word of MAC Address 2.

4.2.12.6 Source Address Filtering MAC Address 2 Register High (0x0BA – 0x0BB): SAFMACA2H

The following table shows the register bit fields for the high word of MAC Address 2.

TABLE 4-85: SOURCE ADDRESS FILTERING MAC ADDRESS 2 REGISTER HIGH (0X0BA – 0X0BB): SAFMACA2H

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Source Filtering MAC Address High 2** The most significant word of MAC Address 2.

4.2.12.7 0x0BC – 0x0C7: Reserved

4.2.13 TXQ RATE CONTROL REGISTERS

4.2.13.1 Port 1 TXQ Rate Control Register 1 (0x0C8 – 0x0C9): P1TXQRCR1

This register contains the q2 and q3 rate control bits for port 1.

TABLE 4-86: PORT 1 TXQ RATE CONTROL REGISTER 1 (0X0C8 – 0X0C9): P1TXQRCR1

Bit	Default	R/W	Description
15	1	RW	**Port 1 Transmit Queue 2 (high) Ratio Control** 0 = Strict priority. Port 1 will transmit all the packets from this priority q2 before transmit lower priority queue. 1 = Bit[14:8] reflect the number of packets allow to transmit from this priority q2 within a certain time.
14 - 8	0x04	RW	**Port 1 Transmit Queue 2 (high) Ratio** This ratio indicates the number of packet for high priority packet can transmit within a given period.
7	1	RW	**Port 1 Transmit Queue 3 (highest) Ratio Control** 0 = Strict priority. Port 1 will transmit all the packets from this priority q3 before transmit lower priority queue. 1 = Bit[6:0] reflect the number of packets allow to transmit from this priority q3 within a certain time.
6 - 0	0x08	RW	**Port 1 Transmit Queue 3 (highest) Ratio** This ratio indicates the number of packet for highest priority packet can transmit within a given period.

4.2.13.2 Port 1 TXQ Rate Control Register 2 (0x0CA – 0x0CB): P1TXQRCR2

This register contains the q0 and q1 rate control bits for port 1.

TABLE 4-87: PORT 1 TXQ RATE CONTROL REGISTER 2 (0X0CA – 0X0CB): P1TXQRCR2

Bit	Default	R/W	Description
15	1	RW	**Port 1 Transmit Queue 0 (lowest) Ratio Control** 0 = Strict priority. Port 1 will transmit all the packets from this priority q0 after transmit higher priority queue. 1 = Bit[14:8] reflect the number of packets allow to transmit from this priority q0 within a certain time.
14 - 8	0x01	RW	**Port 1 Transmit Queue 0 (lowest) Ratio** This ratio indicates the number of packet for lowest priority packet can transmit within a given period.
7	1	RW	**Port 1 Transmit Queue 1 (low) Ratio Control** 0 = Strict priority. Port 1 will transmit all the packets from this priority q1 before transmit lower priority queue. 1 = Bit[6:0] reflect the number of packets allow to transmit from this priority q1 within a certain time.

TABLE 4-87: PORT 1 TXQ RATE CONTROL REGISTER 2 (0X0CA – 0X0CB): P1TXQRCR2

Bit	Default	R/W	Description
6 - 0	0x02	RW	**Port 1 Transmit Queue 1 (low) Ratio** This ratio indicates the number of packet for low priority packet can transmit within a given period.

4.2.13.3 Port 2 TXQ Rate Control Register 1 (0x0CC – 0x0CD): P2TXQRCR1

This register contains the q2 and q3 rate control bits for port 2.

TABLE 4-88: PORT 2 TXQ RATE CONTROL REGISTER 1 (0X0CC – 0X0CD): P2TXQRCR1

Bit	Default	R/W	Description
15	1	RW	**Port 2 Transmit Queue 2 (high) Ratio Control** 0 = Strict priority. Port 2 will transmit all the packets from this priority q2 before transmit lower priority queue. 1 = Bit[14:8] reflect the number of packets allow to transmit from this priority q2 within a certain time.
14 - 8	0x04	RW	**Port 2 Transmit Queue 2 (high) Ratio** This ratio indicates the number of packet for high priority packet can transmit within a given period.
7	1	RW	**Port 2 Transmit Queue 3 (highest) Ratio Control** 0 = Strict priority. Port 2 will transmit all the packets from this priority q3 before transmit lower priority queue. 1 = Bit[6:0] reflect the number of packets allow to transmit from this priority q3 within a certain time.
6 - 0	0x08	RW	**Port 2 Transmit Queue 3 (highest) Ratio** This ratio indicates the number of packet for highest priority packet can transmit within a given period.

4.2.13.4 Port 2 TXQ Rate Control Register 2 (0x0CE – 0x0CF): P2TXQRCR2

This register contains the q0 and q1 rate control bits for port 2.

TABLE 4-89: PORT 2 TXQ RATE CONTROL REGISTER 2 (0X0CE – 0X0CF): P2TXQRCR2

Bit	Default	R/W	Description
15	1	RW	**Port 2 Transmit Queue 0 (lowest) Ratio Control** 0 = Strict priority. Port 2 will transmit all the packets from this priority q0 after transmit higher priority queue. 1 = Bit[14:8] reflect the number of packets allow to transmit from this priority q0 within a certain time.
14 - 8	0x01	RW	**Port 2 Transmit Queue 0 (lowest) Ratio** This ratio indicates the number of packet for lowest priority packet can transmit within a given period.
7	1	RW	**Port 2 Transmit Queue 1 (low) Ratio Control** 0 = Strict priority. Port 2 will transmit all the packets from this priority q1 before transmit lower priority queue. 1 = Bit[6:0] reflect the number of packets allow to transmit from this priority q1 within a certain time.
6 - 0	0x02	RW	**Port 2 Transmit Queue 1 (low) Ratio** This ratio indicates the number of packet for low priority packet can transmit within a given period.

4.2.13.5 Port 3 TXQ Rate Control Register 1 (0x0D0 – 0x0D1): P3TXQRCR1

This register contains the q2 and q3 rate control bits for port 3.

TABLE 4-90: PORT 3 TXQ RATE CONTROL REGISTER 1 (0X0D0 – 0X0D1): P3TXQRCR1

Bit	Default	R/W	Description
15	1	RW	**Port 3 Transmit Queue 2 (high) Ratio Control** 0 = Strict priority. Port 3 will transmit all the packets from this priority q2 before transmit lower priority queue. 1 = Bit[14:8] reflect the number of packets allow to transmit from this priority q2 within a certain time.
14 - 8	0x04	RW	**Port 3 Transmit Queue 2 (high) Ratio** This ratio indicates the number of packet for high priority packet can transmit within a given period.
7	1	RW	**Port 3 Transmit Queue 3 (highest) Ratio Control** 0 = Strict priority. Port 3 will transmit all the packets from this priority q3 before transmit lower priority queue. 1 = Bit[6:0] reflect the number of packets allow to transmit from this priority q3 within a certain time.
6 - 0	0x08	RW	**Port 3 Transmit Queue 3 (highest) Ratio** This ratio indicates the number of packet for highest priority packet can transmit within a given period.

4.2.13.6 Port 3 TXQ Rate Control Register 2 (0x0D2 – 0x0D3): P3TXQRCR2

This register contains the q0 and q1 rate control bits for port 3.

TABLE 4-91: PORT 3 TXQ RATE CONTROL REGISTER 2 (0X0D2 – 0X0D3): P3TXQRCR2

Bit	Default	R/W	Description
15	1	RW	**Port 3 Transmit Queue 0 (lowest) Ratio Control** 0 = Strict priority. Port 3 will transmit all the packets from this priority q0 after transmit higher priority queue. 1 = Bit[14:8] reflect the number of packets allow to transmit from this priority q0 within a certain time.
14 - 6	0x01	RW	**Port 3 Transmit Queue 0 (lowest) Ratio** This ratio indicates the number of packet for lowest priority packet can transmit within a given period.
7	1	RW	**Port 3 Transmit Queue 1 (low) Ratio Control** 0 = Strict priority. Port 3 will transmit all the packets from this priority q1 before transmit lower priority queue. 1 = Bit[6:0] reflect the number of packets allow to transmit from this priority q1 within a certain time.
6 - 0	0x02	RW	**Port 3 Transmit Queue 1 (low) Ratio** This ratio indicates the number of packet for low priority packet can transmit within a given period.

4.2.13.7 0x0D4 – 0x0D5: Reserved

4.2.14 INPUT AND OUTPUT MULTIPLEX SELECTION REGISTER

4.2.14.1 Input and Output Multiplex Selection Register (0x0D6 – 0x0D7): IOMXSEL

This register is used to select the functionality of pins 59, 61, and 62. Note that further programmability of the LED function is controlled via bits [9:8] in the SGCR7 Control register.

TABLE 4-92: INPUT AND OUTPUT MULTIPLEX SELECTION REGISTER (0X0D6 – 0X0D7): IOMXSEL

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11	1	RW	Reserved
10	1	RW	**Selection of P2LED1 or GPIO9 on Pin 61** 1 = This pin is used for P2LED1 (default). 0 = This pin is used for GPIO9.
9	1	RW	**Selection of P2LED0 or GPIO10 on Pin 62** 1 = This pin is used for P2LED0 (default). 0 = This pin is used for GPIO10.
8	1	RW	**Selection of P1LED1 or GPIO7 on Pin 59** 1 = This pin is used for P1LED1 (default). 0 = This pin is used for GPIO7.
7	1	RW	Reserved
6	1	RW	Reserved
5	1	RW	Reserved
4	1	RW	Reserved
3	1	RW	Reserved
2	1	RW	Reserved
1	1	RW	Reserved
0	1	RW	Reserved

4.2.15 CONFIGURATION STATUS AND SERIAL BUS MODE REGISTER

4.2.15.1 Configuration Status and Serial Bus Mode Register (0x0D8 – 0x0D9): CFGR

This register is used to select the Serial Bus and Fiber mode. The state of bits [1:0] are determined at reset time using the RXD[1:0] pins.

TABLE 4-93: CONFIGURATION STATUS AND SERIAL BUS MODE REGISTER (0X0D8 – 0X0D9): CFGR

Bit	Default	R/W	Description
15 - 8	0x00	RO	Reserved
7	1	RW	**Selection of Port 2 Mode of Operation** 1 = Select copper mode 0 = Select fiber mode (bypass MLT3 encoder/decoder, scrambler and descrambler). Valid for FML and FRL devices only. When fiber mode is selected, bit[13] in DSP_CNTRL_6 (0x734 – 0x735) should be cleared.
6	1	RW	**Selection of Port 1 Mode of Operation** 1 = Select copper mode 0 = Select fiber mode (bypass MLT3 encoder/decoder, scrambler and descrambler). Valid for FML and FRL devices only. When fiber mode is selected, bit[13] in DSP_CNTRL_6 (0x734 – 0x735) should be cleared.
5 - 4	11	RO	Reserved
3 - 2	11	RW	Reserved
1 - 0	Strap-in value from RXD[1:0]	RW	**Selection of Serial Bus Mode** 00 = Reserved 01 = Reserved 10 = SPI slave Mode 11 = MIIM Mode

4.2.16 PORT 1 AUTO-NEGOTIATION REGISTERS

4.2.16.1 Port 1 Auto-Negotiation Next Page Transmit Register (0x0DC – 0x0DD): P1ANPT

This register contains the port 1 auto-negotiation next page transmit related bits.

TABLE 4-94: PORT 1 AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER (0X0DC – 0X0DD): P1ANPT

Bit	Default	R/W	Description
15	0	RO	**Next Page** Next Page (NP) is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. NP shall be set as follows: 1 = Additional Next Page(s) will follow. 0 = Last page.
14	0	RO	Reserved
13	1	RO	**Message Page** Message Page (MP) is used by the Next Page function to differentiate a Message Page from an Unformatted Page. MP shall be set as follows: 1 = Message Page. 0 = Unformatted Page.
12	0	RO	**Acknowledge 2** Acknowledge 2 (Ack2) is used by the Next Page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows: 1 = Able to comply with message. 0 = Unable to comply with message.
11	0	RO	**Toggle** Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Codeword. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit [11] in the base Link Codeword and, therefore, may assume a value of logic one or zero. The Toggle bit shall be set as follows: 1 = Previous value of the transmitted Link Codeword equal to logic zero. 0 = Previous value of the transmitted Link Codeword equal to logic one.
10 - 0	0x001	RO	**Message and Unformatted Code Field** Message/Unformatted code field bit[10:0]

4.2.16.2 Port 1 Auto-Negotiation Link Partner Received Next Page Register (0x0DE – 0x0DF): P1ALPRNP

This register contains the port 1 auto-negotiation link partner received next page related bits.

TABLE 4-95: PORT 1 AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER (0X0DE – 0X0DF): P1ALPRNP

Bit	Default	R/W	Description
15	0	RO	**Next Page** Next Page (NP) is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. NP shall be set as follows: 1 = Additional Next Page(s) will follow. 0 = Last page.

TABLE 4-95: PORT 1 AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER (0X0DE – 0X0DF): P1ALPRNP (CONTINUED)

Bit	Default	R/W	Description
14	0	RO	**Acknowledge** Acknowledge (Ack) is used by the auto-negotiation function to indicate that a device has successfully received its Link Partner's Link Codeword. The Acknowledge bit is encoded in bit 14 regardless of the value of the Selector Field or Link Codeword encoding. If no Next Page information is to be sent, this bit shall be set to logic one in the Link Codeword after the reception of at least three consecutive and consistent FLP Bursts (ignoring the Acknowledge bit value).
13	0	RO	**Message Page** Message Page (MP) is used by the Next Page function to differentiate a Message Page from an Unformatted Page. MP shall be set as follows: 1 = Message Page. 0 = Unformatted Page.
12	0	RO	**Acknowledge 2** Acknowledge 2 (Ack2) is used by the Next Page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows: 1 = Able to comply with message. 0 = Unable to comply with message.
11	0	RO	**Toggle** Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Codeword. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit [11] in the base Link Codeword and, therefore, may assume a value of logic one or zero. The Toggle bit shall be set as follows: 1 = Previous value of the transmitted Link Codeword equal to logic zero. 0 = Previous value of the transmitted Link Codeword equal to logic one.
10 - 0	0x000	RO	**Message and Unformatted Code Field** Message/Unformatted code field bit[10:0]

4.2.17 PORT 1 EEE REGISTERS

4.2.17.1 Port 1 EEE and Link Partner Advertisement Register (0x0E0 – 0x0E1): P1EEEA

This register contains the port 1 EEE advertisement and link partner advertisement information. Note that EEE is not supported in fiber mode.

TABLE 4-96: PORT 1 EEE AND LINK PARTNER ADVERTISEMENT REGISTER (0X0E0 – 0X0E1): P1EEEA

Bit	Default	R/W	Description
15	0	RO	Reserved
14	0	RO	**10GBASE-KR EEE** 1 = Link Partner EEE is supported for 10GBASE-KR. 0 = Link Partner EEE is not supported for 10GBASE-KR.
13	0	RO	**10GBASE-KX4 EEE** 1 = Link Partner EEE is supported for 10GBASE-KX4. 0 = Link Partner EEE is not supported for 10GBASE-KX4.
12	0	RO	**1000BASE-KX EEE** 1 = Link Partner EEE is supported for 1000BASE-KX. 0 = Link Partner EEE is not supported for 1000BASE-KX.

TABLE 4-96: PORT 1 EEE AND LINK PARTNER ADVERTISEMENT REGISTER (0X0E0 – 0X0E1): P1EEEA (CONTINUED)

Bit	Default	R/W	Description
11	0	RO	**10GBASE-T EEE** 1 = Link Partner EEE is supported for 10GBASE-T. 0 = Link Partner EEE is not supported for 10GBASE-T.
10	0	RO	**1000BASE-T EEE** 1 = Link Partner EEE is supported for 1000BASE-T. 0 = Link Partner EEE is not supported for 1000BASE-T.
9	0	RO	**100BASE-TX EEE** 1 = Link Partner EEE is supported for 100BASE-TX. 0 = Link Partner EEE is not supported for 100BASE-TX.
8 - 7	00	RO	Reserved
6	0	RO	**10GBASE-KR EEE** 1 = Port 1 EEE is supported for 10GBASE-KR. 0 = Port 1 EEE is not supported for 10GBASE-KR.
5	0	RO	**10GBASE-KX4 EEE** 1 = Port 1 EEE is supported for 10GBASE-KX4. 0 = Port 1 EEE is not supported for 10GBASE-KX4.
4	0	RO	**1000BASE-KX EEE** 1 = Port 1 EEE is supported for 1000BASE-KX. 0 = Port 1 EEE is not supported for 1000BASE-KX.
3	0	RO	**10GBASE-T EEE** 1 = Port 1 EEE is supported for 10GBASE-T. 0 = Port 1 EEE is not supported for 10GBASE-T.
2	0	RO	**1000BASE-T EEE** 1 = Port 1 EEE is supported for 1000BASE-T. 0 = Port 1 EEE is not supported for 1000BASE-T.
1	1	RW	**100BASE-TX EEE** 1 = Port 1 EEE is supported for 100BASE-TX. 0 = Port 1 EEE is not supported for 100BASE-TX. To disable EEE capability, clear the port 1 Next Page Enable bit in the PCSEEEC register (0x0F3).
0	0	RO	Reserved

4.2.17.2 Port 1 EEE Wake Error Count Register (0x0E2 – 0x0E3): P1EEEWEC

This register contains the port 1 EEE wake error count information. Note that EEE is not supported in Fiber mode.

TABLE 4-97: PORT 1 EEE WAKE ERROR COUNT REGISTER (0X0E2 – 0X0E3): P1EEEWEC

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Port 1 EEE Wake Error Count** This counter is incremented by each transition of lpi_wake_timer_done from FALSE to TRUE. It means the wakeup time is longer than 20.5 µs. The value will be held at all ones in the case of overflow and will be cleared to zero after this register is read.

4.2.17.3 Port 1 EEE Control/Status and Auto-Negotiation Expansion Register (0x0E4 – 0x0E5): P1EEECS

This register contains the port 1 EEE control/status and auto-negotiation expansion information. Note that EEE is not supported in Fiber mode.

TABLE 4-98: PORT 1 EEE CONTROL/STATUS AND AUTO-NEGOTIATION EXPANSION REGISTER (0X0E4 – 0X0E5): P1EEECS

Bit	Default	R/W	Description
15	1	RW	Reserved
14	0	RO	**Hardware 100BASE-TX EEE Enable Status** 1 = 100BASE-TX EEE is enabled by hardware-based NP exchange. 0 = 100BASE-TX EEE is disabled.
13	0	RO/LH (Latching High)	**TX LPI Received** 1 = Indicates that the transmit PCS has received low power idle (LPI) signaling one or more times since the register was last read. 0 = Indicates that the PCS has not received low power idle (LPI) signaling. The status will be latched high and stay that way until cleared. To clear this status bit, a “1” needs to be written to this register bit.
12	0	RO	**TX LPI Indication** 1 = Indicates that the transmit PCS is currently receiving low power idle (LPI) signals. 0 = Indicates that the PCS is not currently receiving low power idle (LPI) signals. This bit will dynamically indicate the presence of the TX LPI signal.
11	0	RO/LH (Latching High)	**RX LPI Received** 1 = Indicates that the receive PCS has received low power idle (LPI) signaling one or more times since the register was last read. 0 = Indicates that the PCS has not received low power idle (LPI) signaling. The status will be latched high and stay that way until cleared. To clear this status bit, a “1” needs to be written to this register bit.
10	0	RO	**RX LPI Indication** 1 = Indicates that the receive PCS is currently receiving low power idle (LPI) signals. 0 = Indicates that the PCS is not currently receiving low power idle (LPI) signals. This bit will dynamically indicate the presence of the RX LPI signal.
9 - 8	00	RW	Reserved
7	0	RO	Reserved
6	1	RO	**Received Next Page Location Able** 1 = Received Next Page storage location is specified by bit[6:5]. 0 = Received Next Page storage location is not specified by bit[6:5].
5	1	RO	**Received Next Page Storage Location** 1 = Link partner Next Pages are stored in P1ALPRNP (Reg. 0x0DE – 0x0DF). 0 = Link partner Next Pages are stored in P1ANLPR (Reg. 0x056 – 0x057).
4	0	RO/LH (Latching High)	**Parallel Detection Fault** 1 = A fault has been detected via the parallel detection function. 0 = A fault has not been detected via the parallel detection function. This bit is cleared after read.
3	0	RO	**Link Partner Next Page Able** 1 = Link partner is Next Page abled. 0 = Link partner is not Next Page abled.

TABLE 4-98: PORT 1 EEE CONTROL/STATUS AND AUTO-NEGOTIATION EXPANSION REGISTER (0X0E4 – 0X0E5): P1EEECS (CONTINUED)

Bit	Default	R/W	Description
2	0	RO	**Next Page Able** 1 = Local device is Next Page abled. 0 = Local device is not Next Page abled.
1	0	RO/LH (Latching High)	**Page Received** 1 = A New Page has been received. 0 = A New Page has not been received.
0	0	RO	**Link Partner Auto-Negotiation Able** 1 = Link partner is auto-negotiation abled. 0 = Link partner is not auto-negotiation abled.

4.2.18 PORT 1 LPI RECOVERY TIME COUNTER REGISTER

4.2.18.1 Port 1 LPI Recovery Time Counter Register (0x0E6): P1LPIRTC

This register contains the port 1 LPI recovery time counter information.

TABLE 4-99: PORT 1 LPI RECOVERY TIME COUNTER REGISTER (0X0E6): P1LPIRTC

Bit	Default	R/W	Description
7 - 0	0x27 (25 µs)	RW	**Port 1 LPI Recovery Time Counter** This register specifies the time that the MAC device has to wait before it can start to send out packets. This value should be the maximum of the LPI recovery time between local device and remote device. Each count is 640 ns.

4.2.19 BUFFER LOAD-TO-LPI CONTROL 1 REGISTER

4.2.19.1 Buffer Load to LPI Control 1 Register (0x0E7): BL2LPIC1

This register contains the buffer load to LPI Control 1 information.

TABLE 4-100: BUFFER LOAD TO LPI CONTROL 1 REGISTER (0X0E7): BL2LPIC1

Bit	Default	R/W	Description
7	0	RW	**LPI Terminated by Input Traffic Enable** 1 = LPI request will be stopped if input traffic is detected. 0 = LPI request won't be stopped by input traffic.
6	0	RO	Reserved
5 - 0	0x08	RW	**Buffer Load Threshold for Source Port LPI Termination** This value defines the maximum buffer usage allowed for a single port before it starts to trigger the LPI termination for the specific source port. (512 bytes per unit)

4.2.20 PORT 2 AUTO-NEGOTIATION REGISTERS

4.2.20.1 Port 2 Auto-Negotiation Next Page Transmit Register (0x0E8 – 0x0E9): P2ANPT

This register contains the port 2 auto-negotiation next page transmit related bits.

TABLE 4-101: PORT 2 AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER (0X0E8 – 0X0E9): P2ANPT

Bit	Default	R/W	Description
15	0	RO	**Next Page** Next Page (NP) is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. NP shall be set as follows: 1 = Additional Next Page(s) will follow. 0 = Last page.
14	0	RO	Reserved
13	1	RO	**Message Page** Message Page (MP) is used by the Next Page function to differentiate a Message Page from an Unformatted Page. MP shall be set as follows: 1 = Message Page. 0 = Unformatted Page.
12	0	RO	**Acknowledge 2** Acknowledge 2 (Ack2) is used by the Next Page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows: 1 = Able to comply with message. 0 = Unable to comply with message.
11	0	RO	**Toggle** Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Codeword. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit[11] in the base Link Codeword and, therefore, may assume a value of logic one or zero. The Toggle bit shall be set as follows: 1 = Previous value of the transmitted Link Codeword equal to logic zero. 0 = Previous value of the transmitted Link Codeword equal to logic one.
10 - 0	0x001	RO	**Message and Unformatted Code Field** Message/Unformatted code field bit[10:0]

4.2.20.2 Port 2 Auto-Negotiation Link Partner Received Next Page Register (0x0EA – 0x0EB): P2ALPRNP

This register contains the port 2 auto-negotiation link partner received next page related bits.

TABLE 4-102: PORT 2 AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER (0X0EA – 0X0EB): P2ALPRNP

Bit	Default	R/W	Description
15	0	RO	**Next Page** Next Page (NP) is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. NP shall be set as follows: 1 = Additional Next Page(s) will follow. 0 = Last page.

TABLE 4-102: PORT 2 AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER (0X0EA – 0X0EB): P2ALPRNP (CONTINUED)

Bit	Default	R/W	Description
14	0	RO	**Acknowledge** Acknowledge (Ack) is used by the auto-negotiation function to indicate that a device has successfully received its Link Partner's Link Codeword. The Acknowledge bit is encoded in bit [14] regardless of the value of the Selector Field or Link Codeword encoding. If no Next Page information is to be sent, this bit shall be set to logic one in the Link Codeword after the reception of at least three consecutive and consistent FLP Bursts (ignoring the Acknowledge bit value).
13	0	RO	**Message Page** Message Page (MP) is used by the Next Page function to differentiate a Message Page from an Unformatted Page. MP shall be set as follows: 1 = Message Page. 0 = Unformatted Page.
12	0	RO	**Acknowledge 2** Acknowledge 2 (Ack2) is used by the Next Page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows: 1 = Able to comply with message. 0 = Unable to comply with message.
11	0	RO	**Toggle** Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Codeword. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit[11] in the base Link Codeword and, therefore, may assume a value of logic one or zero. The Toggle bit shall be set as follows: 1 = Previous value of the transmitted Link Codeword equal to logic zero. 0 = Previous value of the transmitted Link Codeword equal to logic one.
10 - 0	0x000	RO	**Message and Unformatted Code Field** Message/Unformatted code field bit[10:0]

4.2.21 PORT 2 EEE REGISTERS

4.2.21.1 Port 2 EEE and Link Partner Advertisement Register (0x0EC – 0x0ED): P2EEEA

This register contains the port 2 EEE advertisement and link partner advertisement information. Note that EEE is not supported in Fiber mode. Note that EEE is not supported in Fiber mode.

TABLE 4-103: PORT 2 EEE AND LINK PARTNER ADVERTISEMENT REGISTER (0X0EC – 0X0ED): P2EEEA

Bit	Default	R/W	Description
15	0	RO	Reserved
14	0	RO	**10GBASE-KR EEE** 1 = Link Partner EEE is supported for 10GBASE-KR. 0 = Link Partner EEE is not supported for 10GBASE-KR.
13	0	RO	**10GBASE-KX4 EEE** 1 = Link Partner EEE is supported for 10GBASE-KX4. 0 = Link Partner EEE is not supported for 10GBASE-KX4.
12	0	RO	**1000BASE-KX EEE** 1 = Link Partner EEE is supported for 1000BASE-KX. 0 = Link Partner EEE is not supported for 1000BASE-KX.

TABLE 4-103: PORT 2 EEE AND LINK PARTNER ADVERTISEMENT REGISTER (0X0EC – 0X0ED): P2EEEA (CONTINUED)

Bit	Default	R/W	Description
11	0	RO	**10GBASE-T EEE** 1 = Link Partner EEE is supported for 10GBASE-T. 0 = Link Partner EEE is not supported for 10GBASE-T.
10	0	RO	**1000BASE-T EEE** 1 = Link Partner EEE is supported for 1000BASE-T. 0 = Link Partner EEE is not supported for 1000BASE-T.
9	0	RO	**100BASE-TX EEE** 1 = Link Partner EEE is supported for 100BASE-TX. 0 = Link Partner EEE is not supported for 100BASE-TX.
8 - 7	00	RO	Reserved
6	0	RO	**10GBASE-KR EEE** 1 = Port 2 EEE is supported for 10GBASE-KR. 0 = Port 2 EEE is not supported for 10GBASE-KR.
5	0	RO	**10GBASE-KX4 EEE** 1 = Port 2 EEE is supported for 10GBASE-KX4. 0 = Port 2 EEE is not supported for 10GBASE-KX4.
4	0	RO	**1000BASE-KX EEE** 1 = Port 2 EEE is supported for 1000BASE-KX. 0 = Port 2 EEE is not supported for 1000BASE-KX.
3	0	RO	**10GBASE-T EEE** 1 = Port 2 EEE is supported for 10GBASE-T. 0 = Port 2 EEE is not supported for 10GBASE-T.
2	0	RO	**1000BASE-T EEE** 1 = Port 2 EEE is supported for 1000BASE-T. 0 = Port 2 EEE is not supported for 1000BASE-T.
1	1	RW	**100BASE-TX EEE** 1 = Port 2 EEE is supported for 100BASE-TX. 0 = Port 2 EEE is not supported for 100BASE-TX. To disable EEE capability, clear the port 2 Next Page Enable bit in the PCSEEEC register (0x0F3).
0	0	RO	Reserved

4.2.21.2 Port 2 EEE Wake Error Count Register (0x0EE – 0x0EF): P2EEEWEC

This register contains the port 2 EEE wake error count information. Note that EEE is not supported in Fiber mode.

TABLE 4-104: PORT 2 EEE WAKE ERROR COUNT REGISTER (0X0EE – 0X0EF): P2EEEWEC

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Port 2 EEE Wake Error Count** This counter is incremented by each transition of lpi_wake_timer_done from FALSE to TRUE. It means the wake-up time is longer than 20.5 µs. The value will be held at all ones in the case of overflow and will be cleared to zero after this register is read.

4.2.21.3 Port 2 EEE Control/Status and Auto-Negotiation Expansion Register (0x0F0 – 0x0F1): P2EEECS

This register contains the port 2 EEE control/status and auto-negotiation expansion information. Note that EEE is not supported in Fiber mode.

TABLE 4-105: PORT 2 EEE CONTROL/STATUS AND AUTO-NEGOTIATION EXPANSION REGISTER (0X0F0 – 0X0F1): P2EEECS

Bit	Default	R/W	Description
15	1	RW	Reserved
14	0	RO	**Hardware 100BASE-TX EEE Enable Status** 1 = 100BASE-TX EEE is enabled by hardware based NP exchange. 0 = 100BASE-TX EEE is disabled.
13	0	RO/LH (Latching High)	**TX LPI Received** 1 = Indicates that the transmit PCS has received low power idle (LPI) signaling one or more times since the register was last read. 0 = Indicates that the PCS has not received low power idle (LPI) signaling. The status will be latched high and stay that way until cleared. To clear this status bit, a “1” needs to be written to this register bit.
12	0	RO	**TX LPI Indication** 1 = Indicates that the transmit PCS is currently receiving low power idle (LPI) signals. 0 = Indicates that the PCS is not currently receiving low power idle (LPI) signals. This bit will dynamically indicate the presence of the TX LPI signal.
11	0	RO/LH (Latching High)	**RX LPI Received** 1 = Indicates that the receive PCS has received low power idle (LPI) signaling one or more times since the register was last read. 0 = Indicates that the PCS has not received low power idle (LPI) signaling. The status will be latched high and stay that way until cleared. To clear this status bit, a “1” needs to be written to this register bit.
10	0	RO	**RX LPI Indication** 1 = Indicates that the receive PCS is currently receiving low power idle (LPI) signals. 0 = Indicates that the PCS is not currently receiving low power idle (LPI) signals. This bit will dynamically indicate the presence of the RX LPI signal.
9 - 8	00	RW	Reserved
7	0	RO	Reserved
6	1	RO	**Received Next Page Location Able** 1 = Received Next Page storage location is specified by bit[6:5]. 0 = Received Next Page storage location is not specified by bit[6:5].
5	1	RO	**Received Next Page Storage Location** 1 = Link partner Next Pages are stored in P2ALPRNP (Reg. 0x0EA – 0x0EB). 0 = Link partner Next Pages are stored in P2ANLPR (Reg. 0x062 – 0x063).
4	0	RO/LH (Latching High)	**Parallel Detection Fault** 1 = A fault has been detected via the parallel detection function. 0 = A fault has not been detected via the parallel detection function. This bit is cleared after read.
3	0	RO	**Link Partner Next Page Able** 1 = Link partner is Next Page abled. 0 = Link partner is not Next Page abled.

TABLE 4-105: PORT 2 EEE CONTROL/STATUS AND AUTO-NEGOTIATION EXPANSION REGISTER (0X0F0 – 0X0F1): P2EEECS (CONTINUED)

Bit	Default	R/W	Description
2	1	RO	**Next Page Able** 1 = Local device is Next Page abled. 0 = Local device is not Next Page abled.
1	0	RO/LH (Latching High)	**Page Received** 1 = A New Page has been received. 0 = A New Page has not been received.
0	0	RO	**Link Partner Auto-Negotiation Able** 1 = Link partner is auto-negotiation abled. 0 = Link partner is not auto-negotiation abled.

4.2.22 PORT 2 LPI RECOVERY TIME COUNTER REGISTER

4.2.22.1 Port 2 LPI Recovery Time Counter Register (0x0F2): P2LPIRTC

This register contains the port 2 LPI recovery time counter information.

TABLE 4-106: PORT 2 LPI RECOVERY TIME COUNTER REGISTER (0X0F2): P2LPIRTC

Bit	Default	R/W	Description
7 - 0	0x27 (25 µs)	RW	**Port 2 LPI Recovery Time Counter** This register specifies the time that the MAC device has to wait before it can start to send out packets. This value should be the maximum of the LPI recovery time between local device and remote device. Each count is 640 ns.

4.2.23 PCS EEE CONTROL REGISTER

4.2.23.1 PCS EEE Control Register (0x0F3): PCSEEEC

This register contains the PCS EEE control information.

TABLE 4-107: PCS EEE CONTROL REGISTER (0X0F3): PCSEEEC

Bit	Default	R/W	Description
7	0	RW	Reserved
6	0	RW	Reserved
5 - 2	0x0	RO	Reserved
1	1	RW	**Port 2 Next Page Enable** 1 = Enable next page exchange during auto-negotiation. 0 = Skip next page exchange during auto-negotiation. Auto-negotiation uses next page to negotiate EEE. To disable EEE auto-negotiation on port 2, clear this bit to zero. Restarting auto-negotiation may then be required.
0	1	RW	**Port 1 Next Page Enable** 1 = Enable next page exchange during auto-negotiation. 0 = Skip next page exchange during auto-negotiation. Auto-negotiation uses next page to negotiate EEE. To disable EEE auto-negotiation on port 1, clear this bit to zero. Restarting auto-negotiation may then be required.

4.2.24 EMPTY TXQ-TO-LPI WAIT TIME CONTROL REGISTER

4.2.24.1 Empty TXQ to LPI Wait Time Control Register (0x0F4 – 0x0F5): ETLWTC

This register contains the empty TXQ to LPI wait time control information.

TABLE 4-108: EMPTY TXQ TO LPI WAIT TIME CONTROL REGISTER (0X0F4 – 0X0F5): ETLWTC

Bit	Default	R/W	Description
15 - 0	0x03E8	RW	**Empty TXQ to LPI Wait Time Control** This register specifies the time that the LPI request will be generated after a TXQ has been empty exceeds this configured time. This is only valid when EEE 100BASE-TX is enabled. This setting will apply to all the three ports. The unit is 1.3 ms. The default value is 1.3 seconds (range from 1.3 ms to 86 seconds)

4.2.25 BUFFER LOAD-TO-LPI CONTROL 2 REGISTER

4.2.25.1 Buffer Load to LPI Control 2 Register (0x0F6 – 0x0F7): BL2LPIC2

This register contains the buffer load to LPI control 2 information.

TABLE 4-109: BUFFER LOAD TO LPI CONTROL 2 REGISTER (0X0F6 – 0X0F7): BL2LPIC2

Bit	Default	R/W	Description
15 - 8	0x01	RO	Reserved
7 - 0	0x40	RW	**Buffer Load Threshold for All Ports LPI Termination** This value defines the maximum buffer usage allowed for a single port before it starts to trigger the LPI termination for every port. (128 bytes per unit)

4.2.25.2 0x0F8 – 0x0FF: Reserved

4.2.26 INTERNAL I/O REGISTER SPACE MAPPING FOR INTERRUPTS AND GLOBAL RESET (0X100 – 0X1FF)

4.2.26.1 0x100 – 0x123: Reserved

4.2.26.2 Memory BIST Info Register (0x124 – 0x125): MBIR

This register indicates the built-in self-test results for both TX and RX memories after power-up/reset. The device should be reset after the BIST procedure to ensure proper subsequent operation.

TABLE 4-110: MEMORY BIST INFO REGISTER (0X124 – 0X125): MBIR

Bit	Default	R/W	Description
15	0	RO	**Memory BIST Done** 0 = BIST In progress 1 = BIST Done
14 - 13	00	RO	Reserved
12	—	RO	**TXMBF TX Memory BIST Completed** 0 = TX Memory built-in self-test has not completed. 1 = TX Memory built-in self-test has completed.
11	—	RO	**TXMBFA TX Memory BIST Failed** 0 = TX Memory built-in self-test has completed without failure. 1 = TX Memory built-in self-test has completed with failure.
10 - 8	—	RO	**TXMBFC TX Memory BIST Fail Count** 0 = TX Memory built-in self-test completed with no count failure. 1 = TX Memory built-in self-test encountered a failed count condition.
7 - 5	—	RO	Reserved

TABLE 4-110: MEMORY BIST INFO REGISTER (0X124 – 0X125): MBIR (CONTINUED)

Bit	Default	R/W	Description
4	—	RO	**RXMBF RX Memory BIST Completed** 0 = Completion has not occurred for the RX Memory built-in self-test. 1 = Indicates completion of the RX Memory built-in self-test.
3	—	RO	**RXMBFA RX Memory BIST Failed** 0 = No failure with the RX Memory built-in self-test. 1 = Indicates the RX Memory built-in self-test has failed.
2 - 0	—	RO	**RXMBFC RX Memory BIST Test Fail Count** 0 = No count failure for the RX Memory BIST. 1 = Indicates the RX Memory built−in self-test failed count.

4.2.26.3 Global Reset Register (0x126 – 0x127): GRR

This register controls the global and PTP reset functions with information programmed by the CPU.

TABLE 4-111: GLOBAL RESET REGISTER (0X126 – 0X127): GRR

Bit	Default	R/W	Description
15 - 4	0x000	RO	Reserved
3	0	RW	**Memory BIST Start** 1 = Setting this bit will start the Memory BIST. 0 = Setting this bit will stop the Memory BIST.
2	0	RW	**PTP Module Soft Reset** 1 = Setting this bit resets the 1588/PTP blocks including the time stamp input units, the trigger output units and the PTP clock. 0 = Software reset is inactive.
1	0	RO	Reserved
0	0	RW	**Global Soft Reset** 1 = Software reset is active. 0 = Software reset is inactive. Global software reset will reset all registers to their default value. The strap−in values are not affected. This bit is not self-clearing. After writing a “1” to this bit, wait for 10 ms to elapse then write a “0” for normal operation.

4.2.26.4 0x128 – 0x18F: Reserved

4.2.26.5 Interrupt Enable Register (0x190 – 0x191): IER

This register either enables various interrupts or indicates that the interrupts have been enabled.

TABLE 4-112: INTERRUPT ENABLE REGISTER (0X190 – 0X191): IER

Bit	Default	R/W	Description
15	0	RW	**LCIE Link Change Interrupt Enable** 1 = When this bit is set, the link change interrupt is enabled. 0 = When this bit is reset, the link change interrupt is disabled.
14 - 13	00	RO	Reserved
12	0	RO	**PTP Time stamp Interrupt Enable** 1 = When set, this bit indicates that the PTP time stamp interrupt is enabled. 0 = When cleared, this bit indicates that the PTP time stamp interrupt is disabled. Note that this bit is an “OR” of the PTP_TS_IE[11:0] bits. Clearing the appropriate enable bit in the PTP_TS_IE register (0x68E – 0x68F) or clearing the appropriate status bit in the PTP_TS_IS register (0x68C – 0x68D) will clear this bit. Always write this bit as a zero.

TABLE 4-112: INTERRUPT ENABLE REGISTER (0X190 – 0X191): IER (CONTINUED)

Bit	Default	R/W	Description
11	0	RO	Reserved
10	0	RO	**PTP Trigger Unit Interrupt Enable** 1 = When set, this bit indicates that the PTP trigger output unit interrupt is enabled. 0 = When cleared, this bit indicates that the PTP trigger output unit interrupt is disabled. Note that this bit is an “OR” of the PTP_TRIG_IE[11:0] bits. Clearing the appropriate enable bit in the PTP_TRIG_IE register (0x68A – 0x68B) or clearing the appropriate status bit in the PTP_TRIG_IS register (0x688 – 0x689) will clear this bit. Always write this bit as a zero.
9 - 4	0x00	RO	Reserved
3	0	RW	**LDIE Linkup Detect Interrupt Enable** 1 = When this bit is set, the wake-up from a link up detect interrupt is enabled. 0 = When this bit is reset, the link up detect interrupt is disabled.
2	0	RW	**EDIE Energy Detect Interrupt Enable** 1 = When this bit is set, the wake-up from energy detect interrupt is enabled. 0 = When this bit is reset, the energy detect interrupt is disabled.
1	0	RO	Reserved
0	0	RO	Reserved

4.2.26.6 Interrupt Status Register (0x192 – 0x193): ISR

This register contains the status bits for all interrupt sources. When the corresponding enable bit is set, it causes the interrupt pin to be asserted. This register is usually read by the host CPU and device drivers during an interrupt service routine or polling. The register bits are not cleared when read. To clear the bits, the user has to either write a “1” to a specific bit to clear it, or write a “1” to another bit in another specified register to clear it.

TABLE 4-113: INTERRUPT STATUS REGISTER (0X192 – 0X193): ISR

Bit	Default	R/W	Description
15	0	RO (W1C)	**LCIS Link Change Interrupt Status** When this bit is set, it indicates that the link status has changed from link up to link down, or link down to link up. This edge-triggered interrupt status is cleared by writing a “1” to this bit.
14 - 13	00	RO	Reserved
12	0	RO	**PTP Time stamp Interrupt Status** When this bit is set, it indicates that one of 12 time stamp input units is ready (TS_RDY = “1”) and an event has been captured, or the egress time stamp is available from either port 1 or port 2. This edge-triggered interrupt status is cleared by writing a “1” to this bit.
11	0	RO	Reserved
10	0	RO	**PTP Trigger Unit Interrupt Status** When this bit is set, it indicates that one of 12 trigger output units is done or has an error. This edge-triggered interrupt status is cleared by writing a “1” to this bit.
9 - 4	0x00	RO	Reserved
3	0	RO	**LDIS Linkup Detect Interrupt Status** When this bit is set, it indicates that wake-up from linkup detect status has occurred. Write 0010 to PMCTRL[5:2] to clear this bit.

TABLE 4-113: INTERRUPT STATUS REGISTER (0X192 – 0X193): ISR (CONTINUED)

Bit	Default	R/W	Description
2	0	RO	**EDIS Energy Detect Interrupt Status** When this bit is set, it indicates that wake-up from energy detect status has occurred. Write 0001 to PMCTRL[5:2] to clear this bit.
1 - 0	00	RO	Reserved

4.2.26.7 0x194 – 0x1FF: Reserved

4.2.27 INTERNAL I/O REGISTER SPACE MAPPING FOR TRIGGER OUTPUT UNITS (12 UNITS, 0X200 – 0X3FF)

4.2.27.1 Trigger Error Register (0x200 – 0x201): TRIG_ERR

This register contains the trigger output unit error status.

TABLE 4-114: TRIGGER ERROR REGISTER (0X200 – 0X201): TRIG_ERR

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 0	0x000	RO	**Trigger Output Unit Error** 1 = The trigger time is set earlier than the system time clock when TRIG_NOTIFY bit is set to “1” in TRIG_CFG1 register and it will generate interrupt to host if interrupt enable bit is set in PTP_TRIG_IE register. This bit can be cleared by resetting the TRIG_EN bit to “0”. 0 = No trigger output unit error. There are 12 trigger output units and therefore there is a corresponding Error bit for each of the trigger output units, bit[11:0] = unit[12:1].

4.2.27.2 Trigger Active Register (0x202 – 0x203): TRIG_ACTIVE

This register contains the trigger output unit active status.

TABLE 4-115: TRIGGER ACTIVE REGISTER (0X202 – 0X203): TRIG_ACTIVE

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 0	0x000	RO	**Trigger Output Unit Active** 1 = The trigger output unit is enabled and active without error. 0 = The trigger output unit is finished and inactive. There are 12 trigger output units and therefore there is a corresponding active bit for each of the trigger output units, bit[11:0] = unit[12:1].

4.2.27.3 Trigger Done Register (0x204 – 0x205): TRIG_DONE

This register contains the trigger output unit event done status.

TABLE 4-116: TRIGGER DONE REGISTER (0X204 – 0X205): TRIG_DONE

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 0	0x000	RO (W1C)	**Trigger Output Unit Event Done** 1 = The trigger output unit event has been generated when TRIG_NOTIFY bit is set to “1” in TRIG_CFG1 register (write “1” to clear this bit) and it will generate interrupt to host if interrupt enable bit is set in PTP_TRIG_IE register. 0 = The trigger output unit event is not generated. There are 12 trigger output units and therefore there is a corresponding Done bit for each of the trigger output units, bit[11:0] = unit[12:1].

4.2.27.4 Trigger Enable Register (0x206 – 0x207): TRIG_EN

This register contains the trigger output unit enable control bits.

TABLE 4-117: TRIGGER ENABLE REGISTER (0X206 – 0X207): TRIG_EN

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 0	0x000	RW	**Trigger Output Unit Enable** 1 = Enables the selected trigger output unit and will self-clear when the trigger output is generated. In cascade mode, only enable the head of trigger unit. 0 = The trigger output unit is disabled. There are 12 trigger output units and therefore there is a corresponding enable bit for each of the trigger output units, bit[11:0] = unit[12:1].

4.2.27.5 Trigger Software Reset Register (0x208 – 0x209): TRIG_SW_RST

This register contains the software reset bits for the trigger output units.

TABLE 4-118: TRIGGER SOFTWARE RESET REGISTER (0X208 – 0X209): TRIG_SW_RST

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 0	0x000	RW/SC	**Trigger Output Unit Software Reset** 1 = When set, the selected trigger output unit is put into the inactive state and default setting. This can be used to stop the cascade mode in continuous operation and prepare the selected trigger unit for the next operation. 0 = While zero, the selected trigger output unit is in normal operating mode. There are 12 trigger output units and therefore there is a corresponding software reset bit for each of the trigger output units, bit[11:0] = unit[12:1].

4.2.27.6 Trigger Output Unit 12 Output PPS Pulse-Width Register (0x20A – 0x20B): TRIG12_PPS_WIDTH

This register contains the trigger output unit 12 PPS pulse width and trigger output unit 1 path delay compensation.

TABLE 4-119: TRIGGER OUTPUT UNIT 12 OUTPUT PPS PULSE-WIDTH REGISTER (0X20A – 0X20B): TRIG12_PPS_WIDTH

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11	0	RW	Reserved
10 - 8	000	RW	**Path Delay Compensation for Trigger Output Unit 1** These three bits are used to compensate the path delay of clock skew for event trigger output unit 1 in the range of 0 ns ~ 7 ns (bit[11] = “1”) or 0 ns ~ 28 ns (bit[11] = “0”).
7 - 0	0x00	RW	**PPS Pulse Width for Trigger Output Unit 12** This is upper third byte [23:16] in conjunction with the unit 12 trigger output pulse width in TRIG12_CFG_2[15:0] (0x38A) register to make this register value for PPS pulse width up to 134 ms.

4.2.27.7 0x20C – 0x21F: Reserved

4.2.27.8 Trigger Output Unit 1 Target Time in Nanoseconds Low-Word Register (0x220 – 0x221): TRIG1_TGT_NSL

This register contains the trigger output unit 1 target time in nanoseconds low-word.

TABLE 4-120: TRIGGER OUTPUT UNIT 1 TARGET TIME IN NANOSECONDS LOW-WORD REGISTER (0X220 – 0X221): TRIG1_TGT_NSL

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Trigger Output Unit 1Target Time in Nanoseconds Low-Word [15:0]** This is low-word of target time for trigger output unit 1 in nanoseconds.

4.2.27.9 Trigger Output Unit 1 Target Time in Nanoseconds High-Word Register (0x222 – 0x223): TRIG1_TGT_NSH

This register contains the trigger output unit 1 target time in nanoseconds high-word.

TABLE 4-121: TRIGGER OUTPUT UNIT 1 TARGET TIME IN NANOSECONDS HIGH-WORD REGISTER (0X222 – 0X223): TRIG1_TGT_NSH

Bit	Default	R/W	Description
15 - 14	00	RO	Reserved
13 - 0	0x0000	RW	**Trigger Output Unit 1Target Time in Nanoseconds High-Word [29:16]** This is high-word of target time for trigger output unit 1 in nanoseconds.

4.2.27.10 Trigger Output Unit 1 Target Time in Seconds Low-Word Register (0x224 – 0x225): TRIG1_TGT_SL

This register contains the trigger output unit 1 target time in seconds low-word.

TABLE 4-122: TRIGGER OUTPUT UNIT 1 TARGET TIME IN SECONDS LOW-WORD REGISTER (0X224 – 0X225): TRIG1_TGT_SL

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Trigger Output Unit 1Target Time in Seconds Low-Word [15:0]** This is low-word of target time for trigger output unit 1 in seconds.

4.2.27.11 Trigger Output Unit 1 Target Time in Seconds High-Word Register (0x226 – 0x227): TRIG1_TGT_SH

This register contains the trigger output unit 1 target time in seconds high-word.

TABLE 4-123: TRIGGER OUTPUT UNIT 1 TARGET TIME IN SECONDS HIGH-WORD REGISTER (0X226 – 0X227): TRIG1_TGT_SH

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Trigger Output Unit 1 Target Time in Seconds High-Word [31:16]** This is high-word of target time for trigger output unit 1 in seconds.

4.2.27.12 Trigger Output Unit 1 Configuration and Control Register 1 (0x228 – 0x229): TRIG1_CFG_1

This register (1 of 8) contains the trigger output unit 1 configuration and control bits.

TABLE 4-124: TRIGGER OUTPUT UNIT 1 CONFIGURATION AND CONTROL REGISTER 1 (0X228 – 0X229): TRIG1_CFG_1

Bit	Default	R/W	Description
15	0	RW	**Enable This Trigger Output Unit in Cascade Mode** 1 = Enable this trigger output unit in cascade mode. 0 = disable this trigger output unit in cascade mode.

TABLE 4-124: TRIGGER OUTPUT UNIT 1 CONFIGURATION AND CONTROL REGISTER 1 (0X228 – 0X229): TRIG1_CFG_1 (CONTINUED)

Bit	Default	R/W	Description
14	0	RW	**Indicate a Tail Unit for This Trigger Output Unit in Cascade Mode** 1 = This trigger output unit is the last unit of the chain in cascade mode. 0 = This trigger output unit is not the last unit of a chain in cascade mode. **Note:** When this bit is set “0” in all CFG_1 trigger units, and all units are in cascade mode, the iteration count is ignored and it becomes infinite. To stop the infinite loop, set the respective bit[11:0] in TRIG_SW_RST register.
13 - 10	0xF	RW	**Select Upstream Trigger Unit in Cascade Mode** These bits are used to select one of the 12 upstream trigger output units in Cascade mode. **Note:** 0x0 indicates TOU1, and 0xB indicates TOU12. (0xC to 0xF are not used.) For example, if units 1, 2 and 3 (tail unit) are set up in cascade mode, then these 4 bits are set as follows at the three trigger output units: unit 1 is set to 0x2 (indicates TOU3), at unit 2 is set to 0x0 (indicates TOU1) and at unit 3 is to set 0x1 (indicates TOU2).
9	0	RW	**Trigger Now** 1 = Immediately create the trigger output if the trigger target time is less than the system time clock. 0 = Wait for the trigger target time to occur to trigger the event output.
8	0	RW	**Trigger Notify** 1 = Enable reporting both TRIG_DONE and TRIG_ERR status as well as interrupt to host if the interrupt enable bit is set in the TRIG_IE register. 0 = Disable reporting both TRIG_DONE and TRIG_ERR status.
7	0	RO	Reserved
6 - 4	000	RW	**Trigger Output Signal Pattern** This field is used to select the trigger output signal pattern when TRIG_EN = “1” and trigger target time has reached the system time: 000: TRIG_NEG_EDGE - Generates negative edge (from default “H” -> “L” and stays “L”). 001: TRIG_POS_EDGE - Generates positive edge (from default “L” -> “H” and stays “H”). 010: TRIG_NEG_PULSE - Generates negative pulse (from default “H” -> “L” pulse -> “H” and stays “H”). The pulse width is defined in TRIG1_CFG_2 register. 011: TRIG_POS_PULSE - Generates positive pulse (from default “L” -> “H” pulse -> “L” and stays “L”). The pulse width is defined in TRIG1_CFG_2 register. 100: TRIG_NEG_CYCLE - Generates negative periodic signal. The “L” pulse width is defined in TRIG1_CFG_2 register, the cycle width is defined in TRIG1_CFG_3/4 registers and the number of cycles is defined in TRIG1_CFG_5 register (it is an infinite number if this register value is zero). 101: TRIG_POS_CYCLE - Generates positive periodic signal. The “H” pulse width is defined in TRIG1_CFG_2 register, the cycle width is defined in TRIG1_CFG_3/4 registers and the number of cycles is defined in TRIG1_CFG_5 register (it is an infinite number if this register value is zero). 110: TRIG_REG_OUTPUT - Generates an output signal from a 16-bit register. This 16-bit register bit-pattern in TRIG1_CFG_6 is shifted LSB bit first and looped, each bit width is defined in TRIG1_CFG_3/4 registers and total number of bits to shift out is defined in TRIG1_CFG_5 register (it is an infinite number if this register value is zero). 111: Reserved Note: the maximum output clock frequency is up to 12.5 MHz.

TABLE 4-124: TRIGGER OUTPUT UNIT 1 CONFIGURATION AND CONTROL REGISTER 1 (0X228 – 0X229): TRIG1_CFG_1 (CONTINUED)

Bit	Default	R/W	Description
3 - 0	0x0	RW	**Select GPIO[11:0] for This Trigger Output Unit** Associate one of the 12 GPIO pins to this trigger output unit. The trigger output signals are OR'ed together to form a combined signal if multiple trigger output units have selected the same GPIO output pin. 0x0 indicates GPIO0, and 0xB indicates GPIO11. (0xC to 0xF are not used.)

4.2.27.13 Trigger Output Unit 1 Configuration and Control Register 2 (0x22A – 0x22B): TRIG1_CFG_2

This register (2 of 8) contains the trigger output unit 1 configuration and control bits.

TABLE 4-125: TRIGGER OUTPUT UNIT 1 CONFIGURATION AND CONTROL REGISTER 2 (0X22A – 0X22B): TRIG1_CFG_2

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Trigger Output Pulse Width** This number defines the width of the generated pulse or periodic signal from this trigger output unit. Its unit value is equal to 8 ns. For example, the pulse width is 80 ns if this register value is 10 (0xA). **Iteration Count** This number defines the iteration count for register trigger output pattern (TRIG1_CFG_6) in cascade mode when this trigger output unit is the tail unit. For example, 0x0000 = 1 count and 0x000F = 16 counts. It is an infinite number if there is no tail unit in Cascade mode.

4.2.27.14 Trigger Output Unit 1 Configuration and Control Register 3 (0x22C – 0x22D): TRIG1_CFG_3

This register (3 of 8) contains the trigger output Unit 1 configuration and control bits.

TABLE 4-126: TRIGGER OUTPUT UNIT 1 CONFIGURATION AND CONTROL REGISTER 3 (0X22C – 0X22D): TRIG1_CFG_3

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Trigger Output Cycle Width or Bit Width Low-Word [15:0]** To define cycle width for generating periodic signal or to define each bit width in TRIG1_CFG_8. A unit number of value equals to 1 ns. For example, the cycle or bit width is 80 ns if this register value is 80 (0x50) and next register value = 0x0000.

4.2.27.15 Trigger Output Unit 1 Configuration and Control Register 4 (0x22E – 0x22F): TRIG1_CFG_4

This register (4 of 8) contains the trigger output unit 1 configuration and control bits.

TABLE 4-127: TRIGGER OUTPUT UNIT 1 CONFIGURATION AND CONTROL REGISTER 4 (0X22E – 0X22F): TRIG1_CFG_4

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Trigger Output Cycle Width or Bit Width High-Word [31:16]** This number defines the cycle width when generating periodic signals using this trigger output unit. Also, it is used to define each bit width in TRIG1_CFG_8. Each unit is equal to 1 ns.

4.2.27.16 Trigger Output Unit 1 Configuration and Control Register 5 (0x230 – 0x231): TRIG1_CFG_5

This register (5 of 8) contains the trigger output unit 1 configuration and control bits.

TABLE 4-128: TRIGGER OUTPUT UNIT 1 CONFIGURATION AND CONTROL REGISTER 5 (0X230 – 0X231): TRIG1_CFG_5

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Trigger Output Cycle Count** This number defines the quantity of cycles of the periodic signal output by the trigger output unit. Use a value of zero for infinite repetition. Valid for TRIG_NEG_CYCLE and TRIG_POS_CYCLE modes. **Bit Count** This number can define the number of bits that are output when generating output signals from the bit pattern register. It is an infinite number if this register value is zero. Valid for TRIG_REG_OUTPUT mode.

4.2.27.17 Trigger Output Unit 1 Configuration and Control Register 6 (0x232 – 0x233): TRIG1_CFG_6

This register (6 of 8) contains the trigger output unit 1 configuration and control bits.

TABLE 4-129: TRIGGER OUTPUT UNIT 1 CONFIGURATION AND CONTROL REGISTER 6 (0X232 – 0X233): TRIG1_CFG_6

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Trigger Output Unit Bit Pattern** This register is used to define the output bit pattern when the TRIG_REG_OUTPUT mode is selected. **Iteration Count** This register is used as the iteration count for the trigger output unit when the tail unit is in cascade mode but not using register mode. It is the number of cycles programmed in CFG_5 to be output by the trigger output unit. For example, 0x0000 = 1 count, 0x000F = 16 counts. An infinite number of cycles will occur if there is no tail unit in Cascade mode.

4.2.27.18 Trigger Output Unit 1 Configuration and Control Register 7 (0x234 – 0x235): TRIG1_CFG_7

This register (7 of 8) contains the trigger output unit 1 configuration and control bits.

TABLE 4-130: TRIGGER OUTPUT UNIT 1 CONFIGURATION AND CONTROL REGISTER 7 (0X234 – 0X235): TRIG1_CFG_7

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Trigger Output Iteration Cycle Time in Cascade Mode Low-Word [15:0]** The value in this pair of registers defines the iteration cycle time for the trigger output unit in cascade mode. This value will be added to the current trigger target time for establishing the next trigger time for the trigger output unit. A unit number of value equals to 1 ns. For example, the cycle is 800 ns if this register value is 800 (0x320) and next register value = 0x0000. The iteration count (CFG_6) × trigger output cycle count (CFG_5) x waveform cycle time must be less than the iteration cycle time specified in CFG_7 and CFG_8.

4.2.27.19 Trigger Output Unit 1 Configuration and Control Register 8 (0x236 – 0x237): TRIG1_CFG_8

This register (8 of 8) contains the trigger output unit 1 configuration and control bits.

TABLE 4-131: TRIGGER OUTPUT UNIT 1 CONFIGURATION AND CONTROL REGISTER 8 (0X236 – 0X237): TRIG1_CFG_8

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Trigger Output Iteration Cycle Time in Cascade Mode High-Word [31:16]** The value in this pair of registers defines the iteration cycle time for the trigger output unit in cascade mode. This value will be added to the current trigger target time for establishing the next trigger time for the trigger output unit. A unit number of value equals 1 ns.

4.2.27.20 0x238 – 0x23F: Reserved

4.2.27.21 Trigger Output Unit 2 Target Time and Output Configuration/Control Registers (0x240 – 0x257)

These 12 registers contain the trigger output unit 2 target time and configuration/control bits, TRIG2_CFG_[1:8]. See descriptions in Section 4.2.27.8 through Section 4.2.27.19. Note that there is one bit that is different in this set of register bits. It is indicated in the following text.

4.2.27.22 Trigger Output Unit 2 Configuration and Control Register 1 (0x248 – 0x249): TRIG2_CFG_1

This register contains the trigger output unit 2 configuration and control bits.

TABLE 4-132: TRIGGER OUTPUT UNIT 2 CONFIGURATION AND CONTROL REGISTER 1 (0X248 – 0X249): TRIG2_CFG_1

Bit	Default	R/W	Description
7	0	RW	**Trigger Unit 2 Clock Edge Output Select** This bit is used to select either the positive edge or negative edge of the 125 MHz to clock out the trigger unit 2 output. This bit only pertains to usage with GPIO1 pin. This bit will not function with any other GPIO pin. 1 = Use negative edge of 125 MHz clock to clock out data 0 = Use positive edge of 125 MHz clock to clock out data

4.2.27.23 0x258 – 0x25F: Reserved

4.2.27.24 Trigger Output Unit 3 Target Time and Output Configuration/Control Registers (0x260 – 0x277)

These 12 registers contain the trigger output unit 3 target time and configuration/control bits, TRIG3_CFG_[1:8]. See descriptions in Section 4.2.27.8 through Section 4.2.27.19.

4.2.27.25 0x278 – 0x27F: Reserved

4.2.27.26 Trigger Output Unit 4 Target Time and Output Configuration/Control Registers (0x280 – 0x297)

These 12 registers contain the trigger output unit 4 target time and configuration/control bits, TRIG4_CFG_[1:8]. See descriptions in Section 4.2.27.8 through Section 4.2.27.19.

4.2.27.27 0x298 – 0x29F: Reserved

4.2.27.28 Trigger Output Unit 5 Target Time and Output Configuration/Control Registers (0x2A0 – 0x2B7)

These 12 registers contain the trigger output unit 5 target time and configuration/control bits, TRIG5_CFG_[1:8]. See descriptions in Section 4.2.27.8 through Section 4.2.27.19.

4.2.27.29 0x2B8 – 0x2BF: Reserved

4.2.27.30 Trigger Output Unit 6 Target Time and Output Configuration/Control Registers (0x2C0 – 0x2D7)

These 12 registers contain the trigger output unit 6 target time and configuration/control bits, TRIG6_CFG_[1:8]. See descriptions in Section 4.2.27.8 through Section 4.2.27.19.

4.2.27.31 0x2D8 – 0x2DF: Reserved

4.2.27.32 Trigger Output Unit 7 Target Time and Output Configuration/Control Registers (0x2E0 – 0x2F7)

These 12 registers contain the trigger output unit 7 target time and configuration/control bits, TRIG7_CFG_[1:8]. See descriptions in Section 4.2.27.8 through Section 4.2.27.19.

4.2.27.33 0x2F8 – 0x2FF: Reserved

4.2.27.34 Trigger Output Unit 8 Target Time and Output Configuration/Control Registers (0x300 – 0x317)

These 12 registers contain the trigger output unit 8 target time and configuration/control bits, TRIG8_CFG_[1:8]. See descriptions in Section 4.2.27.8 through Section 4.2.27.19.

4.2.27.35 0x318 – 0x31F: Reserved

4.2.27.36 Trigger Output Unit 9 Target Time and Output Configuration/Control Registers (0x320 – 0x337)

These 12 registers contain the trigger output unit 9 target time and configuration/control bits, TRIG9_CFG_[1:8]. See descriptions in Section 4.2.27.8 through Section 4.2.27.19.

4.2.27.37 0x338 – 0x33F: Reserved

4.2.27.38 Trigger Output Unit 10 Target Time and Output Configuration/Control Registers (0x340 – 0x357)

These 12 registers contain the trigger output unit 10 target time and configuration/control bits, TRIG10_CFG_[1:8]. See descriptions in Section 4.2.27.8 through Section 4.2.27.19.

4.2.27.39 0x358 – 0x35F: Reserved

4.2.27.40 Trigger Output Unit 11 Target Time and Output Configuration/Control Registers (0x360 – 0x377)

These 12 registers contain the trigger output unit 11 target time and configuration/control bits, TRIG11_CFG_[1:8]. See descriptions in Section 4.2.27.8 through Section 4.2.27.19.

4.2.27.41 0x378 – 0x37F: Reserved

4.2.27.42 Trigger Output Unit 12 Target Time and Output Configuration/Control Registers (0x380 – 0x397)

These 12 registers contain the trigger output unit 12 target time and configuration/control bits, TRIG12_CFG_[1:8]. See descriptions in Section 4.2.27.8 through Section 4.2.27.19.

4.2.27.43 0x398 – 0x3FF: Reserved

4.2.28 INTERNAL I/O REGISTER SPACE MAPPING FOR PTP TIME STAMP INPUTS (12 UNITS, 0X400 – 0X5FF)

4.2.28.1 Time Stamp Ready Register (0x400 – 0x401): TS_RDY

This register contains the PTP time stamp input unit ready-to-read status bits.

TABLE 4-133: TIME STAMP READY REGISTER (0X400 – 0X401): TS_RDY

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 0	0x000	RO	**Time Stamp Input Unit Ready** 1 = This time stamp input unit is ready to read and will generate a time stamp interrupt if PTP_TS_IE = “1”. This bit will clear when TS_EN is disabled. 0 = This time stamp input unit is not ready to read or disabled. There are 12 time stamp units and therefore there is a corresponding time stamp input ready bit for each of the time stamp units, bit[11:0] = unit[12:1].

4.2.28.2 Time Stamp Enable Register (0x402 – 0x403): TS_EN

This register contains the PTP time stamp input unit enable control bits.

TABLE 4-134: TIME STAMP ENABLE REGISTER (0X402 – 0X403): TS_EN

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 0	0x000	RO	**Time Stamp Input Unit Enable** 1 = Enable the selected time stamp input unit. Writing a ”1” to this bit will clear the TS[12:1]_EVENT_DET_CNT. 0 = Disable the selected time stamp input unit. Writing a “0” to this bit will clear the TS_RDY and TS[12:1]_DET_CNT_OVFL. There are 12 time stamp units and therefore there is a corresponding time stamp input unit enable bit for each of the time stamp units, bit[11:0] = unit[12:1].

4.2.28.3 Time Stamp Software Reset Register (0x404 – 0x405): TS_SW_RST

This register contains the PTP time stamp input unit software reset control bits.

TABLE 4-135: TIME STAMP SOFTWARE RESET REGISTER (0X404 – 0X405): TS_SW_RST

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 0	0x000	RW/SC	**Time Stamp Input Unit Software Reset** 1 = Reset the selected time stamp input unit to inactive state and default setting. 0 = The selected time stamp input unit is in normal mode of operation. There are 12 time stamp units and therefore there is a corresponding time stamp input unit software reset bit for each of the time stamp units, bit[11:0] = unit[12:1].

4.2.28.4 0x406 – 0x41F: Reserved

4.2.28.5 Time Stamp Unit 1 Status Register (0x420 – 0x421): TS1_STATUS

This register contains PTP time stamp input unit 1 status.

TABLE 4-136: TIME STAMP UNIT 1 STATUS REGISTER (0X420 – 0X421): TS1_STATUS

Bit	Default	R/W	Description
15 - 4	0x000	RO	Reserved
4 - 1	0x0	RO	**Number of Detected Event Count for Time stamp Input Unit 1 (TS1_EVENT_DET_CNT)** This field is used to report the number of detected events (either rising or falling edge) count. in single mode, it can detect up to 15 events in any single time stamp input unit. In cascade mode, it can detect up to two events in time stamp input units 1-11 or up to 8 events at time stamp input unit 12 as a non-tail unit, and it can detect up to 15 events for any time stamp input unit as a tail unit. Pulses or edges can be detected up to 25 MHz. The pulse width can be measured by the difference between consecutive time stamps in the same time stamp input unit.
0	0	RO	**Number of Detected Event Count Overflow for Time stamp Input Unit 1 (TS1_DET_CNT_OVFL)** 1 = The number of detected event (either rising or falling edge) count has overflowed. In cascade mode, only tail unit will set this bit when overflow is occurred. The TS1_EVENT_DET_CNT will stay at 15 when overflow is occurred. 0 = The number of events (either rising or falling edge) detected count has not overflowed.

4.2.28.6 Time Stamp Unit 1 Configuration and Control Register (0x422 – 0x423): TS1_CFG

This register contains PTP time stamp input unit 1 configuration and control bits.

TABLE 4-137: TIME STAMP UNIT 1 CONFIGURATION AND CONTROL REGISTER (0X422 – 0X423): TS1_CFG

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 8	0x0	RW	**Select GPIO[11:0] for Time stamp Unit 1** This field is used to select one of the 12 GPIO pins to serve this time stamp unit. It is GPIO0 if these bits = “0000” and it is GPIO11 if these bits = “1011” (from “1100” to “1111” are not used).
7	0	RW	**Enable Rising Edge Detection** 1 = Enable rising edge detection. 0 = Disable rising edge detection.
6	0	RW	**Enable Falling Edge Detection** 1 = Enable falling edge detection. 0 = Disable falling edge detection.
5	0	RW	**Select Tail Unit for this Time stamp Unit in Cascade Mode** 1 = This time stamp unit is the last unit of the chain in cascade mode. 0 = This time stamp unit is not the last unit of the chain in cascade mode.
4 - 1	0x0	RW	**Select Upstream Time stamp Done Unit in Cascade Mode** This is used to select one of the 12 upstream time stamps units for done input in cascade mode. For example, if units 1 (head unit), 2 and 3 (tail unit) are set up in cascade mode, then these 4-bits at unit 1 are set to 0x0, at unit 2 are set to 0x1, at unit 3 are set to 0x2.
0	0	RW	**Enable This Time stamp Unit in Cascade Mode** 1 = Enable the selected time stamp input unit in Cascade mode. 0 = Disable the time stamp input unit in Cascade mode.

4.2.28.7 Time Stamp Unit 1 Input 1st Sample Time in Nanoseconds Low-Word Register (0x424 – 0x425): TS1_SMPL1_NSL

This register contains the first sample time in nanoseconds low-word (the resolution of 40 ns) for PTP time stamp unit 1.

TABLE 4-138: TIME STAMP UNIT 1 INPUT 1ST SAMPLE TIME IN NANOSECONDS LOW-WORD REGISTER (0X424 – 0X425): TS1_SMPL1_NSL

Bit	Default	R/W	Description
15 - 0	0x0000	RO	**1st Sample Time in ns Low-Word [15:0] Time stamp Unit 1** This is the low-word of first sample time for time stamp unit 1 in nanoseconds.

4.2.28.8 Time Stamp Unit 1 Input 1st Sample Time in Nanoseconds High-Word Register (0x426 – 0x427): TS1_SMPL1_NSH

This register contains the first sample time in nanoseconds high-word and edge detection status for PTP time stamp unit 1.

TABLE 4-139: TIME STAMP UNIT 1 INPUT 1ST SAMPLE TIME IN NANOSECONDS HIGH-WORD REGISTER (0X426 – 0X427): TS1_SMPL1_NSH

Bit	Default	R/W	Description
15	0	RO	Reserved
14	0	RO	**1st Sample Edge Indication for Time stamp Unit 1** 0 = Indicates the event is a falling edge signal. 1 = Indicates the event is a rising edge signal.
13 - 0	0x0000	RO	**1st Sample Time in ns High-Word [29:16] for Time stamp Unit 1** This is the high-word of first sample time for time stamp unit 1 in nanoseconds.

4.2.28.9 Time Stamp Unit 1 Input 1st Sample Time in Seconds Low-Word Register (0x428 – 0x429): TS1_SMPL1_SL

This register contains the first sample time in seconds low-word for PTP time stamp unit 1.

TABLE 4-140: TIME STAMP UNIT 1 INPUT 1ST SAMPLE TIME IN SECONDS LOW-WORD REGISTER (0X428 – 0X429): TS1_SMPL1_SL

Bit	Default	R/W	Description
15 - 0	0x0000	RO	**1st Sample Time in Seconds Low-Word [15:0] for Time stamp Unit 1** This is the low-word of first sample time for time stamp unit 1 in seconds.

4.2.28.10 Time Stamp Unit 1 Input 1st Sample Time in Seconds High-Word Register (0x42A – 0x42B): TS1_SMPL1_SH

This register contains the first sample time in seconds high-word for PTP time stamp unit 1.

TABLE 4-141: TIME STAMP UNIT 1 INPUT 1ST SAMPLE TIME IN SECONDS HIGH-WORD REGISTER (0X42A – 0X42B): TS1_SMPL1_SH

Bit	Default	R/W	Description
15 - 0	0x0000	RO	**1st Sample Time in Seconds High-Word [31:16] for Time Stamp Unit 1** This is the high-word of first sample time for time stamp unit 1 in seconds.

4.2.28.11 Time Stamp Unit 1 Input 1st Sample Time in Sub-Nanoseconds Register (0x42C – 0x42D): TS1_SMPL1_SUB_NS

This register contains the first sample time in sub-8 nanoseconds (the resolution of 8 ns) for PTP time stamp unit 1.

TABLE 4-142: TIME STAMP UNIT 1 INPUT 1ST SAMPLE TIME IN SUB-NANOSECONDS REGISTER (0X42C – 0X42D): TS1_SMPL1_SUB_NS

Bit	Default	R/W	Description
15 - 3	0x0000	RO	Reserved
2 - 0	000	RO	**1st Sample Time in Sub-8 Nanoseconds for Time stamp Unit 1** These bits indicate one of the 8 ns cycles for the first sample time for time stamp unit 1. 000: 0 ns (sample time at the first 8 ns cycle in 25 MHz/40 ns) 001: 8 ns (sample time at the second 8 ns cycle in 25 MHz/40 ns) 010: 16 ns (sample time at the third 8 ns cycle in 25 MHz/40 ns) 011: 24 ns (sample time at the fourth 8 ns cycle in 25 MHz/40 ns) 100: 32 ns (sample time at the fifth 8 ns cycle in 25 MHz/40 ns) 101-111: NA

4.2.28.12 0x42E – 0x433: Reserved

4.2.28.13 Time Stamp Unit 1 Input 2nd Sample Time in Nanoseconds Low-Word Register (0x434 – 0x435): TS1_SMPL2_NSL

This register contains the second sample time in nanoseconds low-word (the resolution of 40 ns) for PTP time stamp Unit 1.

TABLE 4-143: TIME STAMP UNIT 1 INPUT 2ND SAMPLE TIME IN NANOSECONDS LOW-WORD REGISTER (0X434 – 0X435): TS1_SMPL2_NSL

Bit	Default	R/W	Description
15 - 0	0x0000	RO	**2nd Sample Time in Nanoseconds for Low-Word [15:0] for Time stamp Unit 1** This is the low-word of the 2nd sample time for time stamp unit 1 in nanoseconds.

4.2.28.14 Time stamp Unit 1 Input 2nd Sample Time in Nanoseconds High-Word Register (0x436 – 0x437): TS1_SMPL2_NSH

This register contains the 2nd sample time in nanoseconds high-word and edge detection status for the PTP time stamp unit 1.

TABLE 4-144: TIME STAMP UNIT 1 INPUT 2ND SAMPLE TIME IN NANOSECONDS HIGH-WORD REGISTER (0X436 – 0X437): TS1_SMPL2_NSH

Bit	Default	R/W	Description
15	0	RO	Reserved
14	0	RO	**2nd Sample Edge Indication for Time stamp Unit 1** 0 = Indicates the event is a falling edge signal. 1 = Indicates the event is a rising edge signal.
13 - 0	0x0000	RO	**2nd Sample Time in Nanoseconds High-Word [29:16] for Time stamp Unit 1** This is the high-word of the 2nd sample time for time stamp unit 1 in nanoseconds.

4.2.28.15 Time Stamp Unit 1 Input 2nd Sample Time in Seconds Low-Word Register (0x438 – 0x439): TS1_SMPL2_SL

This register contains the 2nd sample time in seconds low-word for PTP time stamp unit 1.

TABLE 4-145: TIME STAMP UNIT 1 INPUT 2ND SAMPLE TIME IN SECONDS LOW-WORD REGISTER (0X438 – 0X439): TS1_SMPL2_SL

Bit	Default	R/W	Description
15 - 0	0x0000	RO	**2nd Sample Time in Seconds Low-Word [15:0] for Time stamp Unit 1** This is the low-word of the second sample time for time stamp unit 1 in seconds.

4.2.28.16 Time Stamp Unit 1 Input 2nd Sample Time in Seconds High-Word Register (0x43A – 0x43B): TS1_SMPL2_SH

This register contains the 2nd sample time in seconds high-word for PTP time stamp unit 1.

TABLE 4-146: TIME STAMP UNIT 1 INPUT 2ND SAMPLE TIME IN SECONDS HIGH-WORD REGISTER (0X43A – 0X43B): TS1_SMPL2_SH

Bit	Default	R/W	Description
15 - 0	0x0000	RO	**2nd Sample Time in Seconds High-Word [31:16] for Time stamp Unit 1** This is the high-word of the second sample time for time stamp unit 1 in seconds.

4.2.28.17 Time Stamp Unit 1 Input 2nd Sample Time in Sub-Nanoseconds Register (0x43C – 0x43D): TS1_SMPL2_SUB_NS

This register contains the 2nd sample time in sub-8 nanoseconds (the resolution of 8 ns) for PTP time stamp unit 1.

TABLE 4-147: TIME STAMP UNIT 1 INPUT 2ND SAMPLE TIME IN SUB-NANOSECONDS REGISTER (0X43C – 0X43D): TS1_SMPL2_SUB_NS

Bit	Default	R/W	Description
15 - 3	0x0000	RO	Reserved
2 - 0	000	RO	**2nd Sample Time in Sub-8 Nanoseconds for Time stamp Unit 1** These bits indicate one of the 8 ns cycle for the second sample time for time stamp unit 1. 000: 0 ns (sample time at the first 8 ns cycle in 25 MHz/40 ns) 001: 8 ns (sample time at the second 8 ns cycle in 25 MHz/40 ns) 010: 16 ns (sample time at the third 8 ns cycle in 25 MHz/40 ns) 011: 24 ns (sample time at the fourth 8 ns cycle in 25 MHz/40 ns) 100: 32 ns (sample time at the fifth 8 ns cycle in 25 MHz/40 ns) 101-111: NA

4.2.28.18 0x43E – 0x43F: Reserved

4.2.28.19 Time Stamp Unit 2 Status/Configuration/Control and Input 1st Sample Time Registers (0x440 – 0x44D)

These seven registers contain the first sample time and status/configuration/control information for PTP time stamp unit 2. See description in time stamp unit 1 (0x420 – 0x42D).

4.2.28.20 0x44E – 0x453: Reserved

4.2.28.21 Time Stamp Unit 2 Input 2nd Sample Time Registers (0x454 – 0x45D)

These five registers contain the second sample time for PTP time stamp unit 2. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.22 0x45E – 0x45F: Reserved

4.2.28.23 Time Stamp Unit 3 Status/Configuration/Control and Input 1st Sample Time Registers (0x460 – 0x46D)

These seven registers contain the first sample time and status/configuration/control information for PTP time stamp unit 3. See description in time stamp unit 1 (0x420 – 0x42D).

4.2.28.24 0x46E – 0x473: Reserved

4.2.28.25 Time Stamp Unit 3 Input 2nd Sample Time Registers (0x474 – 0x47D)

These five registers contain the 2nd sample time for PTP time stamp unit 3. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.26 0x47E – 0x47F: Reserved

4.2.28.27 Time Stamp Unit 4 Status/Configuration/Control and Input 1st Sample Time Registers (0x480 – 0x48D)

These seven registers contain the1st sample time and status/configuration/control information for PTP time stamp unit 4. See description in time stamp unit 1 (0x420 – 0x42D).

4.2.28.28 0x48E – 0x493: Reserved

4.2.28.29 Time Stamp Unit 4 Input 2nd Sample Time Registers (0x494 – 0x49D)

These five registers contain the 2nd sample time for PTP time stamp unit 4 input. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.30 0x49E – 0x49F: Reserved

4.2.28.31 Time Stamp Unit 5 Status/Configuration/Control and Input 1st Sample Time Registers (0x4A0 – 0x4AD)

These seven registers contain the 1st sample time and status/configuration/control information for PTP time stamp unit 5. See description in time stamp unit 1 (0x420 – 0x42D).

4.2.28.32 0x4AE – 0x4B3: Reserved

4.2.28.33 Time Stamp Unit 5 Input 2nd Sample Time Registers (0x4B4 – 0x4BD)

These five registers contain the 2nd sample time for PTP time stamp unit 5. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.34 0x4BE – 0x4BF: Reserved

4.2.28.35 Time Stamp Unit 6 Status/Configuration/Control and Input 1st Sample Time Registers (0x4C0 – 0x4CD)

These seven registers contain the 1st sample time and status/configuration/control information for PTP time stamp unit 6. See description in time stamp unit 1 (0x420 – 0x42D).

4.2.28.36 0x4CE – 0x4D3: Reserved

4.2.28.37 Time Stamp Unit 6 Input 2nd Sample Time Registers (0x4D4 – 0x4DD)

These five registers contain the 2nd sample time for PTP time stamp unit 6. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.38 0x4DE – 0x4DF: Reserved

4.2.28.39 Time Stamp Unit 7 Status/Configuration/Control and Input 1st Sample Time Registers (0x4E0 – 0x4ED)

These seven registers contain the 1st sample time and status/configuration/control information for PTP time stamp unit 7. See description in time stamp unit 1 (0x420 – 0x42D).

4.2.28.40 0x4EE – 0x4F3: Reserved

4.2.28.41 Time Stamp Unit 7 Input 2nd Sample Time Registers (0x4F4 – 0x4FD)

These five registers contain the 2nd sample time for PTP time stamp unit 7. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.42 0x4FE – 0x4FF: Reserved

4.2.28.43 Time Stamp Unit 8 Status/Configuration/Control and Input 1st Sample Time Registers (0x500 – 0x50D)

These seven registers contain the1st sample time and status/configuration/control information for PTP time stamp unit 8. See description in time stamp unit 1 (0x420 – 0x42D).

4.2.28.44 0x50E – 0x513: Reserved

4.2.28.45 Time Stamp Unit 8 Input 2nd Sample Time Registers (0x514 – 0x51D)

These five registers contain the 2nd sample time for PTP time stamp unit 8. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.46 0x51E – 0x51F: Reserved

4.2.28.47 Time Stamp Unit 9 Status/Configuration/Control and Input 1st Sample Time Registers (0x520 – 0x52D)

These seven registers contain the 1st sample time and status/configuration/control information for PTP time stamp unit 9. See description in time stamp unit 1 (0x420 – 0x42D).

4.2.28.48 0x52E – 0x533: Reserved

4.2.28.49 Time Stamp Unit 9 Input 2nd Sample Time Registers (0x534 – 0x53D)

These five registers contain the 2nd sample time for PTP time stamp unit 9. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.50 0x53E – 0x53F: Reserved

4.2.28.51 Time Stamp Unit 10 Status/Configuration/Control and Input 1st Sample Time Registers (0x540 – 0x54D)

These seven registers contain the 1st sample time and status/configuration/control information for PTP time stamp unit 10. See description in time stamp unit 1 (0x420 – 0x42D).

4.2.28.52 0x54E – 0x553: Reserved

4.2.28.53 Time Stamp Unit 10 Input 2nd Sample Time Registers (0x554 – 0x55D)

These five registers contain the 2nd sample time for PTP time stamp unit 10. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.54 0x55E – 0x55F: Reserved

4.2.28.55 Time Stamp Unit 11 Status/Configuration/Control and Input 1st Sample Time Registers (0x560 – 0x56D)

These seven registers contain the1st sample time and status/configuration/control information for PTP time stamp unit 11. See description in time stamp unit 1 (0x420 – 0x42D).

4.2.28.56 0x56E – 0x573: Reserved

4.2.28.57 Time Stamp Unit 11 Input 2nd Sample Time Registers (0x574 – 0x57D)

These five registers contain the 2nd sample time for PTP time stamp unit 11. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.58 0x57E – 0x57F: Reserved

4.2.28.59 Time Stamp Unit 12 Status/Configuration/Control and Input 1st Sample Time Registers (0x580 – 0x58D)

(**Note:** Time stamp unit 12 has eight sample time registers available)

These seven registers contain the 1st sample time and status/configuration/control information for PTP time stamp unit 12. See description in time stamp unit 1 (0x420 – 0x42D).

4.2.28.60 0x58E – 0x593: Reserved

4.2.28.61 Time Stamp Unit 12 Input 2nd Sample Time Registers (0x594 – 0x59D)

These 5 registers contain the 2nd sample time for PTP time stamp unit 12. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.62 0x59E – 0x5A3: Reserved

4.2.28.63 Time Stamp Unit 12 Input 3rd Sample Time Registers (0x5A4 – 0x5AD)

These 5 registers contain the 3rd sample time for PTP time stamp unit 12. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.64 0x5AE – 0x5B3: Reserved

4.2.28.65 Time Stamp Unit 12 Input 4th Sample Time Registers (0x5B4 – 0x5BD)

These five registers contain the 4th sample time for PTP time stamp unit 12. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.66 0x5BE – 0x5C3: Reserved

4.2.28.67 Time Stamp Unit 12 Input 5th Sample Time Registers (0x5C4 – 0x5CD)

These five registers contain the 5th sample time for PTP time stamp unit 12. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.68 0x5CE – 0x5D3: Reserved

4.2.28.69 Time Stamp Unit 12 Input 6th Sample Time Registers (0x5D4 – 0x5DD)

These five registers contain the 6th sample time for PTP time stamp unit 12. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.70 0x5DE – 0x5E3: Reserved

4.2.28.71 Time Stamp Unit 12 Input 7th Sample Time Registers (0x5E4 – 0x5ED)

These five registers contain the 7th sample time for PTP time stamp unit 12. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.72 0x5EE – 0x5F3: Reserved

4.2.28.73 Time stamp Unit 12 Input 8th Sample Time Registers (0x5F4 – 0x5FD)

These five registers contain the 8th sample time for PTP time stamp unit 12. See description in time stamp unit 1 (0x434 – 0x43D).

4.2.28.74 0x5FE – 0x5FF: Reserved

4.2.29 INTERNAL I/O REGISTERS SPACE MAPPING FOR PTP 1588 CLOCK AND GLOBAL CONTROL (0X600 – 0X7FF)

4.2.29.1 PTP Clock Control Register (0x600 – 0x601): PTP_CLK_CTL

This register contains control of PTP 1588 clock.

TABLE 4-148: PTP CLOCK CONTROL REGISTER (0X600 – 0X601): PTP_CLK_CTL

Bit	Default	R/W	Description
15 - 7	0x000	RO	Reserved
6	0	RW/SC	**Enable Step Adjustment Mode to PTP 1588 Clock (PTP_STEP_ADJ_CLK)** Setting this bit will cause the time value in PTP_RTC_NSH/L registers to be added (PTP_STEP_DIR, bit [5]= “1” or subtracted (PTP_STEP_DIR, bit [5] = “0”) from the system time clock. This bit is self-clearing.
5	0	RW	**Direction Control for Step Adjustment Mode (PTP_STEP_DIR)** 1 = To add the time value in PTP_RTC_NSH/L registers to system time clock. 0 = To subtract the time value in PTP_RTC_NSH/L registers from system time clock.
4	0	RW/SC	**Enable Read PTP 1588 Clock (PTP_READ_CLK)** Setting this bit will cause the device to sample the PTP 1588 clock time value. This time value will be made available for reading through the PTP_RTC_SH/L, PTP_RTC_NSH/L and PTP_RTC_PHASE registers. This bit is self-clearing.
3	0	RW/SC	**Enable Load PTP 1588 Clock for Direct Time Setting Mode (PTP_LOAD_CLK)** Setting this bit will cause the device to load the PTP 1588 clock time value from PTP_RTC_SH/L, PTP_RTC_NSH/L and PTP_RTC_PHASE registers. The writes to PTP_RTC_SH/L, PTP_RTC_NSH/L and PTP_RTC_PHASE are performed before setting this bit. This bit is self-clearing.
2	0	RW	**Enable Continuous Adjustment Mode for PTP 1588 Clock (PTP_CONTINU_ADJ_CLK)** 1 = Enable continuous incrementing (PTP_RATE_DIR = “0”) or decrementing (PTP_RATE_DIR = “1”) frequency adjustment by the value in PTP_SNS_RATE_H [29:16] and PTP_SNS_RATE_L [15:0] on every 25 MHz clock cycle. 0 = Disable continuous adjustment mode to PTP 1588 clock.
1	1	RW	**Enable PTP 1588 Clock (EN_PTP_CLK)** 1 = To enable the PTP clock. 0 = To disable the PTP clock and the PTP clock will be frozen. For non-PTP mode, this bit is set to “0” for stopping clock toggling.
0	0	RW/SC	**Reset PTP 1588 Clock (RESET_PTP _CLK)** Setting this bit will reset the PTP 1588 clock.

4.2.29.2 0x602 – 0x603: Reserved

4.2.29.3 PTP Real Time Clock in Nanoseconds Low-Word Register (0x604 – 0x605): PTP_RTC_NSL

This register contains the PTP real time clock in nanoseconds low-word.

TABLE 4-149: PTP REAL TIME CLOCK IN NANOSECONDS LOW-WORD REGISTER (0X604 – 0X605): PTP_RTC_NSL

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Real Time Clock in Nanoseconds Low-Word [15:0]** This is low-word of the PTP real time clock in nanoseconds.

4.2.29.4 PTP Real Time Clock in Nanoseconds High-Word Register (0x606 – 0x607): PTP_RTC_NSH

This register contains the PTP real time clock in nanoseconds high-word.

TABLE 4-150: PTP REAL TIME CLOCK IN NANOSECONDS HIGH-WORD REGISTER (0X606 – 0X607): PTP_RTC_NSH

Bit	Default	R/W	Description
15 - 14	00	RW	Upper two bits in counter not used.
13 - 0	0x0000	RW	**PTP Real Time Clock in Nanoseconds High-Word [29:16]** This is high-word of the PTP real time clock in nanoseconds.

4.2.29.5 PTP Real Time Clock in Seconds Low-Word Register (0x608 – 0x609): PTP_RTC_SL

This register contains the PTP real time clock in seconds low-word.

TABLE 4-151: PTP REAL TIME CLOCK IN SECONDS LOW-WORD REGISTER (0X608 – 0X609): PTP_RTC_SL

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Real Time Clock in Seconds Low-Word [15:0]** This is low-word of the PTP real time clock in seconds.

4.2.29.6 PTP Real Time Clock in Seconds High-Word Register (0x60A – 0x60B): PTP_RTC_SH

This register contains the PTP real time clock in seconds high-word.

TABLE 4-152: PTP REAL TIME CLOCK IN SECONDS HIGH-WORD REGISTER (0X60A – 0X60B): PTP_RTC_SH

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Real Time Clock in Seconds High-Word [31:16]** This is high-word of the PTP real time clock in seconds.

4.2.29.7 PTP Real Time Clock in Phase Register (0x60C – 0x60D): PTP_RTC_PHASE

This register indicates which sub-phase of the PTP real time clock is current. The resolution is 8 ns. The PTP real time clock is updated every 40 ns.

TABLE 4-153: PTP REAL TIME CLOCK IN PHASE REGISTER (0X60C – 0X60D): PTP_RTC_PHASE

Bit	Default	R/W	Description
15 - 3	0x0000	RO	Reserved

TABLE 4-153: PTP REAL TIME CLOCK IN PHASE REGISTER (0X60C – 0X60D): PTP_RTC_PHASE

Bit	Default	R/W	Description
2 - 0	000	RW	**PTP Real Time Clock in Sub 8ns Phase** These bits indicate one of the 8ns sub-cycle times of the 40 ns period PTP real time clock. 000: 0 ns (real time clock at the first 8 ns cycle in 25 MHz/40 ns) 001: 8 ns (real time clock at the second 8 ns cycle in 25 MHz/40 ns) 010: 16 ns (real time clock at the third 8 ns cycle in 25 MHz/40 ns) 011: 24 ns (real time clock at the fourth 8 ns cycle in 25 MHz/40 ns) 100: 32 ns (real time clock at the fifth 8 ns cycle in 25 MHz/40 ns) 101-111: NA This register is set to zero whenever the PTP_RTC_NSL, PTP_RTC_NSH, PTP_RTC_SL, PTP_RTC_SH registers are written to by the CPU.

4.2.29.8 0x60E – 0x60F: Reserved

4.2.29.9 PTP Rate in Sub-Nanoseconds Low-Word Register (0x610 – 0x611): PTP_SNS_RATE_L

This register contains the PTP rate control in sub-nanoseconds low-word.

TABLE 4-154: PTP RATE IN SUB-NANOSECONDS LOW-WORD REGISTER (0X610 – 0X611): PTP_SNS_RATE_L

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Rate Control in Sub-Nanoseconds Low-Word [15:0]** This is low-word of PTP rate control value in units of 2^{-32} ns. The PTP rate control value is used for incrementing (PTP_RATE_DIR = “0”) or decrementing (PTP_RATE_DIR = “1”) the frequency adjustment by the value in PTP_SNS_RATE_H [29:16] and PTP_SNS_RATE_L [15:0] per reference clock cycle (40 ns). On each reference clock cycle, the PTP clock will be adjusted REF_CLK_PERIOD ±PTP_SNS_RATE_H/L value. Setting both PTP_SNS_RATE_H/L registers value to “0x0” will disable both continuous and temporary adjustment modes.

4.2.29.10 PTP Rate in Sub-Nanoseconds High-Word and Control Register (0x612 – 0x613): PTP_SNS_RATE_H

This register contains the PTP rate control in sub-nanoseconds high-word and configuration.

TABLE 4-155: PTP RATE IN SUB-NANOSECONDS HIGH-WORD AND CONTROL REGISTER (0X612 – 0X613): PTP_SNS_RATE_H

Bit	Default	R/W	Description
15	0	RW	**Rate Direction Control for Temporary or Continuous Adjustment Mode (PTP_RATE_DIR)** 1 = Lower frequency. The PTP_SNS_RATE_H/L value will be added to system time clock on every 25 MHz clock cycle. 0 = Higher frequency. The PTP_SNS_RATE_H/L value will be subtracted from system time clock on every 25 MHz clock cycle.
14	0	RW/SC	**Enable Temporary Adjustment Mode for PTP 1588 Clock (PTP_TEMP_ADJ_CLK)** 1 = Enable the temporary incrementing (PTP_RATE_DIR = “0”) or decrementing (PTP_RATE_DIR = “1”) frequency adjustment by the value in the PTP_SNS_RATE_H/L registers over the duration of time set in the PTP_ADJ_DURA_H/L registers on every 25 MHz clock cycle. This bit is self-cleared when the adjustment is completed. Software can read this bit to check whether the adjustment is still in progress. 0 = Disable the temporary adjustment mode to the PTP clock.

TABLE 4-155: PTP RATE IN SUB-NANOSECONDS HIGH-WORD AND CONTROL REGISTER (0X612 – 0X613): PTP_SNS_RATE_H (CONTINUED)

Bit	Default	R/W	Description
13 - 0	0x0000	RW	**PTP Rate Control in Sub-Nanoseconds High-Word [29:16] (PTP_SNS_RATE_H[29:16])** This is high-word of PTP rate control value in units of 2^{-32} ns. The PTP rate control value is used for incrementing (PTP_RATE_DIR = "0") or decrementing (PTP_RATE_DIR = "1") the frequency adjustment by the value in PTP_SNS_RATE_H [29:16] and PTP_SNS_RATE_L [15:0] per reference clock cycle (40 ns). On each reference clock cycle, the PTP clock will be adjusted by a REF_CLK_PERIOD ±PTP_SNS_RATE_H/L value. Setting both PTP_SNS_RATE_H/L registers value to "0x0" will disable both continuous and temporary adjustment modes.

4.2.29.11 PTP Temporary Adjustment Mode Duration in Low-Word Register (0x614 – 0x615): PTP_TEMP_ADJ_DURA_L

This register contains the PTP temporary rate adjustment duration in low-word.

TABLE 4-156: PTP TEMPORARY ADJUSTMENT MODE DURATION IN LOW-WORD REGISTER (0X614 – 0X615): PTP_TEMP_ADJ_DURA_L

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Temporary Rate Adjustment Duration in Low-Word [15:0]** This register is used to set the duration for the temporary rate adjustment in number of 25 MHz clock cycles.

4.2.29.12 PTP Temporary Adjustment Mode Duration in High-Word Register (0x616 – 0x617): PTP_TEMP_ADJ_DURA_H

This register contains the PTP temporary rate adjustment duration in high-word.

TABLE 4-157: PTP TEMPORARY ADJUSTMENT MODE DURATION IN HIGH-WORD REGISTER (0X616 – 0X617): PTP_TEMP_ADJ_DURA_H

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Temporary Rate Adjustment Duration in High-Word [31:16]** This register is used to set the duration for the temporary rate adjustment in number of 25 MHz clock cycles.

4.2.29.13 0x618 – 0x61F: Reserved

4.2.29.14 PTP Message Configuration 1 Register (0x620 – 0x621): PTP_MSG_CFG_1

This register contains the PTP message configuration 1.

TABLE 4-158: PTP MESSAGE CONFIGURATION 1 REGISTER (0X620 – 0X621): PTP_MSG_CFG_1

Bit	Default	R/W	Description
15 - 8	0x00	RO	Reserved
7	0	RW	**Enable IEEE 802.1AS Mode** Setting this bit will enable the IEEE 802.1AS mode and all PTP packets are forwarded to port 3.
6	1	RW	**Enable IEEE 1588 PTP Mode** 1 = To enable the IEEE 1588 PTP mode. 0 = To disable the IEEE 1588 PTP mode.
5	0	RW	**Enable Detection of IEEE 802.3 Ethernet PTP Message** 1 = Enable to detect the Ethernet PTP message. 0 = Disable to detect the Ethernet PTP message.

TABLE 4-158: PTP MESSAGE CONFIGURATION 1 REGISTER (0X620 – 0X621): PTP_MSG_CFG_1

Bit	Default	R/W	Description
4	1	RW	**Enable Detection of IPv4/UDP PTP Message** 1 = Enable to detect the IPv4/UDP PTP message. 0 = Disable to detect the IPv4/UDP PTP message.
3	1	RW	**Enable Detection of IPv6/UDP PTP Message** 1 = Enable to detect the IPv6/UDP PTP message. 0 = Disable to detect the IPv6/UDP PTP message.
2	0	RW	**Selection of P2P or E2E** 1 = Select Peer-to-Peer (P2P) transparent clock mode. 0 = Select End-to-End (E2E) transparent clock mode.
1	0	RW	**Selection of Master or Slave** 1 = Select port 3 as master in ordinary clock mode. 0 = Select port 3 as slave in ordinary clock mode.
0	1	RW	**Selection of One-step or Two-Step Operation** 1 = Select one-step clock mode. 0 = Select two-step clock mode.

4.2.29.15 PTP Message Configuration 2 Register (0x622 – 0x623): PTP_MSG_CFG_2

This register contains the PTP message configuration 2.

TABLE 4-159: PTP MESSAGE CONFIGURATION 2 REGISTER (0X622 – 0X623): PTP_MSG_CFG_2

Bit	Default	R/W	Description
15 - 13	000	RO	Reserved
12	0	RW	**Enable Unicast PTP** 1 = The Unicast PTP packet can be recognized. If the packet UDP destination port is either 319 or 320 and the packet MAC/IP address is not the PTP reserved address, then the packet will be considered as Unicast PTP packet and the packet forwarding will be decided by regular table lookup. 0 = Only multicast PTP packet will be recognized.
11	0	RW	**Enable Alternate Master** 1 = Alternate master clock is supported. The Sync, Follow_Up, Delay_Req, and Delay_Resp messages of the same domain received at port 1/port 2 by active master clock of same domain will be forwarded to port 2/port 1. 0 = Alternate master clock is not supported. The Sync message will not be forwarded to the other port when this bit = “0”. The Delay_Req message of same domain received at port 1/port 2 by active master clock of same domain will be discarded on port 3 and be forwarded to port 2/port 1 if Delay_Req is for other domains.
10	1	RW	**PTP Messages Priority TX Queue** 1 = All PTP messages are assigned to highest priority TX queue. 0 = Only the PTP event messages are assigned to highest priority TX queue.
9	0	RW	**Enable Checking of Associated Sync and Follow_Up PTP Messages** Setting this bit will associate Follow_Up message with Sync message under certain situations. This bit only applies to PTP frames on port 3.

TABLE 4-159: PTP MESSAGE CONFIGURATION 2 REGISTER (0X622 – 0X623): PTP_MSG_CFG_2

Bit	Default	R/W	Description
8	0	RW	**Enable Checking of Associated Delay_Req and Delay_Resp PTP Messages** While this bit is set, the Delay_Resp message will be forwarded to port 1/ port 2 if the associations do not match and is forwarded to port 3 if the associations match. Setting this bit will associate Delay_Resp message with Delay_Req message when it has the same domain, sequenceID, and sourceportID. The PTP frame will be forwarded to port 3 if the ID matches.
7	0	RW	**Enable Checking of Associated Pdelay_Req and Pdelay_Resp PTP Messages** Setting this bit will associate Pdelay_Resp/Pdelay_Resp_Follow_Up messages with Pdelay_Req message when it has the same domain, sequenceID, and sourceportID. The PTP frame will be forwarded to port 3 if the ID matches. This bit only applies to PTP frames on port 3.
6	0	RO	Reserved
5	0	RW	Reserved
4	0	RW	**Enable Checking of Domain Field: DOMAIN_EN** Setting this DOMAIN_EN bit will enable the device to automatically check the domain field in PTP message with the PTP_DOMAIN_VER[7:0]. The PTP message will be forwarded to port 3 if the domain field is matched to PTP_DOMAIN_VER[7:0] otherwise the PTP message will be dropped. If set this bit to “0”, regardless of domain field, PTP messages are always forwarded to port 3 according to hardware default rules.
3	0	RO	Reserved
2	1	RW	**Enable the IPv4/UDP Checksum Calculation for Egress Packets** 1 = The device will re-calculate and generate a 2-byte checksum value due to a frame contents change. 0 = The checksum field is set to zero. If the IPv4/UDP checksum is zero, the checksum will remain zero regardless of this bit setting. For IPv6/UDP, the checksum is always updated.
1	0	RW	**Announce Message from Port 1** 1 = The Announce message is received from port 1 direction. 0 = The Announce message is not received from port 1 direction.
0	0	RW	**Announce Message from Port 2** 1 = The Announce message is received from port 2 direction. 0 = The Announce message is not received from port 2 direction.

4.2.29.16 PTP Domain and Version Register (0x624 – 0x625): PTP_DOMAIN_VER

This register contains the PTP Domain and Version Information.

TABLE 4-160: PTP DOMAIN AND VERSION REGISTER (0X624 – 0X625): PTP_DOMAIN_VER

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 8	0x2	RW	**PTP Version** This is the value of PTP message version number field. All PTP packets will be captured when the receive PTP message version matches the value in this field. All PTP packets will be dropped if the receive PTP message version does not match the value in this field. Except for the value of version 1, the device is always forwarding PTP packets between port 1 and port 2, and not to port 3.

TABLE 4-160: PTP DOMAIN AND VERSION REGISTER (0X624 – 0X625): PTP_DOMAIN_VER

Bit	Default	R/W	Description
7 - 0	0x00	RW	**PTP Domain** This is the value of the PTP message domain number field. If the DOMAIN_EN bit is set to “1”, the PTP messages will be filtered out and only forwarded to port 3 if the domain number matches. If the DOMAIN_EN bit is set to “0”, the domain number field will be ignored under certain circumstances.

4.2.29.17 0x626 – 0x63F: Reserved

4.2.29.18 PTP Port 1 Receive Latency Register (0x640 – 0x641): PTP_P1_RX_LATENCY

This register contains the PTP port 1 receive latency value in nanoseconds.

TABLE 4-161: PTP PORT 1 RECEIVE LATENCY REGISTER (0X640 – 0X641): PTP_P1_RX_LATENCY

Bit	Default	R/W	Description
15 - 0	0x019F	RW	**PTP Port 1 RX Latency in Nanoseconds [15:0]** This register is used to set the fixed receive delay value from port 1 wire to RX time stamp reference point. The default value is 415 ns.

4.2.29.19 PTP Port 1 Transmit Latency Register (0x642 – 0x643): PTP_P1_TX_LATENCY

This register contains the PTP port 1 transmit latency value in nanoseconds.

TABLE 4-162: PTP PORT 1 TRANSMIT LATENCY REGISTER (0X642 – 0X643): PTP_P1_TX_LATENCY

Bit	Default	R/W	Description
15 - 0	0x002D	RW	**PTP Port 1 TX Latency in Nanoseconds [15:0]** This register is used to set the fixed transmit delay value from port 1 TX time stamp reference point to wire. The default value is 45 ns.

4.2.29.20 PTP Port 1 Asymmetry Correction Register (0x644 – 0x645): PTP_P1_ASYM_COR

This register contains the PTP port 1 asymmetry correction value in nanoseconds.

TABLE 4-163: PTP PORT 1 ASYMMETRY CORRECTION REGISTER (0X644 – 0X645): PTP_P1_ASYM_COR

Bit	Default	R/W	Description
15	0	RW	**PTP Port 1 Asymmetry Correction Sign Bit** 1 = The magnitude in bit[14:0] is negative. 0 = The magnitude in bit[14:0] is positive.
14 - 0	0x0000	RW	**PTP Port 1 Asymmetry Correction in Nanoseconds [14:0]** This register is used to set the fixed asymmetry value to add in the correction field for ingress Sync and Pdelay_Resp or to subtract from correction field for egress Delay_Req and Pdelay_Req.

4.2.29.21 PTP Port 1 Link Delay Register (0x646 – 0x647): PTP_P1_LINK_DLY

This register contains the PTP port 1 link delay in nanoseconds.

TABLE 4-164: PTP PORT 1 LINK DELAY REGISTER (0X646 – 0X647): PTP_P1_LINK_DLY

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Port 1 Link Delay in Nanoseconds [15:0]** This register is used to set the link delay value between port 1 and link partner port.

4.2.29.22 PTP Port 1 Egress Time stamp Low-Word Register for Pdelay_Req and Delay_Req (0x648 – 0x649): P1_XDLY_REQ_TSL

This register contains the PTP port 1 egress time stamp low-word value for Pdelay_Req and Delay_Req frames in nanoseconds.

TABLE 4-165: PTP PORT 1 EGRESS TIME STAMP LOW-WORD REGISTER FOR PDELAY_REQ AND DELAY_REQ (0X648 – 0X649): P1_XDLY_REQ_TSL

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Port 1 Egress Time stamp for Pdelay_Req and Delay_Req in Nanoseconds [15:0]** This register contains port 1 egress time stamp low-word value for Pdelay_Req and Delay_Req frames in nanoseconds.

4.2.29.23 PTP Port 1 Egress Time stamp High-Word Register for Pdelay_Req and Delay_Req (0x64A – 0x64B): P1_XDLY_REQ_TSH

This register contains the PTP port 1 egress time stamp high-word value for Pdelay_Req and Delay_Req frames in nanoseconds.

TABLE 4-166: PTP PORT 1 EGRESS TIME STAMP HIGH-WORD REGISTER FOR PDELAY_REQ AND DELAY_REQ (0X64A – 0X64B): P1_XDLY_REQ_TSH

Bit	Default	R/W	Description
15 - 14	00	RW	**PTP Port 1 Egress Time stamp for Pdelay_Req and Delay_Req in Seconds [1:0]** These bits are bits [1:0] of the port 1 egress time stamp value for Pdelay_Req and Delay_Req frames in seconds.
13 - 0	0x0000	RW	**PTP Port 1 Egress Time stamp for Pdelay_Req and Delay_Req in Nanoseconds [29:16]** These bits are bits [29:16] of the port 1 egress time stamp value for Pdelay_Req and Delay_Req frames in nanoseconds.

4.2.29.24 PTP Port 1 Egress Time stamp Low-Word Register for Sync (0x64C – 0x64D): P1_SYNC_TSL

This register contains the PTP port 1 egress time stamp low-word value for Sync frame in nanoseconds.

TABLE 4-167: PTP PORT 1 EGRESS TIME STAMP LOW-WORD REGISTER FOR SYNC (0X64C – 0X64D): P1_SYNC_TSL

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Port 1 Egress Time stamp for Sync in Nanoseconds [15:0]** This register contains port 1 egress time stamp low-word value for Sync frame in nanoseconds.

4.2.29.25 PTP Port 1 Egress Time stamp High-Word Register for Sync (0x64E – 0x64F): P1_SYNC_TSH

This register contains the PTP port 1 egress time stamp high-word value for Sync frame in nanoseconds.

TABLE 4-168: PTP PORT 1 EGRESS TIME STAMP HIGH-WORD REGISTER FOR SYNC (0X64E – 0X64F): P1_SYNC_TSH

Bit	Default	R/W	Description
15 - 14	00	RW	**PTP Port 1 Egress Time stamp for Sync in Seconds [1:0]** These bits are bits [1:0] of the port 1 egress time stamp value for Sync frame in seconds.
13 - 0	0x0000	RW	**PTP Port 1 Egress Time stamp for Sync in Nanoseconds [29:16]** These bits are bits [29:16] of the Port 1 egress time stamp value for Sync frame in nanoseconds.

4.2.29.26 PTP Port 1 Egress Time stamp Low-Word Register for Pdelay_Resp (0x650 – 0x651): P1_PDLY_RESP_TSL

This register contains the PTP port 1 egress time stamp low-word value for Pdelay_Resp frame in nanoseconds.

TABLE 4-169: PTP PORT 1 EGRESS TIME STAMP LOW-WORD REGISTER FOR PDELAY_RESP (0X650 – 0X651): P1_PDLY_RESP_TSL

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Port 1 Egress Time stamp for Pdelay_Resp in Nanoseconds [15:0]** This register contains port 1 egress time stamp low-word value for Pdelay_Resp frame in nanoseconds.

4.2.29.27 PTP Port 1 Egress Time stamp High-Word Register for Pdelay_Resp (0x652 – 0x653): P1_PDLY_RESP_TSH

This register contains the PTP port 1 egress time stamp high-word value for Pdelay_Resp frame in nanoseconds.

TABLE 4-170: PTP PORT 1 EGRESS TIME STAMP HIGH-WORD REGISTER FOR PDELAY_RESP (0X652 – 0X653): P1_PDLY_RESP_TSH

Bit	Default	R/W	Description
15 - 14	00	RW	**PTP Port 1 Egress Time stamp for Pdelay_Resp in Seconds [1:0]** These bits are bits [1:0] of the port 1 egress time stamp value for Pdelay_Resp frame in seconds.
13 - 0	0x0000	RW	**PTP Port 1 Egress Time stamp for Pdelay_Resp in Nanoseconds [29:16]** These bits are bits [29:16] of the port 1 egress time stamp high-word value for Pdelay_Resp frame in nanoseconds.

4.2.29.28 0x654 – 0x65F: Reserved

4.2.29.29 PTP Port 2 Receive Latency Register (0x660 – 0x661): PTP_P2_RX_LATENCY

This register contains the PTP port 2 receive latency value in nanoseconds.

TABLE 4-171: PTP PORT 2 RECEIVE LATENCY REGISTER (0X660 – 0X661): PTP_P2_RX_LATENCY

Bit	Default	R/W	Description
15 - 0	0x019F	RW	**PTP Port 2 RX Latency in Nanoseconds [15:0]** This register is used to set the fixed receive delay value from port 2 wire to the RX time stamp reference point. The default value is 415 ns.

4.2.29.30 PTP Port 2 Transmit Latency Register (0x662 – 0x663): PTP_P2_TX_LATENCY

This register contains the PTP port 2 transmit latency value in nanoseconds.

TABLE 4-172: PTP PORT 2 TRANSMIT LATENCY REGISTER (0X662 – 0X663): PTP_P2_TX_LATENCY

Bit	Default	R/W	Description
15 - 0	0x002D	RW	**PTP Port 2 TX Latency in Nanoseconds [15:0]** This register is used to set the fixed transmit delay value from port 2 TX time stamp reference point to the wire. The default value is 45 ns.

4.2.29.31 PTP Port 2 Asymmetry Correction Register (0x664 – 0x665): PTP_P2_ASYM_COR

This register contains the PTP port 2 asymmetry correction value in nanoseconds.

TABLE 4-173: PTP PORT 2 ASYMMETRY CORRECTION REGISTER (0X664 – 0X665): PTP_P2_ASYM_COR

Bit	Default	R/W	Description
15	0	RW	**PTP Port 2 Asymmetry Correction Sign Bit** 1 = The magnitude in bit[14:0] is negative. 0 = The magnitude in bit[14:0] is positive.
14 - 0	0x0000	RW	**PTP Port 2 Asymmetry Correction in Nanoseconds [14:0]** This register is used to set the fixed asymmetry value to add in the correction field for ingress Sync and Pdelay_Resp or to subtract from correction field for egress Delay_Req and Pdelay_Req.

4.2.29.32 PTP Port 2 Link Delay Register (0x666 – 0x667): PTP_P2_LINK_DLY

This register contains the PTP port 2 link delay in nanoseconds.

TABLE 4-174: PTP PORT 2 LINK DELAY REGISTER (0X666 – 0X667): PTP_P2_LINK_DLY

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Port 2 Link Delay in Nanoseconds [15:0]** This register is used to set the link delay value between port 2 and link partner port.

4.2.29.33 PTP Port 2 Egress Time stamp Low-Word Register for Pdelay_Req and Delay_Req (0x668 – 0x669): P2_XDLY_REQ_TSL

This register contains the PTP port 2 egress time stamp low-word value for Pdelay_Req and Delay_Req frames in nanoseconds.

TABLE 4-175: PTP PORT 2 EGRESS TIME STAMP LOW-WORD REGISTER FOR PDELAY_REQ AND DELAY_REQ (0X668 – 0X669): P2_XDLY_REQ_TSL

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Port 2 Egress Time stamp for Pdelay_Req and Delay_Req in Nanoseconds [15:0]** This register contains port 2 egress time stamp low-word value for Pdelay_Req and Delay_Req frames in nanoseconds.

4.2.29.34 PTP Port 2 Egress Time stamp High-Word Register for Pdelay_Req and Delay_Req (0x66A – 0x66B): P2_XDLY_REQ_TSH

This register contains the PTP port 2 egress time stamp high-word value for Pdelay_Req and Delay_Req frames in nanoseconds.

TABLE 4-176: PTP PORT 2 EGRESS TIME STAMP HIGH-WORD REGISTER FOR PDELAY_REQ AND DELAY_REQ (0X66A – 0X66B): P2_XDLY_REQ_TSH

Bit	Default	R/W	Description
15 - 14	00	RW	**PTP Port 2 Egress Time stamp for Pdelay_Req and Delay_Req in Seconds [1:0]** These are bits [1:0] of the port 2 egress time stamp value for Pdelay_Req and Delay_Req frames in seconds.
13 - 0	0x0000	RW	**PTP Port 2 Egress Time stamp for Pdelay_Req and Delay_Req in Nanoseconds [29:16]** These are bits [29:16] of the port 2 egress time stamp value for Pdelay_Req and Delay_Req frames in nanoseconds.

4.2.29.35 PTP Port 2 Egress Time stamp Low-Word Register for Sync (0x66C – 0x66D): P2_SYNC_TSL

This register contains the PTP port 2 egress time stamp low-word value for Sync frame in nanoseconds.

TABLE 4-177: PTP PORT 2 EGRESS TIME STAMP LOW-WORD REGISTER FOR SYNC (0X66C – 0X66D): P2_SYNC_TSL

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Port 2 Egress Time stamp for Sync in Nanoseconds [15:0]** This register contains port 2 egress time stamp low-word value for Sync frame in nanoseconds.

4.2.29.36 PTP Port 2 Egress Time stamp High-Word Register for Sync (0x66E – 0x66F): P2_SYNC_TSH

This register contains the PTP port 2 egress time stamp high-word value for Sync frame in nanoseconds.

TABLE 4-178: PTP PORT 2 EGRESS TIME STAMP HIGH-WORD REGISTER FOR SYNC (0X66E – 0X66F): P2_SYNC_TSH

Bit	Default	R/W	Description
15 - 14	00	RW	**PTP Port 2 Egress Time stamp for Sync in Seconds [1:0]** These are bits [1:0] of the port 2 egress time stamp value for Sync frame in seconds.
13 - 0	0x0000	RW	**PTP Port 2 Egress Time stamp for Sync Nanoseconds [29:16]** These are bits [29:16] of the port 2 egress time stamp value for Sync frame in nanoseconds.

4.2.29.37 PTP Port 2 Egress Time stamp Low-Word Register for Pdelay_Resp (0x670 – 0x671): P2_PDLY_RESP_TSL

This register contains the PTP port 2 egress time stamp low-word value for Pdelay_Resp frame in nanoseconds.

TABLE 4-179: PTP PORT 2 EGRESS TIME STAMP LOW-WORD REGISTER FOR PDELAY_RESP (0X670 – 0X671): P2_PDLY_RESP_TSL

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Port 2 Egress Time stamp for Pdelay_Resp in Nanoseconds [15:0]** This register contains port 2 egress time stamp low-word value for Pdelay_Resp frame in nanoseconds.

4.2.29.38 PTP Port 2 Egress Time stamp High-Word Register for Pdelay_Resp (0x672 – 0x673): P2_PDLY_RESP_TSH

This register contains the PTP port 2 egress time stamp high-word value for Pdelay_Resp frame in nanoseconds.

TABLE 4-180: PTP PORT 2 EGRESS TIME STAMP HIGH-WORD REGISTER FOR PDELAY_RESP (0X672 – 0X673): P2_PDLY_RESP_TSH

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**PTP Port 2 Egress Time stamp for Pdelay_Resp in Nanoseconds [31:16]** This register contains port 2 egress time stamp high-word value for Pdelay_Resp frame in nanoseconds.

4.2.29.39 0x674 – 0x67F: Reserved

4.2.29.40 GPIO Monitor Register (0x680 – 0x681): GPIO_MONITOR

This register contains read-only access for the current values on GPIO inputs.

TABLE 4-181: GPIO MONITOR REGISTER (0X680 – 0X681): GPIO_MONITOR

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 0	0x000	RO	**GPIO Inputs Monitor** This field reflects the current values seen on the GPIO inputs. GPIOs 11 through 0 are mapped to bits [11:0] in order.

4.2.29.41 GPIO Output Enable Register (0x682 – 0x683): GPIO_OEN

This register contains the control bits for GPIO output enable.

TABLE 4-182: GPIO OUTPUT ENABLE REGISTER (0X682 – 0X683): GPIO_OEN

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 0	0x000	RW	**GPIO Output Enable** 0 = Enables the GPIO pin as trigger output. 1 = Enables the GPIO pin as time stamp input. GPIOs 11 through 0 are mapped to bits [11:0] in order.

4.2.29.42 0x684 – 0x687: Reserved

4.2.29.43 PTP Trigger Unit Interrupt Status Register (0x688 – 0x689): PTP_TRIG_IS

This register contains the interrupt status of PTP event trigger units.

TABLE 4-183: PTP TRIGGER UNIT INTERRUPT STATUS REGISTER (0X688 – 0X689): PTP_TRIG_IS

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 0	0x000	RO (W1C)	**Trigger Output Unit Interrupt Status** When this bit is set to 1, it indicates that the trigger output unit is done or has an error. The trigger output units from 12 to 1 are mapped to bit [11:0]. These 12 trigger output unit interrupt status bits are logical OR'ed together and connected to ISR bit [10]. Any of the interrupt status bits are cleared by writing a "1" to the particular bit.

4.2.29.44 PTP Trigger Unit Interrupt Enable Register (0x68A – 0x68B): PTP_TRIG_IE

This register contains the interrupt enable of PTP trigger output units.

TABLE 4-184: PTP TRIGGER UNIT INTERRUPT ENABLE REGISTER (0X68A – 0X68B): PTP_TRIG_IE

Bit	Default	R/W	Description
15 - 12	0x0	RO	Reserved
11 - 0	0x000	RW	**Trigger Output Unit Interrupt Enable** When this bit is set to "1", it indicates that the trigger output unit interrupt is enabled. The trigger output units from 12 to 1 are mapped to bit [11:0]. These 12 trigger output unit interrupt enables are logical OR'ed together and connected to IER bit [10].

4.2.29.45 PTP Time stamp Unit Interrupt Status Register (0x68C – 0x68D): PTP_TS_IS

This register contains the interrupt status of PTP time stamp units. Each bit in this register is cleared by writing a “1” to it.

TABLE 4-185: PTP TIME STAMP UNIT INTERRUPT STATUS REGISTER (0X68C – 0X68D): PTP_TS_IS

Bit	Default	R/W	Description
15	0	RO (W1C)	**Port 2 Egress Time stamp for Pdelay_Req/Resp and Delay_Req Frames Interrupt Status** When this bit is set to “1”, it indicates that the egress time stamp is available from port 2 for Pdelay_Req/Resp and Delay_Req frames. This bit will be logical OR’ed together with the rest of bits in this register and the logical OR’ed output is connected to ISR bit[12].
14	0	RO (W1C)	**Port 2 Egress Time stamp for Sync Frame Interrupt Status** When this bit is set to “1”, it indicates that the egress time stamp is available from port 2 for Sync frame. This bit will be logical OR’ed together with the rest of bits in this register and the logical OR’ed output is connected to ISR bit[12].
13	0	RO (W1C)	**Port 1 Egress Time stamp for Pdelay_Req/Resp and Delay_Req Frames Interrupt Status** When this bit is set to “1”, it indicates that the egress time stamp is available from port 1 for Pdelay_Req/Resp and Delay_Req frames. This bit will be logical OR’ed together with the rest of bits in this register and the logical OR’ed output is connected to ISR bit[12].
12	0	RO (W1C)	**Port 1 Egress Time stamp for Sync Frame Interrupt Status** When this bit is set to “1”, it indicates that the egress time stamp is available from port 1 for Sync frame. This bit will be logical OR’ed together with the rest of bits in this register and the logical OR’ed output is connected to ISR bit[12].
11 - 0	0x000	RO (W1C)	**Time stamp Unit Interrupt Status** When this bit is set to “1”, it indicates that the time stamp unit is ready (TS_RDY = “1”). The time stamp units from 12 to 1 are mapped to bit [11:0]. These 12 time stamp interrupts status are logical OR’ed together with the rest of bits in this register and the logical OR’ed output is connected to ISR bit[12].

4.2.29.46 PTP Time stamp Unit Interrupt Enable Register (0x68E – 0x68F): PTP_TS_IE

This register contains the interrupt enable of PTP time stamp units.

TABLE 4-186: PTP TIME STAMP UNIT INTERRUPT ENABLE REGISTER (0X68E – 0X68F): PTP_TS_IE

Bit	Default	R/W	Description
15	0	RW	**Port 2 Egress Time stamp for Pdelay_Req/Resp and Delay_Req Frames Interrupt Enable** When this bit is set to “1”, it is enabled the interrupt when the egress time stamp is available from port 2 for Pdelay_Req/Resp and Delay_Req frames. This bit will be logical OR’ed together with the rest of bits in this register and the logical OR’ed output is connected to IER bit[12].
14	0	RW	**Port 2 Egress Time stamp for Sync Frame Interrupt Enable** When this bit is set to “1”, it is enabled the interrupt when the egress time stamp is available from port 2 for Sync frame. This bit will be logical OR’ed together with the rest of bits in this register and the logical OR’ed output is connected to IER bit[12].

TABLE 4-186: PTP TIME STAMP UNIT INTERRUPT ENABLE REGISTER (0X68E – 0X68F): PTP_TS_IE (CONTINUED)

Bit	Default	R/W	Description
13	0	RW	**Port 1 Egress Time stamp for Pdelay_Req/Resp and Delay_Req Frames Interrupt Enable** When this bit is set to “1”, it is enabled the interrupt when the egress time stamp is available from port 1 for Pdelay_Req/Resp and Delay_Req frames. This bit will be logical OR’ed together with the rest of bits in this register and the logical OR’ed output is connected to IER bit[12].
12	0	RW	**Port 1 Egress Time stamp for Sync Frame Interrupt Enable** When this bit is set to “1”, it is enabled the interrupt when the egress time stamp is available from port 1 for Sync frame. This bit will be logical OR’ed together with the rest of bits in this register and the logical OR’ed output is connected to IER bit[12].
11 - 0	0x000	RW	**Time stamp Unit Interrupt Enable** When this bit is set to “1”, it indicates that the time stamp unit interrupt is enabled. The time stamp units from 12 to 1 are mapped to bit[11:0]. These 12 time stamp interrupts enable are logical OR’ed together with the rest of bits in this register and the logical OR’ed output is connected to IER bit[12].

4.2.29.47 0x690 – 0x733: Reserved

4.2.29.48 DSP Control 1 Register (0x734 – 0x735): DSP_CNTRL_6

This register contains control bits for the DSP block.

TABLE 4-187: DSP CONTROL 1 REGISTER (0X734 – 0X735): DSP_CNTRL_6

Bit	Default	R/W	Description
15 - 14	00	RW	Reserved
13	1	RW	**Receiver Adjustment** Set this bit to “1” when both ports 1 and 2 are in copper mode. When port 1 and/or port 2 is in fiber mode, this bit should be cleared to “0”. Note that the fiber or copper mode is selected in the CFGR register (0x0D8 – 0x0D9).
12 - 0	0x1020	RW	Reserved

4.2.29.49 0x736 – 0x747: Reserved

4.2.29.50 Analog Control 1 Register (0x748 – 0x749): ANA_CNTRL_1

This register contains control bits for the analog block.

TABLE 4-188: ANALOG CONTROL 1 REGISTER (0X748 – 0X749): ANA_CNTRL_1

Bit	Default	R/W	Description
15 - 8	0x00	RW	Reserved
7	0	RW	**LDO Off** This bit is used to control the on/off state of the internal low-voltage regulator. 0 = LDO On (Default) 1 = Turn LDO Off
6 - 0	0x00	RW	Reserved

4.2.29.51 0x74A – 0x74B: Reserved

4.2.29.52 Analog Control 3 Register (0x74C – 0x74D): ANA_CNTRL_3

This register contains control bits for the analog block.

TABLE 4-189: ANALOG CONTROL 3 REGISTER (0X74C – 0X74D): ANA_CNTRL_3

Bit	Default	R/W	Description
15	0	RW	**HIPLS3 Mask** This bit must be set prior to initiating the LinkMD function.
14 - 4	0x000	RW	Reserved
3	0	RW	**BTRX Reduce** This bit must be set prior to initiating the LinkMD function.
2 - 0	000	RW	Reserved

4.2.29.53 0x74E – 0x7FF: Reserved

4.3 MII Management (MIIM) Registers

The MIIM interface is used to access the MII PHY registers within the two embedded PHY blocks. The SPI interface can also be used to access these registers. The latter three interfaces use a different mapping mechanism than the MIIM interface. Note that when accessing these registers via the SPI interface, the relative order of the registers is not exactly the same.

The “PHYADs” by defaults are assigned “0x1” for PHY1 (port 1) and “0x2” for PHY2 (port 2).

The “REGAD” supported addresses are 0x0-0x5, 0x1D and 0x1F.

TABLE 4-190: PHY REGISTER MAPPING USING THE MII INTERFACE

PHY and Register Address	Description
PHYAD = 0x1, REGAD = 0x0	PHY1 Basic Control Register
PHYAD = 0x1, REGAD = 0x1	PHY1 Basic Status Register
PHYAD = 0x1, REGAD = 0x2	PHY1 Physical Identifier I
PHYAD = 0x1, REGAD = 0x3	PHY1 Physical Identifier II
PHYAD = 0x1, REGAD = 0x4	PHY1 Auto-Negotiation Advertisement Register
PHYAD = 0x1, REGAD = 0x5	PHY1 Auto-Negotiation Link Partner Ability Register
PHYAD = 0x1, 0x6 – 0x1C	PHY1 Not supported
PHYAD = 0x1, 0x1D	PHY1 LinkMD Control/Status
PHYAD = 0x1, 0x1E	PHY1 Not supported
PHYAD = 0x1, 0x1F	PHY1 Special Control/Status
PHYAD = 0x2, REGAD = 0x0	PHY2 Basic Control Register
PHYAD = 0x2, REGAD = 0x1	PHY2 Basic Status Register
PHYAD = 0x2, REGAD = 0x2	PHY2 Physical Identifier I
PHYAD = 0x2, REGAD = 0x3	PHY2 Physical Identifier II
PHYAD = 0x2, REGAD = 0x4	PHY2 Auto-Negotiation Advertisement Register
PHYAD = 0x2, REGAD = 0x5	PHY2 Auto-Negotiation Link Partner Ability Register
PHYAD = 0x2, 0x6 – 0x1C	PHY2 Not supported
PHYAD = 0x2, 0x1D	PHY2 LinkMD Control/Status
PHYAD = 0x2, 0x1E	PHY2 Not supported
PHYAD = 0x2, 0x1F	PHY2 Special Control/Status

TABLE 4-191: PHY1 (PHYAD = 0X1) AND PHY2 (PHYAD = 0X2): REGISTER 0 (REGAD = 0X0) -> MII BASIC CONTROL

Bit	Default	R/W	Description
15	0	RO	Reserved
14	0	RW	**Far-End Loopback** 1 = Perform port 1 loopback example as follows: Start: RXP2/RXM2 (port 2) Loopback: PMD/PMA of port 1's PHY End: TXP2/TXM2 (port 2) 0 = Normal operation.
13	0	RW	**Force 100BASE-TX** 1 = Force 100 Mbps if auto-negotiation is disabled (bit[12]) 0 = Force 10 Mbps if auto-negotiation is disabled (bit[12])
12	1	RW	**Auto-Negotiation Enable** 1 = Auto-negotiation enabled. 0 = Auto-negotiation disabled.
11	0	RW	**Power-Down** 1 = Power-down. 0 = Normal operation.
10	0	RO	**Isolate** Not supported.
9	0	RW	**Restart Auto-Negotiation** 1 = Restart auto-negotiation. 0 = Normal operation.
8	0	RW	**Force Full-Duplex** 1 = Force full-duplex. 0 = Force half-duplex. Applies if auto-negotiation is disabled. It is always in half-duplex if auto-negotiation is enabled but failed.
7	0	RO	**Collision Test** Not supported.
6	0	RO	Reserved
5	1	RW	**HP_MDIX** 1 = HP Auto-MDI-X mode. 0 = Microchip Auto-MDI-X mode.
4	0	RW	**Force MDI-X** 1 = Force MDI-X. 0 = Normal operation.
3	0	RW	**Disable Auto-MDI-X** 1 = Disable Auto-MDI-X. 0 = Normal operation.
2	0	RW	**Disable Far-End Fault** 1 = Disable far-end fault detection. 0 = Normal operation. For 100BASE-FX fiber mode operation.
1	0	RW	**Disable Transmit** 1 = Disable transmit. 0 = Normal operation.
0	0	RW	**Disable LED** 1 = Disable LED. 0 = Normal operation.

TABLE 4-192: PHY1 (PHYAD = 0X1) AND PHY2 (PHYAD = 0X2): REGISTER 1 (REGAD = 0X1) -> MII BASIC STATUS

Bit	Default	R/W	Description
15	0	RO	**T4 Capable** 1 = 100 BASE-T4 capable. 0 = Not 100 BASE-T4 capable.
14	1	RO	**100BASE-TX Full Capable** 1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable.
13	1	RO	**100BASE-TX Half Capable** 1 = 100BASE-TX half-duplex capable. 0 = Not 100BASE-TX half-duplex capable.
12	1	RO	**10BASE-T Full Capable** 1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.
11	1	RO	**10BASE-T Half Capable** 1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.
10 - 7	0x0	RO	Reserved
6	0	RO	**Preamble Suppressed** Not supported.
5	0	RO	**Auto-Negotiation Complete** 1 = Auto-negotiation complete. 0 = Auto-negotiation not completed.
4	0	RO	**Far-End Fault** 1 = Far-end fault detected. 0 = No far-end fault detected. For 100BASE-FX fiber-mode operation.
3	1	RO	**Auto-Negotiation Capable** 1 = Auto-negotiation capable. 0 = Not auto-negotiation capable.
2	0	RO	**Link Status** 1 = Link is up. 0 = Link is down.
1	0	RO	**Jabber Test** Not supported.
0	0	RO	**Extended Capable** 1 = Extended register capable. 0 = Not extended register capable.

TABLE 4-193: PHY1 (PHYAD = 0X1) AND PHY2 (PHYAD = 0X2): REGISTER 2 (REGAD = 0X2) -> PHYID HIGH

Bit	Default	R/W	Description
15 - 0	0x0022	RO	PHY ID High Word

TABLE 4-194: PHY1 (PHYAD = 0X1) AND PHY2 (PHYAD = 0X2): REGISTER 3 (REGAD = 0X3) -> PHYID LOW

Bit	Default	R/W	Description
15 - 0	0x1430	RO	PHY ID Low Word

TABLE 4-195: PHY1 (PHYAD = 0X1) AND PHY2 (PHYAD = 0X2): REG. 4 (REGAD = 0X4) -> AUTO-NEGOTIATION ADVERTISEMENT ABILITY

Bit	Default	R/W	Description
15	0	RO	**Next Page** Not supported.
14	0	RO	Reserved
13	0	RO	**Remote Fault** Not supported.
12 - 11	0x0	RO	Reserved
10	1	RW	**Pause (Flow Control Capability)** 1 = Advertise pause ability. 0 = Do not advertise pause capability.
9	0	RW	Reserved
8	1	RW	**Advertise 100BASE-TX Full-Duplex** 1 = Advertise 100BASE-TX full-duplex capable. 0 = Do not advertise 100BASE-TX full-duplex capability.
7	1	RW	**Advertise 100BASE-TX Half-Duplex** 1= Advertise 100BASE-TX half-duplex capable. 0 = Do not advertise 100BASE-TX half-duplex capability.
6	1	RW	**Advertise 10BASE-T Full-Duplex** 1 = Advertise 10BASE-T full-duplex capable. 0 = Do not advertise 10BASE-T full-duplex capability.
5	1	RW	**Advertise 10BASE-T Half-Duplex** 1 = Advertise 10BASE-T half-duplex capable. 0 = Do not advertise 10BASE-T half-duplex capability.
4 - 0	0x01	RO	**Selector Field** 802.3

TABLE 4-196: PHY1 (PHYAD = 0X1) AND PHY2 (PHYAD = 0X2): REG. 5 (REGAD = 0X5) -> AUTO-NEGOTIATION LINK PARTNER ABILITY

Bit	Default	R/W	Description
15	0	RO	**Next Page** Not supported.
14	0	RO	**LP ACK** Not supported.
13	0	RO	**Remote Fault** Not supported.
12 - 11	0x0	RO	Reserved
10	0	RO	**Pause** Link partner pause capability.
9	0	RO	Reserved
8	0	RO	**Advertise 100BASE-TX Full-Duplex** Link partner 100BASE-TX full capability.
7	0	RO	**Advertise 100BASE-TX Half-Duplex** Link partner 100 half capability.
6	0	RO	**Advertise 10BASE-T Full-Duplex** Link partner 10BASE-T full capability.
5	0	RO	**Advertise 10BASE-T Half-Duplex** Link partner 10BASE-T half capability.
4 - 0	0x1	RO	Reserved

TABLE 4-197: PHY1 (PHYAD = 0X1) AND PHY2 (PHYAD = 0X2): REG. 29 (REGAD = 0X1D) -> LINKMD CONTROL AND STATUS

Bit	Default	R/W	Description
15	0	RW/SC	**Cable Diagnostic Test Enable** 1 = Cable diagnostic test is enabled. It is self-cleared after the test is done. 0 = Indicates that the cable diagnostic test has completed and the status information is valid for read.
14 - 13	0x0	RO	**Cable Diagnostic Test Results** [00] = Normal condition. [01] = Open condition detected in the cable. [10] = Short condition detected in the cable. [11] = Cable diagnostic test has failed.
12	—	RO	**CDT 10M Short** 1 = Less than 10m short.
11 - 9	0x0	RO	Reserved
8 - 0	0x000	RO	**CDT_Fault_Count** Distance to the fault. The distance is approximately 0.4m*CDT_-Fault_Count.

TABLE 4-198: PHY1 (PHYAD = 0X1) AND PHY2 (PHYAD = 0X2): REG. 31 (REGAD = 0X1F) -> PHY SPECIAL CONTROL AND STATUS

Bit	Default	R/W	Description
15 - 6	0x000	RO	Reserved
5	0	RO	**Polarity Reverse** 1 = Polarity is reversed. 0 = Polarity is not reversed.
4	0	RO	**MDI-X Status** 0 = MDI 1 = MDI-X
3	0	RW	**Force Link** 1 = Force link pass. 0 = Normal operation.
2	1	RW	**Enable Energy Efficient Ethernet (EEE) on 10BASE-Te** 1 = Disable 10BASE-Te. 0 = Enable 10BASE-Te.
1	0	RW	**Remote (Near-End) Loopback** 1 = Perform remote loopback at Port 1's PHY (RXP1/RXM1 -> TXP1/TXM1) Port 2's PHY (RXP2/RXM2 -> TXP2/TXM2) 0 = Normal operation
0	0	RW	Reserved

4.4 Management Information Base (MIB) Counters

The KSZ8463 provides 34 MIB counters for each port. These counters are used to monitor the port activity for network management. The MIB counters are formatted “per port” and “all ports dropped packet” as shown in Table 4-199.

TABLE 4-199: FORMAT OF PER-PORT MIB COUNTERS

Bit	Name	R/W	Description	Default
31	Overflow	RO	1 = Counter overflow. 0 = No counter overflow.	0
30	Count Valid	RO	1 = Counter value is valid. 0 = Counter value is not valid.	0
29 - 0	Counter Values	RO	Counter value (read clear)	0x00000000

“Per Port” MIB counters are read using indirect memory access. The base address offsets and address ranges for all three ports are:

Port 1, base address is 0x00 and range is from 0x00 to 0x1F.

Port 2, base address is 0x20 and range is from 0x20 to 0x3F.

Port 3 (Host MII/RMII), base address is 0x40 and range is from 0x40 to 0x5F.

“Per Port” MIB counters are read using indirect access control in the IACR register (0x030 – 0x031) and the indirect access data registers in IADR4[15:0], IADR5[31:16] (0x02C – 0x02F). The port 1 MIB counters address memory offset as in Table 4-200.

TABLE 4-200: PORT 1 MIB COUNTERS – INDIRECT MEMORY OFFSET

Offset	Counter Name	Description
0x0	RxLoPriorityByte	Rx lo-priority (default) octet count including bad packets.
0x1	RxHiPriorityByte	Rx hi-priority octet count including bad packets.
0x2	RxUndersizePkt	Rx undersize packets with good CRC.
0x3	RxFragments	Rx fragment packets with bad CRC, symbol errors or alignment errors.
0x4	RxOversize	Rx oversize packets with good CRC (maximum: 2000 bytes).
0x5	RxJabbers	Rx packets longer than 1522 bytes with either CRC errors, alignment errors, or symbol errors (depends on max packet size setting).
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal packet size.
0x7	RxCRCError	Rx packets within (64,1522) bytes w/ an integral number of bytes and a bad CRC (upper limit depends on maximum packet size setting).
0x8	RxAlignmentError	Rx packets within (64,1522) bytes w/ a non-integral number of bytes and a bad CRC (upper limit depends on maximum packet size setting).
0x9	RxControl8808Pkts	Number of MAC control frames received by a port with 88-08h in Ether-Type field.
0xA	RxPausePkts	Number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B minimum), and a valid CRC.
0xB	RxBroadcast	Rx good broadcast packets (not including error broadcast packets or valid multicast packets).
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets).
0xD	RxUnicast	Rx good unicast packets.
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length.
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length.
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in length.

TABLE 4-200: PORT 1 MIB COUNTERS – INDIRECT MEMORY OFFSET (CONTINUED)

Offset	Counter Name	Description
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length.
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length.
0x13	Rx1024to2000Octets	Total Rx packets (bad packets included) that are between 1024 and 2000 octets in length (upper limit depends on max packet size setting).
0x14	TxLoPriorityByte	Tx lo-priority good octet count, including PAUSE packets.
0x15	TxHiPriorityByte	Tx hi-priority good octet count, including PAUSE packets.
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet.
0x17	TxPausePkts	Number of PAUSE frames transmitted by a port.
0x18	TxBroadcastPkts	Tx good broadcast packets (not including error broadcast or valid multi-cast packets).
0x19	TxMulticastPkts	Tx good multicast packets (not including error multicast packets or valid broadcast packets).
0x1A	TxUnicastPkts	Tx good unicast packets.
0x1B	TxDeferred	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium.
0x1C	TxTotalCollision	Tx total collision, half duplex only.
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions.
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision.
0x1F	TxMultipleCollision	Successfully Tx frames on a port for which Tx is inhibited by more than one collision.

TABLE 4-201: "ALL PORTS DROPPED PACKET" MIB COUNTER FORMAT

Bit	Default	R/W	Description
30 - 16	—	N/A	Reserved
15 - 0	0x0000	RO	Counter Value

Note: “All Ports Dropped Packet” MIB Counters do not indicate overflow or validity; therefore, the application must keep track of overflow and valid conditions.

“All Ports Dropped Packet” MIB counters are read using indirect memory access. The address offsets for these counters are in Table 4-202.

TABLE 4-202: "ALL PORTS DROPPED PACKET" MIB COUNTERS – INDIRECT MEMORY OFFSETS

Offset	Counter Name	Description
0x100	Port 1 TX Drop Packets	TX packets dropped due to lack of resources
0x101	Port 2 TX Drop Packets	TX packets dropped due to lack of resources
0x102	Port 3 TX Drop Packets	TX packets dropped due to lack of resources
0x103	Port 1 RX Drop Packets	RX packets dropped due to lack of resources
0x104	Port 2 RX Drop Packets	RX packets dropped due to lack of resources
0x105	Port 3 RX Drop Packets	RX packets dropped due to lack of resources

Examples:

1. MIB Counter Read (read port 1 “Rx64Octets” counter at indirect address offset 0x0E)

Write to Reg. IACR with 0x1C0E (set indirect address and trigger a read MIB counters operation)

Then:

Read Reg. IADR5 (MIB counter value [31:16]) // If bit [31] = “1”, there was a counter overflow // If bit [30] = “0”, restart (re-read) from this register

Read Reg. IADR4 (MIB counter value [15:0])

2. MIB Counter Read (read port 2 “Rx64Octets” counter at indirect address offset 0x2E)

Write to reg. IACR with 0x1C2E (set indirect address and trigger a read MIB counters operation)

Then:

Read Reg. IADR5 (MIB counter value [31:16]) // If bit [31] = “1”, there was a counter overflow // If bit [30] = “0”, restart (re-read) from this register

Read Reg. IADR4 (MIB counter value [15:0])

3. MIB Counter Read (read “port 1 TX Drop Packets” counter at indirect address offset 0x100)

Write to Reg. IACR with 0x1D00 (set indirect address and trigger a read MIB counters operation)

Then:

Read Reg. IADR4 (MIB counter value [15:0])

4.4.1 ADDITIONAL MIB INFORMATION

“Per Port” MIB counters are designed as “read clear”. That is, these counters will be cleared after they are read.

“All Ports Dropped Packet” MIB counters are not cleared after they are accessed. The application needs to keep track of overflow and valid conditions on these counters.

4.5 Static MAC Address Table

The KSZ8463 supports both a static and a dynamic MAC address table. In response to a destination address (DA) look up, The KSZ8463 searches both tables to make a packet forwarding decision. In response to a source address (SA) look up, only the dynamic table is searched for aging, migration and learning purposes.

The static DA look up result takes precedence over the dynamic DA look up result. If there is a DA match in both tables, the result from the static table is used. These entries in the static table will not be aged out by the KSZ8463.

TABLE 4-203: STATIC MAC TABLE FORMAT (8 ENTRIES)

Bit	Default	R/W	Description
57 - 54	0000	RW	**FID** Filter VLAN ID - identifies one of the 16 active VLANs.
53	0	RW	**Use FID** 1 = Specifies the use of FID+MAC for static table look up. 0 = Specifies only the use of MAC for static table look up.
52	0	RW	**Override** 1 = Overrides the port setting transmit enable = “0” or receive enable = “0” setting. 0 = Specifies no override. Note: The override bit also allows usage (turns on the entry) even if the Valid bit = “0”.
51	0	RW	**Valid** 1 = Specifies that this entry is valid, and the look up result will be used. 0 = Specifies that this entry is not valid.

TABLE 4-203: STATIC MAC TABLE FORMAT (8 ENTRIES) (CONTINUED)

Bit	Default	R/W	Description
50 - 48	000	RW	**Forwarding Ports** These 3 bits control the forwarding port(s): 000 = No forward. 001 = Forward to port 1. 010 = Forward to port 2. 100 = Forward to port 3. 011 = Forward to port 1 and port 2. 110 = Forward to port 2 and port 3. 101 = Forward to port 1 and port 3. 111 = Broadcasting (excluding the ingress port).
47 - 0	0	RW	**MAC Address** 48-bit MAC Address

Static MAC Table Lookup Examples:

- Static Address Table Read (read the second entry at indirect address offset 0x01)
  - Write to Reg. IACR with 0x1001 (set indirect address and trigger a read static MAC table operation)
  - Then:
  - Read Reg. IADR3 (static MAC table bits [57:48])
  - Read Reg. IADR2 (static MAC table bits [47:32])
  - Read Reg. IADR5 (static MAC table bits [31:16])
  - Read Reg. IADR4 (static MAC table bits [15:0])
- Static Address Table Write (write the eighth entry at indirect address offset 0x07)
  - Write to Reg. IADR3 (static MAC table bits [57:48])
  - Write to Reg. IADR2 (static MAC table bits [47:32])
  - Write to Reg. IADR5 (static MAC table bits [31:16])
  - Write to Reg. IADR4 (static MAC table bits [15:0])
  - Write to Reg. IACR with 0x0007 (set indirect address and trigger a write static MAC table operation)

4.6 Dynamic MAC Address Table

The Dynamic MAC Address is a read-only table.

TABLE 4-204: DYNAMIC MAC ADDRESS TABLE FORMAT (1024 ENTRIES)

Bit	Default	R/W	Description
71	—	RO	**Data Not Ready** 1 = Specifies that the entry is not ready, continue retrying until bit is set to “0”. 0 = Specifies that the entry is ready.
70 - 67	—	RO	Reserved
66	1	RO	**MAC Empty** 1 = Specifies that there is no valid entry in the table 0 = Specifies that there are valid entries in the table
65 - 56	0x000	RO	**Number of Valid Entries** Indicates how many valid entries in the table. 0x3FF means 1K entries. 0x001 means 2 entries. 0x000 and bit [66] = “0” means 1 entry. 0x000 and bit [66] = “1” means 0 entry.
55 - 54	—	RO	**Time stamp** Specifies the 2-bit counter for internal aging.

TABLE 4-204: DYNAMIC MAC ADDRESS TABLE FORMAT (1024 ENTRIES) (CONTINUED)

Bit	Default	R/W	Description
53 - 52	00	RO	**Source Port** Identifies the source port where FID+MAC is learned: 00 = Port 1 01 = Port 2 10 = Port 3
51 - 48	0x0	RO	**FID** Specifies the filter ID.
47 - 0	0x0000_0000_0000	RO	**MAC Address** Specifies the 48-bit MAC Address.

Dynamic MAC Address Lookup Example

- Dynamic MAC Address Table Read (read the first entry at indirect address offset 0 and retrieve the MAC table size)
  - Write to Reg. IACR with 0x1800 (set indirect address and trigger a read dynamic MAC Address table operation)
  - Then:
  - Read Reg. IADR1 (dynamic MAC table bits [71:64]) // If bit [71] = “1”, restart (reread) from this register
  - Read Reg. IADR3 (dynamic MAC table bits [63:48])
  - Read Reg. IADR2 (dynamic MAC table bits [47:32])
  - Read Reg. IADR5 (dynamic MAC table bits [31:16])
  - Read Reg. IADR4 (dynamic MAC table bits [15:0])

4.7 VLAN Table

The KSZ8463 uses the VLAN table to perform look-ups. If 802.1Q VLAN mode is enabled (SGCR2[15]), this table will be used to retrieve the VLAN information that is associated with the ingress packet. This information includes FID (Filter ID), VID (VLAN ID), and VLAN membership as described in Table 29.

TABLE 4-205: VLAN TABLE FORMAT (16 ENTRIES)

Bit	Default	R/W	Description
19	1	RW	**Valid** 1 = Specifies that this entry is valid, the look up result will be used. 0 = Specifies that this entry is not valid.
18 - 16	111	RW	**Membership** Specifies which ports are members of the VLAN. If a DA look up fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. For example: “101” means port 3 and port 1 are in this VLAN.
15 - 12	0x0	RW	**FID** Specifies the Filter ID. The KSZ8463 supports 16 active VLANs represented by these four bit fields. The FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA.
11 - 0	0x001	RW	**VID** Specifies the IEEE 802.1Q 12 bits VLAN ID.

If 802.1Q VLAN mode is enabled, then KSZ8463 will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, then the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non-null VID, then VID in the tag will be used. The look up process will start from the VLAN table look up. If the VID is not found in any of the VLAN table entries, or if the VID is found but is not valid, then packet will be dropped and no address learning will take place. If the VID is valid, then FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look up determines the forwarding ports. If FID+DA fails, then the packet will be broadcast to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, then the FID+SA will be learned.

VLAN Table Lookup Examples

1. VLAN Table Read (read the third entry, at the indirect address offset 0x02)

Write to Reg. IACR with 0x1402 (set indirect address and trigger a read VLAN table operation)

Then:

Read Reg. IADR5 (VLAN table bits [19:16])

Read Reg. IADR4 (VLAN table bits [15:0])

2. VLAN Table Write (write the seventh entry, at the indirect address offset 0x06)

Write to Reg. IADR5 (VLAN table bits [19:16])

Write to Reg. IADR4 (VLAN table bits [15:0])

Write to Reg. IACR with 0x1406 (set indirect address and trigger a read VLAN table operation)

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings*

Supply Voltage ($V_{DD\_A3.3}$, V_{DD_IO}) ..... –0.5V to +5.0V

Supply Voltage (V_{DD_AL}, V_{DD_L}) ..... –0.5V to +1.8V

Input Voltage (All Inputs) ..... –0.5V to +5.0V

Output Voltage (All Outputs) ..... –0.5V to +5.0V

Lead Temperature (soldering, 10s) ..... +260°C

Storage Temperature (T_S) ..... –65°C to +150°C

Maximum Junction Temperature (T_J) ..... +125°C

HBM ESD Rating ..... 2 kV

*Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

5.2 Operating Ratings**

Supply Voltage

$V_{DDA\_3.3}$ ..... +3.135V to +3.465V

V_{DD_L}, V_{DD_AL}, V_{DD_COL} ..... +1.25V to +1.4V

V_{DD_IO} (3.3V) ..... +3.135V to +3.465V

V_{DD_IO} (2.5V) ..... +2.375 to +2.625V

V_{DD_IO} (1.8V) ..... +1.71V to +1.89V

Ambient Operating Temperature (T_A)

Industrial ..... –40°C to +85°C

Thermal Resistance (Note 5-1)

Junction-to-Ambient (Θ_{JA}) ..... +49°C/W

Junction-to-Case (Θ_{JC}) ..... +19°C/W

**The device is not guaranteed to function outside its operating ratings. Unused inputs must always be tied to an appropriate logic voltage level (GROUND to V_{DD_IO}).

Note:	Do not drive input signals without power supplied to the device.

Note 5-1 No heat spreader (HS) in this package. The Θ_{JC}/Θ_{JA} is under air velocity 0m/s.

6.0 ELECTRICAL CHARACTERISTICS

TABLE 6-1: ELECTRICAL CHARACTERISTICS (Note 6-1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Note
Supply Current for 100BASE-TX Operation (Internal Low-Voltage Regulator On, MII MAC Mode, $V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = 3.3V) (Note 6-1, Note 6-2)						
—	$I_{VDD\_A3.3}$	—	46	—	mA	100% traffic on both ports
	I_{VDD_IO}	—	98	—	mA	
	$PDISS_{DEVICE}$	—	476	—	mW	
—	$I_{VDD\_A3.3}$	—	4.5	—	mA	Ports 1 and 2 Powered Down (P1CR4, P2CR4 bit[11] = “1”)
	I_{VDD_IO}	—	74	—	mA	
	$PDISS_{DEVICE}$	—	259	—	mW	
—	$I_{VDD\_A3.3}$	—	5.3	—	mA	Ports 1 and 2 Not Connected, using EDPD Feature (PMCTRL bits[1:0] = “01”)
	I_{VDD_IO}	—	73	—	mA	
	$PDISS_{DEVICE}$	—	260	—	mW	
—	$I_{VDD\_A3.3}$	—	5.9	—	mA	Ports 1 and 2 Connected, No Traffic, using EEE Feature
	I_{VDD_IO}	—	74	—	mA	
	$PDISS_{DEVICE}$	—	264	—	mW	
—	$I_{VDD\_A3.3}$	—	1.1	—	mA	Soft Power-Down Mode (PMCTRL bits[1:0] = “10”)
	I_{VDD_IO}	—	3.2	—	mA	
	$PDISS_{DEVICE}$	—	14	—	mW	
—	$I_{VDD\_A3.3}$	—	0.1	—	mA	Hardware Power-Down Mode While the PWDRN pin (pin 17) is Held Low. (Note 6-3)
	I_{VDD_IO}	—	1.3	—	mA	
	$PDISS_{DEVICE}$	—	4.6	—	mW	
Supply Current for 100BASE-TX Operation (Internal Low-Voltage Regulator Off, MII PHY Mode, $V_{DD\_A3.3}$ and V_{DD_IO} = 3.3V; V_{DD_L}, V_{DD_AL}, and V_{DD_COL} = 1.4V) (Note 6-1, Note 6-2)						
—	$I_{VDD\_A3.3}$	—	46	—	mA	100% Traffic on Both Ports
	I_{VDD_IO}	—	21	—	mA	
	$I_{VDD\_AL} + I_{VDD\_DL}$	—	84	—	mA	
	$PDISS_{DEVICE}$	—	328	—	mW	
—	$I_{VDD\_A3.3}$	—	3.8	—	mA	Ports 1 and 2 Powered Down (P1CR4, P2CR4 bit[11] = “1”)
	I_{VDD_IO}	—	15.2	—	mA	
	$I_{VDD\_AL} + I_{VDD\_DL}$	—	71	—	mA	
	$PDISS_{DEVICE}$	—	155	—	mW	
—	$I_{VDD\_A3.3}$	—	4.6	—	mA	Ports 1 and 2 Not Connected, using EDPD Feature (PMCTRL bits[1:0] = “01”)
	I_{VDD_IO}	—	15.1	—	mA	
	$I_{VDD\_AL} + I_{VDD\_DL}$	—	69	—	mA	
	$PDISS_{DEVICE}$	—	155	—	mW	
—	$I_{VDD\_A3.3}$	—	5.2	—	mA	Ports 1 and 2 Connected, No Traffic, using EEE Feature
	I_{VDD_IO}	—	15.4	—	mA	
	$I_{VDD\_AL} + I_{VDD\_DL}$	—	70	—	mA	
	$PDISS_{DEVICE}$	—	159	—	mW	

TABLE 6-1: ELECTRICAL CHARACTERISTICS (Note 6-1) (CONTINUED)

Parameters	Symbol	Min.	Typ.	Max.	Units	Note
—	$I_{VDD\_A3.3}$	—	0.1	—	mA	Soft Power-Down Mode (PMCTRL bits[1:0] = "10")
	I_{VDD_IO}	—	2.1	—	mA	
	I_{VDD_AL} + I_{VDD_DL}	—	1.4	—	mA	
	$PDISS_{DEVICE}$	—	9	—	mW	
—	$I_{VDD\_A3.3}$	—	0.1	—	mA	Hardware Power-Down Mode While the PWDRN pin (pin 17) is Held Low. (Note 6-3)
	I_{VDD_IO}	—	2.1	—	mA	
	I_{VDD_AL} + I_{VDD_DL}	—	1.2	—	mA	
	$PDISS_{DEVICE}$	—	9	—	mW	
Supply Current for 10BASE-T Operation (Internal Low-Voltage Regulator On, MII MAC Mode, $V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = 3.3V) (Note 6-1, Note 6-2)						
—	$I_{VDD\_A3.3}$	—	51	—	mA	100% Traffic on Both Ports
	I_{VDD_IO}	—	78	—	mA	
	$PDISS_{DEVICE}$	—	425	—	mW	
—	$I_{VDD\_A3.3}$	—	19.2	—	mA	Link, No Traffic on Both Ports
	I_{VDD_IO}	—	72	—	mA	
	$PDISS_{DEVICE}$	—	302	—	mW	
Supply Current for 10BASE-T Operation (Internal Low-Voltage Regulator Off, MII PHY Mode, $V_{DD\_A3.3}$ and V_{DD_IO} = 3.3V; V_{DD_L}, V_{DD_AL}, and V_{DD_COL} = 1.4V) (Note 6-1, Note 6-2)						
—	$I_{VDD\_A3.3}$	—	50	—	mA	100% Traffic on Both Ports
	I_{VDD_IO}	—	15.7	—	mA	
	I_{VDD_AL} + I_{VDD_DL}	—	71	—	mA	
	$PDISS_{DEVICE}$	—	315	—	mW	
—	$I_{VDD\_A3.3}$	—	19	—	mA	Link, No Traffic on Both Ports
	I_{VDD_IO}	—	15.3	—	mA	
	I_{VDD_AL} + I_{VDD_DL}	—	69	—	mA	
	$PDISS_{DEVICE}$	—	212	—	mW	
Internal Voltage Regulator Output Voltage						
Output Voltage at V_{DD_L}	V_{LDO}	—	1.32	—	V	V_{DD_IO} = 2.5V or 3.3V; internal regulator enabled; measured at pins 40 and 51
CMOS Inputs (V_{DD_IO} = 3.3V/2.5V/1.8V)						
Input High Voltage	V_{IH}	2.1/1.7/1.3	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.9/0.9/0.6	V	—
Input Current	I_{IN}	–10	—	10	µA	V_{IN} = GND ~ V_{DD_IO}
X1 Crystal/Osc Input Pin						
Input High Voltage	V_{IH}	2.1	—	—	V	$V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = any
Input Low Voltage	V_{IL}	—	—	0.9	V	$V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = any
Input Current	I_{IN}	—	—	10	µA	—
PWRDN Input (Note 6-3)						
Input High Voltage	V_{IH}	1.1	—	—	V	$V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = any

TABLE 6-1: ELECTRICAL CHARACTERISTICS (Note 6-1) (CONTINUED)

Parameters	Symbol	Min.	Typ.	Max.	Units	Note
Input Low Voltage	V_{IL}	—	—	0.3	V	$V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = any
FXSD Input						
Input High Voltage	V_{IH}	2.1	—	—	V	$V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = any
Input Low Voltage	V_{IL}	—	—	1.2	V	$V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = any
CMOS Outputs (V_{DD_IO} = 3.3V/2.5V/1.8V)						
Output High Voltage	V_{OH}	2.4/1.9/1.5	—	—	V	I_{OH} = –8 mA
Output Low Voltage	V_{OL}	—	—	0.4/0.4/0.2	V	I_{OL} = 8 mA
Output Tri-State Leakage	$\|I_{OZ}\|$	—	—	10	µA	—
100BASE-TX Transmit (Measured Differentially After 1:1 Transformer)						
Peak Differential Output Voltage	V_O	±0.95	—	±1.05	V	100Ω termination on the diff. output
Output Voltage Imbalance	V_{IMB}	—	—	2	%	100Ω termination on the diff. output
Rise/Fall Time	t_r/t_f	3	—	5	ns	—
Rise/Fall Time Imbalance	—	0	—	0.5	ns	—
Duty Cycle Distortion	—	—	—	±0.25	ns	—
Overshoot	—	—	—	5	%	—
Reference Voltage of ISET	V_{SET}	—	0.65	—	V	Using 6.49 kΩ – 1% resistor
Output Jitter	—	—	0.7	1.4	ns	Peak-to-peak
10BASE-T Receive						
Squelch Threshold	V_{SQ}	—	400	—	mV	5 MHz square wave
10BASE-T Transmit (Measured Differentially After 1:1 Transformer)						
Peak Differential Output Voltage	V_P	2.2	2.5	2.8	V	100Ω termination on the differential output
Jitter Added	—	—	1.8	3.5	ns	100Ω termination on the differential output (peak-to-peak)
Rise/Fall Time	t_r/t_f	—	25	—	ns	—
LED Outputs						
Output Drive Current	I_{LED}	—	8	—	mA	Each LED pin (P1/2LED0, P1/2LED1)
I/O Pin Internal Pull-Up and Pull-Down Effective Resistance						
1.8V Pull-Up Resistance	R1.8PU	57	100	187	kΩ	V_{DD_IO} = 1.8V
1.8V Pull-Down Resistance	R1.8PD	55	100	190	kΩ	
2.5V Pull-Up Resistance	R2.5PU	37	59	102	kΩ	V_{DD_IO} = 2.5V
2.5V Pull-Down Resistance	R2.5PD	35	60	110	kΩ	
3.3V Pull-Up Resistance	R3.3PU	29	43	70	kΩ	V_{DD_IO} = 3.3V
3.3V Pull-Down Resistance	R3.3PD	27	43	76	kΩ	

Note 6-1 $I_{VDD\_A3.3}$ measured at pin 9. I_{VDD_IO} measured at pins 21, 30, and 56. I_{VDD_AL} measured at pins 6 and 16. I_{VDD_DL} measured at pins 40 and 51.

Note 6-2 T_A = 25°C. Specification is for packaged product only.

Note 6-3 For PWRDN pin (pin 17), the operating value of V_{IH} is lower than the other CMOS input pins. It is not dependent on V_{DD_IO}.

7.0 TIMING SPECIFICATIONS

7.1 MII Transmit Timing in MAC Mode

FIGURE 7-1: MII TRANSMIT TIMING IN MAC MODE

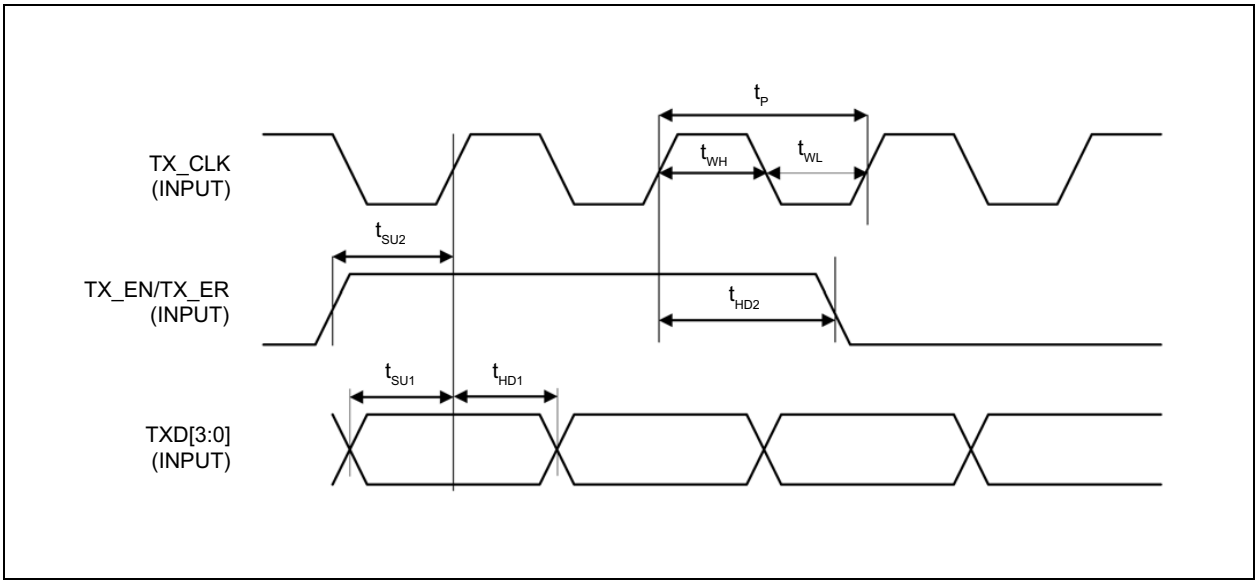


TABLE 7-1: MII TRANSMIT TIMING IN MAC MODE PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t_P (100BASE-TX/10BASE-T)	RX_CLK Period	—	40/400	—	ns
t_{WL} (100BASE-TX/ 10BASE-T)	RX_CLK Pulse Width Low	—	20/200	—	ns
t_{WH} (100BASE-TX/ 10BASE-T)	RX_CLK Pulse Width High	—	20/200	—	ns
t_{OD}	RX_DV, RXD[3:0] Output Delay from Rising Edge of RX_CLK	—	16	—	ns

7.2 MII Receive Timing in MAC Mode

This timing illustrates a read operation by the KSZ8463 from a PHY or other device while operating the KSZ8463 in MAC mode.

FIGURE 7-2: MII RECEIVE TIMING IN MAC MODE

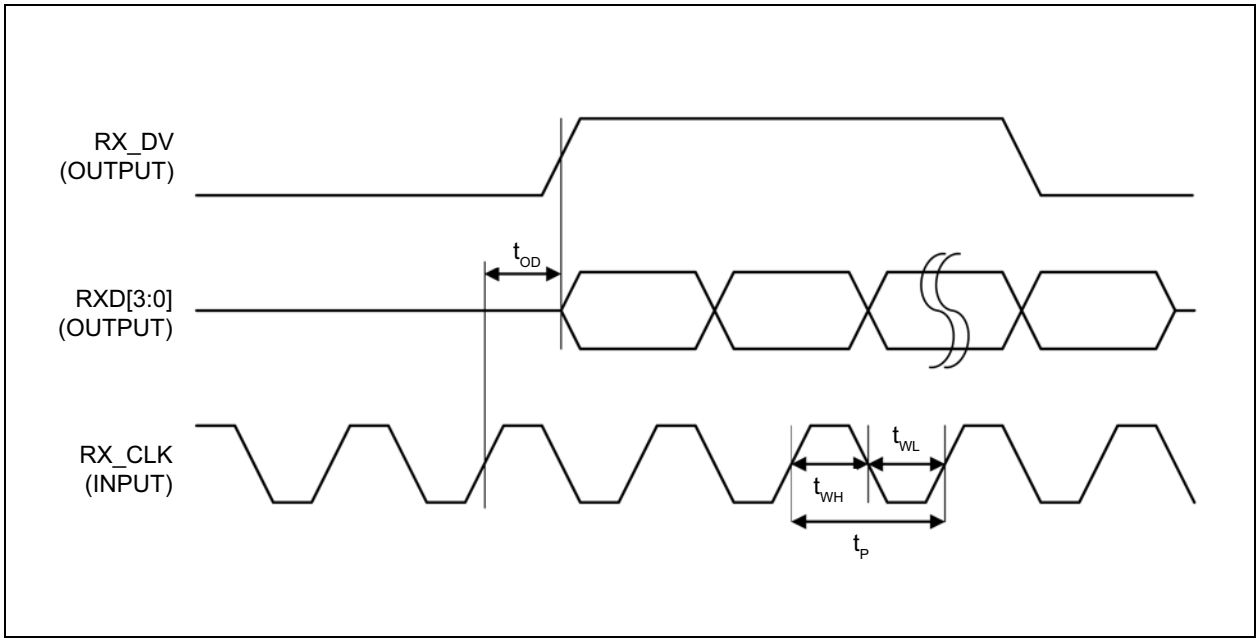


TABLE 7-2: MII RECEIVE TIMING IN MAC MODE PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t_P (100BASE-TX/10BASE-T)	TX_CLK period	—	40/400	—	ns
t_{WL} (100BASE-TX/ 10BASE-T)	TX_CLK pulse width low	—	20/200	—	ns
t_{WH} (100BASE-TX/ 10BASE-T)	TX_CLK pulse width high	—	20/200	—	ns
t_{SU1}	TXD[3:0] setup time to rising edge of TX_CLK	10	—	—	ns
t_{SU2}	TX_EN, TX_ER setup time to rising edge of TX_-CLK	10	—	—	ns
t_{HD1}	TXD[3:0] hold time from rising edge of TX_CLK	10	—	—	ns
t_{HD2}	TX_EN, TX_ER hold time from rising edge of TX_-CLK	10	—	—	ns

7.3 MII Receive Timing in PHY Mode

FIGURE 7-3: MII RECEIVE TIMING IN PHY MODE

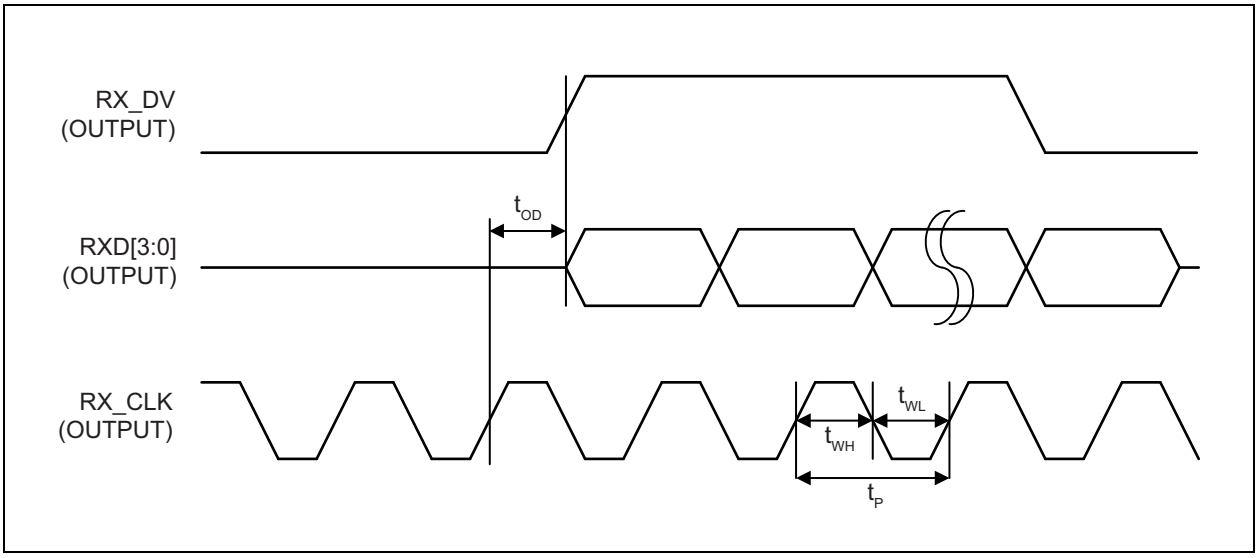


TABLE 7-3: MII RECEIVE TIMING IN PHY MODE PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_P (100BASE-TX/10BASE-T)	RX_CLK period	—	40/400	—	ns
t_{WL} (100BASE-TX/ 10BASE-T)	RX_CLK pulse width low	—	20/200	—	ns
t_{WH} (100BASE-TX/ 10BASE-T)	RX_CLK pulse width high	—	20/200	—	ns
t_{OD}	RX_DV, RXD[3:0] output delay from rising edge of RX_CLK	—	20	—	ns

7.4 MII Transmit Timing in PHY Mode

FIGURE 7-4: MII TRANSMIT TIMING IN PHY MODE

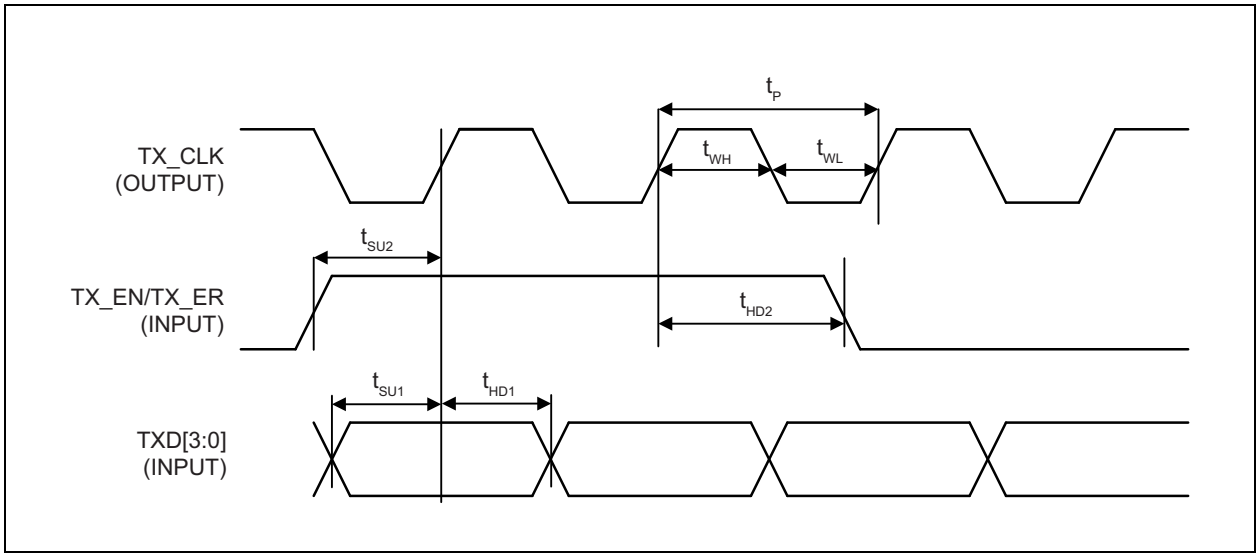


TABLE 7-4: MII TRANSMIT TIMING IN PHY MODE PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_P (100BASE-TX/10BASE-T)	TX_CLK period	—	40/400	—	ns
t_{WL} (100BASE-TX/ 10BASE-T)	TX_CLK pulse width low	—	20/200	—	ns
t_{WH} (100BASE-TX/ 10BASE-T)	TX_CLK pulse width high	—	20/200	—	ns
t_{SU1}	TXD[3:0] setup time to rising edge of TX_CLK	10	—	—	ns
t_{SU2}	TX_EN, TX_ER setup time to rising edge of TX_-CLK	10	—	—	ns
t_{HD1}	TXD[3:0] hold time from rising edge of TX_CLK	0	—	—	ns
t_{HD2}	TX_EN, TX_ER hold time from rising edge of TX_-CLK	0	—	—	ns

7.5 Reduced MII (RMII) Timing

FIGURE 7-5: RMII TRANSMIT TIMING

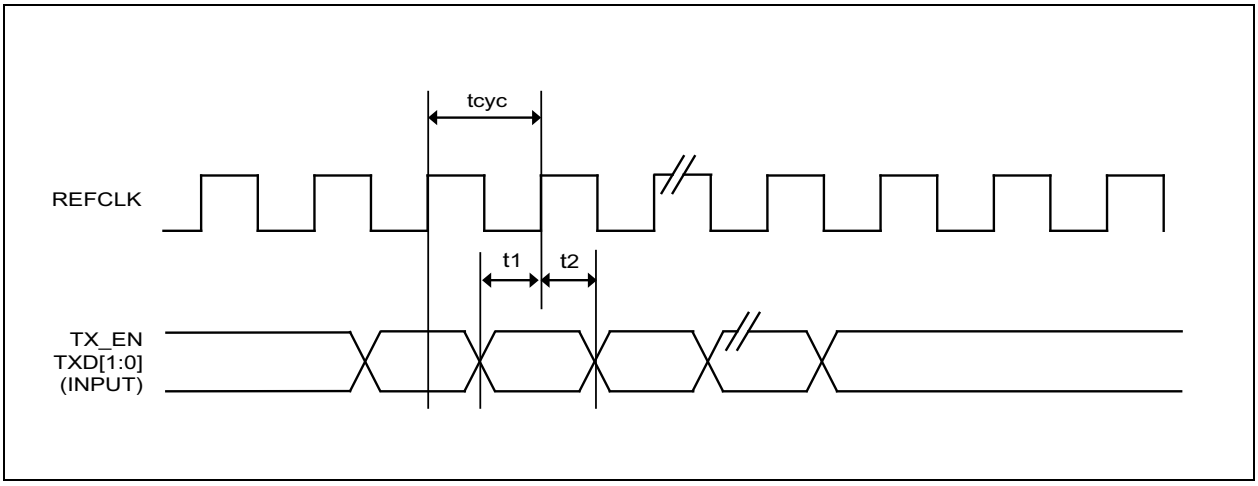


FIGURE 7-6: RMII RECEIVE TIMING

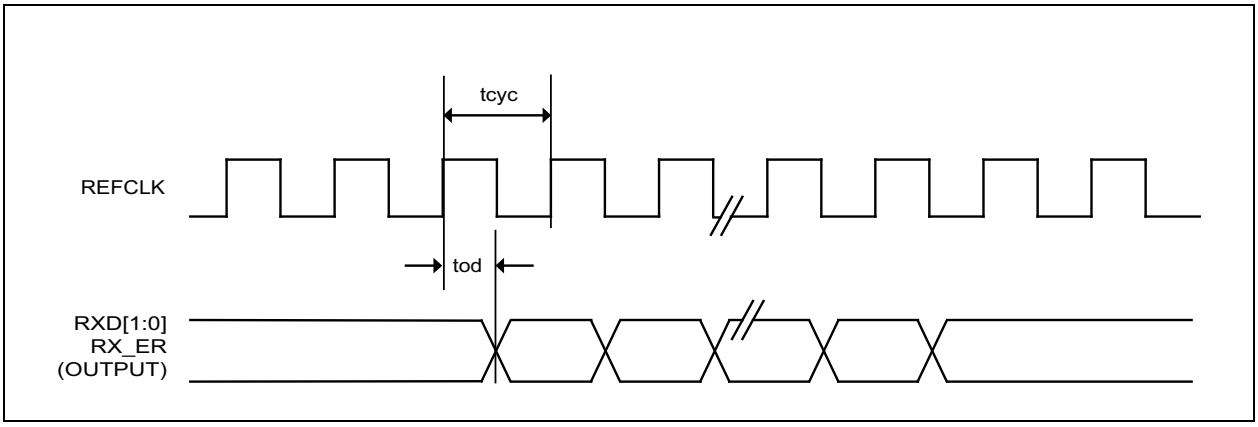


TABLE 7-5: MII RECEIVE TIMING (100BASE-TX) PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{CYC}	Clock cycle	—	20	—	ns
t_1	Set-up time	4	—	—	ns
t_2	Hold time	2	—	—	ns
t_{OD}	Output delay	7	9	13	ns

7.6 MIIM (MDC/MDIO) Timing

FIGURE 7-7: MIIM (MDC/MDIO) TIMING

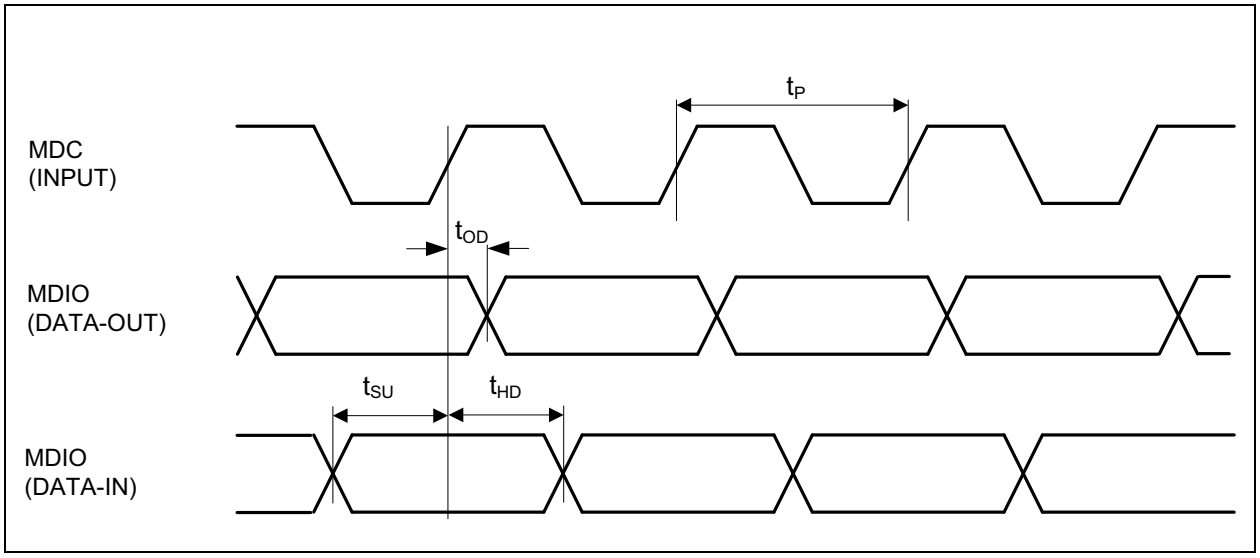


TABLE 7-6: MIIM (MDC/MDIO) TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_P	MDC period	—	400	—	ns
t_{OD}	Output delay	—	200	—	ns
t_{SU}	MDIO setup time to rising edge of MDC	2	—	—	ns
t_{HD}	MDIO hold time from rising edge of MDC	5	—	—	ns

7.7 SPI Input and Output Timing

FIGURE 7-8: SPI INTERFACE DATA INPUT TIMING

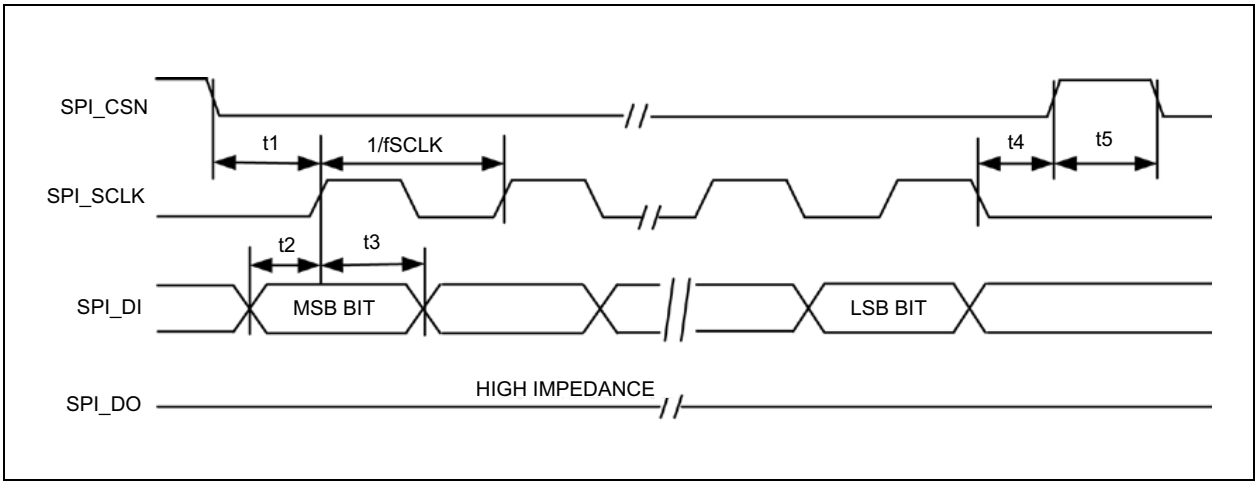


FIGURE 7-9: SPI INTERFACE DATA OUTPUT TIMING

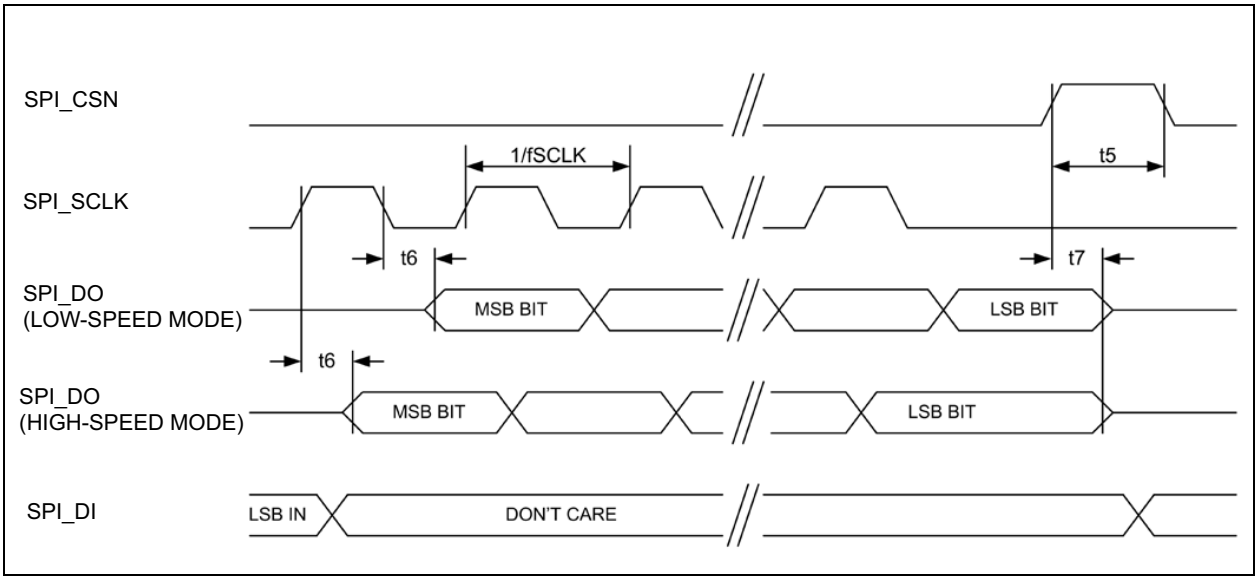


TABLE 7-7: SMII TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
f_{SCLK}	SPI_SCLK Clock Frequency	—	—	50	MHz
t_1	SPI_CSN active setup time	8	—	—	ns
t_2	SPI_DI data input setup time	3	—	—	ns
t_3	SPI_DI data input hold time	3	—	—	ns
t_4	SPI_CSN active hold time	8	—	—	ns
t_5	SPI_CSN disable high time	8	—	—	ns
t_6	SPI_SCLK falling edge to SPI_DO data output valid	2	—	9	ns
t_7	SPI_CSN inactive to SPI_DO data output invalid	1	—	—	ns

7.8 Auto-Negotiation Timing

FIGURE 7-10: AUTO-NEGOTIATION TIMING

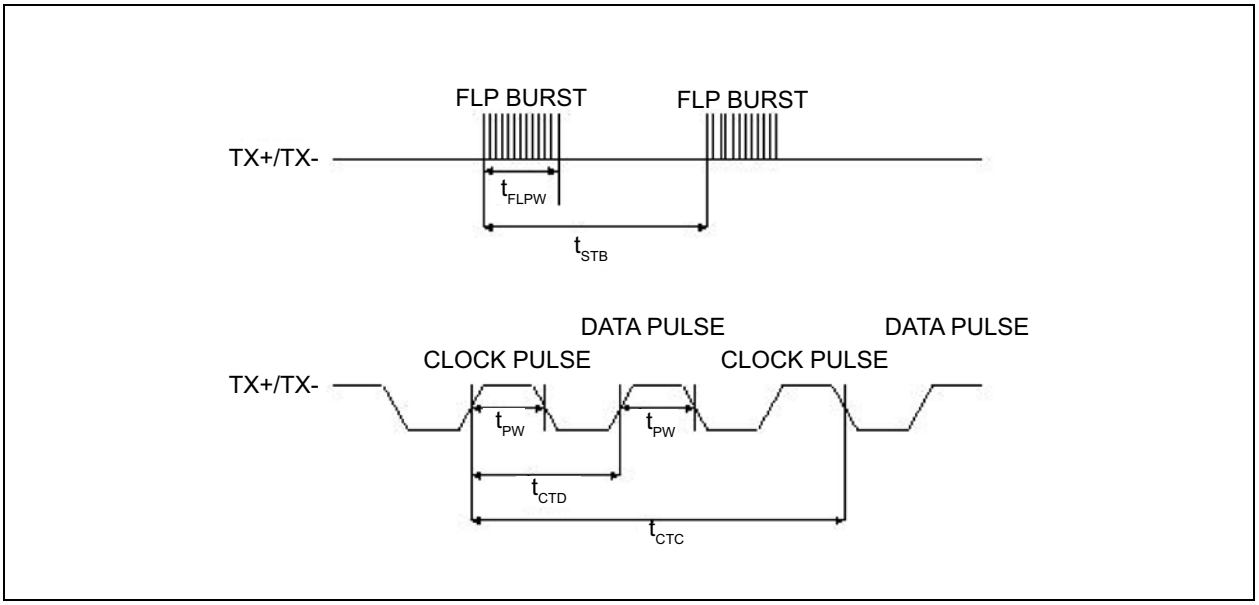


TABLE 7-8: AUTO-NEGOTIATION TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{BTB}	FLP Burst to FLP Burst	8	16	24	ms
t_{FLPW}	FLP Burst Width	—	2	—	ms
t_{PW}	Clock/Data Pulse Width	—	100	—	ns
t_{CTD}	Clock Pulse to Data Pulse	55.5	64	69.5	µs
t_{CTC}	Clock Pulse to Clock Pulse	111	128	139	µs
—	Number of Clock/Data Pulses per FLP Burst	17	—	33	—

7.9 Trigger Output Unit and Time Stamp Input Unit Timing

The timing information in the following figure provides details and constraints on various timing relationships within the twelve trigger output units and the time stamp input units.

FIGURE 7-11: TRIGGER OUTPUT UNIT AND TIME STAMP INPUT UNIT TIMING

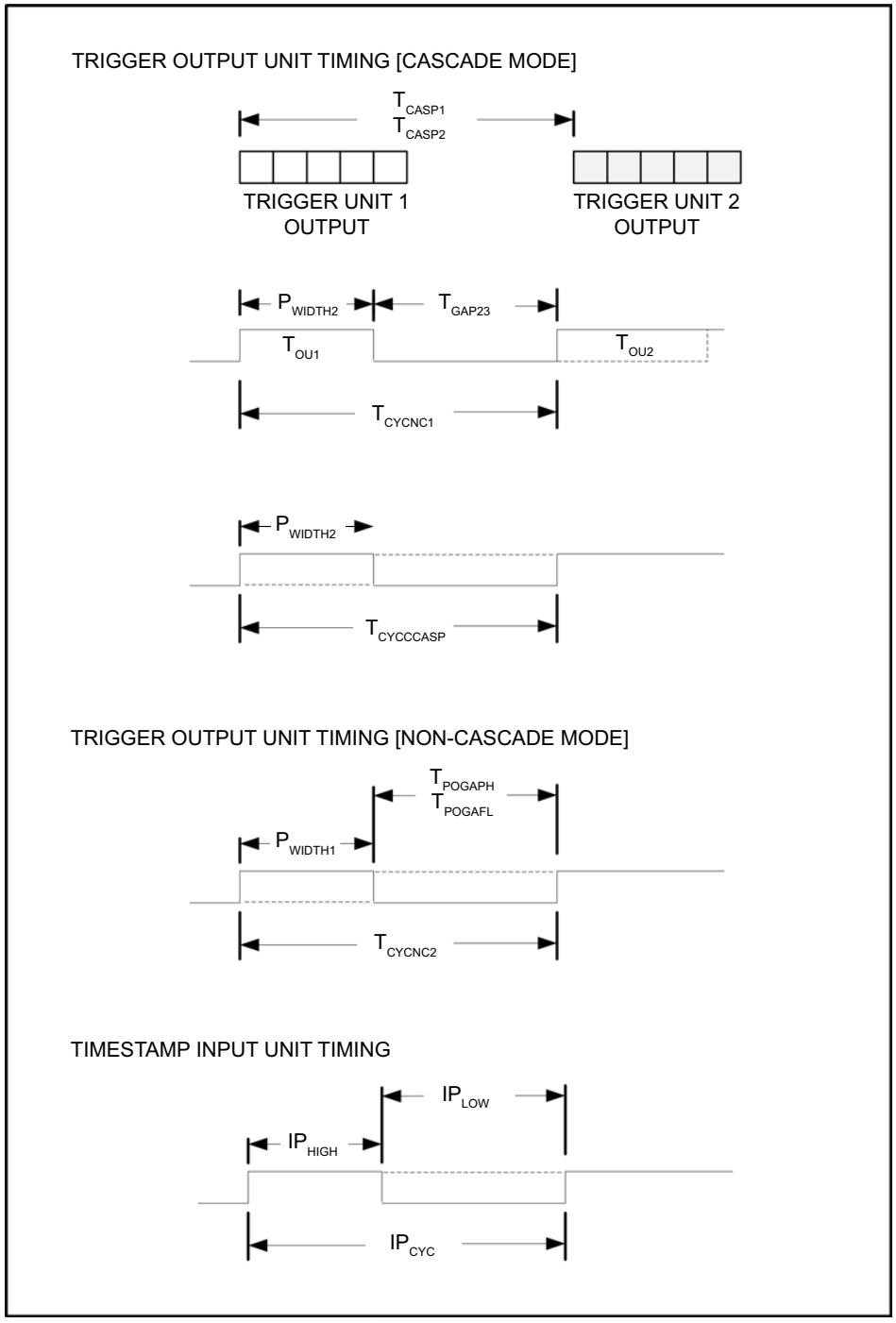


TABLE 7-9: TRIGGER OUTPUT UNIT AND TIME STAMP INPUT UNIT TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
Trigger Output Unit Timing [Cascade Mode}					
T_{CASP1}	In cascade mode for TRIGX_CFG_1[6:4] = 100, or 101, or 110 (Neg. Edge, Pos. Edge, and Shift Reg. Output signals). Minimum time between start of one TOU and the start of another TOU cascaded on the same GPIO pin.	80	—	—	ns
T_{CASP2}	In cascade mode for TRIGX_CFG_1[6:4] = 010, 011, 100, or 101 (Neg. Pulse, Pos. Pulse, Neg. Periodic, and Pos. Periodic Output signals). Minimum time between start of one TOU and the start of another TOU cascaded on the same GPIO pin.	120	—	—	ns
$T_{CYCCASP}$	In cascade mode for TRIGX_CFG_1[6:4] = 010, and 011 (Neg. Pulse, Pos. Pulse Output signals). In cascade mode, the cycle time of the trigger output unit operating in the indicated modes.	80	≥32 + P_{WIDTH2}		ns
T_{CYCNC1}	In cascade mode for TRIGX_CFG_1[6:4] = 100 or 101 (Neg. Periodic, Pos. periodic Output signals). Minimum cycle time for any trigger output unit operating in the indicated modes.	80	≥32 + P_{WIDTH2}		ns
T_{GAP23}	In cascade mode for TRIGX_CFG_1[6:4] = 010, and 011 (Neg. Pulse, Pos. Pulse Output signals): Minimum gap time required between end of period of first trigger output unit to beginning of output of 2nd trigger output unit.	80	—	—	ns
P_{WIDTH2}	In cascade mode, the minimum low or high pulse width of the trigger output unit.	8	—	—	ns
Trigger Output Unit Timing [Non-Cascade Mode]					
T_{CYCNC2}	In non-cascade mode, the minimum cycle time for any trigger output unit.	80	≥32 + P_{WIDTH2}		ns
T_{POGAP}	In non-cascade mode, the minimum time between the end of the generated pulse to the start of the next pulse.	32	—	—	ns
P_{WIDTH1}	In non-cascade mode, the minimum low or high pulse width of the trigger output unit.	8	—	—	ns
Time Stamp Input Unit Timing					
IP_{HIGH}	Allowable high time of an incoming digital waveform on any GPIO pin	24	—	—	ns
IP_{LOW}	In non-cascade mode, the minimum time between the end of the generated pulse to the start of the next pulse.	24	—	—	ns
IP_{CYC}	In non-cascade mode, the minimum time between the end of the generated pulse to the start of the next pulse.	48	—	—	ns

7.10 Reset and Power Sequence Timing

The KSZ8463 reset timing and power sequence requirements are summarized in the following figure and table.

FIGURE 7-12: RESET AND POWER SEQUENCE TIMING

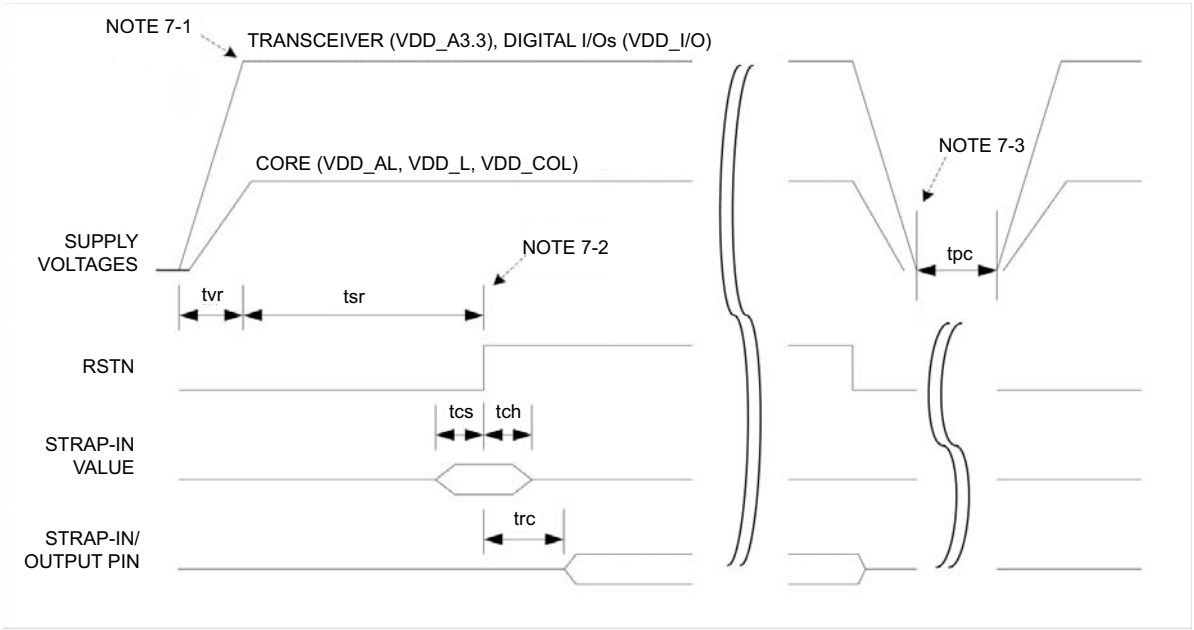


TABLE 7-10: RESET AND POWER SEQUENCE TIMING PARAMETERS (Note 7-1, Note 7-2, Note 7-3)

Parameter	Description	Min.	Typ.	Max.	Units
t_{VR}	Supply voltages rise time (must be monotonic)	0	—	—	µs
t_{SR}	Stable supply voltages to de-assertion of reset	10	—	—	ms
t_{CS}	Strap-in pin configuration setup time	5	—	—	ns
t_{CH}	Strap-in pin configuration hold time	5	—	—	ns
t_{RC}	De-assertion of reset to strap-in pin output	6	—	—	ns

Note 7-1 The recommended powering sequence is to bring up all voltages at the same time. However, if that cannot be attained, then a recommended power-up sequence is to have the transceiver ($V_{DD\_A3.3}$) and digital I/Os (V_{DD_IO}) voltages power up before the low voltage core (V_{DD_AL}, V_{DD_L}, and V_{DD_COL}) voltage, if an external low voltage core supply is used. There is no power sequence requirement between transceiver ($V_{DD\_A3.3}$) and digital I/Os (V_{DD_IO}) power rails. The power-up waveforms should be monotonic for all supply voltages to the KSZ8463.

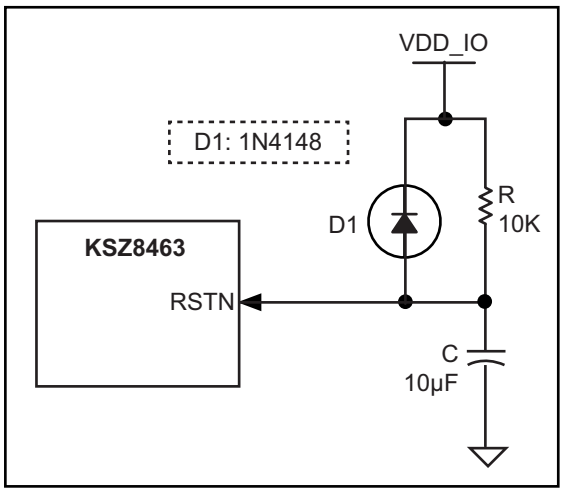
Note 7-2 After the de-assertion of reset, it is recommended to wait a minimum of 100 µs before starting programming of the device through any interface.

Note 7-3 The recommended power-down sequence is to have the low voltage core voltage power down first before powering down the transceiver and digital I/O voltages.

7.11 Reset Circuit

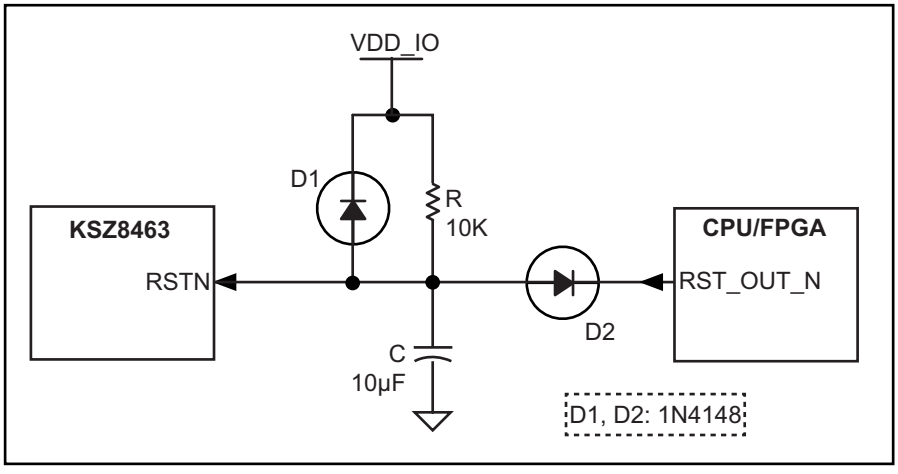
The following reset circuit is recommended for powering up the KSZ8463 device if reset is triggered by the power supply.

FIGURE 7-13: SIMPLE RESET CIRCUIT



The following reset circuit is recommended for applications where reset is driven by another device (e.g., CPU or FPGA). At POR, R, C and D1 provide the necessary ramp rise time to reset the KSZ8463 device. The RST_OUT_N from CPU/FPGA provides the warm reset after power-up.

FIGURE 7-14: RECOMMENDED RESET CIRCUIT FOR INTERFACING WITH CPU/FPGA RESET OUTPUT



8.0 REFERENCE CLOCK: CONNECTION AND SELECTION

The three different sources for a reference clock are shown in Figure 8-1. Note that MII clocks are not discussed in this section. The KSZ8463ML and KSZ8463FML require an external 25 MHz crystal attached to X1/X2, or a 25 MHz oscillator attached to X1.

The KSZ8463RL and KSZ8463FRL have two options for a reference clock, as determined by the strapping option on pin 41. The 25 MHz option on X1/X2 is as described above. When the 50 MHz option is selected, an external 50 MHz clock is applied to the REFCLK_I pin, while X1 and X2 are unconnected. Note that in the 25 MHz mode, REFCLK_O must be enabled, and it must be externally connected to REFCLK_I.

The resistor shown on X2 is optional and can be used to limit current to the crystal if needed, depending on the specific crystal that is used. The maximum recommended value is 30Ω.

FIGURE 8-1: INPUT REFERENCE CLOCK CONNECTION OPTIONS

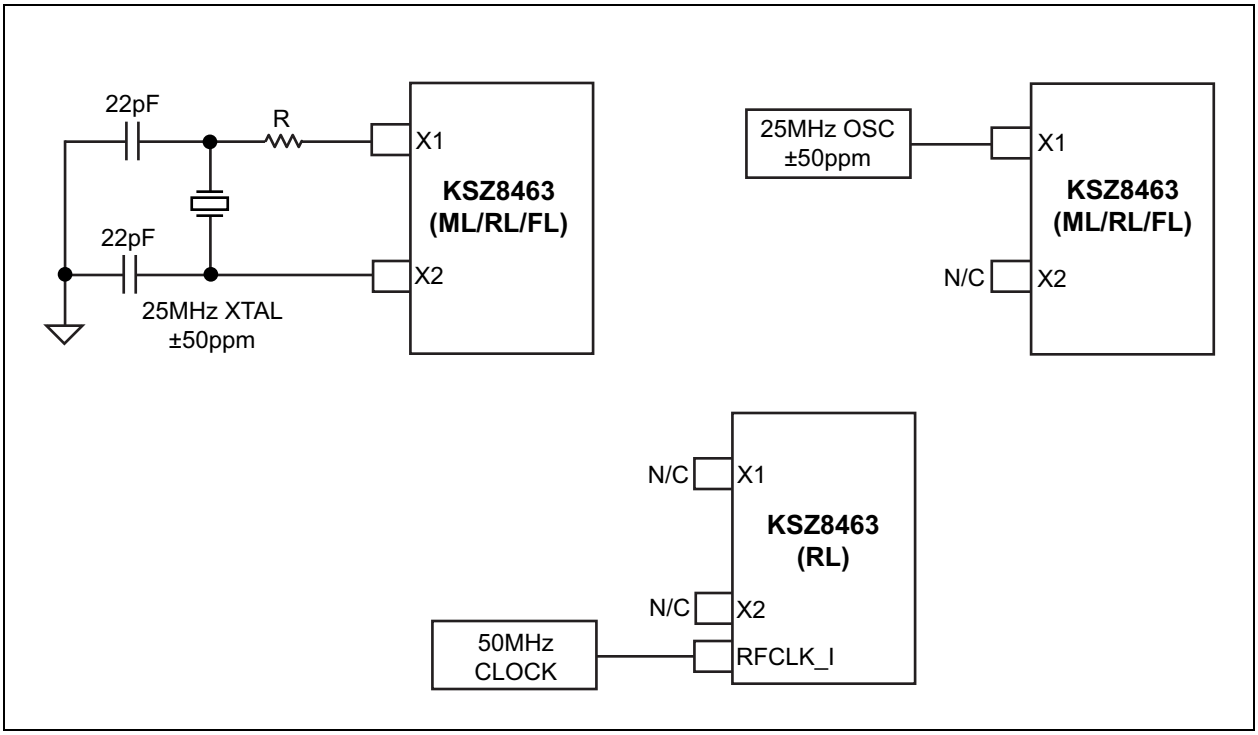


TABLE 8-1: TYPICAL REFERENCE CRYSTAL CHARACTERISTICS

Characteristics	Value
Frequency	25 MHz
Frequency tolerance (maximum)	±50 ppm
Effective Series resistance (maximum)	50Ω

9.0 SELECTION OF ISOLATION TRANSFORMERS

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements.

Table 9-1 lists recommended transformer characteristics.

TABLE 9-1: TRANSFORMER SELECTION CRITERIA

Parameter	Value	Test Conditions
Turns Ratio	1 CT:1 CT	—
Open-Circuit Inductance (min.)	350 µH	100 mV, 100 kHz, 8 mA
Leakage Inductance (max.)	0.4 µH	1 MHz (min.)
Interwinding Capacitance (max.)	12 pF	—
D.C. Resistance (max.)	0.9Ω	—
Insertion Loss (max.)	–1.0 dB	100 kHz to 100 MHz
HIPOT (min.)	1500 V_{RMS}	—

TABLE 9-2: QUALIFIED SINGLE-PORT MAGNETICS

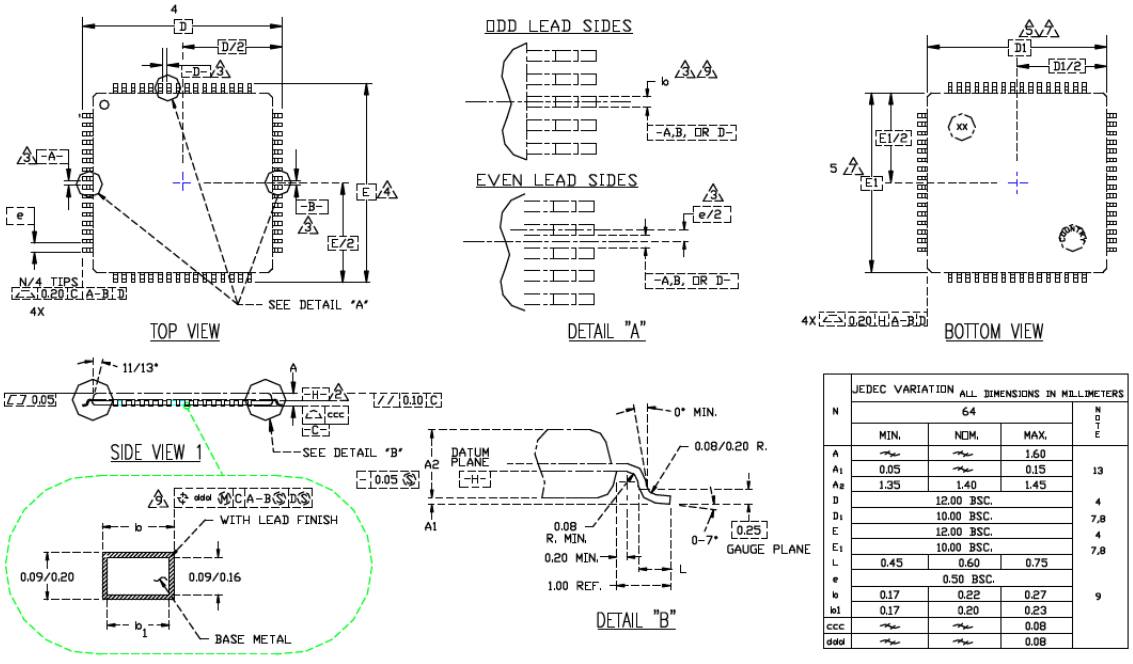
Manufacturer	Part Number	Auto MDI-X
Pulse	H1102NL	Yes
Pulse (low cost)	H1260	Yes
Transpower	HB726	Yes
Bel Fuse	S558-5999-U7	Yes
Delta	LF8505	Yes
LanKom	LF-H41S	Yes
TDK (Mag Jack)	TLA-6T718	Yes

10.0 PACKAGE OUTLINE

FIGURE 10-1: 64-LEAD LQFP 10 MM X 10 MM PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

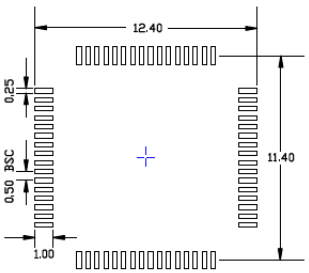
TITLE
64 LEAD LQFP 10x10mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	LQFP10x10-64LD-PL-1	UNIT	MM



N	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			NOTE
	64			
	MIN.	NOM.	MAX.	
A			1.60	
A1	0.05		0.15	13
A2	1.35	1.40	1.45	
D		12.00 BSC.		4
D1		10.00 BSC.		7,8
E		12.00 BSC.		4
E1		10.00 BSC.		7,8
L	0.45	0.60	0.75	
e		0.50 BSC.		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS -A-B- AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLANE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H- .
8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.38 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATIONS BCB, BCC, BCD & BCE.
13. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.



RECOMMENDED LAND PATTERN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002642A (2-22-18)	—	Converted Micrel data sheet KSZ8463ML/RL/FML/FRL to Microchip DS00002642A. Minor text changes throughout.

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PART NO.	X	X	X	—	XX
Device	Interface	Package	Temperature		Media Type

Device:	KSZ8463
Interface:	M = MII Interface R = RMII Interface FM = MII Interface with 100BASE-FX Fiber support FR = RMII Interface with 100BASE-FX Fiber support
Package:	L = 64-Lead LQFP
Temperature:	I = –40°C to +85°C (Industrial)
Media Type:	<blank> = 160/Tray

Examples:

a) KSZ8463MLI:	MII Interface, 64-Lead LQFP, Industrial Temperature, 160/Tray
b) KSZ8463FMLI:	MII Interface with 100BASE-FX Fiber support, 64-Lead LQFP, Industrial Temperature, 160/Tray
c) KSZ8463RLI:	RMII Interface, 64-Lead LQFP, Industrial Temperature, 160/Tray
d) KSZ8463FRLI:	RMII Interface with 100BASE-FX Fiber support, 64-Lead LQFP, Industrial Temperature, 160/Tray

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