KSZ8863MLL

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip KSZ8863MLL. These checklist items should be followed when utilizing the KSZ8863MLL in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary," on page 10. Detailed information on these subjects can be found in the corresponding sections:

2.0 GENERAL CONSIDERATIONS

2.1 Pin Check

Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.2 Ground

- The ground pin, **GND** and **AGND**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

3.0 POWER

- KSZ8863MLL 3.3V analog supply (**VDDA_3.3**) is on pin 5. A ferrite bead should be placed in series between the 3.3V supply and this pin. Be sure to place bulk capacitance on each side of the ferrite bead.
- The **VDDA_3.3** pin should have a 0.1 uF capacitor to decouple the device. The capacitor size should be SMD_0603 or smaller.
- Pins 22 and 40 (**VDDIO**) should be connected to the +1.8V, +2.5V, or +3.3V supply of the board.
- The 1.8V digital core supply (**VDDC**) is on pin 32. When **VDDIO** is 3.3V or 2.5V, connect this pin directly to the 1.8V regulator output (**VDDCO**) on pin 42. When **VDDIO** is 1.8V, an external 1.8V supply is required for this pin, and this pin should not be connected to **VDDCO**.
- KSZ8863MLL 1.8V analog supply (**VDDA_1.8**) is on pin 7. A ferrite bead should be placed in series between the 1.8V supply at pin 32 (**VDDC**) and this pin. Be sure to place bulk capacitance on each side of the ferrite bead.

The power and ground connections are shown in Figure 3-1 and Figure 3-2.

FIGURE 3-1: POWER AND GROUND CONNECTIONS FOR VDDIO = 3.3V OR 2.5V

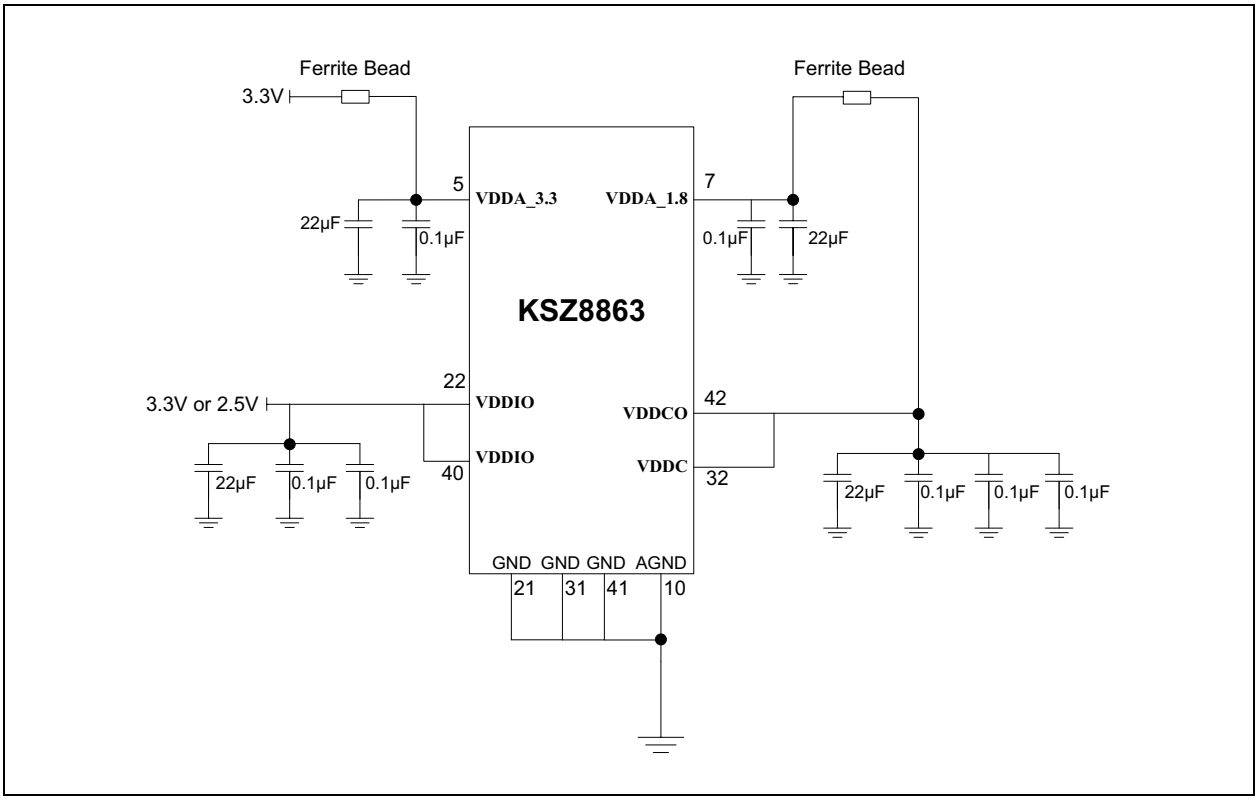
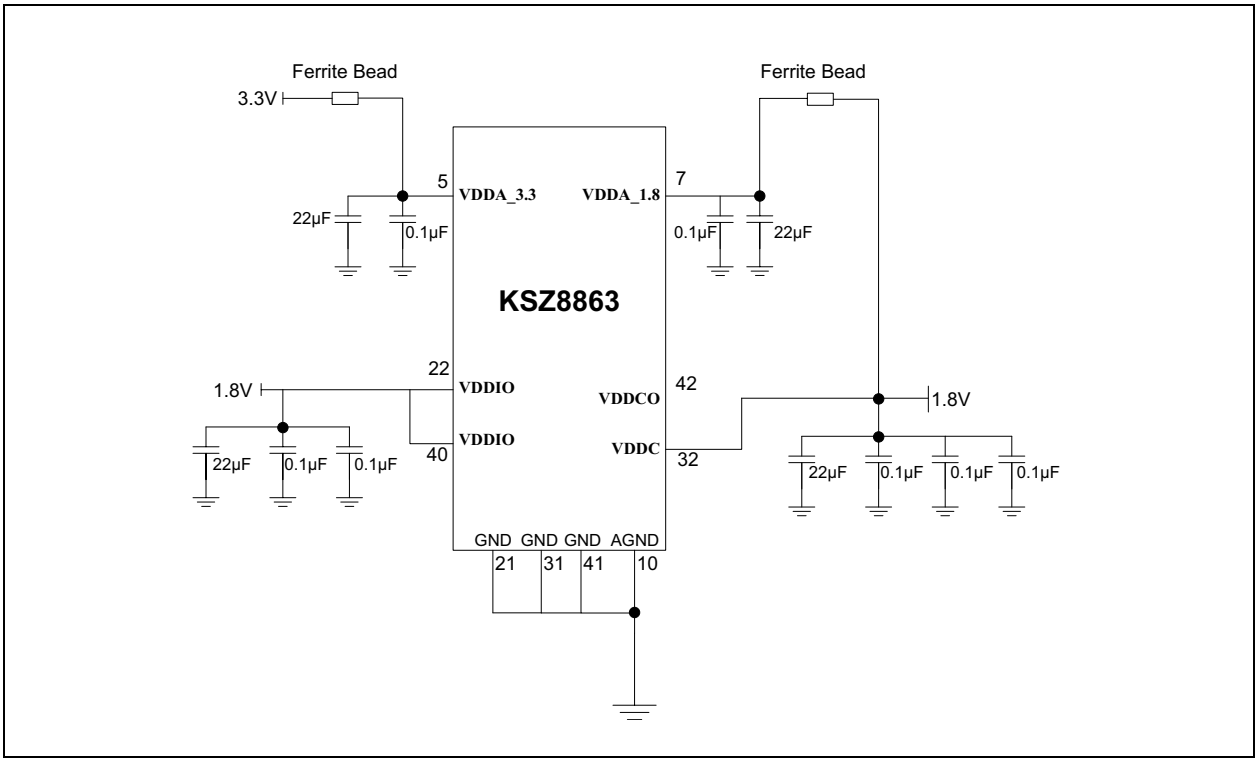


FIGURE 3-2: POWER AND GROUND CONNECTIONS FOR VDDIO = 1.8V



4.0 ETHERNET SIGNALS

4.1 PHY No. 1 Interface

- **TXP1** (pin 4): This pin is the transmit twisted pair output positive connection from the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- **TXM1** (pin 3): This pin is the transmit twisted pair output negative connection from the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- For transmit channel connection and termination details, refer to Figure 4-1.
- **RXP1** (pin 2): This pin is the receive twisted pair input positive connection to the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- **RXM1** (pin 1): This pin is the receive twisted pair input negative connection to the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- For receive channel connection and termination details, refer to Figure 4-2.

4.2 PHY No. 2 Interface

- **TXP2** (pin 12): This pin is the transmit twisted pair output positive connection from the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- **TXM2** (pin 11): This pin is the transmit twisted pair output negative connection from the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- For transmit channel connection and termination details, refer to Figure 4-1.
- **RXP2** (pin 9): This pin is the receive twisted pair input positive connection to the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- **RXM2** (pin 8): This pin is the receive twisted pair input negative connection to the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- For receive channel connection and termination details, refer to Figure 4-2.

FIGURE 4-1: TRANSMIT CHANNEL CONNECTIONS AND TERMINATIONS

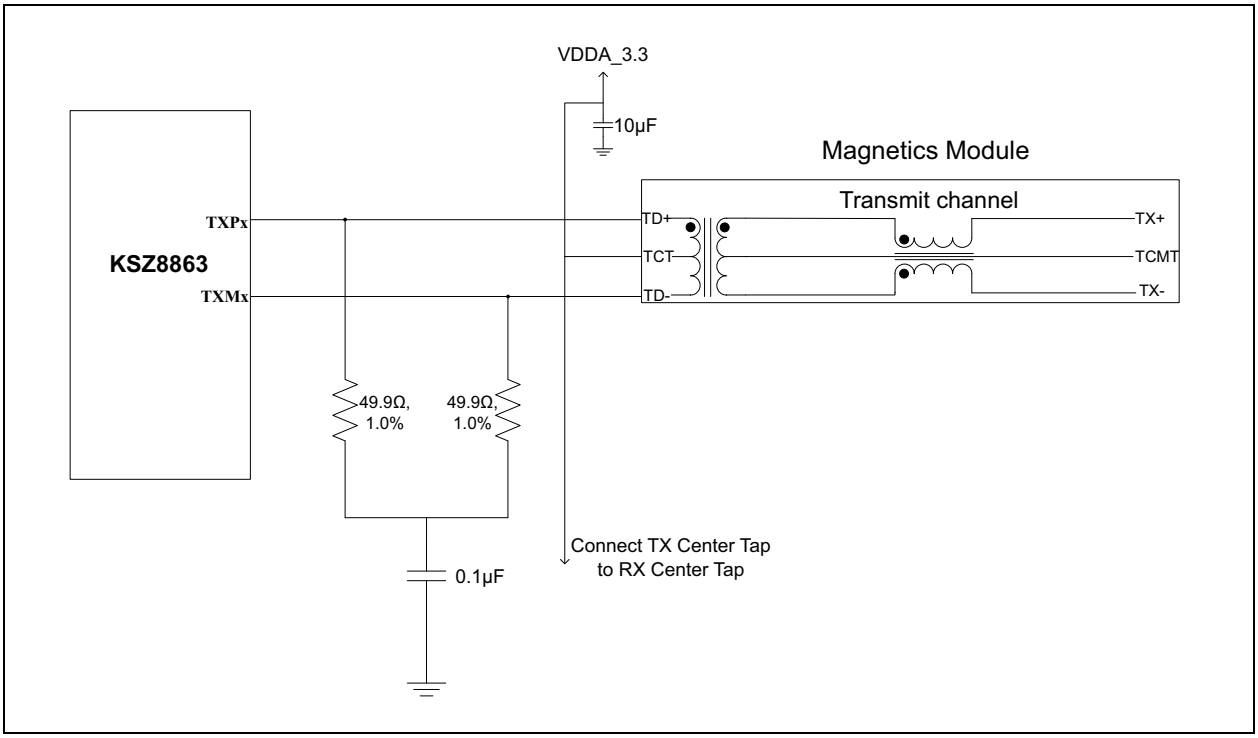
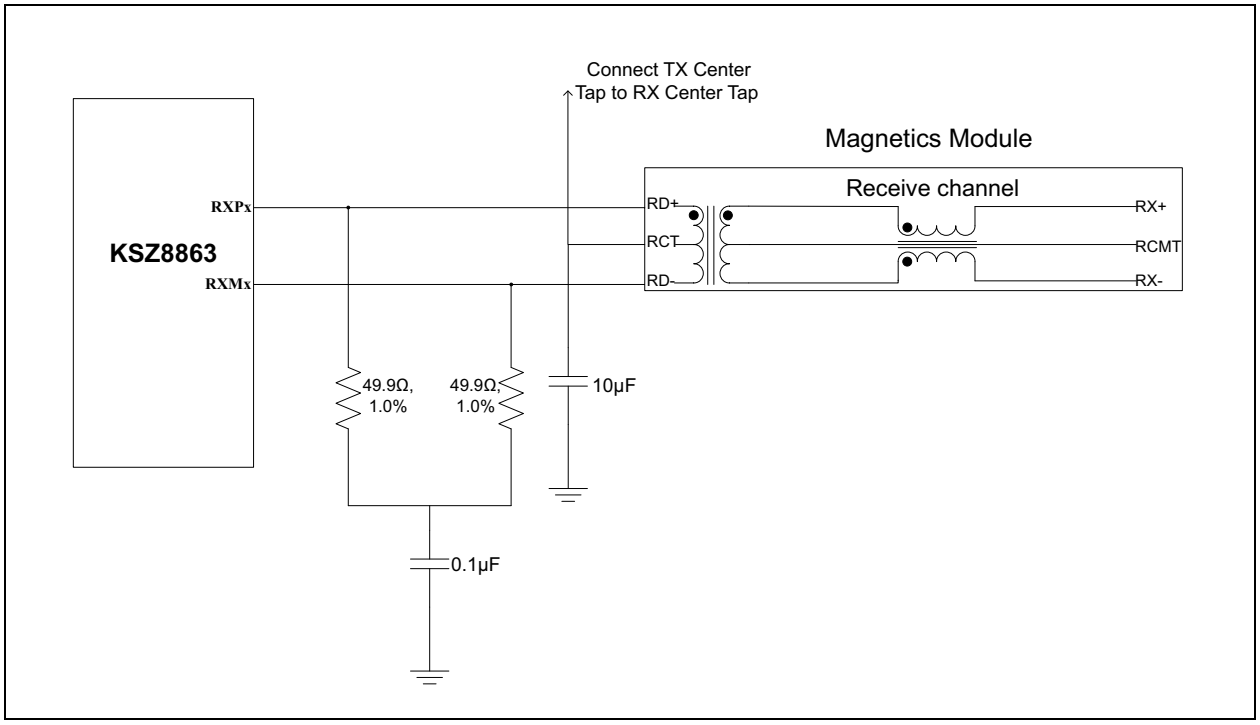


FIGURE 4-2: RECEIVE CHANNEL CONNECTIONS AND TERMINATIONS



4.3 Magnetics Connection

- The center tap connection on the KSZ8863MLL side for the transmit channel must be directly connected to **VDDA** (created from +3.3V). The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics. In addition, a 10 uF capacitor is required from the receive channel center tap of the magnetics to digital ground.
- The center tap connection on the KSZ8863MLL side for the receive channel is connected to the transmit channel center tap on the magnetics.
- The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 pF, 2 KV capacitor to chassis ground.
- The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 pF, 2 KV capacitor to chassis ground.
- Only one 1000 pF, 2 KV capacitor to chassis ground is required. It is shared by both TX and RX center taps.
- Assuming the design of an end-point device (NIC):
  - Pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXPx of the KSZ8863MLL.
  - Pin 2 of the RJ45 is TX– and should trace through the magnetics to TXMx of the KSZ8863MLL.
  - Pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXPx of the KSZ8863MLL.
  - Pin 6 of the RJ45 is RX– and should trace through the magnetics to RXMx of the KSZ8863MLL.
- When using the KSZ8863MLL device in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required.

4.4 RJ45 Connector

- Pins 4 and 5 of the RJ45 connector interface to one pair of unused wires in CAT 5-type cables. These should be terminated to chassis ground through a 1000 pF, 2 KV capacitor. There are two methods of accomplishing this:
  - Pins 4 and 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 KV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like

a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. So, by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 KV capacitor to chassis ground, an equivalent circuit is created.

- Pins 7 and 8 of the RJ45 connector interface to one pair of unused wires in CAT 5-type cables. These should be terminated to chassis ground through a 1000 pF, 2 KV capacitor. There are two methods of accomplishing this:
  - Pins 7 and 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 KV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. Therefore, by shorting pins 7 and 8 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 KV capacitor to chassis ground, an equivalent circuit is created.
- The RJ45 shield should be attached directly to chassis ground.

5.0 CLOCK CIRCUIT

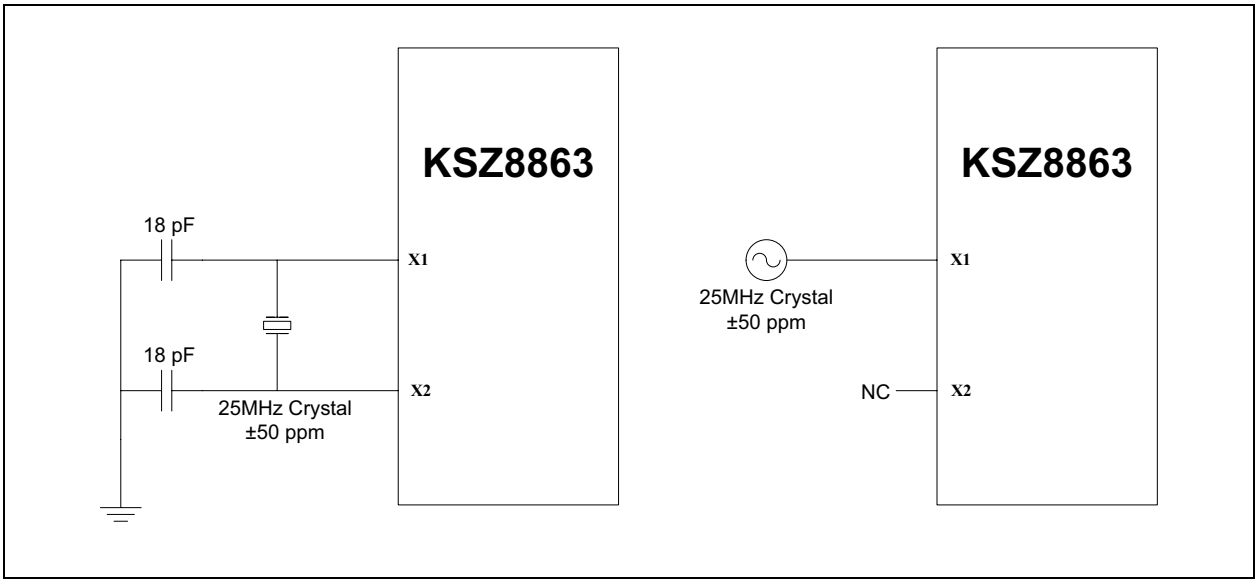
5.1 Crystal and External Oscillator/Clock Connections

When using the KSZ8863MLL, a 25.000-MHz (±50ppm) crystal should be used to provide the clock source. For exact specifications and tolerances, refer to the latest revision of the *KSZ8863MLL Data Sheet*.

- **X1** (pin 14) is the clock circuit input for the KSZ8863MLL device. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **X2** (pin 15) is the clock circuit output for the KSZ8863MLL device. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- Since every system design is unique, the capacitor values are system dependent based on the CL specifications of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.

Alternately, a 25.000 MHz clock oscillator may be used to provide the clock source for the KSZ8863MLL. When using a single-ended clock source, **X1** (pin 14) connects to a 3.3V-tolerant oscillator and **X2** (pin 15) should be left floating as No Connect (NC).

FIGURE 5-1: CRYSTAL AND OSCILLATOR CONNECTIONS



6.0 DIGITAL INTERFACES

6.1 MII Interface

- The MII that the KSZ8863MLL provides is connected to the device's third MAC port. The MII default is PHY mode and can be set to MAC mode with the register 53 bit 7. Table 6-1 describes the signals used by the MII bus.

Note: The external MAC signals should also be checked to ensure the pin types are consistent and match correspondingly with the KSZ8863MLL pin types (that is, MII outputs are connected to the corresponding MII inputs). Do not depend only on the pin names to match the MII pin connections between two devices.

TABLE 6-1: MII CONNECTIONS

PHY Mode Connections		Pin Description	MAC Mode Connections	
External MAC Controller Signal	KSZ8863MLL PHY Signal		External PHY Signal	KSZ8863MLL MAC Signal
MTXEN	SMTXEN3	Transmit Enable	MTXEN	SMRXDV3
MTXER	SMTXER3	Transmit Error	MTXER	(NOT USED)
MTXD3	SMTXD33	Transmit Data Bit 3	MTXD3	SMRXD33
MTXD2	SMTXD32	Transmit Data Bit 2	MTXD2	SMRXD32
MTXD1	SMTXD31	Transmit Data Bit 1	MTXD1	SMRXD31
MTXD0	SMTXD30	Transmit Data Bit 0	MTXD0	SMRXD30
MTXC	SMTXC3	Transmit Clock	MTXC	SMRXC3
MCOL	SCOL3	Collision Detection	MCOL	SCOL3
MCRS	SCRS3	Carrier Sense	MCRS	SCRS3
MRXDV	SMRXDV3	Receive Data Valid	MRXDV	SMTXEN3
MRXER	(NOT USED)	Receive Error	MRXER	SMTXER3
MRXD3	SMRXD33	Receive Data Bit 3	MRXD3	SMTXD33
MRXD2	SMRXD32	Receive Data Bit 2	MRXD2	SMTXD32
MRXD1	SMRXD31	Receive Data Bit 1	MRXD1	SMTXD31
MRXD0	SMRXD30	Receive Data Bit 0	MRXD0	SMTXD30
MRXC	SMRXC3	Receive Clock	MRXC	SMTXC3

- The KSZ8863MLL does not provide the MRXER signal for the PHY mode operation and the MTXER signal for the MAC mode operation. Normally, MRXER indicates a receive error coming from the physical layer device and MTXER indicates a transmit error from the MAC device. Because the switch filters error frames, these MII error signals are not used by KSZ8863MLL. Therefore, for PHY mode operation, if the device interfacing with KSZ8863MLL has an MRXER input pin, it needs to be tied low. For MAC mode operation, if the device interfacing with KSZ8863MLL has an MTXER input pin, it also needs to be tied low.
- Provisions should be made for series terminations for all outputs on the MII interface. Series resistors enable the designer to closely match the output driver impedance of the KSZ8863MLL and the PCB trace impedance to minimize ringing on these signals. Exact resistor values are application-dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors would be 22Ω.

6.2 Series Termination Resistor Values

TABLE 6-2: SERIES TERMINATION RESISTOR VALUES

Signal	Series Resistor Value
SMRXD33	22Ω
SMRXD32	22Ω
SMRXD31	22Ω
SMRXD30	22Ω
SMRXDV3	22Ω
SMRXC3	22Ω
SMTXC3	22Ω
SCOL3	22Ω
SCRS3	22Ω

6.3 Required External Pull-ups

- When using the MII interface of the KSZ8863MLL with a MAC device on board, a pull-up resistor of 4.7 kΩ on the **SDA_MDIO** signal (pin 37) is required.
- **INTRN** (pin 35) requires a 4.7 kΩ external pull-up resistor since this output is an open drain type. If **INTRN** is not used, the pull-up resistor is not required.

7.0 STARTUP

7.1 Reset Circuit

RSTN (pin 47) is an active-low reset input. This signal resets all logic and registers within the KSZ8863MLL. A hardware reset (**RSTN** assertion) is required following power-up. Please refer to the latest copy of the *KSZ8863MLL Data Sheet* for reset timing requirements. Figure 7-1 shows a recommended reset circuit for powering up the KSZ8863MLL device when reset is triggered by the power supply.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

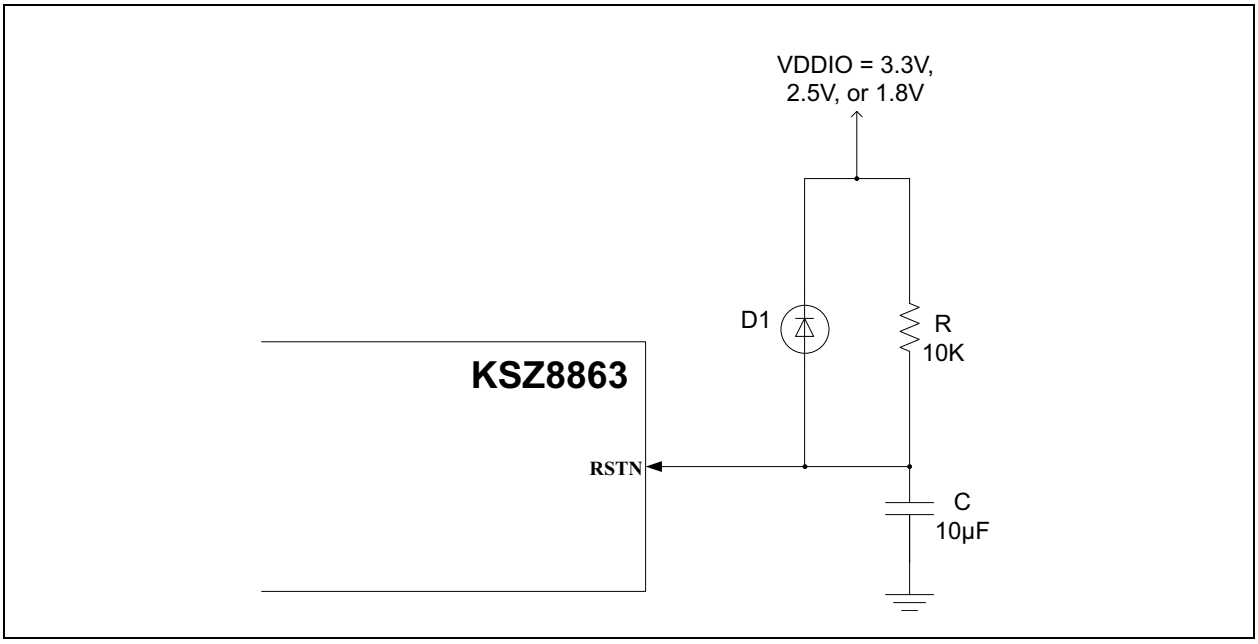
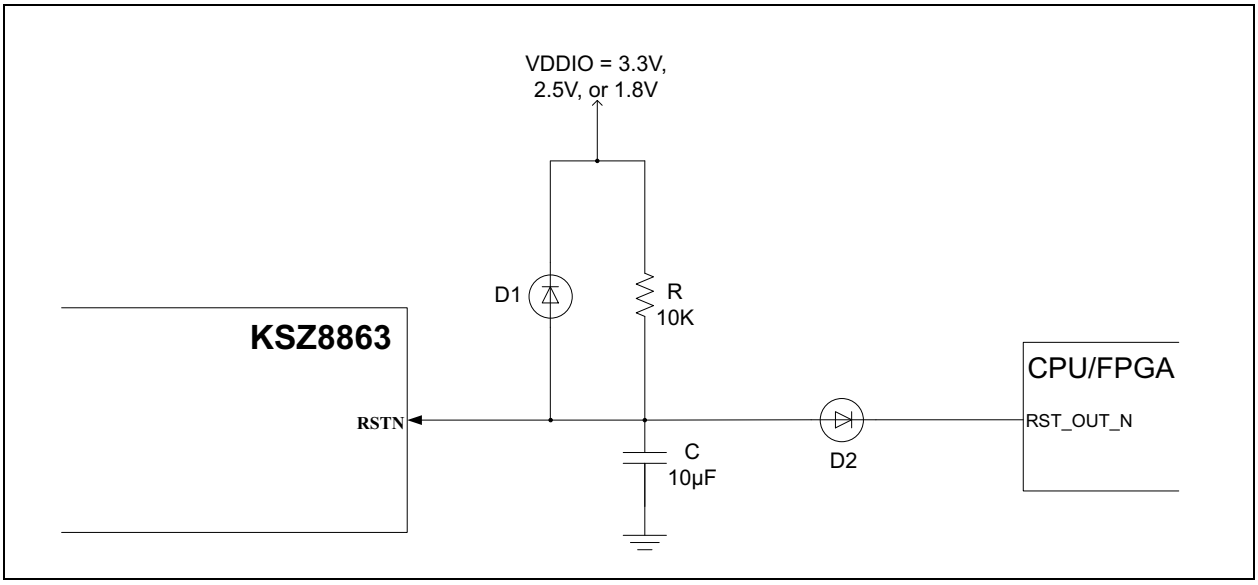


Figure 7-2 shows the recommended reset circuit for applications where reset is driven by an external CPU or FPGA. The reset out pin, RST_OUT_N, from CPU/FPGA provides the warm reset after power-up. If the Ethernet device and CPU/FPGA use the same VDDIO voltage, D2 can be removed and both reset pins can be connected directly.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/FPGA RESET OUTPUT



7.2 Configuration Mode Pins (Strapping Options)

The default configuration of the 10/100 PHY for Speed, Duplex, Autonegotiation, flow control and Serial Bus mode functionality can be configured through strip option pins. The value of these ten pins are latched in upon power-up and reset. As indicated in the data sheet, each of these pins has either an internal pull-up or pull-down resistor to set the default strapping level. To choose the non-default option for a strapping pin, an external pull-up or pull-down resistor is needed. Resistor values can be 1 kΩ to 10 kΩ, except for pull-down resistors on LED pins that should be 1 kΩ or less to ensure they are pulled adequately low during reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the MII/RMII signals to be latched high. Refer to the *KSZ8863MLL Data Sheet* for the complete details on the operation of strapping pins.

The strapping option for pin 44 (P1LED0) determines whether port 1 autonegotiation is enabled or disabled. This pin has an internal pull-down, causing port 1 autonegotiation to be disabled by default. To enable port 1 autonegotiation, this pin needs an external 10 kΩ resistor to VDDIO.

It is also important to ensure that pins 45 and 46 (P2LED1 and P2LED0) strapping settings are correct for selecting the Serial Bus mode: either I^2C master (EEPROM), I^2C slave, SPI, or SMI/MIIM.

7.3 LED Pins

- The KSZ8863MLL provides two LED signals per port. These indicators display speed, link, and activity information about the current state of the PHY ports. The LED pins are active low and require a 220Ω series resistor. See *KSZ8863MLL Data Sheet* for further details on how to strap each pin for correct operation.

8.0 MISCELLANEOUS

8.1 ISET Resistor

ISET (pin 6) on the KSZ8863MLL should connect to digital ground through a 11.8 kΩ resistor with a tolerance of 1.0%. This pin is used to set up critical bias currents for the embedded 10/100 Ethernet physical device.

8.2 Other Considerations

- Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. This allows some flexibility at EMI testing for different grounding options. Leaving the footprint open allows the two grounds to remain separate. Shorting them together with a 0Ω resistor will connect them. For best performance, short them together with a cap or a ferrite bead.
- Be sure to incorporate enough bulk capacitors (4.7 µF to 22 µF) for each power plane.

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	N
Section 2.0, "General Considerations"	Section 2.1, "Pin Check"	Verify if the pins match the data sheet.		
	Section 2.2, "Ground"	Verify if grounds are tied together.		
Section 3.0, "Power"	Section 3.0, "Power"	• Ensure that **VDDA_3.3** is in the range 3.135V to 3.465V, and a 22 µF capacitor is on each pin. • Ensure that **VDDIO** is connected to 3.3V, 2.5V, or 1.8V, with a ±5% tolerance each. Operating ranges are as follows: - 3.135V to 3.465V for 3.3V - 2.375V to 2.625V for 2.5V - 1.710V to 1.890V for 1.8V • If **VDDIO** is 3.3V or 2.5V, use pin 42 as the 1.8V power source, and do not use an external 1.8V source. • If **VDDIO** is 1.8V, leave pin 42 open, and use an external 1.8V source for pins 32 and 7. • Ferrite beads are recommended for **VDDA_3.3** and **VDDA_1.8**.		
Section 4.0, "Ethernet Signals"	Section 4.1, "PHY No. 1 Interface"	Verify the termination resistors (49.9Ω, 1.0%) and capacitors (0.1 uF) on the TX and RX pins.		
	Section 4.2 “PHY No. 2 Interface”	Verify the termination resistors (49.9Ω, 1.0%) and capacitors (0.1 uF) on the TX and RX pins.		
	Section 4.3, "Magnetics Connection"	Verify if the center taps are connected to the **VDDA_3.3** (pin 3) supply on the KSZ8863MLL device side and are terminated with 75Ω resistors through a 1000 pF, 2 kV capacitor to chassis ground on the RJ45 line side.		
	Section 4.4, "RJ45 Connector"	Verify if pins 4/5 and 7/8 of the RJ45 connect to CAT 5 cable and are terminated to chassis ground through a 1000 pF, 2 kV capacitor.		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	N
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal and External Oscillator/Clock Connections"	Verify usage of 25 MHz (±50 ppm) crystal or external oscillator/clock.		
Section 6.0, "Digital Interfaces"	Section 6.1, "MII Interface"	Confirm proper MII signals between MAC and PHY interface with correct series termination resistors. (22Ω).		
	Section 6.2 “Series Termination Resistor Values”	Confirm proper MII signals between MAC and PHY interface with correct series termination resistors. (22Ω).		
	Section 6.3 “Required External Pull-ups”	• A 4.7 kΩ pull-up on SDA_MDIO signal is required when using MII interface with a MAC device. • A 4.7 kΩ pull-up is required if INTRN signal is used.		
Section 7.0, "Startup"	Section 7.1, "Reset Circuit"	Confirm proper reset circuit design: standalone reset or external CPU/FPGA reset.		
	Section 7.2 “Configuration Mode Pins (Strapping Options)”	• Confirm if the strapping options are correctly configured as per the application requirements. • To choose the non-default option, an external pull-up or pull-down of 1 kΩ to 10 kΩ should be used.		
	Section 7.3, "LED Pins"	If used, confirm proper connections, taking into consideration shared functionality on select LED pins.		
Section 8.0, "Miscellaneous"	Section 8.1, "ISET Resistor"	Confirm proper ISET resistor (11.8 kΩ, 1.0%) with a 100 uF capacitor in parallel.		
	Section 8.2, "Other Considerations"	• Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. • Incorporate sufficient power plane bulk capacitors (4.7 µF to 22 µF).		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002713A (06-14-18)	Initial release.	

NOTES:

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