Le79272 SLIC

Dual Subscriber Line Interface Circuit

Next Generation Carrier Chipset (NGCC)

APPLICATIONS

- **Cost-effective voice solution for long or short loops providing POTS and integrated test capabilities**
  - IVD
  - CO, DLC
  - Voice-enabled DSLAM
  - PBX/KTS
  - MDU, MSAP, MSAN

FEATURES

- **Designed to minimize POTS transients, optimizing CRC performance for triple play applications**
- **Best-in-class GR-844 equivalent testing**
  - Fully validated test primitives and host routines
  - Guaranteed performance parameters
- **Optimized for best-in-class density**
- **Monitor of two-wire interface voltages and currents supports:**
  - Voice transmission
  - Internal ringing generation
  - Programmable DC feed characteristics
    - Current limited and independent of battery
  - Selectable off-hook and ground-key thresholds
  - Subscriber line diagnostics
    - Leakage and loop resistance
    - Line capacitance and bell capacitance
    - Foreign voltage sensing
  - Power cross and fault detection
- **Supports 85 Vrms internal ringing**
  - Supports balanced and unbalanced ringing
- **3.3 V and battery supplies**
  - Supports two negative and one positive battery
- **Dual battery operation for system power saving**
  - Automatic battery switching
  - Intelligent thermal management
- **Compatible with inexpensive protection networks**
- **Metering capable**
  - 12 kHz and 16 kHz
  - Smooth polarity reversal
- **Tip-open mode supports ground start signaling**
- **Integrated test load switch**
- **5 REN with DC offset**

FEATURES WITH LE79124 NGVCP

- **72 channel call aggregation**
- **GR-844 equivalent line testing**

ORDERING INFORMATION

An Le79238 or ZL79258 SLAC device must be used with this part.

Device	Package Type (Green)[1]	Packing[2]
Le79272PQC	48-Pin QFN	Tray

1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

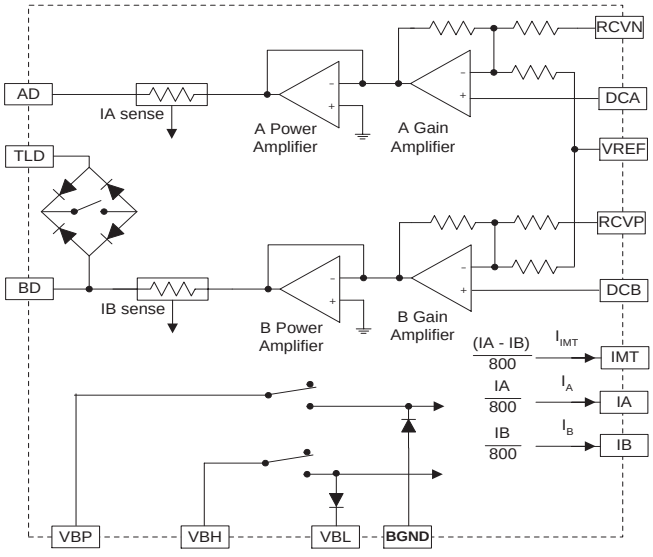
DESCRIPTION

The Le79272 Next Generation Dual Subscriber Line Interface Circuit (SLIC) device, in combination with an NGCC SLAC device, implements a DSL friendly, high density universal telephone line interface. This enables the design of a low cost, high performance, fully software programmable line interface with worldwide applicability. All AC, DC, and signaling parameters are programmable. Additionally, the NGCC has integrated self-test and line-test capabilities to resolve faults to the line or line circuit.

RELATED LITERATURE

- **126583 NGCC Hardware Design Guide**
- **128623 NGCC Designer's Guide**
- **081555 Le79271 NGSLIC Device Data Sheet**
- **081193 Le79238 Octal NGSLAC Device Data Sheet**
- **136868 ZL79258 Octal External Ringing NGSLAC Device Data Sheet**
- **081567 Le79124 NGVCP Device Data Sheet**

BLOCK DIAGRAM (1 CHANNEL)



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PRODUCT DESCRIPTION

Microsemi's Next Generation Carrier Chipset (NGCC) integrates all functions required to interface to a subscriber line. Two chip types are used to implement the line card — the Le79272 SLIC device and an NGSLAC device. These provide the following basic functions:

1. The Le79272 Next Generation Dual SLIC device: A high voltage, bipolar device that drives the subscriber lines and senses line conditions. The Le79272 is a dual channel device (two channels per package).
2. The Le79238 or ZL79258 Next Generation Octal SLAC devices: Low voltage CMOS IC that provides conversion, control and DSP functions for four Le79272 devices and senses line conditions.

The Le79272 device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It is controlled by the NGSLAC device to operate in different modes that control power consumption and signaling. The Le79272 device is designed to be used exclusively with the NGSLAC device. The Le79272 device requires only VCC and the battery supplies for its operation.

The Le79272 SLIC device functions as the interface between the low-voltage NGSLAC device and the high-voltage POTS loop. The basic SLIC architecture is voltage feed and current sense. In the 4-Wire to 2-Wire (receive) direction it provides two gain paths to the POTS loop (A & B Leads). One path is used to feed DC and ringing signals to the loop. The second is used to feed AC transmission and PPM signals to the loop. The drive amplifiers can deliver at least ±120 mA to the loop for the transmission, DC feed and ringing signals. In the 2-Wire to 4-Wire (transmit) direction the SLIC senses the AC and DC current in the loop and translates these currents into signals that are compliant with the low-voltage circuitry in the NGSLAC. It passes three currents to the NGSLAC – one current equal to the A-Lead current divided by 800, one current equal to the B-Lead current divided by 800, and one current equal to the A-Lead current minus the B-Lead current divided by 800 (the loop metallic current divided by 400). The SLIC provides no signal processing other than gain and level conversion for these transmit and receive signals. Any signal processing required to support the Le79272 feature set is provided by the NGSLAC device and associated digital processor.

The SLIC device provides the necessary high-voltage functions that the NGSLAC device cannot implement using low-voltage signal processing. The SLIC device has a normal operating mode (for transmission, supervision, etc.), a Tip Open mode (high impedance A-Lead), a Ring Open mode (high impedance B-Lead) and a Disconnect mode (high impedance A-Lead and B-Lead). The normal, Tip Open and Ring Open modes are available with either standard or low-power (for power conservation) biasing. The functionality of each mode in low-power biasing is identical to standard biasing, except that some operational limits and/or accuracies may be reduced. The standard biasing modes are Active (normal transmission, DC feed, supervision and ringing), Tip Open Test and Ring Open Test; the low-power modes are Standby (reduced transmission, DC feed, supervision and ringing capability), Tip Open (ground start supervision) and Ring Open. Switching the SLIC from Active to Standby or from Standby to Active is designed not to create transients that could cause CRC errors in IVD applications, provided that the customer end is properly terminated. When the SLIC is programmed in any of the low-power modes, it will automatically switch to the corresponding standard mode when the current in either the A-Lead or B-Lead exceeds ~±15 mA. In order to return to the low-power mode, the device must be reprogrammed via the latched data bus (P-bus (P0-P2, SEL)). All operating modes and switches are controlled by the NGSLAC device via the P-bus.

The SLIC device also provides two internal switches (per channel) that connect the internal supply rails to alternative power supplies in order to minimize power consumption under various operating conditions. Switch operation is designed not to create transients that could cause CRC errors in IVD applications. The device also provides a switch (per channel) that is used to connect the B-Lead to the A-Lead through an external resistor for line testing.

Per channel thermal protection is provided internally to protect the device during fault conditions. When a channel's device temperature exceeds a temperature threshold the thermal protection automatically places the respective drive amplifiers in the Disconnect mode and turns the Test Switch off. When the device cools, the thermal protection returns the device to the operating mode and switch configuration that it was in prior to thermal overload.

The SLIC device is designed to provide balanced and unbalanced ringing, with or without dc offset, to the subscriber loop.

The NGSLAC device contains high-performance circuits that provide A/D and D/A conversion for voice (codec/filter), DC-feed control, ringing, and supervision signals. The NGSLAC device contains a DSP core that handles signaling, DC-feed, supervision and line diagnostics for all eight channels. The DSP core also interfaces to a standard PCM/MPI backplane. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or µ-law.

The NGSLAC device provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, the NGSLAC device provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

User-programmable filters include receive and transmit gain, transhybrid balance, two-wire termination impedance, and frequency attenuation (equalization) of the receive and transmit signals. All programmable digital filter coefficients can be

calculated using WinSLAC™ software. This PC software allows the designer to enter a description of system requirements, WinSLAC™ then computes the necessary coefficients and plots the predicted system results.

The main functions that can be observed and/or controlled through the NGSLAC device backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring trip detection
- Abrupt and smooth battery reversal
- Subscriber line impedance matching
- Transmit and receive paths frequency response
- 4-wire to 2-wire hybrid impedance balance, or transhybrid loss
- DTMF detection (Q.24 compliant)
- Dial Pulse detection and decode
- Ringing signal generation
- Sophisticated line and circuit tests

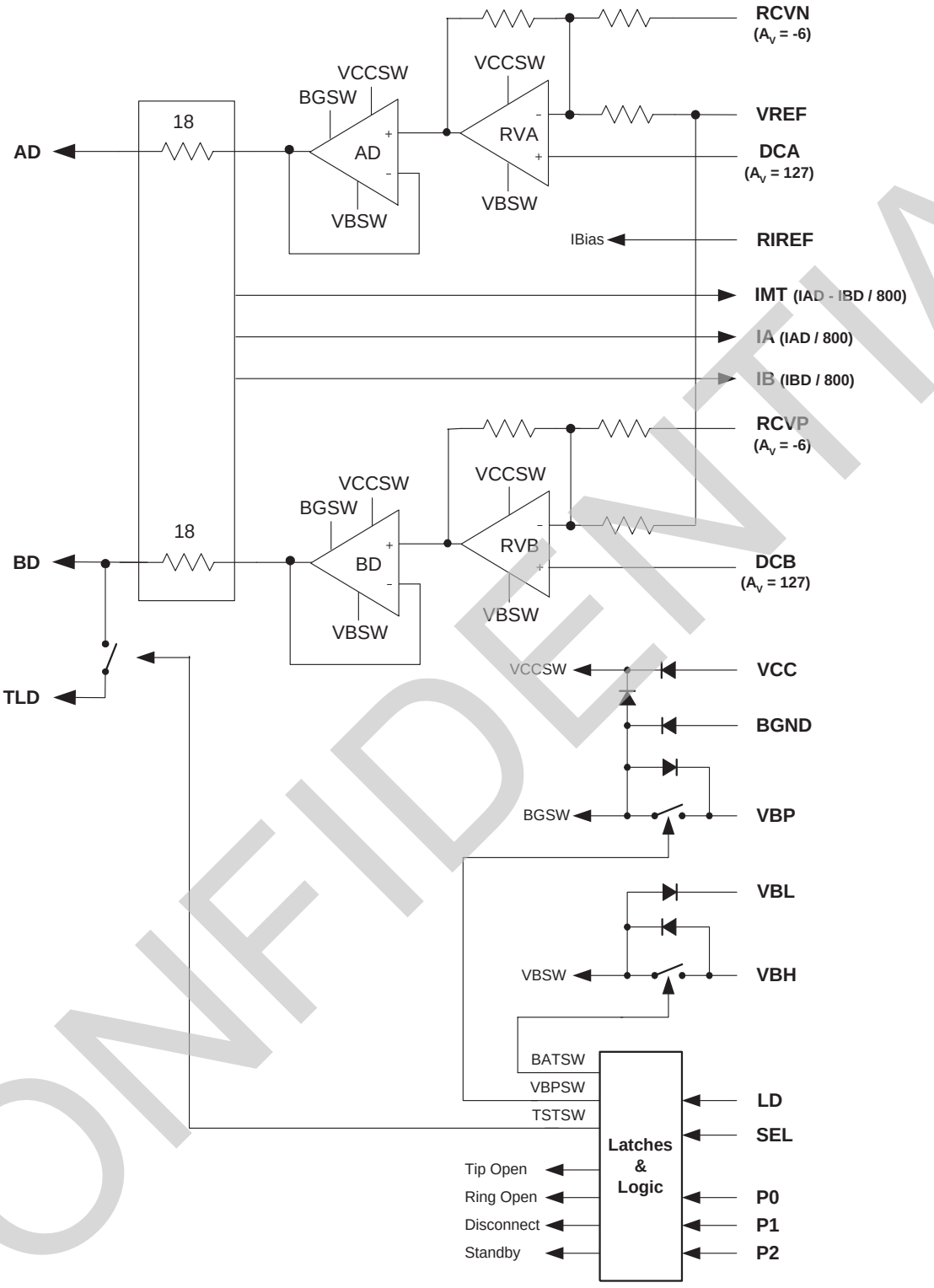
Refer to the *Next Generation Carrier Chipset Hardware Design Guide (Document ID 126583)* for detailed Application Circuits and Parts Lists for various applications using the Le79272 SLIC device, the Le79238 and ZL79258 SLAC devices, and the Le79124 and Le79234 VCP devices.

Next Generation VCP Features

The optional Le79124 Next Generation Voice Control Processor (NGVCP) provides the following features to the chip set:

- Provides expanded line and circuit testing in conjunction with Microsemi's NGCC
  - Le79272 SLIC device features extremely low leakage and tight gain tolerances for high accuracy measurements
- Aggregated call control lowers demand on host micro-processor
- Software interface using VoicePath™ API-II
- Software downloadable, field upgradeable, expandable
- Two Master SPI ports
- Two Slave PCM Highway ports
  - Single or dual PCM highways capable of operating up to 16.384 MHz
- Internal PLL and hardware network timing recovery for creating analog sampling clocks
- Real Time clock capable of being driven from the slave PCM clock
- Host controller interface options
- 32 General Purpose I/Os
- Internal 3.3 V to 1.8 V linear regulator for the core logic

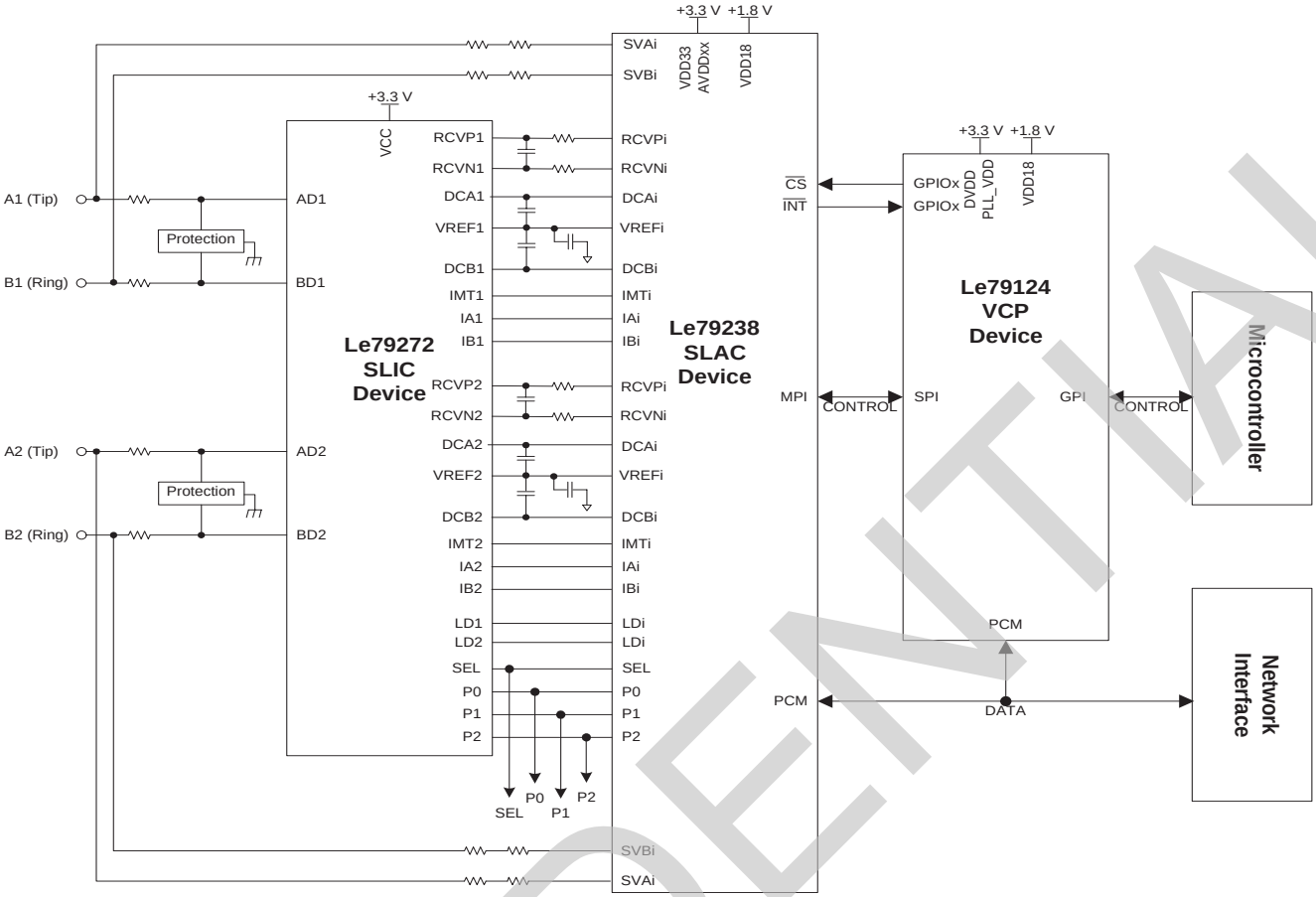
Figure 1. Le79272 Device Internal Block Diagram (1 Channel)



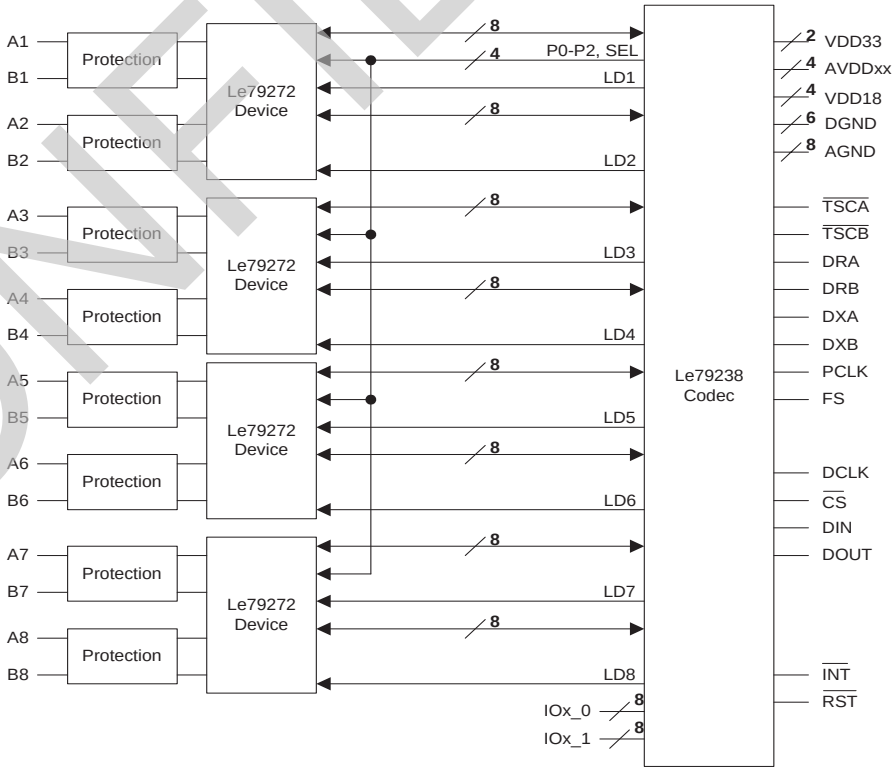
Features of the NGCC

- Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions
- Controlled state changes to eliminate transients that could cause CRC errors
- Two or three chip solution supports high density, multi-channel architecture
- Supports two negative batteries and one positive battery
- Single hardware design meets multiple country requirements through software programming of:
  - Ringing waveform and frequency
  - DC loop-feed characteristics and current-limit
  - Loop-supervision detection thresholds
  - Off-hook debounce circuit
  - Ground-key and ring-trip filters
  - Off-hook detect de-bounce interval
  - Two-wire AC impedance
  - Transhybrid balance impedance
  - Transmit and receive gains
  - Equalization
  - Digital I/O pins
  - A-law/µ-law and linear selection
- Supports internal battery-backed ringing
  - Programmed ringing cadence
  - Self-contained ringing generation and control
  - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Supports metering generation with envelope shaping
  - Programmable metering cadencing
- Smooth polarity reversal
- Supports both loop-start and ground-start signaling
- SPI and PCM interfaces
- Exceeds LSSGR and CCITT central office requirements
- On-hook transmission
- Power/service denial mode
- Line-feed characteristics independent of battery voltage
- Low idle-power per line
- Compatible with inexpensive protection networks
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Can monitor and/or drive A and B lead independently
- Automatic CID and Signaling and FSK and DTMF modes
- Tone generation
  - Howler
  - Call Progress
  - DTMF
- Modem support
- DTMF tone detection
- Dial Pulse and Flash detection
- Power-cross, fault, and foreign voltage detection
- Integrated line-test and self-test features
  - GR-909 and GR-844 equivalent
  - Built-in voice path test modes
  - 15 kHz noise filter
- Small physical size

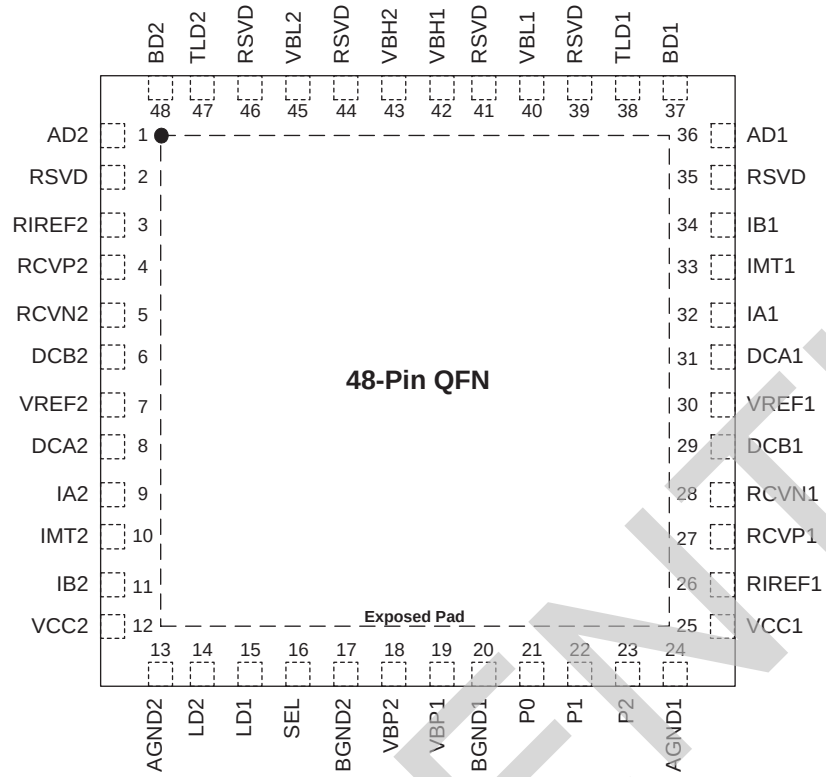
NGCC WITH NEXT GENERATION VCP DEVICE



NGCC BLOCK DIAGRAM - EIGHT CHANNEL LINE CARD EXAMPLE



CONNECTION DIAGRAM



TOP VIEW

PIN DESCRIPTIONS

Pin Name	Pin #	Type	Description
AD [1,2]	36, 1	Output	Provides the drive voltage to the A lead of the subscriber loop.
BD [1,2]	37, 48	Output	Provides the drive voltage to the B lead of the subscriber loop.
AGND [1,2]	24, 13	Ground	Analog ground return for VCC.
BGND [1,2]	20, 17	Ground	Ground return for the VBH, VBL and VBP battery supplies.
DCA [1,2]	31, 8	Input	The voltage on output AD is equal to VREF plus 127 times the difference of the voltage between DCA and VREF. This input is used to supply DC and ringing voltages to the A-Lead.
DCB [1,2]	29, 6	Input	The voltage on output BD is equal to VREF plus 127 times the difference of the voltage between DCB and VREF. This input is used to supply DC and ringing voltages to the B-Lead.
EPAD		Exposed Pad	Power dissipation pad - connect to BGND.
IA [1,2]	32, 9	Output	IA is proportional to the current in the AD lead (loop A-Lead current).
IB [1,2]	34, 11	Output	IB is proportional to the current in the BD lead (loop B-Lead current).
IMT [1,2]	33, 10	Output	IMT is proportional to the differential current in the AD and BD leads. Thermal overload is indicated by forcing IMT to AGND. This output is used to supply the metallic transmission (transmit) voltage from the loop.
LD [1,2]	15, 14	Input	Logic input that controls the data transfer into the data latches. When LD is Low, the data on inputs P0–P2 is transferred to the respective data latches as directed by the SEL pin. When LD is High, the data is locked in the latches.
P0–P2	21, 22, 23	Input	Logic inputs to the latches for the operating mode decoder and switches.
RCVN [1,2]	28, 5	Input	Receive AC Signal Input (Inverting). The voltage on output AD is equal to VREF minus 6 times the difference of the voltage between RCVN and VREF. This input, in conjunction with RCVP, is used to supply the metallic transmission voltage to the loop.
RCVP [1,2]	27, 4	Input	Receive AC Signal Input (Non Inverting). The voltage on output BD is equal to VREF minus 6 times the difference of the voltage between RCVP and VREF. This input, in conjunction with RCVN, is used to supply the metallic transmission voltage to the loop.
RIREF [1,2]	26, 3	Input	External resistor connected from RIREF to AGND sets the internal bias currents for the Le79272.
RSVD	2, 35, 39, 41, 44, 46	Reserved	No connect pins necessary for voltage separation. May not be used as a tie point.
SEL	16	Input	Logic input that selects data inputs P0–P2 to either control the operating modes or the switches.
TLD [1,2]	38, 47	Output	Resistor connected from this pin to AD is connected from AD to BD when the Test Switch is programmed on.
VBH [1,2]	42, 43	Battery (Power)	High negative battery supply. Connect these pins together.
VBL [1,2]	40, 45	Battery (Power)	Low negative battery supply. Used to save power during Off-Hook for short loops. Connect directly to VBH pins if only one negative battery is used.
VBP [1,2]	19, 18	Battery (Power)	Positive battery supply. Connect these pins together. Used for ringing and very long loops. If positive supply is not used, connect these pins to BGND.
VCC [1,2]	25, 12	Power Supply	Positive 3.3 V supply for low voltage analog and digital circuits.
VREF [1,2]	30, 7	Input	Reference voltage provided by the NGSLAC that the SLIC uses for an internal reference. Analog inputs RCVP, RCVN, DCA and DCB are referenced to this pin.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(T_A = 23°C)

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	–55 to +150°C
Ambient Temperature under Bias; Humidity	–40 to +85°C; 5% to 95%
VBP with respect to AGND	–0.4 to +110 V
VBP with respect to VBH	–0.4 to +160 V
VCC with respect to AGND	–0.4 to +4 V
VBH with respect to AGND	+0.4 to –150 V
VBL with respect to AGND	+0.4 to –80 V
VBL with respect to VBH	$\lvert VBL \rvert \leq \lvert VBH \rvert + 1$ V and (VBL - VBH) < 90 V
BGND with respect to AGND	–3 to +3 V
Test Switch On-mode Current	100 mA
AD, BD and TLD: Continuous 10 ms (F = 0.1 Hz) 1 µs (F = 0.1 Hz) 250 ns (F = 0.1 Hz)	 VBH – 3 to VBP + 3 VBH – 5 to VBP + 5 VBH – 10 to VBP + 10 VBH – 15 to VBP + 15
Current through AD or BD	± 150 mA
Digital Control Inputs to AGND	–0.4 to VCC + 0.4 V
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

Thermal Resistance

Thermal resistance is discussed in the *Next Generation Carrier Chipset Hardware Design Guide*.

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane.

Package Assembly

Green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. Refer to IPC/JEDEC J-Std-020 for recommended peak soldering temperature and solder reflow temperature profile.

Electrical Operating Ranges

Microsemi guarantees the performance of this device over commercial (0ºC to 70ºC) and industrial (-40ºC to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with the Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	–40 to +85 °C
Ambient Relative Humidity	15% to 85%

Electrical Ranges

VCC*	+3.3 V ± 5%
VBL*	–15 to –80 V, with the constraint of $\|VBL\| \leq \|VBH\|$
VBH*	–40 to –145 V
VBP*	AGND to +100 V
Maximum supply voltage across device, VBP - VBH	150 V
BGND with respect to AGND	–300 to +300 mV

** If the power supply rails are floating before being connected to the power source (a typical hot insertion), no power-up sequencing is required, except to apply AGND and BGND first. However, if the power supply rails are switched or ramped from ground to their final operating voltages, VBH must be applied before VBL, or a diode must be included in series with the VBH supply in order to prevent reverse current flow from VBL to VBH.*

SPECIFICATIONS

Power Dissipation

VBH = –48 V, VBL = –24 V, VCC = +3.3 V, VBP = +48 V

All power numbers are per channel when on-hook with no loop current and no load.

Table 1. Power Dissipation Specifications (Per Channel)

Operating Mode	Operating Condition	Test Condition	Min	Typ	Max	Unit
Disconnect	BATSW Off, VBPSW Off			8	15	mW
Standby	BATSW On, VBPSW Off			35	42	
Active	High Battery: BATSW On, VBPSW Off	Normal or Reverse Polarity		87	104	
	Low Battery: BATSW Off, VBPSW Off			47	58	
	Boosted Battery (Ringing): BATSW On, VBPSW On			187	217	
Tip Open	BATSW On, VBPSW Off			32	38	

Supply Currents

VBH = –60 V, VBL = –36 V, VCC = +3.3 V, VBP = +60 V

All supply currents are per channel when on-hook with no loop current and no load.

Test conditions are the same as listed in Power Dissipation Specifications, Table 1.

Operating Mode	Operating Condition	Parameter	Min	Typ	Max	Unit
Disconnect	BATSW Off, VBPSW Off	I_{VCC}		2.3	3.0	mA
		I_{VBH}		0.1	20.0	µA
		I_{VBL}		27.0	100.0	µA
		I_{VBP}		1.0	20.0	µA
Standby	BATSW On, VBPSW Off	I_{VCC}		2.5	2.8	mA
		I_{VBH}		0.55	0.65	mA
		I_{VBL}		0.35	2.0	µA
		I_{VBP}		0.55	20.0	µA
Active, High Battery	BATSW On, VBPSW Off	I_{VCC}		4.5	5.0	mA
		I_{VBH}		1.5	1.8	mA
		I_{VBL}		0.27	2.0	µA
		I_{VBP}		0.6	20.0	µA
Active, Low Battery	BATSW Off, VBPSW Off	I_{VCC}		4.1	4.5	mA
		I_{VBH}		1.0	25.0	µA
		I_{VBL}		1.4	1.7	mA
		I_{VBP}		0.6	20.0	µA
Active, Boosted Battery (Ringing)	BATSW On, VBPSW On	I_{VCC}		1.30	1.65	mA
		I_{VBH}		1.5	1.9	mA
		I_{VBL}		0.35	2.0	µA
		I_{VBP}		2.3	2.5	mA
Tip Open	BATSW On, VBPSW Off	I_{VCC}		2.5	3.0	mA
		I_{VBH}		0.5	0.55	mA
		I_{VBL}		0.35	2.0	µA
		I_{VBP}		0.6	20.0	µA

DC Specifications

Unless otherwise specified, test conditions are: VCC = +3.3 V, VBH = –60 V, VBL = –36 V, VBP = +60 V, Loop resistance (AD to BD) = On-Hook. For this document, currents flowing into a SLIC pin are defined as positive and currents flowing out of a SLIC pin are defined as negative. The specifications apply for Active and Standby operating modes with switches BATSW and VBPSW switched either ON or OFF. However, although the device meets the specifications in both modes, there may be a slight difference in the actual values between Active and Standby so that calibrating in one mode and testing in the other could result in measurement errors.

Table 2. DC Specifications

#	Item	Condition	Min	Typ	Max	Unit	Note
1	Gain DCA to AD	VAD / (VDCA – VREF)	125.7	127	128.3	V/V	
	Gain DCB to BD	VBD / (VDCB – VREF)	125.7	127	128.3	V/V	
2	(a) Gain RCVN to AD	VAD / (VRCVN – VREF)	–6.06	–6	–5.94	V/V	
	(b) Gain RCVP to BD	VBD / (VRCVP – VREF)	–6.06	–6	–5.94	V/V	
	RCV Gain Ratio	Ratio of 2(a) to 2(b)	0.995	1	1.005		
3	AD Offset	DCA = RCVN = VREF	–0.5		0.5	V	1
	BD Offset	DCB = RCVP = VREF	–0.5		0.5	V	1
4	Amplifier AD & BD Positive Saturation	I = 0 mA; VBPSW ON I = –40 mA; VBPSW ON I = –100 mA; VBPSW ON	VBP – 4.0 VBP – 4.5 VBP – 5.0		VBP	V	2
		I = 0mA; VBPSW OFF I = –40 mA; VBPSW OFF I = –100 mA; VBPSW OFF	BGND BGND – 2.5 BGND – 3.0		+2.0 BGND BGND	V	
5	Amplifier AD & BD Negative Saturation	I = 0 mA; BATSW ON I = 40 mA; BATSW ON I = 100 mA; BATSW ON	VBH		VBH + 3.4 VBH + 3.8 VBH + 5.0	V	2
		I = 0 mA; BATSW OFF I = 40 mA; BATSW OFF I = 100 mA; BATSW OFF	VBL		VBL + 3.4 VBL + 3.8 VBL + 5.0	V	
6	AD & BD DC Feed Resistance (per pin)		15	18	21	Ω	
7	AD Pull-Up Current	Disconnect & Tip Open	0		50	µA	3
8	AD Voltage	Disconnect & Tip Open; 2 MΩ AD to VREF	–0.5		0	V	
9	BD Pull-Up Current	Disconnect & Ring Open	0		50	µA	3
10	BD Voltage	Disconnect & Ring Open; 2 MΩ BD to VREF	–0.5		0	V	
11	DCA & DCB Input Bias Current (per pin)	DCA = VREF ± 1.2 V DCB = VREF ± 1.2 V	–0.1	0	+0.1	µA	
12	RCVP & RCVN Input Bias Current (per pin)	RCVP = DCB RCVN = DCA	–1	0	+1	µA	
13	RCVP & RCVN Input Resistance (per pin)	RCVP = VREF ± 1.2 V RCVN = VREF ± 1.2 V	40		100	KΩ	
14	VREF Input Current	VREF = 1.5 V	–500		500	µA	4
15	Gain IA to IAD	IAD / IA; IAD from –100 mA to +100 mA	784	800	816	A/A	5
	Gain IB to IBD	IBD / IB; IBD from –100 mA to +100 mA	784	800	816	A/A	5
16	Gain IMT to (IAD – IBD)	(IAD – IBD) / IMT; (IAD – IBD) from –200 mA to +200 mA	784	800	816	A/A	5
17	IA, IB & IMT Voltage Compliance	VIA, VIB, VIAB	1.4	1.5	1.6	V	
18	IA output offset	IA = VREF; AD Open	–1	0	1	µA	
	IB output offset	IB = VREF; BD Open	–1	0	1	µA	

Table 2. DC Specifications (Continued)

#	Item	Condition	Min	Typ	Max	Unit	Note
19	IMT output offset	IMT = VREF; AD & BD Open	-2	0	2	µA	
20	IA, IMT Rejection Ratio	ΔIA and ΔIMT ΔVAD = ±50 V (–55 V to –5 V) with AD & BD Open		6.2		nA	
21	IB, IMT Rejection Ratio	ΔIB and ΔIMT ΔVBD = ±50 V (–55 V to –5 V) with AD & BD Open		10.6		nA	
22	Logic Inputs P0, P1, P2, SEL & LD	Input high voltage Input low voltage Input current	VCC/2 + 0.5 –50		 VCC/2 – 0.5 50	V V µA	
23	IMT fault output	Thermal Overload	0		0.2	V	6

Notes:

1. *Offset applies for any voltage at AD and BD, assuming amplifiers AD and BD are not saturated. In order to achieve these exact test conditions, VBPSW must be switched ON.*
2. *Applies only to the amplifiers and switches and does not include the internal 18-Ω sense resistors.*
3. *Positive voltage compliance for the leakage specification is VBP if VBPSW is ON and BGND if VBPSW is OFF. Negative voltage compliance is VBH if BATSW is ON and VBL if BATSW is OFF. When the switches are OFF the pin can be pulled by an external source to the maximum supply voltages, VBP (or VCC) and VBH, but the leakage current may increase up to the respective supply currents as defined by the operational mode of the SLIC.*
4. *Varies depending on the voltages applied to DCA and DCB and thus may also have an AC component.*
5. *If the SLIC is in the Standby mode, it automatically switches to the Active Mode when (IAD or IBD) exceeds ±15 mA. In order to return to the Standby mode, the SLIC must be programmed via the P-bus. Positive voltage compliance on AD and BD is VBP if VBPSW is ON and BGND if VBPSW is OFF. Negative voltage compliance is VBH if BATSW is ON and VBL if BATSW is OFF. However, the gain accuracy may be degraded when AD or BD are within 2 V of either VBH or VBL and within 3 V of VBP.*
6. *Not tested in production.*

Transmission Specifications

Unless otherwise specified, test conditions are: VCC = +3.3 V, VBH = –60 V, VBL = –36 V, VBP = +60 V. There is a 30 Ω protection resistor from AD to the loop A-Lead, a 30 Ω protection resistor from BD to the loop B-Lead, and a 600 Ω AC termination on the loop between the A-Lead and B-Lead (typical protection resistors are expected to be 50 Ω but the worst case value is used here). There is a feedback path from output IMT to input pins RCVP and RCVN which creates a 600 Ω AC terminating impedance. The feedback generates no noise, has no gain at DC and has a perfect trans-impedance gain of –33600 Ω from 50 Hz to 20 kHz. The feedback input (connected to IMT) is 0 Ω referenced to 1.5 V and the output is a differential voltage source applied from RCVP to RCVN with a common mode voltage equal to VREF. The specifications apply for Active and Standby operating modes with switches BATSW and VBPSW switched either ON or OFF. However, although the device meets the specifications in both modes, there may be a slight difference in the actual values between Active and Standby so that calibrating in one mode and testing in the other could result in measurement errors. The specifications apply for any DC voltages on AD and BD that are within the operating voltage range as specified in Item #4 and Item #5 of DC Specifications and for any DC current in leads AD and BD from –100 mA to +100 mA.

Table 3. Transmission Specifications

Item #	Item	Condition	Min	Typ	Max	Unit	Note
1	AD or BD drive current = DC + longitudinal + signal + ringing current (per pin)	Active Mode	120	150		mApk	1
		Standby Mode	35	50			
2	Longitudinal impedance AD or BD to Ground		15	18	21	Ω	1
3	Differential impedance AD to BD		30	36	42	Ω	1
4	2-4 Wire gain	$(I_{AD} – I_{BD})$ / IMT; f = 1 kHz	784	800	816	A/A	
5	4-2 Wire gain	$(V_{AD} – V_{BD}) / (V_{RCVP} – V_{RCVN})$ f = 1 kHz; Loop Open AC	5.94	6	6.06	V/V	
6	2-4 Wire gain variation versus frequency	f = 300 to 3400 Hz Relative to 1 kHz	–0.1	0	+0.1	dB	1
7	2-4 Wire gain tracking	+3 dBm to –55 dBm Reference: –10 dBm, 1 kHz	–0.1	0	+0.1		
8	4-2 Wire gain variation versus frequency	f = 300 to 3400 Hz Relative to 1 kHz	–0.1	0	+0.1		
9	4-2 Wire gain tracking	+3 dBm to –55 dBm Reference: –10 dBm, 1 kHz	–0.1	0	+0.1		
10	Total harmonic distortion	0 dBm, 1 kHz, 600 Ω 2-Wire & 4-Wire			0.3	%	1
11	Metering Total Harmonic Distortion	Active Mode; I_{LOOP} = 20 mA; 2.8 Vrms, f = 12 kHz or 16 kHz Metering Load = 200 Ω,			1.0	%	1
12	Ringing Total Harmonic Distortion	Active Mode 75 Vrms, f = 20 Hz or 50 Hz Ringing Load = 15 KΩ or 5 REN (1386 Ω + 40 µF)		0.3	2.0	%	1
13	Idle channel noise	Active Mode: 2-Wire 4-Wire		9 9	13 13	dBrnC dBrnC0	
		Active Mode: 2-Wire 4-Wire		–81 –81	–77 –77	dBmp dBmp0	1
		Standby Mode: 2-Wire 4-Wire 2-Wire 4-Wire		15 15 –75 –75	19 19 –71 –71	dBrnC dBrnC0 dBmp dBmp0	1
		Active Mode with Metering 2.5 Vrms, f = 12 kHz or 16 kHz 2-Wire			–65	dBmp	1

Table 3. Transmission Specifications (Continued)

Item #	Item	Condition	Min	Typ	Max	Unit	Note
14	Longitudinal to Metallic Balance (IEEE method)	Active Mode f = 200 to 1000 Hz f = 3000 Hz	 58 56	66		 dB dB	3
		Standby Mode f = 200 to 1000 Hz f = 3000 Hz	 52 50	58		 dB dB	4
15	Metallic to Longitudinal Balance (HARM)	Metallic to longitudinal (HARM) f = 200 to 3000 Hz	46			dB	5
16	VBH, VBL, VBP PSRR	f = 50 to 3400 Hz f = 3.4 to 50 kHz	40 25			dB	1
17	VCC PSRR	f = 50 to 3400 Hz f = 3.4 to 50 kHz	35 25			dB	1
18	BGND Rejection	f = 50 to 3400 Hz f = 3.4 to 50 kHz	50 30			dB	1
19	EMC, per ETSI EN 300 386 V1.3.1 (2001-09) and EN 61000-4-6	3 Vrms, f = 150 kHz – 80 MHz, 80% modulated with 1 kHz; 150 Ω common mode source impedance (300 Ω per leg)			–40	dBm	1
20	Crosstalk between channels	f = 200 to 3400 Hz, 0 dBm			–80	dB	1, 6
		f = 12 kHz or 16 kHz, 2.8 Vrms			–60		1

Test Switch Specifications

Item	Condition	Min	Typ	Max	Unit	Note
Test Switch	ON Resistance; $(V_{ON(25mA)} – V_{ON(20mA)}) / 5$ mA			30	Ω	
	ON Voltage; I_{TLD} = ±20 mA	–3		3	V	
	OFF-Mode Leakage, VBP to VBH with VBP and VBH switches on			5	µA	

Thermal Shutdown Fault Indications

Item	Condition	Min	Typ	Max	Unit	Description	Note
Thermal Overload	Temperature of power amplifiers AD and/or BD		190		°C	The channel enters a ‘disconnect like’ mode that denies current to the loop (amplifiers AD and BD are shut down). Outputs IA and IB are both forced to source >150 µA. TSTSW operates normally	1, 2
Thermal Hysteresis	Temperature of power amplifiers AD and BD	20	30	40	°C	IA and IB return to normal operation, and the SLIC channel returns to the mode that it was in prior to thermal overload when the temperature of the amplifier (or amplifiers) in thermal overload decreases by this hysteresis value.	1

Notes:

1. *Not tested in production.*
2. *Continuous operation above 150°C junction temperature may degrade device reliability.*
3. *This parameter is tested at 1 kHz normal polarity with 40 mA loop current in production. Performance at other frequencies is guaranteed by characterization.*
4. *This parameter is tested at 1 kHz normal polarity with open loop in production. Performance at other frequencies is guaranteed by characterization.*
5. *This parameter is tested with DC in production. Performance at frequencies is guaranteed by characterization.*
6. *Both channels in any combination of active on-hook or off-hook or standby state. No impulse noise is recorded on adjacent channel using a 47 dBrnC threshold. Also in presence of dial pulse, no impulse noise is recorded on adjacent channel using a 47 dBrnC threshold.*

Data Friendly Transient Specifications

The Le79272 SLIC is one device of a chipset that will be used in integrated voice and data (IVD) applications. The basic requirement for devices used in IVD applications is not to create CRC errors during normal operating conditions. In IVD applications the Le79272 device will be used with a splitter and a data transformer circuit. The basic requirement of no CRC errors ultimately translates to a requirement on the maximum allowable transient at the output of the data transformer.

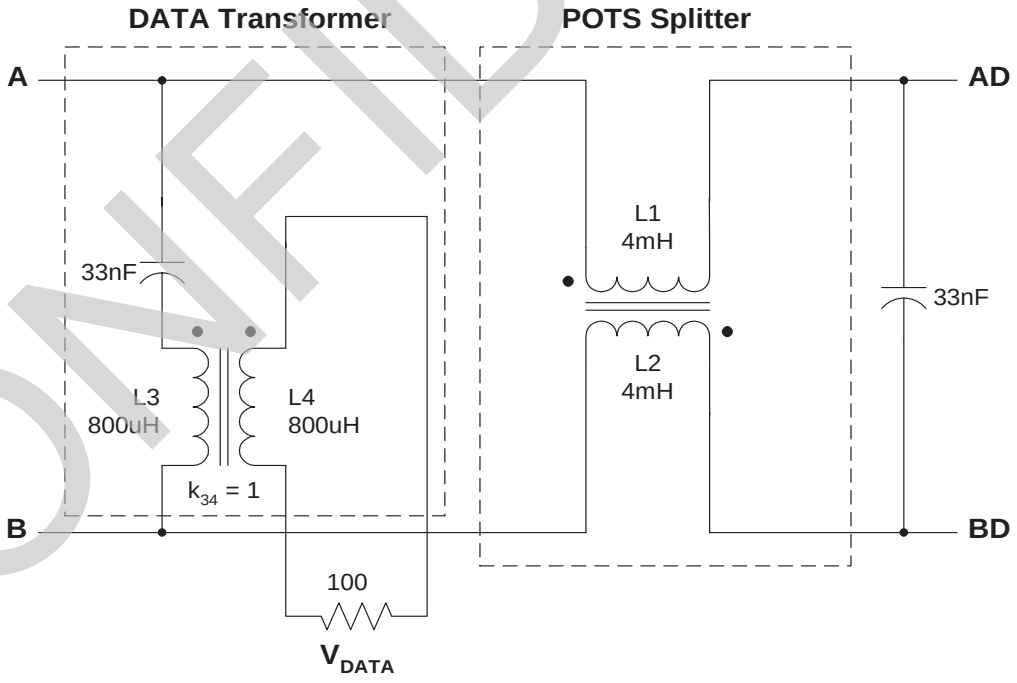
IVD Specifications

Unless otherwise specified, test conditions are: VCC = +3.3 V, VBH = –60 V, VBL = –36 V, VBP = +60 V. A simplified diagram of an IVD POTS Splitter and Data Transformer circuit is shown in Figure 2. The A/B (TIP/RING) output of the splitter is terminated with 600 Ω AC in the voiceband and 100 Ω in the xDSL band. The specifications are for the peak transient voltage, V_{DATA}, generated across a 100 Ω data termination resistor.

Table 4. IVD Specifications

#	Item	Condition	Min	Typ	Max	Unit
1	BATSW Transient	VBH = -140V; VBP = 0V Switch BATSW from OFF to ON		±5		mVpk
		VBH = -140V; VBP = 0V Switch BATSW from ON to OFF		±5		mVpk
2	VBPSW Transient	VBH = -40V; VBP = +100V Switch VBPSW from OFF to ON		±5		mVpk
		VBH = -40V; VBP = +100V Switch VBPSW from ON to OFF		±5		mVpk
3	Standby Mode Transient	Switch Mode from Active to Standby		±5		mVpk
		Switch Mode from Standby to Active		±5		mVpk

Figure 2. IVD POTS Splitter and Data Transformer



OPERATING MODES

The Le79272 device receives multiplexed control data on the P0, P1 and P2 pins (the P-bus). The LD pins control the loading of the P-bus data into the proper bits of the channel's control register as directed by the SEL pin. When SEL is "0", data on P0, P1 and P2 is loaded into one 3-bit register that controls the operating modes of the SLIC. When SEL is "1", data on P0, P1 and P2 is loaded into another 3-bit register that controls the operating condition of the switches in the SLIC. When LD is a "1", data on the P-bus is prohibited from entering the control register. When LD is a "0", data on the P-bus is directed by SEL to control the corresponding bits of the control register (transparent latch). The "0" to "1" transition of LD latches the data into the control register.

Table 5. Operating Modes

SEL	P2	P1	P0	Operating Mode
0	0	0	0	Disconnect
0	0	0	1	TIP Open
0	0	1	0	Ring Open
0	0	1	1	Standby
0	1	0	0	Disconnect
0	1	0	1	Tip Open Test
0	1	1	0	Ring Open Test
0	1	1	1	Active

Table 6. Operating Conditions

				Operating Condition		
SEL	**P2**	**P1**	**P0**	**BATSW**	**VBPSW**	**TSTSW**
1	0	0	0	OFF	OFF	OFF
1	0	0	1	ON	OFF	OFF
1	0	1	0	OFF	ON	OFF
1	0	1	1	ON	ON	OFF
1	1	0	0	OFF	OFF	ON
1	1	0	1	ON	OFF	ON
1	1	1	0	OFF	ON	ON
1	1	1	1	ON	ON	ON

Note:

BATSW Off applies VBL.

BATSW On applies VBH.

VBPSW On applies VBP.

TSTSW On applies test load.

Operating Mode Descriptions

The operating condition of battery switches BATSW and VBPSW determine the battery voltage for all operating modes. The supply voltages are thus completely independent of the mode selected.

Table 7. Operating Mode Descriptions

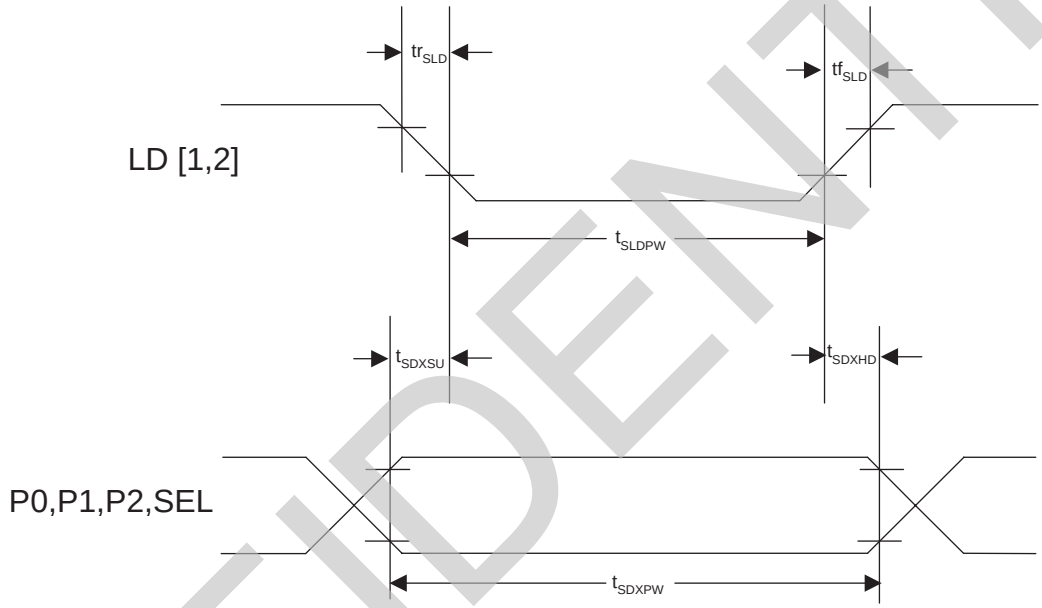
Operating Mode	Description
Disconnect	As much SLIC circuitry as possible is turned OFF (powered down). The AD and BD amplifiers are high impedance (> 2 MΩ) to any external voltage between VBP (VBPSW ON) or BGND (VBPSW OFF) and VBH (BATSW ON) or VBL (BATSW OFF). However, if the battery switches are OFF the amplifier outputs can be pulled to VBP and VBH, but the leakage current may increase up to the value of the respective supply current as specified for the disconnect mode. Pins AD and BD are forced to AGND by a high impedance current source. Output currents IA, IB and IMT are invalid.
Active	Normal operation. All SLIC circuits for the given channel are active at full bias current for maximum performance.
Standby	Same as the Active Mode except bias currents are reduced as much as possible to conserve power. Performance is reduced for some SLIC parameters. The SLIC channel automatically returns to the Active Mode if the IAD current and/or IBD current exceeds ±15 mA. This is accomplished by resetting the SLIC control register; therefore, in order to return to the Standby Mode, the SLIC control register must be set again to the Standby Mode via the P-bus.
Tip Open	Uses Standby Mode biasing. The SLIC channel automatically returns to the Tip Open Test Mode if the current in BD exceeds ±15 mA. The AD drive amplifier is turned OFF (powered down). The AD amplifier is high impedance (> 2 MΩ) to any external voltage between VBP (VBPSW ON) or BGND (VBPSW OFF) and VBH (BATSW ON) or VBL (BATSW OFF). However, if the battery switches are OFF the amplifier output can be pulled to VBP and VBH, but the leakage current may increase up to the value of the respective supply current as specified for the Tip Open mode. Pin AD is forced to AGND by a high impedance current source. Output currents IA and IMT are invalid; output current IB is valid.
Ring Open	Uses Standby Mode biasing. The SLIC channel automatically returns to the Ring Open Test Mode if the current in AD exceeds ±15 mA. The BD drive amplifier is turned OFF (powered down). The BD amplifier is high impedance (> 2 MΩ) to any external voltage between VBP (VBPSW ON) or BGND (VBPSW OFF) and VBH (BATSW ON) or VBL (BATSW OFF). However, if the battery switches are OFF the amplifier output can be pulled to VBP and VBH, but the leakage current may increase up to the value of the respective supply current as specified for the Ring Open mode. Pin BD is forced to AGND by a high impedance current source. Output currents IB and IMT are invalid; output current IA is valid.
Tip Open Test	Same as the Tip Open Mode except Active Mode biasing is used.
Ring Open Test	Same as the Ring Open Mode except Active Mode biasing is used.

TIMING SPECIFICATIONS

Table 8. Timing Specifications

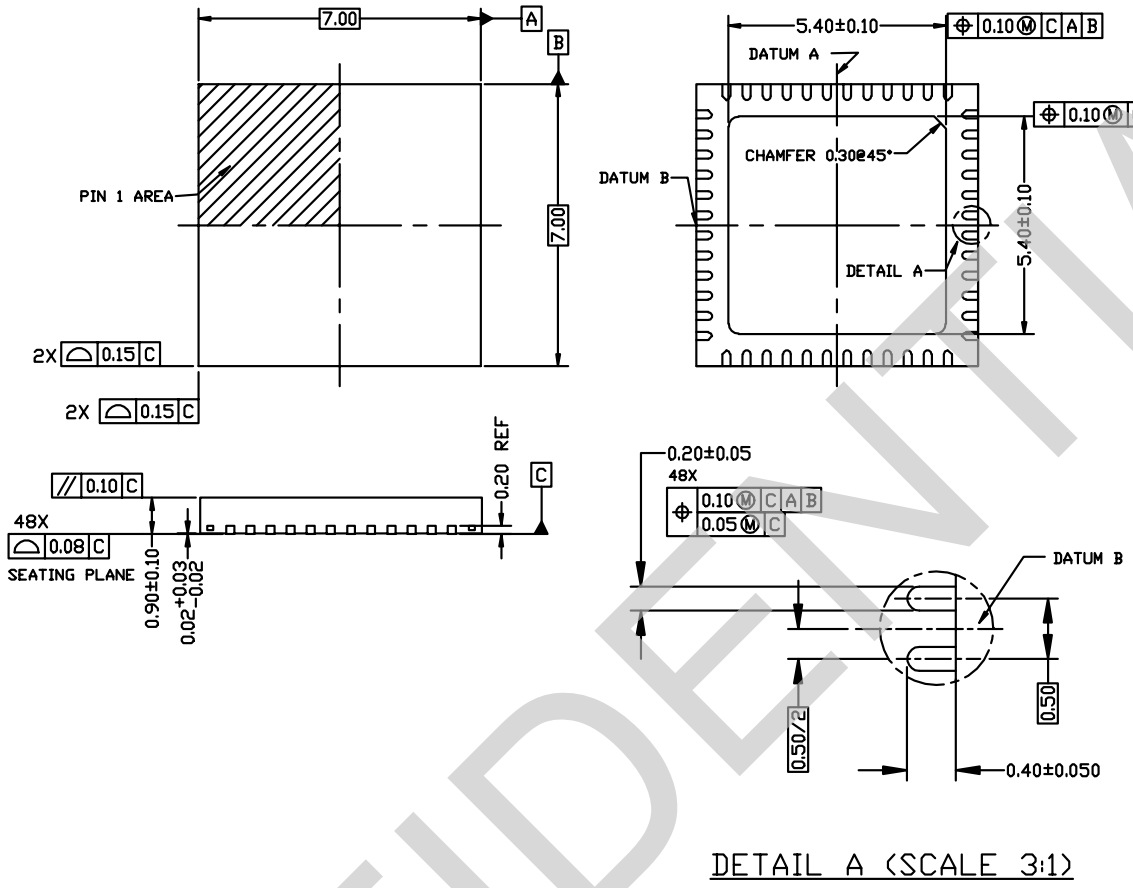
Symbol	Signal	Parameter	Min	Typ	Max	Unit
trSLD	LD [1,2]	Rise time			2	µs
tfSLD	LD [1,2]	Fall time			2	
tSLDPW	LD [1,2]	Pulse width	3			
tSDXSU	P0, P1, P2, SEL	Data setup time	2			
tSDXHD	P0, P1, P2, SEL	Data hold time	2			
tSDXDPW	P0, P1, P2, SEL	Pulse width	7			

Waveforms



PHYSICAL DIMENSIONS

48-Pin QFN



Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

All dimensions are in millimeters.

REVISION HISTORY

Version 1 to 2

- Changed branding from Zarlink Semiconductor to Microsemi Corporation.
- Page 11; Electrical Operating Ranges description, changed reliability reference document from "section 4.6.2 of Bellcore TR-TSY-000357" to "Telcordia GR-357-CORE".
- Page 11, 12; Specifications, Table 1, Table 2, added Ringing descriptor after Boosted Battery.

Version 2 to 3

- Page 11, Specifications, updated Power Dissipation section.
- Page 12, Supply Currents, Table 2, updated Supply Current Specifications (Per Channel).
- Minor text edits.

Version 3 to 4

- Page 8, Connection Diagram, replaced incorrect connection diagram with correct connection diagram.

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