Le87285

Preliminary Datasheet

G.Fast Single Channel Line Driver

July 2019

Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Moved from Advance to Preliminary.

2 Product Overview

The Le87285 device is a single-channel line driver designed for home gateway applications. It supports the transmission of xDSL and G.Fast signals with low-power dissipation. It also contains a pair of wideband amplifiers designed with Microsemi's HV15 Bipolar SOI process for low power consumption.

The line driver gain is fixed internally. The amplifiers are powered from a single supply. The device can be programmed to one-of-three preset Bias levels or to impedance controlled Disable or Standby states. The control pins respond to input levels that can be generated with a standard tri-state GPIO.

The Le87285 device is available in a 16-pin (4mm x 4mm) QFN package with exposed pad for enhanced thermal conductivity.

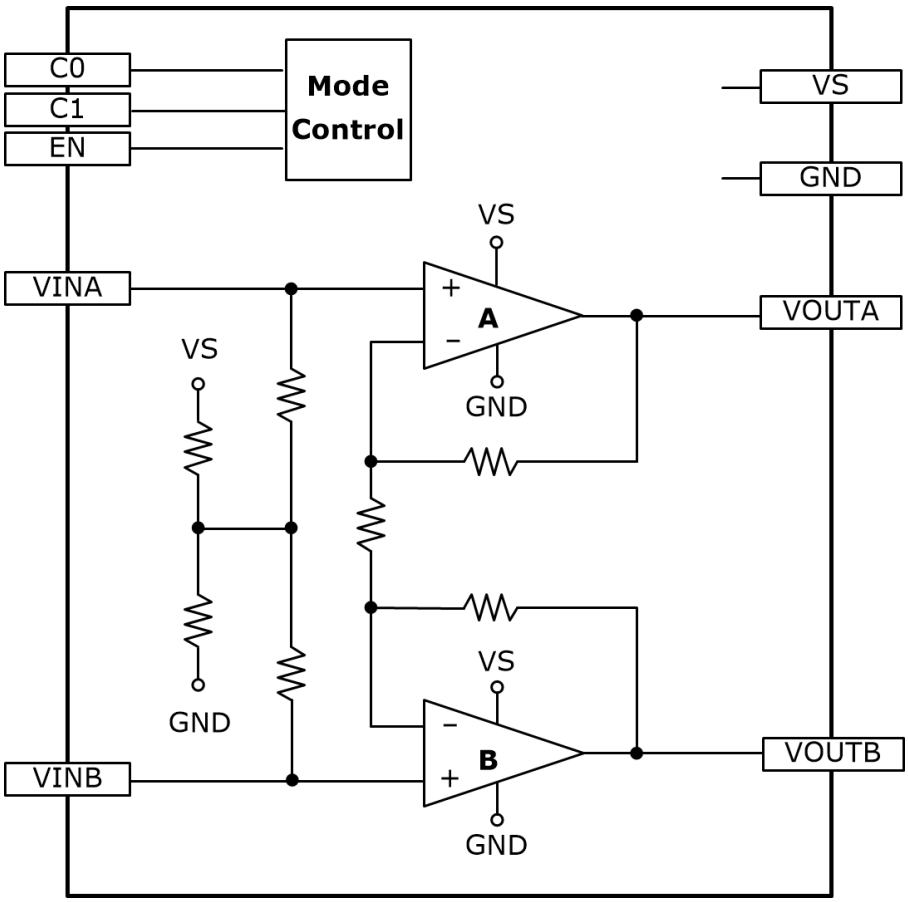
2.1 Features

- Supports high-frequency G.Fast transmission
- Supports VDSL2 and ADSL2+ operation
- Low-power dissipation
  - Class AB operation
- Five programmable operational states
- No external gain resistors required
- Small footprint package
  - 16-pin (4mm x 4mm) QFN
- RoHS compliant

2.2 Applications

- G.Fast Line Driver
- VDSL2 Line Driver
- ADSL2+ Line Driver

Figure 1 • Block Diagram



3 Functional Descriptions

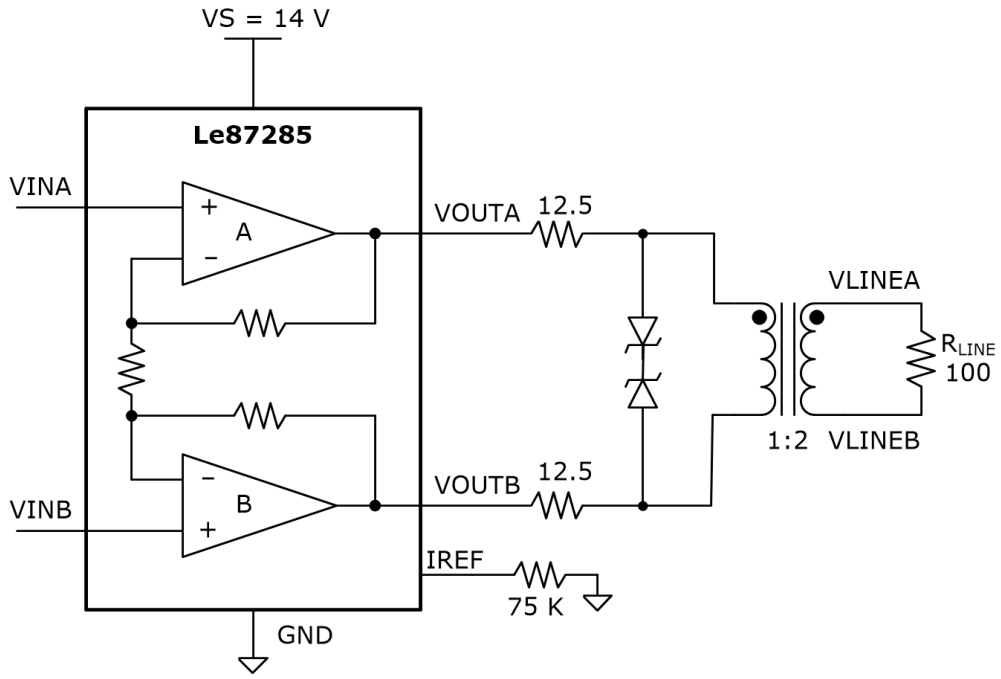
The following sections describe the functionalities of the Le87285 device.

3.1 XDSL/G.Fast Applications

Le87285 integrates a set of high-power line driver amplifiers that can be connected for half-duplex differential line transmissions for ADSL, VDSL, or G.Fast. In this application, the amplifiers are designed to be used with signals up to the signal bandwidth with low signal distortion.

The following figure shows an application circuit for 13 dBm line power with amplifiers A and B in transmission for ADSL or VDSL, or 8 dBM for G.Fast.

Figure 2 • Typical Application Circuit for xDSL/G.Fast

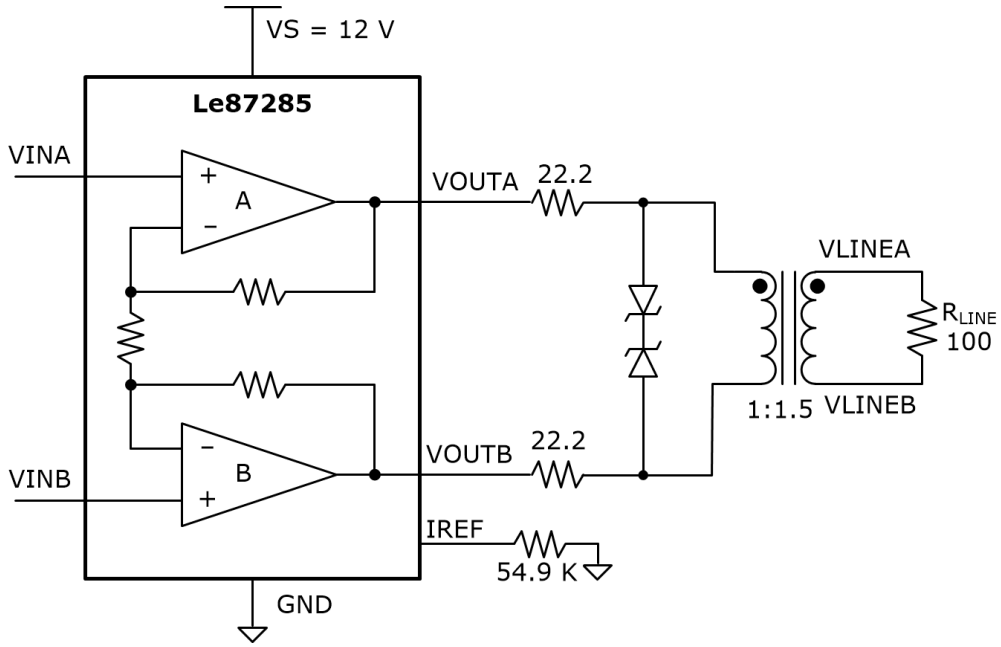


3.2 G.Fast Applications

Le87285 line driver amplifiers that can be connected for half-duplex differential line transmissions for G. Fast. In this application, the amplifiers are designed to be used with signals up to 106 MHz with low signal distortion.

The following figure shows an application circuit for 8 dBm line power with amplifiers A and B in transmission for G.Fast.

Figure 3 • Typical Application Circuit for G.Fast



3.3 Design Considerations

3.3.1 Input Considerations

The driving source impedance should be less than 100 nH to avoid any ringing or oscillation.

3.3.2 Output Driving Considerations

The internal metallization is designed to carry up to about 100 mA of steady DC current and there is no current limit mechanism. The device does feature integrated thermal shutdown protection however with hysteresis. Driving lines with no series resistor is not recommended. The 75 kΩ resistor on the IREF pin could be reduced to increase the line driver power and signal bandwidth for better MTPR performance. This is a design trade off and will result in greater power dissipation.

3.3.3 Power Supplies and Component Placement

The power supplies should be well bypassed close to the Le87285 device. A 2.2 µF tantalum capacitor and a 0.1 µF ceramic capacitor for the VS supply is recommended.

3.3.4 Line Driver Protection

High voltage transients such as lightning can appear on the telephone lines. Transient protection devices should be used to absorb the transient energy and clamp the transient voltages. The series output termination resistors limit the current going into the line driver and internal clamps. The protection scheme depends on the type of data transformer used and the line protection components used in the front of the data transformer.

4 Electrical Specifications

The following sections describe the electrical specifications of the Le87285 device.

4.1 Absolute Maximum Ratings

If you stress values above than what is listed in the following table, it can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Table 1 • Absolute Maximum Ratings

Parameter	Ranges
Storage Temperature	–65 ≤ T_A ≤ +150 °C
Operating Junction Temperature[1]	–40 ≤ Tj ≤ +150 °C
VS with respect to GND	–0.3 V to +16 V
Control inputs with respect to GND	–0.3 V to 4 V
Continuous Driver Output Current	100 mA
ESD Immunity (Human Body Model)	JESD22 Class 2 compliant
ESD Immunity (Charge Device Model)	JESD22 Class IV compliant

1. Continuous operation above 145 °C junction temperature may degrade device reliability.

4.1.1 Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to larger internal copper planes.

The following table lists the simulation results of a device mounted on a 4-layer JEDEC PCB with 12 thermal vias in still air. These numbers are only for reference.

Table 2 • Thermal Resistance

Parameter	Ranges
Maximum device power dissipation, continuous - T_A = 85 °C, PD	1.0 W
Junction to ambient thermal resistance, θ_{JA}	52.0 °C/W
Junction to board thermal resistance, θ_{JB}	26.0 °C/W
Junction to case bottom (exposed pad) thermal resistance, θ_{JC} (BOTTOM)	14.6 °C/W
Junction-to-top characterization parameter, Ψ_{JT}	3.1 °C/W

4.1.2 Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes.

See IPC/JEDEC J-Std-020 Table 4 for recommended peak soldering temperature and Table 5-2 for the recommended solder reflow temperature profile.

4.2 Operating Ranges

Microsemi guarantees the performance of this device over the industrial (–40 °C to 85 °C) temperature range by conducting electrical characterization over each range and by conducting a production test with single insertion coupled with periodic sampling. These characterization and test procedures comply with the Telcordia GR-357- CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.

Table 3 • Operating Ranges

Parameter	Min.	Max.	Units
Ambient temperature (T_A)	−40	+85	°C
Power Supply (VS with respect to GND)		+12 ±10% or 14 ± 5%	V

4.3 Device Specifications

Typical Conditions: As shown in the basic test circuit (Figure 4 (see page 9)) with VS = +12 V unless otherwise specified,
R_{REF} = 75 kΩ, 1%, and T_A = 25 °C.

Min/Max Parameters: T_A = –40 to +85 °C

4.3.1 Electrical Specifications

Table 4 • Electrical Specifications

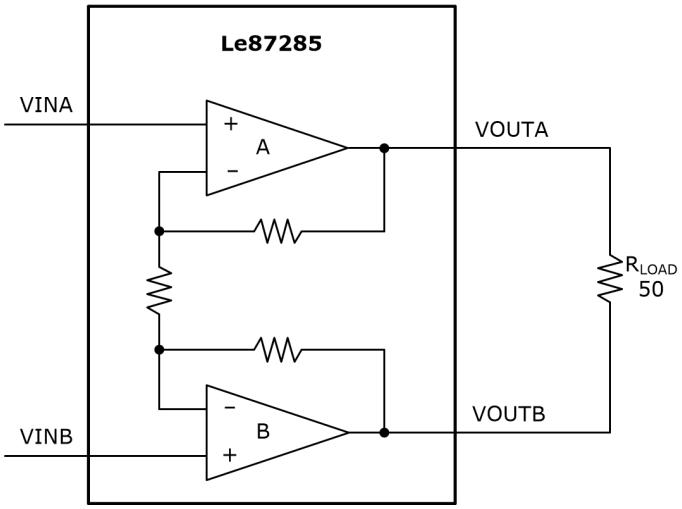
Parameter	Parameter Description	Condition	Min.	Typ.	Max.	Unit	Notes
Supply Current Specifications							
P_{IS}	Supply Current	Enable Full Bias	25	31	37	mA	
		Enable Medium Bias	21	27	31	mA	
		Enable Low Bias	17	21	25.5	mA	
		Receive	1	3	5	mA	
		Disable	0.2	1.1	2	mA	
Control Input (C0, C1, and EN) Electrical Specifications							
V_{IH}	Input High Voltage		2.0	3.3	3.6	V	
V_{IL}	Input Low Voltage		–0.3	0	0.8	V	
Z_{IL}	Input Impedance			20		kΩ	
T_{TE}	Transmit Enable Time	Enable Full Bias			400	nS	1
		Enable Medium/Low Bias			2	µS	1
T_{TR}	Transmit to Receive Time	All Modes			400	nS	1

Parameter	Parameter Description	Condition	Min.	Typ.	Max.	Unit	Notes
T_D	TX/RX to Disable	All Modes			2	µS	1
Amplifier Electrical Specifications							
V_I	Max Input Voltage	Differential	1.4			V_{pkd}	
V_o	Output Voltage	Differential, VS = 12 V		8.5		V_{pkd}	
		Differential, VS = 14 V		11.2		V_{pkd}	
	Differential Gain	V_{OUT}/V_{IN}	8.1	8.5	8.9	V/V	
I_O	Max Output Current	Enable Full Bias	140			mA_{pk}	1
		Enable Medium/Low Bias	250			mA_{pk}	1
		Receive, Pline = 8 dBm		90		mA_{pk}	1
Z_I	Input Impedance	Differential	10			kΩ	
Z_O	Output Impedance	Enable		0.1		Ω	1
		Receive			5	Ω	
		Disable		900		Ω	
Amplifier Dynamic Specifications							
BW	Bandwidth	Enable Full Bias		240		MHz	1
		Enable Medium Bias		240		MHz	1
		Enable Low Bias		200		MHz	1
	Analog Signal Bandwidth	Enable Full Bias			106	MHz	1
		Enable Medium Bias			35	MHz	1
		Enable Low Bias			0.276	MHz	1
	Gain Flatness	Variation within Analog Signal BW			2	dB	1
	Noise	Enable Full Bias, f > 100 KHz		6	8	nV/rtHz	1
		Enable Medium Bias, f > 100 KHz		6	8	nV/rtHz	1
		Enable Low Bias, f > 100 KHz		6	8	nV/rtHz	1
		Receive, f > 100 KHz		1	4	nV/rtHz	1
MTPR	Multi-Tone Power Ratio	Enable Full Bias, Pline = 8 dBm, PAR = 6.8		–48	–40	dBc	1, 2
		Enable Medium Bias, Pline = 13 dBm, PAR = 6.8		–60	–58	dBc	1, 2
		Enable Low Bias, Pline = 13 dBm, PAR = 6.3		–100	–52	dBc	1, 2
		Receive, Pline = 8 dBm		–65	–63	dBc	1, 2
PSRR	Power Supply Rejection Ratio			45		dB	1, 3
TSD	Thermal Shutdown Temperature			170		°C	1

1. Not tested in production. Guaranteed by characterization and design.

2. MTPR measured at 25 °C.
3. G.Fast mode.

Figure 4 • Basic Test Circuit



4.3.2 Optional G.Fast Only Operation

Typical Conditions: As shown in the basic test circuit (Figure 4 (see page 9)) with VS = +12 V, R_{REF} = 54.9 kΩ, 1%, and T_A = 25 °C. **Min/Max Parameters:** T_A = –40 to +85 °C.

Table 5 • Electrical Specifications

Symbol	Parameter Description	Condition	Min	Typ	Max	Unit	Notes
Supply Current Specifications							
P_{IS}	Supply Current	Enable Full Bias	36	43	50	mA	
		Receive	1.2	3.5	5.0	mA	
		Disable	0.2	1.3	2.2	mA	
Control Input (C0, C1, and EN) Electrical Specifications							
V_{IH}	Input High Voltage		2.0	3.3	3.6	V	
V_{IL}	Input Low Voltage		–0.3	0	0.8	V	
Z_{IL}	Input Impedance			20		kΩ	
T_{TE}	Transmit Enable Time	Enable Full Bias			400	nS	1
T_{TR}	Transmit to Receive Time	All Modes			400	nS	1
T_D	TX/RX to Disable	All Modes			2	µS	1
Amplifier Electrical Specifications							
V_I	Max Input Voltage	Differential	1.4			V_{pkd}	
V_o	Output Voltage	Differential		6.5		V_{pkd}	

Symbol	Parameter Description	Condition	Min	Typ	Max	Unit	Notes
	Differential Gain	V_{OUT}/V_{IN}	8.1	8.5	8.9	V/V	
I_O	Max Output Current	Enable Full Bias	110			mA_{pk}	1
		Receive, Pline = 8 dBm		91		mA_{pk}	1
Z_I	Input Impedance	Differential	10			kΩ	
Z_O	Output Impedance	Enable		0.1		Ω	1
		Receive			5	Ω	
		Disable		900		Ω	
Amplifier Dynamic Specifications							
BW	Bandwidth	Enable Full Bias		270		MHz	1
	Analog Signal Bandwidth	Enable Full Bias			106	MHz	1
	Gain Flatness	Variation within Analog Signal BW			2	dB	1
	Noise	Enable Full Bias, f > 100 KHz		6.5	8	nV/rtHz	1
		Receive, f > 100 KHz		1	4	nV/rtHz	1
MTPR	Multi-Tone Power Ratio	Enable Full Bias, Pline = 8 dBm, PAR = 6.8		–48	–40	dBc	1, 2
		Receive, Pline = 8 dBm		–65	–63	dBc	1, 2
PSRR	Power Supply Rejection Ratio			45		dB	1
TSD	Thermal Shutdown Temperature			170		°C	1

1. Not tested in production. Guaranteed by characterization and design.
2. MTPR measured at 25 °C.

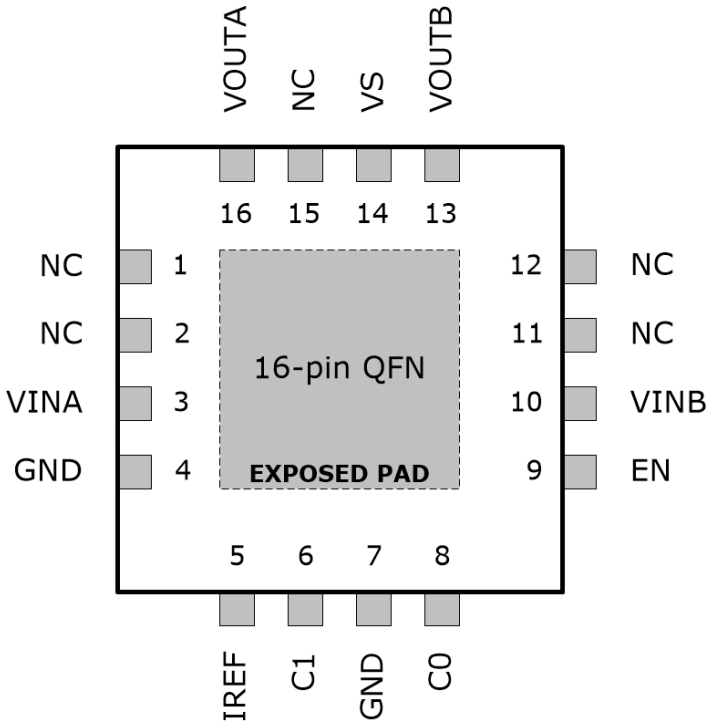
5 Pin Description

The Le87285 device has 16 pins, which are described in this section.

5.1 Pin Diagram

The following illustration is a representation of the Le87285 device, as seen from the top view.

Figure 5 • Le87285 Pin Diagram



Notes:

- Pin 1 is marked for orientation.
- The Le87285 device incorporates an exposed die pad on the underside of its package. The pad acts as a heat sink and must be connected to a copper plane through thermal vias, for proper heat dissipation. It is electrically isolated and maybe connected to GND.

5.2 Pin Description

The following table shows the functional pin descriptions for the Le87285 device.

Table 6 • Le87285 Pin Description

Pin Name	Pin #	Type	Description
1	NC		No internal connection
2	NC		No internal connection
3	VINA	Input	Non-inverting input of amplifier A
4	GND	Ground	Reference ground

Pin Name	Pin #	Type	Description
5	IREF	Input	Device internal reference current. Connect a resistor (R_{REF}) to GND
6	C1	Input	State Control Signal
7	GND	Ground	Reference ground
8	C0	Input	State Control Signal
9	EN	Input	Output Enable Signal
10	VINB	Input	Non-inverting input of amplifier B
11	NC		No internal connection
12	NC		No internal connection
13	VOUTB	Output	Amplifier B output
14	VS	Power	Power Supply
15	NC		No internal connection
16	VOUTA	Output	Amplifier A output
	Exposed pad		Electrically isolated thermal conduction pad, can be grounded

6 Control State

EN, C0, and C1 pins are used as combinatorial logic inputs to control the line driver operating states. The following table lists the programmable states.

EN, C0, and C1 pins have internal pull-down resistors. EN is meant to rapidly toggle between TX/RX states during G.Fast operation. It has a response time under 400 nS.

Table 7 • Control Matrix

EN	C1	C0	State	Application
0	1	1	Receive	Receive
1	0	0	Disable	Disable
1	0	1	Enable Low Bias	TX ADSL
1	1	0	Enable Medium Bias	TX VDSL
1	1	1	Enable Full Bias	TX G.Fast

6.1 Receive State

Used for receive time periods during G.Fast operation. Amplifier outputs have a low differential output impedance. This state uses less power than transmission states.

6.2 Disable State

Bias current is removed from amplifiers and amplifier outputs are high-impedance. Gain setting resistors around the amplifiers remain in place and present a differential impedance at the output pins. This impedance is typically 900 ohms.

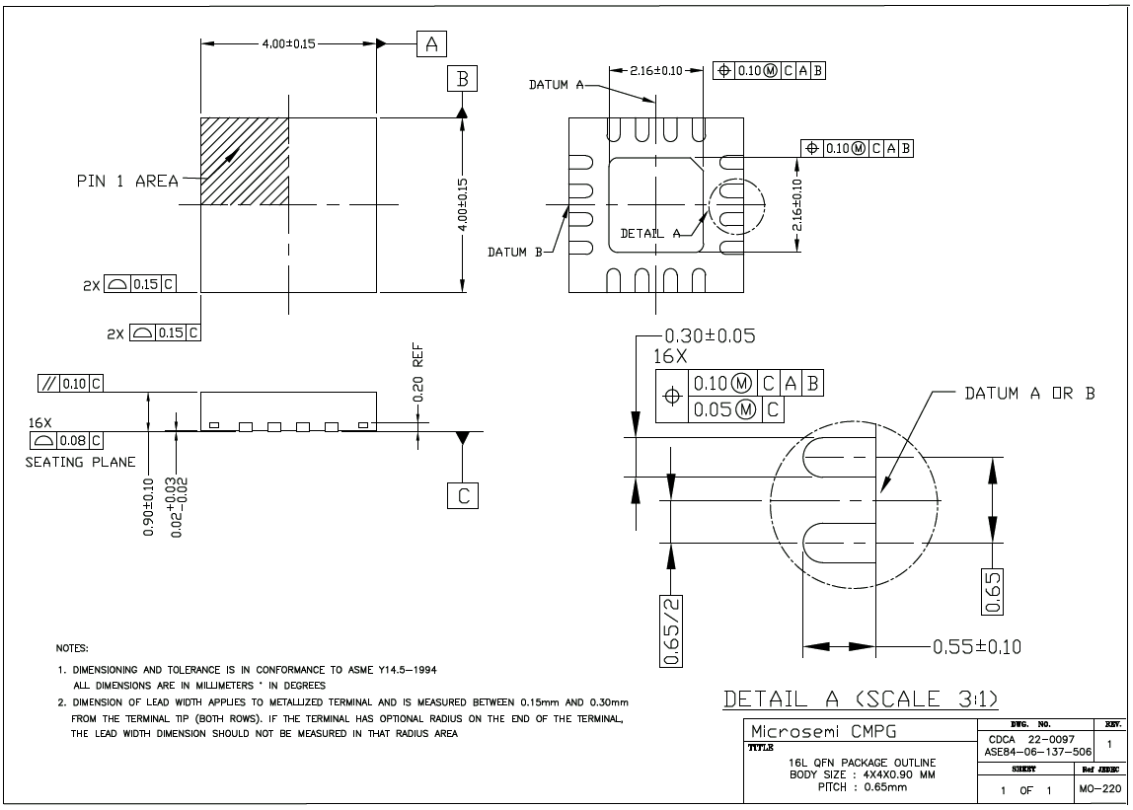
6.3 Bias States

Line Driver is active for transmission. Bias current is applied to the amplifiers and the line driver provides gain from VIN to VOUT. These states are different in the amount of bias current to the amplifiers and in the amplifier bandwidth. ADSL uses the lowest bias setting, G.Fast uses the highest bias/bandwidth. The external resistor at IREF pin sets the internal reference current. Adjustments to this resistance value will also affect the bias currents in all TX states.

7 Physical Dimensions

The following figure shows the physical dimensions of the Le87285 device.

Figure 6 • 16-Pin QFN



Note:

Packages may have mold tool markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used during manufacturing.

8 Ordering Information

The following section describes the ordering information of the Le87285 device.

Table 8 • Ordering Information

Part Number	Package	Packaging Type
Le87285NQC	16-pin QFN Green Package	Tray
Le87285NQCT	16-pin QFN Green Package	Tape and Reel

Note:

The green package meets RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

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