# VE8820

## Dual Channel Tracking Battery Wideband VoicePort™ Chipset
## VE880 Series

Document ID#**081574** **October 2014**

## APPLICATIONS

- **Voice enabled Cable and DSL Modems**
- **Residential VoIP Gateways and Routers**
- **Media Terminal Adapters (MTA) Standalone & Embedded**
- **Fiber to the User/Premise/Home (FTTH/P/H), Fiber in the Loop (FITL) Optical Network Terminals (ONT)**
- **Wireless Local Loop (WLL), PBX, ISDN NT1/TA**

## FEATURES

- **Complete BORSCHT Function for Two Channels in a Single VoicePort™ chipset**
  - — **B**attery Feed, **O**ver-voltage support, integrated **R**inging, line **S**upervision, **C**odec, **H**ybrid (2 W/4 W), **T**est
- **Integrated Power Management**
  - — Integrated high voltage switching regulator controllers
    - – Wide input voltage range (VSW =+3.3 V to +35 V)
    - – Switching power supply tracks line voltage minimizing active & ringing state power dissipation
  - — Low power Idle and On-hook transmission states
- **Worldwide Programmability**
  - — Two-wire AC impedance, Balance Impedance, Gain
  - — DC feed voltage and current limit
  - — Ringing frequency, voltage and current limit
  - — 12 kHz and 16 kHz Metering
  - — Programmable loop closure and ring trip thresholds
- **Ringing**
  - — 5 REN
  - — Up to 140-Vpk internal balanced sinusoidal or trapezoidal ringing with programmable DC offset
  - — Unbalanced ringing for PBX trunk compatibility
- **Powerful Signal Generator**
  - — Universal Caller ID generation
  - — Up to 4 simultaneous tones
  - — Automatic cadencing feature
- **VoicePath™ API-II Software Available to Implement FXS Functions**
  - — Supports chipset calibration
  - — Line configuration via VoicePath Profile Wizard
- **VeriVoice™ Test Suite Subscriber Loop Test**
  - — Seamless integration with API-II software
  - — Utilizes integrated self test capabilities
  - — Line fault detection and reporting
- **Pin-Selectable PCM/MPI or GCI Interface**
- **G.711 µ-law, A-law, or 16-bit Linear Coding**
- **Wideband 16 kHz Sampling Mode**
- **Integrated 150 mW 3-V or 5-V Relay Driver**
- **Small Footprint Chipset**
  - — 64-pin TQFP and exposed pad 24-pin QFN

## ORDERING INFORMATION

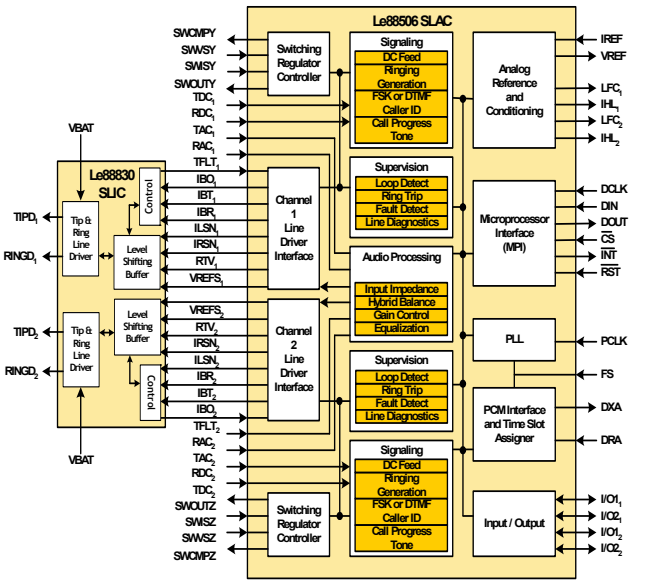
| Device OPN | Package Type | Packing[2] |
|---|---|---|
| Le88506DVC | 64-pin 10 x 10 TQFP (Green)[1] | Tray |
| Le88830KQC | 24-pin 6 x 6 QFN (Green)[1] | Tray |

1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

## DESCRIPTION

Microsemi®'s dual channel VE8820 Tracking Battery VoicePort™ chipset implements a dual-channel telephone line interface by providing all the necessary voice interface functions from the high voltage subscriber line to the µP/DSP digital interface. This chipset reduces system level cost, space, and power. Designers benefit by having a simple, cost effective, low-power and dense, interface design without sacrificing features or functionality. The programmable, feature rich VoicePort chipset provides a highly functional line interface which meets the requirements of short and medium loop (up to 1500 Ohms total) applications. Features include: high voltage switching regulator, self-test, line test capabilities, integrated ringing (up to 140-Vpk), worldwide software programmability with wideband capability, flexible signal generator with tone cadencing, caller ID generation and all BORSCHT functions. These VoicePort chipset features are crucial for designing cost-effective, full-featured Voice over Broadband solutions.

## VOICEPORT™ CHIPSET BLOCK DIAGRAM



# Table of Contents

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## PRODUCT DESCRIPTION

The VE8820 chipset implements a dual-channel universal telephone line interface. This enables the addition of a dual, low cost, high performance, software programmable line interface to cable EMTA's, fiber ONTs, Integrated Access Devices, DSL modems, SMTA's or set top boxes for multiple country applications worldwide. The VE8820 chipset performs all necessary voice telephony functions from driving a high voltage subscriber telephone line to DSP codec functions for two lines. All AC, DC, and signaling parameters are fully programmable via microprocessor interfaces. The VE8820 chipset has integrated high voltage switching regulator controllers which generate the high voltages needed for efficiently powering and ringing analog telephones. The high performance architecture permits high efficiency in all operating states and corresponding low power dissipation. Additionally, the VE8820 has self-test and line-test support to allow the system to resolve faults to the line or line circuit. The integrated digital access to important line information such as AC and DC line voltage on Tip or Ring and Metallic or Longitudinal currents is crucial for remote applications where dedicated test hardware is not cost effective.

The dual-channel VE8820 chipset is a highly functional voice-over-broadband system that meets the needs of short and medium loop customers. The VE8820 chipsets are targeted toward voice applications and provide all BORSCHT functions. The VE8820 chipset has 140-Vpk internal ringing capability that has been optimized for short loop and medium loop applications, can operate in a balanced or unbalanced ringing mode, and offers an integrated test load switch.

The Le88506 device selectively interfaces with a PCM or GCI backplane and can be controlled over the MPI or GCI interface.

The software programmed transmission filter coefficients and supervision data are easily calculated with the WinSLAC™ software, which allows the designer to enter a description of system requirements. WinSLAC then returns the necessary data and plots the predicted system results. This data is then processed by the Profile Wizard and compiled into the VoicePath™ software API to allow easy integration with system software and quickly enable implementation of the required product features.

## DETAILED FEATURES OF THE VE8820 CHIPSET

The VE8820 chipset supports the following features:

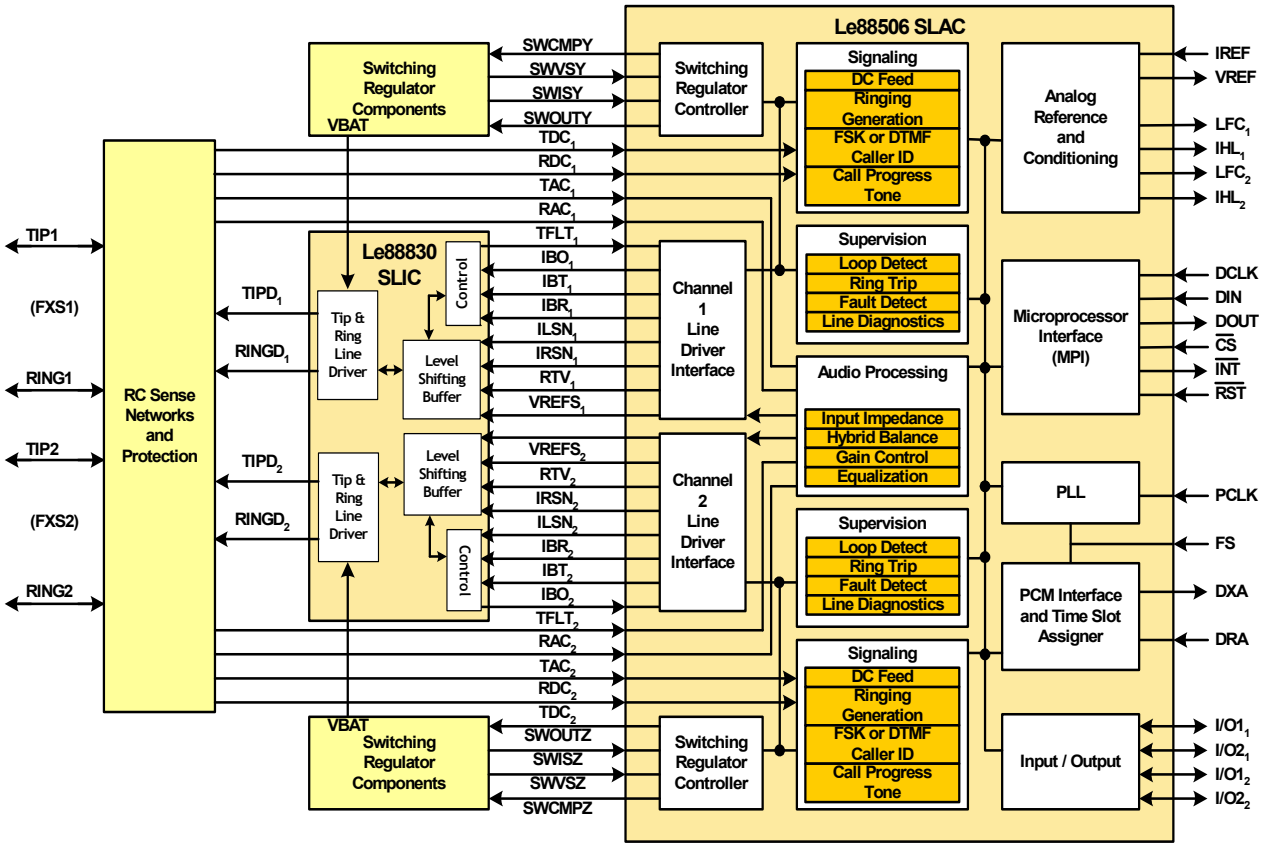
- Performs all Battery feed, Ringing, Signaling, Coding, Hybrid and Test (BORSCHT) functions
- Two chip solution provides high voltage line driving, digital signal processing, and high voltage power generation for two lines
- Wideband 7 kHz and narrowband 3.4 kHz codec modes
- Exceeds GR-909 transmission requirements
- Single hardware design meets worldwide requirements through software programming of:
  - –Ringing waveform, frequency and amplitude
  - –DC loop-feed characteristics and current-limit
  - –Loop-supervision detection thresholds
  - –Off-hook debounce circuit
  - –Ground-key and ring-trip filters
  - –Two-wire AC impedance
  - –Transhybrid balance impedance
  - –Transmit and receive gains
  - –Transmit and receive equalization
  - –Digital I/O pins
  - –A-law/µ-law and linear coding selection
  - –Switching Power Supply
- Supports both loop-start and ground-start signaling
- On-hook transmission
- Power/service denial mode
- Smooth polarity reversal
- Supports wink function
- Neon lamp driving capability
- Metering generation with envelope shaping
  - Programmable metering duration
- Self-contained ringing generation and control
  - Programmable Ringing Cadencing
  - Internal battery-backed balanced or unbalanced, sine or trapezoidal ringing
- Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Flexible tone generation
  - Howler tone generation
  - Call progress tone generation
  - DTMF tone generation
  - Universal Caller ID generation
- Only 3.3 V logic and single battery supply needed
- Integrated switching regulator controller
  - Good efficiency in all states
  - Low idle-power per line
  - Line-feed characteristics independent of battery voltage
- MPI, PCM or GCI interfaces
  - Supports most required PCM clock frequencies from 1.024 MHz to 8.192 MHz
- Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Can monitor and/or drive Tip and Ring independent
- Built-in voice-path test modes
- Integrated self-test features
- Internal relay driver
- –40°C to 85°C operation

## BLOCK DESCRIPTIONS

The VE8820 chipset provides a complete software-configurable solution to BORSCHT functions from digital interface to Tip and Ring for two channels.

The chipset comprises a CMOS device that includes a PLL to generate the necessary clocks for the internal processing functions, digital interfaces implemented in the PCM, MPI and GCI blocks, digital I/O, analog references, switching regulator controllers, voice signal processors, supervision, signalling and signal generation blocks and separate high voltage dual SLIC line driver.

**Figure 1. VE8820 VoicePort™ Block Diagram**




## Digital Interfaces

The VE8820 chipset offers two digital interface options. The first is PCM/MPI mode, in which separate serial control and voice data interfaces are provided. Voice data is interfaced via a PCM highway with time slot assignment capability, and control information is communicated over the Micro-Processor Interface (MPI). The second is GCI mode, in which a single serial interface supports both voice data and control. Wideband mode is only available in PCM/MPI mode.

The two modes are mutually exclusive and have different advantages and disadvantages. The PCM/MPI mode is most flexible and allows a wide range of DCLK (MPI data clock) and PCLK (PCM data clock) frequencies. PCM/MPI mode also allows use of the $\overline{INT}$ interrupt pin to signal pending interrupts to the external controller. GCI mode offers the advantage of using only four signals (FSC, DCL, DU, DD) to carry voice and control data. PCM/MPI mode uses twice as many signals (FS, PCLK, DXA, DRA for voice data and CSL, DCLK, DIN, DOUT for control data) to carry the same information. GCI mode has several disadvantages, however: only 2.048 MHz and 4.096 MHz DCL frequencies are allowed; the control interface is slow (250 µS/byte maximum throughput); and interrupt handling is more complex due to the lack of an interrupt pin. Multifunction pins are implemented to support these different modes while keeping the pin count low.

### PCM and GCI Mode Selection

The VE8820 chipset enters PCM/MPI or GCI modes based on the conditions outlined in Table .

The PCM / $\overline{GCI}$ select pin ($\overline{CS}$/PG) is used in combination with the DCLK pin to determine which mode the chipset is in on power up. If PG is held Low and DCLK is held static, GCI mode is entered 1 ms after power up or hardware reset and the application of valid GCI DCLK and FSC signals. GCI mode will be exited at any time if PG is pulled high or a clock is detected on DCLK.

If PG is High then PCM/MPI mode is entered following power up. At this point, the mode can be changed to GCI if the GCI conditions are met. However, once a command is sent over the MPI interface, GCI mode cannot be entered without resetting the chipset.

### PCM/GCI Mode Selection

| From mode | To mode | Requirement |
|---|---|---|
| Power On or Hardware Reset | PCM | $\overline{CS}$/PG = 1 *or* DCLK has ac clock present |
| Power On or Hardware Reset | GCI | $\overline{CS}$/PG = 0 *and* DCLK does not have ac clock present |
| GCI | PCM | $\overline{CS}$/PG = 1 *or* DCLK has clock present |
| PCM | GCI | No commands yet sent in PCM state *and* $\overline{CS}$/PG = 0 (for more than 2 FS) *and* DCLK does not have clock present |

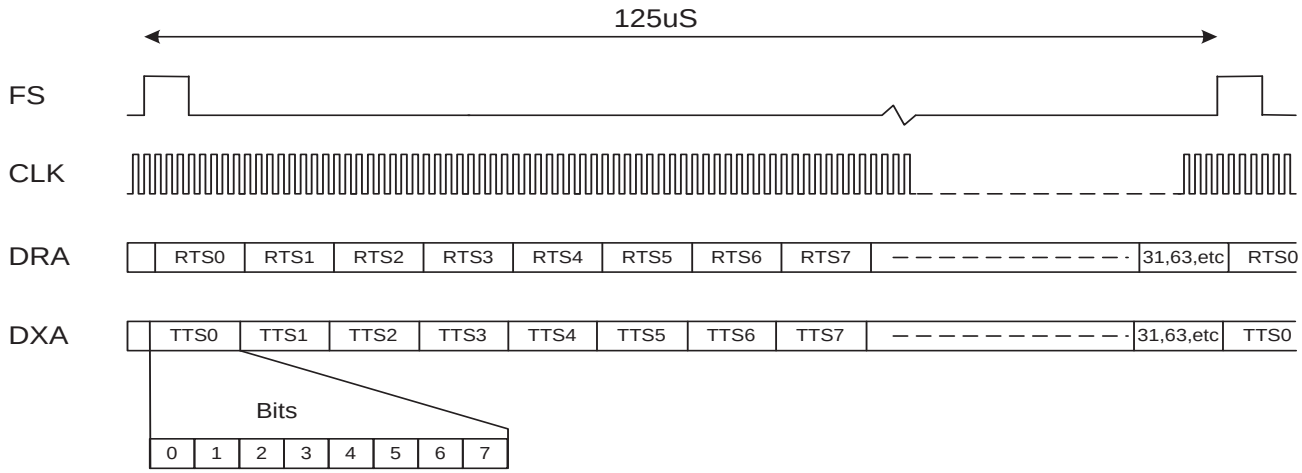
These methods are used to ensure the chipset operates in the desired mode at all times.

## PCM/MPI Interface and Time Slot Assigner (PCM)

This is a synchronized serial mode of communication between the system and the VE8820 chipset. In PCM mode, data can be transmitted/received on a serial PCM highway. This highway uses FS and PCLK as reference.

Data is transmitted out of the DXA pin and received on the DRA pin. The VE8820 chipset transmits/receives single 8-bit time slot (A-law/µ-law) compressed voice data or 16-bit two's complement linear voice data, occupying two conventional time slots. The PCLK is a data clock supplied to the chipset that determines the rate at which the data is shifted in/out of the PCM ports. The Frame Sync (FS) pulse identifies the beginning of a transmit/receive frame and all time slots are referenced to it. For the VE8820 chipset, the frequency of the FS signal is 8 kHz. In wideband mode, two evenly spaced sets of time slots are exchanged in each frame.The user programs the first time slot and the second one is generated automatically and placed 125/2 µsec from the first time slot (the frame is assumed to have an even number of time slots). The PCLK frequency can be a number of fixed frequencies as defined by command *46/47h Write/Read Device Configuration Register*, on page 70. For each channel, voice data compression and type of coding is selected by the C/L (Compressed/Linear) and A/µ-law bits in command *60/61h Write/Read Operating Functions*, on page 77. The wideband mode is selected with the WBAND bit in command *4A/4Bh Write/Read Channel Enable and Operating Mode Register*, on page 71 and it affects both channels of the chipset.

**Figure 2. PCM highway structure**



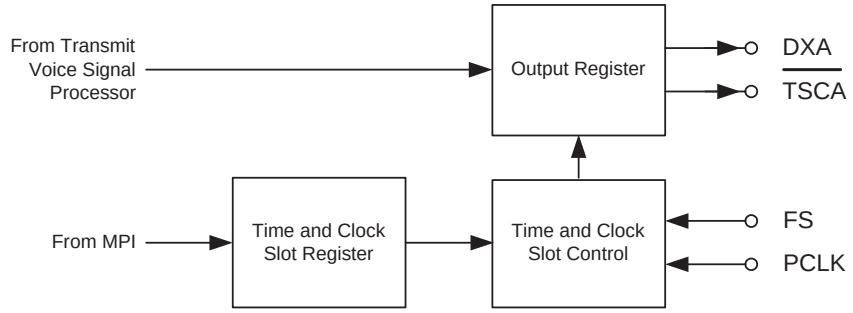
The VE8820 chipset command *44/45h Write/Read Transmit and Receive Clock Slot and Transmit Clock Edge*, on page 70 allows the time slots to be offset to eliminate any clock skew in the system. The Transmit Clock Slot and Receive Clock Slot fields are each three bits wide to offset the time slot assignment by 0 to 7 PCLK periods. The Transmit and Receive Clock Slot is a global command that is applied at the chipset level. Thus, for each channel, two time slots must be assigned—one for transmitting voice data and the other for receiving voice data. Figure 2 shows the PCM highway time slot structure.

### Transmit PCM Interface

The Transmit PCM interface receives a code from the voice signal processor (compressor), which may be either 8 bit compressed code (A-law/μ-law) or a 16-bit two's complement linear code. The transmit PCM interface logic (Figure 3) controls the transmission of the data onto the PCM highway through the output port selection circuitry and the time and clock slot control block. The time slot control signal ($\overline{\text{TSCA}}$) is low whenever PCM data is transmitted on the DXA pin. This signal can be used for arbitration when there are multiple VE8820 chipsets on the PCM bus. The data can be transmitted on either edge of the PCLK. The clock edge on which the data is transmitted is selected by the XE bit in the Transmit and Receive Clock Slot Register (Command 44h/45h).

Command *40/41h Write/Read Transmit Time Slot*, on page 69 allows the time slot of the selected channel to be programmed. The Transmit Time Slot Register allows up to 128 8-bit time slots (using a PCLK of 8.192 MHz) in each frame. The PCLK frequency can be a number of fixed frequencies as defined by command *46/47h Write/Read Device Configuration Register*, on page 70; this means that for compressed data the number of 8-bit time slots can vary between 24 and 128, while linear mode supports between 12 and 64 pairs of time slots. In wideband mode, the user must only program time slots in the lower half of the range. Note that linear mode requires two back-to-back time slots to transmit one voice channel. The data is transmitted in bytes with the most significant bit first. Figure 5, *PCM Interface Timing for XE = 0 (Transmit Data On Negative PCLK Edge)*, on page 9 illustrates data flow on the PCM highway.

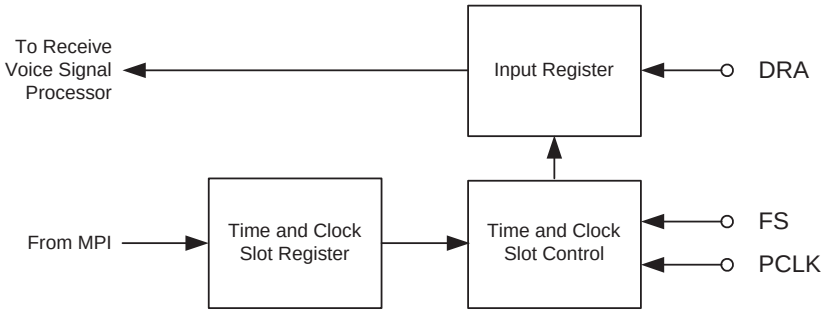
**Figure 3. Transmit PCM interface**




### Receive PCM Interface

The receive PCM interface logic (Figure 4) controls the reception of data bytes from the PCM highway. 8-bit compressed (A-law/μ-law) or 16-bit two's complement linear data is formatted and passed to the voice signal processor (expander).

**Figure 4. Receive PCM Interface**




Command *42/43h Write/Read Receive Time Slot*, on page 70 allows the time slot of the selected channel to be programmed. The Receive Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots (using a PCLK of 8.192 MHz) in each frame. The PCLK frequency can be a number of fixed frequencies as defined by command *46/47h Write/Read Device Configuration Register*, on page 70; this means that for compressed data the number of 8-bit time slots can vary between 24 and 128, while linear mode supports between 12 and 64 pairs of time slots. In wideband mode, the user must only program time slots in the lower half of the range. Note that linear mode requires two back-to-back time slots to transmit/receive one voice channel. The data is transmitted/received in bytes with the most significant bit first. Figure 5, *PCM Interface Timing for XE = 0 (Transmit Data On Negative PCLK Edge)*, on page 9 illustrates data flow on the PCM highway.

### Signaling on the PCM Highway

Signaling information can be sent on the PCM output if A- or µ-Law companding is selected and the SMODE bit in command *46/47h Write/Read Device Configuration Register*, on page 70 is set. In this case an extra time slot of signaling data is transmitted every frame immediately after the PCM voice data for the channel (see Figure 5, *PCM Interface Timing for XE = 0 (Transmit Data On Negative PCLK Edge)*, on page 9) and is transmitted whether or not the voice channel is active. The signaling data is defined in Table  and Table .

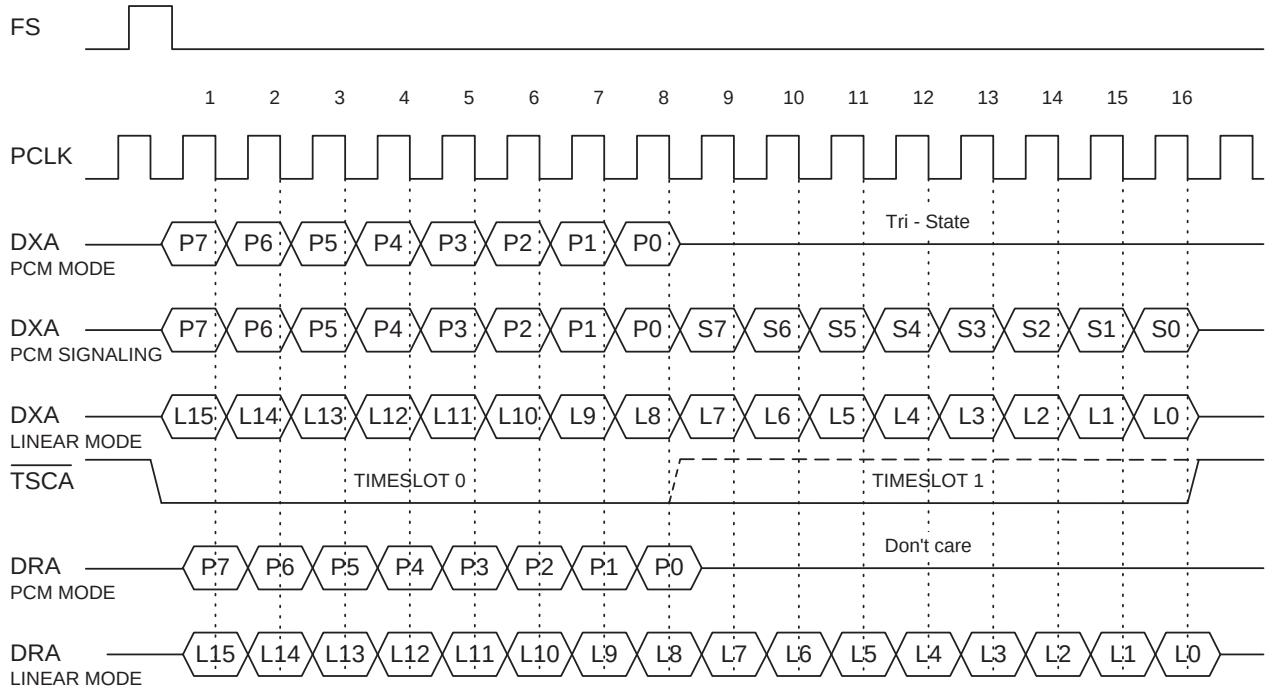
**PCM Highway Real Time Signaling Data Definition**

| | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |
|---|---|---|---|---|---|---|---|---|
| Channel 1 | CFAIL | $OCALMY_1$ | $TEMPA_1$ | $IO2_1$ | $CAD_1$ | $CID_1$ | $GNK_1$ | $HOOK_1$ |
| Channel 2 | DAT | $OCALMZ_2$ | $TEMPA_2$ | $IO2_2$ | $CAD_2$ | $CID_2$ | $GNK_2$ | $HOOK_2$ |

Default settings, of consecutive time slots for Channel 2, cannot be used with PCM signaling. Also, the monitor A-->D converter output on the PCM highway is in linear mode which conflicts with PCM signaling.

Masking or unmasking of the interrupts in the interrupt mask register does not affect the real time signaling data. See command *4D/4Fh Read Signaling Register*, on page 72 for bit definitions.

**Figure 5. PCM Interface Timing for XE = 0 (Transmit Data On Negative PCLK Edge)**




## MICROPROCESSOR INTERFACE (MPI)

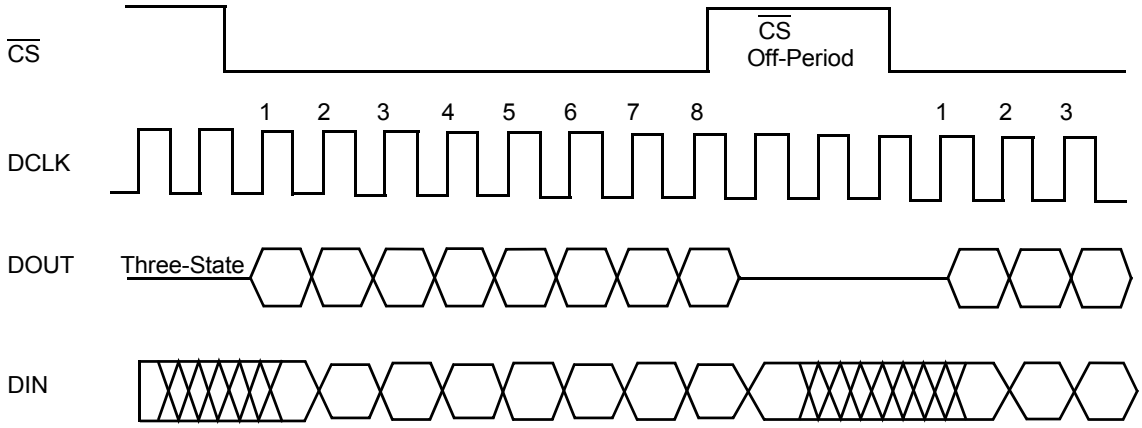
The microprocessor interface (MPI) block communicates with the external host microprocessor over a serial interface. It passes user control information to the other blocks, and it passes status information back to the external host.

The MPI physically consists of a serial data input (DIN) serial data output (DOUT), a data clock (DCLK), a chip select ($\overline{CS}$) and an interrupt signal ($\overline{INT}$) (see Figure 6, *Microprocessor Interface Timing*, on page 10). The serial input consists of 8-bit commands that can be followed with additional bytes of input data, or can be followed by the VE8820 chipset sending out bytes of data. All data input and output is MSB (D7) first and LSB (D0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going High for

at least a minimum off period (see *Microprocessor Interface Timing*, on page 54) before the next byte is read or written. Only a single channel should be enabled during read commands.

All commands that require additional input data to the chipset must have the input data as the next N words written into the chipset (for example, framed by the next N transitions of $\overline{CS}$). All unused bits must be programmed to 0 to ensure compatibility with future parts. All commands that are followed by output data will cause the chipset to output data for the next N transitions of $\overline{CS}$ going Low. The VE8820 chipset will not accept any commands until all the data has been shifted out. The output values of unused bits are not specified. Note that the Voice Channel Enable bits, EC1, EC2 in command *4A/4Bh Write/Read Channel Enable and Operating Mode Register*, on page 71 are used to control access to voice channel specific registers within the chipset.

**Figure 6. Microprocessor Interface Timing**




An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the $\overline{CS}$ lines are held in the High state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK can be run to a number of VE8820 chipsets and the individual $\overline{CS}$ lines will select the appropriate chipset to access. Between command sequences, DCLK can stay in the High state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. Between bytes of a multi byte read or write command sequence, DCLK can also stay in the High state indefinitely. DCLK can stay in the Low state indefinitely with no loss of internal control information, provided the $\overline{CS}$ line remains at a High level. If the system controller has a single bi-directional serial data pin, the DOUT pin of the VE8820 chipset can be connected to its DIN pin.

If a low period of $\overline{CS}$ contains less than 8 positive DCLK transitions, it is ignored. If it contains 8 to 15 positive transitions, only the last 8 transitions matter. If it contains 16 or more positive transitions, a hardware reset in the part occurs. If the chip is in the middle of a read sequence when $\overline{CS}$ goes Low, data will be present at the DOUT pin even if DCLK has no activity.

### Controlling Registers using read / modify / write.

In general, this coding method is not recommended for updating VoicePort chipset registers. The MPI interface is relatively slow speed, so operating on a local copy of this type of register data will provide higher performance.

In particular, some read / write registers are also accessed and modified by the internal state machine, especially on entering and exiting the Ringing States. This means that for these registers, a read modify write sequence can produce unpredictable results. The list of registers which must not be accessed using this technique is:

*50/51h Write/Read Voice Path Gains*, on page 74
*56/57h Write/Read System State*, on page 75
*60/61h Write/Read Operating Functions*, on page 77
*70/71h Write/Read Operating Conditions*, on page 79
*A6/A7h Write/Read Converter Configuration*, on page 85
*CA/CBh Write/Read Digital Impedance Scaling Network (DISN)*, on page 88
*E6/E7h Write/Read Switching Regulator Control*, on page 97
*EA/EBh Write/Read Caller Identification Number Parameters*, on page 99

### Interrupt Servicing in MPI Mode

The VE8820 chipset has a well-defined interrupt structure. All the interrupts in the VE8820 chipset can be masked. Interrupts are caused only when a status bit is unmasked and the status bit is subsequently set or toggles (depending on the interrupt).

The VE8820 chipset generates interrupts in response to a number of line supervision events. When an interrupt is generated, its status is placed in the *4D/4Fh Read Signaling Register*, on page 72. Multiple interrupts can be reported in the signaling register. When the first interrupt occurs, the interrupt pin, $\overline{INT}$, will be pulled Low to signal the external microprocessor that an interrupt has occurred. When the external microprocessor has serviced the interrupts by reading *4D/4Fh Read Signaling Register* and clearing the interrupt (Command 4Fh) or *CDh Read Transmit PCM/Test Data*, on page 88 (if ATI is set), the $\overline{INT}$ pin will go High. An interrupt is generated whenever a signaling register status bit changes (1 to 0 or 0 to 1) and the corresponding mask bit in *6C/6Dh Write/Read Interrupt Mask Register*, on page 79 is unmasked. Therefore, the software application is responsible for keeping track of the previous status and deciding the transition type (rising edge transition or falling edge transition). The interrupt pin drive mode can be programmed to be 3.3 V CMOS push/pull or open drain. Signaling status can also be polled without upsetting any pending interrupt status by using command 4Dh.

The following status bits related to channel 1 and channel 2 can cause an interrupt to occur:

**Definitions of Status Bits**

| | |
|---|---|
| CFAIL: | PCM clock (PCLK) or 8 kHz frame sync (FS) failure |
| OCALMY: | Switching regulator Y over current indication |
| $TEMPA_1$: | Thermal Fault has been detected |
| $IO2_1$: | Input 2 Status. The input value at $IO2_1$ has changed |
| $CAD_1$: | Cadencer interrupt when programmed on period is completed |
| $CID_1$: | Caller ID Buffer Ready |
| $GNK_1$: | Ground-key status has changed |
| $HOOK_1$: | Hook status has changed |
| DAT: | Measurement data available in XDAT register |
| OCALMZ: | Switching regulator Z over current indication |
| $TEMPA_2$: | Thermal Fault has been detected |
| $IO2_2$: | Input 2 Status. The input value at $IO2_2$ has changed |
| $CAD_2$: | Cadencer interrupt when programmed on period is completed |
| $CID_2$: | Caller ID Buffer Ready |
| $GNK_2$: | Ground-key status has changed |
| $HOOK_2$: | Hook status has changed |

## General Circuit Interface (GCI)

The GCI block does not support the wideband (16kHz) sampling mode.

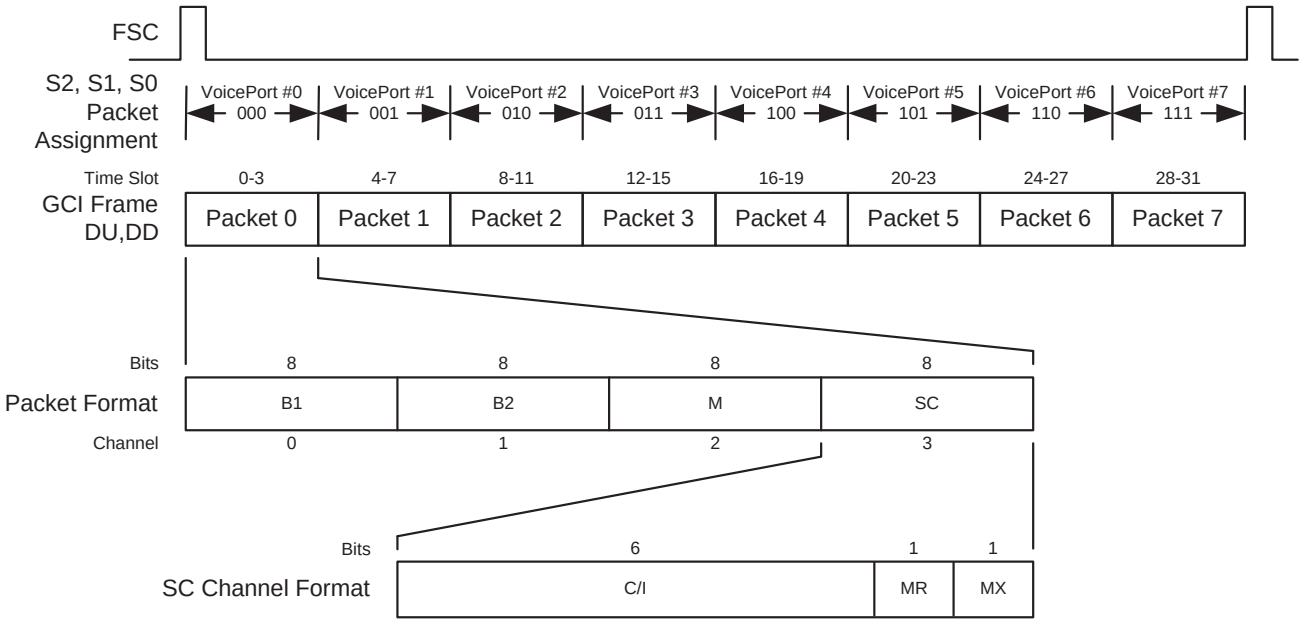
In GCI mode, this block carries both control and data on the same serial bus, replacing both MPI and PCM functionality. When the $\overline{CS}$/PG pin is connected to DGND and DCLK/S0 is static (not toggling), GCI operation is selected. The VE8820 chipset conforms to the GCI standard where data for eight GCI packets are combined into one serial bit stream. A GCI packet contains the control and voice data for the two analog channels of the VE8820 chipset. The VE8820 chipset sends Data Upstream out of the DU pin and receives Data Downstream on the DD pin. Data clock rate and frame synchronization information goes to the VE8820 chipset on the DCL (Data Clock) and FSC (Frame Sync.) input pins, respectively.

### GCI Format and Command Structure

The GCI interface provides communication of both control and voice data between the GCI highway and subscriber Voice Ports over a single pair of pins on the VE8820 chipset. A complete GCI frame is sent upstream on the DU pin and received downstream on the DD pin every 125 µs. Each frame consists of eight 4-byte GCI packets that contain voice and control information for 8 pairs of channels. The overall structure of the GCI frame is shown in Figure 7. The four-time slot GCI packets contain the following:

- Two voice-data channels
  - B1 provides compressed PCM data for Voice Channel 1
  - B2 provides compressed PCM data for Voice Channel 2
- One Monitor (M) channel for reading and writing control data and coefficients to the chip set in combination with the MX and MR bits in the Signaling and Control channel
- One Signaling and Control (SC) channel containing a 6-bit Command/Indicate (C/I) field for real time control information and a two-bit field with Monitor Receive and Monitor Transmit (MR and MX) bits for handshaking functions linked to the Monitor channel. All principal signaling (real-time critical) information is carried on the C/I channel.

**Figure 7. Multiplexed GCI Time Slot Structure**




In the packet control block (shown in Figure 8), the Frame Sync (FSC) pulse identifies the beginning of the Transmit and Receive frames and all GCI packets are referenced to it. Voice (B1 and B2), C/I, and Monitor data are sent to the Upstream Multiplexer where they are combined and serially shifted out of the DU pin in the selected GCI packet time slots. The Downstream Demultiplexer uses the same packet control block information to demultiplex the incoming GCI packet into separate voice (B1 and B2), C/I, and Monitor channels.

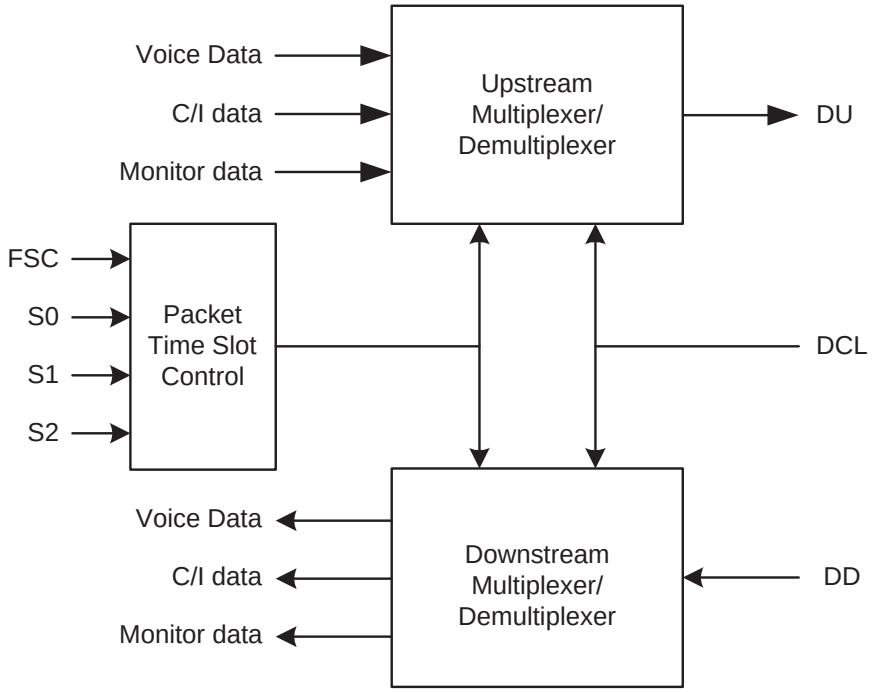
### GCI Packet Assignment Codes

| $\overline{\text{INT}}$/S2 | DIN/S1 | DCLK/S0 | GCI Packet |
|---|---|---|---|
| DGND | DGND | DGND | 0 |
| DGND | DGND | DVDD | 1 |
| DGND | DVDD | DGND | 2 |
| DGND | DVDD | DVDD | 3 |
| DVDD | DGND | DGND | 4 |
| DVDD | DGND | DVDD | 5 |
| DVDD | DVDD | DGND | 6 |
| DVDD | DVDD | DVDD | 7 |

The external clock applied to the DCL pin must be either 2.048 MHz or 4.096 MHz. The VE8820 chipset determines the incoming clock frequency and adjusts internal timing automatically to accommodate single or double clock rates. Correct clock detection can be determined by reading the CSEL bits in *46/47h Write/Read Device Configuration Register,* on page 70. Upstream and Downstream Data is always transmitted at a 2.048 MHz data rate.

The VE8820 chipset supports access to all eight GCI packets (16 analog channels). The S0, S1 and S2 GCI Packet Assignment pins on the VE8820 chipset are encoded as shown in Table .

**Figure 8. GCI Interface and Packet Time Slot Selection**



### Signaling and Control (SC)

The downstream and upstream SC channels are continuously sending state control and loop supervision data every frame to and from the VE8820 chipset in the C/I field. This allows the upstream processor to have immediate access to the VoicePort line status. The MR and MX bits are used for handshaking during data exchange on the monitor channel.

The format of the downstream control (C) field is shown in Table . The VE8820 chipset receives the most significant bit first.

**Down Stream SC Channel Definition**

| Channel | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 1 | A | POLNR | System_State[3:0] | | | | MR | MX |

A: Channel address bit.
0: Select Channel 1 as the downstream data destination.
1: Select Channel 2 as the downstream data destination.

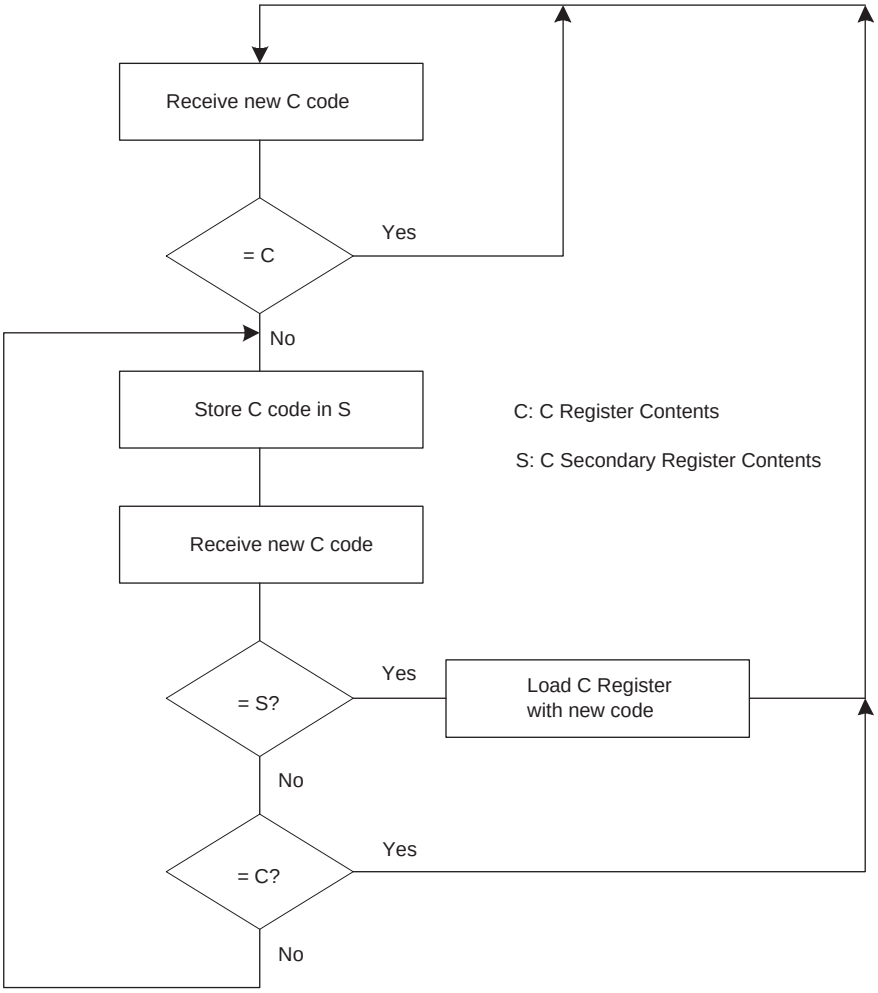
POLNR: VoicePort Feed Polarity
0: Normal Polarity feed - TipD more positive than RingD
1: Reverse Polarity feed - RingD more positive than TipD

$SS3_i$-$SS0_i$: System State. Valid system states are listed here. All other codes are reserved.
0000: Disconnect, ACT = 0
0001: Tip Open, ACT = 0
0010: Ring Open, ACT = 0
0011: Active, ACT = 1
0100: Idle, ACT = 0
0101: Longitudinal Test, ACT = 1
0110: Metallic Test, ACT = 1
0111: Balanced Ringing, ACT = 1
1000: Low Gain, ACT = 1
1010: Unbalanced Ringing, ACT = 1
1111: Shutdown, ACT = 0

See *56/57h Write/Read System State*, on page 75 for more description of the system states.

Figure 9 shows a flow chart describing the transmission protocol for the downstream channel, which provides a high level of security for the C field data exchange. Whenever the received pattern of C bits 6 through 1 is different from the pattern currently in the C input register, the new pattern is loaded into a secondary C register, and a latch is set. When the next pattern is received (in the following frame) while the latch is set, the following rules apply:

**Figure 9. Security Procedure For C Downstream Byte**




- If the received pattern corresponds to the pattern in the secondary register, the new pattern is loaded into the C register, and the latch is reset.
- If the received pattern is different from the pattern in the secondary register and different from the pattern currently in the C register, the newly received pattern is loaded into the secondary C register, and the latch remains set.
- If the received pattern is the same as the pattern currently in the C register, the C register is unchanged, and the latch is reset.

The format of the upstream indication (I) field is shown in Table . The VE8820 chipset transmits the I field most significant bit first each frame.

### Upstream SC Channel

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| $SLCX_2$ | $GNK_2$ | $HOOK_2$ | $SLCX_1$ | $GNK_1$ | $HOOK_1$ | MR | MX |

$SLCX_2$ Summary output of the Channel 2 Signaling Register

1: One or more of the unmasked bits in the Signaling Register has toggled.

0: None of the unmasked bits in the Signaling Register has toggled.
This is a logic “or” of $TEMPA_2$, DAT, $IO2_2$, $CAD_2$, $GNK_2$, $HOOK_2$ and $OCALM_2$. This bit is reset when the signalling register is read using the 4F read and clear interrupt from *4D/4Fh Read Signaling Register,* on page 72.

$GNK_2$: Indication if a ground connection is taking place
- 1: Ground connection
- 0: No ground connection

$HOOK_2$: Indication of loop condition
- 1: Subscriber is off-hook
- 0: Subscriber is on-hook

$SLCX_1$ Summary output of the Channel 1 Signaling Register
- 1: One or more of the unmasked bits in the Signaling Register has toggled.
- 0: None of the unmasked bits in the Signaling Register has toggled.
  This is a logic "or" of $TEMPA_1$, CFAIL, $IO2_1$, $CAD_1$, $GNK_1$, $HOOK_1$ and $OCALM_1$. This bit is reset when the signalling register is read using the 4F read and clear interrupt from *4D/4Fh Read Signaling Register*, on page 72.

$GNK_1$: Indication if a ground connection is taking place
- 1: Ground connection
- 0: No ground connection

$HOOK_1$: Indication of loop condition
- 1: Subscriber is off-hook
- 0: Subscriber is on-hook

Data from the loop supervision circuitry (with applicable debouncing) is latched by a derivative of Frame Sync every 125 µs. This real-time latched data is transmitted upstream in the I field every frame (125 µs). Note that it is not the data in the Signaling Register. Hence masking or unmasking of the HOOK and GNK interrupts in the interrupt mask register will not affect the HOOK and GNK data in the SC channel.

### Monitor Channel Protocol

The Monitor (M) channel (see Figure 10) loads the VE8820 chipset internal registers, reads the status of the chipset and the contents of the internal registers, and provides supplementary signaling. Information is transferred on the Monitor Channel using the MR and MX bits of the third (SC) channel to provide a reliable method of data exchange between the higher level processor and the VE8820 chipset (see Figure 10).

The monitor channel is the third channel in the 4-channel packet sent and received every 125 µs. A monitor command consists of one address byte and one or more command bytes followed by additional bytes of input data. The command can be followed by the VE8820 chipset sending data bytes upstream via the DU pin.

**Figure 10. Maximum Speed Monitor Handshake Timing**

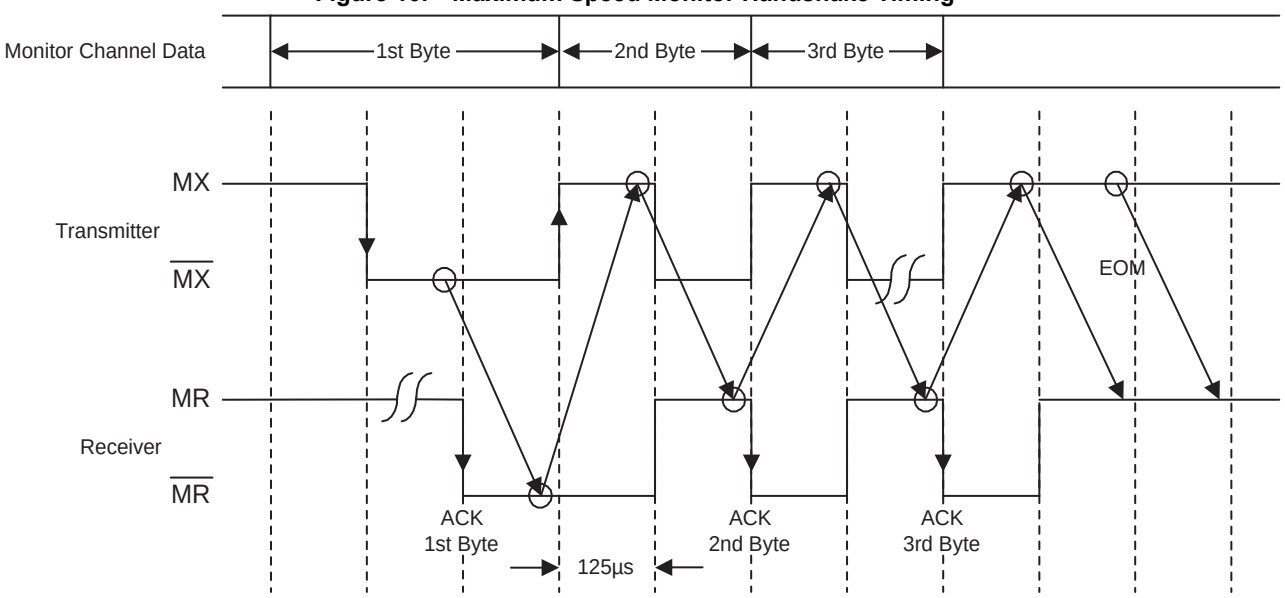
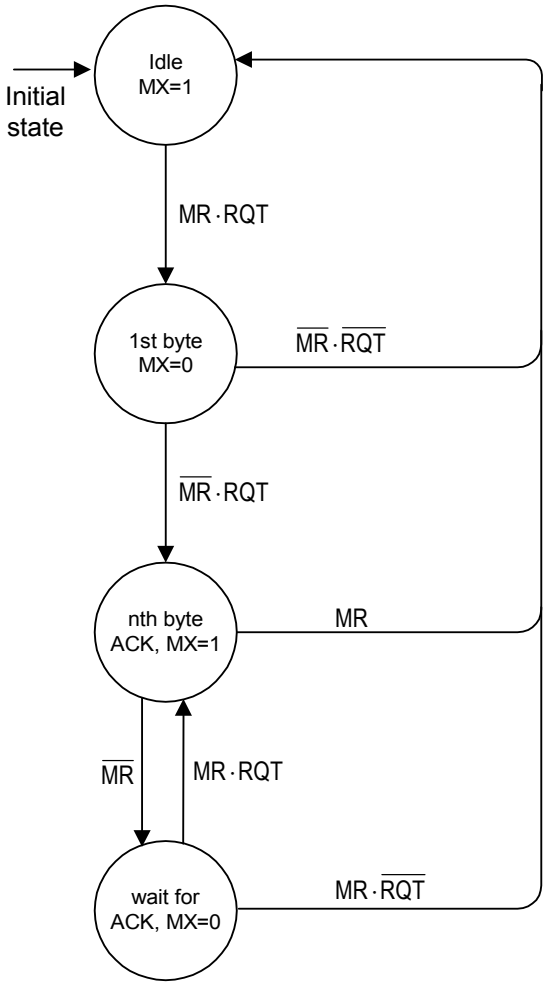


**Figure 11. Monitor Transmitter Mode Diagram**

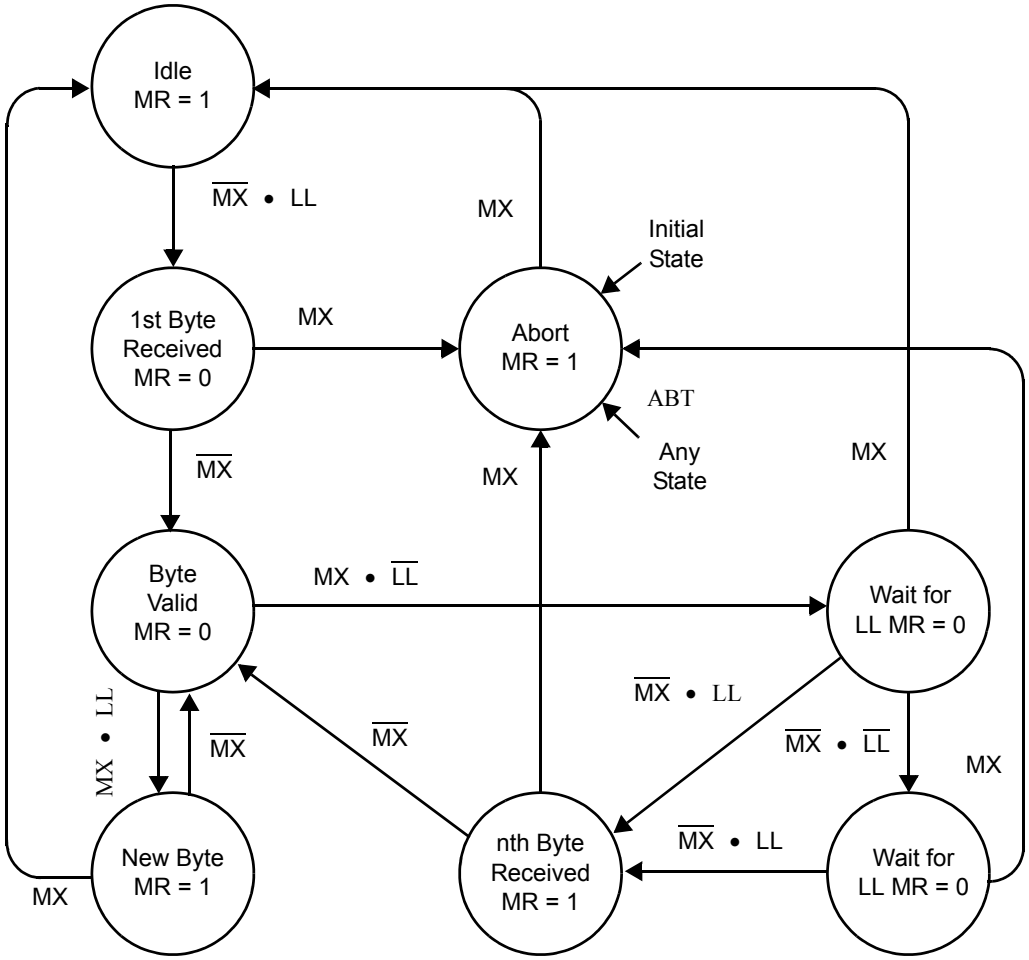



MR ... MR - bit received
MX ... MX - bit calculated and expected on the DU line
RQT ... Request for transmission from internal source

- An inactive (High) MX and MR pair bit for two or more consecutive frames shows an idle state on the monitor channel and the end of message (EOM).
- Figure 10 shows that transmission is initiated by the transition of the transmitter MX bit from the inactive to the active state. The transition coincides with the beginning of the first byte sent on the monitor channel. The receiver acknowledges the first byte by setting MR bit to active and keeping it active for at least one more frame.
- The same data must be received in two consecutive frames in order to be accepted by the receiver.
- The same byte is sent in each of the succeeding frames until either a new byte is transmitted, the message ends, or an abort occurs. Any abort command resets any pending commands in the VE8820 chipset. The chipset remains in the previous configuration and is ready to receive a new command.
- Any false MX or MR bit received by the receiver or transmitter leads to a request-for-abort or an abort, respectively.
- To obtain maximum data transfer speed, the transmitter anticipates the falling edge of the receiver's acknowledgment as shown in Figure 10.

Figure 11 and Figure 12 are state diagrams that define the operation of the monitor transmitter and receiver sections in the VE8820 chipset.

**Figure 12. Monitor Receiver Mode Diagram**




MR: MR bit transmitted on DU line
MX: MX bit received on DD line
LL: Last look at monitor byte received
ABT: Abort indication from internal source

### Programming with the Monitor Channel

The VE8820 chipset uses the monitor channel for the transfer of status or mode information to and from higher level processors. The higher level processor is synchronized to the VE8820 chipset using the time slot straps S0, S1 and S2.

The messages transmitted in the monitor channel have different structures. The first byte of monitor channel data in the GCI format indicates the address of the chipset either sending or receiving the data. All monitor channel messages to/from the VE8820 chipset begin with this address byte:

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | A | B | 0 | 0 | C |

A

0: Channel 1 is the source (upstream) or destination (downstream)
1: Channel 2 is the source (upstream) or destination (downstream)

B

0: Data destination determined by A
1: Both Channel 1 and 2 receive the data

C

0: Address for channel identification command
1: Address for all other commands

Transmission in the GCI monitor channel starts with an address byte followed by a command byte. If the command byte specifies a write, from 1 to 14 additional data bytes can follow (see Table ). If the command byte specifies a read, additional data bytes can follow. The VE8820 chipset responds to the read command by sending out the original address byte and up to 14 bytes upstream that contain the information requested by the upstream controller. Generic byte transmission sequence over the GCI monitor channel is shown in Table .

### Monitor Byte Transmission Sequence

| GCI Monitor Channel | |
|---|---|
| **Downstream** | **Upstream** |
| ADDRESS<br>Control byte, write<br>Data byte 1*<br>•<br>Data byte m*<br>ADDRESS<br>Control byte, read<br><br>m ≤ 14 | <br><br><br><br><br><br>Data byte 1<br>•<br>Data Byte n*<br>n ≤ 14 |

***Note:***

** May or may not be present*

## Channel Identification Command (CIC)

When the monitor channel address byte is 80H or 90H, a command of 00H is interpreted by the VE8820 chipset as a two-byte Channel Identification Command (CIC).

The format for this command is shown next:

| | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| Address Byte | 1 | 0 | 0 | A | 0 | 0 | 0 | 0 |
| Command Byte | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

A

0: Channel 1 is the destination
1: Channel 2 is the destination

Immediately after the last bit of the CIC command is received, the VE8820 chipset responds with the two-byte channel ID code indicating an analog transceiver chipset type in bits 6 and 7 of byte 2, with the following configuration options:

| | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| Byte 1 | 1 | 0 | 0 | A | PCN4 | PCN3 | PCN2 | PCN1 |
| Byte 2 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

A

0: Channel 1 is the destination
1: Channel 2 is the destination

PCN[4:1] Product Code Number
Fh Le88506 device

When the VE8820 chipset has completed transmission of the channel ID information, it sends an EOM (MX = 1 for two successive frames) on the upstream C/I channel. The VE8820 chipset also expects an EOM to be received on the downstream C/I channel before any further message sequences are received.

## General Structure of Other Commands

When the monitor channel address byte is 81h, 89h, 91h, or 99h, the command byte is interpreted by the VE8820 chipset as either a Transfer Operation (TOP), Status Operation (SOP), or a Coefficient Operation (COP).

| | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| Address Byte | 1 | 0 | 0 | A | B | 0 | 0 | 1 |

A

0: Channel 1 is the source (upstream) or destination (downstream)
1: Channel 2 is the source (upstream) or destination (downstream)

B

0: Data destination determined by A
1: Both Channel 1 and 2 receive the data

Commands are sent to the VE8820 chipset to:

- Read the status of the system without changing its operation
- Write/read the VE8820 chipset operating mode
- Write/read filter coefficients

## Input / Output Block

This block controls general-purpose pins that can be configured by the user as inputs, outputs, or relay drivers. CMOS-compatible I/O pins (I/O1 and I/O2) are provided per channel. I/O1 can act either as a standard digital input, as a CMOS output, or can be configured as a 5-V tolerant open drain relay driver. When configured as such, it is capable of directly driving a 150-mW 3-V or 5-V relay and has an integrated protection circuit. I/O2 is a standard digital I/O pin that can also generate interrupts when configured as an input. The pins are accessed using Command *52/53h Write/Read Input/Output Data Register,* on page 74. The direction of the I/O pins (input or output) and output type is specified by programming *54/55h Write/Read Input/Output Direction Register,* on page 75.

## Voice Signal Processors

This block performs digital signal processing for the transmission and reception of voice. It includes G.711 compression/decompression, impedance matching, filtering, gain control, DTMF generation and general-purpose tone generators for each channel. Additionally caller ID FSK generation and metering generation are provided.

This block performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters perform the following functions:

- Sets the receive and transmit gain
- Performs the transhybrid balancing function
- Permits adjustment of the two-wire termination impedance
- Provides frequency attenuation adjustment (equalization) of the receive and transmit paths

All programmable digital filter coefficients can be calculated using Microsemi's WinSLAC software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or µ-law.

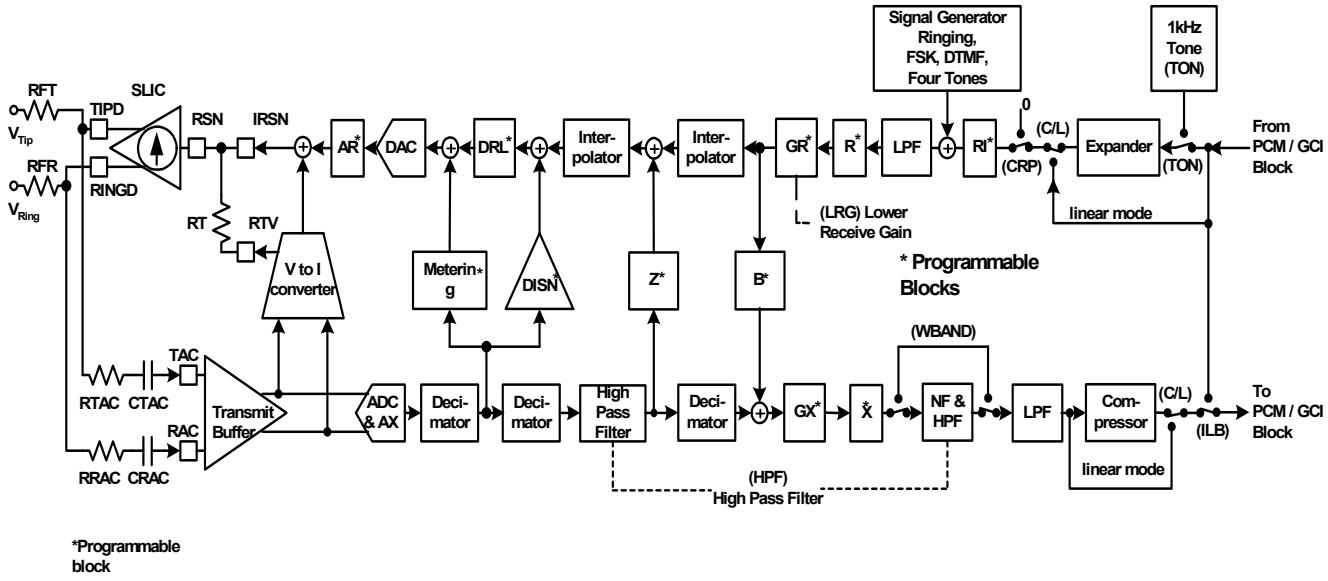
### Overview of Digital Filters

Several of the blocks in the signal processing section are user programmable. These allow the user to optimize the performance of the VE8820 chipset for the system. Figure 13 shows the VE8820 chipset signal processing for one channel and indicates the programmable blocks and how this section interfaces with the high voltage line driver and line sensing circuits.

The advantages of digital filters are:

- High reliability
- No drift with time or temperature
- Unit-to-unit repeatability
- Superior transmission performance
- Flexibility
- Maximum bandwidth for V.90 modems

**Figure 13. Voice Signal Processing Block Diagram**




### Analog Impedance Synthesis

The analog impedance synthesis loop is comprised of the high voltage line driver, the AC sense path components, the transmit amplifier, and a voltage to current converter. Nominally, this converter uses an external resistor, $R_T$. $R_T$ synthesizes the nominal impedance in the analog domain.

### Two-Wire Impedance Matching

Two feedback paths in the voice signal processor modify the two-wire input impedance by providing a programmable feedback path from the AC sense path to the line driver outputs.

The DISN path is comprised of the voice A/D and its first stage of decimation, a Digital Impedance Scaling Network (DISN), and the voice DAC. The DISN synthesizes a portion of the ac impedance which appears in parallel with $R_T$ and is used to modify the

impedance set by the external analog network. The DISN is controlled by an 8-bit word. See *CA/CBh Write/Read Digital Impedance Scaling Network (DISN)*, on page 88..

The Z filter is a programmable digital filter providing an additional path and programming flexibility over the DISN in modifying the transfer function of the synthesis loop. Together, the RT, DISN, and Z-Filter enable the user to synthesize virtually all required telephony device input impedances. See *98/99h Write/Read Z Filter FIR Coefficients*, on page 84. and *9A/9Bh Write/Read Z Filter IIR Coefficients*, on page 84.

### Frequency Response Correction and Equalization

The voice signal processor contains programmable filters in the receive (R) and transmit (X) directions that may be programmed for line equalization and to correct any attenuation distortion caused by the Z filter. See *8A/8Bh Write/Read R Filter Coefficients*, on page 83. and *88/89h Write/Read X Filter Coefficients*, on page 82.

### Transhybrid Balancing

The voice signal processor's programmable B filter is used to adjust transhybrid balance. The filter has a single pole IIR section (BIIR) and an eight-tap FIR section (BFIR), both operating at 16 kHz. See *86/87h Write/Read B Filter FIR Coefficients*, on page 81. and *96/97h Write/Read B Filter IIR Coefficients*, on page 84.

### Gain Adjustment

The transmit path has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2.0), located immediately before the A/D converter. See *50/51h Write/Read Voice Path Gains*, on page 74.. GX is a digital gain block that is programmable from 0 dB to +12 dB, with a worst-case step size of 0.1 dB for gain settings below +10 dB, and a worst-case step size of 0.3 dB for gain settings above +10 dB. The filters provide a net gain in the range of 0 dB to 18 dB. See *80/81h Write/Read GX Filter Coefficients*, on page 80..

The receive voice path has three programmable gain blocks. GR is a digital loss block that is programmable from 0 dB to 12 dB, with a worst-case step size of 0.1 dB. See *82/83h Write/Read GR Filter Coefficients*, on page 80.. DRL is a digital loss block of 0 dB or 6.02 dB. AR is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2) or a loss of 6.02 dB (gain of 0.5), located immediately after the D/A converter. See *50/51h Write/Read Voice Path Gains*, on page 74. This provides a net loss in the range of 0 dB to 18 dB. AR is limited to 0 or -6.02 dB when DRL is 0 dB, and +6.02 dB or 0 dB if DRL is 6.02 d of loss.

Metering is affected by the AR gain block. To achieve the specified levels, the DRL loss is enabled, and AR gain is applied whenever metering is used.

### Transmit Signal Processing

In the transmit path (A/D), the AC Tip - Ring analog input signal is sensed by the TAC and RAC pins, buffered, amplified by the analog AX gain and sampled by the A/D converter, filtered, companded (for A-law or µ-law), and made available to the PCM or GCI blocks. Linear mode is only available in the PCM/MPI mode. If linear format is selected, the 16-bit data will be transmitted in two consecutive time slots starting at the programmed time slot. The B, X, and GX digital filter blocks are user-programmable digital filter sections with coefficients stored in the coefficient RAM. The B, X, and GX filters can also be operated from an alternate set of default coefficients stored in ROM. See *60/61h Write/Read Operating Functions*, on page 77..

The first high-pass filter is for DC rejection, and the second high pass and notch filters reject low frequencies such as 50 Hz or 60 Hz. In wideband mode, the second high pass and notch filters are bypassed as shown in Figure 13, *Voice Signal Processing Block Diagram*, on page 21. All of these filters may be disabled with the DHP bit in command *70/71h Write/Read Operating Conditions*, on page 79.

### Receive Signal Processing

In the receive path (D/A), the digital signal is expanded (for A-law or µ-law), filtered, interpolated, converted to analog, and driven onto the TIPD and RINGD pins by the high voltage line driver. The DRL, DISN, Z, R, and GR blocks are user-programmable filter sections with their coefficients stored in the coefficient RAM, while AR is an analog amplifier. The Z, R, GR and RI filters can also be operated from an alternate set of default coefficients stored in ROM. See *60/61h Write/Read Operating Functions*, on page 77..

### Programmable Filters

The filter coefficients that the user sends to the voice ALU are in a form known as Canonical Signed Digits (CSDs). The coefficients take the following general form:

$$h = I0 + C1 \bullet 2^{-m1} \bullet (1 + C2 \bullet 2^{-m2} \bullet (1 + I3 \bullet C3 \bullet 2^{-m3} \bullet (1 + I4 \bullet C4 \bullet 2^{-m4})))$$

where: Cj = –1 or +1 (represented as 1 or 0 in user programming)

mj = 0, 1, 2,... or 7 (user programming)

I0 = 1 for GX; I0 = 0 for all other coefficients

I4 = 1 for 4 • CSD coefficients; I4 = 0 otherwise

I3 = 1 for 3 and 4 CSD coefficients; I3 = 0 for 2 CSD coefficients

### Calculating Coefficients with WinSLAC™ Software

The WinSLAC™ software is a program that models the VE8820 chipset, the line conditions, and the external VoicePort components to calculate the coefficients of the programmable filters and predict important transmission performance plots.

The following parameters relating to the desired line conditions and the external components are provided as input to the program:

- Line impedance or the balance impedance of the line is specified by the local telephone system.
- Desired two-wire impedance that is to appear at the line card terminals of the exchange.
- Tabular data for templates describing the frequency response or attenuation distortion limits of the design.
- Relative analog signal levels for both the transmit and receive two-wire signals.
- Component values for the analog portion of the VoicePort.
- Two-wire return loss template that is usually specified by the local telephone system.
- Four-wire return loss template that is usually specified by the local telephone system.

The output from the WinSLAC program includes the coefficients of the AR, AX, DRL, DISN, GR, GX, Z, R, X, and B filters as well as transmission performance plots of stability, input impedance, two-wire return loss, receive and transmit path frequency responses, and four-wire return loss.

The coefficients are formatted in a way that allows easy integration with the VoicePath API software or VP Script demonstration software.

### Speech Coding

The A/D and D/A conversion follows either the A-law or the µ-law standard as defined in ITU-T Recommendation G.711. A-law or µ-law operation is programmed using command *60/61h Write/Read Operating Functions*, on page 77. Alternate bit inversion is performed as part of the A-law coding. In PCM/MPI mode linear code is an option on both the transmit and receive sides of the chipset. Linear code is also selected using Command 60/61h. Two successive time slots are required for linear code operation. The linear code is a 16-bit two's-complement number which appears sign bit first on the PCM highway.

### Wideband Codec Mode

The VE8820 chipset can be operated in a Wideband mode when using the PCM/MPI control option. GCI does not support wideband mode. The wideband mode is selected with the WBAND bit in command *4A/4Bh Write/Read Channel Enable and Operating Mode Register*, on page 71 and it affects both channels of the chipset. In this mode, the nominal voice bandwidth is doubled to 300Hz to 7000Hz to provide better voice quality. In this mode, internal clocks are doubled, increasing the sampling rates of the internal digital filters. One stage of interpolation and decimation is skipped so that the DSP data can be sent to the A/D converter, and part of the transmit high pass filter and notch filter are disabled. The coefficients of the VE8820 must be reprogrammed from the nominal values in Wideband mode. In this mode the increased data rate is processed by accessing a second set of timeslots equally spaced in the frame. Linear data should be used in the Wideband mode.

### Voice Path Test States and Operating Conditions (per channel)

The VE8820 chipset supports testing by providing test states and special operating conditions as shown in Figure 13, *Voice Signal Processing Block Diagram*, on page 21 (see *70/71h Write/Read Operating Conditions*, on page 79).

**Cutoff Transmit Path (CTP):** When CTP = 1, DXA and $\overline{\text{TSCA}}$ are high impedance and the transmit time slot does not exist. This state takes precedence over the Interface Loopback (ILB).

**Cutoff Receive Path (CRP):** When CRP = 1, the receive signal is forced to 0 just ahead of the low pass filter (LPF) block. This state blocks the 1 kHz receive tone (TON). The signal generators can still be used to send signals in the receive path.

**High Pass Filter disable (HPF):** When HPF = 1, all of the high pass and notch filters in the transmit path are disabled.

**Lower Receive Gain (LRG):** When LRG = 1, an extra 6.02 dB of digital loss is inserted into the receive path.

**Interface Loopback (ILB):** When ILB = 1, data from the TSA receive time slot is looped back to the TSA transmit time slot. Any other data in the transmit path is overwritten.

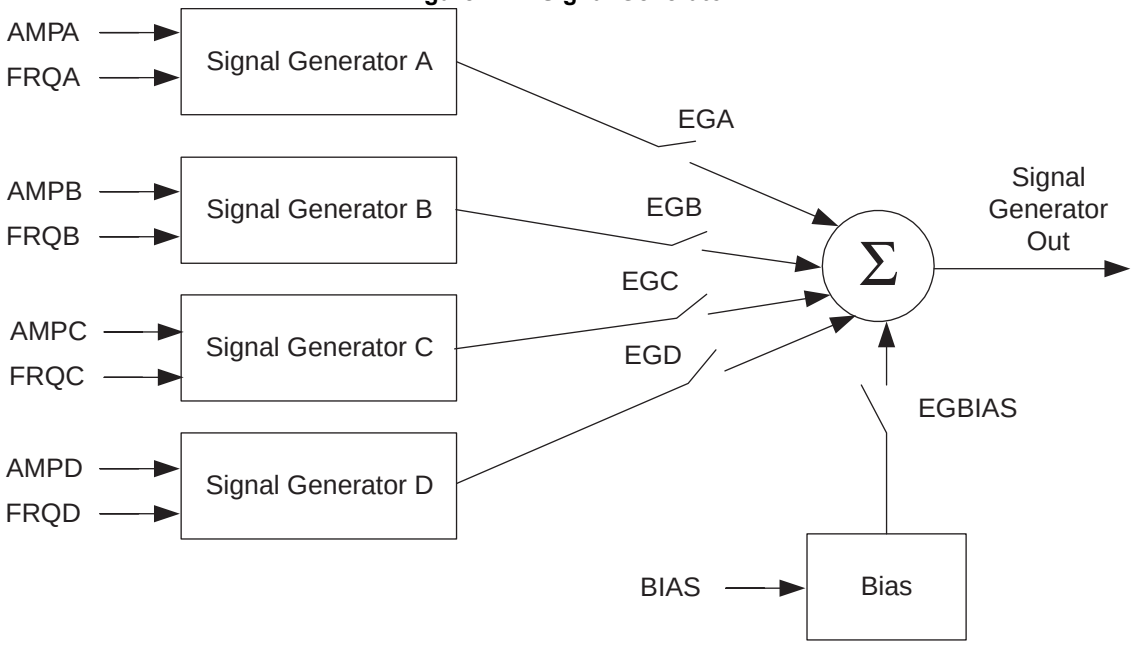
**1 kHz Receive Tone (TON):** When TON = 1, a 1 kHz "digital milliwatt" (2 kHz in Wideband mode) is injected into the receive path, replacing any receive signal from the TSA.

## Signal Generation and Cadence Control

Up to five digital signal generators are available for each channel (see Figure 14) that are summed into the receive path, as shown in Figure 13. They are configured with commands *D2/D3h Write/Read Signal Generator A, B and Bias Parameters.*, on page 91 and *D4/D5h Write/Read Signal Generator C and D Parameters.*, on page 93 and controlled with command *DE/DFh Write/Read Signal Generator Control*, on page 94 in combination with the cadencer configuration in *E0/E1h Write/Read Cadence Timer*, on page 95.

The Bias generator produces a DC bias that can be used to provide DC offset during ringing or DC test signals during diagnostic tests. This generator is automatically enabled when entering the ringing state.

**Figure 14. Signal Generator**




Signal Generator A is used for ringing signal generation and is automatically enabled when entering the ringing state. It can produce sinusoidal or trapezoidal signals. When generating a trapezoid, Signal Generator B is not available and some of its parameters are used to configure the trapezoid. For more details on trapezoidal ringing, see the Trapezoidal Ringing Application Note (Document ID #081476).

In addition, Signal Generator A can be used with the Bias Generator to produce slow ramps. This allows a complex sequence of diagnostic test voltages to be generated in a controlled manner without generating unwanted transients on the line.

When available, Signal Generator B produces a programmable sine wave and can be used for call progress tone generation.

Signal generators C and D are also used for call progress tone generation, DTMF generation and can be configured for FSK based Caller ID generation in combination with command *EA/EBh Write/Read Caller Identification Number Parameters*, on page 99.

Each generator has independent frequency and amplitude parameters. The frequency accuracy is basically the same as the crystal accuracy of the system. The amplitude accuracy and spectral purity are limited only by the voice DAC.

### Cadencing

The signal generator may be sequenced with an on and off time controlled by the user. This feature allows the VE8820 chipset to automatically cadence the ringing bursts. The cadence function can also be used to control the general purpose signal generator during the Active state to send call progress or other specialized tones. Additionally, the sequencer may be used as a general purpose timer/counter which can send interrupts to the user's micro controller after timing out events.

The cadencer has 5 ms resolution, with a maximum on time of 10.24 s and a maximum off time of 10.24 s. *See E0/E1h Write/Read Cadence Timer*, on page 95.. It is enabled with the SGCAD bit in command *DE/DFh Write/Read Signal Generator Control*, on page 94. The CAD bit in the Signalling register is set at the end of the on period, and this event can generate an interrupt if the bit is unmasked.

### Calling Number Identification (CID)

The CID block uses tone generators C and D for each channel to generate phase continuous 1200 baud FSK tones for on or off hook data transmission such as caller ID information. The duration of each (bit) tone is fixed at 0.833 ms (1200 baud).

When the CID bit is 0 (space), the transmitted tone is from signal generator C.

When the CID bit is 1 (mark), the transmitted tone is from signal generator D.

The typical configurations for signal generators C and D when used for CID is shown in Table .

The GR-30 frequencies are used in the US market, and the V.23 frequencies are used in most other international markets. The signal generator amplitude may need to be adjusted depending on the programmed loss plan. Data transmission levels are normally specified as -13.5 dBm +/-1.5 dB. The default amplitude of -7 dBm0 can be used if the programmed receive relative level is -6 or -7 dBr. The amplitudes of AMPC and AMPD are normally set equal, and the dBm0 level from the generator is given by:

$$AC(dBm0) = 20 \cdot \log\left(\frac{|AMPCd|}{22827}\right)$$

$$AD(dBm0) = 20 \cdot \log\left(\frac{|AMPDd|}{22827}\right)$$

The programmed parameters FRQC and FRQD can be determined with the following equations:

$$FRQCh = (FC \bullet 2.73)h$$

$$FRQDh = (FD \bullet 2.73)h$$

From the CID block point of view, once generators C and D have been programmed, the CID generation is configured and can be monitored using command *EA/EBh Write/Read Caller Identification Number Parameters*, on page 99 which allows control of framing, end of message, and disabling the block. Information to be transmitted is received from the MPI as a string of characters using command *E2/E3h Write/Read Caller Identification Number Data*, on page 95, which is a 2 byte deep buffer, allowing a 10 ms polling rate to support the real time requirements. Each character is 8 bits wide, and is assumed to include appropriate parity information according to the character set being used. If framing is enabled, for each character, the CID block first transmits a start bit, then it serially transmits the 8-bit character, LSB first, followed by a stop bit, giving a total of 10 bits sent for each character. The CID block sets the CID bit in the signaling register whenever it needs data to transmit, and this can generate an interrupt if the bit is unmasked.

### CID Tone Programming

| Parameter | Number of Bits | Value | Description |
|---|---|---|---|
| FRQC | 14 | 1777h | 2200 Hz GR30 space frequency (Default) |
| FRQC | 14 | 1666h | 2100 Hz ITU V.23 space frequency |
| AMPC | 15 | 27D4h | -7 dBm0 level (Default) |
| FRQD | 14 | 0CCDh | 1200 Hz GR30 mark frequency (Default) |
| FRQD | 14 | 0DDEh | 1300 Hz ITU V.23 mark frequency |
| AMPD | 15 | 27D4h | -7 dBm0 level (Default) |

Exact preamble and mark sequences can be generated by adjusting the framing mode and sending the appropriate number of characters.

The VoicePath API-II supports this mechanism along with a software programmable sequencer that enables any worldwide Caller ID protocol to be supported. The complex signalling sequences are defined using the Profile Wizard, and a number of pre-defined sequences for various markets are included in the API-II package.

## Signaling Control

The Signaling Control blocks handle the System State and performs the related control functions such as DC feed, metering and ringing generation and line test for each channel. The System State register has a 4-bit System State field and three state modifier bits, POLNR, ACT and METR (see command *56/57h Write/Read System State*, on page 75). All channel specific control requires that the *4A/4Bh Write/Read Channel Enable and Operating Mode Register*, on page 71 select the channel to be accessed.

Nine system states are possible for the VE8820 chipset: Shutdown, Disconnect, Idle, Active, Tip Open, Ring Open, Balanced Ringing, Unbalanced Ringing, and Low Gain.

### Shutdown

Shutdown is the power-up and hardware reset state of the chipset. When the System State register is in Shutdown, the voice channel is deactivated (ACT = 0) and the switching regulators are off. Once the correct clocks have been programmed and the chipset registers initialized, writing disconnect to *56/57h Write/Read System State*, on page 75 places the chipset in the normal disconnect state and enables the switching regulators from which other state transitions can occur.

### Disconnect

In the Disconnect state, the high voltage line drivers are shut off providing a high impedance to the line. This state can be used for denial of service. The switching regulators are active and output the programmed SWYV floor voltage. In order to ensure smooth transition from the Disconnect state to the Idle or Active states, the following byte sequences should be written on entering and exiting Disconnect state immediately after the system state register is written.

```
EC0F080000EEC0400C0C          ;# enable CHL VREF bias on entry to Disconnect state
EC00000000EE00000C0C          ;# disable CHL VREF bias when exiting Disconnect state
```

The voice channel and associated analog circuitry is normally deactivated, but can be activated and used with the converter configuration command to monitor the voltages on Tip or Ring for line diagnostics by setting the ACT bit in the system state register and sending the following byte sequence to the channel:

```
EE0C0C0C0CF401010000F220200000    ;# enable line voltage sensing via codec transmit path
EEC0400C0CF400000000F200000000    ;# disable line voltage sensing via codec transmit path
```

Converter configuration register must be written appropriately along with other codec settings to measure the selected voltage.

### Low Power Idle

The Low Power Idle state is used when on hook. In this state, the DC feed is active and hook and ground key supervision functions are operating. The loop feed polarity is controlled by the POLNR bit. The high voltage switching regulator only generates the voltage needed to support the DC line voltage defined by the DC feed. Voice transmission is disabled to minimize power dissipation.

Even with the special configuration described under the Disconnect state, the Disconnect to Idle state transition can generate spurious off hook interrupts even into an open circuit. If the line has significant capacitance to charge, this off hook event can last a significant time. These hook events can be minimized if the state transition sequence is Disconnect to Active to Idle.

### Active

The Active state is used when off hook or for on hook transmission (OHT) such as CID. In this state the DC feed is activated and voice transmission is controlled by the ACT bit. Metering signals can be generated in this state using the METR bit. The loop feed polarity is controlled by the POLNR bit. Hook and ground key supervision functions are operating. The high voltage switching regulator only generates the voltage needed to support the DC line voltage defined by the DC feed. In this way, power dissipation is minimized.

### Tip Open

In the Tip Open state, the VE8820 chipset provides a high impedance on the Tip lead and drives the Ring lead to the programmed VOC voltage. The loop supervision detector monitors the Ring current. When this current is larger than the programmed threshold, the HOOK bit is set which reports a ground start event. An automatic state transition to the Active state can be enabled to occur upon a ground start detection. A separate application note on VoicePort Ground Start Procedures (Document ID #081344) provides more details of the necessary call control sequences if ground start support is needed.

### Ring Open

In the Ring Open state, the VE8820 chipset provides a high impedance on the Ring lead and drives the Tip lead to the programmed VOC voltage.

### DC Feed

DC feed is active in the Idle, Active and Tip and Ring Open states. The parameters that control DC feed are summarized in Table and programmed in *C6/C7h Write/Read DC Feed Parameters*, on page 87. The Idle and Active feed characteristics appear between Tip and Ring, while the feed characteristic appears from Ring to ground in the Tip Open state, and from Tip to ground in the Ring Open state.

The DC feed parameters produce a DC feed curve at Tip and Ring as shown in Figure 15 when the fuse resistors are inside the feedback loop formed by the RTDC, RRDC feedback network.

The normal polarity ILA setting must be calibrated by software to meet the data sheet specification.
VOC calibration is also required to meet the open circuit voltage specification, and includes some special register configuration depending on the selected VOC voltage.

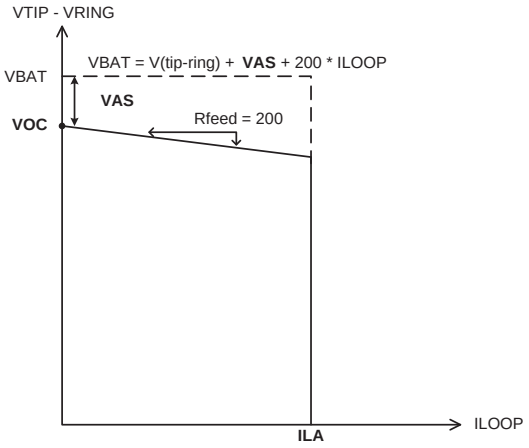
if VOC >= 51V write `EE00000C0CF200004040FAAAB0`
if VOC <= 48V write `EE00000C0CF210000000FAAAB0`

VAS should also be calibrated for optimum performance and to meet the data sheet power specifications. VAS should be set to 14.25 V if calibration is not used. VP API-II includes recommended calibration procedures for these parameters.

### DC Feed Programmable Parameters

| Parameter | Number of Bits | Range | Description |
|---|---|---|---|
| ILA | 5 | 20 - 45 mA | Sets the current limit for DC feed |
| VOC | 3 | 12 - 57 V | Sets open circuit DC feed voltage.<br>Two ranges, 12 - 33 V and 36 - 57 V provided by VOCSFT bit |
| VAS | 4 | 3 – 14.25 V | Sets the overhead voltage between the tracking regulator and the DC feed voltage |

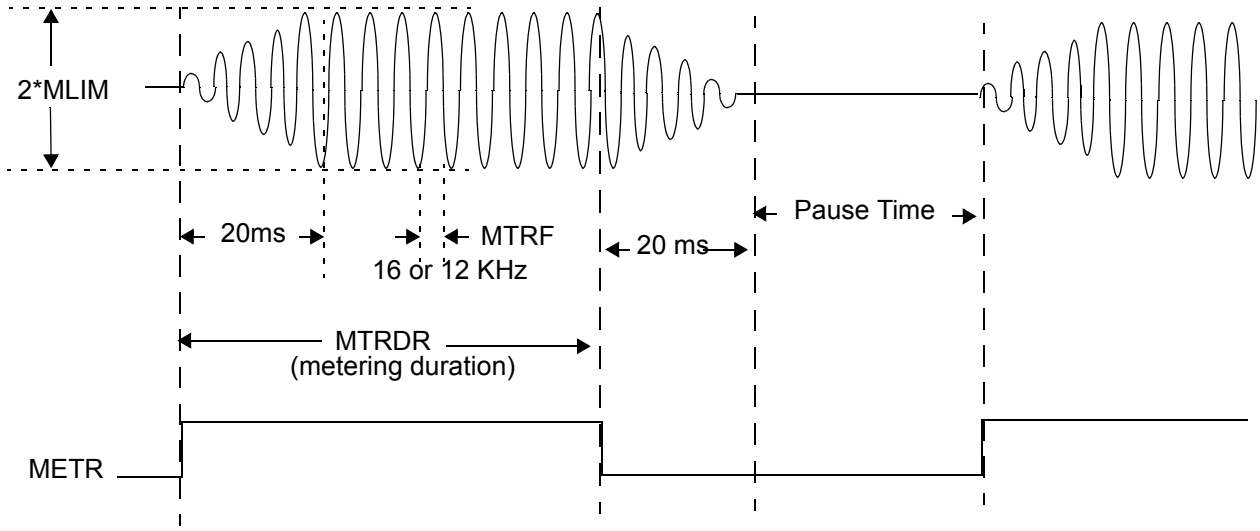
**Figure 15. DC Feed I / V Characteristic**



## Metering

The VE8820 chipset is capable of 0.5 Vrms metering into a 200-Ω metering load at either 12 kHz or 16 kHz. Smooth metering application and abrupt metering application are supported. A typical metering sequence is shown in Figure 16.

**Figure 16. Metering Pulse Definitions**




The duration of the metering pulses may be programmed by the user via the MTRDR parameter. This off loads much of the timing from the user's micro controller. Table lists the programmable metering parameters which are accessed either in command *D0/D1h Write/Read Metering Parameters*, on page 90 or command *56/57h Write/Read System State*, on page 75.

### Metering Programmable Parameters

| Parameter | Number of Bits | Range | Description |
|---|---|---|---|
| METR | 1 | 0, 1 | "1" starts a metering pulse. |
| MTRF | 1 | 0, 1 | Metering frequency.<br>"1" is for 16 khz. "0" is for 12 khz (default). |
| MLIM | 7 | 0 - 1.9 V<br>0 - 2.3 V | RMS limit voltage of 12 kHz metering signal sensed at tip-ring<br>RMS limit voltage of 16 kHz metering signal sensed at tip-ring |
| SOREV | 1 | 0, 1 | Controls the ramping of the metering signal.<br>"1" abrupt ramping. "0" smooth ramping (default). |
| MTRSL | 7 | 0 - 8.636 mA | RMS output current of the ramped metering signal with TIPD-RINGD short circuit |
| MTRDR | 8 | 2.5 - 637.5 ms | Metering duration. From 2.5 to 637.5 ms with step size of 2.5ms<br>0 produces continuous metering |
| MTRPK | 8 | 0 - 2 V | Peak voltage of metering signal at AC sense point (read only) |

## Ringing

In this state, the voice DAC is used to apply the ringing signal generated from Signal Generator A and the Bias generator to the high voltage line driver. Internal feedback maintains a low (200-Ω) system output impedance during ringing. The current limit is increased in the Ringing state and is programmable via the parameter, ILR in register *C2/C3h Write/Read Loop Supervision Parameters*, on page 87. In order to minimize line transients, entry and exit from the Ringing states are intelligently managed by the VE8820 chipset. When ringing is requested by the user, the signal generator is started but not applied to the subscriber line until the ringing voltage is equal to the on-hook Tip-Ring voltage. This algorithm, known as *Ring Entry*, assures that there is a smooth line transition when entering ringing. Ring entry is guaranteed to occur within one period of the programmed ringing frequency. Ring Exit is an analogous procedure whereby the ringing signal is not immediately removed from the line after a ring trip or new state request. The ringing signal will persist until its voltage is equal to the required line voltage.

While in Ringing, the integrated switching regulator may be programmed to behave in one of two ways, tracking or fixed. In tracking mode, the switching regulator will generate just enough voltage to support the instantaneous ringing voltage. In fixed regulator mode, the switching regulator will generate a fixed user-programmed voltage.

### *Balanced Ringing*

Internal balanced ringing drives the subscriber line with balanced ringing voltage waveforms (see Figure 17). The VE8820 chipset can be programmed to output either sinusoidal or trapezoidal ringing waveforms. The ringing amplitude, frequency, and DC bias is also programmable in register *D2/D3h Write/Read Signal Generator A, B and Bias Parameters.*, on page 91. In the balanced ringing mode, the ringing signal is driven differentially, thus maximizing the ringing signal swing. The DC bias parameter should always be programmed as a positive value. This will normally generate a negative bias between TIP and RING, and a positive bias can be generated if the POLNR bit is set in *56/57h Write/Read System State*, on page 75. The switching regulator may be programmed to track the ringing waveform envelope (see Figure 18), or to rise to a preset programmable fixed high voltage (see Figure 17). When in the balanced ringing mode, the VE8820 chipset appears to the subscriber line as a voltage source with an output impedance of 200Ω and is capable of 140-V peak ringing in balanced mode (Maximum AC plus DC ringing voltage).

**Figure 17. Balanced Ringing with Fixed Supply**

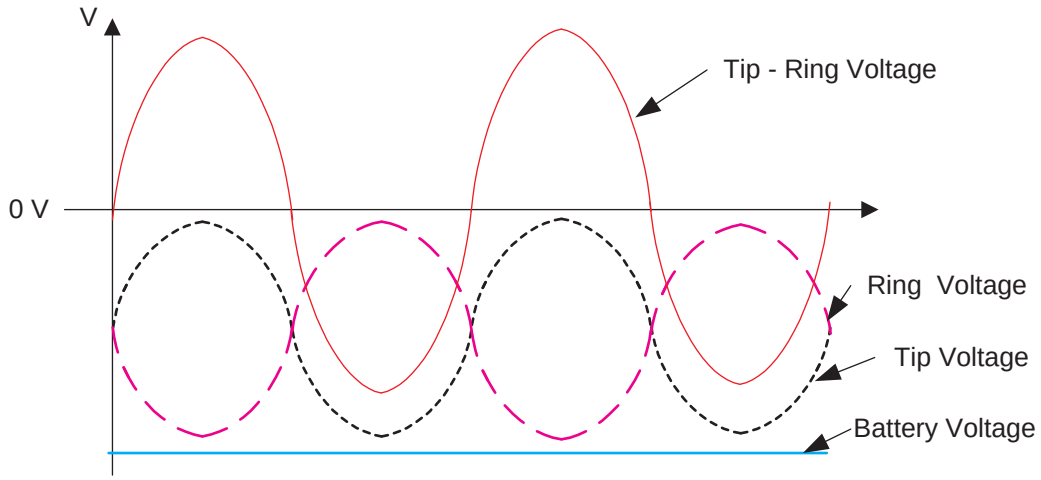
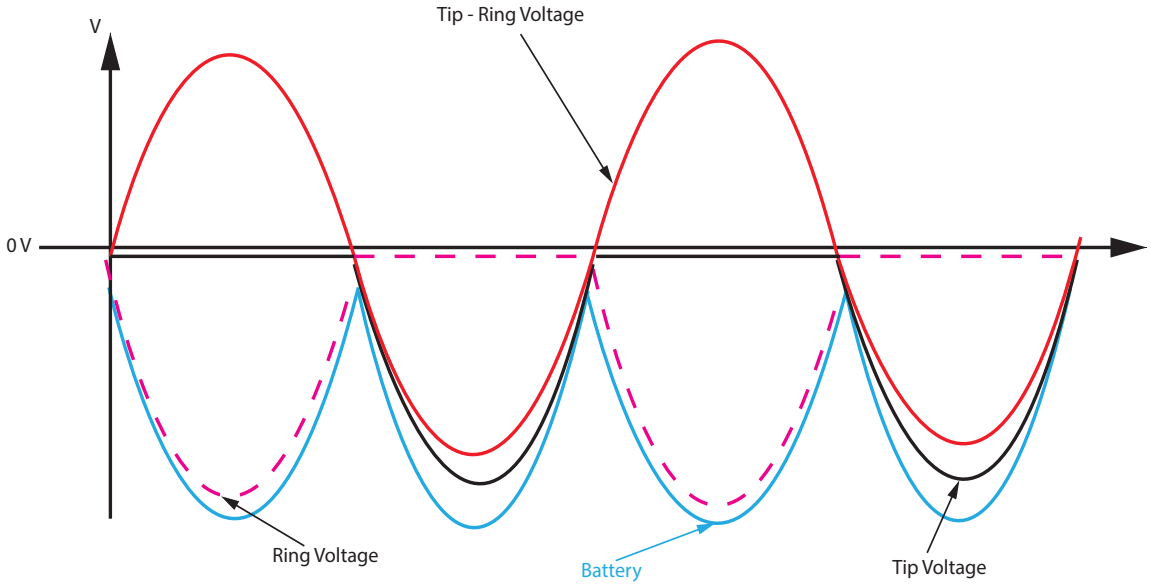



**Figure 18. Balanced Ringing with Tracking Supply**



### *Unbalanced Ringing*

Unbalanced ringing holds the TIPD output to a voltage close to ground while applying the ringing in a single ended fashion to the ring lead (see Figure 19). When in the unbalanced ringing mode, the VE8820 chipset appears to the subscriber line as a voltage source with an output impedance of 200 Ω. The VE8820 chipset is capable of 70-V peak AC ringing in unbalanced mode with a 70-V DC offset. Setting the POLNR bit in the System State register allows the ringing signal to be applied on the TIP lead while RING is held near ground.

**Figure 19. Unbalanced Ringing with Fixed Supply**

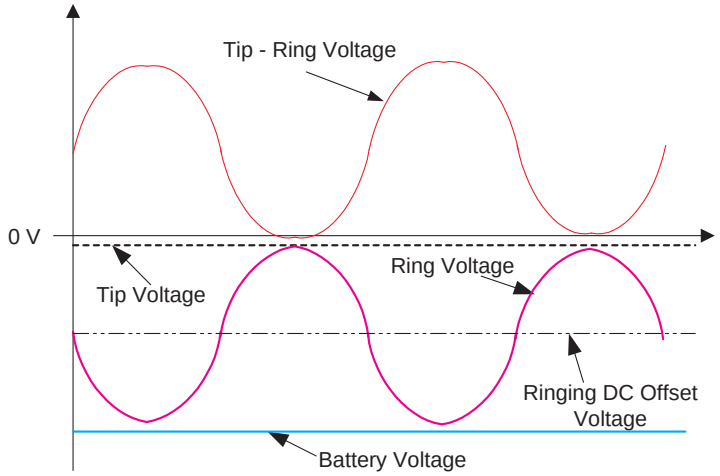
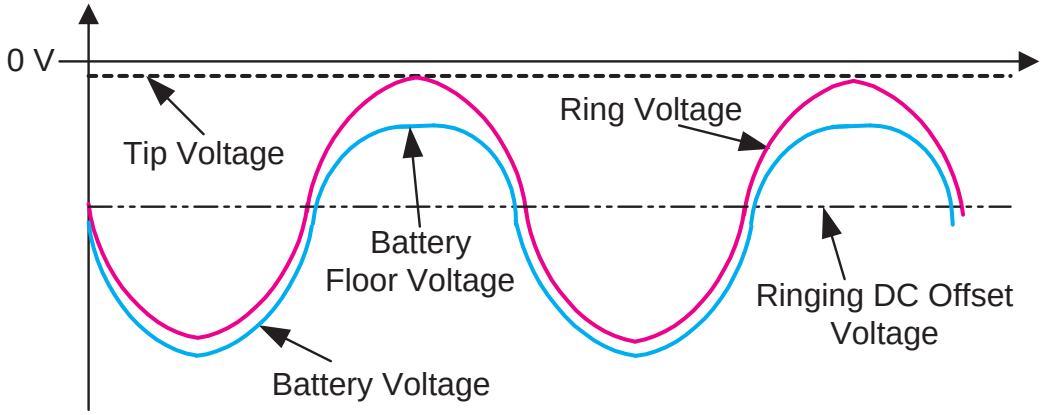



**Figure 20. Unbalanced Ringing with Tracking Supply**




### Ringing Cadencing

The on-chip cadencer is available to automate the cadencing of the ringing signal. When this feature is used, ring entry and exit are smooth when the ZXR bit in *68/69h Write/Read System State Configuration,* on page 78 is 0.

If the system provides control for the cadence, then the system state used between ringing bursts should be the Idle (no voice transmission) or Active VBM states.

### Low Gain

The Low Gain state reduces the gain of the external Le88830 SLIC device. This special mode increases the accuracy of certain line diagnostic measurements, in particular leakage tests. This is used by the VeriVoice software package to deliver line diagnostics in line with requirements described in GR-909.

## Supervision Processing

The programmable supervision parameters are accessed using register *C2/C3h Write/Read Loop Supervision Parameters*, on page 87.

### Switch Hook Detection

The supervision circuits of the VE8820 chipset provides de-bounced off-hook indications to an external processor via the MPI for each channel. The supervision circuit compares a scaled version of the Tip-Ring current to a programmed off-hook threshold, TSH. The output of the comparator is debounced by a programmable debounce timer, DSH. The debounce time should not be programmed less than 6 ms. A change in hook state can generate an interrupt to the user's micro-controller depending on the interrupt mask register.

In addition, if the TDIM bit in the *5E/5Fh Write/Read Device Mode Register*, on page 76 is set, the status of the Hook bit is saved in *CFh Read Test Data Buffer*, on page 89 at a rate defined by the DRAT field in the *A6/A7h Write/Read Converter Configuration*, on page 85. Up to 6 samples are stored for each channel. If DRAT is configured for 500 Hz, the buffer will support 2 ms resolution for dial pulse measurement even with a system polling rate of only 10 ms. Use of this feature is directly supported by the VP API-II.

### Ground Key Detection

A separate detector is provided for ground key detection for each channel. This detector is similar to the supervision detector and monitors a scaled version of the longitudinal drive current. The scaled longitudinal drive current is compared to a ground key threshold, TGK to determine the existence of a ground key. The output of the comparator is debounced by a programmable debounce timer, DGK. The debounce time should not be programmed less than 4 ms. A change in ground key state can generate an interrupt to the user's micro-controller depending on the interrupt mask register.

### Programmable Supervision Parameters

| Parameter | Number of Bits | Range | Description |
|---|---|---|---|
| TSH | 3 | 8 - 15 mA | Sets the threshold for supervision detector. |
| DSH | 5 | 6 - 62 ms | Sets the debounce time for the supervision detector |
| TGK | 3 | 0 - 42 mA | Sets the threshold for ground key detector. |
| DGK | 5 | 4 - 28 ms | Sets the debounce time for the ground key detector |

### Ring Trip Detection

The ring trip detection circuit for each channel provides de-bounced ring trip indications to an external processor via the MPI. The Ring Trip circuit compares a scaled version of the Tip-Ring current to a programmed Ring Trip Threshold, RTTH. The output of the comparator is processed by the ring trip algorithm on a cycle by cycle basis to provide immunity to false ring trips and filter transients common to ringing and ring trip. In addition, more than 50% of the time near ringing current limit will generate a trip indication. A positive Ring Trip occurs if a trip indication is present for two complete ring cycles, and an interrupt can be raised to the user's micro-controller.

The chipset default configuration is for AC only sinusoidal ringing capable of driving 5 REN ringing loads and a 750 Ω total loop resistance. The following equations can be used to select new ring trip settings when using different ringing waveforms and different loads. They allow the ratio of the open circuit ringing voltage to the ringing threshold current to vary by +/-20%, which is conservative.

### Ring Trip Parameters

| Name | Description |
|---|---|
| AMPA | Amplitude of signal generator A which is used for ringing. |
| FREQA | Frequency of signal generator A which is used for ringing. |
| BIAS | DC bias for ringing. |
| RTDCAC | Ringing trip based on AC only or Battery Backed (DC) Ringing |
| RTTH | Ringing trip threshold in 0.5 mA steps from 0 to 63.5 mA |
| ILR | Ringing current limit programmed in 2 mA steps. ILR=0 represents 50 mA. ILR = 31 represents 112 mA |
| HOOK | Interrupt in signalling register indicating a ring trip occurred. |

For AC only ringing, RTDCAC is 1 and the ringing current is half-wave rectified and averaged over a ringing cycle. If this result exceeds the RTTH threshold for two successive cycles, the HOOK bit will be set. This method limits the supported loop length depending on the minimum must not trip ringing impedance (Rmnt in Ohms) and allowing for errors in the applied ringing voltage and trip level. The maximum loop resistance is given by:

$$RLOOP(max) = 0.67 \cdot Rmnt - Rphone - 66 \cdot \Omega$$

RLOOP(max) excludes the DC resistance of the phone (Rphone, typically 430 Ω in the U.S.), and the fuse resistance if DC line sensing is behind the fuse resistors.

For a sinusoidal ringing waveform of VRING rms volts, and Rmnt impedance, the following ring trip settings should be used:

$$RTTH = \frac{0.54 \cdot VRING}{Rmnt + 200 \cdot \Omega}$$

$$ILR = \frac{1.4 \cdot VRING}{Rmnt + 200 \cdot \Omega}$$

In the case of battery backed ringing where ring trip is based on the DC ringing current, RTDCAC is 0 and the ringing current is averaged over each ringing cycle. If this result exceeds the RTTH threshold for two successive cycles, the HOOK bit will be set. In this case the loop length is limited by the ability to deliver the required AC ringing voltage at the end of the loop (VPHONE, typically 40vrms in the U.S.) to the must not trip ringing load (Rmnt) for a given open loop ringing voltage, VRING.

$$RLOOP(max) = Rmnt \cdot \left(\frac{0.9 \cdot VRING - VPHONE}{VPHONE}\right) - 200 \cdot \Omega$$

For reliable ring trip, the ringing DC bias (VRINGDC) should be greater than 20V, and the following ring trip settings should be used:

$$RTTH = \frac{0.8 \cdot VRINGDC}{RLOOP(max) + RPHONE + 200 \cdot \Omega}$$

$$ILR = \frac{1.4 \cdot VRING}{Rmnt + 200 \cdot \Omega}$$

Note that the ringing source impedance is nominally 200 Ω.

## Analog Reference Circuits

The analog reference circuit generates a reference voltage and reference current for use by both channels. The reference current is generated through the external resistor RREF and the external capacitor, CREF, provides filtering on the reference voltage. Copies of the reference voltage are generated on the VREFS pins and connect to the corresponding SLIC channel.

## Switching Regulator Controllers

The switching regulator controller and the external power train circuitry provide a flexible switching regulator that automatically produces the negative supply voltage required for each channel of the Le88830 dual SLIC device to drive the line.

The recommended fly back application circuit is shown in Figure 45, *VE8820 Switching Regulator Circuit*, on page 65.

The variable output switching regulator is used to generate the $V_{BAT}$ supply voltage on a per line basis. An offset voltage (set by the VAS DC feed parameter) is added to the measured Tip-Ring voltage when on hook and the resulting signal controls the output of the switching regulator. When loop current is drawn in the Active or Ringing states, an additional offset defined as 200 * Iloop is added, to ensure overhead is maintained with up to 150 Ohms of total fuse resistance present in the DC feed loop. This architecture enables the switching regulator output voltage to generate the required voltage to feed the line whether in the on-hook, off-hook or ringing states. The result is maximum power efficiency and minimum power dissipation in all states because the regulator output is always optimum for the current state.

In addition, the regulator has two modes when a fixed output is generated. The first is the Floor Voltage, which limits how low the power supply will drop when driving very short loops. Typically this is set to -25 V to ensure compatibility with call waiting caller ID equipment that performs a momentary extension check (MEC). The second fixed output can be generated in fixed ringing voltage mode if dynamic tracking of the ringing waveform is not needed for efficiency or power dissipation reasons. In this case the power supply ramps up to a pre-programmed voltage that is sufficient to support the programmed ringing waveform just before entering the ringing state. These voltages are set in the *E4/E5h Write/Read Switching Regulator Parameters*, on page 96, and should be calibrated by the API-II software VpCalLine() function using the *E8/E9h Write/Read Battery Calibration Register*, on page 98.

The switching regulator has three modes of operation: Low, Medium, and High, which roughly correspond with On-Hook, Off-Hook, and Ringing states. These modes of operation provide for increased efficiency over a wide load range. In Low power mode the switcher operates at 48kHz, which produces maximum efficiency in the idle condition while providing up to one watt of output power capability. In Medium power mode the switching frequency is doubled to 96kHz, providing twice the output power without significant sacrifice of efficiency. High power mode, which is usually of short duration, uses 384kHz and enables the switching regulator to support up to 10 watts of output power. Power modes are normally set by the internal state machine when SWYAP = 0 or Manually through YM bits in E6/E7. Switching regulator parameters that are programmed in *E4/E5h Write/Read Switching Regulator Parameters*, on page 96 and *E6/E7h Write/Read Switching Regulator Control*, on page 97 may control the switching frequency. In addition, the controller detects over current events and terminates the output pulse on a cycle by cycle basis.

### Le88830 Dual SLIC Device

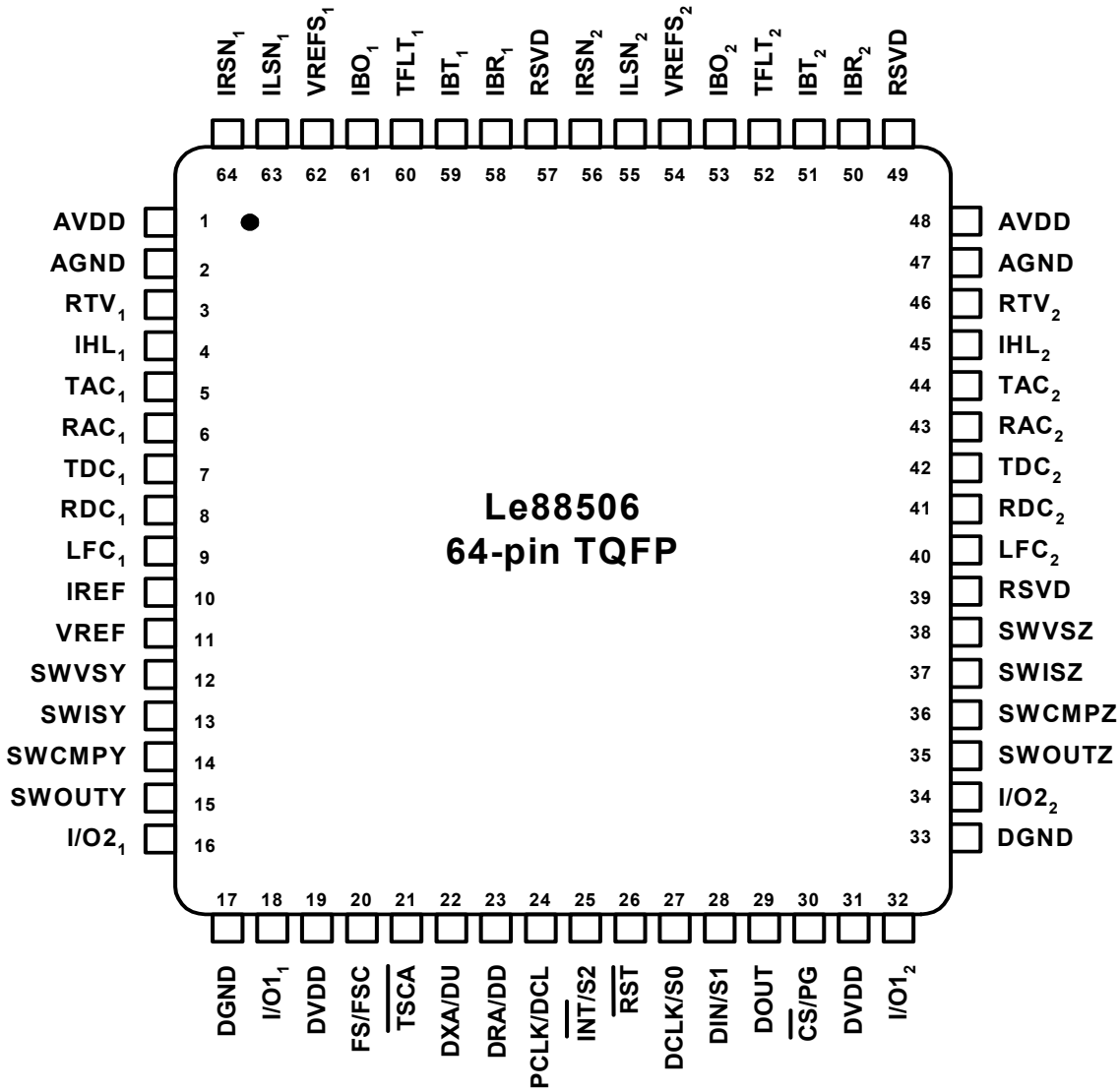
The dual SLIC device interfaces to Tip/Ring and drives all DC and AC signals onto the line, including the ringing signal. The SLIC device is capable of generating a 140 Vpk differential signal. Each channel of the SLIC device is current limited and has integrated thermal shutdown protection.

## CONNECTION DIAGRAMS AND PIN DESCRIPTIONS

The VE8820 Chipset devices are described in the following sections

## Le88506 Connection Diagram and Pin Descriptions

**Figure 21. Le88506 SLAC Device 64-pin TQFP Package**

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### Le88506 SLAC Device Pin Descriptions

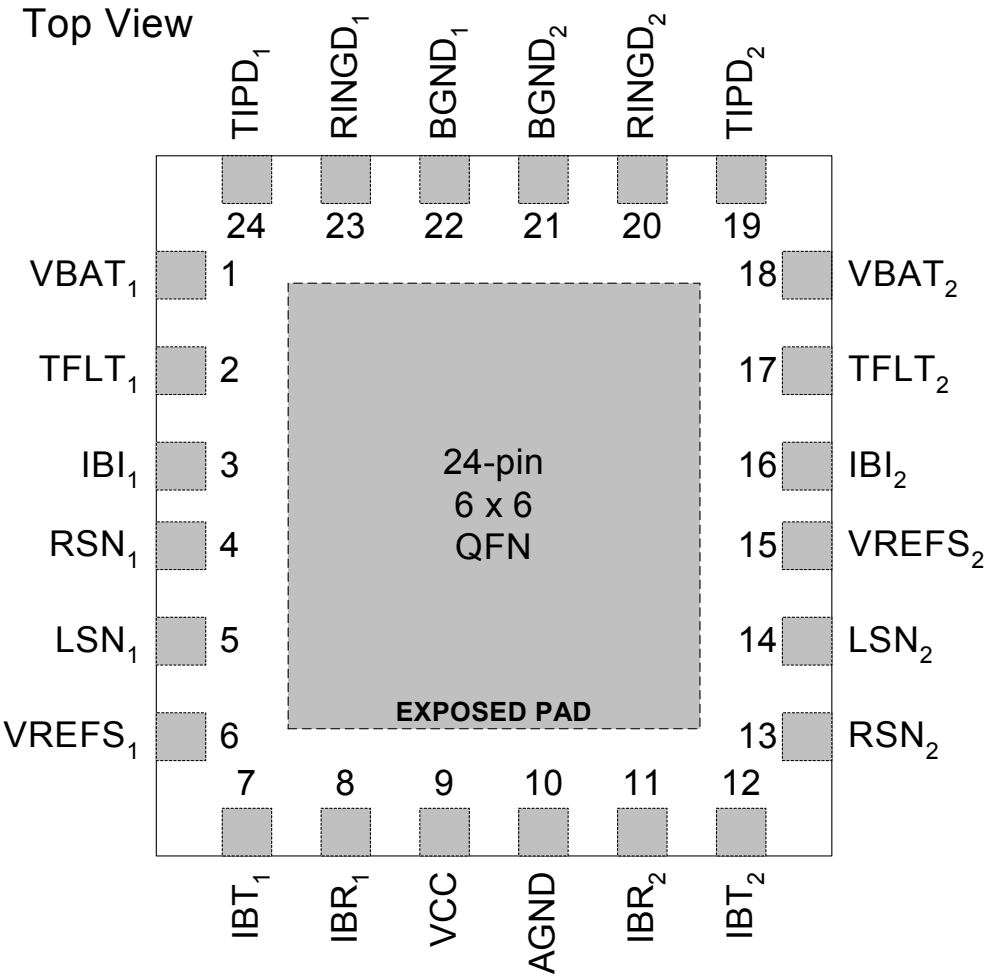
| NAME | Type | Description |
|---|---|---|
| AGND/DGND | Power | Separate analog and digital grounds are provided to allow noise isolation; however, the grounds are connected inside the part, and must also be connected together on the circuit board. |
| AVDD/DVDD | Power | Analog and digital power supply inputs. AVDD and DVDD are provided to allow for noise isolation and proper power supply decoupling techniques. For best performance, all of the VDD power supply pins should be connected together at the power supply or power connection to the printed circuit board. |
| $\overline{CS}$/PG | Input | Chip Select/PCM-GCI. The $\overline{CS}$/PG input along with the DCLK/S0 input are used to determine the operating state of the programmable PCM/GCI interface. On power up, the device will initialize to GCI mode if $\overline{CS}$/PG is low *and* there is no toggling (no high to low or low to high transitions) of the DCLK/S0 input. The device will initialize to the PCM/MPI mode if either $\overline{CS}$ is high *or* DCLK is toggling.<br>Once the device is in PCM/MPI mode, it is ready to receive commands through its serial interface pins, DIN, DOUT and DCLK. Once a valid command has been sent through the MPI serial interface, GCI mode cannot be entered unless a hardware reset is asserted or power is removed from the part. If a valid command has not been sent since the last hardware reset or power up, then GCI mode can be re-entered (after a delay of one PCM frame) by holding $\overline{CS}$/PG low and keeping DCLK static. While the part is in GCI mode, $\overline{CS}$/PG going high or DCLK toggling will immediately place the device in PCM/MPI mode.<br>In the PCM/MPI mode, the Chip Select input (active Low) enables the device so that control data can be written to or read from the part. The device coefficient registers selected by the write or read command must be enabled by writing a 1 to the EC bit in the Channel Enable Register. See the Channel Enable Register and Command 4A/4Bh for more information. If Chip Select is held Low for 16 rising edges of DCLK, a hardware reset is executed when Chip Select returns High. |
| DCLK/S0 | Input | Data Clock. In addition to providing both a data clock input and an S0 GCI address input, DCLK/S0 acts in conjunction with $\overline{CS}$/PG to determine the operational mode of the system interface, PCM/MPI or GCI. See $\overline{CS}$/PG for details. In the PCM/MPI mode, the Data Clock input shifts data into and out of the microprocessor interface of the device. The maximum clock rate is 8.192 MHz. |
| | Input | Packet assignment bit 0. In GCI mode, S0 is one of three inputs (S0, S1, S2) that is decoded to determine in which GCI packet the device transmits and receives data. |
| DIN/S1 | Input | Data Input. In the PCM/MPI mode, control data is serially written into the device via the DIN pin, most significant bit first. The Data Clock determines the data rate. |
| | Input | Packet assignment bit 1. In GCI mode, S1 is one of three inputs (S0, S1, S2) that is decoded to determine in which GCI packet the device transmits and receives data. |
| DOUT | Output | Data Output. In the PCM/MPI mode, control data is serially written from the device via the DOUT pin, most significant bit first. The Data Clock determines the data rate. DOUT is high impedance except when data is being transmitted, which allows DIN and DOUT to be directly tied together in systems which use a single line for data input and output. |
| DRA/DD | Input | PCM Data Receive. In the PCM/MPI mode, the PCM data is serially received on the DRA port during the user-programmed time slot. Data is always received with the most significant bit first. For compressed signals, 1 byte of data is received every 125 µs at the PCLK rate. In the Linear mode, 2 consecutive bytes of data for each channel are received every 125 µs at the PCLK rate. In Wideband mode, the frame sync stays at 8kHz, VoicePort operates internally at 16kHz and outputs data twice per frame in evenly spaced time slots. |
| | Input | GCI Data Downstream. In GCI mode, the B1, B2, Monitor and SC channel data is serially received on the DD input. The device uses one of the eight GCI packets for operation. Which of the 8 GCI packets is determined by the S0, S1 and S2 inputs. Data is always received with the most significant bit first. 4 bytes of data is received every 125 µs at the 2.048 Mbit/s data rate. |
| DXA/DU | Output | PCM Data Transmit. In the PCM/MPI mode, the transmit data is sent serially on the DXA port during the programmed time slot. Data is always transmitted most significant bit first. The output is available every 125 µs and the data is shifted out in 8-bit (16-bit in Linear or PCM Signaling mode) bursts at the PCLK rate. In Wideband mode, the frame sync stays at 8kHz, VoicePort operates internally at 16kHz and outputs data twice per frame in evenly spaced time slots. DXA is high impedance between time slots, while the device is in the Inactive mode with no PCM signaling, or while the Cutoff Transmit Path bit (CTP) is on. |
| | Output | GCI Data Upstream. In the GCI mode, the B1, B2, Monitor and SC channel data is serially transmitted on the DU output. Which GCI packet the device uses is determined by the S0, S1 and S2 inputs. Data is always transmitted with the most significant bit first. 4 bytes of data is transmitted every 125 µs at the 2.048 Mbit/s data rate. |
| FS/FSC | Input | Frame Sync. In the PCM/MPI mode, the Frame Sync (FS) pulse is an 8 kHz signal that identifies Time Slot 0 and Clock Slot 0 of a system's PCM frame. Individual time slots are referenced to this input, which must be synchronized to PCLK. |

| NAME | Type | Description |
|---|---|---|
| FS/FSC | Input | Frame Sync. In GCI mode, the Frame Sync (FSC) pulse is an 8 kHz signal that identifies the beginning of GCI packet 0 of a system's GCI frame. The device can access packets 0 to 7 based on the setting of the S0, S1 and S2 inputs. FSC must be synchronized to DCL. |
| $I/O1_1$,$I/O1_2$ | I/O | General Purpose Input/ Output (Can directly drive a 150 mW 3-V or 5-V relay). |
| $I/O2_1$, $I/O2_2$ | I/O | General Purpose Input/ Output. |
| $IBO_1$, $IBO_2$ | Output | SLIC input stage bias current |
| $IBR_1$, $IBR_2$ | Output | SLIC Ring amplifier bias current |
| $IBT_1$, $IBT_2$ | Output | SLIC Tip amplifier bias current |
| $IHL_1$,$IHL_2$ | Output | High Level Current Drive. |
| $ILSN_1$, $ILSN_2$ | Output | Longitudinal control current to the SLIC longitudinal summing node. |
| $\overline{INT}$/S2 | Output | Interrupt. $\overline{INT}$ is an active Low output signal, which is programmable as either 3V CMOS-compatible or open drain. The $\overline{INT}$ output goes Low any time one of the input bits in the Signaling register changes state and is not masked. It also goes Low any time new transmit data appears if the ATI interrupt is armed. $\overline{INT}$ remains Low until the appropriate register is read via the microprocessor interface, or the device receives either a software or hardware reset. The individual bits in the Signaling register can be masked from causing an interrupt by using MPI Command 6C/6Dh. |
| | Input | Packet assignment bit 2. In GCI mode, S2 is one of three inputs (S0, S1, S2) that is decoded to determine in which GCI packet the device transmits and receives data. |
| IREF | Input | Current Reference. An external resistor $R_{REF}$ connected between this pin and analog ground generates an accurate current reference used by the analog circuits on the chip. |
| $IRSN_1$, $IRSN_2$ | Output | Metallic control current to SLIC receive summing node. |
| $LFC_1$,$LFC_2$ | Output | Connection for longitudinal filter capacitor to Agnd. |
| PCLK/DCL | Input | PCM Clock. The PCM clock determines the rate at which data is serially shifted in and out on the PCM highway and provides the clock reference for the internal PLL. |
| | Input | GCI Data Clock. In GCI mode, DCL is either 2.028 MHz or 4.096 MHz and an integer multiple of the FSC frequency. The internal PLL is automatically configured to run from this clock. |
| $RAC_1$,$RAC_2$ | Input | Ring lead AC sense. A series R + C network is connected from this pin to the Ring lead. The connection can be to either side of the protection resistor. |
| $RDC_1$,$RDC_2$ | Input | Ring lead DC Sense. A resistor is connected from this pin to the Ring lead. The connection can be to either side of the protection resistor. |
| $\overline{RST}$ | Input | Device Hardware Reset. A logic Low signal at this pin resets the device to its default state. |
| RSVD | Open | Reserved. Make no connection to this pin. |
| $RTV_1$, $RTV_2$ | Output | Drive output for two-wire AC impedance scaling resistor. |
| SWCMPY, SWCMPZ | Output | Compensation connection for switching regulator controller. |
| SWISY, SWISZ | Input | Current sense input for switching regulator controller. |
| SWOUTY, SWOUTZ | Output | Pulse output for gate drive to switching regulator FET. |
| SWVSY, SWVSZ | Input | Voltage sense for switching regulator controller. |
| $TAC_1$,$TAC_2$ | Input | Tip lead AC Sense. A series R + C network is connected from this pin to the Tip lead. The connection can be to either side of the protection resistor. |
| $TDC_1$,$TDC_2$ | Input | Tip lead DC Sense. A resistor is connected from this pin to the Tip lead. The connection can be to either side of the protection resistor. |
| $TFLT_1$,$TFLT_2$ | Input | Thermal fault input |
| $\overline{TSCA}$ | Output | Time Slot Control. The Time Slot Control output is open-drain (requiring a pull-up resistor to DVDD) and is normally inactive (high impedance). In the PCM/MPI mode, $\overline{TSCA}$ is active (low) when PCM data is transmitted on the DXA pin. In GCI mode, $\overline{TSCA}$ is active (low) during the GCI packet selected by S0, S1 and S2. |
| VREF | Output | Analog Voltage Reference. The VREF output is provided in order for an external capacitor to be connected from VREF to ground, filtering noise present on the internal voltage reference. VREF is buffered before it is used by internal circuitry. The voltage on VREF and the output resistance are given in *Electrical Characteristics*, on page 40. |

| NAME | Type | Description |
|---|---|---|
| $VREFS_1$,$VREFS_2$ | Output | Analog Voltage Reference for each SLIC channel |

## Le88830 Connection Diagram and Pin Descriptions

**Figure 22. Le88830 Device 24-pin QFN Package**




### Le88830 Dual SLIC Device Pin Descriptions

| NAME | Type | Description |
|---|---|---|
| AGND | Power | Analog Ground. Must be directly connected to BGND. |
| $BGND_1$, $BGND_2$ | Power | Battery Ground for each channel. |
| EXPOSED PAD | Power | Exposed pad substrate connection. This pad is at ground potential and should be soldered to the PCB and connected by multiple vias to a heatsink area on the bottom of the board and to the internal ground plane if present. |
| $IBI_1$, $IBI_2$ | Input | Input stage bias current for each channel |
| $IBR_1$, $IBR_2$ | Input | Ring amplifier bias current for each channel |
| $IBT_1$, $IBT_2$ | Input | Tip amplifier bias current for each channel |
| $LSN_1$,$LSN_2$ | Input | Longitudinal current summing node for each channel |
| $RINGD_1$, $RINGD_2$ | Output | RING-lead (B) driver output to the two-wire line for each channel. |
| $RSN_1$, $RSN_2$ | Input | Receive current summing node for each channel. |

| NAME | Type | Description |
|---|---|---|
| $TFLT_1$,$TFLT_2$ | Output | Thermal Shutdown indicator output for each channel. |
| $TIPD_1$, $TIPD_2$ | Output | TIP-lead (A) driver output to two-wire line for each channel. |
| $VBAT_1$, $VBAT_2$ | Supply | Tracking Negative Battery Supply. Provides power for each SLIC channel in all states. |
| VCC | Power | Analog and digital power supply inputs. |
| $VREFS_1$, $VREFS_2$ | Power | Analog Voltage Reference for each SLIC channel. |

## ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

### Absolute maximum Ratings - Le88506 SLAC Device

| | |
|---|---|
| Storage Temperature | –55° C < $T_A$ < +125° C |
| Ambient Temperature, under Bias | –40° C < $T_A$ < +85° C |
| Ambient relative humidity (non condensing) | 5 to 95% |
| AVDD with respect to AGND | –0.4 V to + 4.0 V |
| AVDD with respect to DVDD | –0.4 V to + 4.0 V |
| DVDD with respect to DGND | –0.4 V to + 4.0 V |
| AGND with respect to DGND | –0.05 V to + 0.05 V |
| Digital pins with respect to DGND | –0.4 V to the smaller of +4.0 V or DVDD + 0.4 V |
| $I/O1_i$ with respect to DGND | –0.4 V to the smaller of +5.5 V or DVDD + 2.37 V |
| $I/O1_i$ current sink to DGND | 70mA |
| Latch up immunity (any pin) | ± 100 mA |
| ESD Immunity (Human Body Model) | JESD22 Class 1C compliant |

### Absolute maximum Ratings - Le88830 SLIC Device

| | |
|---|---|
| Storage Temperature | –55° C < $T_A$ < +125° C |
| Ambient Temperature, under Bias | –40° C < $T_A$ < +85° C |
| Ambient relative humidity (non condensing) | 5 to 95% |
| VCC with respect to AGND | –0.4 V to + 4.0 V |
| BGND with respect to AGND | -0.4 V to +0.4 V |
| $VBAT_i$ with respect to BGND<br>for Le88830 device | <br>-160 V to +0.4 V |
| TIPD, RINGD to BGND:<br>Continuous<br>10 ms (F = 0.1 Hz)<br>1 µs (F = 0.1 Hz)<br>250 ns (F = 0.1 Hz) | <br>$V_{BAT}$ –1 to BGND +1<br>$V_{BAT}$ –5 to BGND +5<br>$V_{BAT}$ –10 to BGND +10<br>$V_{BAT}$ –15 to BGND +15 |
| Current from TIPD or RINGD | ±150 mA |
| Digital pins with respect to DGND | –0.4 V to the smaller of +4.0 V or DVDD + 0.4 V |
| $I/O1_i$ with respect to DGND | –0.4 V to the smaller of +5.5 V or DVDD + 2.37 V |
| $I/O1_i$ current sink to DGND | 70mA |
| Latch up immunity (any pin) | ± 100 mA |
| Maximum power dissipation,<br>$T_A$ = 85° C (See notes) | 1.8 W |
| Thermal Data:<br>In 24-pin QFN package | $\theta_{JA}$<br>30° C/W |
| ESD Immunity (Human Body Model) | JESD22 Class 1C compliant |

### Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane. Thermal performance depends on the number of PCB layers and the size of the copper area. Please refer to Microsemi's *QFN Package* application note, available from http://www.Microsemi.com, for layout and heat sinking guidelines. Continuous operation above 145ºC junction temperature may degrade device reliability. Thermal limiting circuitry on each channel of the Le88830 chip will shut down the channel at a junction temperature of about 165ºC.

### Package Assembly

The green package devices are assembled with enhanced, environmental and compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B table 5-2 for the recommended solder reflow temperature profile.

## OPERATING RANGES

Microsemi guarantees the performance of this device over commercial (0ºC to 70ºC) and industrial (-40ºC to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

## Recommended Operating Conditions - Le88506 SLAC Device

| | |
|---|---|
| Ambient Temperature | –40 °C < $T_A$ < +85 °C |
| Ambient Relative Humidity | 15 to 85% |
| Analog Supply AVDD | +3.3 V ± 5%<br>DVDD ± 50 mV |
| Digital Supply DVDD | +3.3 V ± 5% |
| DGND | 0 V |
| AGND with respect to DGND | ±10 mV |
| Voltage Reference Capacitor: VREF to AGND | 10 µF ± 20% |
| Current Reference Resistor: IREF to AGND | 75 kΩ ± 1% |
| Digital Pins | DGND to 3.465 V |
| $I/O1_i$ | DGND to +5.25 V |
| Analog Pins | AGND – 0.3 V to AVDD + 0.3 V |

## Recommended Operating Conditions - Le88830 SLIC Device

| | |
|---|---|
| Ambient Temperature | –40 °C < $T_A$ < +85 °C |
| Ambient Relative Humidity | 15 to 85% |
| Analog Supply VCC | +3.3 V ± 5% |
| $VBAT_i$ Supplies | -150 V to +0.4 V |
| AGND | 0 V |
| BGND with respect to AGND | ±100 mV |
| $VREFS_i$ to AGND | 1.5 V ± 5% |
| Analog Pins | AGND – 0.3 V to VCC + 0.3 V |

# ELECTRICAL CHARACTERISTICS

## Test Conditions

Unless otherwise noted, test conditions are:

- Typical values are for TA = 25º C and nominal supply voltages. Minimum and maximum values are over the temperature and supply voltage ranges shown in Operating Ranges, except where noted
- Default (unity) gain in X, R, DRL, AX and AR blocks
- Default coefficients in DISN, Z and B filters
- DC feed programmed to ILA = 26 mA, VOC = 48.0 V, VAS = 12 V
- AC and DC load resistance $R_L$ = 600 Ω
- 0 dBm0 = 0 dBm (600 Ω) = 0.7746 Vrms. Digital gains GX0 and GR0 to achieve 0 dBr relative levels are
  GX0 = +6.797 dB (7A20h) A-law or linear and
  GX0 = +6.737 dB (2A20h) µ-Law to set A/D transmit gain to 0dB
  GR0 = -1.793 dB (6AA0h) A-law or linear and
  GR0 = -1.720 dB (3AA0h) µ-Law to set D/A receive gain to 0dB
- Ringing Tests have two conditions: C1 and C2 both with ILR = 78 mA and RTTH =25.5 mA AC
  - C1 programmed ringing 118 $V_{PK}$ (83.4 Vrms) 20 $V_{DC}$ offset and 1386 Ω + 40-µF load (5 REN)
  - C2 programmed ringing 70 $V_{PK}$ (50 Vrms) 0 $V_{DC}$ offset and 7000 Ω in series with 8-µF load (1 REN)

## Supply Currents and Power Dissipation

- External Switcher circuit as shown in Figure 45, *VE8820 Switching Regulator Circuit*, on page 65 with input voltage Vsw = 12 $V_{DC}$
- Supply currents and power consumption are per channel of the chipset based on both channels in the same state
- Device or package power does not include power delivered to the load
- Fuse resistors for power tests are $R_F$ = 0 Ω

| Operational State | Condition | $I_{DD}$ mA (Note Note 3.) | $I_{VSW}$ mA | $I_{VBAT}$ mA (Note Note 2.) | Package Power mW | Note |
|---|---|---|---|---|---|---|
| | | Typ | Typ | Typ | Typ | |
| Shutdown | Disconnect, Switcher off | 2.7 | 0 | 0 | 9 | Note 1. |
| Disconnect | $V_{BAT}$ = –59 V | 12 | 3 | 0.2 | 55 | Note 1. |
| Disconnect | $V_{BAT}$ = –25 V | 14 | 3 | 0.2 | 55 | Note 1. |
| Idle | On-Hook | 14 | 8 | 0.8 | 95 | Note 1. |
| **Active (Normal or Polarity** Reversal) | **On-Hook Transmission** | 25 | 16 | 2.0 | 200 | Note 1. |
| | **Off-Hook** 600 Ω | 25 | 66 | 28 | 380 | Note 1. |
| Ringing | C1 | 26 | 900 | 60 | 1800 | Note 1., Note 4., Note 5. |
| | C2 | 26 | 70 | 8 | 300 | Note 1., Note 5. |

***Note:***

1. *Not Tested in Production. Parameter is guaranteed by characterization or correlation to other tests.*
2. *Measured output of switching regulator feeding into Le88830 device $VBAT_i$ pin.*
3. *$I_{DD}$ supply current is the sum of $I_{AVDD}$, $I_{DVDD}$ and $I_{VCC}$ for the chipset divided by 2. Wideband mode increases $I_{DD}$ by 5mA per channel.*
4. *Ringing signal must be cadenced to produce an average power that can be handled by the package.*
5. *Fixed ringing regulation mode was used for these measurements.*

## Le88506 SLAC DC Characteristics

| Symbol | Parameter Descriptions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Digital Input Low voltage | | | 0.8 | V | |
| $V_{IH}$ | Digital Input High voltage | 2.0 | | | | |
| $I_{IL}$ | Digital Input leakage current | –7 | | +7 | µA | |
| $I_{AIL}$ | Analog input leakage current | –1 | | +1 | | |
| $V_{HYS}$ | Digital Input hysteresis | 0.16 | 0.25 | 0.34 | V | Note 1. |
| $V_{OL}$ | Digital Output Low voltage<br>I/O1 ($I_{OL}$ = 50 mA)<br>I/O2 and SWOUTx ($I_{OL}$ = 4 mA)<br>I/O2 and SWOUTx ($I_{OL}$ = 8 mA)<br>$\overline{TSCA}$ ($I_{OL}$ =14 mA)<br>Other digital outputs ($I_{OL}$ = 2 mA) | | | <br>0.8<br>0.4<br>0.8<br>0.4<br>0.4 | V | Note 2. |
| $V_{OH}$ | Digital Output High voltage<br>I/O1, I/O2 ($I_{OH}$ = 4 mA)<br>I/O1, I/O2 ($I_{OH}$ = 8 mA)<br>Other digital outputs ($I_{OH}$ = 400 µA) | <br>$V_{DVDD}$ – 0.4 V<br>$V_{DVDD}$ – 0.8 V<br>2.4 | | | | Note 2. |
| $I_{OL}$ | Digital Output leakage current (Hi-Z state)<br>0 < V < DVDD | <br>–7 | | <br>+7 | µA | |
| $V_{REF}$ | VREF output open circuit voltage ($I_{VREF}$ = +/- 100 µA) | 1.43 | 1.5 | 1.57 | V | |
| $C_{IREF}$ | IREF pin maximum load capacitance | | | 20 | pF | Note 1. |
| $C_I$ | Digital Input capacitance | | | 4 | | Note 1. |
| $C_O$ | Digital Output capacitance | | | 4 | | Note 1. |
| $PSRR_1$ | AVDD, DVDD Power supply rejection ratio<br>(1.02 kHz, 100 $mV_{RMS}$, either path, GX = GR = 0 dB) | 32 | 38 | | dB | |
| $PSRR_2$ | $VBAT_i$ Power supply rejection ratio<br>(1.02 kHz, 100 $mV_{RMS}$, either path, GX = GR = 0 dB) | 40 | | | | |

***Note:***

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *The I/O1, I/O2 outputs are resistive for less than a 0.8 V drop. Total current must not exceed absolute maximum ratings.*

## DC Feed and Signaling

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| $I_L$, Loop-current accuracy, Active state | $I_L$ in constant-current region after ILA calibration | -10 | | +10 | % | Note 1. |
| $I_{RINGD}$, RINGD leakage, Ring Open state | VBAT = -59 V<br>$R_L$ = 0 to GND or VBAT | | | 1000 | µA | |
| $I_{TIPD}$, TIPD leakage, Tip Open state | VBAT = -59 V<br>$R_L$ = 0 to GND or VBAT | | | 1000 | µA | |
| TIPD, RINGD leakage, Disconnect state | VBAT = -59 V<br>$R_L$ = 0 to GND or VBAT | | | 10 | µA | |
| $I_{RINGD}$, RINGD current accuracy, Tip Open state | RINGD to ground | -10 | | +10 | % | Note 1. |
| $V_{TIPD}$, ground-start signaling | TIPD to –48 V = 7 kΩ,<br>RINGD to ground = 100 Ω | –7.5 | –5 | | V | Note 1.,Note 2. |
| TDC, RDC input offset current | | 3.3 | 3.7 | 4.1 | µA | Note 1.,Note 3. |
| Ground key accuracy | | -20 | | +20 | % | Note 1. |
| Switch hook accuracy | | -20 | | +20 | | Note 1. |
| Open circuit voltage | VOC = 48 V, after VOC calibration | -8 | | +8 | | Note 1. |
| $V_{RINGD}$, open circuit | VOC = 48 V, after VOC calibration | –56.5 | | -49.0 | V | Note 1.,Note 2. |

***Note:***

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *The following bytes must be sent to the Le88506 device in the Normal Active state in order to meet this specification when responding to a ground start: F2 00 00 80 00.*
3. *Analog input pad leakage can add to this value - see specification under Le88506 SLAC DC Characteristics*

## Metering

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Level accuracy | 0.5 Vrms, 12 or 16 kHz<br>200 or 3000 Ω AC load | -5 | | +10 | % | Note 1. |
| Frequency accuracy | 12 or 16 kHz | –0.1 | | +0.1 | % | Note 1. |

***Note:***

1. *This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.*

## Ringing

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Ringing Voltage Accuracy | Case C1 or C2 | -5 | | +5 | % | Note 1. |
| $V_{AB}$, Ringing DC offset | $R_L$ = open, $V_{RING}$ = 0 V | -2 | | +4 | V | Note 1. |
| Harmonic distortion | Case C1 or C2 | | 3 | 5 | % | Note 1. |
| Ringing current limit accuracy | $R_L$ = 300 Ω | -10 | | 10 | % | Note 1. |
| Ringing source impedance | | | 200 | | Ω | Note 1. |
| DC ring trip accuracy | EGBIAS = 1 | -15 | | +15 | % | Note 2. |
| AC ring trip accuracy | EGBIAS = 0 | -15 | | +15 | % | |
| Ring trip delay | Periods of ringing | 1 | | 3 | cycles | Note 1. |

***Note:***

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *If the ringing current in the loop is near the current limit more than 50% of the time, a ring trip will occur regardless of the average current.*

## Le88506 Switching Regulator Controller

The following specifications apply to switching regulator controllers Y and Z.

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| SWISx shutdown threshold | Referenced to AGND | 85 | 100 | 115 | mV | |
| SWISx hysteresis | | | 5 | | mV | Note 1. |
| SWISx input bias current | | -10 | | 10 | µA | Note 1. |
| SWISx shutdown delay | $V_{SWISx}$ > 115mV | 12 | | 88 | ns | Note 2. |
| SWCPMx output current | | -200 | | 200 | µA | Note 1. |
| SWCMPx operating range | | 0.4 | | 2.6 | V | Note 1. |
| SWVSx to SWCMPx gain | | 0.4 | | 40 | V/nA | Note 1. |
| SWVSx to SWCMPx bandwidth | | 100 | | | kHz | Note 1. |
| SWVSx input offset current | | 3.3 | 3.7 | 4.1 | µA | Note 3. |
| LFC output impedance | | | 80 | | kΩ | Note 1. |
| SWxV output voltage accuracy | Calibrated -95 V Absolute Battery Voltage | TBD | | TBD | V | Note 1., Note 4. |

***Note:***

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *Time from SWISx exceeding threshold to SWOUTx voltage passing through VDD/2.*
3. *Analog input pad leakage can add to this value - see specification under Le88506 SLAC DC Characteristics*
4. *Target accuracy based on self calibration is +/-5 V*

## Le88506 Converter Configuration Signal Sense Accuracy

See command *A6/A7h Write/Read Converter Configuration*, on page 85 for measurement ranges and resolution.

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Metallic AC coupled voltage | Converter Configuration = 00h | -4 | | +4 | % | |
| Switcher input at SWVSY | Converter Configuration = 01h | -2.5 V - 4% | | +2.5 V + 4% | V | Note 1.,Note 3. |
| Switcher input at SWVSZ | Converter Configuration = 02h | -2.5 V - 4% | | +2.5 V + 4% | V | |
| Tip voltage to ground | Converter Configuration = 04h | - 6% | | + 6% | V | Note 1.,Note 2.,Note 3. |
| Ring voltage to ground | Converter Configuration = 05h | - 6% | | + 6% | V | |
| Metallic DC line voltage | Converter Configuration = 06h | - 7% | | + 7% | V | |
| Metallic loop current | Converter Configuration = 07h | -1.5 mA - 5% | | 1.5 mA + 5% | mA | Note 1.,Note 3. |
| Total longitudinal current | Converter Configuration = 08h | -2.5 mA - 5% | | 2.5 mA + 5% | mA | Note 1.,Note 4. |
| Voice DAC (Full loopback) | Converter Configuration = 0Ah | -0.7 | | +0.7 | dB | |
| Tip Voltage to Longitudinal Current Ratio | Ratio of Voltage to current in Low Gain state, two point measurement | -6.5 | | +6.5 | % | Note 3. |
| Ring Voltage to Longitudinal Current Ratio | | -6.5 | | +6.5 | % | |
| Metallic Voltage to Metallic Current Ratio | | -6.5 | | +6.5 | % | |

## Note:

1. *The % limits are defined as the % of programmed threshold value or the % of the actual voltage on Tip / Ring The offset and percentage errors are independent and combine as rms errors.*
2. *This is measured in production by calibrating offset voltage and applying -26V for Ring voltage to ground and 20 V metallic. Accurately measuring smaller voltage requires care in offset calibration.*
3. *For DC measurements these limits require that the high pass filters are disabled in the operating conditions register and the residual A/D offset is removed by reading the no connect value (Converter Configuration 0Bh) and subtracting it from the measured value. DISN should be cut off (00h), the analog Voice Path Gains set to unity (00h) and the operating functions register set to linear mode (80h).*
4. *For DC measurements these limits require that the high pass filters are disabled in the operating conditions register, DISN should be cut off (00h), the analog Voice Path Gains set to unity (00h) and the operating functions register set to linear mode (80h).*

## Transmission Characteristics - Narrowband Codec Mode

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TAC - RAC overload level | Active state, GX = AX = 0 dB | 3.4 | | | Vpk | Note 1.,Note 2. |
| Transmit level, A/D | 0 dBm, GX = GX0, 1014 Hz | | 0 | | dBm0 | |
| Receive level, D/A | 0 dBm0, GR = GR0, 1014 Hz | | 0 | | dBm | |
| Gain accuracy, D/A or A/D | 0 dBm0, 1014 Hz, off-hook | –0.35 | | +0.35 | dB | |
| Gain accuracy, D/A or A/D | 0 dBm0, 1014 Hz, on-hook | –0.25 | | +0.75 | dB | |
| Idle channel noise<br>$V_{TIPD}$ - $V_{RINGD}$<br><br>DXA, Digital out | <br>DRA, Digital input = 0 A-law, 0 dBr<br>DRA, Digital input = 0 µ-law, 0 dBr<br>$V_{TIPD}$ - $V_{RINGD}$ = 0 VAC A-law, 0 dBr<br>$V_{TIPD}$ - $V_{RINGD}$ = 0 VAC µ-law, 0 dBr | | | <br>–74<br>16<br>–65<br>19 | <br>dBm0p<br>dBrnC0<br>dBm0p<br>dBrnC0 | Note 5.<br>Note 1.,<br>Note 5.<br>Note 5.<br>Note 1.,<br>Note 5. |
| Two-wire return loss | 200 to 3400 Hz | 26 | | | dB | Note 1. |
| Longitudinal to Metallic balance TIPD - RINGD or DXA | 200 to 3400 Hz | 50 | | | dB | Note 7. |
| DRA to Longitudinal signal generation | 300 to 3400 Hz | 42 | | | | Note 7. |
| Longitudinal current capability, TIPD or RINGD | Active state | 8.5 | | | mArms | Note 1. |
| Longitudinal impedance at TIPD or RINGD | 0 to 100 Hz | | 100 | | Ω/pin | Note 1. |
| Crosstalk between channels<br>TX or RX to TX<br>RX or TX to RX | <br>0 dBm0, 1014Hz, Average<br>0 dBm0, 1014Hz, Average | | | <br>-76<br>-78 | dBm0 | Note 1. |
| Attenuation distortion | 300 to 3000 Hz | –0.125 | | +0.125 | dB | Note 1.,Note 3. |
| Single frequency distortion | | | | –46 | | Note 4. |
| Second harmonic distortion, D-A | GR = 0 dB, linear mode | | | –55 | | |
| End-to-end absolute group delay | B = Z = 0; X = R = 1, C/L = 0 | | | 678 | µs | Note 1.,Note 6. |

***Note:***

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *Overload level is defined when THD = 1%.*
3. *See Figure 23 and Figure 24.*
4. *0 dBm0 input signal, 300 to 3400 Hz measurement at any other frequency, 300 Hz to 3400 Hz.*
5. *No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.*
6. *The End-to-End Group Delay is the absolute group delay of the echo path with the B filter turned off.*
7. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

## Attenuation Distortion - Narrowband Codec Mode

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 23 and Figure 24. The reference frequency is 1014 Hz and the signal level is –10 dBm0.

**Figure 23. Transmit Path Attenuation vs. Frequency**

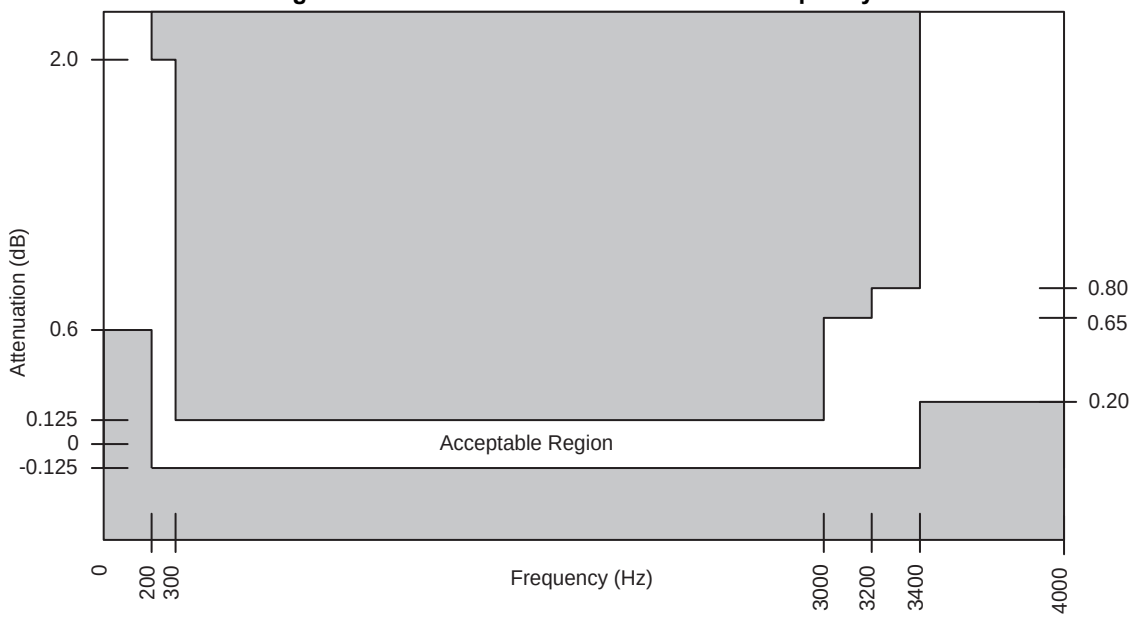
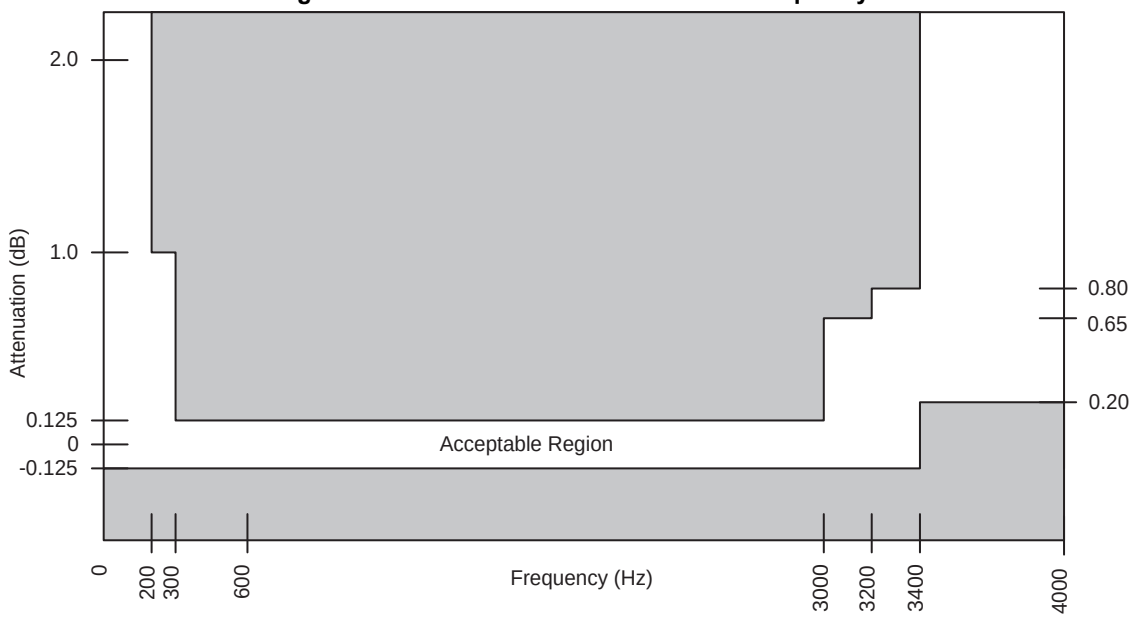



**Figure 24. Receive Path Attenuation vs. Frequency**




## Discrimination Against Out-of-Band Input Signals - Narrowband Codec Mode

When an out-of-band sine wave signal of frequency f, and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014-Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in Table .

***Note:***

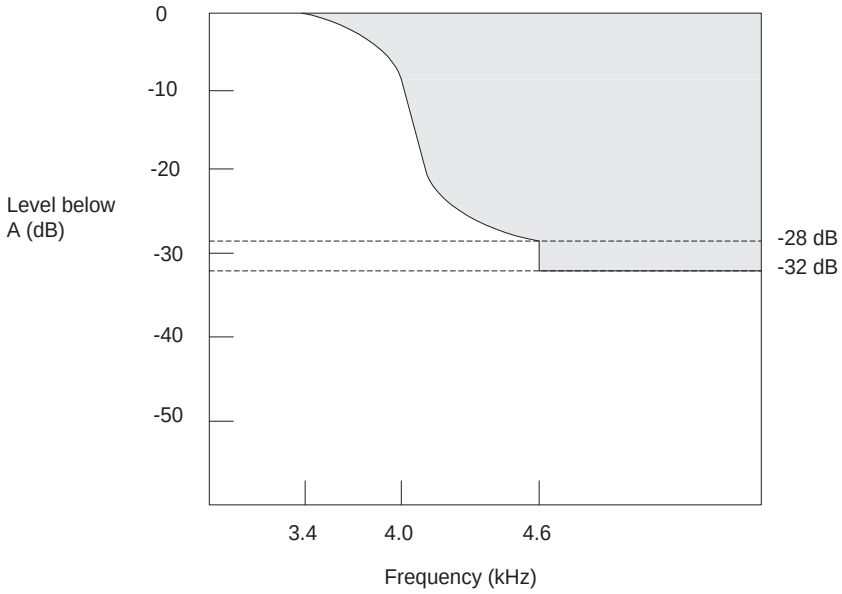
*The attenuation of the waveform below amplitude A, between 3400 Hz and 4600 Hz, is given by the formula:*

$$\text{Attenuation} = \left[14 - 14\sin\left(\frac{\pi(4000 - f)}{1200}\right)\right] \text{dB}$$

### Out of Band Discrimination, Narrowband Codec Mode.

| Frequency of Out-of-Band Signal | Amplitude of Out-of-Band Signal | Level below A |
|---|---|---|
| 16.6 Hz < f < 45 Hz | –25 dBm0 < A ≤ 0 dBm0 | 18 dB |
| 45 Hz < f < 65 Hz | –25 dBm0 < A ≤ 0 dBm0 | 25 dB |
| 65 Hz < f < 100 Hz | –25 dBm0 < A ≤ 0 dBm0 | 10 dB |
| 3400 Hz < f < 4600 Hz | –25 dBm0 < A ≤ 0 dBm0 | see Figure 25 |
| 4600 Hz < f < 100 kHz | –25 dBm0 < A ≤ 0 dBm0 | 32 dB |

**Figure 25. Discrimination Against Out-of-Band Signals**




## Discrimination Against 12- and 16-kHz Metering Signals - Narrowband Codec Mode

If the VE8820 chipset is used in a metering application where 12- or 16-kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of these tones may also appear at the transmit input. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12-kHz or 16-kHz tone, the frequency components below 4 kHz are reduced from the input by at least 70 dB. The sum of the peak metering and signal voltages must be within the TAC - RAC pin overload level.

## Spurious Out-of-Band Signals at the Analog Output - Narrowband Codec Mode

With PCM idle code being applied to the digital input and either a quiet 600 ohm termination or an open being applied to Tip and Ring, any single frequency tone between 0 and 16kHz measured at the analog output shall be less than -50dBm0.

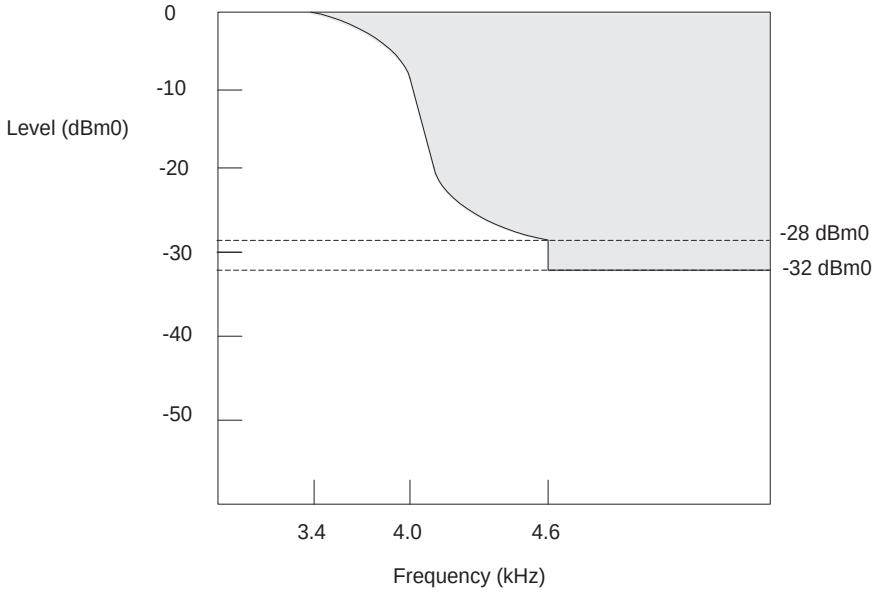
With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

| Frequency | Level |
|---|---|
| 4.6 kHz to 40 kHz | –32 dBm0 |
| 40 kHz to 240 kHz | –46 dBm0 |
| 240 kHz to 1 MHz | –36 dBm0 |

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 26. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$Level = \left[ -14 - 14\sin\left(\frac{\pi(f-4000)}{1200}\right)\right] dBm0$$

**Figure 26. Spurious Out-of-Band Signals**

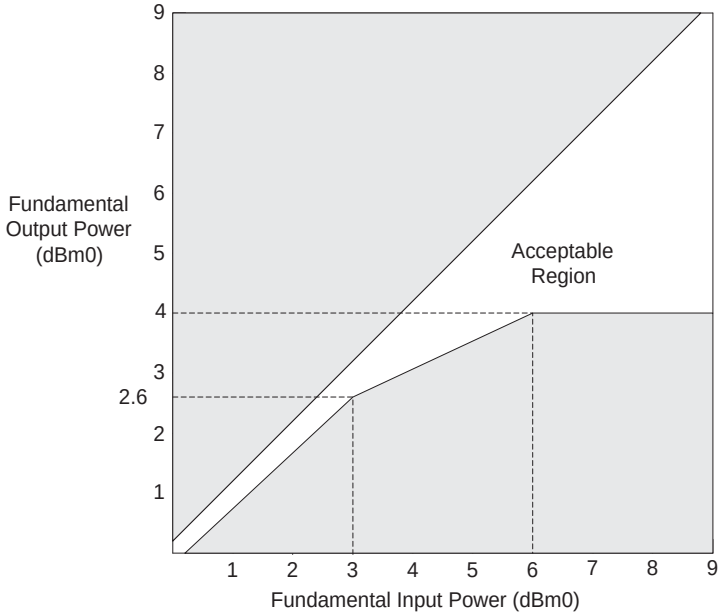



## Overload Compression - Narrowband Codec Mode

Figure 27 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

1. 1.2 dB < GX ≤ + 12 dB
2. –12 dB ≤ GR < –1.2 dB
3. Digital voice output of one VoicePort channel connected to digital voice input of a second VoicePort channel.
4. Measurement analog-to-analog.

**Figure 27. Analog-to-Analog Overload Compression**



## Gain Linearity - Narrowband Codec Mode

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 28 (A-law) and Figure 29 (µ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

**Figure 28. A-law Gain Linearity with Tone Input (Both Paths)**

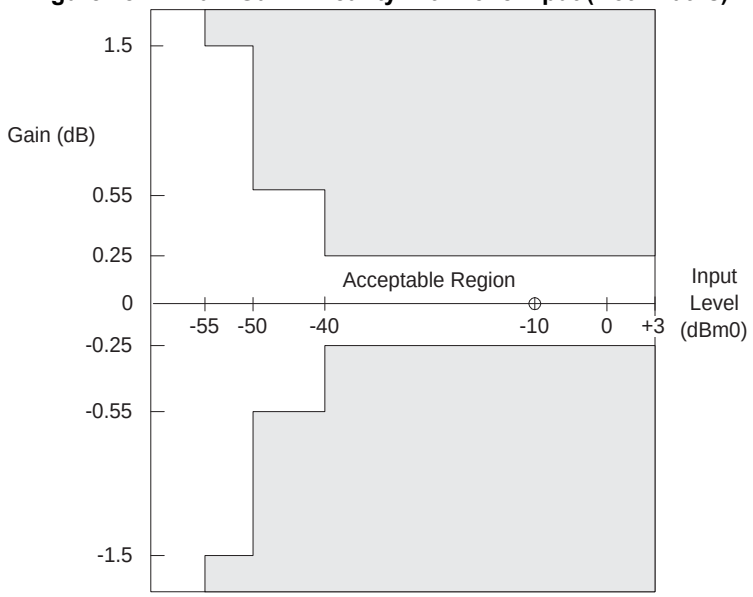
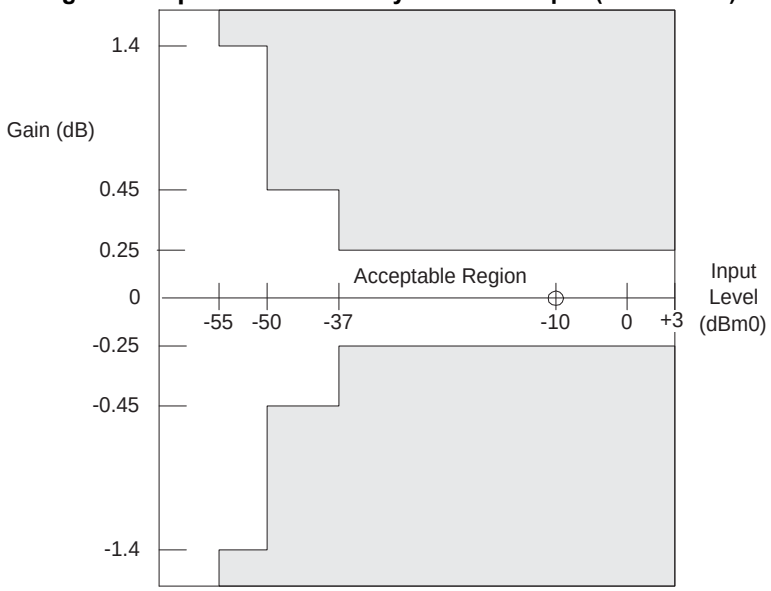


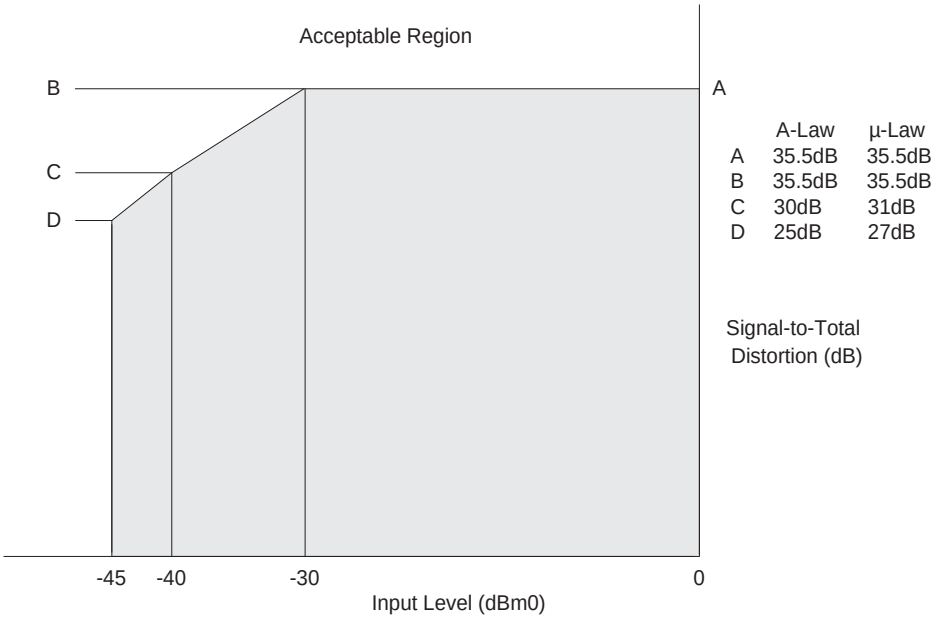

**Figure 29. µ-law Gain Linearity with Tone Input (Both Paths)**




## Total Distortion Including Quantizing Distortion - Narrowband Codec Mode

The signal to total distortion ratio will exceed the limits shown in Figure 30 for either path when the input signal is a sine wave with a frequency of 1014 Hz, using psophometric weighting for A-law and C-message weighting for µ-law

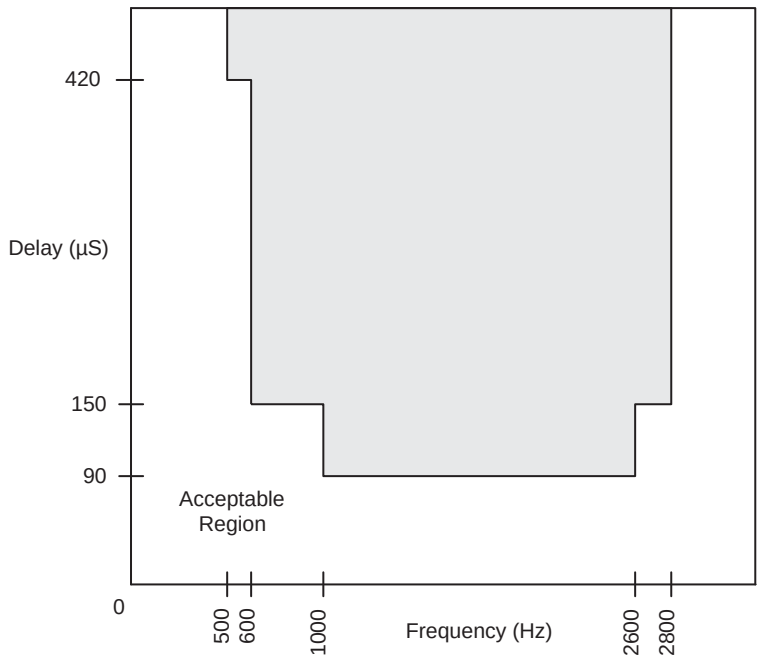
**Figure 30. Total Distortion with Tone Input (Both Paths)**




## Group Delay Distortion - Narrowband Codec Mode

For either transmission path, the group delay distortion is within the limits shown in Figure 31. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

**Figure 31. Group Delay Distortion**



## Transmission Characteristics - Wideband Codec Mode

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TAC - RAC overload level | Active state GX = AX = 0 dB | 3.4 | | | Vpk | Note 2. |
| Transmit level, A/D | 0 dBm, GX = GX0, 1014 Hz | | 0 | | dBm0 | |
| Receive level, D/A | 0 dBm0, GR = GR0, 1014 Hz | | 0 | | dBm | |
| Gain accuracy, D/A or A/D | 0 dBm0, 1014 Hz, off-hook | –0.5 | | +0.5 | dB | |
| Gain accuracy, D/A or A/D | 0 dBm0, 1014 Hz, on-hook | –0.25 | | +0.75 | | |
| Attenuation distortion | 100 Hz to 6.0 kHz | –0.25 | | +0.25 | | Note 3. |
| Single frequency distortion | 50 Hz to 7.0 kHz | | | –46 | | Note 4. |
| Signal to noise + distortion | Linear Mode 50 Hz to 7.0 kHz | TBD | | | | Note 4. |
| Second harmonic distortion, D-A | GR = 0 dB | | | –55 | | |
| Idle channel noise, 7 kHz Flat<br>$V_{TIPD}$ - $V_{RINGD}$<br>DXA, Digital out | <br>DRA, Digital input = 0 Linear, 0 dBr<br>$V_{TIPD}$ - $V_{RINGD}$ = 0 VAC Linear, 0 dBr | | | <br>TBD<br>TBD | <br>dBm0<br>dBrn0 | <br>Note 5.<br>Note 5. |
| End-to-end absolute group delay | B = Z = 0; X = R = 1, C/L = 0 | | | 340 | µs | Note 1.,Note 6. |
| Two-wire return loss | 50 to 7000 Hz | 20 | 26 | | dB | Note 1. |
| Longitudinal to Metallic balance TIPD - RINGD or DXA | 50 to 7000 Hz | TBD | | | dB | Note 7. |
| DRA to Longitudinal signal generation | 300 to 7000 Hz | 40 | | | | Note 1. |
| Longitudinal current capability, TIPD or RINGD | Active state | 8.5 | | | mArms | Note 1. |
| Longitudinal impedance at TIPD or RINGD | 0 to 100 Hz | | 100 | | Ω/pin | Note 1. |

***Note:***

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *Overload level is defined when THD = 1%.*
3. *See Figure 32 and Figure 33.*
4. *0 dBm0 input signal, 50 to 7000 Hz measurement at any other frequency, 50 to 7000 Hz.*
5. *No single frequency component in the range above 7600 Hz may exceed a level of –55 dBm0.*
6. *The End-to-End Group Delay is the absolute group delay of the echo path with the B filter turned off.*
7. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

## Attenuation Distortion - Wideband Codec Mode

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 32 and Figure 33. The reference frequency is 1014 Hz and the signal level is –10 dBm0.

**Figure 32. Transmit Path Attenuation vs. Frequency**

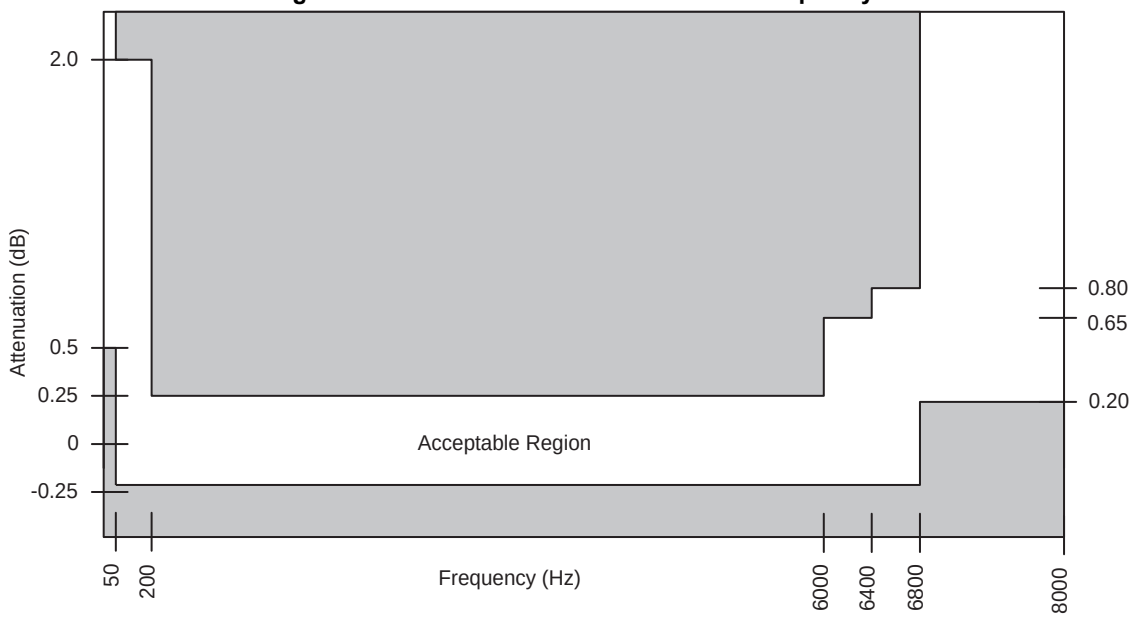
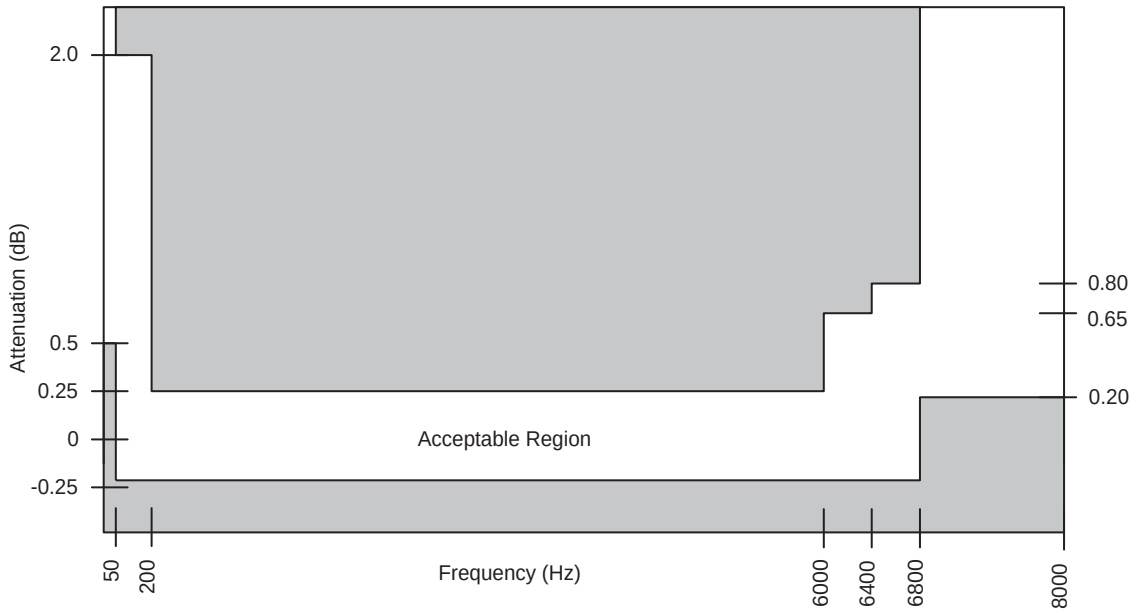


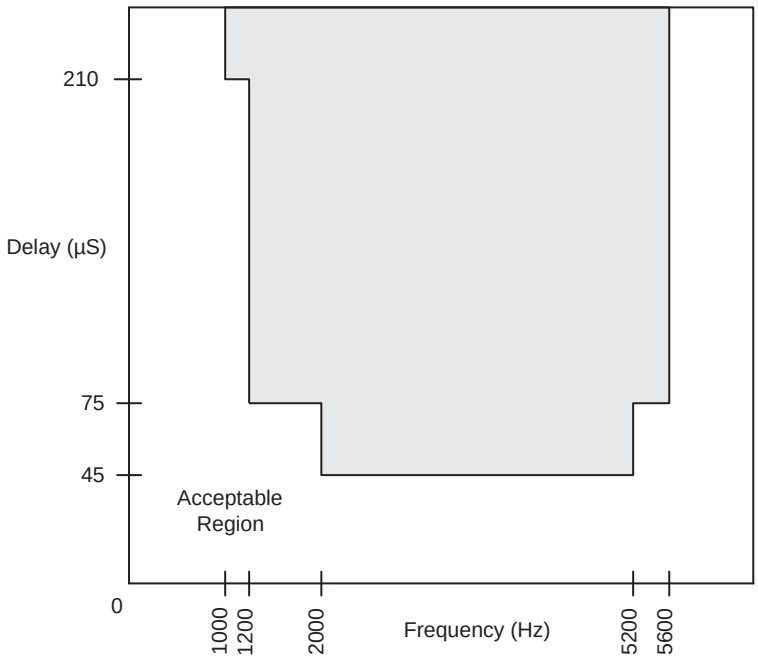

**Figure 33. Receive Path Attenuation vs. Frequency**




## Group Delay Distortion - Wideband Codec Mode

For either transmission path, the group delay distortion is within the limits shown in Figure 34. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

**Figure 34. Group Delay Distortion**




## SWITCHING CHARACTERISTICS AND WAVEFORMS

The following are the switching characteristics over operating range (unless otherwise noted). Min and max values are valid for all digital outputs with a 115-pF load. (See Figure 35 and Figure 36 for the microprocessor interface timing diagrams.)

## Microprocessor Interface Timing

| No. | Symbol | Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 1 | $t_{DCY}$ | Data clock period | 122 | | | ns | |
| 2 | $t_{DCH}$ | Data clock HIGH pulse width | 48 | | | | |
| 3 | $t_{DCL}$ | Data clock LOW pulse width | 48 | | | | |
| 4 | $t_{DCR}$ | Rise time of clock | | | 25 | | |
| 5 | $t_{DCF}$ | Fall time of clock | | | 25 | | |
| 6 | $t_{ICSS}$ | Chip select setup time, Input mode | 30 | | $t_{DCY}$ –10 | | |
| 7 | $t_{ICSH}$ | Chip select hold time, Input mode | 0 | | $t_{DCH}$ –20 | | |
| 8 | $t_{ICSL}$ | Chip select pulse width, Input mode | | $8t_{DCY}$ | | | |
| 9 | $t_{ICSO}$ | Chip select off time, Input mode | 2500 | | | | |
| 10 | $t_{IDS}$ | Input data setup time | 25 | | | | |
| 11 | $t_{IDH}$ | Input data hold time | 20 | | | | |
| 12 | $t_{OLH}$ | I/O1, I/O2 output latch valid | | | 2500 | | |
| 13 | $t_{OCSS}$ | Chip select setup time, Output mode | 30 | | $t_{DCY}$ –10 | | |
| 14 | $t_{OCSH}$ | Chip select hold time, Output mode | 0 | | $t_{DCH}$ –20 | | |
| 15 | $t_{OCSL}$ | Chip select pulse width, Output mode | | $8t_{DCY}$ | | | |
| 16 | $t_{OCSO}$ | Chip select off time, Output mode | 2500 | | | | |
| 17 | $t_{ODD}$ | Output data turn on delay | | | 36 | | Note 1. |
| 18 | $t_{ODH}$ | Output data hold time | 3 | | | | |
| 19 | $t_{ODOF}$ | Output data turn off delay | | | 36 | | |
| 20 | $t_{ODC}$ | Output data valid | | | 36 | | |
| 21 | $t_{RST}$ | Reset pulse width | 50 | | | µs | |

***Notes:***

*1. The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.*

**Figure 35. Microprocessor Interface (Input Mode)**

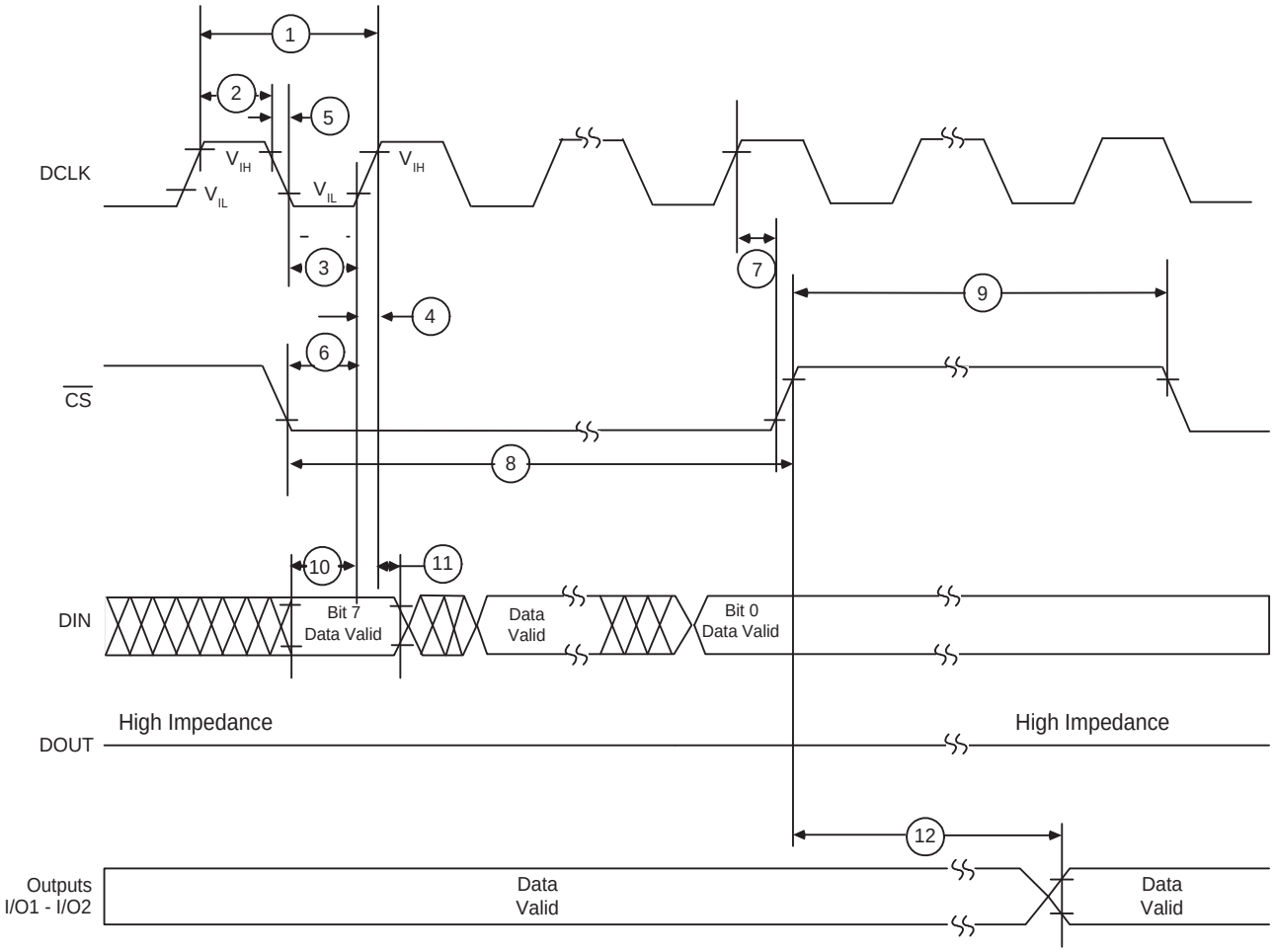
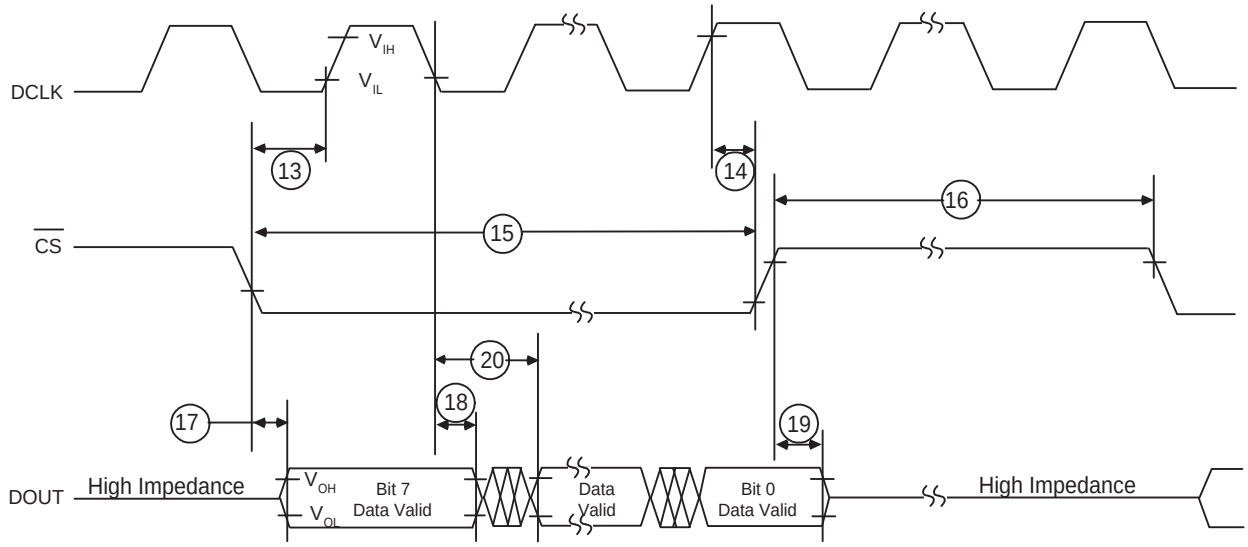



**Figure 36. Microprocessor Interface (Output Mode)**



## PCM Interface Timing

PCLK shall not exceed 8.192 MHz. Pull-up resistor to DVDD of 240 Ω is attached to $\overline{\text{TSCA}}$.
(See Figure 37 through Figure 39 for the PCM interface timing diagrams.)

| No. | Symbol | Parameter | Min. | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 22 | $t_{PCY}$ | PCM Clock (PCLK) period | 122 | | 651 | ns | Note 1. |
| 23 | $t_{PCH}$ | PCLK HIGH pulse width | 48 | | | | |
| 24 | $t_{PCL}$ | PCLK LOW pulse width | 48 | | | | |
| 25 | $t_{PCF}$ | PCLK fall time | | | 15 | | |
| 26 | $t_{PCR}$ | PCLK rise time | | | 15 | | |
| 27 | $t_{FSS}$ | FS setup time | 25 | | $t_{PCY}$–30 | | |
| 28 | $t_{FSH}$ | FS hold time | 50 | | | | |
| 29 | $t_{FST}$ | Allowed PCLK or FS jitter time - narrowband | –50 | | 50 | | Note 1. |
| 29 | $t_{FST}$ | Allowed PCLK or FS jitter time - wideband | –25 | | 25 | | Note 1. |
| 30 | $t_{TSD}$ | Delay to $\overline{\text{TSCA}}$ valid | 5 | | 80 | | Note 2. |
| 31 | $t_{TSO}$ | Delay to $\overline{\text{TSCA}}$ off | 5 | | | | Note 2., Note 3. |
| 32 | $t_{DXD}$ | PCM data output delay | 5 | | 70 | | |
| 33 | $t_{DXH}$ | PCM data output hold time | 5 | | 70 | | |
| 34 | $t_{DXZ}$ | PCM data output delay to high Z | 10 | | 70 | | |
| 35 | $t_{DRS}$ | PCM data input setup time | 25 | | | | |
| 36 | $t_{DRH}$ | PCM data input hold time | 5 | | | | |

***Notes:***

1. *The PCLK frequency must be an integer multiple of the frame sync (FS) frequency. Frame sync is expected to be an accurate 8-kHz pulse train. The actual PCLK rate depends on the CSEL bit setting in the Device Configuration register. The minimum frequency is 1.024MHz and the maximum frequency is 8.192 MHz.*
   *If PCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.*
2. *$\overline{TSC}$ is delayed from FS by a typical value of N • $t_{PCY}$, where N is the value stored in the time/clock-slot register.*
3. *$t_{TSO}$ is defined as the time at which the output achieves the Open Circuit state.*

**Figure 37. PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)**

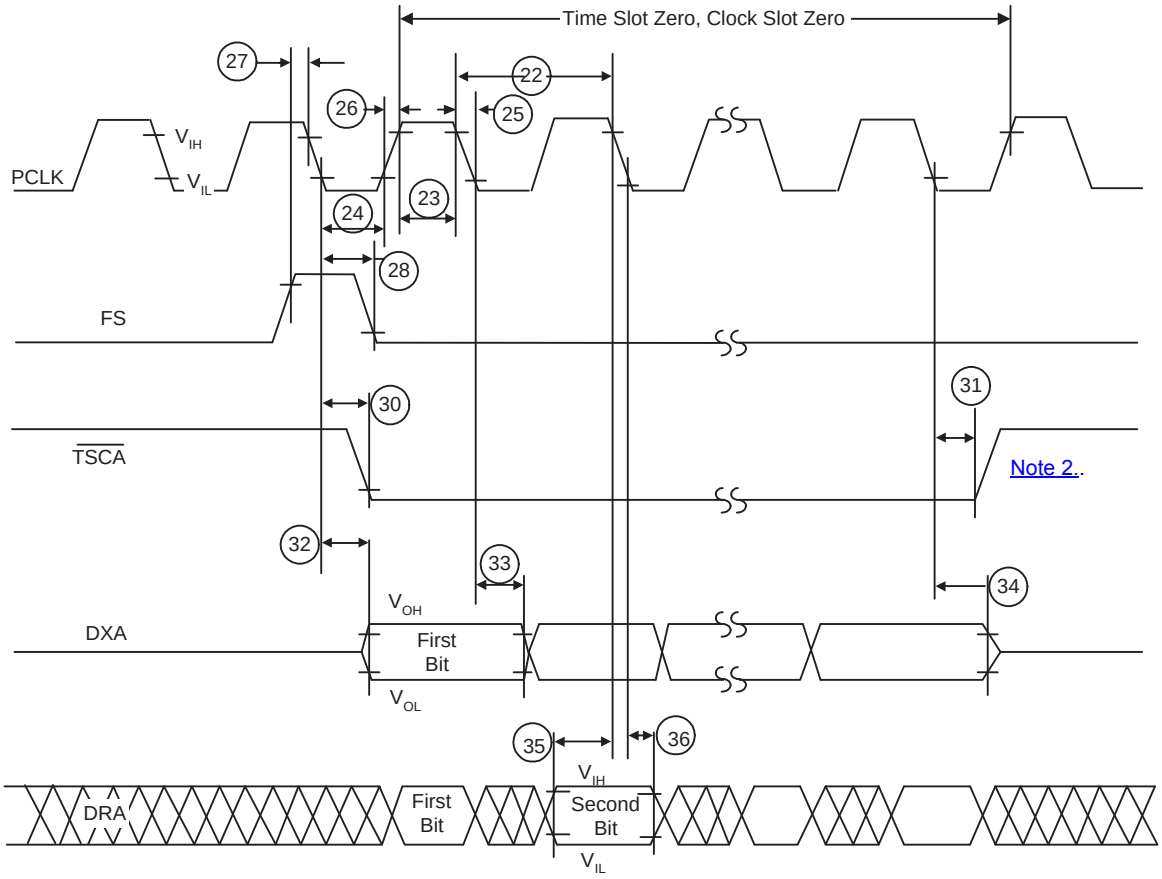


**Figure 38. PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)**

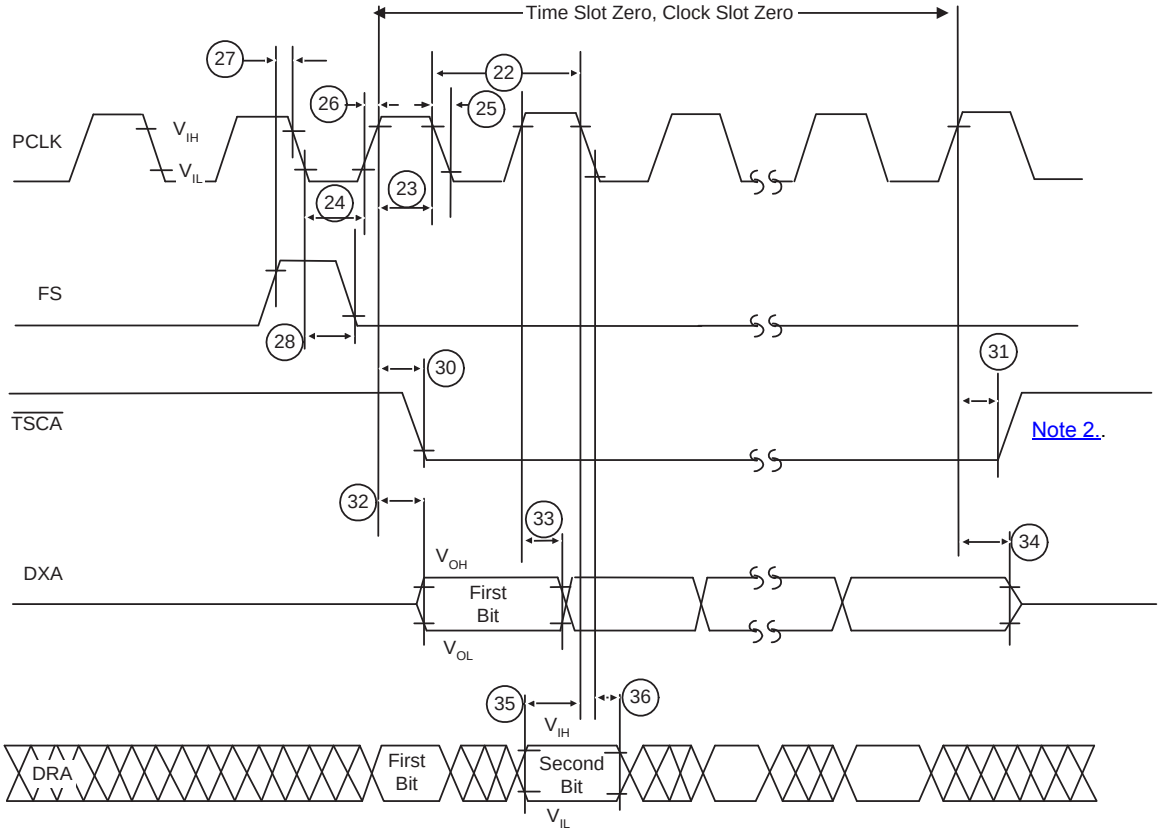



**Figure 39. PCM Clock Timing**

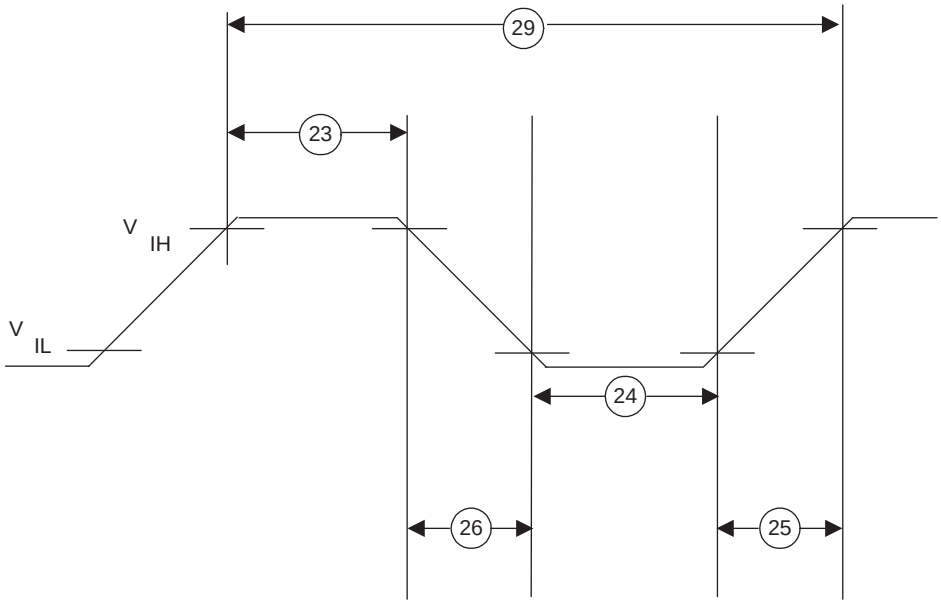
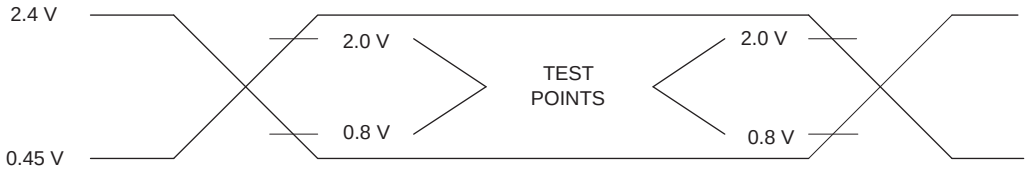


**Figure 40. Input and Output Waveforms for AC Tests**




## GCI Timing

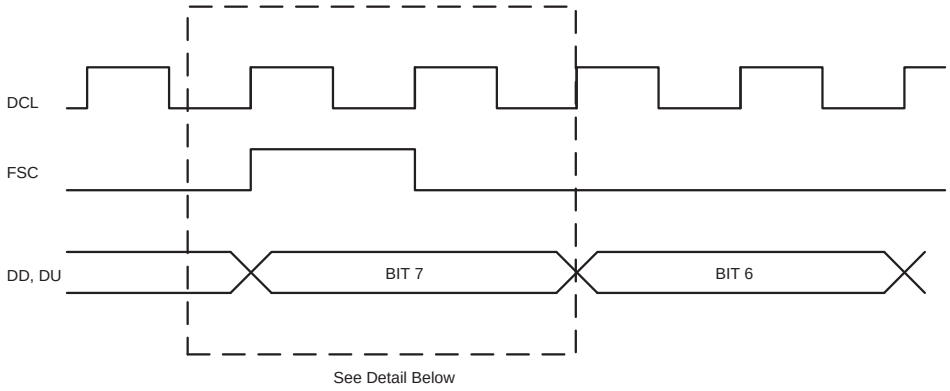
(See Figure 41 and Figure 42 for the GCI interface timing diagrams.)

| No. | Symbol | Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 37 | $J_{DCL}$ | DCL Jitter | | | 50 | ns | Note 1. |
| 38 | $t_R$, $t_F$ | Rise/fall time | | | 60 | | |
| 39 | $t_{DCL}$ | Period, $F_{DCL}$ = 2048 kHz | 488.23 | 488.28 | 488.33 | | |
| | | $F_{DCL}$ = 4096 kHz | 244.11 | 244.14 | 244.17 | | |
| 40 | $t_{WH}$, $t_{WL}$ | Pulse width | 90 | | | | |
| 41 | $t_{SF}$ | Setup time | 70 | | $t_{DCL}$–50 | | |
| 42 | $t_{HF}$ | Hold time | 50 | | | | |
| 43 | $t_{WFH}$ | High pulse width | 130 | | | | |
| 44 | $t_{DDC}$ | Delay from DCL edge | | | 100 | | |
| 45 | $t_{DDF}$ | Delay from FS edge | | | 150 | | |
| 46 | $t_{SD}$ | Data setup | twH+20 | | | | |
| 47 | $t_{HD}$ | Data hold | 50 | | | | |

***Notes:***

*1. If DCL has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.*

**Figure 41. 4.096 MHz DCL Operation**



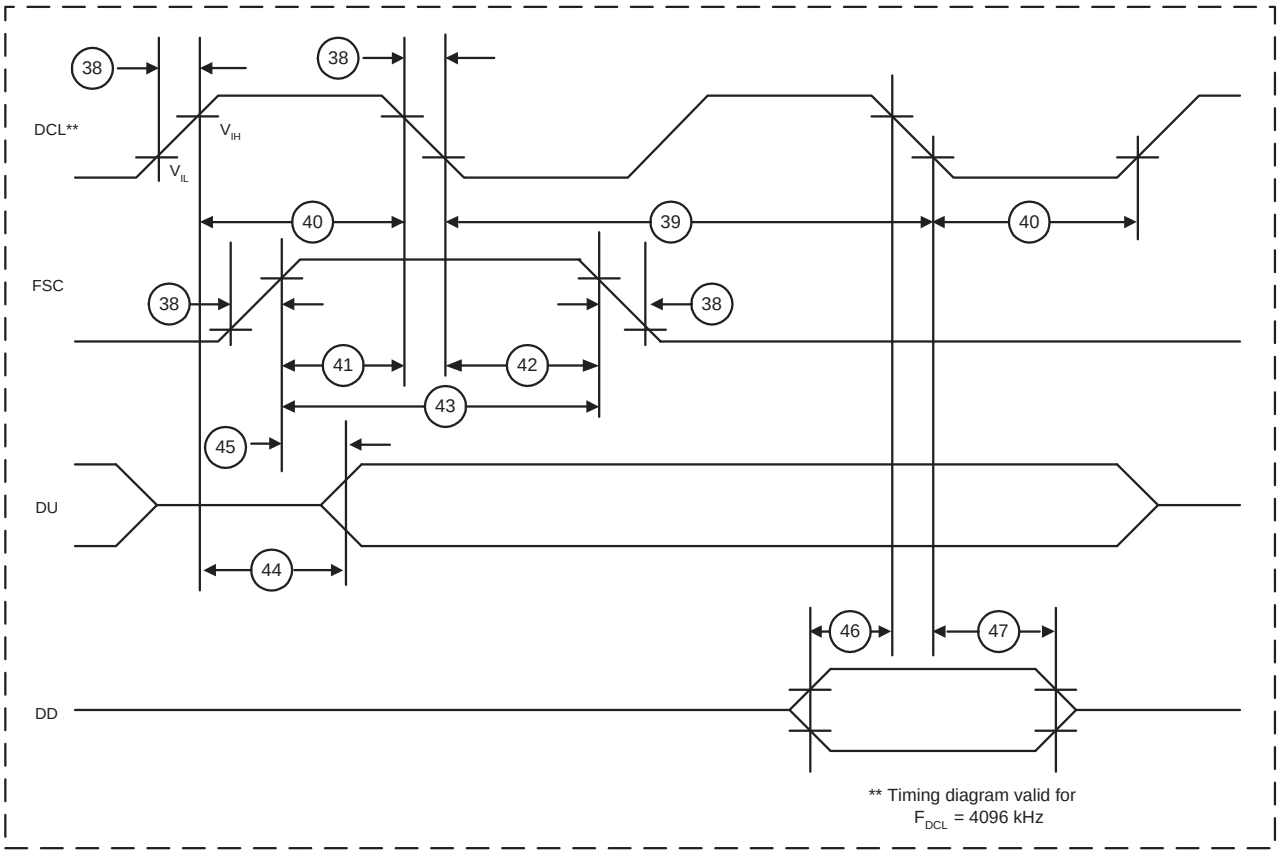
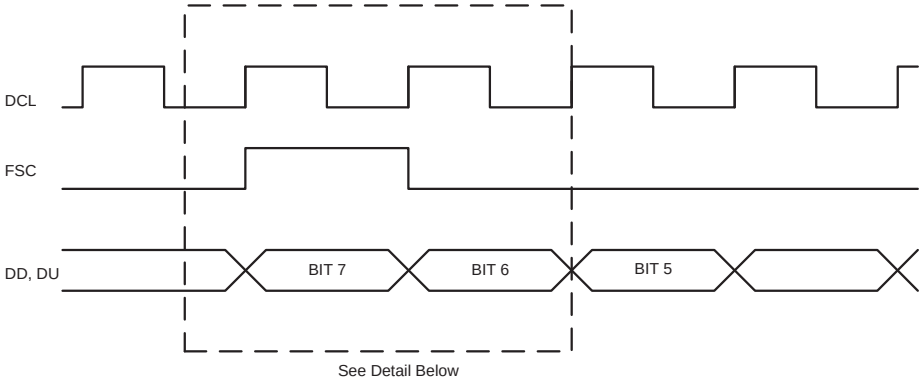
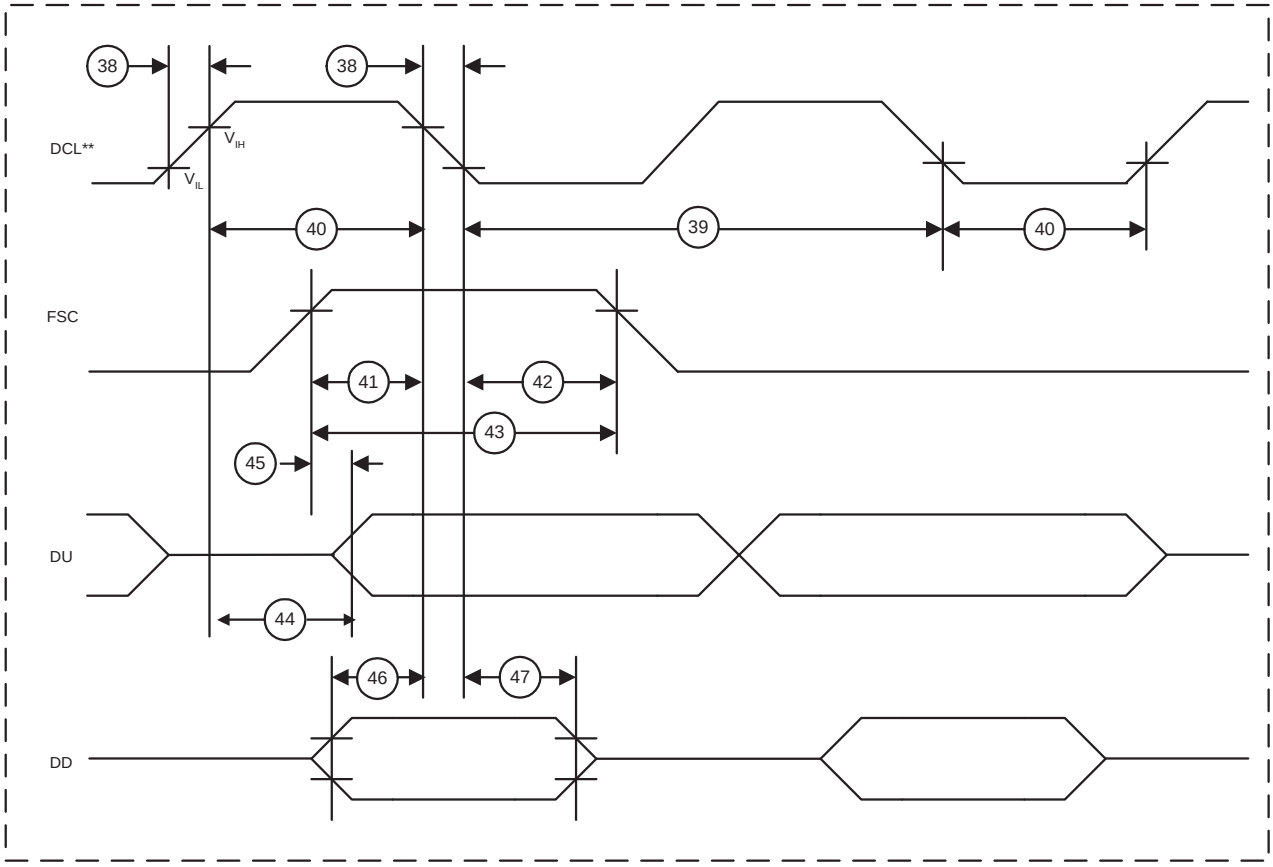



**Figure 42. 2.048 MHz DCL Operation**



## Switcher Output Timing

(See Figure 43 for the SWOUTY, SWOUTZ timing diagram, and note Note 5.)

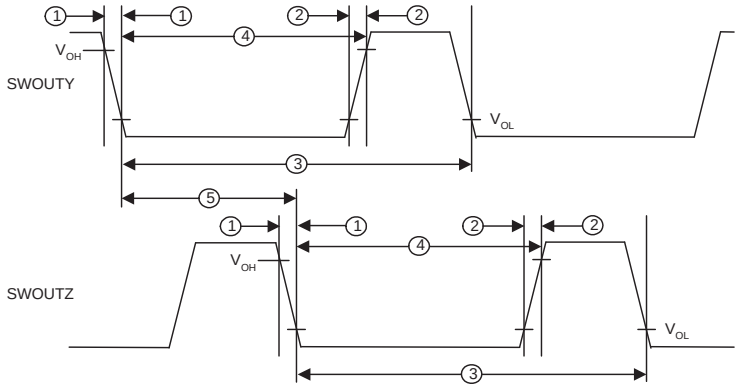
| No. | Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Tfall | Output Fall Time | | 1 | 10 | ns | Note 1. |
| 2 | Trise | Output Rise Time | | 1 | 10 | ns | Note 1. |
| 3LP | TPeriod | Period for Low Power Mode | | 20.833 | | µs | Note 2.,Note 5. |
| 4LP | Tmax | Max On-Time for Low Power Mode | | 1.830 | 1.845 | µs | Note 2.,Note 5. |
| 3MP | TPeriod | Period for Medium Power Mode | | 10.417 | | µs | Note 3.,Note 5. |
| 4MP | Tmax | Max On-Time for Medium Power Mode | | 1.830 | 1.845 | µs | Note 3.,Note 5. |
| 3HP | TPeriod | Period for High Power Mode | | 2.604 | | µs | Note 4.,Note 5. |
| 4HP | Tmax | Max On-Time for High Power Mode | | 1.830 | 1.845 | µs | Note 4.,Note 5. |
| | Duty Cycle LP | Duty Cycle Low Power Mode | 0 | | 8.8 | % | Note 2.,Note 5. |
| | Duty Cycle MP | Duty Cycle Medium Power Mode | 0 | | 17.6 | % | Note 3.,Note 5. |
| | Duty Cycle HP | Duty Cycle High Power Mode | 0 | | 70.3 | % | Note 4.,Note 5. |
| 5 | Y to Z offset | Delay from SWOUTZ to SWOUTY on | | 1.302 | | µs | Note 4.,Note 5. |
| | | SWISY leading edge blanking period | | 120 | | ns | |

***Notes:***

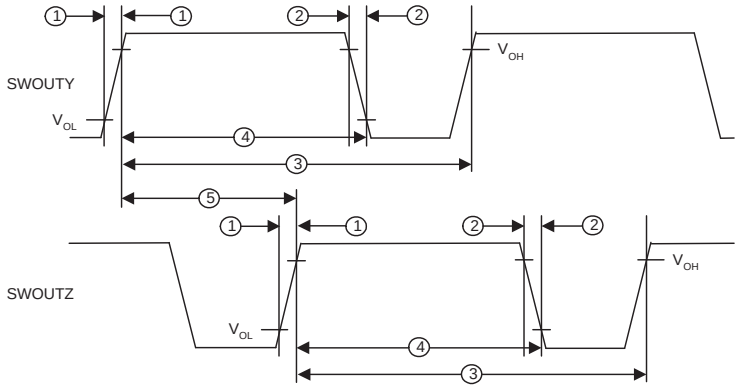
1. *Measured with an RC load on SWOUTY of 330 pF in series with 180 Ω to ground.*
2. *Register E6/E7h Write/Read Switching Regulator Control is loaded with low power mode 01h.*
3. *Register E6/E7h Write/Read Switching Regulator Control is loaded with medium power mode 02h.*
4. *Register E6/E7h Write/Read Switching Regulator Control is loaded with high power mode 03h*
5. *Timing values assume SWFS[1:0] = 00b in E4/E5h Write/Read Switching Regulator Parameters. Stated periods and on times scale inversely with frequency selected.*

**Figure 43. Switcher Output Waveform SWOUTY, SWOUTZ**

**Flyback Mode (Representative of High Power setting)**




**Inverting Buckboost Mode (Representative of High Power setting)**



## APPLICATIONS

The VE8820 VoicePort chipset implements a complete dual channel interface between a digital highway (PCM/MPI or GCI) and two telephone lines. The VE8820 chipset provides access to time-critical information, such as off/on-hook and ring trip, via a single read operation. When various country or transmission requirements must be met, the VE8820 chipset can be reprogrammed to meet the required DC feed, ringing and transmission characteristics.

Several VE8820 chipsets can be tied together in one bus interfacing to a common PCM or GCI interface. In MPI mode, the VE8820 chipset is controlled through the microprocessor interface.

## Application Circuit

**Figure 44. VE8820 Chipset Application Circuit**

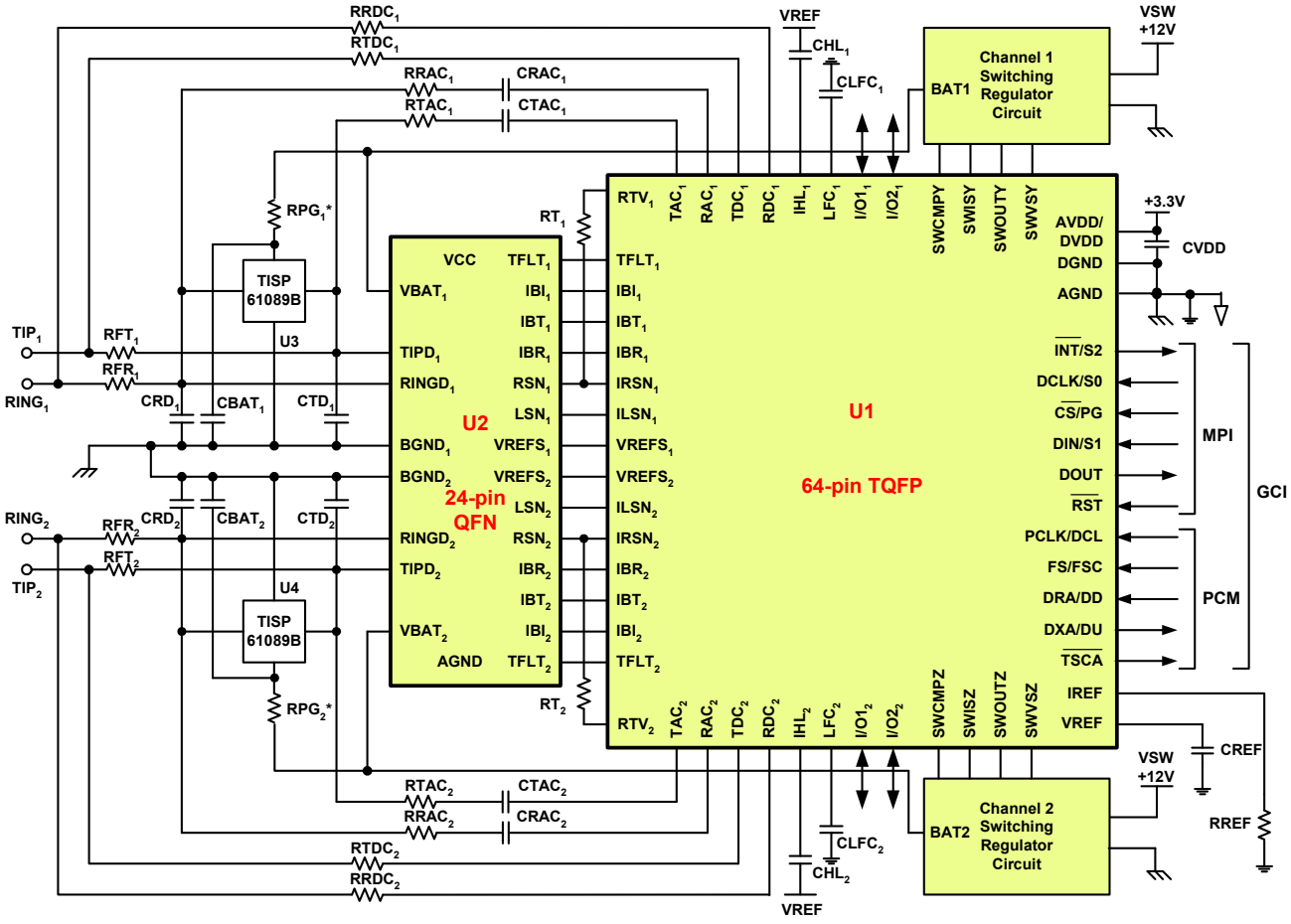
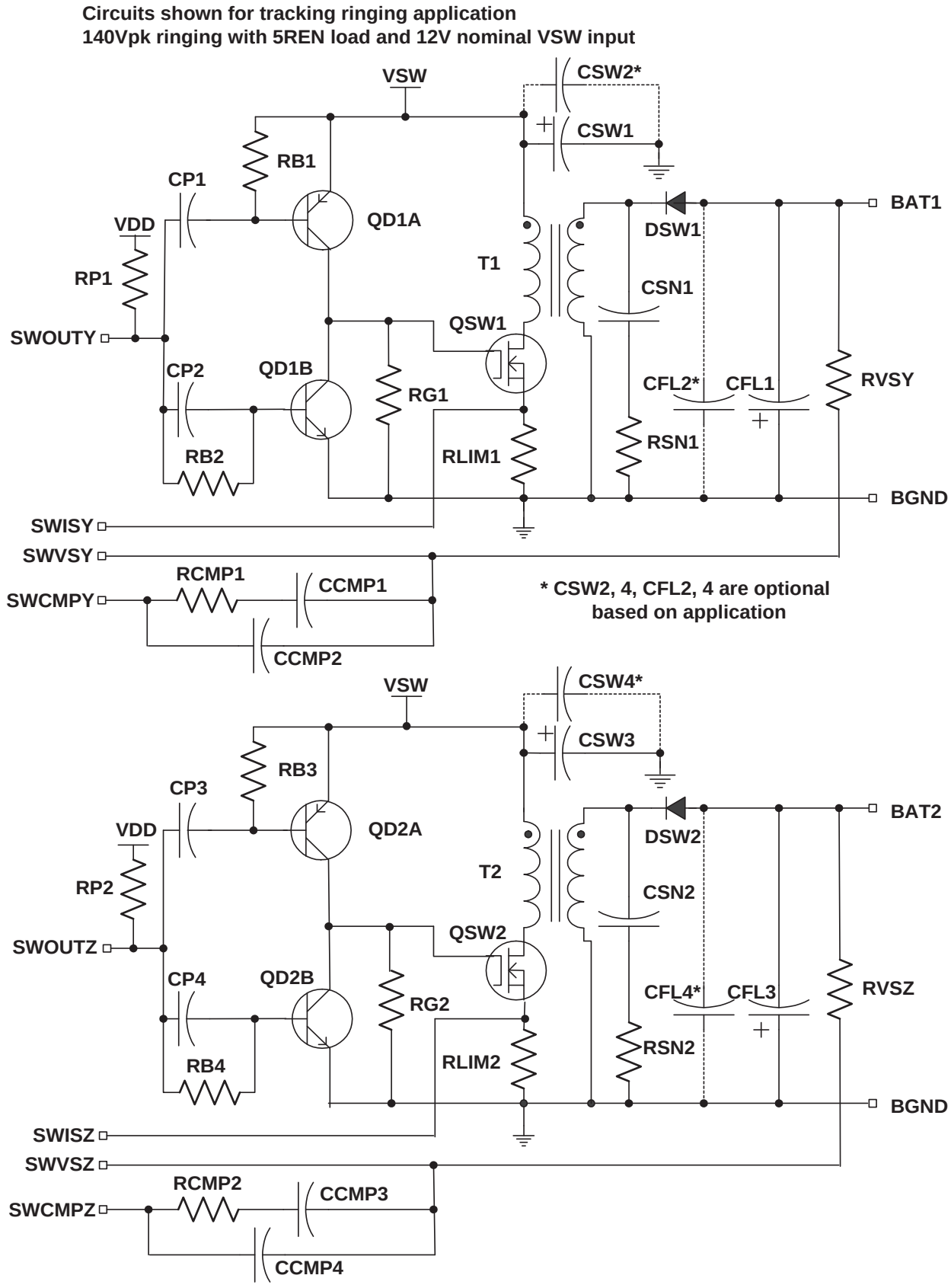


**Figure 45. VE8820 Switching Regulator Circuit**



## VE8820 VoicePort™ Chipset Parts List

The following list defines the parts and part values required to meet target specifications based on the application circuits shown in Figure 44 and Figure 45.

*For an application using the VE8820 chipset with lower voltage ringing, some device ratings may be reduced, and smaller package sizes used. $R_{LIM}$ 1/4 W, $R_{VS}$ 1/16 W, and 200-V rated components are reduced, depending on the selected ringing voltage.

** $R_{PG}$ is not required for GR1089 intra-building applications or if fixed regulator mode is always used for ringing; for these applications, connect the gate of the protector directly to $VBAT_i$.

| Item | Quantity | Type | Value | Tol. | Rating | Comments |
|---|---|---|---|---|---|---|
| $C_{BAT1}$, $C_{BAT2}$ | 2 | Capacitor | 0.1 µF | 10% | 200 V* | GMC31X7R104K200NT 1206 |
| $C_{CMP1}$, $C_{CMP3}$ | 2 | Capacitor X7R | 820 pF | 10% | 10 V | Panasonic ECJ-0EB1E821K 0402 |
| $C_{CMP2}$, $C_{CMP4}$ | 2 | Capacitor NPO | 4 pF | 10% | 10 V | Panasonic ECJ-1VC1H040D 0402 |
| $C_{FL1}$, $C_{FL3}$ | 2 | Capacitor | 2.2 µF | 10% | 200 V* | UCC THCR70E2D225MT 1825 |
| $C_{HL1}$, $C_{HL2}$ $C_{LFC1}$, $C_{LFC2}$ | 4 | Capacitor | 4.7 µF | 20% | 6.3 V | Panasonic ECJ-1VB0J475M 0603 |
| $C_{P1}$,$C_{P2}$, $C_{P3}$,$C_{P4}$ | 4 | Capacitor X7R | 220 pF | 10% | 25 V | Yageo 06032R221K9B20D 0603 |
| $C_{RAC1}$,$C_{RAC2}$, $C_{TAC1}$,$C_{TAC2}$ | 4 | Capacitor | 0.068 µF | 10% | 200 V* | Kemet 12062C683KAT2A 1206 |
| $C_{RD}$, $C_{TD}$ | 2 | Capacitor | 0.22 µF | 10% | 200 V* | Kemet 08052C223KAT2A 0805 |
| $C_{REF}$ | 1 | Capacitor X5R | 10µF | 10% | 6.3 V | Panasonic ECJ-2FB0J106M |
| $C_{SN1}$,$C_{SN2}$ | 2 | Capacitor COG | 47 pF | 10% | 200 V | Kemet C0603C470K2RAC 0603 |
| $C_{SW1}$, $C_{SW2}$ | 1 | Capacitor Low ESR | 100 µF | 20% | 25 V | Panasonic EEU-FC1E101S TH |
| $C_{VDD1,2,3}$ | 3 | Capacitor | 0.1 µF | 20% | 10 V | Panasonic ECJ-1VB1C104K 0603 |
| $D_{SW1}$, $D_{SW2}$ | 2 | Diode | Ultra Fast | <50 nS | 1 A/200 V | On Semi MURS120DICT-ND |
| $Q_{D1}$, $Q_{D2}$ | 2 | Dual transistor | 100mA | | 40V | On Semi MBT3946DW1T1LRG |
| $Q_{SW1}$, $Q_{SW2}$ | 2 | MOSFET | 170 mΩ | 9 A | 60 V* | Fairchild NDT3055 SOT-223 |
| $R_{B1}$, $R_{B3}$ | 2 | Resistor | 560 Ω | 5% | 1/16 W | Panasonic ERJ-2GEJ561X 0402 |
| $R_{B2}$, $R_{B4}$, $R_{G1}$, $R_{G2}$, $R_{P1}$, $R_{P2}$ | 6 | Resistor | 10 kΩ | 5% | 1/16 W | Panasonic ERJ-2GEJ103X 0402 |
| $R_{CMP1}$, $R_{CMP2}$ | 2 | Resistor | 1.0 MΩ | 5% | 1/16 W | Panasonic ERJ-2GEJ105X 0402 |
| $R_{FT1}$, $R_{FT2}$, $R_{FR1}$, $R_{FR2}$ | 4 | PTC | 50 Ω | | 250 V | Asiacom MZ2L-50R |
| $R_{LIM1}$, $R_{LIM2}$ | 2 | Resistor | 0.020 Ω | 1% | 1/4 W* | Panasonic ERJ-14KF020U 1210 |
| $R_{PG}$** | 2 | Resistor | 4.75 kΩ | 1% | 1/4 W | Panasonic ERJ-8ENF4751V 1206 |
| $R_{RAC1}$, $R_{RAC2}$, $R_{TAC1}$, $R_{TAC2}$ | 4 | Resistor | 3.01 kΩ | 1% | 1/10 W | Panasonic ERJ-6ENF3011V 0805 |
| $R_{REF}$ | 1 | Resistor | 75 kΩ | 1% | 1/16 W | Panasonic ERJ-2RKF7502X 0402 |
| $R_{RDC1}$, $R_{RDC2}$, $R_{TDC1}$, $R_{TDC2}$, $R_{VSY}$, $R_{VSZ}$ | 6 | Resistor | 402 kΩ | 1% | 1/10 W | Panasonic ERJ-6ENF4023V 0805 |
| $R_{SN1}$, $R_{SN2}$ | 2 | Resistor | 1.0 kΩ | 5% | 1/8 W | Panasonic ERJ-6GEYJ102V 0805 |
| $R_{T1}$, $R_{T2}$ | 2 | Resistor | 47.5 kΩ | 1% | 1/16 W | Panasonic ERJ-2RKF4752X 0402 |
| $T_1$, $T_2$ | 2 | Flyback Transformer | | | | Sumida C8100 or CoEv MGPTWT-00113 |

| Item | Quantity | Type | Value | Tol. | Rating | Comments |
|---|---|---|---|---|---|---|
| U1 | 1 | Dual VoicePort SLAC device | | | | Le88506 |
| U2 | 1 | Dual VoicePort SLIC device | | | | Le88830 |
| U3, U4 | 2 | Protector | | | 170 V | TISP61089BDR |

# COMMAND DESCRIPTION AND FORMATS

## Command Field Summary

A microprocessor can program and control the VE8820 device using the MPI or GCI. Data programmed previously can be read out for verification. See *Detailed Descriptions Of Commands*, on page 69 for the channel and global chip parameters assigned.

# MPI DESCRIPTION

If desired, multiple voice channel data can be programmed simultaneously with identical information by setting multiple Channel Enable bits. Channel Enable bits are contained in the Channel Enable register and written or read using MPI Command 4A/4Bh. If multiple Channel Enable bits are set for a read operation, only voice data from the first enabled channel will be read. Other functions within the device are accessible on a global basis independent of the setting of the Channel Enable bits.

The MPI consists of a serial data input (DIN) a data output (DOUT), a data clock (DCLK), and a chip select ($\overline{CS}$). The scope of the commands can be either Global or Voice Channel specific, as indicated in the *Summary of Commands*, on page 68. Access to the Voice Channel commands are controlled by the voice Channel Enable bits (EC1 and EC2) in the *4A/4Bh Write/Read Channel Enable and Operating Mode Register*, on page 71. The serial input consists of 8-bit commands that can be followed by additional bytes of input data, or by the VE8820 device sending out bytes of data. All data input and output is MSB (D7) first and LSB (D0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going High for at least a minimum off period before the next byte is read or written. Only a single channel should be enabled during read commands.

All commands that require additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of $\overline{CS}$). All unused bits must be programmed as 0 (unless otherwise noted) to ensure compatibility with future parts. All commands that are followed by output data will cause the device to output data for the next N transitions of $\overline{CS}$ going Low. The VE8820 device will not accept any commands until all the data has been shifted out. The output values of unused bits are not specified.

An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the $\overline{CS}$ lines are held in the High state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK can be run to a number of VE8820 devices, and the individual $\overline{CS}$ lines will select the appropriate device to access. Between command sequences, DCLK can stay in the High state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. Between bytes of a multibyte read or write command sequence, DCLK can also stay in the High state indefinitely. DCLK can stay in the Low state indefinitely with no loss of internal control information, provided the $\overline{CS}$ line remains at a High level.

If a low period of $\overline{CS}$ contains less than 8 positive DCLK transitions, it is ignored. If it contains 8 to 15 positive transitions, only the last 8 transitions matter. If it contains 16 or more positive transitions, a hardware reset in the part occurs. If the chip is in the middle of a read sequence when $\overline{CS}$ goes Low, data will be present at the DOUT pin even if DCLK has no activity.

## SUMMARY OF COMMANDS

| Hex* | Description | Scope | Page # |
|---|---|---|---|
| 02h | Software Reset | Channel | page 69 |
| 04h | Hardware Reset | Global | page 69 |
| 06h | No Operation | Global | page 69 |
| 40/41h | Write/Read Transmit Time Slot | Channel | page 69 |
| 42/43h | Write/Read Receive Time Slot | Channel | page 70 |
| 44/45h | Write/Read Transmit and Receive Clock Slot and Transmit Clock Edge | Global | page 70 |
| 46/47h | Write/Read Device Configuration Register | Global | page 70 |
| 4A/4Bh | Write/Read Channel Enable & Operating Mode Register | Global | page 71 |
| 4D/4Fh | Read Signaling Register | Global | page 72 |
| 50/51h | Write/Read Voice Path Gains | Channel | page 74 |
| 52/53h | Write/Read Input/Output Data Register | Channel | page 74 |
| 54/55h | Write/Read Input/Output Direction Register | Channel | page 75 |
| 56/57h | Write/Read System State | Channel | page 75 |
| 5E/5Fh | Write/Read Device Mode Register | Global | page 76 |
| 60/61h | Write/Read Operating Functions | Channel | page 77 |
| 68/69h | Write/Read System State Configuration | Channel | page 78 |
| 6C/6Dh | Write/Read Interrupt Mask Register | Global | page 79 |
| 70/71h | Write/Read Operating Conditions | Channel | page 79 |
| 73h | Read Revision and Product Code Number (RCN, PCN)) | Global | page 80 |
| 80/81h | Write/Read GX Filter Coefficients | Channel | page 80 |
| 82/83h | Write/Read GR Filter Coefficients | Channel | page 80 |
| 86/87h | Write/Read B Filter FIR Coefficients | Channel | page 81 |
| 88/89h | Write/Read X Filter Coefficients | Channel | page 82 |
| 8A/8Bh | Write/Read R Filter Coefficients | Channel | page 83 |
| 96/97h | Write/Read B Filter IIR Coefficients | Channel | page 84 |
| 98/99h | Write/Read Z Filter FIR Coefficients | Channel | page 84 |
| 9A/9Bh | Write/Read Z Filter IIR Coefficients | Channel | page 84 |
| A6/A7h | Write/Read Converter Configuration | Channel | page 85 |
| C2/C3h | Write/Read Loop Supervision Parameters | Channel | page 87 |
| C6/C7h | Write/Read DC Feed Parameters | Channel | page 87 |
| CA/CBh | Write/Read Digital Impedance Scaling Network (DISN) | Channel | page 88 |
| CDh | Read Transmit PCM/Test Data | Channel | page 88 |
| CFh | Read Test Data FIFO | Channel | page 89 |
| D0/D1h | Write/Read Metering Parameters | Channel | page 90 |
| D2/D3h | Write/Read Signal Generator A, B and Bias Parameters | Channel | page 91 |
| D4/D5h | Write/Read Signal Generator C and D Parameters | Channel | page 93 |
| DE/DFh | Write/Read Signal Generator Control | Channel | page 94 |
| E0/E1h | Write/Read Cadence Timer | Channel | page 95 |
| E2/E3h | Write/Read Caller Identification Number Data | Channel | page 95 |
| E4/E5h | Write/Read Switching Regulator Parameters | Global | page 96 |
| E6/E7h | Write/Read Switching Regulator Control | Global | page 97 |
| E8/E9h | Write/Read Battery Calibration Register | Channel | page 98 |
| EA/EBh | Write/Read Caller Identification Number Parameters | Channel | page 99 |
| FC/FDh | Write/Read DC Calibration Register | Channel | page 100 |

*Note:*

**All codes not listed are reserved by Microsemi and should not be used.*

## DETAILED DESCRIPTIONS OF COMMANDS

This section details each command used by the VE8820 device. The command is shown, along with the format of any additional data bytes that follow. Unused bits are indicated by “RSVD”; 0’s should be written to these bits (unless otherwise noted), but 0’s are not guaranteed when they are read.

In all commands:

R/$\overline{W}$ = 0: Write

R/$\overline{W}$ = 1: Read

*Default field values are marked by an asterisk. A hardware reset forces the default values.

### 02h Software Reset

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 02h | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

This command only operates on the channels selected by the Channel Enable Register and it does not change clock slots, time slots or global chip parameters. The selected channels will be put into the Disconnect state as a result of a Software reset unless that channel is in the Shutdown state in which case it will stay in the Shutdown state.

### 04h Hardware Reset

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 04h | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

Hardware reset is equivalent to pulling the $\overline{RST}$ pin on the device Low.
This command does not depend on the state of the Channel Enable Register. A Hardware reset will put all channels into the Shutdown state.

*Note:*
*The action of a hardware reset is described in the section on operating the VE8820 device.*

### 06h No Operation

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 06h | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

### 40/41h Write/Read Transmit Time Slot

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 40h R: 41h | 0 | 1 | 0 | 0 | 0 | 0 | 0 | R/$\overline{W}$ |
| I/O Data | RSVD | TTS6 | TTS5 | TTS4 | TTS3 | TTS2 | TTS1 | TTS0 |

TTS[6:0]:Transmit Time Slot

0–127: Time Slot Number (TTS0 is LSB, TTS6 is MSB)

This command applies to PCM mode only. Its contents are ignored in GCI mode.

Power Up and Hardware Reset ($\overline{RST}$) Value = 00h for Channel 1.

Power Up and Hardware Reset ($\overline{RST}$) Value = 01h for Channel 2.

### 42/43h Write/Read Receive Time Slot

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 42h R: 43h | 0 | 1 | 0 | 0 | 0 | 0 | 1 | R/$\overline{W}$ |
| I/O Data | RSVD | RTS6 | RTS5 | RTS4 | RTS3 | RTS2 | RTS1 | RTS0 |

RTS[6:0]:Receive Time Slot

0–127: Time Slot Number (RTS0 is LSB, RTS6 is MSB)

This command applies to PCM mode only. Its contents are ignored in GCI mode.

Power Up and Hardware Reset ($\overline{RST}$) Value = 00h for Channel 1.

Power Up and Hardware Reset ($\overline{RST}$) Value = 01h for Channel 2.

### 44/45h Write/Read Transmit and Receive Clock Slot and Transmit Clock Edge

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 44h R: 45h | 0 | 1 | 0 | 0 | 0 | 1 | 0 | R/$\overline{W}$ |
| I/O Data | RSVD | XE | RCS2 | RCS1 | RCS0 | TCS2 | TCS1 | TCS0 |

XE Transmit Edge

0*: Transmit changes on negative edge of PCLK
1: Transmit changes on positive edge of PCLK

RCS[2:0]:Receive Clock Slot

0*–7: Receive Clock Slot number

TCS[2:0]:Transmit Clock Slot

0*–7: Transmit Clock Slot number

This command does not depend on the state of the Channel Enable Register.
This command applies to PCM mode only. Its contents are ignored in GCI mode.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

### 46/47h Write/Read Device Configuration Register

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 46h R: 47h | 0 | 1 | 0 | 0 | 0 | 1 | 1 | R/$\overline{W}$ |
| I/O Data | INTM | RSVD | SMODE | RSVD | CSEL3 | CSEL2 | CSEL1 | CSEL0 |

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

INTM: Interrupt Mode

0: CMOS-compatible output
1*: Open drain output

SMODE:PCM Signaling Mode

0*: No signaling on PCM highway
1: Signaling on PCM highway

The PCM clock frequency can be selected by CSEL. The PCLK frequency selection affects all channels.

CSEL[3:0]:PCM Clock Frequency

| | |
|---|---|
| 0000 | 1.536 MHz |
| 0001 | 1.544 MHz |
| 0010 | 2.048 MHz |
| 0011 | 1.024 MHz |
| 0100 | 3.072 MHz |
| 0101 | 3.088 MHz |
| 0110 | 4.096 MHz |
| 0111 | Reserved |
| 1000 | 6.144 MHz |
| 1001 | 6.176 MHz |
| 1010* | 8.192 MHz |
| 1011 | Reserved |
| 1100 | Reserved |
| 1101 | Reserved |
| 1110 | Reserved |
| 1111 | Reserved |

This command does not depend on the state of the Channel Enable Register.
This command applies to PCM mode only. Its contents are ignored in GCI mode.

In the absence of external PCLK, the on chip master clock will slow down to it's minimum operating frequency which will be in the range of 1/5 - 1/2 of its normal operating frequency. If the ACFS bit is reset in command *68/69h Write/Read System State Configuration*, on page 78 then this enables a low power system standby state to be implemented where supervision functions are still operational and interrupts can be generated in the absence of any system clocks.

* Power Up and Hardware Reset ($\overline{RST}$) Value = 8Ah.

**4A/4Bh Write/Read Channel Enable and Operating Mode Register**

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 4Ah R: 4Bh | 0 | 1 | 0 | 0 | 1 | 0 | 1 | R/$\overline{W}$ |
| I/O Data | RSVD | RSVD | WBAND | RSVD | RSVD | RSVD | EC2 | EC1 |

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

WBAND:Wideband Codec Mode (Global Parameter)

0*: Normal Codec Mode. The codec has a 3.4 kHz bandwidth.
1: Wideband Codec Mode. The codec has a 7.0 kHz bandwidth.

EC2: Channel Enable 2

0: Disabled, channel 2 cannot receive commands
1*: Enabled, channel 2 can receive commands

EC1: Channel Enable 1

0: Disabled, channel 1 cannot receive commands
1*: Enabled, channel 1 can receive commands

* Power Up and Hardware Reset ($\overline{RST}$) Value = 03h.

### 4D/4Fh Read Signaling Register

This register reads signaling data with (4F) or without (4D) clearing any corresponding interrupt.

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| R: 4Dh R: 4Fh | 0 | 1 | 0 | 0 | 1 | 1 | x | 1 |
| I/O Data Byte 1 | CFAIL | OCALMY | $TEMPA_1$ | $IO2_1$ | $CAD_1$ | $CID_1$ | $GNK_1$ | $HOOK_1$ |
| I/O Data Byte 2 | DAT | OCALMZ | $TEMPA_2$ | $IO2_2$ | $CAD_2$ | $CID_2$ | $GNK_2$ | $HOOK_2$ |

The read without clearing interrupt command (4D) allows signaling bits that are masked (see *6C/6Dh Write/Read Interrupt Mask Register*, on page 79) to be monitored via polling the signaling register, while other bits that are unmasked are serviced in response to interrupts.

An interrupt is generated by pulling the $\overline{INT}$ pin low, or setting the SLCX bit in the upstream GCI SC channel, whenever any unmasked bit in the signaling register changes. There are two types of interrupt:

Type A interrupts are generated on both edge transitions and present the current status of the signal. When the signal state changes, the new state is locked in the signaling register, and an interrupt is generated. When the interrupt is cleared by reading the status in the signaling register (4Fh), the status corresponding to the interrupt is not necessarily cleared. A new interrupt will be generated only when a new change occurs.
CFAIL, OCALMY, OCALMZ, $TEMPA_i$, $IO2_i$, $GNK_i$, and $HOOK_i$ are type A interrupts

Type B interrupts are generated when a specific event occurs. The corresponding signal is set to 1 and an interrupt is generated. When the read signaling register and clear interrupt (4Fh) command is issued, the interrupt is cleared and the signal is reset.
$CAD_i$ and $CID_i$ are type B interrupts.

Other status bits may change while an interrupt is pending. In this case, an additional interrupt is not generated if the new status is reported when the register is read. If the bit that caused the original interrupt has changed after it was latched in the signaling register but before the interrupt was cleared, the latched value will be read and a new interrupt with the new value (which will be latched) will be generated immediately after the interrupt is cleared.

The behavior of the various signals in this register depends on the contents of *C2/C3h Write/Read Loop Supervision Parameters*, on page 87 where thresholds and debounce periods are set.

This command does not depend on the state of the Channel Enable register

DAT: Converter data.

0: No new data is available in *CDh Read Transmit PCM/Test Data*, on page 88
1: New data is available in *CDh Read Transmit PCM/Test Data*, on page 88

When unmasked by the ATI bit in the *A6/A7h Write/Read Converter Configuration*, on page 85 the DAT interrupt will be asserted at the time new data is ready to be read from *CDh Read Transmit PCM/Test Data*, on page 88. The interrupt pin is returned to a high level after 54 μsec (26 μs in wideband mode). When the ATI bit is masked the DAT status is not reported.

CFAIL: Clock Fail

0: The internal clock is synchronized to frame sync.
1: The internal clock is not synchronized to frame sync.

When clock fail is set, the data path is cleared for all channels.

OCALMY:Switching regulator Y overcurrent indicator.

0*: Switching Regulator Y working properly.
1: Switching regulator Y has an overcurrent/power fault problem.

The OCALMY bit is an indicator of a continuing over-current condition. This indicates to the user's system that a fault in switching regulator Y is probably occurring. When the ABAT bit is zero, the switcher is automatically shut off and the system state is set to shutdown.

OCALMZ:Switching regulator Z over current indicator.

0*: Switching Regulator Z working properly.
1: Switching regulator Z has an overcurrent/power fault problem.

The OCALMZ bit is an indicator of a continuing over-current condition. This indicates to the user's system that a fault in switching regulator Z is probably occurring. When the ABAT bit is zero, the switcher is automatically shut off and the system state is set to shutdown.

TEMPA:Thermal Fault Alarm

0*: High voltage line driver within safe operating temperature region
1: High voltage line driver at unsafe operating temperature and in thermal shutdown.
This bit is not updated when the system is in disconnect.

IO2: Input 2 Status. The input value at $IO2_1$ or $IO2_2$

0: $IO2_i$ input is low
1: $IO2_i$ input is high

CAD: Cadencer status when masked or interrupt if unmasked

0: Cadence timer is in the programmed on period (masked)
1: Cadence timer is in the programmed off period (masked)

0: Cadence interrupt has not occurred (unmasked).
1: Cadence interrupt has occurred (unmasked)
Cadencer has completed the programmed on period

CID: Caller ID Buffer Ready

0: The CID buffer is full
1*: The CID buffer is ready
If unmasked, an interrupt is only generated when the CID buffer becomes ready

GNK: Ground-key or Ground Fault detection.

0: No Ground Key (Longitudinal current less than TGK for longer than DGNK)
1: Ground Key detected (Longitudinal current greater than TGK for longer than DGNK)

HOOK: Hook switch, Ground Start or Ring Trip event

0: On hook
1: Off hook

This bit signals events based on the system state illustrated in the table below.

| State | Hook Interrupt Event |
|---|---|
| Active | On hook (Metallic current less than TSH for longer than DSH<br>Off hook (Metallic current greater than TSH for longer than DSH) |
| Tip Open | On hook (Metallic current less than TSH for longer than DSH<br>Off hook (Metallic current greater than TSH for longer than DSH) |
| Ring Open | On hook (Metallic current less than TSH for longer than DSH<br>Off hook (Metallic current greater than TSH for longer than DSH) |
| Balanced Ringing or Unbalanced Ringing | On hook (Metallic current less than RTTH for two ring periods)<br>Off hook (Metallic current greater than RTTH for two ring periods) |

* Power Up and Hardware Reset ($\overline{RST}$) Value = 0000

### 50/51h Write/Read Voice Path Gains

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 50h R: 51h | 0 | 1 | 0 | 1 | 0 | 0 | 0 | R/$\overline{W}$ |
| I/O Data | RSVD | AX | AR1 | AR0 | DRL | RSVD | RSVD | RSVD |

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

AX: Transmit Analog Gain

0*: 0 dB gain
1: 6.02 dB gain

AR[1:0]:Receive Analog Loss

00*: 0 dB loss
01: 6.02 dB loss
10: 6.02 dB gain
11: RSVD

DRL: Digital Receive Loss. This mode is used in high current metering applications in combination with the 6.02 dB AR gain.

0*: No digital receive loss
1: A 6.02 dB loss is inserted in the voice receive path.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

### 52/53h Write/Read Input/Output Data Register

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 52h R: 53h | 0 | 1 | 0 | 1 | 0 | 0 | 1 | R/$\overline{W}$ |
| I/O Data | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | IO2 | IO1 |

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

IO1-IO2:Value at general purpose IO pins.

This register provides both data input and data output functions per channel depending on the setting of the corresponding IOD bits in *54/55h Write/Read Input/Output Direction Register*. The data written appears latched on the I/O pin. In input mode, the logic state of the I/O pin is read. In output mode, the state of the I/O pin is read. A logic 1 written to the data register will cause the output to be logic 1. If the IOD1x bits = 10, then the I/O1 pin is an open drain output capable of driving a relay. A logic 1 written to the data register will cause the output to pull low (current flows in the open drain transistor). In this case, a read of IO1 will read the I/O pin voltage and invert the outcome. Thus, in open drain, if the pin voltage is logic low, the system will read back a one.

### 54/55h Write/Read Input/Output Direction Register

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 54h R: 55h | 0 | 1 | 0 | 1 | 0 | 1 | 0 | R/$\overline{W}$ |
| I/O Data | RSVD | RSVD | RSVD | RSVD | RSVD | IOD2 | IOD12 | IOD11 |

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

IOD1[2:1]:Direction of the IO1 pins (input or output)

00*: IO1 is an input
01: IO1 is an output
10: IO1 is open drain
11: Reserved

IOD2: Direction of the IO2 pins (input or output)

0*: IOx is an input
1: IOx is an output

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

### 56/57h Write/Read System State

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 56h R: 57h | 0 | 1 | 0 | 1 | 0 | 1 | 1 | R/$\overline{W}$ |
| I/O Data | REX | METR | ACT | POLNR | SS3 | SS2 | SS1 | SS0 |

REX: Ringing Status. This bit is read-only. Writes to this bit have no effect.

0*: System is not in ring exit state.
1: System is in ring exit or ringing state.
When the system is in ringing and the user exits to a new state, the state register will reflect the new state that was last written by the user. However, the system may not change immediately to the new state, but may wait for a zero cross, in order to minimizes line transients. During this period, REX will be 1 indicating the system is waiting for a zero cross. REX will also be 1 during ringing.

METR: Metering

0*: Metering off
1: Metering on. Metering will stay on for the duration specified in the MTRDR parameter of command *D0/D1h Write/Read Metering Parameters*, on page 90 and METR will be reset to zero at the end of this time, terminating the meter pulse.

ACT: Activate Codec

0*: Codec deactivated
1: Codec Activated

No valid PCM data is transmitted until after the third FS pulse is received after the ACT bit is set.

POLNR:Normal or Reverse Polarity feed

0*: Normal Polarity feed - TIPD more positive than RINGD
1: Reverse Polarity feed - RINGD more positive than TIPD

SS[3:0]:System State is defined by the table below. These states can be switched between automatically by the VE8820 device if the ASSC bit is set. The table lists the default values of the states when the ASSC bit is set. Modifying other bits in this register will subsequently alter these states. Writing a new value to SS will change the system state.

| SS3 | SS2 | SS1 | SS0 | Mode |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disconnect |
| 0 | 0 | 0 | 1 | Tip Open |
| 0 | 0 | 1 | 0 | Ring Open |
| 0 | 0 | 1 | 1 | Active |
| 0 | 1 | 0 | 0 | Idle |
| 0 | 1 | 0 | 1 | RSVD |
| 0 | 1 | 1 | 0 | RSVD |
| 0 | 1 | 1 | 1 | Balanced Ringing |
| 1 | 0 | 0 | 0 | Low Gain |
| 1 | 0 | 0 | 1 | RSVD |
| 1 | 0 | 1 | 0 | Unbalanced Ringing |
| 1 | 0 | 1 | 1 | RSVD |
| 1 | 1 | 0 | 0 | RSVD |
| 1 | 1 | 0 | 1 | RSVD |
| 1 | 1 | 1 | 0 | RSVD |
| 1* | 1* | 1* | 1* | Shutdown |

***Note:***

1. *Where there is a conflict on a write to this register between the System State (SS) and the other bits, the other bits take precedence.*
2. *Ringing uses signal generator A and the bias parameter to generate the ringing waveform.*

Power Up and Hardware Reset ($\overline{RST}$) Value = 0Fh

**5E/5Fh Write/Read Device Mode Register**

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 68h R: 69h | 0 | 1 | 1 | 0 | 1 | 0 | 0 | R/$\overline{W}$ |
| I/O Data | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | CBS | TDIM |

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

CBS: Channel Buffer Select
This bit only has significance when TDIM is set.

0*: The data reflected in the test data register and the test data buffer comes from channel 1. The interrupt refers to channel 1 data.

1: The data reflected in the test data register and the test data buffer comes from channel 2. The interrupt refers to channel 2 data.

TDIM: Test Data Interrupt Mode

0*: DAT status interrupt behaves as described in command *CDh Read Transmit PCM/Test Data*, on page 88.
The interrupt is generated after each new sample. The data rate set by the DRAT field in the Converter Configuration Register affects the data rate written to the PCM/Test Data register, the data buffer, and the PCM highway.

1: DAT status interrupt behaves as described in command *CFh Read Test Data Buffer, on page 89*.
This bit changes the way the test data interrupt works. By default the interrupt is generated after each new sample. This is useful when reading a single sample from the Transmit Data Register. If this bit is set to 1, the interrupt indicates that the Test data buffer has data in it. The data rate set by the DRAT field in the Converter Configuration Register affects only the data rate written to the PCM/Test Data register and the data buffer. The PCM highway data is output at 8Khz.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00

**60/61h Write/Read Operating Functions**

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 60h R: 61h | 0 | 1 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ |
| I/O Data | C/L | A/µ | EGR | EGX | EX | ER | EZ | EB |

C/L: Linear Code

0*: Compressed coding
1: Linear coding

A/µ: A-law or µ-law

0*: A-law coding
1: µ-law coding

EGR: GR Filter

0*: Default GR filter enabled
1: Programmed GR filter enabled

EGX: GX Filter

0*: Default GX filter enabled
1: Programmed GX filter enabled

EX: X Filter

0*: Default X filter enabled
1: Programmed X filter enabled

ER: R Filter

0*: Default R filter enabled
1: Programmed R filter enabled

EZ: Z Filter

0*: Default Z filter enabled
1: Programmed Z filter enabled

EB: B Filter

0*: Default B filter enabled
1: Programmed B filter enabled

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

### 68/69h Write/Read System State Configuration

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 68h R: 69h | 0 | 1 | 1 | 0 | 1 | 0 | 0 | R/$\overline{W}$ |
| I/O Data | RSVD | RSVD | ACFS | ATFS | ZXR | SPR | ASSC | ABAT |

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

ACFS: Automatic Clock Fail Switching

0: Automatic Clock Fail switching disabled

1*: Automatic Clock Fail switching enabled

When a Clock Fail alarm is detected and persists for between 0.5 ms and 3 ms the channel will switch to the Shutdown state.

ATFS: Automatic Thermal Fault Switching

0*: Automatic thermal fault switching disabled

1: Automatic thermal fault switching enabled

The channel will switch to the Disconnect state when a high voltage line driver thermal fault alarm is detected.

See TEMPA bit description in command *4D/4Fh Read Signaling Register*, on page 72.

ZXR: Zero Cross Ringing Entry/Exit

0*: System will enter and exit the Ringing State smoothly by waiting for zero cross between the ringing waveform and the DC Tip-Ring voltage. This ensures a smooth transition between states and gives the switching regulator time to rise to an appropriate ringing voltage on ring entry.

1: System will enter and exit ringing immediately according to command *56/57h Write/Read System State*, on page 75.

SPR: Smooth Polarity Reversal

0*: Polarity reversals will be abrupt.

1: Polarity reversals will be smooth.

ASSC: Automatic System State Control

0*: Automatic system state switching enabled

System State will change due to the following supervision stimuli:
Hook in Idle will cause a transition to Active.
Hook due to ring trip will cause a transition from Ringing to Active
Hook due to ground start in Tip or Ring Open will cause a transition to Active
In all three cases, the resulting line polarity is defined by the POLNR bit
ACT will be updated appropriately

1: Automatic system state switching disabled

State changes only occur as a result of user commands

ABAT: Auto battery shutdown

0: Automatic switching regulator shutdown on over current alarm (OCALM in *4D/4Fh Read Signaling Register*, on page 72) disabled

1*: Automatic switching regulator shutdown on over current alarm enabled

*Power Up and Hardware Reset ($\overline{RST}$) Value = 21h.

### 6C/6Dh Write/Read Interrupt Mask Register

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 6Ch R: 6Dh | 0 | 1 | 1 | 0 | 1 | 1 | 0 | R/$\overline{W}$ |
| I/O Data Byte 1 | MCFAIL | MOCALMY | $MTEMPA_1$ | $MIO2_1$ | $MCAD_1$ | $MCID_1$ | $MGNK_1$ | $MHOOK_1$ |
| I/O Data Byte 2 | RSVD | MOCALMZ | $MTEMPA_2$ | $MIO2_2$ | $MCAD_2$ | $MCID_2$ | $MGNK_2$ | $MHOOK_2$ |

In the MPI mode, this register defines which signals can generate interrupts and be latched in the *4D/4Fh Read Signaling Register*, on page 72. In GCI mode, this register defines which signals can cause the SLCX bit to be set in the upstream signalling channel. In GCI mode, $MGNK_i$, $MHOOK_i$ should always be masked.

RSVD: Reserved for future use. Always write as 1, but 1 is not guaranteed when read.

Mx: Mask Interrupt/Signaling bits

0: Signal is NOT masked, change will generate an interrupt or set SLCX
1*: Signal is masked, a change does not cause an interrupt or set SLCX

This command does not depend on the state of the Channel Enable Register.

*Power Up and Hardware Reset ($\overline{RST}$) Value = FFFFh.

### 70/71h Write/Read Operating Conditions

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 70h R: 71h | 0 | 1 | 1 | 1 | 0 | 0 | 0 | R/$\overline{W}$ |
| I/O Data | CTP | CRP | HPF | LRG | RSVD | ILB | RSVD | TON |

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

CTP: Cutoff Transmit Path

0*: Transmit path connected
1: Transmit path cut off

CRP: Cutoff Receive Path

0*: Receive path connected
1: Receive path cutoff

HPF: High Pass Filter

0*: Transmit Highpass filters enabled
1: Transmit Highpass filters disabled

LRG: Lower Receive Gain

0*: 6-dB loss not inserted
1: 6-dB loss inserted

ILB: Interface Loopback

0*: TSA loopback disabled
1: TSA loopback enabled

TON: 1 kHz Receive Tone

0*: 1 kHz receive tone off
1: 1 kHz receive tone on

This tone is 2 Khz in wideband mode.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

### 73h Read Revision and Product Code Number (RCN,PCN)

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| R: 73h | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| Output Data Byte 1 | RCN7 | RCN6 | RCN5 | RCN4 | RCN3 | RCN2 | RCN1 | RCN0 |
| Output Data Byte 2 | PCN7 | PCN6 | PCN5 | PCN4 | PCN3 | PCN2 | PCN1 | PCN0 |

This command returns an 8-bit number (RCN) describing the revision number of the device and an 8-bit product code number indicating the VE880 series part number.

The revision code (RCN) of the Le88506 JA is 04h.

PCN: Product Code Number

BCh Le88506 device

This command does not depend on the state of the Channel Enable Register.

### 80/81h Write/Read GX Filter Coefficients

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 80h R: 81h | 1 | 0 | 0 | 0 | 0 | 0 | 0 | R/$\overline{W}$ |
| I/O Data Byte 1 | C40 | m40 | | | C30 | m30 | | |
| I/O Data Byte 2 | C20 | m20 | | | C10 | m10 | | |

Cxy = 0 or 1 in the command above corresponds to Cxy = +1 or −1, respectively, in the equation below.

The coefficient for the GX filter is defined as:

$$H_{GX} = 1 + (C10 \bullet 2^{-m10}\{1 + C20 \bullet 2^{-m20}[1 + C30 \bullet 2^{-m30}(1 + C40 \bullet 2^{-m40})]\}$$

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0190h ($H_{GX}$ = 1 (0 dB)).

*Note:*

*The default value is contained in a ROM register separate from the programmable coefficient RAM and the ROM register's default value can not be read. There is a filter enable bit in Operating Functions register to switch between the default and programmed values.*

### 82/83h Write/Read GR Filter Coefficients

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 82h R: 83h | 1 | 0 | 0 | 0 | 0 | 0 | 1 | R/$\overline{W}$ |
| I/O Data Byte 1 | C40 | m40 | | | C30 | m30 | | |
| I/O Data Byte 2 | C20 | m20 | | | C10 | m10 | | |

Cxy = 0 or 1 in the command above corresponds to Cxy = +1 or −1, respectively, in the equation below.

The coefficient for the GR filter is defined as:

$$H_{GR} = C10 \bullet 2^{-m10}\{1 + C20 \bullet 2^{-m20}[1 + C30 \bullet 2^{-m30}(1 + C40 \bullet 2^{-m40})]\}$$

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0111h ($H_{GR}$ = 1 (0 dB)).

See note under Command 80/81h on page 80

### 86/87h Write/Read B Filter FIR Coefficients

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 86h R: 87h | 1 | 0 | 0 | 0 | 0 | 1 | 1 | R/$\overline{W}$ |
| I/O Input Data Byte 1 | C32 | m32 | | | C22 | m22 | | |
| I/O Input Data Byte 2 | C12 | m12 | | | C33 | m33 | | |
| I/O Input Data Byte 3 | C23 | m23 | | | C13 | m13 | | |
| I/O Input Data Byte 4 | C34 | m34 | | | C24 | m24 | | |
| I/O Input Data Byte 5 | C14 | m14 | | | C35 | m35 | | |
| I/O Input Data Byte 6 | C25 | m25 | | | C15 | m15 | | |
| I/O Input Data Byte 7 | C36 | m36 | | | C26 | m26 | | |
| I/O Input Data Byte 8 | C16 | m16 | | | C37 | m37 | | |
| I/O Input Data Byte 9 | C27 | m27 | | | C17 | m17 | | |
| I/O Input Data Byte 10 | C38 | m38 | | | C28 | m28 | | |
| I/O Input Data Byte 11 | C18 | m18 | | | C39 | m39 | | |
| I/O Input Data Byte 12 | C29 | m29 | | | C19 | m19 | | |
| I/O Input Data Byte 13 | C310 | m310 | | | C210 | m210 | | |
| I/O Input Data Byte 14 | C110 | m110 | | | RSVD | RSVD | | |

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

Cxy = 0 or 1 in the command above corresponds to Cxy = +1 or –1, respectively, in the equation below.

The Z-transform equation for the B filter is defined as:

$$H_B(z) = B_2 \bullet z^{-2} + \ldots + B_9 \bullet z^{-9} + \frac{B_{10} \bullet z^{-10}}{1 - B_{11} \bullet z^{-1}}$$

Sample rate = 16 kHz

The coefficients for the FIR B section and the gain of the IIR B section are defined as:

For i = 2 to 10,

$$B_i = C1i \bullet 2^{-mli}[1 + C2i \bullet 2^{-m2i}(1 + C3i \bullet 2^{-m3i})]$$

The feedback coefficient of the IIR B section is defined as:

$$B_{11} = C111 \bullet 2^{-m111}\{1 + C211 \bullet 2^{-m211}[1 + C311 \bullet 2^{-m311}(1 + C411 \bullet 2^{-m411})]\}$$

Refer to Command *96/97h Write/Read B Filter IIR Coefficients*, on page 84 for programming of the $B_{11}$ coefficients.

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0900 9009 0090 0900 9009 0090 0900h

$$H_B(z) = 0$$

See note under Command 80/81h on page 80.

### 88/89h Write/Read X Filter Coefficients

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 88h R: 89h | 1 | 0 | 0 | 0 | 1 | 0 | 0 | R/$\overline{W}$ |
| I/O Input Data Byte 1 | C40 | m40 | | | C30 | m30 | | |
| I/O Input Data Byte 2 | C20 | m20 | | | C10 | m10 | | |
| I/O Input Data Byte 3 | C41 | m41 | | | C31 | m31 | | |
| I/O Input Data Byte 4 | C21 | m21 | | | C11 | m11 | | |
| I/O Input Data Byte 5 | C42 | m42 | | | C32 | m32 | | |
| I/O Input Data Byte 6 | C22 | m22 | | | C12 | m12 | | |
| I/O Input Data Byte 7 | C43 | m43 | | | C33 | m33 | | |
| I/O Input Data Byte 8 | C23 | m23 | | | C13 | m13 | | |
| I/O Input Data Byte 9 | C44 | m44 | | | C34 | m34 | | |
| I/O Input Data Byte 10 | C24 | m24 | | | C14 | m14 | | |
| I/O Input Data Byte 11 | C45 | m45 | | | C35 | m35 | | |
| I/O Input Data Byte 12 | C25 | m25 | | | C15 | m15 | | |

Cxy = 0 or 1 in the command above corresponds to Cxy = +1 or –1, respectively, in the equation below.

The Z-transform equation for the X filter is defined as:

$$H_x(z) = x_0 + x_1 z^{-1} + x_2 z^{-2} + x_3 z^{-3} + x_4 z^{-4} + x_5 z^{-5}$$

Sample rate = 16 kHz

For i = 0 to 5, the coefficients for the X filter are defined as:

$$Xi = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0111 0190 0190 0190 0190 0190h

($H_X(z) = 1$)

See note under Command 80/81h on page 80.

### 8A/8Bh Write/Read R Filter Coefficients

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 8Ah R: 8Bh | 1 | 0 | 0 | 0 | 1 | 0 | 1 | R/$\overline{W}$ |
| I/O Input Data Byte 1 | C46 | m46 | | | C36 | m36 | | |
| I/O Input Data Byte 2 | C26 | m26 | | | C16 | m16 | | |
| I/O Input Data Byte 3 | C40 | m40 | | | C30 | m30 | | |
| I/O Input Data Byte 4 | C20 | m20 | | | C10 | m10 | | |
| I/O Input Data Byte 5 | C41 | m41 | | | C31 | m31 | | |
| I/O Input Data Byte 6 | C21 | m21 | | | C11 | m11 | | |
| I/O Input Data Byte 7 | C42 | m42 | | | C32 | m32 | | |
| I/O Input Data Byte 8 | C22 | m22 | | | C12 | m12 | | |
| I/O Input Data Byte 9 | C43 | m43 | | | C33 | m33 | | |
| I/O Input Data Byte 10 | C23 | m23 | | | C13 | m13 | | |
| I/O Input Data Byte 11 | C44 | m44 | | | C34 | m34 | | |
| I/O Input Data Byte 12 | C24 | m24 | | | C14 | m14 | | |
| I/O Input Data Byte 13 | C45 | m45 | | | C35 | m35 | | |
| I/O Input Data Byte 14 | C25 | m25 | | | C15 | m15 | | |

Cxy = 0 or 1 in the command above corresponds to Cxy = +1 or –1, respectively, in the equation below.

$$HR = H_{IIR} \bullet H_{FIR}$$

The Z-transform equation for the IIR filter (RI) is defined as:

$$H_{IIR} = \frac{1 - z^{-1}}{1 - \left(R_6 \bullet z^{-1}\right)}$$

Sample rate = 8 kHz

The coefficient for the IIR filter is defined as:

$$R_6 = C16 \bullet 2^{-m16}\{1 + C26 \bullet 2^{-m26}[1 + C36 \bullet 2^{-m36}(1 + C46 \bullet 2^{-m46})]\}$$

R6 should normally not be set to unity. If it is required to generate DC levels through the receive path from the PCM, the CRP bit (*70/71h Write/Read Operating Conditions*, on page 79) should be set 5ms before writing R6 to unity. The RTP bit can then be reset and DC or low frequency signals passed from the PCM.

The Z-transform equation for the FIR filter is defined as:

$$H_{FIR}(z) = R_0 + R_1 z^{-1} + R_2 z^{-2} + R_3 z^{-3} + R_4 z^{-4} + R_5 z^{-5}$$

Sample rate = 16 kHz

For i = 0 to 5, the coefficients for the R2 filter are defined as:

$$R_i = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

*Power Up and Hardware Reset ($\overline{RST}$) Values = 2E01 0111 0190 0190 0190 0190 0190h

($H_{FIR}$ (z) = 1, $R_6$ = 0.9902)

See note under Command 80/81h on page 80.

**96/97h Write/Read B Filter IIR Coefficients**

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 96h R: 97h | 1 | 0 | 0 | 1 | 0 | 1 | 1 | R/$\overline{W}$ |
| I/O Data Byte 1 | C411 | m411 | | | C311 | m311 | | |
| I/O Data Byte 2 | C211 | m211 | | | C111 | m111 | | |

This function is described in command *86/87h Write/Read B Filter FIR Coefficients*, on page 81

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0190h ($B_{11}$ = 0)

See note under Command 80/81h on page 80.

**98/99h Write/Read Z Filter FIR Coefficients**

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 98h R: 99h | 1 | 0 | 0 | 1 | 1 | 0 | 0 | R/$\overline{W}$ |
| I/O Data Byte 1 | C40 | m40 | | | C30 | m30 | | |
| I/O Data Byte 2 | C20 | m20 | | | C10 | m10 | | |
| I/O Data Byte 3 | C41 | m41 | | | C31 | m31 | | |
| I/O Data Byte 4 | C21 | m21 | | | C11 | m11 | | |
| I/O Data Byte 5 | C42 | m42 | | | C32 | m32 | | |
| I/O Data Byte 6 | C22 | m22 | | | C12 | m12 | | |
| I/O Data Byte 7 | C43 | m43 | | | C33 | m33 | | |
| I/O Data Byte 8 | C23 | m23 | | | C13 | m13 | | |
| I/O Data Byte 9 | C44 | m44 | | | C34 | m34 | | |
| I/O Data Byte 10 | C24 | m24 | | | C14 | m14 | | |

This function is described in command *9A/9Bh Write/Read Z Filter IIR Coefficients*, on page 84

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0190 0190 0190 0190 0190h

($H_Z(z)$ = 0)

**9A/9Bh Write/Read Z Filter IIR Coefficients**

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: 9Ah R: 9Bh | 1 | 0 | 0 | 1 | 1 | 0 | 1 | R/$\overline{W}$ |
| I/O Data Byte 1 | C45 | m45 | | | C35 | m35 | | |
| I/O Data Byte 2 | C25 | m25 | | | C15 | m15 | | |
| I/O Data Byte 3 | C26 | m26 | | | C16 | m16 | | |
| I/O Data Byte 4 | C47 | m47 | | | C37 | m37 | | |
| I/O Data Byte 5 | C27 | m27 | | | C17 | m17 | | |

Cxy = 0 or 1 in the command above corresponds to Cxy = +1 or −1, respectively, in the equation below.

The Z-transform equation for the Z filter is defined as:

$$H_z(z) = z_0 + z_1 \bullet z^{-1} + z_2 \bullet z^{-2} + z_3 \bullet z^{-3} + z_4 \bullet z^{-4} + \frac{z_5 \bullet z_6 \bullet z_7 \bullet z^{-1}}{1 - z_7 \bullet z^{-1}}$$

Sample rate = 32 kHz

For i = 0 to 5 and 7

$$z_i = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

$$z_6 = C16 \bullet 2^{-m16}\{1 + C26 \bullet 2^{-m26}\}$$

*Power Up and Hardware Reset ($\overline{RST}$) Values = 0190 01 0190h

($H_Z(z) = 0$)

See note under Command 80/81h on page 80.

*Note:*

*$Z_6$ is used for IIR filter scaling only. Its value is typically greater than zero but less than or equal to one. The input to the IIR filter section is first increased by a gain of $1/Z_6$, improving dynamic range and avoiding truncation limitations through processing within this filter. The IIR filter output is then multiplied by $Z_6$ to normalize the overall gain. $Z_5$ is the actual IIR filter gain value defined by the programmed coefficients, but it also includes the initial $1/Z_6$ gain. The theoretical effective IIR gain, without the $Z_6$ gain and normalization, is actually $Z_5/Z_6$.*

**A6/A7h Write/Read Converter Configuration**

| Command | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| W: A6 R: A7h | 1 | 0 | 1 | 0 | 0 | 1 | 1 | R/$\overline{W}$ |
| I/O Data | ATI | DRAT2 | DRAT1 | DRAT0 | SEL3 | SEL2 | SEL1 | SEL0 |

ATI: Arm Transmit PCM data Interrupt.

0*: Transmit Data Ready interrupt disabled
1: Transmit Data Ready interrupt enabled

When ATI is 1, the interrupt pin will go active when the transmit data becomes available in *CDh Read Transmit PCM/Test Data*, on page 88. The interrupt will be cleared automatically after 54 µs (26 µs in wideband mode) (or when the data is read from the XDAT register). This interrupt indicates that data is available on both channels.

DRAT[2:0]:Data rate at which the converter data is updated.

The sampled data is output on the PCM highway and in register *CDh Read Transmit PCM/Test Data*, on page 88, as defined below. The ATI interrupt will also occur at this data rate if unmasked.

| | Narrowband | Wideband |
|---|---|---|
| 000*: | 8 kHz | 16kHz |
| 001: | 4 kHz | 8kHz |
| 010: | 2 kHz | 4kHz |
| 011: | 1 kHz | 2kHz |
| 100: | 500 Hz | 1kHz |
| 101: | Reserved | Reserved |
| 110: | Reserved | Reserved |
| 111: | Reserved | Reserved |

SEL[3:0]:This register selects the transmit path analog input source

The bits SEL3 - SEL0 select which input is routed to the A/D converter and hence which measurement shows up at the PCM highway and in register *CDh Read Transmit*

*PCM/Test Data*, on page 88. All unspecified codes are reserved.
When selecting a new input source, wait at least 3 ms for the data to become stable.

| SEL3 | SEL2 | SEL1 | SEL0 | Value written to measurement register | Operating Range Note 2. | Scale |
|---|---|---|---|---|---|---|
| 0* | 0* | 0* | 0* | Tip - Ring Metallic AC coupled Voltage | -3.44 V to 3.44 V | 105 µV |
| 0 | 0 | 0 | 1 | Switcher/Battery input at SWY | -160 V to 0 V | -7.324 mV |
| 0 | 0 | 1 | 0 | Switcher/Battery input at SWZ | -160 V to 0 V | -7.324 mV |
| 0 | 1 | 0 | 0 | Tip Voltage to ground | -240 V to 240 V | -7.324 mV |
| 0 | 1 | 0 | 1 | Ring Voltage to ground | -240 V to 240 V | -7.324 mV |
| 0 | 1 | 1 | 0 | Tip - Ring Metallic DC coupled Voltage | -240 V to 240 V | -7.324 mV |
| 0 | 1 | 1 | 1 | Tip - Ring Metallic Current - Ringing State | -119 mA to 119 mA | -3.63 µA |
| 0 | 1 | 1 | 1 | Tip - Ring Metallic Current - DC Feed State | -60 mA to 60 mA | -1.83 µA |
| 0 | 1 | 1 | 1 | Total Longitudinal Current - Low Gain State | -600 µA to 600 µA | -18.3 nA |
| 1 | 0 | 0 | 0 | Tip + Ring Longitudinal Current, LI = 0 | -42 mA to 42 mA | 1.3 µA |
| 1 | 0 | 0 | 0 | Tip + Ring Longitudinal Current, LI = 1 | -84 mA to 84 mA | 2.6 µA |
| 1 | 0 | 0 | 0 | Metallic Current - Low Gain State, LI = 0 | -105 µA to 105 µA | 3.20 nA |
| 1 | 0 | 0 | 0 | Metallic Current - Low Gain State, LI = 1 | -210 µA to 210 µA | 6.41 nA |
| 1 | 0 | 0 | 1 | Calibration Current (IREF) | -25 µA to 25 µA | 2.27 nA |
| 1 | 0 | 1 | 0 | Voice DAC Analog Loopback | -3.44 V to 3.44 V | 105 µV |
| 1 | 0 | 1 | 1 | No connection - read ADC output offset Note 1. | -3.44 V to 3.44 V | 105 µV |

1. The ADC output offset is defined relative to the default metallic AC coupled tip-ring voltage.
2. Operating ranges assume the standard external application circuit component values are used.

The operating range values may be less than the full scale ranges of the output. The scale assumes:
Register *50/51h Write/Read Voice Path Gains*, on page 74 = 00 h,
Register *60/61h Write/Read Operating Functions*, on page 77 = 80 h,
Register *70/71h Write/Read Operating Conditions*, on page 79 = 20 h and
Register *CA/CBh Write/Read Digital Impedance Scaling Network (DISN)*, on page 88 = 00 h.
Note that the SEL bit settings are overwritten when a system state change occurs. Wait 15 ms after the desired system state is selected before configuring the converter. It is also recommended that the ASSC bit in register *68/69h Write/Read System State Configuration*, on page 78 be set when performing measurements to avoid unexpected state changes that would disrupt the measurement.

The voltage and current scales define the typical values and do not imply a specific accuracy for the measurement path and A/D converter. The absolute accuracy of the measurement paths can be found in the electrical specification section. To achieve the specified accuracies, the ADC offset voltage should first be read by selecting the 'No connection' option and subtracting this result from subsequent measurements.
A full digital loop back from the digital input through the DAC to the ADC and back to the digital output is achieved by making the connection to the voice DAC. The nominal gain of this path is 0 dB.

For the battery inputs, Tip and Ring voltages, a negative voltage on the line reads as a positive value.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

### C2/C3h Write/Read Loop Supervision Parameters

| Command | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| W: C2h R: C3h | 1 | 1 | 0 | 0 | 0 | 0 | 1 | R/$\overline{W}$ |
| I/O Data Byte 1 | RSVD | RSVD | TGK2 | TGK1 | TGK0 | TSH2 | TSH1 | TSH0 |
| I/O Data Byte 2 | DGK2 | DGK1 | DGK0 | DSH4 | DSH3 | DSH2 | DSH1 | DSH0 |
| I/O Data Byte 3 | RTDCAC | RTTH6 | RTTH5 | RTTH4 | RTTH3 | RTTH2 | RTTH1 | RTTH0 |
| I/O Data Byte 4 | RSVD | RSVD | RSVD | ILR4 | ILR3 | ILR2 | ILR1 | ILR0 |

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

TGK[2:0]:Ground-key threshold; 0–42 mA, with a scale of 6 mA/step.
(default = 011b = 18mA)

TSH[2:0]:Switch hook threshold 8 - 15mA with a scale of 1mA Ω/step
(default = 011b = 11mA)

DGK[2:0]:Ground-key debounce; 0–28 ms, with a scale of 4 ms/step
(default = 100b = 16 ms)

DSH[4:0]:Switch-hook debounce interval; 0–62 ms, with a scale of 2 ms/step
Debounce settings less than 6 ms are not recommended
(default = 00100b = 8 ms)

RTDCAC:Ring Trip DC or AC.

0: Use DC ring trip detection algorithm which requires DC bias.
1*: Use AC ring trip detection algorithm which does not require DC bias.

RTTH[6:0]:Ring trip threshold; 0 - 63.5 mA with a scale of 0.5 mA/step.
(default = 110011b = 25.5mA)

ILR[4:0]:Ringing current limit; 50 - 112mA with a scale of 2 mA/step.
(default = 01110b = 78 mA)

*Power Up and Hardware Reset ($\overline{RST}$) Value = 1B84 B30Eh

### C6/C7h Write/Read DC Feed Parameters

| Command | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| W: C6h R: C7h | 1 | 1 | 0 | 0 | 0 | 1 | 1 | R/$\overline{W}$ |
| I/O Data Byte 1 | RSVD | VOCSFT | LI | VOC2 | VOC1 | VOC0 | VAS3 | VAS2 |
| I/O Data Byte 2 | VAS1 | VAS0 | RSVD | ILA4 | ILA3 | ILA2 | ILA1 | ILA0 |

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

VOCSFT:VOC shift

0*: VOC open circuit DC feed voltage. 36 - 57 V, with a step size of 3.0 V
1: VOC open circuit DC feed voltage. 12 - 33 V, with a step size of 3.0 V

LI: Longitudinal Impedance

0*: Longitudinal Impedance set to 100 Ω/leg
1: Longitudinal Impedance set to 50 Ω/leg

VOC[2:0]:Open circuit DC feed voltage. 36 - 57 V, with a step size of 3.0 V, VOCSFT = 0
Open circuit DC feed voltage. 12 - 33 V, with a step size of 3.0 V, VOCSFT = 1
(default = 100b = 48.0 V)

VAS[3:0]:Anti-sat offset voltage; 3 – 14.25 V, with a step size of 0.75 V
(default = 1000b = 9 V)

This voltage is the difference between the tracking regulator output and the sensed Tip-Ring Feed voltage with an open circuit load.*E6/E7h Write/Read Switching Regulator Control, on page 97*

ILA[4:0]:Current Limit Active mode; 18–49 mA, with a step size of 1 mA
(default = 01000b = 26 mA)

Power Up and Hardware Reset ($\overline{RST}$) Value = 1108h

**CA/CBh Write/Read Digital Impedance Scaling Network (DISN)**

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: CAh R: CBh | 1 | 1 | 0 | 0 | 1 | 0 | 1 | R/$\overline{W}$ |
| I/O Data | DISN7 | DISN6 | DISN5 | DISN4 | DISN3 | DISN2 | DISN1 | DISN0 |

DISN[7:0]:Digital Impedance scaling network two's complement gain value.

The DISN gain can be varied from -1.0 to 0.992 in steps of 0.0078. A value of 0 removes the DISN from the impedance loop.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

**CDh Read Transmit PCM/Test Data**

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| R: CDh | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| Output Data Byte 1 | XDAT15 | XDAT14 | XDAT13 | XDAT12 | XDAT11 | XDAT10 | XDAT9 | XDAT8 |
| Output Data Byte 2 | XDAT7 | XDAT6 | XDAT5 | XDAT4 | XDAT3 | XDAT2 | XDAT1 | XDAT0 |

This register will behave as described when the TDIM bit in *5E/5Fh Write/Read Device Mode Register, on page 76* is left in its default state (reset).

XDAT: Read signal Value.

XDAT[15:8]Contains A-law or μ-law transmit data in Companded mode.
XDAT[15:0]Contains upper and lower data bytes in Linear mode with sign in XDAT15.

XDAT can only be read from one channel at a time as selected by the EC register. If two channels or no channel are selected, the data for channel 1 will be returned.

In test mode, as defined by command *A6/A7h Write/Read Converter Configuration, on page 85*, the A/D converter is connected either to the voice path (codec bypass), or to other signals as defined by the SEL bits. In this case the XDAT[0-15] bits indicate the measured value of the signal connected to the A/D converter in 1.15 format assuming linear mode is selected. The maximum values and scales are given in the chart. Negative Tip, Ring and battery voltages are reported as positive values.

This register input is sampled data at a rate set by DRAT in command *A6/A7h Write/Read Converter Configuration, on page 85* and the register is updated at the programmed data rate. A new measurement may be made by updating the converter configuration register. An interrupt can be generated and the DAT bit in *4D/4Fh Read Signaling Register, on page 72* is set every time this register is updated by setting the ATI bit in the same converter configuration register. The signal may be sampled by the user as fast as 8KSa/sec in this mode.

To get meaningful DC test data, the device should be configured as described in *A6/A7h Write/Read Converter Configuration, on page 85*. This data will also be transmitted on the DXA pin unless the CTP bit is set.

While this register can be read in GCI mode, the monitor channel protocol only allows this data to be sampled at a slow rate. It is recommended that the compressed B channel data is read directly from the GCI bus in this mode.

### CFh Read Test Data Buffer

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| R: CFh | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| Output Data Byte 1 | RSVD | LEN2 | LEN1 | LEN0 | HK25 | HK24 | HK23 | HK22 |
| Output Data Byte 2 | HK21 | HK20 | HK15 | HK14 | HK13 | HK12 | HK11 | HK10 |
| Output Data Byte 3 | $DAT1_{15}$ | $DAT1_{14}$ | $DAT1_{13}$ | $DAT1_{12}$ | $DAT1_{11}$ | $DAT1_{10}$ | $DAT1_9$ | $DAT1_8$ |
| Output Data Byte 4 | $DAT1_7$ | $DAT1_6$ | $DAT1_5$ | $DAT1_4$ | $DAT1_3$ | $DAT1_2$ | $DAT1_1$ | $DAT1_0$ |
| Output Data Byte 5 | $DAT2_{15}$ | $DAT2_{14}$ | $DAT2_{13}$ | $DAT2_{12}$ | $DAT2_{11}$ | $DAT2_{10}$ | $DAT2_9$ | $DAT2_8$ |
| Output Data Byte 6 | $DAT2_7$ | $DAT2_6$ | $DAT2_5$ | $DAT2_4$ | $DAT2_3$ | $DAT2_2$ | $DAT2_1$ | $DAT2_0$ |
| Output Data Byte 7 | $DAT3_{15}$ | $DAT3_{14}$ | $DAT3_{13}$ | $DAT3_{12}$ | $DAT3_{11}$ | $DAT3_{10}$ | $DAT3_9$ | $DAT3_8$ |
| Output Data Byte 8 | $DAT3_7$ | $DAT3_6$ | $DAT3_5$ | $DAT3_4$ | $DAT3_3$ | $DAT3_2$ | $DAT3_1$ | $DAT3_0$ |
| Output Data Byte 9 | $DAT4_{15}$ | $DAT4_{14}$ | $DAT4_{13}$ | $DAT4_{12}$ | $DAT4_{11}$ | $DAT4_{10}$ | $DAT4_9$ | $DAT4_8$ |
| Output Data Byte 10 | $DAT4_7$ | $DAT4_6$ | $DAT4_5$ | $DAT4_4$ | $DAT4_3$ | $DAT4_2$ | $DAT4_1$ | $DAT4_0$ |
| Output Data Byte 11 | $DAT5_{15}$ | $DAT5_{14}$ | $DAT5_{13}$ | $DAT5_{12}$ | $DAT5_{11}$ | $DAT5_{10}$ | $DAT5_9$ | $DAT5_8$ |
| Output Data Byte 12 | $DAT5_7$ | $DAT5_6$ | $DAT5_5$ | $DAT5_4$ | $DAT5_3$ | $DAT5_2$ | $DAT5_1$ | $DAT5_0$ |
| Output Data Byte 13 | $DAT6_{15}$ | $DAT6_{14}$ | $DAT6_{13}$ | $DAT6_{12}$ | $DAT6_{11}$ | $DAT6_{10}$ | $DAT6_9$ | $DAT6_8$ |
| Output Data Byte 14 | $DAT6_7$ | $DAT6_6$ | $DAT6_5$ | $DAT6_4$ | $DAT6_3$ | $DAT6_2$ | $DAT6_1$ | $DAT6_0$ |

This register will behave as described when the TDIM bit in *5E/5Fh Write/Read Device Mode Register,* on page 76 is set.

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

LEN[2:0]: Number of valid PCM data words and Hook bits stored in the FIFOs.

Values from 0 to 6 indicate the number of new DAT words and HK bits collected since this register was last read.
A value of 7 indicates that the buffers have overflowed and that samples have been discarded.
This field is reset to zero when the register is read. An interrupt can be generated and the DAT bit in *4D/4Fh Read Signaling Register,* on page 72 set when the first new sample is loaded into the FIFO and the length field increments to 001b if the ATI bit is set.

HK1[5:0]: Hook Bit Channel 1 FIFO

This FIFO stores the status of the debounced Hook Switch Detector output.
The LEN field defines the number of valid detector samples stored in the 1 bit wide FIFO.

HK2[5:0]: Hook Bit Channel 2 FIFO

This FIFO stores the status of the debounced Hook Switch Detector output.
The LEN field defines the number of valid detector samples stored in the 1 bit wide FIFO.

DAT1-6: PCM Sample FIFO data.

DATn[15:8]Contains A-law or μ-law transmit data in Companded mode.
DATn[15:0]Contains upper and lower data bytes in Linear mode with sign in DATn15.

The DATn FIFO can only be read from one channel at a time as selected by the CDS bit in the *5E/5Fh Write/Read Device Mode Register,* on page 76.

In test mode, as defined by command *A6/A7h Write/Read Converter Configuration,* on page 85, the A/D converter is connected either to the voice path (codec bypass), or to other signals as defined by the SEL bits. In this case the DATn words indicate the measured value of the signal connected to the A/D converter in 1.15 format assuming linear mode is selected. The maximum values and scales are given in the chart. Negative Tip, Ring and battery voltages are reported as positive values.

The DATn FIFO input is sampled data at a rate set by DRAT in command *A6/A7h Write/Read Converter Configuration,* on page 85 and the DAT and HK FIFOs and LEN field are updated at the programmed data rate. Using the slowest sample rate of 2 ms in narrow band mode allows 12ms of data to be stored and supports a 10ms nominal polling rate. Use of wideband mode (if available) reduces the maximum sample rate to 1ms, corresponding to a 5ms polling rate.

To get meaningful DC test data, the device should be configured as described in *A6/A7h Write/Read Converter Configuration,* on page 85. This data will also be transmitted on the DXA pin unless the CTP bit is set. To read the hook data in IDLE mode, the codec must also be activated.

While this register can be read in GCI mode, the monitor channel protocol only allows this data to be sampled at a slow rate. It is recommended that the compressed B channel data is read directly from the GCI bus in this mode.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 0000 0000 0000 0000 0000 0000 0000 h

**D0/D1h Write/Read Metering Parameters**

| Command | D7* | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| W: D0h R: D1h | 1 | 1 | 0 | 1 | 0 | 0 | 0 | R/$\overline{W}$ |
| I/O Data Byte 1 | MTRF | MLIM6 | MLIM5 | MLIM4 | MLIM3 | MLIM2 | MLIM1 | MLIM0 |
| I/O Data Byte 2 | SOREV | MTRSL6 | MTRSL5 | MTRSL4 | MTRSL3 | MTRSL2 | MTRSL1 | MTRSL0 |
| I/O Data Byte 3 | MTRDR7 | MTRDR6 | MTRDR5 | MTRDR4 | MTRDR3 | MTRDR2 | MTRDR1 | MTRDR0 |
| I/O Data Byte 4 | MTRPK7 | MTRPK6 | MTRPK5 | MTRPK4 | MTRPK3 | MTRPK2 | MTRPK1 | MTRPK0 |

MTRF: Metering frequency

0*: 12 kHz
1: 16 kHz

MLIM[6:0]: This field sets the peak voltage level of the metering signal voltage at the AC sense point.
MLIM is programmed as an unsigned integer.
If MTRF is 0 (12 kHz), MLIM has a step size of 15 mVrms
If MTRF is 1 (16 kHz), MLIM has a step size of 18 mVrms
(default = 0100001b)

Metering signals up to 0.5 Vrms at the line are supported.

SOREV:Smooth ramping or abrupt application

0*: Smooth ramping
1: Abrupt ramping

MTRSL[6:0]: Metering Slope. This parameter sets the metering output current limit into a short circuit between TIPD and RINGD. MTRSL is programmed as an unsigned integer.
MTRSL has a range of 0 – 8.636 mArms and a step size of 68 µA.
The metering ramp lasts for 20 ms or until the voltage specified by MLIM is reached. The slope in mA/ms can be calculated by $\text{slope} = \frac{\text{MTRSL}}{20\text{msec}}$. If MTRSL is too small to generate the voltage MLIM, the ramp will stop at the

output current MTRSL after 20 ms.
(default = 0111101b)

MTRDR[7:0]: Metering Duration. MTRDR sets the time metering output current is applied to the line. 0 – 637.5 ms with a step size of 2.5 ms. A value of 00h indicates continuous metering. (default = 3Ch = 150 ms)

MTRPK[7:0]: This field reads the maximum voltage level of the metering signal voltage at the AC sense point.
If MTRF is 0 (12 kHz), MTRPK has a step size of 15 mVrms
If MTRF is 1 (16 kHz), MTRPK has a step size of 18 mVrms
This field is read only. Writes to this location are ignored.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 213D 3C00h

**D2/D3h Write/Read Signal Generator A, B and Bias Parameters.**

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: D2h R: D3h | 1 | 1 | 0 | 1 | 0 | 0 | 1 | R/$\overline{W}$ |
| I/O Byte 1 | RSVD | RSVD | RSVD | RSVD | RSVD | RMPSLP | CNTRMP | SINTRAP |
| I/O Byte 2 | BIAS15 | BIAS14 | BIAS13 | BIAS12 | BIAS11 | BIAS10 | BIAS9 | BIAS8 |
| I/O Byte 3 | BIAS7 | BIAS6 | BIAS5 | BIAS1 | BIAS3 | BIAS2 | BIAS1 | BIAS0 |
| I/O Byte 4 | RSVD | FRQA14 | FRQA13 | FRQA12 | FRQA11 | FRQA10 | FRQA9 | FRQA8 |
| I/O Byte 5 | FRQA7 | FRQA6 | FRQA5 | FRQA4 | FRQA3 | FRQA2 | FRQA1 | FRQA0 |
| I/O Byte 6 | AMPA15 | AMPA14 | AMPA13 | AMPA12 | AMPA11 | AMPA10 | AMPA9 | AMPA8 |
| I/O Byte 7 | AMPA7 | AMPA6 | AMPA5 | AMPA4 | AMPA3 | AMPA2 | AMPA1 | AMPA0 |
| I/O Byte 8 | RSVD | FRQB14 | FRQB13 | FRQB12 | FRQB11 | FRQB10 | FRQB9 | FRQB8 |
| I/O Byte 9 | FRQB7 | BRQA6 | FRQB5 | FRQB4 | FRQB3 | FRQB2 | FRQB1 | FRQB0 |
| I/O Byte 10 | AMPB15 | AMPB14 | AMPB13 | AMPB12 | AMPB11 | AMPB10 | AMPB9 | AMPB8 |
| I/O Byte 11 | AMPB7 | AMPB6 | AMPB5 | AMPB4 | AMPB3 | AMPB2 | AMPB1 | AMPB0 |

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

RMPSLP:Ramp Slope

0*: Leaves the sign of AMPA unchanged.
1: Negates AMPA to change the ramp direction.

This bit also has the effect of inverting the sign of a continuous wave driven from signal generator A.

CNTRMP:Continuous or Ramp operation

0*: Signal Generators A and B output continuous waves.
1: A single ramp is output starting from the DC offset set by the BIAS parameter and ramping by an amplitude specified by AMPA. The ramp is started when Generator A is enabled or a set of signal generator A parameters are written.
The new ramp begins wherever the generator A output is sitting, and changes by a value set by AMPA and RMPSLP
In a signal consisting of a series of ramped signal changes, BIAS should normally be kept constant at the beginning value of the signal. Changing BIAS will cause an abrupt signal change.

SINTRAP must be set to 1 if CNTRMP is set to 1.

FRQA is programmed with the rise time of the linear ramp. This is given by:

$$FRQA = \frac{1.365}{T_{rise}}$$

where FRQA is a signed 16 bit integer. Negative values are invalid.

SINTRAP:Sinusoidal or Trapezoidal output

0*: Signal Generators A and B output sinusoidal waves.
1: Signal Generator A outputs trapezoidal waves and signal generator B outputs nothing.

SINTRAP must be set to 1 if CNTRMP is set to 1.

BIAS: Generate DC bias offset parameter.
Signed 16 bit integer with a range of ±154.4 V in ringing and a scale of 4.711 mV/step.
(default = 0000h = 0V).

FRQA[14:0]:Frequency or rise time parameter of signal generator A
When SINTRAP = 0, FRQA is an unsigned number with a frequency step size of 0.3662 Hz. The maximum allowable frequency is 3400 Hz in normal mode and 6800Hz in wideband mode. The signal generator runs through the voice path which has internal filters and a sampling rate of 8KSa/sec (16KSa/sec. in wideband mode).
When SINTRAP = 1, the waveshape is set to trapezoidal, the FRQA parameter sets the rise time according to the following formula:

$$FRQA = \frac{2.73}{T_{rise}}$$

where FRQA is a signed 16 bit integer. Negative values are invalid.
(default = 0037h = 20.1Hz)

AMPA[15:0]: Amplitude parameter of signal generator A
Signed 16 bit integer with a range of ±154.4 V in ringing and a scale of 4.711 mV/step
Up to +3.14 dBm0 in active states into the voice path
AMPA is the peak value of the digital sine wave or trapezoid wave.
A positive value will start the wave at 0 with a positive initial first derivative (wave goes up). A negative value will start the wave at 0 with a negative initial first derivative (wave goes down). In ringing, the signal generator is not connected to the line until a zero voltage cross with VOC if ZXR is set to 0.
(default = 4AA4h = 90V)

FRQB[14:0]:Frequency parameter of signal generator B
When SINTRAP = 0, FRQB is an unsigned number with a frequency step size of 0.3662 Hz. The maximum allowable frequency is 3400 Hz in normal mode and 6800Hz in wideband mode. The signal generator runs through the voice path which has internal filters and a sampling rate of 8KSa/sec (16KSa/sec. in wideband mode).
When SINTRAP = 1, the waveshape is set to trapezoidal, the FRQB parameter sets the frequency according to the following formula:

$$FRQB = \frac{8000}{F_{Ring}}$$

where FRQB is a signed 16 bit integer. Negative values are invalid.
(default = 0000h)

AMPB[15:0]: Amplitude parameter of signal generator B
Up to +3.14 dBm0 in active states into the voice path
AMPB is the peak value of the digital sine wave.
A positive value will start the wave at 0 with a positive initial first derivative (wave

goes up). A negative value will start the wave at 0 with a negative initial first derivative (wave goes down).
(default = 0000h)

Note: Ringing automatically uses signal generator A's parameters. The POLNR bit will affect the sign of the sum of the tone generators and bias. If the generator is used to control the metallic voltage either for ringing or for diagnostic tests, positive generator values produce reverse polarity voltages (ring more positive than tip) when POLNR is 0.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00 0000 0037 4AA4 0000 0000h

**D4/D5h Write/Read Signal Generator C and D Parameters.**

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: D4h R: D5h | 1 | 1 | 0 | 1 | 0 | 1 | 0 | R/$\overline{W}$ |
| I/O Byte 1 | RSVD | FRQC14 | FRQC13 | FRQC12 | FRQC11 | FRQC10 | FRQC9 | FRQC8 |
| I/O Byte 2 | FRQC7 | FRQC6 | FRQC5 | FRQC4 | FRQC3 | FRQC2 | FRQC1 | FRQC0 |
| I/O Byte 3 | AMPC15 | AMPC14 | AMPC13 | AMPC12 | AMPC11 | AMPC10 | AMPC9 | AMPC8 |
| I/O Byte 4 | AMPC7 | AMPC6 | AMPC5 | AMPC4 | AMPC3 | AMPC2 | AMPC1 | AMPC0 |
| I/O Byte 5 | RSVD | FRQD14 | FRQD13 | FRQD12 | FRQD11 | FRQD10 | FRQD9 | FRQD8 |
| I/O Byte 6 | FRQD7 | BRQA6 | FRQD5 | FRQD4 | FRQD3 | FRQD2 | FRQD1 | FRQD0 |
| I/O Byte 7 | AMPD15 | AMPD14 | AMPD13 | AMPD12 | AMPD11 | AMPD10 | AMPD9 | AMPD8 |
| I/O Byte 8 | AMPD7 | AMPD6 | AMPD5 | AMPD4 | AMPD3 | AMPD2 | AMPD1 | AMPD0 |

FRQC[14:0]:Frequency parameter of signal generator C
FRQC is an unsigned number with a frequency step size of 0.3662 Hz.
The maximum allowable frequency is 3400 Hz in normal mode and 6800Hz in wideband mode. The signal generator runs through the voice path which has internal filters and a sampling rate of 8KSa/sec (16KSa/sec in wideband mode).
(default = 1777h = 2200Hz)

AMPC[15:0]:Amplitude parameter of signal generator C
Up to +3.14 dBm0 into the voice path
AMPC is the peak value of the digital sine wave. A positive value will start the wave at 0 with a positive initial first derivative (wave goes up). A negative value will start the wave at 0 with a negative initial first derivative (wave goes down).
(default = 27D4h = -7 dBm0)

FRQD[14:0]:Frequency parameter of signal generator D
FRQD is an unsigned number with a frequency step size of 0.3662 Hz.
The maximum allowable frequency is 3400 Hz in normal mode and 6800Hz in wideband mode. The signal generator runs through the voice path which has internal filters at a sampling rate of 8KSa/sec (16KSa/sec in wideband mode).
(default = 0CCDh = 1200Hz)

AMPD[15:0]:Amplitude parameter of signal generator D
Up to +3.14 dBm0 into the voice path
AMPD is the peak value of the digital sine wave. A positive value will start the wave at 0 with a positive initial first derivative (wave goes up). A negative value will start the wave at 0 with a negative initial first derivative (wave goes down).
(default = 27D4h = -7 dBm0)

Caller ID automatically uses the parameters stored in signal generators C and D.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 1777 27D4 0CCD 27D4

### DE/DFh Write/Read Signal Generator Control

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: DEh R: DFh | 1 | 1 | 0 | 1 | 1 | 1 | 1 | R/$\overline{W}$ |
| I/O Data | SGCAD | CNTOS | RSVD | EGBIAS | EGD | EGC | EGB | EGA |

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

SGCAD:Signal Generator Cadencing

0*: No Signal generator cadencing
1: The enabled tone generators specified by EGA - EGBIAS will cadence on and off as determined by command *E0/E1h Write/Read Cadence Timer*, on page 95

The EGx bits will read back zero in the cadence off time.

This command makes use of the cadence timer. The enabled functions are toggled at a rate specified by the cadence timer. The CAD bit in command *4D/4Fh Read Signaling Register*, on page 72 is set at the end of the on period, which can optionally generate an interrupt if MCAD is reset in command *6C/6Dh Write/Read Interrupt Mask Register*, on page 79. At this time, the user may write new values into the cadence timer and reissue the signal generator control command.

If no enable bits are set, the cadencer will run and will still set the CAD bit at the end of the on period and can produce an interrupt. In this way, the cadencer can be used as a system timer.

CNTOS:Continuous or One Shot cadence operation.

0*: Continuous cadencing. Cadencing will continue until the user intervenes.
1: One shot. The generators will turn on for one on period only. All enable bits and SGCAD will be set to zero after the off period. An interrupt will be sent at the end of the on period.

EGBIAS:Enable DC Bias

0*: DC Bias disabled
1: DC Bias enabled

EGD: Enable Signal Generator D

0*: Generator D disabled
1: Generator D enabled

EGC: Enable Signal Generator C

0*: Generator C disabled
1: Generator C enabled

EGB: Enable Signal Generator B

0*: Generator B disabled
1: Generator B enabled

EGA: Enable Signal Generator A

0*: Generator A disabled
1: Generator A enabled

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

### E0/E1h Write/Read Cadence Timer

| Command | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| W: E0h R: E1h | 1 | 1 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ |
| I/O Byte 1 | RSVD | RSVD | RSVD | RSVD | RSVD | CADON10 | CADON9 | CADON8 |
| I/O Byte 2 | CADON7 | CADON6 | CADON5 | CADON4 | CADON3 | CADON2 | CADON1 | CADON0 |
| I/O Byte 3 | RSVD | RSVD | RSVD | RSVD | RSVD | $CADOFF_{10}$ | $CADOFF_9$ | $CADOFF_8$ |
| I/O Byte 4 | $CADOFF_7$ | $CADOFF_6$ | $CADOFF_5$ | $CADOFF_4$ | $CADOFF_3$ | $CADOFF_2$ | $CADOFF_1$ | $CADOFF_0$ |

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

CADON[10:0]:Cadence On Time. 0 - 10.24 seconds with a scale of 5 ms per step.
(default* = 190h = 2 sec)

CADOFF[10:0]:Cadence Off Time. 0 - 10.24 seconds with a scale of 5 ms per step.
(default* = 320h = 4 sec)

During the ring off time, the system state is Active.

If the cadence off time is 0, the function will be enabled indefinitely.

The cadencer is a shared timer that is used for a variety of functions including: ringing cadencing, and tone pulsing e.g. howler tone generation.The on and off times are set by this command and the individual commands for these functions enable the cadencer.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 0190 0320h

### E2/E3h Write/Read Caller Identification Number Data

| Command | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| W: E2h R: E3h | 1 | 1 | 1 | 0 | 0 | 0 | 1 | R/$\overline{W}$ |
| I/O Data | $CID_7$ | $CID_6$ | $CID_5$ | $CID_4$ | $CID_3$ | $CID_2$ | $CID_1$ | $CID_0$ |

CID: Caller ID Data

Writing to this register will send CID data to the subscriber line based on the status of the CIDDIS bit in command *EA/EBh Write/Read Caller Identification Number Parameters*, on page 99. The CID bit in command *4D/4Fh Read Signaling Register*, on page 72 is set when the VE8820 device becomes ready to receive more data, which can optionally generate an interrupt if MCID is reset in command *6C/6Dh Write/Read Interrupt Mask Register*, on page 79.

The amplitude and frequency parameters for caller number delivery are programmed in *D4/D5h Write/Read Signal Generator C and D Parameters.*, on page 93. Except for the first byte, data may not be written to this register until the CID interrupt is received or CID state is Ready in *EA/EBh Write/Read Caller Identification Number Parameters*, on page 99. If data is written before this interrupt is generated by the VE8820, the operation of the CID sequence is undefined.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

### E4/E5h Write/Read Switching Regulator Parameters

| Command | D7* | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| W: E4h R:E5 h | 1 | 1 | 1 | 0 | 0 | 1 | 0 | R/$\overline{W}$ |
| I/O Data Byte 1 | RSVD | RSVD | FLYBB | RSVD | ZRTM | RSVD | YRTM | RSVD |
| I/O Data Byte 2 | SWYAP | SWFS1 | SWFS0 | $SWYV_4$ | $SWYV_3$ | $SWYV_2$ | $SWYV_1$ | $SWYV_0$ |
| I/O Data Byte 3 | SWZAP | RSVD | RSVD | $SWZV_4$ | $SWZV_3$ | $SWZV_2$ | $SWZV_1$ | $SWZV_0$ |

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read

FLYBB: Converter mode - Flyback or Inverting Buck-Boost

0*: Converters are in Flyback mode
1: Converters are in Inverting Buck-Boost mode.

ZRTM: Switching regulator Z Ringing Tracking Mode

0*: Regulator voltage tracks the ringing voltage when in ringing
1: Regulator voltage in ringing is fixed and defined by the programmed value in the SWZV bits. This bit does not affect non ringing modes.

YRTM: Switching regulator Y Ringing Tracking Mode

0*: Regulator voltage tracks the ringing voltage when in ringing
1: Regulator voltage in ringing is fixed and defined by the programmed value in the SWZV bits. This bit does not affect non ringing modes.

SWYAP: Switching regulator Y Automatic Power mode

0*: Switching regulator Y power mode is automatically selected by the VE8820 device based on the system state.
1: Switching regulator Y power mode is determined by the programming of the YM bits in *E6/E7h Write/Read Switching Regulator Control*.

SWFS[1:0]: Switching regulator frequency select. Selects the switching regulator clock in the three power modes. Non-default values are normally used in buck-boost applications. Applies to both switching regulators.

| | Low Power | Medium Power | High Power |
|---|---|---|---|
| 00*: | 48 kHz | 96 kHz | 384 kHz |
| 01: | 24 kHz | 48 kHz | 192 kHz |
| 10: | 12 kHz | 24 kHz | 96 kHz |
| 11: | Reserved | | |

SWYV[4:0]: Switching regulator floor voltage

Specifies the minimum output voltage of the tracking voltage regulator.
Range -5 V to -160 V with a step size of -5 V
(default = 04h = -25 V)

SWZAP: Switching regulator Z Automatic Power mode

0*: Switching regulator Z power mode is automatically selected by the VE8820 device based on the system state.
1: Switching regulator Z power mode is determined by the programming of the ZM bits in the Write/Read Switching Regulator Control Register.

SWZV[4:0]: Switching regulator ringing voltage

Specifies the fixed output voltage that the tracking regulator will generate in ringing when ZRTM or YRTM is 1.
Range -5 V to -160 V with a step size of -5 V
default = 12h = -95 V)

The available SWxV voltage is internally clamped to -100 V on the low voltage devices and -150 V on the high voltage devices.

This command does not depend on the state of the Channel Enable Register.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00 040Ah

**E6/E7h Write/Read Switching Regulator Control**

| Command | D7* | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| W: E6h R: E7h | 1 | 1 | 1 | 0 | 0 | 1 | 1 | R/$\overline{W}$ |
| I/O Data | RSVD | RSVD | RSVD | SWOVP | $ZM_1$ | $ZM_0$ | $YM_1$ | $YM_0$ |

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

SWOVP:Switcher Over Voltage Protection enable

0: No over voltage sense protection.

1: Over voltage protection enabled.

Nominal threshold is 120 V. If this threshold is exceeded at any of the voltage sense pins, the corresponding switching regulators will be shut down and OCALMY or OCALMZ bits will be set.

If SWOVP is set, at least on channel should be in the disconnect state before the switching regulators are enabled

YM[1:0]:Switcher Y mode bits

ZM[1:0]:Switcher Z mode bits

The mode bits are defined in the following table:

| Mode Bit 1 | Mode Bit 0 | Mode Definition | Designation |
|---|---|---|---|
| 0* | 0* | **Shutdown** | OFF |
| 0 | 1 | Low Power Lowest Switcher Clock | LP |
| 1 | 0 | Medium Power Medium Switcher Clock | MP |
| 1 | 1 | High Power High Switcher Clock | HP |

If the SWYAP and SWZAP bits in the *E4/E5h Write/Read Switching Regulator Parameters*, on page 96 register are set to 0 - Switching regulator mode coupled to system state, the switcher power mode can be written in this mode, but the power mode will be overwritten when a system state change occurs. If the SWYAP or SWZAP bits are set to one, writes to YM[1:0] and ZM[1:0] directly control the switcher power mode and system state changes have no effect on the power mode.

From the power up shutdown state, the power supply should be started in mode 1 or 2. After ten milliseconds in these modes, mode 3 can be selected if high power output is required.

Setting YM[1:0] and ZM[1:0] to 00b places the system into the Shutdown state by turning off the switching supply regardless of the value of SWYAP or SWZAP.

This command does not depend on the state of the Channel Enable Register.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

**E8/E9h Write/Read Battery Calibration Register**

| Command | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| W: FAh R: FBh | 1 | 1 | 1 | 1 | 1 | 0 | 1 | R/$\overline{W}$ |
| I/O Data Byte 1 | RSVD | RSVD | d_swcal2 | d_swcal1 | d_swcal0 | RSVD | RSVD | c_abs_deb |
| I/O Data Byte 2 | RSVD | RSVD | RSVD | RSVD1 | RSVD | RSVD | RSVD | RSVD |

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

RSVD1 Reserved for future use. Always write as 1.

d_swcal[2:0]: Switching regulator voltage calibration.

000 0.00 V
001 1.25 V
010 2.50 V
011 3.75 V
100 0.00 V
101 -1.25 V
110 -2.50 V
111 -3.75 V

CH1 - switcher Y calibration.
CH2 - switcher Z calibration.

c_abs_deb:Auto bat switching debounce algorithm.

0: Use original ABS algorithm.
If line voltage exceeds switch threshold, switch after 2 ms unless line voltage returns past (Threshold + hysteresis) within the 2 ms wait period

1: Use new ABS algorithm.
Line voltage must exceed current switch threshold for 2 ms (Sampled at 8 kHz) before switching. This algorithm is less sensitive to short glitches and AC signals near the threshold. It may require the nominal threshold to be reduced by using a larger VAS to avoid AC signal clipping at the threshold.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 0010h

### EA/EBh Write/Read Caller Identification Number Parameters

| Command | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| W: EAh R: EBh | 1 | 1 | 1 | 0 | 1 | 0 | 1 | R/$\overline{W}$ |
| I/O Data | CIDST2 | CIDST1 | CIDST0 | EOM | FBDIS | FBSRT | FBSTP | CIDDIS |

CIDST[2:0]: These bits report back the state of the CID state machine.

| CIDST2 | CIDST1 | CIDST0 | State |
|---|---|---|---|
| 0 | 0 | 0 | Idle* |
| 0 | 0 | 1 | Empty |
| 0 | 1 | 0 | Half Full |
| 0 | 1 | 1 | Last byte |
| 1 | 0 | 0 | Last 2 bytes |
| 1 | 0 | 1 | Underrun |
| 1 | 1 | 0 | Full |
| 1 | 1 | 1 | Last 3 bytes |

These bits are read only. Writes to these bits are ignored.

EOM: End of Message

0*: The end of message is not the next byte written
1: The next byte written will be the last byte in the CID message

This bit is reset after the last byte is transmitted

FBDIS: Frame Bit Disable

0*: The CID message data written to VE8820 is automatically framed by the VE8820 device with the start and stop bit specified in FBSRT and FBSTP
1: No start/stop bit framing is done by the VE8820 device. The data written to VE8820 is passed directly to the subscriber line. The user may frame their data by embedding start/stop bits within the data.

FBSRT:Frame Bit Start bit

0*: Start bit will be a 0 (space) if FBDIS = 0
1: Start bit will be a 1 (mark) if FBDIS = 0

This bit is ignored if FBDIS = 1.

FRSTP:Frame Bit Stop bit

0: Stop bit will be a 0 (space) if FBDIS = 0
1*: Stop bit will be a 1 (mark) if FBDIS = 0

This bit is ignored if FBDIS = 1

CIDDIS:Caller ID disable

0: Caller ID is enabled. Writes to the CID data register will be driven onto the subscriber line.
1*: Caller ID is disabled. Any writes to the CID data register will not be driven to the subscriber line.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 03h

**FC/FDh Write/Read DC Calibration Register**

| Command | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| W: FCh R: FDh | 1 | 1 | 1 | 1 | 1 | 0 | 1 | R/$\overline{W}$ |
| I/O Data Byte 1 | RSVD | RSVD | RSVD | RSVD | RSVD | mc_inp_offs | RSVD | RSVD |
| I/O Data Byte 2 | RSVD | RDC_sns | TDC_sns | c_ibuff5_ voc_off | RSVD | c_inp_offs | RSVD | RSVD |

mc_inp_offs:Input Offset Override.

0* Disable Override.

1 Enable override of the input offset current applied to the TDC and RDC pins which corrects for the offset voltage created by operating at VREF instead of ground using the c_inp_offs bit.

RDC_sns:RDC pin sense disable

0* Enable voltage sensing via the RDC pin.

1 Disable voltage sensing from the RDC pin. This effectively opens the RDC sense input and allows a DC input offset voltage calibration factor to be measured using the appropriate converter configuration setting.

TDC_sns:TDC pin sense disable

0* Enable voltage sensing via the associated pin.

1 Disable voltage sensing from the TDC pin This effectively opens the TDC sense input and allows a DC input offset voltage calibration factor to be measured using the appropriate converter configuration setting.

Disabling all three sense inputs on each channel allows the Automatic Battery Switch Threshold voltage to be calibrated. Place the device into the Active Mid or Low Battery state with automatic battery switching enabled. The firmware should then increment through each ABSCAL value in turn starting at -5.25 V, checking the d_bat_lm bit after at least 2 ms for each step. The ABSCAL value written before the bit is set is the optimum calibration value for that channel and polarity. Repeat in the other polarity to determine the ABSCAL values to be applied in Normal and Reverse polarity, store them on a per channel basis and apply them to the ABSCAL bits in the corresponding states.

c_ibuff5_voc_off:Turns off Internal current buffer ibuff5
Can be used for debug and/or ILA calibration

0*: Ibuff5 on.

1: Ibuff5 off

c_inp_offs:TDC and RDC pin input offset control.

0* Input offset enabled.

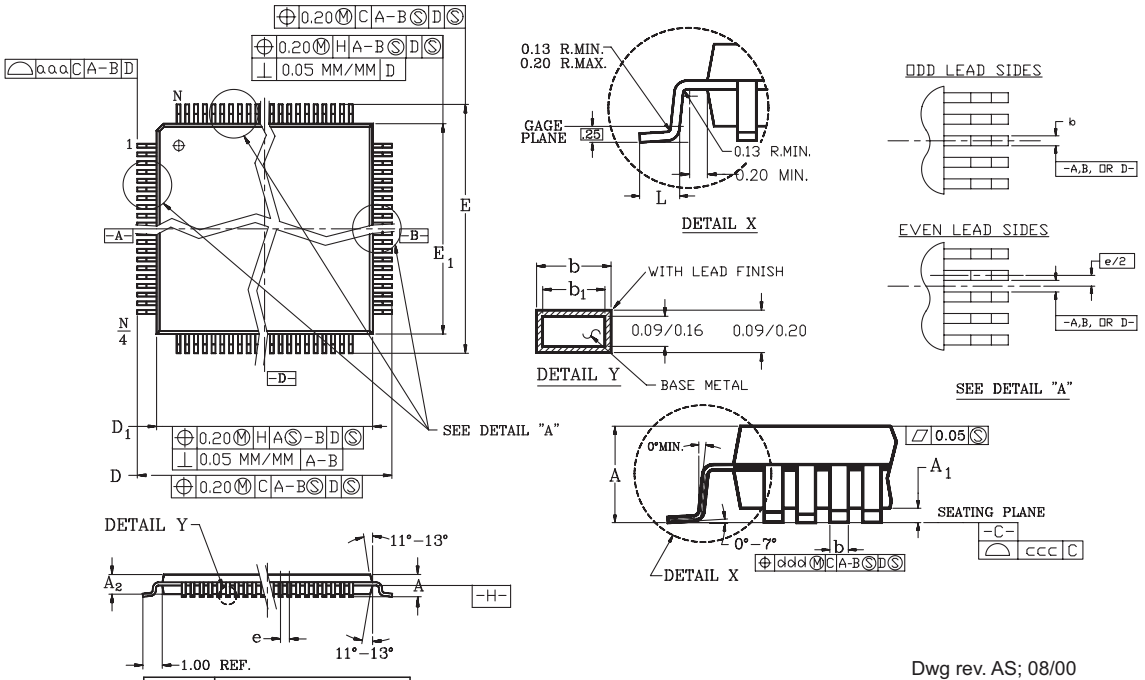
1 Input offset disabled.

*Power Up and Hardware Reset ($\overline{RST}$) Value = 0002h

# PHYSICAL DIMENSIONS

## 64-Pin TQFP

PQT 064




Dwg rev. AS; 08/00

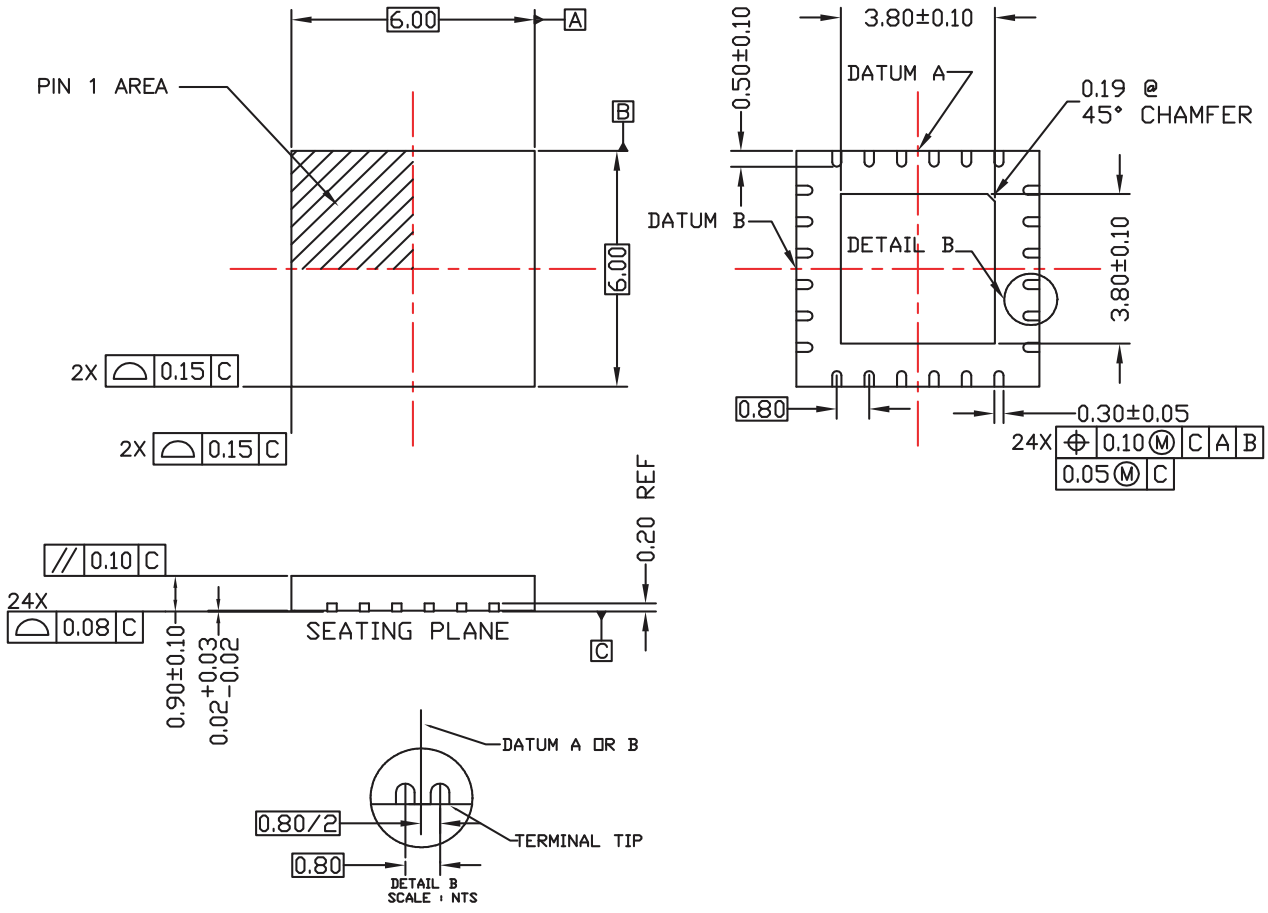
| PACKAGE | PQT 064 | | |
|---|---|---|---|
| JEDEC | MS-026 (C) ACD | | |
| SYMBOL | MIN | NOM | MAX |
| A | — | — | 1.20 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| D | 12.00 BSC | | |
| D1 | 10.00 BSC | | |
| E | 12.00 BSC | | |
| E1 | 10.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| N | 64 | | |
| e | 0.50 BSC. | | |
| b | 0.17 | 0.22 | 0.27 |
| b1 | 0.17 | 0.20 | 0.23 |
| TOLERANCES OF FORM AND POSITION | | | |
| ccc | 0.08 | | |
| ddd | 0.08 | | |
| aaa | 0.20 | | |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE -H- IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254mm PER SIDE. DIMENSIONS "D1" AND "E1" INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
4. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
5. CONTROLLING DIMENSIONS: MILLIMETER.
6. DIMENSIONS "D" AND "E" ARE MEASURED FROM BOTH INNERMOST AND OUTERMOST POINTS.
7. DEVIATION FROM LEAD-TIP TRUE POSITION SHALL BE WITHIN ±0.076 MM. FOR PITCH >0.5mm. AND WITHIN ±0.04 FOR PITCH ≤ 0.5 mm.
8. LEAD COPLANARITY SHALL BE WITHIN: (REFER TO 06-500)
   1- 0.10 mm FOR DEVICES WITH LEAD PITCH OF 0.65-0.80 mm.
   2- 0.076 mm FOR DEVICES WITH LEAD PITCH OF 0.50 mm.
   COPLANARITY IS MEASURED PER SPECIFICATION 06-500.
9. HALF SPAN (CENTER OF PACKAGE TO LEAD TIP) SHALL BE 15.30±.165{.602"±.0065"}
10. "N" IS THE TOTAL NUMBER OF TERMINALS.
11. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026.
13. THE 160 LEAD IS A COMPLIANT DEPOPULATION OF THE 176 LEAD MS-026 VARIATION BGA.

### 24-pin QFN

## 24 Lead QFN with Chamfer




| Symbol | 24 LEAD QFN | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 0.80 | 0.90 | 1.00 |
| A2 | | 0.57 REF | |
| b | 0.18 | 0.23 | 0.38 |
| D | | 6.00 BSC | |
| D2 | 3.70 | 3.80 | 3.90 |
| E | | 6.00 BSC | |
| E2 | 3.70 | 3.80 | 3.90 |
| e | | 0.80 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| N | | 24 | |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |

NOTES:
1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. ⌖ is in degrees.
3. N is the total number of terminals.
4. The Terminal #1 identifier and terminal numbering convention shall conform to JEP 95-1 and SSP-012. Details of the Terminal #1 identifier are optional, but must be located within the zone indicated. The Terminal #1 identifier may be either a mold or marked feature.
5. Coplanarity applies to the exposed pad as well as the terminals.
6. Reference Document: JEDEC MO-220.
7. Lead width deviates from the JEDEC MO-220 standard.

# REVISION HISTORY

## Revision A1 to B1

- Changed Le88830 package to 24-pin QFN, and changed OPN to Le88830KQC on front page.
- Updated *Le88830 Connection Diagram and Pin Descriptions*, on page 37
- Changed thermal data in *Absolute Maximum Ratings*, on page 38
- Corrected PCN code in command *73h Read Revision and Product Code Number (RCN,PCN)*, on page 80
- Replaced 24-eTSSOP with 24-QFN *Physical Dimensions*, on page 101

## Revision B1 to C1

- Updated the datasheet for Microsemi's logo and name for the entire document.

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