Le9540

Dual Ringing Subscriber Line Interface Circuit

VE950 Series

Data Sheet

Features

- Dual Architecture Integrates Two Channels of SLIC Functionality
- High Voltage High Bandwidth Design Supports 7-kHz Wide Band Applications
  - Up to –145 V ringing battery Le9540D
  - Up to –100 V ringing battery Le9540C
- Common Protection Reference Output
- Operation Control and Status Report through Serial Interface with Reset
  - SLIC Operation State/DC Current Limit/Test Load Enable
  - DC Loop Closure/Ring Trip/Thermal Shutdown
- Channel Independent Eight Operating States
  - Scan (Minimal Power Dissipation)
  - Active Forward (Default Power Up State)
  - Active Forward ICV
  - Active Reverse
  - Tip Open
  - Wink
  - Ringing
  - Disconnect
- Per Channel Ringing Inputs for Optimized Interface to BRCM SoC Devices
  - Accepts driving signals from per channel voice outputs as well as from PWM outputs
- DC Current Limited in Active/Scan/Tip Open States
- Loop Start, Ring Trip, and Ring-Ground Detections with two thresholds
- Thermal Shutdown Protection with Hysteresis
- Test Load Switch Supports integrated test algorithms

Applications

- Optimized design to work with BCM3383/85 Broadcom SoCs
- Short loop residential gateways

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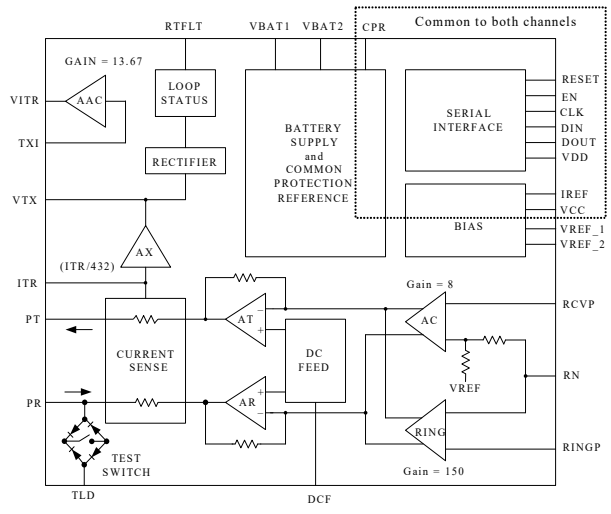
Ordering Information

Le9540CUQC	40-pin QFN	Tray
Le9540DUQC	40-pin QFN	Tray
Le9540CUQCT	40-pin QFN	Tape and Reel
Le9540DUQCT	40-pin QFN	Tape and Reel

1. All devices are in green packages.The green package is Halogen free and meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.

Description

The Le9540 Dual Ringing SLIC device is a dual-channel device optimized to provide battery feed, ringing, and supervision on voice loops found in short-loop VoIP applications. This device is optimized to interface to the Broadcom BCM3383/85 SoC, or equivalent. The SLIC operational control and status report for both channels are communicated through a serial interface with reset. The common protection reference output can trigger either a common protection device or per channel devices for both channels. The SLIC supports wide-band applications.



One channel shown unless otherwise specified

Figure 1 - Block Diagram

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Product Description

The Le9540 device is a dual-channel device optimized to provide battery feed, ringing, and supervision on short Plain Old Telephone Service (POTS) loops. This device is optimized to interface to Broadcom system-on-a-chip (SoC) device for cable modem applications.

Power Supplies

The Le9540 device is powered by a Vcc for analog circuits of both channels, a VDD for the serial logic circuits and a per channel VBAT for DC feed and power ringing. The maximum of VBAT is rated at –100 V for Le9540C and –145 V for Le9540D. The VBAT is expected to be a full tracking supply. The device depends on the tracking power supply to reduce the battery amplitude during off-hook conditions and by doing so may save overall operating power consumption. The VBAT should be no more negative than –100V for Le9540D other than in ringing mode. Also, when –145 V is used for ringing special care should be taken to prevent certain faults from happening, such as tip to ring, tip or ring to ground, or similar alike.

Operating States

The Le9540 device uses a voltage-feed-current-sense architecture. Each channel of this device has active, scan, tip open, wink and disconnect operation states. Power ringing is also provided to the subscriber loop through amplification of a low-voltage input. The active forward state with the low (ILL) dc current limit and the test switch turned off is the default power up state.

Active

There are three active states: Active Forward, Active Reverse and Active Forward ICV.

In the Active Forward state the DC feed voltage on PT is positive with respect to the voltage on PR. In the Active Reverse state the DC feed voltage on PT is negative with respect to the voltage on PR.

In the Active Forward ICV state the PT voltage is forced to be near -20V. The channel will be operating with an Increased Common mode Voltage (ICV).

The DC feed current is limited and can be programmed to either ILL or ILH. There is in the order of a 10 kΩ slope to the I/V characteristic in the current-limit region; thus, once in current limit, the actual loop current will increase slightly as loop length decreases.

For AC operation the SLIC supports off-hook talk mode and on-hook transmission mode as may be required during the quiet interval of ringing. The overhead is about 6 to 8 V, allowing for on-hook transmission of an undistorted signal of 3.14 dBm into 900 Ω, or 500mV of meter pulse.

Scan

Scan is a simple low-power operation state. It is designed primarily for on hook operation. It provides forward DC feed with the voltage on PT positive with respect to the voltage on PR. The loop closure detector is active. The DC feed current is limited and fixed. The AC transmission path and on-hook transmission are not active.

Tip Open

The Tip Open state is the Scan state with high impedance into PT.

Wink

The Wink state is an Active state but the voltages on PT and PR are forced to be the same and near ground.

Disconnect

Both PT and PR are in high impedance.

Ringing

In the Ringing state the signals on RINGP and RN are amplified and provided to the tip/ring pair as the power ringing signal. The signals on RINGP and RN may be a sine wave or a filtered square wave to produce a sine wave or trapezoidal output. A DC offset may also be applied.

The signals on RINGP and RN are desirable to be referenced to VREF or near VREF potential for maximum dynamic ranges on the inputs.

Communication Interface

A serial interface is used for device operational control and for device status reporting. For operational control through DIN, the operation state, dc current limit and test load switch operation can be set on a per channel basis. The upstream status reporting on DOUT are loop closure, ring trip and thermal shutdown. There are two loop closure outputs related to two detection thresholds, two ring trip detection outputs related to two detection thresholds, and one thermal shutdown indication for each channel.

The serial interface has a RESET which is active low. When the RESET pin is a logic 0 the device will enter its default state of active forward with the low (ILL) dc current limit and the test switch turned off. This operation controls both channel simultaneously. The RESET pin has an internal pull down.

Protection

A Common Protection Reference (CPR) output is available. It provides the gate reference voltage for a common shared protector or independent per line protectors for both channels. The reference voltage will be the more negative of VBAT1 and VBAT2. When the circuit is activated it will source at least 10mA of gate trigger current.

Thermal

The device is packaged in a small 40-pin QFN (6mm x 6mm). The Exposed Pad must be connected to a ground plane on the printed circuit board for thermal conduction. Also, the internal analog grounds and battery grounds are connected to the exposed pad, as well as to the GND pin. The single GND pin may not be sufficient for peak current return. The ground plane to which the exposed pad connects is used as analog signal ground and battery ground.

In case of reaching the thermal shutdown temperature, the channel will automatically enter an all off state. Upon cooling, the device will re-enter the state contained in the serial interface control registers. Hysteresis is built in to prevent fast oscillation. This is a self protection operation. Thermal shutdown will not cause performance degradation once the device goes back to normal operation.

Connection Diagram

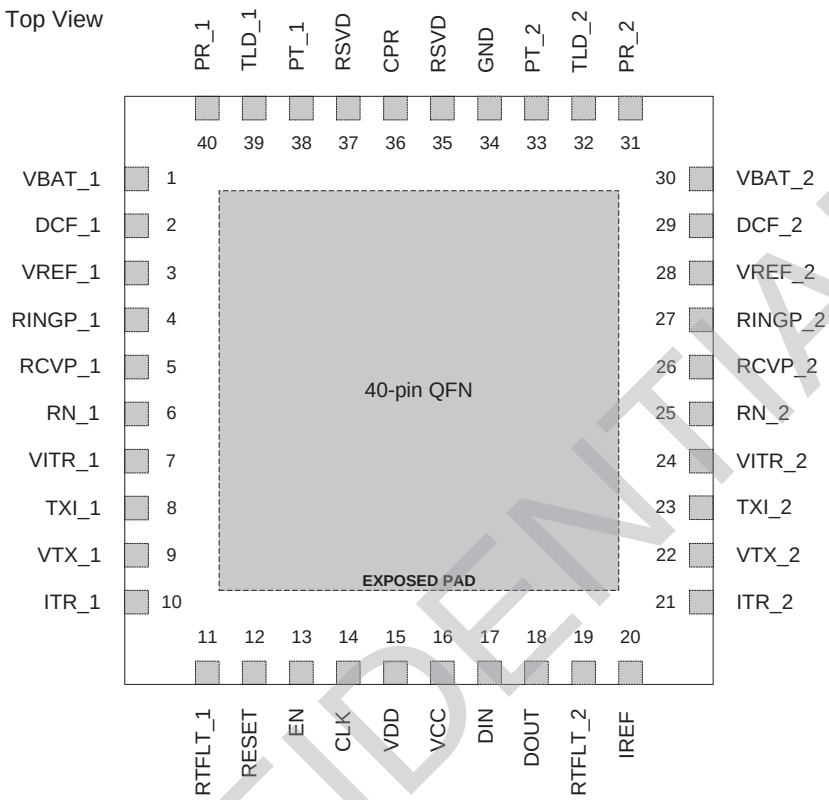


Figure 2 - 40 Pin QFN

Note: Exposed pad should be connected to the ground plane for electrical connection and thermal conduction.

Pin Descriptions

NAME_1 for channel 1 and NAME_2 for channel 2.

Pin Name	Type	Description
VITR_1 VITR_2	Output	**Transmit AC Output Voltage.** Output of internal AAC amplifier. This output is a voltage that is directly proportional to the differential AC tip/ring current.
RCVP_1 RCVP_2	Input	**Receive AC Signal Input (Non inverting).** This high-impedance input controls the AC differential voltage on tip and ring, for voice in Active states. This node is a floating input.
RN_1 RN_2	Input	**Receive AC Signal Input and Power Ringing Signal Input (Inverting).** In Active States this input, with reduced gain and referenced to V_{REF}, is paired with RCVP for voice transmission. In Ringing State this input is paired with RINGP with the same gain as that of RINGP.
RINGP_1 RINGP_2	Input	**Power Ring Signal Input (Non inverting).** Couple to a sine wave or lower crest factor low-voltage ring signal. The input here is amplified to provide the full power ring signal at tip and ring. This signal may be applied continuously, even during non-ringing states.
DCF_1 DCF_2	Input	**Filter Capacitor.** Connect a capacitor from this node to ground.
RTFLT_1 RTFLT_2	Input	**Ring Trip Filter.** Connect a capacitor to ground to filter the ring trip circuit to prevent spurious responses. A single-pole filter is needed.
VREF_1 VREF_2	Output	**SLIC Device Internal Reference Voltage.** Output of internal 1.5 V reference voltage.
IREF	Input	**SLIC Device Internal Reference Current**. Connect a 49.9 kΩ resistor to low noise analog ground.
VCC	Power	**Analog Power Supply**. 3.3 V typical.
VDD	Power	**Digital Power Supply**. 3.3V typical.
VBAT_1 VBAT_2	Power	**Battery Supply**. User adjusted supply per SLIC operation state and device grade.
PT_1 PT_2	Input/ Output	**Protected Tip.** The output drive of the tip amplifier and input to the loop-sensing circuit. Connect to loop through over-voltage and over-current protection.
PR_1 PR_2	Input/ Output	**Protected Ring.** The output drive of the ring amplifier and input to the loop sensing circuit. Connect to loop through over-voltage and over-current protection.
ITR_1 ITR_2	Input	**Transmit Gain.** Input to AX amplifier. Connect a 6.49 kΩ resistor from this node to VTX to set transmit gain of 205V/A.
VTX_1 VTX_2	Output	**DC and AC Output Voltage.** Output of internal AX amplifier. The voltage at this pin is directly proportional to the differential tip/ring current.
TXI_1 TXI_2	Input	**AC/DC Separation.** Input to internal AAC amplifier. Connect a capacitor from this pin to VTX.
TLD_1 TLD_2	Input	**Test Load**. A test load may be connected to this pin.

Pin Name	Type	Description
CPR	Output	**Common Protection Reference**. This output may be used as the protector gate reference point.
RESET	Input	**Reset.** When low it resets the SLIC and both channels will be in default mode. It comes with internal 100kΩ pull down.
EN	Input	**Enable**. Activate the serial interface operations.
CLK	Input	**Clock for the Serial Data Transmission**. Clock that runs the serial interface.
DIN	Input	**Data Input**. Data inputs of the serial interface.
DOUT	Output	**Data Output**. Data outputs of the serial interface.
RSVD		**Reserved**. Leave it floating on PCB layout.
GND	GND	**Ground**. Use together with the exposed pad as ground return.
Exposed Pad		**Thermal and Circuit Ground**. Connect to a ground plane on the printed circuit board for thermal conduction and electrical connection for ground return.

Absolute Maximum Ratings

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. T_A = 25 °C

Parameter	Symbol	Min.	Max.	Unit
DC Supply (V_{CC}, V_{DD})	Vcc, V_{DD}	–0.4	4.0	V
Battery Supply (V_{BAT}) (Le9540C, Le9540D Non-Ringing)	V_{BAT}	–110	GND	V
Battery Supply (V_{BAT}) (Le9540D Ringing)	V_{BAT}	–155 + Vcc	GND	V
Logic Input Voltage		–0.4	V_{DD} + 0.5	V
Logic Output Voltage		–0.4	V_{DD}+ 0.5	V
CPR Voltage (10 x 1000 µs)		–155 + Vcc	min(VBAT1, VBAT2) + 1	V
Operating Temperature Range		–40	125	°C
Storage Temperature Range		–40	150	°C
Relative Humidity Range		5	95	%
PT or PR Fault Voltage (DC)	V_{PT}, V_{PR}	V_{BAT} – 5	3	V
PT or PR Fault Voltage (10 x 1000 µs)	V_{PT}, V_{PR}	V_{BAT} – 15	15	V
ESD Immunity (Human Body Model)			JESD22 Class 1C compliant	

Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane. Thermal performance depends on number of PCB layers and the size of copper area. Continuous operation above 145°C junction temperature may degrade device reliability.

The typical thermal protection shutdown (TjC) temperature is 190°C, with minimum at 175°C.

Package Assembly

Green package devices are assembled with enhanced environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

Operating Ranges

Environmental Ranges

Microsemi guarantees the performance of this device over commercial (0 to 70º C) and industrial (-40 to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Ambient Temperature	–40° C < T_A < +85° C
Ambient Relative Humidity	5 to 95%

Electrical Ranges

Parameter	Min.	Typ.	Max.	Unit
3.3 V DC Supplies (V_{CC}, V_{DD})	3.13	3.3	3.47	V
Office Battery Supply (V_{BAT}) (Le9540C)	–100[1]	—	–12	V
Office Battery Supply (V_{BAT}) (Le9540D)	–100[1]	—	–12	V
Office Battery Supply (V_{BAT}) (Le9540D) (during ringing only)	–145[1]	—	–12	V

Note:

1. *Full tracking supply is expected during off hook and ringing operations. These maximum values may be the maximum on hook voltage or the peak voltage during ringing.*

Electrical Characteristics

Supply Currents

Values are per channel, unless otherwise specified. On-hook with no loop current. V_{DD} = Vcc = 3.3 V. Test switch is off.

Parameter	Min.	Typ.	Max.	Unit
Scan state, VBAT= –60 V:				
I_{VCC}	—	3.42	4.40	mA
I_{VBAT}	—	0.20	0.23	mA
Active state, Forward and Reverse, VBAT= –60 V:				
I_{VCC}	—	4.45	5.40	mA
I_{VBAT}	—	1.25	1.40	mA
Active state, Forward ICV state, VBAT= –60 V:				
I_{VCC}	—	4.60	5.60	mA
I_{VBAT}	—	1.33	1.50	mA
Active state, Forward and Reverse, VBAT= –21 V:				
I_{VCC}	—	4.45	5.40	mA
I_{VBAT}	—	1.20	1.35	mA
Disconnect state, VBAT= –60 V				
I_{VCC}	—	2.80	3.70	mA
I_{VBAT}	—	0.02	0.06	mA
Tip Open state, VBAT= –60 V				
I_{VCC}	—	3.20	4.00	mA
I_{VBAT}	—	0.17	0.21	mA
Wink state, VBAT= –60 V				
I_{VCC}	—	4.6	5.6	mA
I_{VBAT}	—	1.3	1.5	mA
Ring state, no load, V_{BAT}= –100 V (Le9540C)				
I_{VCC}	—	4.5	5.4	mA
I_{VBAT}	—	1.9	2.1	mA
Ring state, no load, V_{BAT}= –145 V (Le9540D)				
I_{VCC}	—	4.5	5.4	mA
I_{VBAT}	—	2.0	2.3	mA
All operation states (for both channels)				
I_{VDD}	—	2.0	2.3	mA

Power Dissipation

Values are per channel. On-hook with no loop current. V_{DD} = Vcc = 3.3 V. Test switch is off.

Parameter	Min.	Typ.	Max.	Unit
Scan state, V_{BAT}= –60 V	—	27	33	mW
Active state, Forward/Reverse, V_{BAT}= –60 V	—	93	106	mW
Active state, Forward ICV V_{BAT}= –60 V	—	99	113	mW
Active state, Forward/Reverse, V_{BAT}= –21 V	—	44	50	mW
Disconnect state, V_{BAT}= –60 V	—	14	20	mW
Tip Open state, V_{BAT}= –60 V	—	24	—	mW
Wink state, V_{BAT}= –60 V	—	97	—	mW
Ring state, no load, V_{BAT}= –100 V (Le9540C)	—	209	232	mW
Ring state, no load, V_{BAT}= –145 V (Le9540D)	—	308	355	mW

Line Characteristics

Unless specified the test condition is specified in Figure 5 - Le9540 Basic Test Circuit.

Typical values are characteristic of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not a part of the testing requirements. Minimum and maximum values apply across the operating temperature range and the entire battery range unless otherwise specified. Typical is defined as T_A=25º C, V_{DD} = Vcc = 3.3V, VBAT= –60V for scan and disconnect state, –30V for active states, –100V/–145V for ringing state (for Le9540C/D). Test Switch is OFF.

Parameter	Min.	Typ.	Max.	Unit
Tip or Ring Drive Current = DC + Longitudinal + Signal Currents, Active states[1]	105	—	—	mApk
Tip or Ring Drive Current = Ringing + Longitudinal, Ring state[1]	65	—	—	
Signal Current, Active states[1]	10	—	—	mArms
Longitudinal Current Capability per Wire (Longitudinal current is independent of DC loop current.)[1]	8.5	15	—	
Ringing Current (Tip-Ring Ringing Load 1386 Ω + 40 µF)[1]	29	—	—	
DC Loop Current Limit, Active States (Tip-Ring DC Load 300 Ω):				
ILL	22.5	23.5	24.5	mA
ILH	38	40	42	mA
DC Loop Current Limit, Scan State (Tip-Ring DC Load 300 Ω)	—	30	—	mA
DC Loop Current Limit, Tip Open State (300 Ω Ring to ground)	—	30	—	mA
DC Feed Resistance (at PT-PR, Active states, non-current limit)	—	40	—	Ω
Open Loop Overhead Voltages:				
Scan state: (VTIP – VRING) – VBAT	2	3.6	4.5	V
Active state: |(VTIP – VRING)| – VBAT	5.75	7.4	8.5	V
Wink state: |VTIP|, |VRING|		0.7	1.0	V
Ring state: |VTIP|, VRING – VBAT	—	3.0	—	V
Open Loop Voltage:				
Active Forward ICV state: PT	-23.0	-21.6	-20.0	V
Loop Closure Detection Threshold:				
Active/Scan states (LCL)	10	11	12	mA
Active/Scan states (LCH)	14	15	16	mA
Tip Open state (LCL)	8.5	11	12.5	mA
Tip Open state (LCH)	13.5	15	16.5	mA
Loop Closure Detection Threshold Hysteresis[2]:				
Active/Scan/Tip Open states	—	2.2	—	mA

Table 1 - Two-Wire Port

Parameter	Min.	Typ.	Max.	Unit
Longitudinal to Metallic Balance at Tip/Ring: Test Method: Q552 (11/96) Section 2.1.2 and *IEEE* ® 455: 200 Hz to 3.4 kHz[3]	52	—	—	dB
Metallic to Longitudinal (HARM) Balance[4]: 100 Hz to 4000 Hz	40	—	—	dB
PSRR 500 Hz to 3000 Hz (Active Forward/Reverse)[1]:				
VBAT	45	—	—	dB
Vcc	25	30	—	dB
V_{DD}	25	30	—	dB

Note 1: This parameter is not tested in production. It is guaranteed by design and device characterization.
Note 2: Refer to “Loop Closure and Ring Trip Detection Thresholds with Hysteresis”.
Note 3: Tested at 1kHz.
Note 4: Tested with DC signals.

Table 1 - Two-Wire Port

Parameter	Min.	Typ.	Max.	Unit
TXI				
Input impedance	—	100	—	kΩ
VTX and VITR				
Output Offset (VTX)	–10	0	10	mV
Output Offset (VITR)	—	—	100	mV
Output Drive Current (VTX) (sinking or sourcing)	300	—	—	µA
Output Drive Current (VITR) (sinking or sourcing)	10	—	—	µA
Output Voltage Swing:				
Maximum (VTX, VITR)	0	—	V_{CC}	V
Minimum (VTX)	+ 0.25	—	V_{CC} – 0.5	V
Minimum (VITR)	+ 0.35	—	V_{CC} – 0.4	V
Output Short-circuit Current (sinking or sourcing)	—	—	50	mA
Output Load Resistance[1]	10	—	—	kΩ
Output Load Capacitance[1]	—	20	—	pF
RN and RCVP (Active States):				
Input Voltage (V_{CC} = 3.3 V)				
RCVP	0	—[2]	V_{CC} – 0.3	V
RN	0	V_{REF}	V_{CC} – 0.3	V
Input Bias Current				
RCVP (sinking)	—	0.12	—	µA
RN (sinking[3] or sourcing[5])	—	0[4]	35	µA
Differential PT/PR Current Sense (RTFLT)[3]:				
Gain (PT/PR to RTFLT)	—	30	—	V/A
Total Harmonic Distortion (200 Hz—4 kHz)[1]:				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain (f = 1004 Hz, 1020 Hz)[6]				
PT/PR Current to VITR	–211	–205	–199	V/A
Receive Gain, f = 1004 Hz, 1020 Hz Open Loop				
RCVP to PT/PR	7.76	8.00	8.24	V/V
RN to PT/PR	3.34	3.44	3.54	V/V

Table 2 - Analog Pin Characteristics

Parameter	Min.	Typ.	Max.	Unit
Gain vs. Frequency (transmit and receive), 600 Ω Termination, 1004 Hz, 1020 Hz Reference[1]:				
200 Hz to 300 Hz	–0.3	0	0.05	
300 Hz to 3.4 kHz	–0.05	0	0.05	dB
3.4 kHz to 20 kHz	–3.0	0	0.05	
20 kHz to 266 kHz	—	—	2.0	
Gain vs. Level, 600 Ω Termination, Transmit +3dBm, Receive 0dBm Reference[1]:				
–55 dB to +3.0 dB	–0.05	0	0.05	dB
Idle-channel Noise (Tip/Ring), 600 Ω Termination:				
C-Message	—	8	13	dBrnC
Psophometric[1]	—	–82	–77	dBrnp
3 kHz Flat[1]	—	—	20	dBrn
Crosstalk between channels[1] (Tip-Ring, 0dBm/600Ω)				
Single frequency signal 1000 Hz	—	—	–80	dB
Single frequency signals 12 kHz, 16 kHz	—	—	–60	dB
CPR				
Output current (sourcing)				
min (VBAT1, VBAT2) - V_CPR = 2.5V	10	—	—	mA
Output Voltage				
min(VBAT1, VBAT2) - V_CPR	-0.5[7]	—	2.0[8]	V

Note 1: This parameter is not tested in production. It is guaranteed by design and device characterization.

Note 2: The RCVP input is floating. However, referencing it to VREF is recommended since RN is internally referenced to VREF.

Note 3: RN = 0V

Note 4: RN = V_{REF}

Note 5: RN = V_{CC}-0.3V

Note 6: VITR transconductance depends on the resistor from ITR to VTX. This gain assumes an ideal 6.49 kΩ, (the recommended value). Positive current is defined as the differential current flowing from PT to PR.

Note 7: Steady state no current.

Note 8: When output current is 1mA.

Table 2 - Analog Pin Characteristics

Parameter	Min.	Typ.	Max.	Unit
RINGP/RN (Ringing State): Input Voltage Swing	0	—	V_{CC}	V
Ring Signal Isolation: PT/PR to VITR Ringing state	—	60	—	dB
Ring Signal Isolation: RINGP to PT/PR Non-ringing state	—	80	—	dB
Ring Signal Distortion[1]: For Le9540C V_{BAT} = –100 V, RINGP/RN = 0.6 Vpp, Open Loop or 5 REN (1386Ω + 40µF) with DC loop 0 to 100Ω	—	3	—	%
For Le9540D V_{BAT} = –145 V, RINGP/RN = 0.9 Vpp, Open Loop or 5 REN (1386Ω + 40µF) with DC loop 0 to 100Ω	—	3	—	%
Differential Gain RINGP/RN to PT/PR For Le9540C V_{BAT} = –100 V, RINGP/RN = 0.6 Vpp, Open Loop	124	130	136	V/V
For Le9540D V_{BAT} = –145 V, RINGP/RN = 0.9 Vpp, Open Loop	124	130	136	V/V
Note 1: This parameter is not tested in production. It is guaranteed by design and device characterization.				

Table 3 - Ringing Parameters

Parameter	Min.	Typ.	Max.	Unit
Ring Trip (RTL):	50.5	52.5	54.5	mA
Ring Trip (RTH):	59.5	62.0	64.5	mA
Trip Time (f = 20 Hz) [1]	—	—	100	ms
Hysteresis (Relative to RTL or RTH)[1, 2]	—	1/3	—	
Note 1: This parameter is not tested in production. It is guaranteed by design and device characterization. Note 2: Refer to “Loop Closure and Ring Trip Detection Thresholds with Hysteresis”.				

Table 4 - Ring Trip

Item	Condition	Min.	Typ.	Max.	Unit.
Test Switch	ON-Resistance, (V(25 mA) – V(20 mA)) / 5 mA	10	19	30	Ω
	On-Voltage drop at ±20 mA[1]	–3	—	+3	V
	Off-state Leakage Current (sinking or sourcing)	—	—	5	µA
Note 1: Additional 10% variations to the minimum and maximum limits at -40° C.					

Table 5 - Test Switch

Serial Interface Characteristics

The electrical characteristics of the serial interface are shown in table 6.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Voltages (DIN, CLK, EN)					
Low Level	V_{IL}			0.8	V
High Level	V_{IH}	2.0	—	V_{DD}	V
Input Current (DIN, CLK, EN)					
Low Level (ground) (sourcing)	I_{IL}			60	µA
High Level (V_{DD}) (sinking)	I_{IH}			1	µA
Output Voltages (DOUT) (Interfacing to a 2.5V input)					
Low Level	V_{OL}			0.55	V
High Level	V_{OH}	2.0		2.6[1]	V
Rising/Falling Time (DOUT) (20% to 80%) with 20pF load	T_R, T_F			100[2]	ns
RESET High Current (at 2.5V) (sinking)	I_{IH}			40	µA

Note 1: Depending on the characteristic of the input that DOUT will be driving an external pull down resistor may be required to keep DOUT below the specified voltage for speedy operation.

Note 2: This parameter is not tested in production. It is guaranteed by design and device characterization.

Table 6 - Serial Interface Electrical Characteristics

The serial interface timing characteristics are shown in Figure 3. The details are in Table 7.

Symbol	Description	Min.	Typ.	Max.	Unit
1	CLK Period	1			µs
2	CLK falling to ENable going high	0			ns
3	ENable going high to CLK rising	300			ns
4	CLK falling to ENable going low	0			ns
5	ENable going low to CLK rising	170			ns
6	Data ready	200			ns
7	Data hold	200			ns
8	Enable rising to DOUT0 data available			420	ns
9	CLK rising to DOUT1+ data available			350	ns
10	CLK, EN rising time (20% to 80%)			25	ns
11	CLK, EN falling time (20% to 80%)			25	ns

Note that the parameters in table 7 are not tested in production. They are guaranteed by design and device characterization.

Table 7 - Serial Interface Timing Characteristics

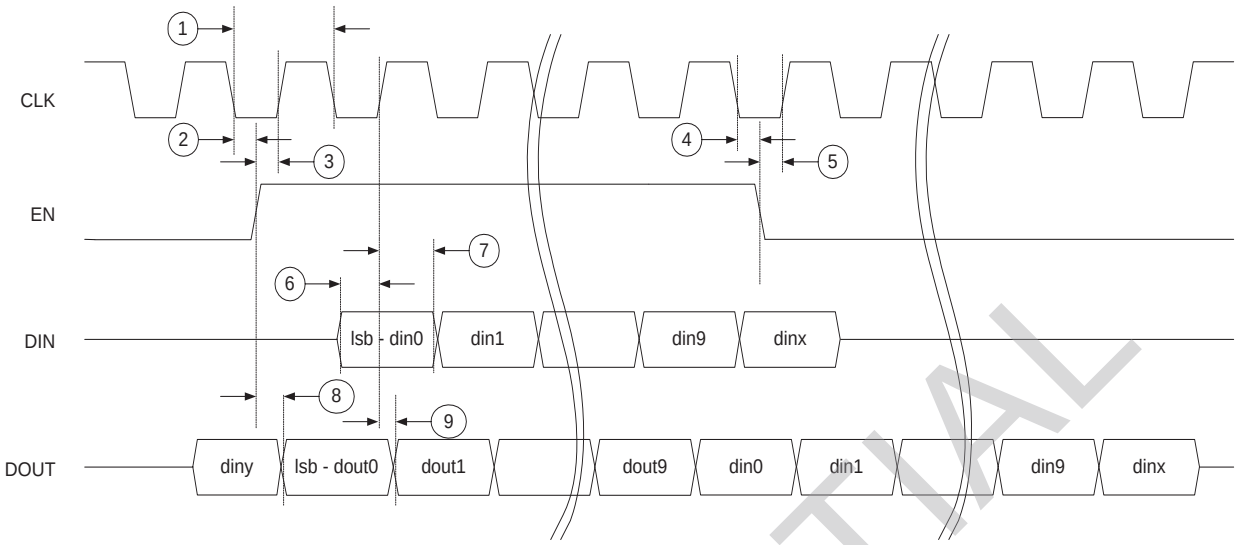


Figure 3 - Serial Interface Timing Diagram

Serial Interface Operations and Definitions

The serial interface has a 10-bit serial shift register and a 10-bit parallel data latch register that controls the SLIC operations. The logic diagram is shown in Figure 4.

Serial Interface Operations

The operation of the serial interface can be described in the following four modes, RESET High Enable No Transition, RESET High Enable Going High, RESET High Enable Going Low and RESET Low.

RESET High Enable No Transition

When RESET is high and there is no recent low-to-high transition on Enable the content in the shift register is continuously moving from DIN to DOUT by CLK. DOUT is continuously repeating DIN delayed by 10 CLK cycles.

Regardless of the CLK status, device state changes are not loaded with the Enable state held static. Data already loaded to the shift register may be reloaded without disrupting the SLIC channel line state.

RESET High Enable Going High

When RESET is high a low-to-high transition on Enable loads the parallel 10 status bits into the shift register, overwriting the previous 10 bit content in the shift register. The first lsb of the 10-bit device status word will immediately appear on the DOUT pin. Subsequent clock edges will continue to shift the status word out until all 10 bits have been presented, as which time the DOUT will return to repeat DIN delayed by 10 CLK cycles.

The second rising edge of CLK after Enable goes high CLK will clock in (new) data from DIN.

RESET High Enable Going Low

When RESET is high a high-to-low transition on Enable latches control bits from the serial shift register (with the content at that instant) into the SLIC parallel control register and immediately take effect.

New control data transactions are only triggered by such a transition on the Enable pin.

RESET Low

When RESET is low it over-writes the content in the SLIC parallel control register and set the control register to “0000 0000 00". Both channels of the SLIC are put into a default mode of active forward with ILL current limit and the test switch off. When RESET is low the operation of Enable is frozen such that the contents in the serial shift register will not be loaded into the SLIC parallel control registers and the status bits will not be loaded into the serial shift register. Asserting RESET does not clear the contents of the shift register. The content in the serial shift register will move from DIN to DOUT by CLK when RESET is low and Enable is low. If Enable is high during the period when RESET is low the content in the shift register will not move from DIN to DOUT by CLK. The content in the shift register will not change.

The RESET function is not included in Figure 4.

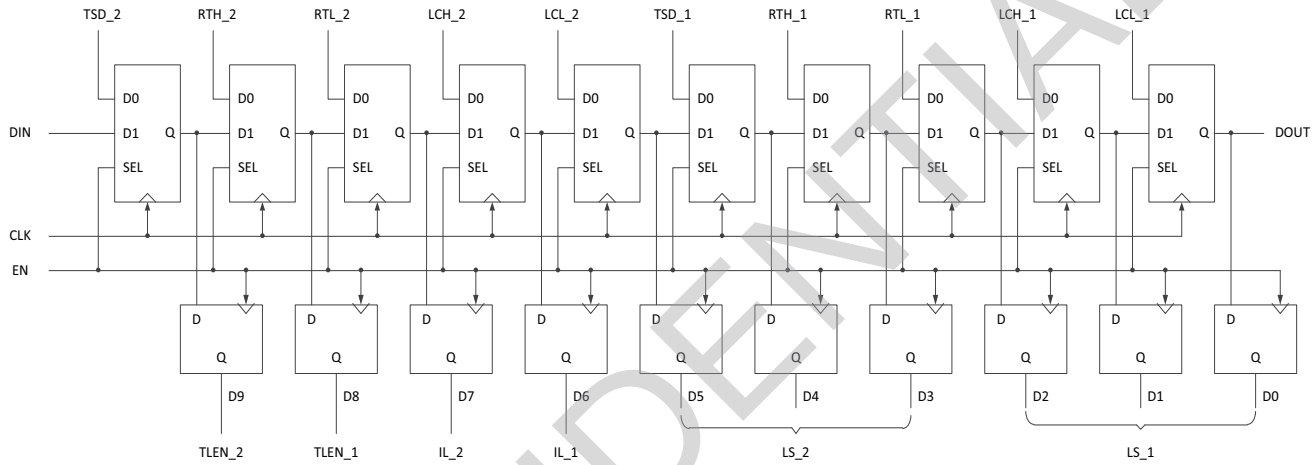


Figure 4 - Serial Interface Logic Diagram

Bit Assignments

The bit assignments for DIN are defined in Table 8. The bit assignments for DOUT are defined in Table 9. “1” stands for channel 1 and “2” stands for channel 2.

d0	d1	d2	d3	d4	d5	d6	d7	d8	d9
LS_1			LS_2			IL_1	IL_2	TLEN_1	TLEN_2

Table 8 - Serial Interface Input Arrangements

d0	d1	d2	d3	d4	d5	d6	d7	d8	d9
LCL_1	LCH_1	RTL_1	RTH_1	TSD_1	LCL_2	LCH_2	RTL_2	RTH_2	TSD_2

Table 9 - Serial Interface Output Arrangements

Line State (LS)

000: Active Forward (Normal)

001: Active Forward ICV (Increased Common mode Voltage)

010: Active Reverse (Normal)

011: Wink

110: Tip Open

100: Scan

101: Ringing

111: Disconnect

(in the sequence of d0/d1/d2 and d3/d4/d5 so scan state d0=1 or d3=1)

DC Current Limit (IL)

0: DC current limit is set to be ILL

1: DC current limit is set to be ILH

Test Load ENable (TLEN)

0: test load switch disabled and the test load is not turned on

1: test load switch enabled and the test load is turned on

Thermal ShutDown (TSD)

0: thermal shutdown

1: no thermal shutdown

Loop Closure with Low Detection Threshold (LCL)

0: dc loop current is greater than LCL threshold[1]

1: dc loop current is smaller than LCL threshold[1]

Loop Closure with High Detection Threshold (LCH)

0: dc loop current is greater than LCH threshold[1]

1: dc loop current is smaller than LCH threshold[1]

Ring Trip with Low Detection Threshold (RTL)

0: rectified and filtered loop current is greater than RTL threshold[1]

1: rectified and filtered loop current is smaller than RTL threshold[1]

Ring Trip with High Detection Threshold (RTH)

0: rectified and filtered loop current is greater than RTH threshold[1]

1: rectified and filtered loop current is smaller than RTH threshold[1]

Note: 1. Refer to "Loop Closure and Ring Trip Detection Thresholds with Hysteresis" for additional details.

Test Circuit

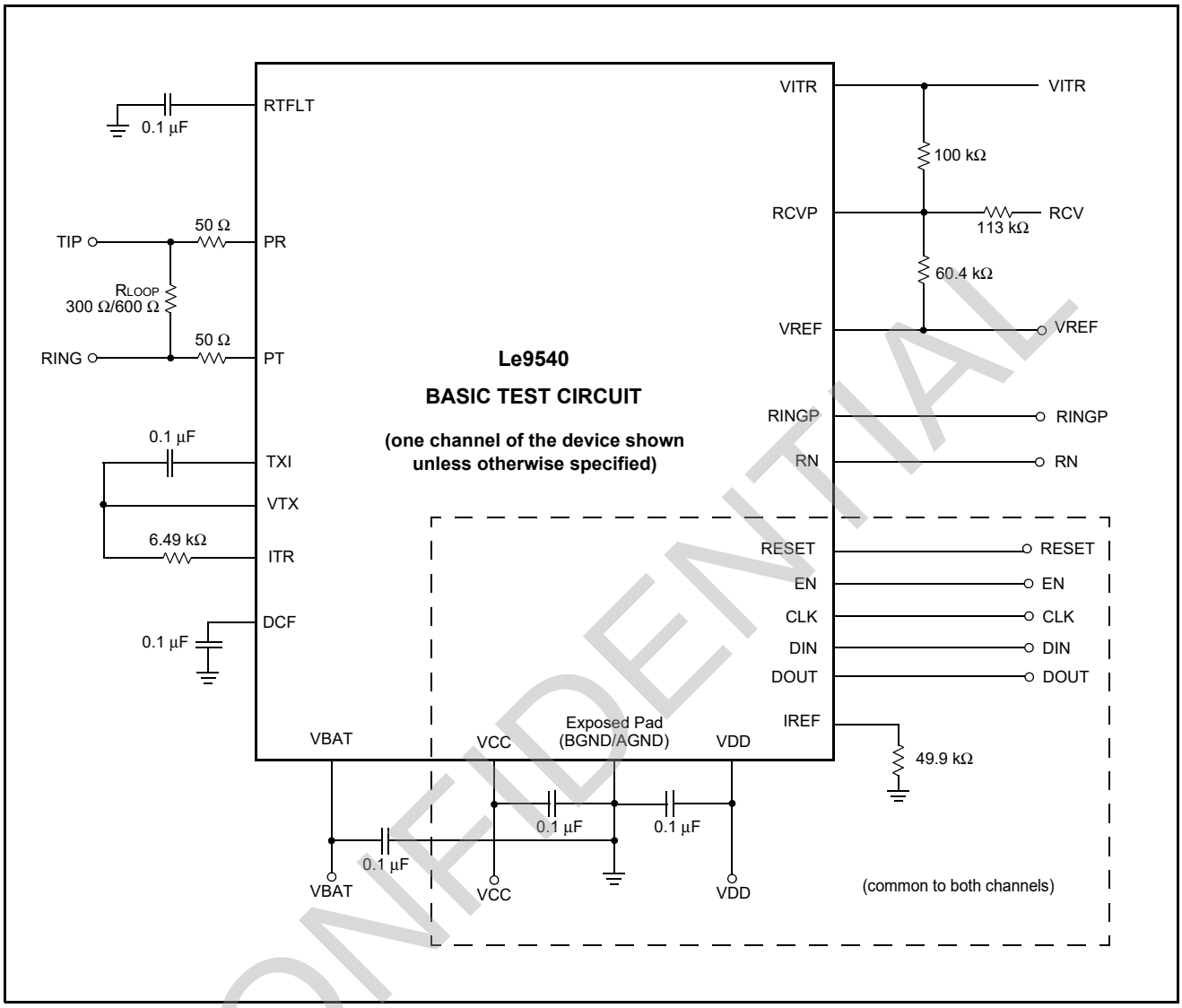


Figure 5 - Le9540 Basic Test Circuit

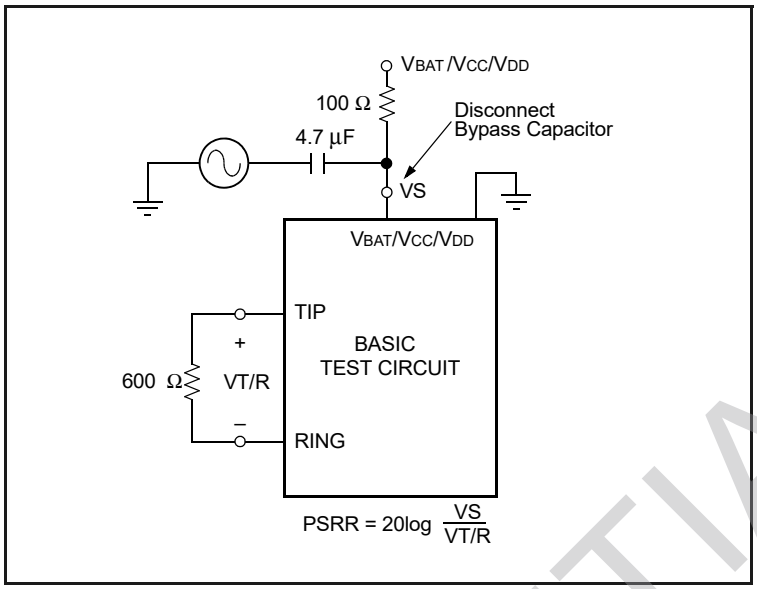


Figure 6 - Metallic PSRR

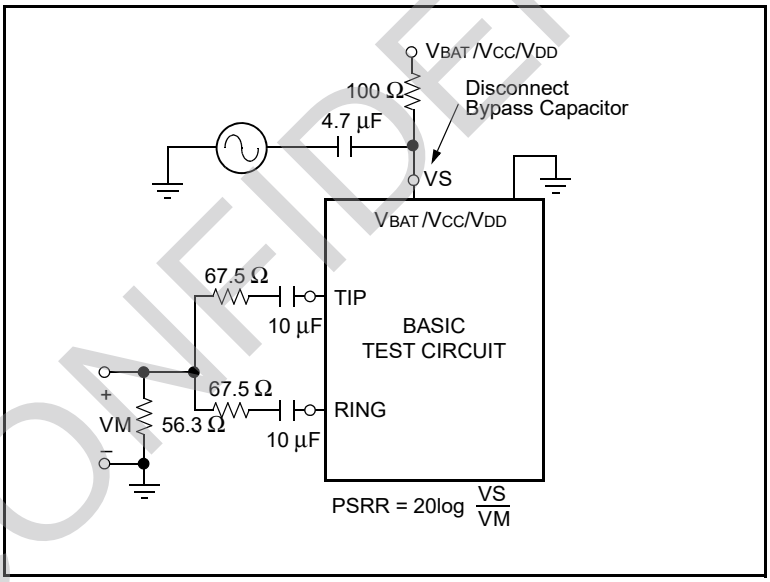


Figure 7 - Longitudinal PSRR

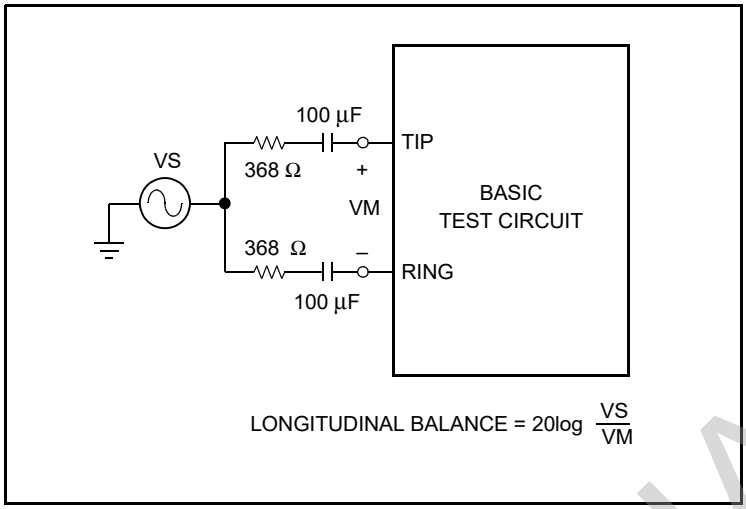


Figure 8 - Longitudinal Balance

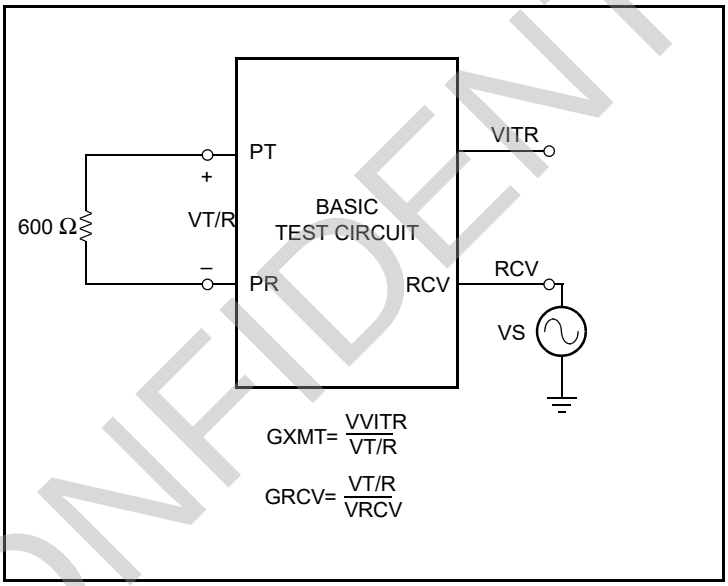


Figure 9 - AC Gains

Applications

In-rush Control

In the Active or Scan states there will be a transient response of the current-limit circuit upon an on- to off-hook transition that is described in the table below.

Parameter	Value	Unit
DC Loop Current: R_{LOOP} = 100 Ω, On- to Off-hook Transition time < 5 ms	ILIM + 60	mA
DC Loop Current: R_{LOOP} = 100 Ω, On- to Off-hook Transition time < 50 ms	ILIM + 20	mA
DC Loop Current: R_{LOOP} = 100 Ω, On- to Off-hook Transition time < 300 ms	ILIM	mA

Table 10 - Typical Active or Scan state On-Hook to Off-Hook Tip/Ring Current-Limit Transient Response

Loop Closure and Ring Trip Detection Thresholds with Hysteresis

Both loop closure and ring trip detections have a programmable threshold and hysteresis. The detection threshold is the point where the current is large enough for loop closure or ring trip to be detected. Once loop closure or ring trip is detected lowering the current will not immediately clear the detection until the current is below the programmed threshold minus the hysteresis.

For loop closure detection the “current” is the rectified loop current. For ring trip detection the “current” is the rectified and filtered loop current.

Figure 10 shows the characteristic graphically.

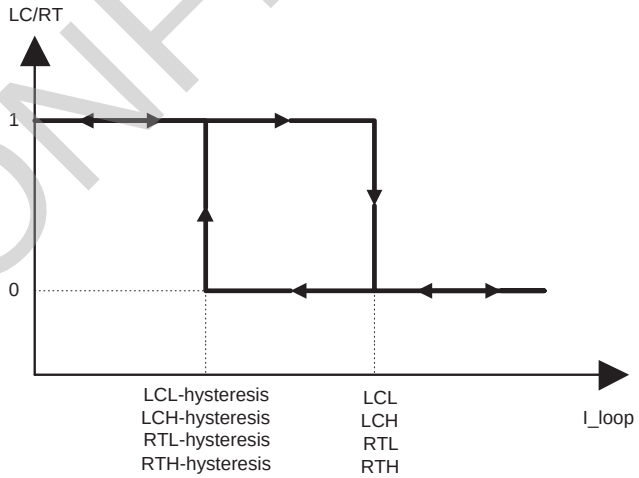


Figure 10 - Detection Thresholds with Hysteresis

All detectors are active regardless of the operational state.

Protection

The SLIC can be protected by using voltage referenced protectors, as shown in Figure 11 and 12. The protector can be a dual or two singles. In Figure 11, the gate references to VBAT. In Figure 12, the two gates reference to the same CPR pin. A shared protection scheme is shown in Figure 13 where one SCR is used alone with steering diodes.

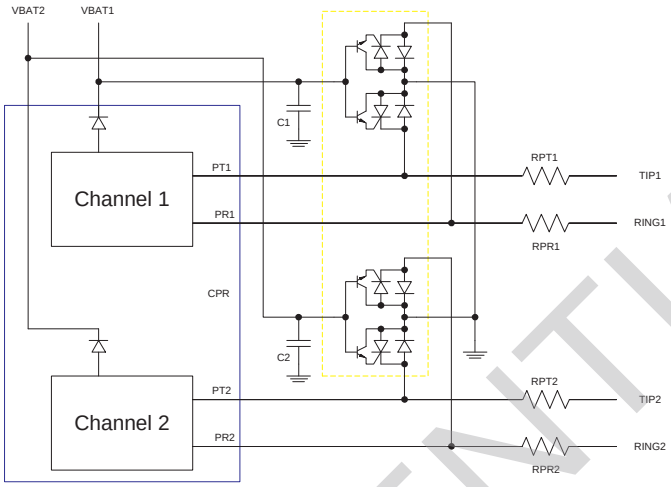


Figure 11 - Protection Device Referenced to VBAT

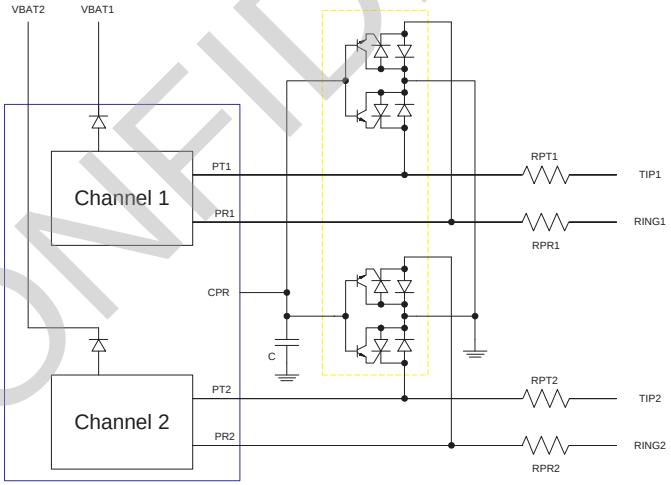


Figure 12 - Protection Device Referenced to CPR

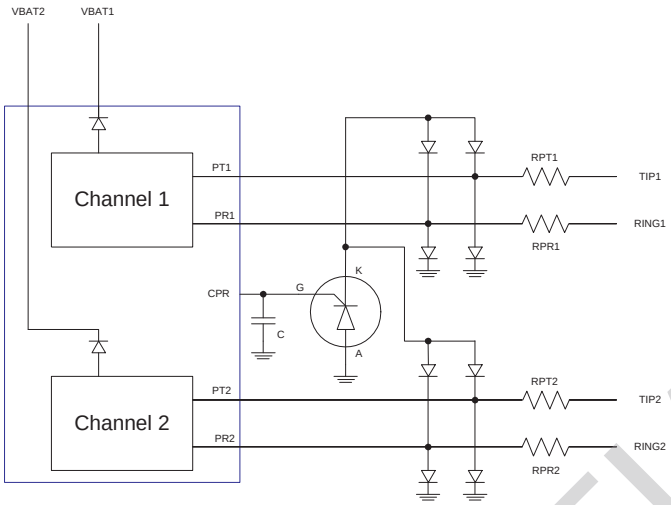


Figure 13 - Shared Protection Device Referenced to CPR

Design Examples

The following circuit shows the SLIC interface to the *Broadcom* BCM3383/85. One channel of the SLIC device is shown. Components with i being 1 are for channel 1 and with i being 2 for channel 2. This circuit has a natural 703-Ω AC termination impedance. The *Broadcom* IC has programmable registers to modify the external 703-Ω termination to any other real or complex terminations, as well as to set transmit and receive gains, and other AC parameters, such as parameters for 7kHz wide-band applications. The *Broadcom* IC also drives ringing inputs, sets SLIC operation states, and monitors line status. The voltage of the battery supply to the SLIC V_{BAT} is expected to be properly set and may vary depending upon SLIC operational states. The ringing maybe driven by the same voice outputs. The details of the protection are not shown. A complete reference design is available from Broadcom.

Contact your Microsemi account representative for assistance with other applications.

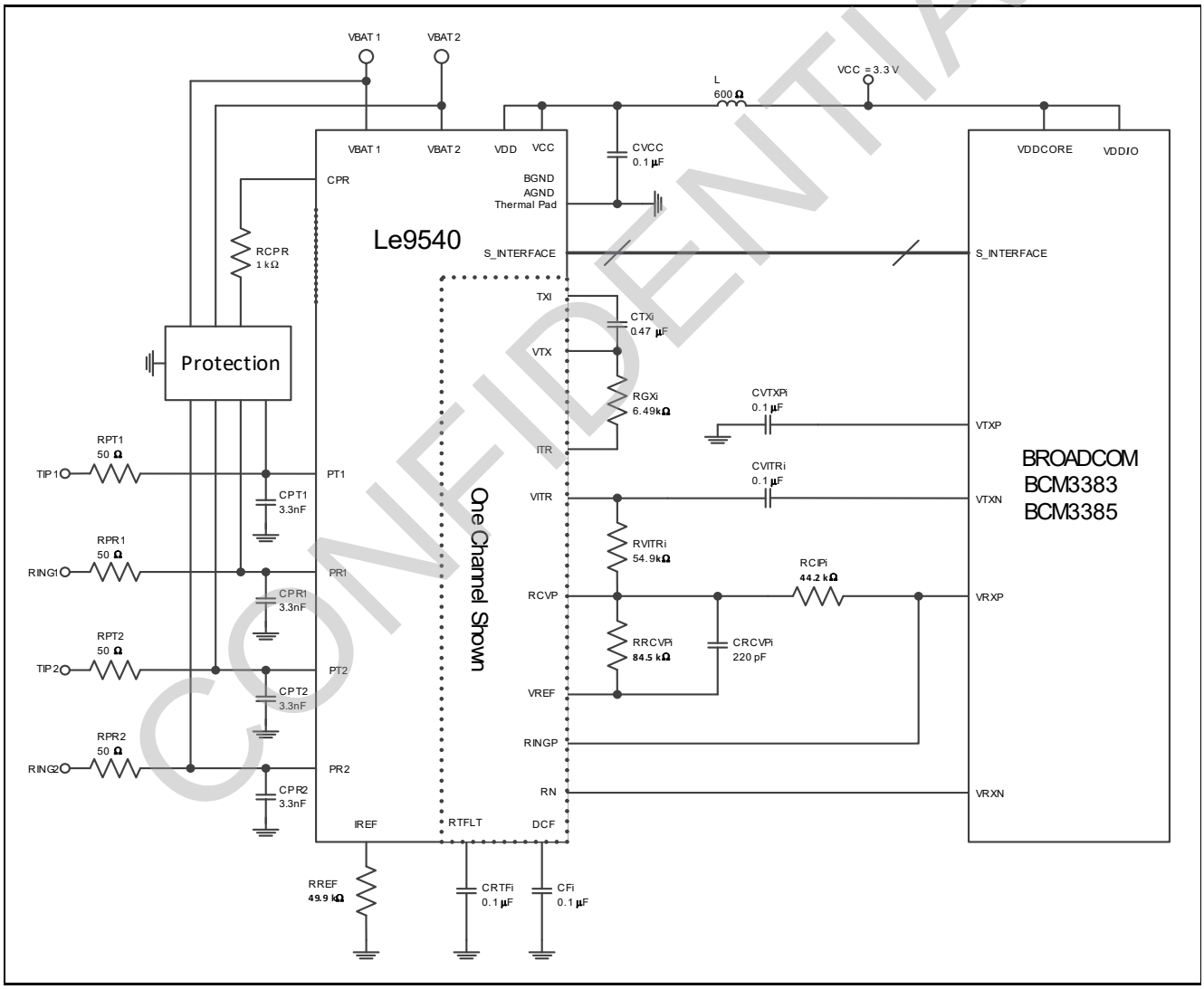


Figure 14 - Reference Schematic Interfacing Broadcom Codec

Application Circuit Parts List

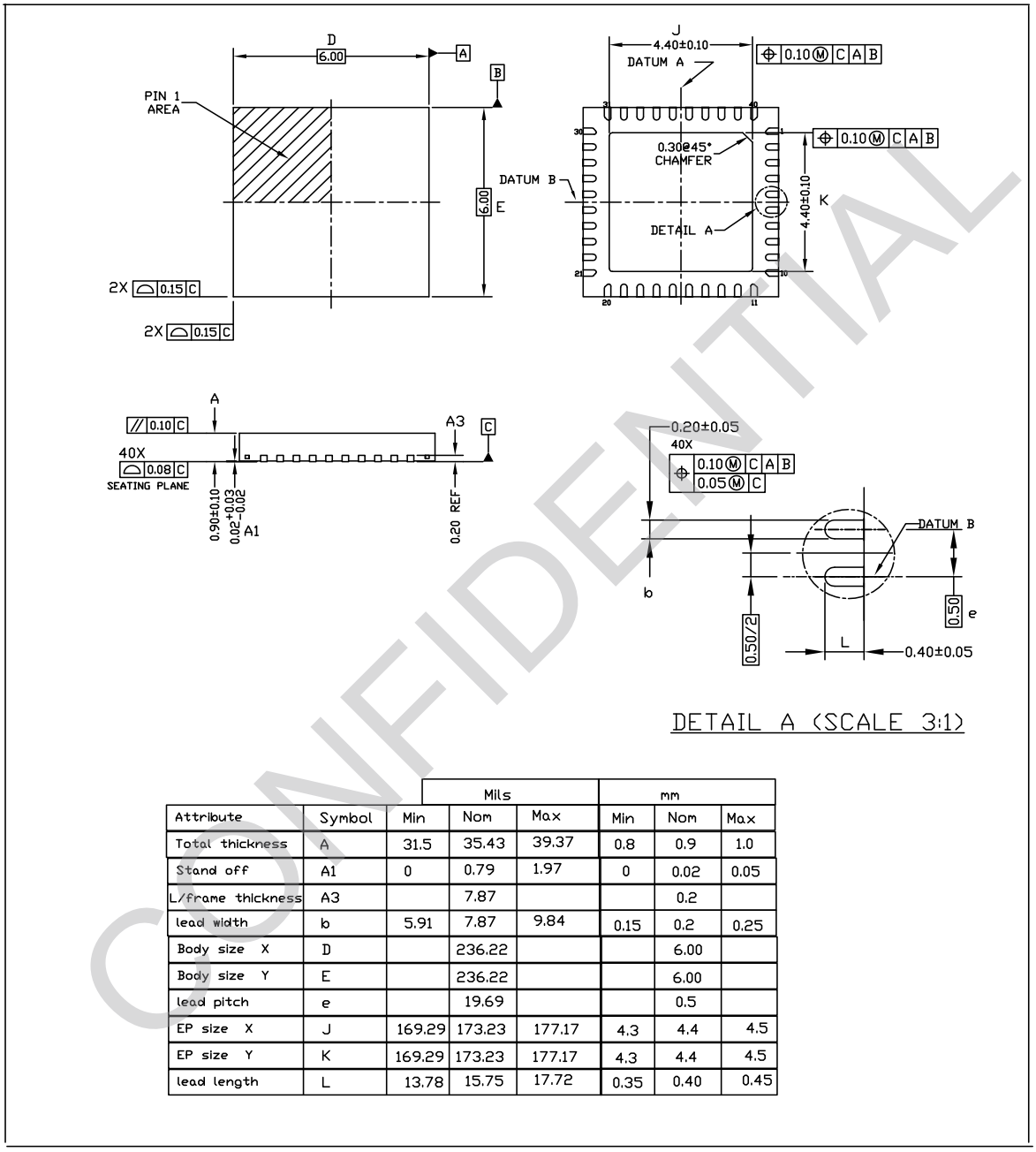
The following parts list is for the Microsemi Le9540 SLIC device and Broadcom BCM3383/85 fully programmable codec. Components ends with “i” are channel independent (i = 1 will for channel 1and i = 2 will for channel 2).

Item	Type	Value	Tolerance	Rating	Comments
Following Components Are For Both Channels					
Protection					Consult Microsemi for a recommendation. May contain one or two capacitors
RCPR	Resistor	1 kΩ	1%	0402	Use with CPR pin
CVCC	Capacitor	0.1 µF	20%	10 V	Ceramic bypass capacitor
L		600 Ω, *Murata*® BLM11A601SPB	—	—	Ferrite Bead for filtering
RREF	Resistor	49.9 kΩ	1%	1/16 W	Sets internal reference current
Le9540	SLIC	—	—	—	Dual-channel SLIC device
Following Components Are Per Channel					
RPTi	Resistor	50 Ω[1]	20% absolute 1% mismatch	Fusible or PTC	Protection resistor
RPRi	Resistor	50 Ω[1]		Fusible or PTC	Protection resistor
CRTFi	Capacitor	0.1 µF	20%	10 V	Ring trip filter capacitor
CFi	Capacitor	0.1 µF	20%	100 V	DC feed filter capacitor
RGXi	Resistor	6.49 kΩ	1%	1/16 W	Sets trans-impedance
CTXi	Capacitor	0.47 µF	20%	10 V	AC/DC separation
CVITRi	Capacitor	0.1 µF	20%	10 V	DC blocking capacitor
RVITRi	Resistor	54.9 kΩ	1%	1/16 W	AC interface
RCIPi	Resistor	44.2kΩ	1%	1/16 W	AC interface
RRCVPi	Resistor	84.5 kΩ	1%	1/16 W	AC interface
CRCVPi	Capacitor	220 pF	20%	10 V	AC interface
CVTXPi	Capacitor	0.1 µF	20%	10 V	AC interface
CPTi	Capacitor	3.3 nF[2]	20%	200V	EMC
CPRi	Capacitor	3.3 nF[2]	20%	200V	EMC
Note 1: Minimum 40Ω required for loop stability. Note 2: Consult Microsemi for further enhanced performance.					

Physical Dimensions

40-Pin QFN

Note: Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.



		Mils			mm		
Attribute	Symbol	Min	Nom	Max	Min	Nom	Max
Total thickness	A	31.5	35.43	39.37	0.8	0.9	1.0
Stand off	A1	0	0.79	1.97	0	0.02	0.05
L/frame thickness	A3		7.87			0.2	
lead width	b	5.91	7.87	9.84	0.15	0.2	0.25
Body size X	D		236.22			6.00	
Body size Y	E		236.22			6.00	
lead pitch	e		19.69			0.5	
EP size X	J	169.29	173.23	177.17	4.3	4.4	4.5
EP size Y	K	169.29	173.23	177.17	4.3	4.4	4.5
lead length	L	13.78	15.75	17.72	0.35	0.40	0.45

Revision History

Version 1 to Version 2

- Added a note in Table 6 on page 18.
- Added RCPR in Figure 14 on page 28 and the table on page 29.
- Updated ring trip thresholds in Table 4 on page 17.
- Updated descriptions to PSRR in Table 1 on page 14.

Version 2 to Version 3

- Data sheet status to “Advanced”.
- Added comments that the SLIC is good for wide-band applications on page 1.

Version 3 to Version 4

- Data sheet status to final "Data Sheet".
- Added Microsemi Logo

Version 4 to Version 5

- Updated descriptions regarding OPN on page 1.
- Tabe 6 on page 18, digital signals are referenced to VDD instead of VCC.
- Updated notes for the table "Application Circuit Parts List" on page 29.

Version 5 to Version 6

- Updated the document logo
- Updated the document number with DMS Document Code on page 1.
- Table 2 on page 16, Gain vs. Level, updated "0dBV Reference" to "Transmit +3dBm and Receive 0dBm Reference".

Version 6 to Version 7

- Updated Loop Closure Detection Threshold for Tip Open state (LCL) in Table 1 on page 13. The specification for the minimum value is changed from 9.5mA to 8.5mA.

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