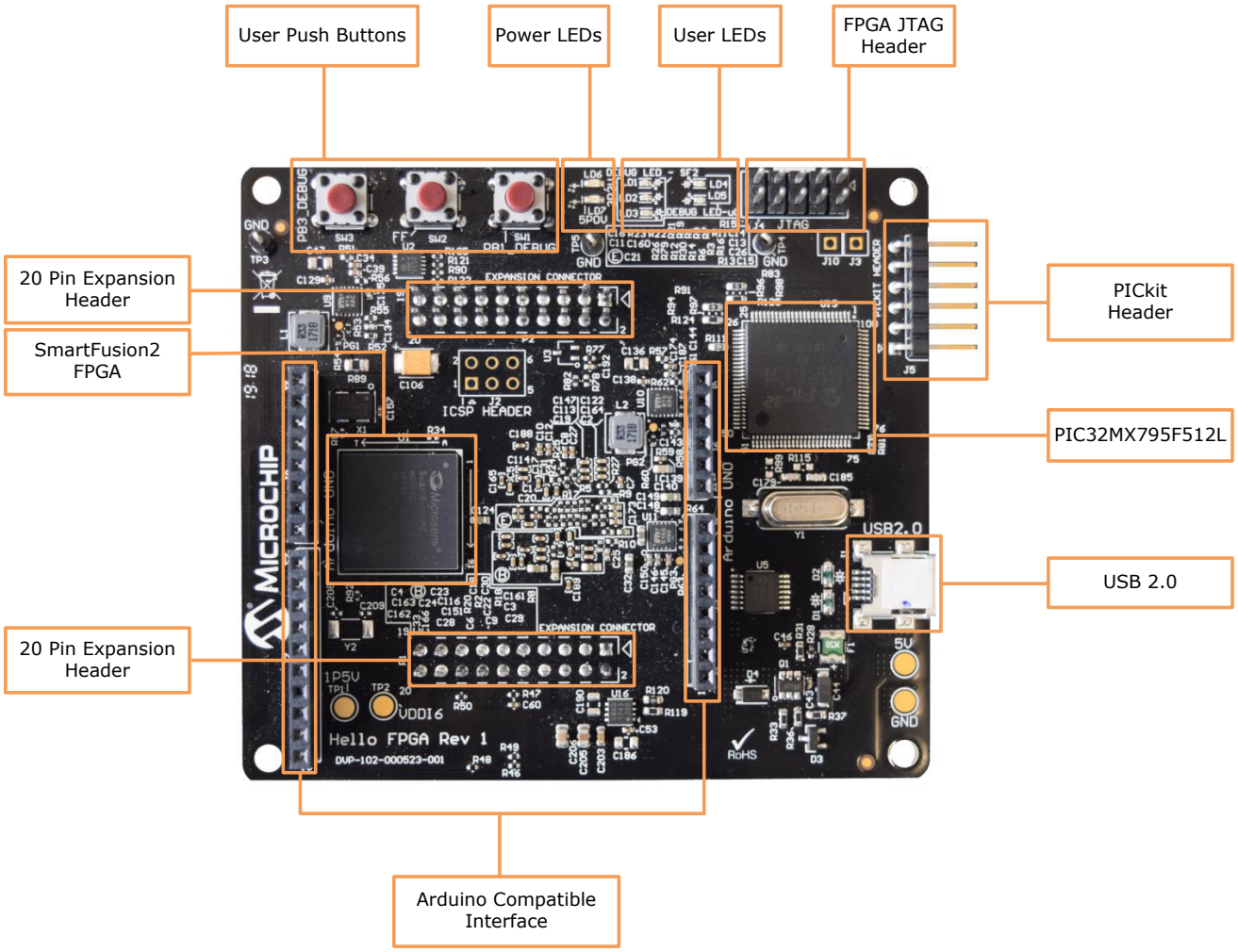
Hello FPGA
Quickstart Guide

Kit Contents

Quantity	Description
1	Hello FPGA Board with SmartFusion®2 M2S010 VF256
1	Camera Sensor Board
1	LCD Board
1	USB 2.0 A to Mini-B cable

Hardware Connectivity

Hello FPGA Board Layout

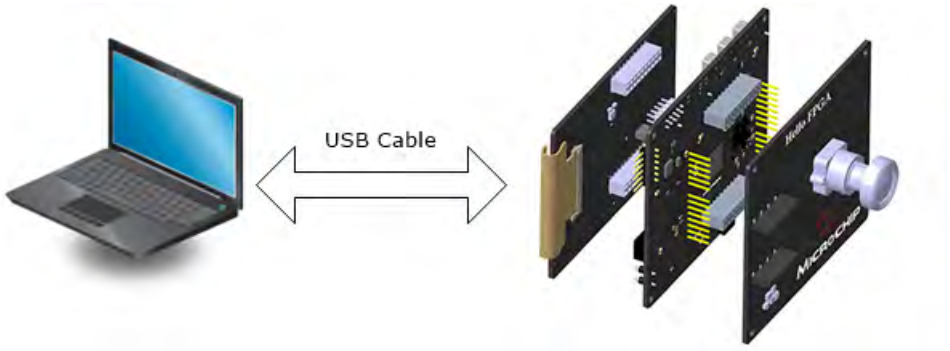


Prerequisite

Before you start, download and install the Hello FPGA GUI Application from the resources section of the Hello FPGA web page.

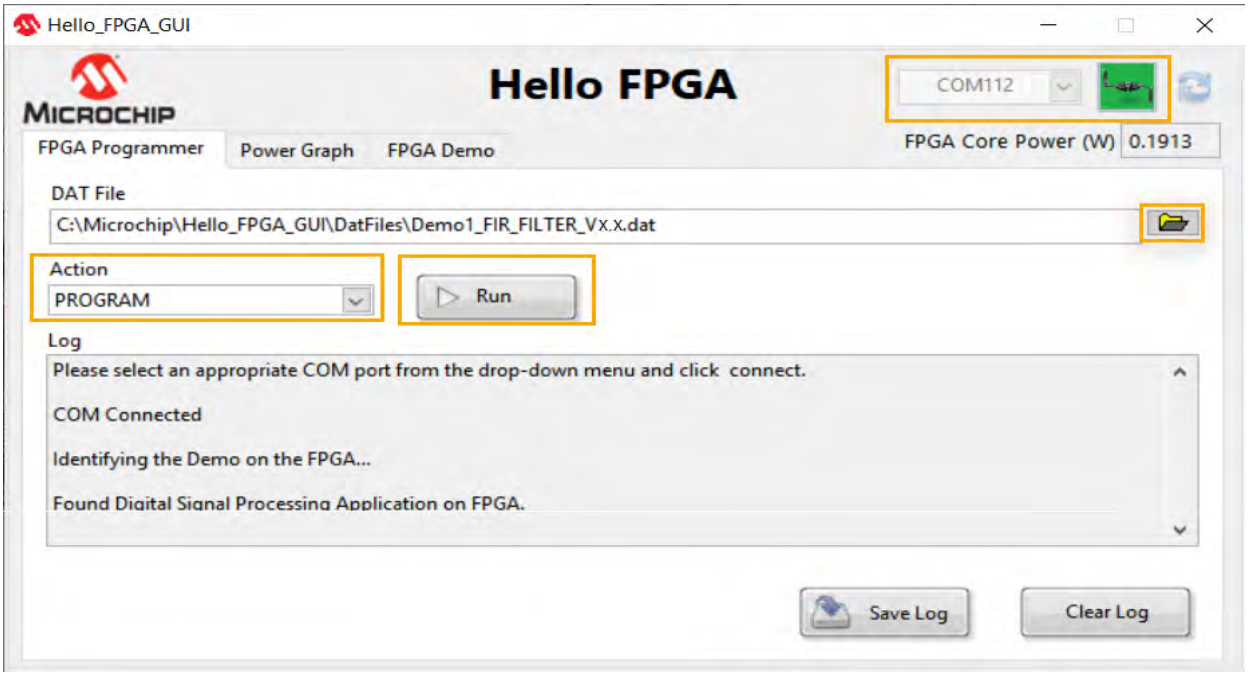
Demo Setup and Instructions

Connect the USB cable from the host PC to USB 2.0 port of the Hello FPGA board.
See Microchip Logo on the display followed by the Hello FPGA board image.

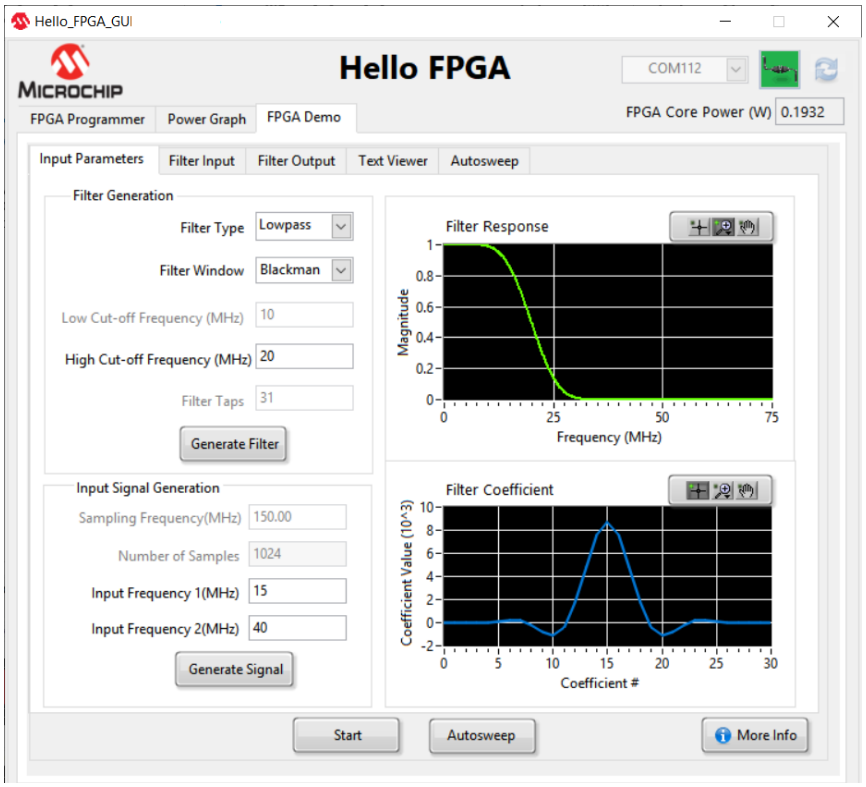


Programming the FPGA

1. Invoke the Hello_FPGA_GUI. Select the appropriate COM port from the drop down list and click Connect . The GUI displays **COM Connected** on successful connection.
2. In the **FPGA Programmer** tab, click browse and select one of the FPGA Programming files (.dat).
3. Select **PROGRAM** under **Action** from the drop-down list and click **Run**.
4. Upon successful completion of FPGA programming, user LEDs 2 and 3 starts blinking on the Hello FPGA board.
5. Unplug the USB cable from the hardware and follow the preceding instructions to reconnect the cable.
6. Click **Power Graph** tab to see the FPGA Core Power information.
7. Click **FPGA Demo** tab to run the demo for the programmed file (.dat).

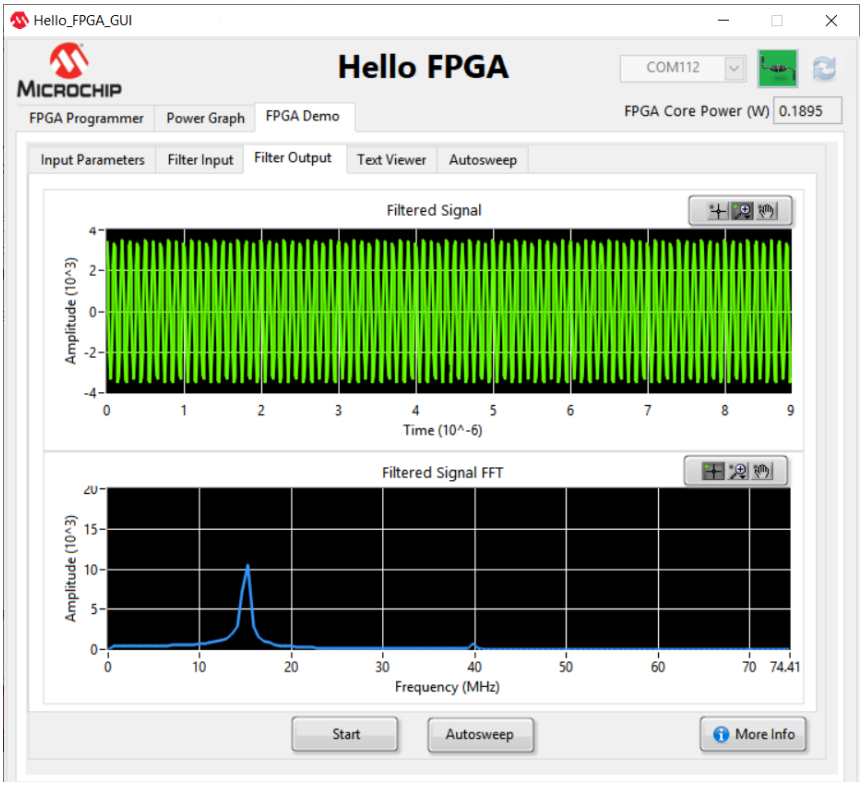


Running a Digital Signal Processing Application



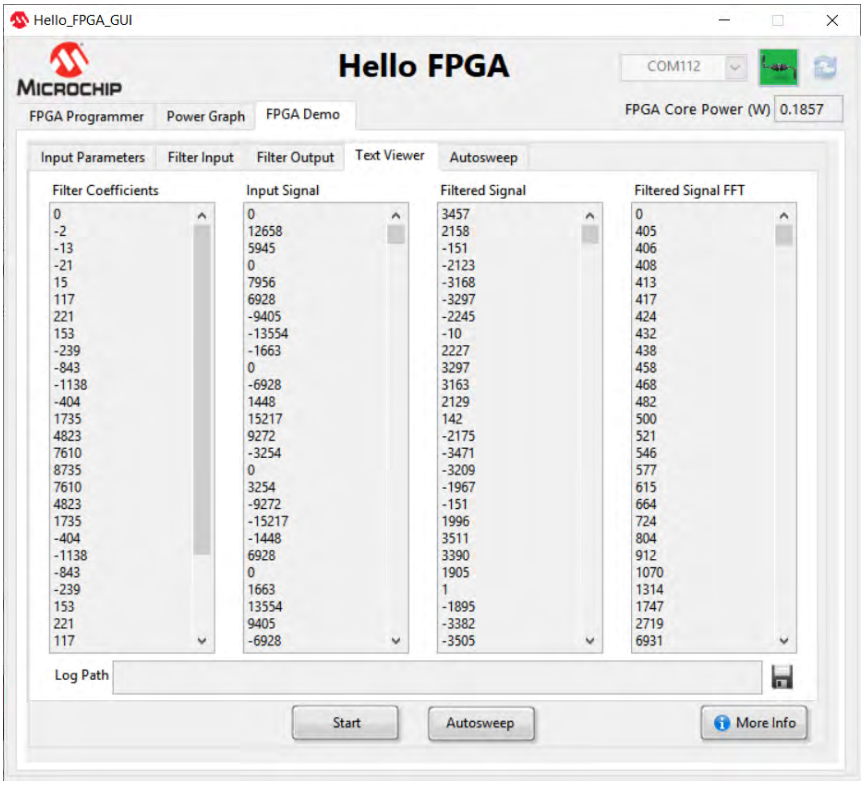
After programming with Demo1_FIR_FILTER_Vx.x.dat file, follow these steps:

1. Go to the FPGA Demo tab > Input Parameters tab.
2. In the Filter Generation pane, select Filter Type, Filter Window, enter Cut-off Frequency (MHz) and click Generate Filter to generate the filter coefficients.
3. In the Input Signal Generation pane, enter the Input frequencies. Click Generate Signal and observe the Filter Input.
4. Click Start to send the generated input signal, filter coefficients to SmartFusion2 FPGA and observe the filtered output.



5. The filtered output from SmartFusion2 FPGA as per the filter configuration can be observed on the Filter Output tab.

6. In the Text Viewer tab, you can see the numerical values of the graphs plotted in the Filter Input and Filter Output tabs.

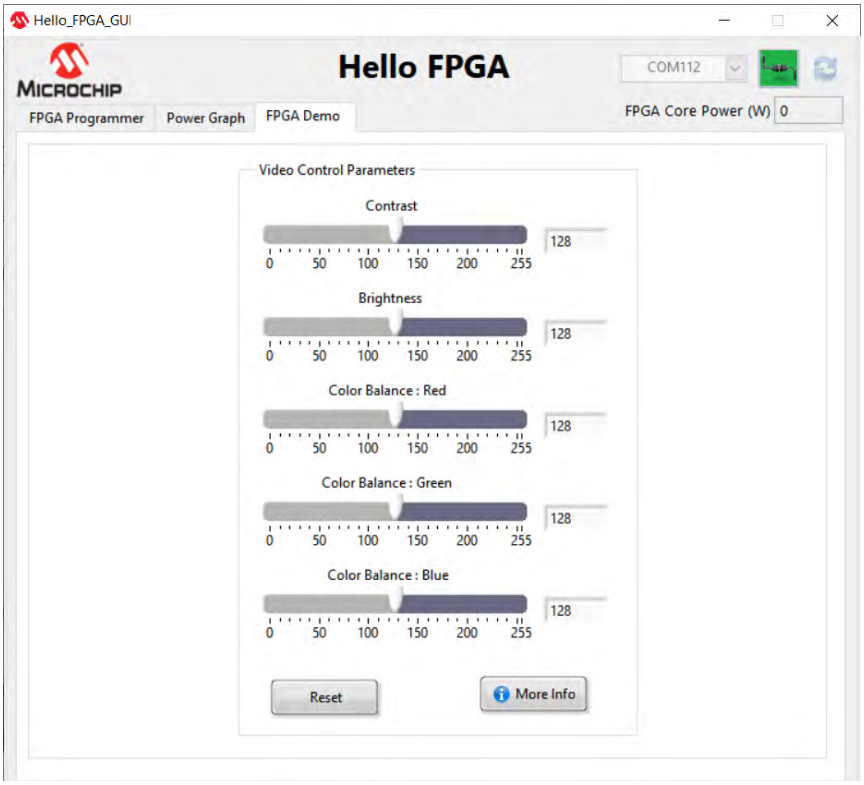


7. Click Autosweep, the GUI automatically sweeps one of the input signal frequencies (Sweep) through a range of values and sends to the FPGA to perform filter operation . Filtered output from FPGA is displayed on the right .

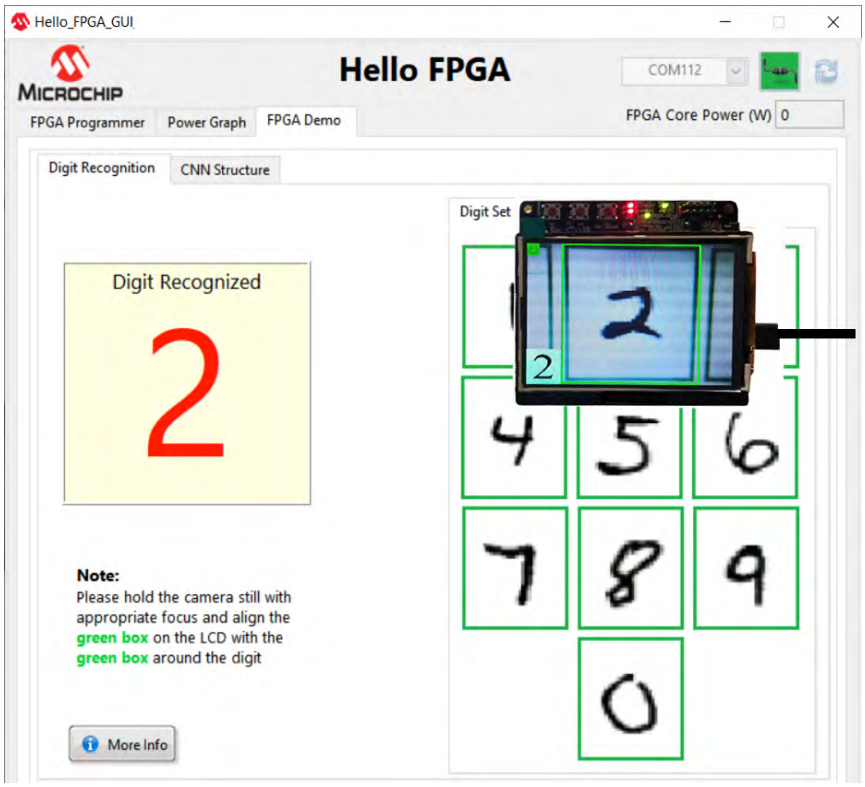
Running an Image Processing Application

After programming with Demo2_HF10_CAM_LCD_FF_Vx.x.dat file, follow these steps:

1. The video captured from camera is displayed on LCD with FPGA running Image Signal processing. If required, turn the lens to adjust the focus.
2. Go to FPGA demo tab to adjust contrast, brightness and color balance through sliders The Contrast, Brightness, and Color Balance can be adjusted through the sliders.
3. Click Reset to set the default values.



Running an AI Digit Recognition Application



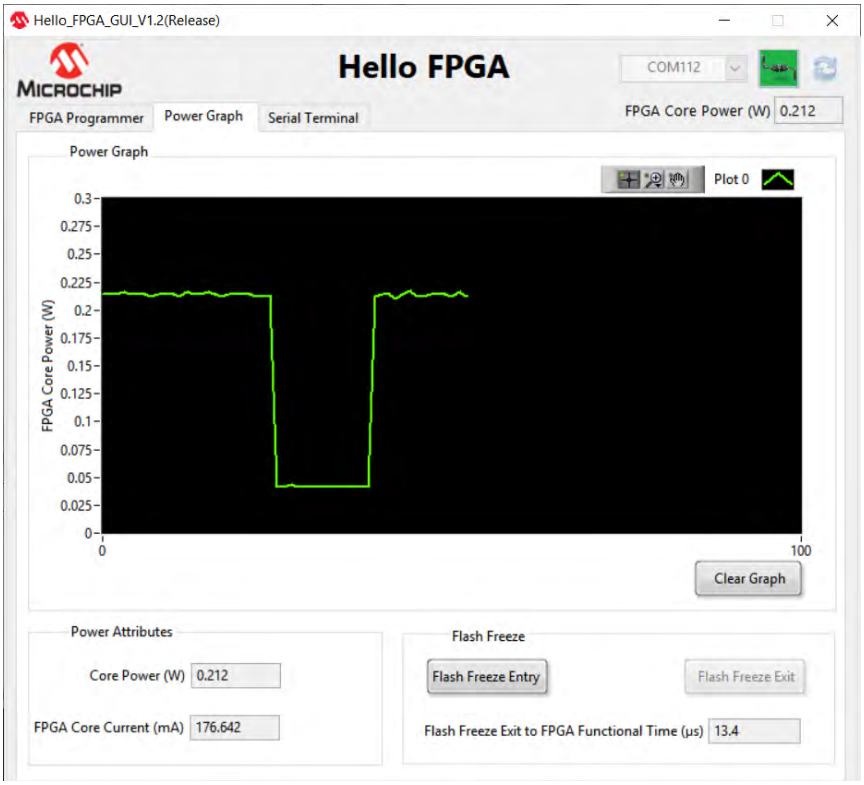
After programming with Demo3_HF10_DIGIT_CNN_FF_Vxx.dat file, follow these steps:

1. Go to the FPGA Demo tab. The FPGA captures the video from camera and runs Convolution Neural Network (CNN) to recognize the digit in the video stream.
2. Point the camera to align green box around a digit with the green box on the LCD. The recognized digit is displayed on the LCD and on the left side of the GUI window.
3. Use Digit Set 1, Digit Set 2 or Digit Set 3 to test with different fonts.

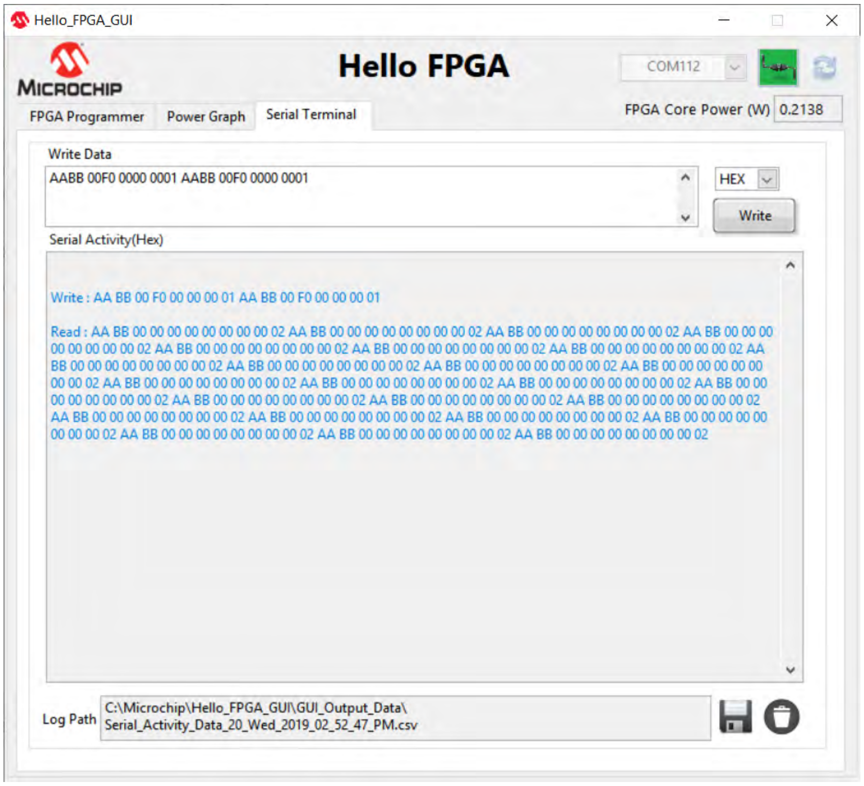
Measuring Power in Active and Low Power Mode

The Power Graph Tab can be used to observe the FPGA Core Power (W) and initiate Flash Freeze.

1. In the Flash Freeze pane, click Flash Freeze Entry to switch the FPGA from functional mode to low power mode and observe the power drop in the GUI.
2. Click Flash Freeze Exit to switch the FPGA back to functional mode. The time to exit Flash Freeze mode can be observed in the Flash Freeze pane.



Serial Terminal



Each demo that comes with the GUI is identified by the design version set in the dat file. Version numbers 4,6, and 7 are reserved. User should not use these design version numbers during dat file generation of their custom designs. GUI reads the current design version on the Kit and loads the appropriate FPGA Demo on a successful connection. For custom designs, a generic 'Serial Terminal' is loaded instead of FPGA Demo. This tab enables the user to communicate to the FPGA over Serial protocol.

Licensing

To create custom applications for the Hello FPGA kit, a free Libero SoC Design Suite silver license is required. For more information, see https://www.microsemi.com/product-directory/design-resources/1711-licensing#overview

Documentation Resources

For more information about the Hello FPGA Kit, including schematics and demo guide, see the documentation at the resources section of the Hello FPGA web page.

Support

Technical support is available Online at https://www.microsemi.com/product-directory/product-support/4217-fpgas-socs-support.

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