

Hello FPGA Quickstart Guide

Kit Contents

Quantity	Description
1	Hello FPGA Board with SmartFusion [®] 2 M2S010 VF256
1	Camera Sensor Board
1	LCD Board
1	USB 2.0 A to Mini-B cable

Hardware Connectivity





Hello FPGA Board Layout



Prerequisite

Before you start, download and install the Hello FPGA GUI Application from the <u>resources</u> section of the Hello FPGA web page.



Demo Setup and Instructions

Connect the USB cable from the host PC to USB 2.0 port of the Hello FPGA board. See Microchip Logo on the display followed by the Hello FPGA board image.



Programming the FPGA

- 1. Invoke the Hello_FPGA_GUI. Select the appropriate COM port from the drop down list and click Connect —. The GUI displays **COM Connected** on successful connection.
- 2. In the **FPGA Programmer** tab, click browse 🗁 and select one of the FPGA Programming files (.dat).
- 3. Select **PROGRAM** under **Action** from the drop-down list and click **Run**.
- 4. Upon successful completion of FPGA programming, user LEDs 2 and 3 starts blinking on the Hello FPGA board.
- 5. Unplug the USB cable from the hardware and follow the preceding instructions to reconnect the cable.
- 6. Click **Power Graph** tab to see the FPGA Core Power information.
- 7. Click **FPGA Demo** tab to run the demo for the programmed file (.dat).

		Hello FPG	СОМ112	L
FPGA Programmer	Power Graph	FPGA Demo	FPGA Core Power (V	V) 0.1913
DAT File				-
C:\Microchip\Hell	o_FPGA_GUI\Da	Files\Demo1_FIR_FILTER_VX.X.dat		
Action PROGRAM Log	2	Run		
Please select an ap COM Connected	propriate COM	port from the drop-down menu and clic	ck connect.	^
Identifying the Der	no on the FPGA			
Found Digital Sign	al Processing Ar	plication on FPGA.		
-				



Running a Digital Signal Processing Application



After programming with Demo1_FIR_FILTER_Vx.x.dat file, follow these steps:

- 1. Go to the FPGA Demo tab > Input Parameters tab.
- 2. In the Filter Generation pane, select Filter Type, Filter Window, enter Cut-off Frequency (MHz) and click Generate Filter to generate the filter coefficients.

- 3. In the Input Signal Generation pane, enter the Input frequencies. Click Generate Signal and observe the Filter Input.
- Click Start to send the generated input signal, filter coefficients to SmartFusion2 FPGA and observe the filtered output.





5. The filtered output from SmartFusion2 FPGA as per the filter configuration can be observed on the Filter Output tab.



6. In the Text Viewer tab, you can see the numerical values of the graphs plotted in the Filter Input and Filter Output tabs.

CROCHIP			ieno	FI GA		COMITE	
GA Programmer	Power Graph	FPGA Demo				FPGA Core Power (W) 0.1857
Input Parameters	Filter Input	Filter Output	Text Viewer	Autosweep			
Filter Coefficient	s	Input Signal		Filtered Signal		Filtered Signal FFT	
0 -2 -3 -2 -13 -21 15 17 221 153 -239 -843 -1138 -404 4823 7610 4823 7610 4823 1735 -404 -1138 -843 -239 -843 -239 -239 -239 -235 -239 -235 -239 -243 -211 -235 -239 -24	~	0 12658 5945 0 7956 6928 -9405 -13554 -13554 -13554 -13554 0 -6928 1448 0 3254 0 3254 0 3254 -9272 -15217 -1448 6928 0 1663 13554 9405 -6928	~	343/ 2158 -151 -2123 -3168 -3297 -2245 -10 2227 3163 2129 142 -2175 -3471 -3209 -1967 -151 1996 3511 3390 1995 1 -1895 -3382 -3505	<	0 405 406 408 413 413 417 424 432 438 458 468 468 468 468 468 468 450 521 546 5577 615 664 724 804 912 912 1070 1314 1747 2719 6931	
Log Path							



- 🕵 Hello FPGA GUI × Hello FPGA COM112 C -440-MICROCHIP FPGA Core Power (W) 0.1876 FPGA Programmer Power Graph FPGA Demo Input Parameters Filter Input Filter Output Text Viewer Autosweep + 😕 🖑 + 🔎 🖑 Filtered Signal Input Signal 10. 15 itude (10^3) 5. Amplitude (10[^] -5 -10 7.87.9 8.0 8.1 8.2 8.3 8.4 8.5 0.3 0.4 0.5 0.6 0.7 0.8 0.9 8.6 87 + • Input Signal FFT + 보 🖑 Filtered Signal FFT 30-6-و 5-25plitude(10^2) ہُe 4-20-Amplitude (15-10-5-0-10 20 30 40 50 60 10 20 30 40 50 70 70 60 80 Input Frequency 1 (MHz) 39.8 Filter Low Cut-off Frequency (MHz) 10 (Sweep) Input Frequency 2 (MHz) 19.9 Filter High Cut-off Frequency (MHz) 30 (Fixed) Start Autosweep Abort 🕤 More Info
- Click Autosweep, the GUI automatically sweeps one of the input signal frequencies (Sweep) through a range of values and sends to the FPGA to perform filter operation .
 Filtered output from FPGA is displayed on the right .

Running an Image Processing Application

After programming with Demo2_HF10_CAM_LCD_FF_Vx.x.dat file, follow these steps:

- The video captured from camera is displayed on LCD with FPGA running Image Signal processing. If required, turn the lens to adjust the focus.
- 2. Go to FPGA demo tab to adjust contrast, brightness and color balance through sliders The Contrast, Brightness, and Color Balance can be adjusted through the sliders.
- 3. Click Reset to set the default values.





Running an AI Digit Recognition Application



After programming with Demo3_ HF10_DIGIT_CNN_FF_Vxx.dat file, follow these steps:

- 1. Go to the FPGA Demo tab. The FPGA captures the video from camera and runs Convolution Neural Network (CNN) to recognize the digit in the video stream.
- Point the camera to align green box around a digit with the green box on the LCD. The recognized digit is displayed on the LCD and on the left side of the GUI window.
- 3. Use Digit Set 1, Digit Set 2 or Digit Set 3 to test with different fonts.

Measuring Power in Active and Low Power Mode

The Power Graph Tab can be used to observe the FPGA Core Power (W) and initiate Flash Freeze.

- 1. In the Flash Freeze pane, click Flash Freeze Entry to switch the FPGA from functional mode to low power mode and observe the power drop in the GUI.
- 2. Click Flash Freeze Exit to switch the FPGA back to functional mode. The time to exit Flash Freeze mode can be observed in the Flash Freeze pane.





Serial Terminal

CROCH	IP		inchio i	1 94				
GA Progra	mmer Power Gra	oh Serial Tern	ninal		FPG	A Core P	ower (W) 0.2
Write Dat	a							
AABB 00F	0 0000 0001 AABB 00	F0 0000 0001				^	HEX	~
						~	W	rite
Serial Act	ivity(Hex)							^
Write : A	A BB 00 F0 00 00 00 0	AA BB 00 F0 00	00 00 01					
Read : AA 00 00 00 00 BB 00 00 00 00 02 A 00 00 00 0 AA BB 00	A BB 00 00 00 00 00 00 00 00 22 AA BB 00 00 00 00 00 00 00 00 00 02 A AA BB 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	00 00 02 AA BB 00 00 00 00 00 00 A BB 00 00 00 00 00 00 00 02 AA B 00 00 00 00 00 00 00 02 AA BB 00 00 00	00 00 00 00 00 00 00 0 02 AA BB 00 00 00 0 00 00 00 00 02 AA B 00 00 00 00 00 00 0 00 02 AA BB 00 00 0 00 02 AA BB 00 00 00 00 00 00 00 00 02	0 00 02 AA BB 00 0 0 00 00 00 00 00 00 02 8 BB 00 00 00 00 00 00 0 00 00 02 AA BB 0 0 00 00 00 00 00 00 00 2 AA BB 00 00 00 00	00 00 00 00 00 00 AA BB 00 00 00 0 00 00 00 00 02 AA B 0 00 00 00 00 00 00 02 AA BB 00 00 0 0 00 00 00 00 02 A	00 02 AA B 0 00 00 00 B 00 00 00 0 00 02 AA 0 00 00 00 A BB 00 0	BB 00 00 00 02 4 0 00 00 0 A BB 00 0 00 00 0 0 00 00 0	0 00 A 00 00 2 00
Read : AA 00 00 00 0 BB 00 000 00 00 02 A 00 00 00 0 AA BB 00 00 00 00 0	X BE 00 00 00 00 00 00 00 00 2 AA BE 00 00 00 00 00 00 00 00 02 A AA BE 00 00 00 00 00 00 00 00 00 00 2 AA BE 00 00 00 00 00 00 00 00 12 AA BE 00 00 00 00 12 AA BE 00 00 00 00	00 00 02 AA BB 00 00 00 00 00 00 A BB 00 00 00 00 10 00 00 02 AA B 00 00 00 00 00 00 2 AA BB 00 00 0 2 AA BB 00 00 0 10 00 00 00 02 Ai	00 00 00 00 00 00 00 102 AA BB 00 00 00 100 00 00 00 00 02 AA 10 00 00 00 00 00 00 00 100 02 AA BB 00 00 100 02 AA BB 00 00 00 02 A BB 00 00 00 00 00 100 00 00 00 00 00 100 00 00 00 100 00 00 100 00 00 100 00 00 100 0	0 00 02 AA BB 00 1 00 00 00 00 00 00 BB 00 00 00 00 00 00 00 02 AA BB 0 00 00 02 AA BB 0 00 00 00 00 00 00 00 00 00 00 00 00 0	20 00 00 00 00 00 AA BB 00 00 00 00 00 00 2 AA B 0 00 00 00 00 00 00 02 AA BB 00 00 00 00 00 00 00 02 AB 00 00 00 00 02 B 00 00 00 00 00 00	00 02 AA 6 0 00 00 00 18 00 00 00 0 00 22 A0 00 0 00 02 A0 0 00 00 00 0 00 00 00 0 00 00 00 0 00 0	BB 00 00 00 02 4 0 00 00 0 A BB 00 0 00 00 0 00 00 0 00 00	000 AA 00 00 12 00

Each demo that comes with the GUI is identified by the design version set in the dat file. Version numbers 4,6, and 7 are reserved. User should not use these design version numbers during dat file generation of their custom designs. GUI reads the current design version on the Kit and loads the appropriate FPGA Demo on a successful connection. For custom designs, a generic 'Serial Terminal' is loaded instead of FPGA Demo. This tab enables the user to communicate to the FPGA over Serial protocol.

Licensing

To create custom applications for the Hello FPGA kit, a free Libero SoC Design Suite silver license is required. For more information, see <u>https://www.microsemi.com/product-directory/design-resources/1711-licensing#overview</u>

Documentation Resources

For more information about the Hello FPGA Kit, including schematics and demo guide, see the documentation at the <u>resources</u> section of the Hello FPGA web page.

Support

Technical support is available Online at https://www.microsemi.com/product-directory/product-support/4217-fpgas-socs-support.



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