

Other Information

To obtain the most recent and complete documentation for this demonstration board, including:

- User's Guide
- Board Description
- Board Schematics
- Source Code
- Application Examples
- Links to Web Seminars

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PIC24FJ256GB110 PIM Manual

Overview

The PIC24FJ256GB110 PIM is designed to demonstrate the capabilities of the PIC24FJ256GB110 family using the Explorer 16 Demonstration Board kit and the PICtail™ Plus Daughter Boards. The PIC24FJ256GB110 is specifically designed to be used in conjunction with the USB PICtail Plus Daughter Board to allow development of USB applications. Because a few pins on the device are dedicated to the USB module, several of the existing features of the Explorer 16 must be rerouted on the PIC24FJ256GB110 PIM. The Peripheral Pin Select (PPS) feature, available on this device, allows the existing peripherals to be remapped to the new I/O pins.

Features

- Enables designs for USB device, embedded host and On-The-Go (OTG) when used in conjunction with the USB PICtail Plus Daughter Board.

Hardware Options

The PIC24FJ256GB110 PIM has been configured to run with the core voltage regulator enabled and the USB voltage regulator disabled.

- **Disabling the core voltage regulator** – R4 pulls ENVREG high enabling the core voltage regulator. In order to modify the board such that the device runs with the voltage regulator disabled, populate R3 with a zero ohm resistor. Once the core voltage regulator is disabled, a voltage of 2.0V-2.7V needs to be applied to the VDDCORE pin. R2 has been added such that a zero ohm resistor that is populated here will short VDDCORE to VDD. This would require that the Explorer 16 be run from an external power supply of the correct voltage and not from the on-board voltage regulators. Alternatively, this pad can be used to attach an external power supply just to VDDCORE such that the pads will still operate at the Explorer 16 VDD, but the PIC24FJ256GB110 core will run at the lower supplied voltage.

Signal Interface

Below is a table of all the pins on the device that are remapped.

PIC24FJ256GB110		Explorer 16		
Pin #	Pin Function	Pin #	Pin Function	PIC24FJ128GA010 Pin
54	VBUS	1	DCI	RG15
1	RG15	8	LCD	RC3
95	RG14	9	LCD	RC4
34	RB10 ⁽¹⁾	25	N/A	RB0
34	RB10 ⁽¹⁾	34	PMPA13	RB10
52	RF2/RP30	51	UART1 TX	RF3
9	RC4/RPI41	52	UART1 RX	RF2
77	RD2/RP23	54	SDI to PIC18F4550	RF7
25	RB0/RP0	55	SCK to PIC18F4550	RF6
67	RA15/RPI35	56	SDA1	RG3
66	RA14/RPI36	57	SCL1	RG2
8	RC3/RPI40	66	INT3	RA14
79	RD12/RPI42	67	INT4	RA15
56	RG3/D-	89	N/A	RG1
57	RG2/D+	90	N/A	RG0
51	RF3/RP3	95	DCI	RG14

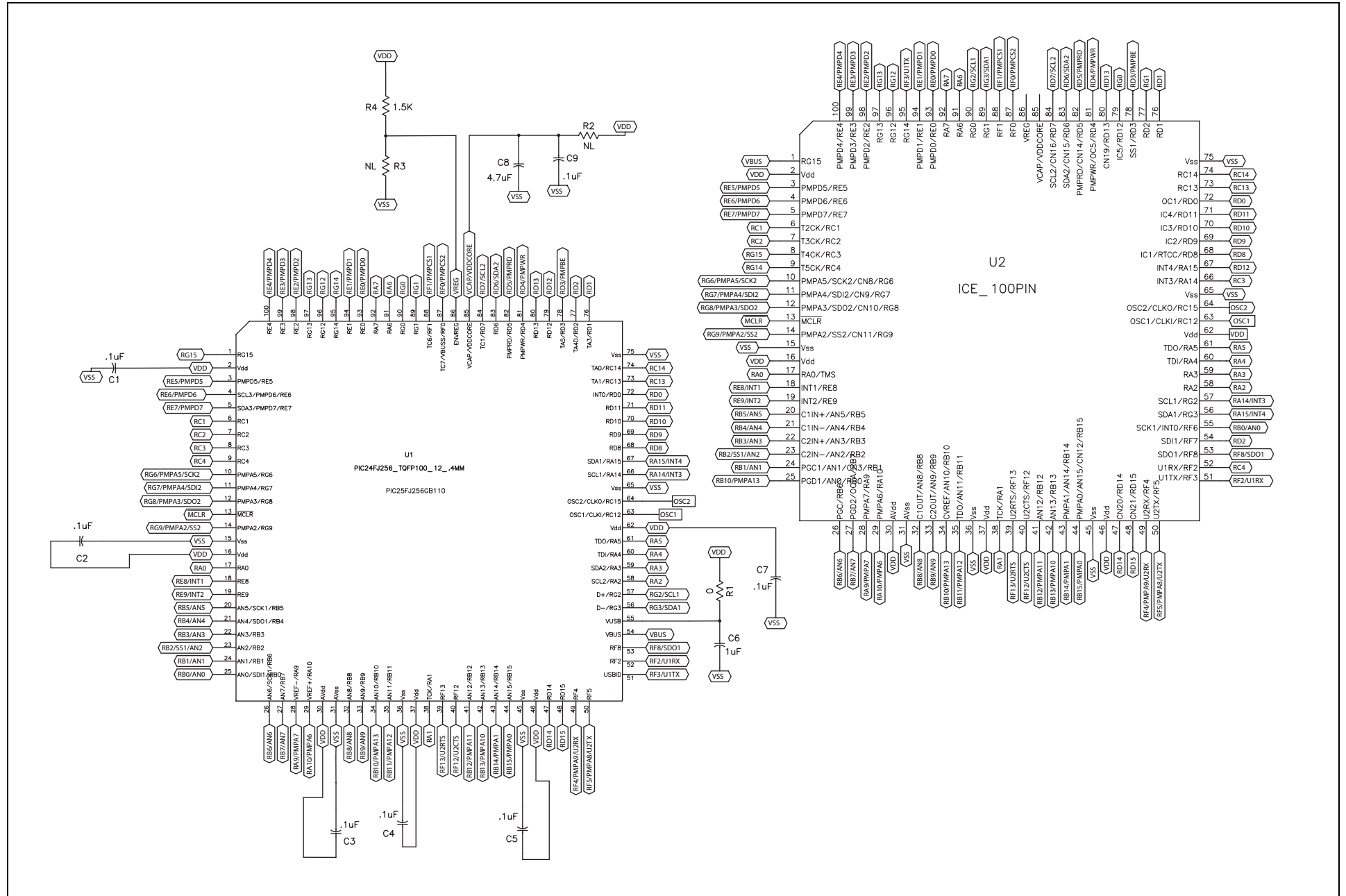
Note 1: The RB10 pin on the PIC24FJ256GB110 PIM is connected to two pins on the Explorer 16 demo board.

Tips for Using the PIC24FJ256GB110 PIM

- When migrating from a PIC24FJ128GA010 PIM to the PIC24FJ256GB110 PIM, please note that all code will need to be modified in order to map the correct peripheral to the corresponding pin. For more information about PPS, please see the "PIC24FJ256GB110 Family Data Sheet".
- Note in the above table, the RB10 of the PIC24FJ256GB110 is connected to two pins on the Explorer 16 board.

PIC24FJ256GB110 PIM Manual

Board Schematic



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