



# PIC32MZ EMBEDDED CONNECTIVITY (EC)

## PIC32MZ Embedded Connectivity (EC) 100-pin to 100-pin Plug-In Module (PIM) Information Sheet

The PIC32MZ Embedded Connectivity (EC) PIM is designed to demonstrate the capabilities of the PIC32MZ Embedded Connectivity (EC) family of devices using development boards, such as the Explorer 16 Development Board, which supports 100-pin PIM interfaces.

The PIC32MZ Embedded Connectivity (EC) is a family of high performance 32-bit microcontrollers.

Table 1 shows the mapping between the 100-pin PIM interface board functions and a 100-pin device.

Figure 1 through Figure 3 provide schematics for the example device and the PIM.

**TABLE 1: PIC32MZ EMBEDDED CONNECTIVITY (EC) FAMILY 100-PIN DEVICE TO 100-PIN PIM**

Device Pin #	PIC32MZ Embedded Connectivity (EC) Functional Description	PIM Pin #	Device Pin #	PIC32MZ Embedded Connectivity (EC) Functional Description	PIM Pin #
1	AN23/AERXERR/RG15	79	28	VREF-/CVREF-/AN27/AERXD2/RA9	32
2	EBIA5/AN34/PMA5/RA5	10	29	VREF+/CVREF+/AN28/AERXD3/RA10	33
3	EBID5/AN17/RPE5/PMD5/RE5	3	30	AVDD	30
4	EBID6/AN16/PMD6/RE6	4	31	AVSS	31
5	EBID7/AN15/PMD7/RE7	5	32	EBIA10/AN48/RPB8/PMA10/RB8	42
6	EBIA6/AN22/RPC1/PMA6/RC1	29	33	EBIA7/AN49/RPB9/PMA7/RB9	28
7	EBIA12/AN21/RPC2/PMA12/RC2	35	34	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10	34
8	EBIWE/AN20/RPC3/PMWR/RC3	81	35	AN6/ERXERR/AETXERR/RB11	76
9	EBIOE/AN19/RPC4/PMRD/RC4	82	36	Vss	15, 36, 45, 65, 75
10	AN14/C1IND/ECOL/RPG6/SCK2/RG6	47	37	VDD	2, 16, 37, 46, 62
11	EBIA4/AN13/C1INC/ECRS/RPG7/SDA4/PMA4/RG7	11	38	TCK/EBIA19/AN29/RA1	38
12	EBIA3/AN12/C2IND/ERXDV/ECRS/SDV/AECRS/SDV/RPG8/SCL4/PMA3/RG8	12	39	TDI/EBIA18/AN30/RPF13/SCK5/RF13	60
13	Vss	15, 36, 45, 65, 75	40	TDO/EBIA17/AN31/RPF12/RF12	61
14	VDD	2, 16, 37, 46, 62	41	EBIA11/AN7/ERXD0/AECRS/PMA11/RB12	41
15	MCLR	13	42	AN8/ERXD1/AECOL/RB13	77
16	EBIA2/AN11/C2INC/ERXCLK/EREFCLK/RPG9/PMA2/RG9	14	43	EBIA1/AN9/ERXD2/AETXD3/RPB14/SCK3/PMA1/RB14	43
17	TMS/EBIA16/AN24/RA0	17	44	EBIA0/AN10/ERXD3/AETXD2/RPB15/OCFB/PMA0/RB15	44
18	AN25/AERXD0/RPE8/RE8	18	45	Vss	15, 36, 45, 65, 75
19	AN26/AERXD1/RPE9/RE9	19	46	VDD	2, 16, 37, 46, 62
20	AN45/C1INA/RPB5/RB5	20	47	AN32/AETXD0/RPD14/RD14	40
21	AN4/C1INB/RB4	21	48	AN33/AETXD1/RPD15/SCK6/RD15	39
22	AN3/C2INA/RPB3/RB3	22	49	OSCI/CLKI/RC12	63
23	AN2/C2INB/RPB2/RB2	23	50	OSCO/CLKO/RC15	64
24	PGEC1/AN1/RPB1/RB1	24	51	VBUS	1
25	PGED1/AN0/RPB0/RB0	25	52	VUSB3V3	N/C
26	PGEC2/AN46/RPB6/RB6	26	53	Vss	15, 36, 45, 65, 75
27	PGED2/AN47/RPB7/RB7	27	54	D-	89

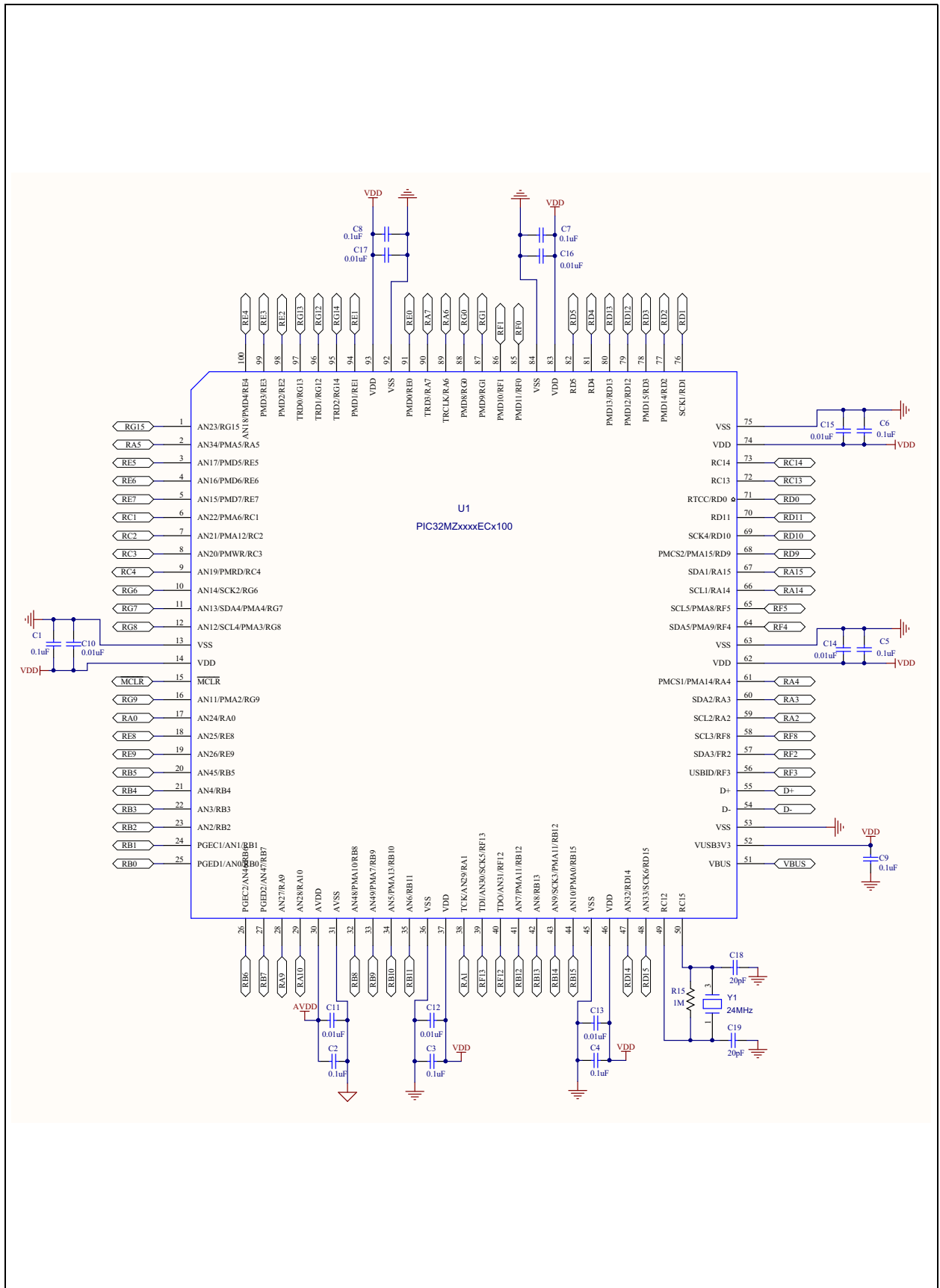
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**TABLE 1: PIC32MZ EMBEDDED CONNECTIVITY (EC) FAMILY 100-PIN DEVICE TO 100-PIN PIM**

Device Pin #	PIC32MZ Embedded Connectivity (EC) Functional Description	PIM Pin #	Device Pin #	PIC32MZ Embedded Connectivity (EC) Functional Description	PIM Pin #
55	D+	90	78	EBID15/ETXCLK/RPD3/PMD15/RD3	67
56	USBID/RPF3/RF3	95	79	EBID12/ETXD2/RPD12/PMD12/RD12	8
57	EBIRDY3/RPF2/SDA3/RF2	52	80	EBID13/ETXD3/PMD13/RD13	84
58	EBIRDY2/RPF8/SCL3/RF8	80	81	SQICS0/RPD4/RD4	69
59	EBICS0/SCL2/RA2	58	82	SQICS1/RPD5/RD5	48
60	EBIRDY1/SDA2/RA3	59	83	VDD	2, 16, 37, 46, 62
61	EBIA14/PMCS1/PMA14/RA4	71	84	VSS	15, 36, 45, 65, 75
62	VDD	2, 16, 37, 46, 62	85	EBID11/ETXD1/RPF0/PMD11/RF0	51
63	VSS	15, 36, 45, 65, 75	86	EBID10/ETXD0/RPF1/PMD10/RF1	54
64	EBIA9/RPF4/SDA5/PMA9/RF4	49	87	EBID9/ETXERR/RPG1/PMD9/RG1	89
65	EBIA8/RPF5/SCL5/PMA8/RF5	50	88	EBID8/RPG0/PMD8/RG0	90
66	AETXCLK/RPA14/SCL1/RA14	57	89	TRCLK/SQICLK/RA6	91
67	AETXEN/RPA15/SDA1/RA15	56	90	TRD3/SQID3/RA7	92
68	EBIA15/RPD9/PMCS2/PMA15/RD9	70	91	EBID0/PMD0/RE0	93
69	RPD10/SCK4/RD10	66	92	VSS	15, 36, 45, 65, 75
70	EMDC/AEMDC/RPD11/RD11	9	93	VDD	2, 16, 37, 46, 62
71	EMDIO/AEMDIO/RPD0/RTCC/INT0/RD0	68	94	EBID1/PMD1/RE1	94
72	SOSCI/RPC13/RC13	73	95	TRD2/SQID2/RG14	97
73	SOSCO/RPC14/T1CK/RC14	74	96	TRD1/SQID1/RG12	96
74	VDD	2, 16, 37, 46, 62	97	TRD0/SQID0/RG13	72
75	VSS	15, 36, 45, 65, 75	98	EBID2/PMD2/RE2	98
76	RPD1/SCK1/RD1	55	99	EBID3/RPE3/PMD3/RE3	99
77	EBID14/ETXEN/RPD2/PMD14/RD2	6	100	EBID4/AN18/PMD4/RE4	100

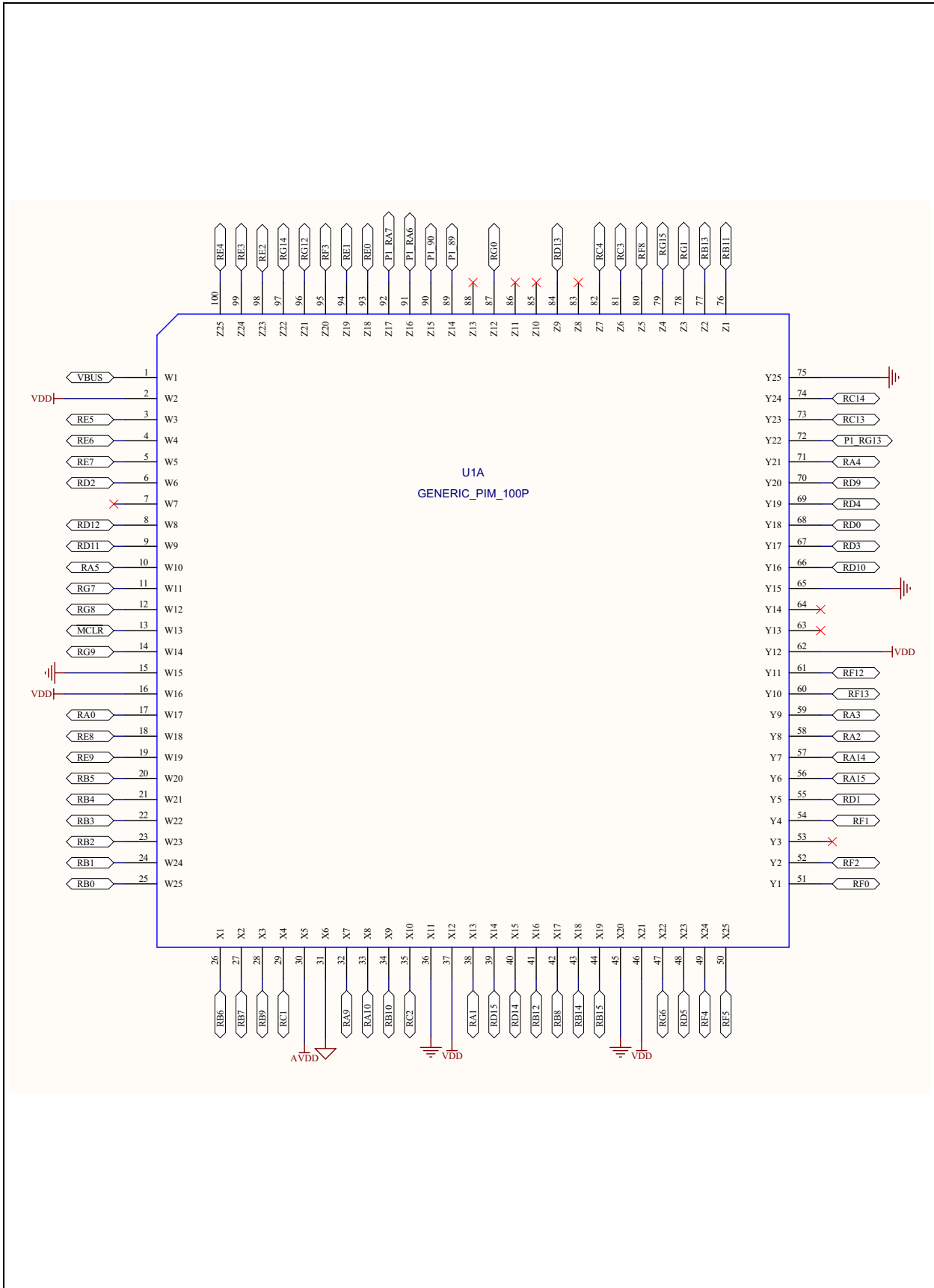
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FIGURE 1: 100-PIN DEVICE SCHEMATIC



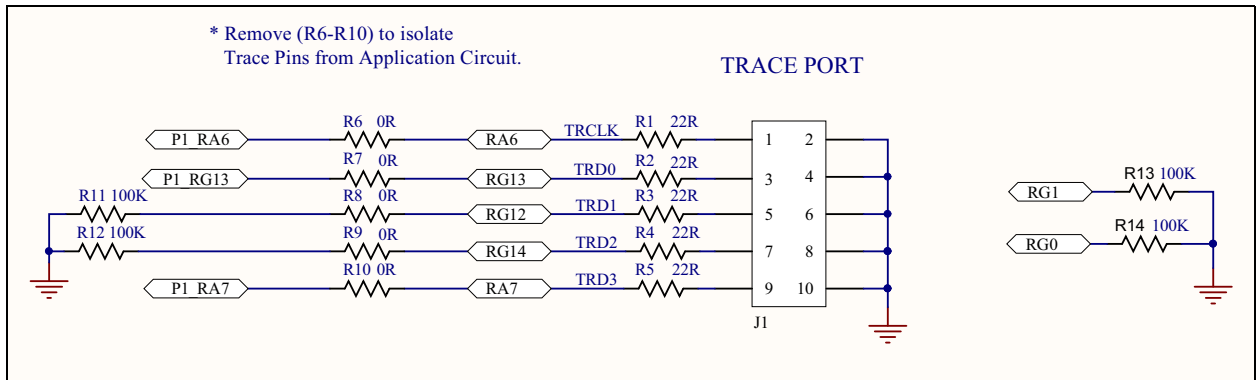
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FIGURE 2: 100-PIN PIM SOCKET SCHEMATIC



# PIC32MZ EMBEDDED CONNECTIVITY (EC)

FIGURE 3: TRACE PORT SCHEMATIC



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NOTES:

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