

0.5A MOSFET Driver With Low Threshold Input And Enable

Features

- High Peak Output Current: 0.5A (typical)
- Wide Input Supply Voltage Operating Range:
 - 4.5V to 18V
- Low Shoot-Through/Cross-Conduction Current in Output Stage
- High Capacitive Load Drive Capability:
 - 1000 pF in 40 ns (typical)
- Short Delay Times: 33 ns (t_{D1}), 24 ns (t_{D2}) (typical)
- Low Supply Current: 375 μ A (typical)
- Low Voltage Threshold Input and Enable with Hysteresis
- Latch-Up Protected: Withstands 500 mA Reverse Current
- Space-Saving Packages:
 - 6L SOT-23
 - 6L 2 x 2 DFN

Applications

- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers
- Level Translator
- Motor and Solenoid Drive

General Description

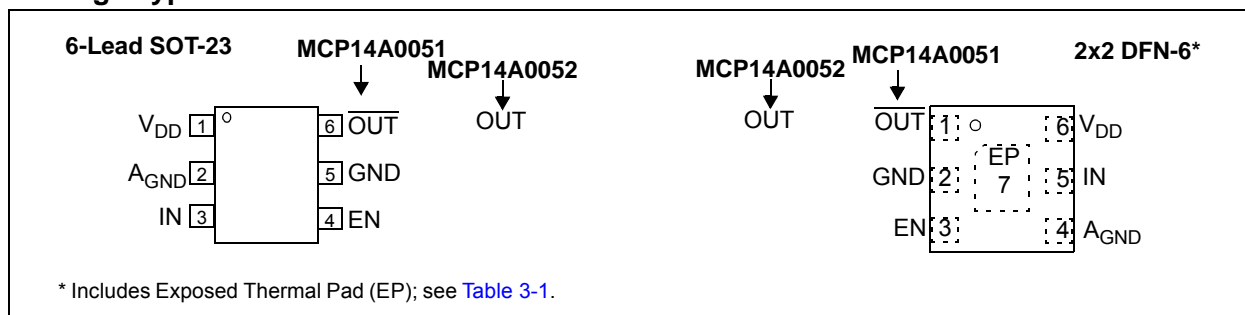
The MCP14A0051/2 devices are high-speed MOSFET drivers that are capable of providing up to 0.5A of peak current while operating from a single 4.5V to 18V supply. The inverting (MCP14A0051) or non-inverting (MCP14A0052) single-channel output is directly controlled from either TTL or CMOS (2V to 18V) logic. These devices also feature low shoot-through current, matched rise and fall times, and short propagation delays which make them ideal for high switching frequency applications.

The MCP14A0051/2 family of devices offer enhanced control with Enable functionality. The active-high Enable pin can be driven low to drive the output of the MCP14A0051/2 low regardless of the status of the Input pin. An integrated pull-up resistor allows the user to leave the Enable pin floating for standard operation.

Additionally, the MCP14A0051/2 devices feature separate ground pins (A_{GND} and GND), allowing greater noise isolation between the level-sensitive Input/Enable pins and the fast, high-current transitions of the push-pull output stage.

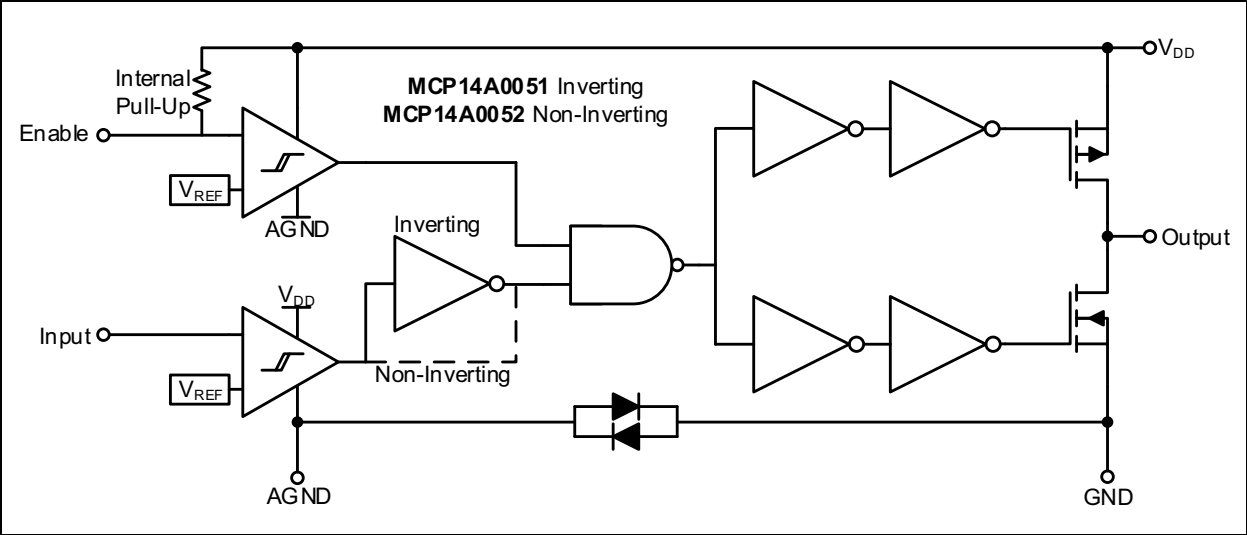
These devices are highly latch-up resistant under any condition within their power and voltage ratings. They can accept up to 500 mA of reverse current being forced back into their outputs without damage or logic upset. All terminals are fully protected against electrostatic discharge (ESD) up to 1.75 kV (HBM) and 100V (MM).

Package Types



MCP14A0051/2

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V _{DD} , Supply Voltage.....	+20V
V _{IN} , Input Voltage..... (V _{DD} + 0.3V) to (GND - 0.3V)	
V _{EN} , Enable Voltage..... (V _{DD} + 0.3V) to (GND - 0.3V)	
Package Power Dissipation (T _A = +50°C)	
6L SOT-23.....	0.52 W
6L 2 x 2 DFN.....	1.09 W
ESD Protection on all Pins.....	1.75 kV (HBM)
.....	100V (MM)

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Input Voltage Range	V _{IN}	GND - 0.3V	—	V _{DD} + 0.3	V	
Logic '1' High Input Voltage	V _{IH}	2.0	1.6	—	V	
Logic '0' Low Input Voltage	V _{IL}	—	1.2	0.8	V	
Input Voltage Hysteresis	V _{HYST(IN)}	—	0.4	—	V	
Input Current	I _{IN}	-1	—	+1	μA	0V ≤ V _{IN} ≤ V _{DD}
Enable						
Enable Voltage Range	V _{EN}	GND - 0.3V	—	V _{DD} + 0.3	V	
Logic '1' High Enable Voltage	V _{EH}	2.0	1.6	—	V	
Logic '0' Low Enable Voltage	V _{EL}	—	1.2	0.8	V	
Enable Voltage Hysteresis	V _{HYST(EN)}	—	0.4	—	V	
Enable Pin Pull-Up Resistance	R _{ENBL}	—	1.8	—	MΩ	V _{DD} = 18V, ENB = A _{GND}
Enable Input Current	I _{EN}	—	10	—	μA	V _{DD} = 18V, ENB = A _{GND}
Propagation Delay	t _{D3}	—	35	43	ns	V _{DD} = 18V, V _{EN} = 5V, see Figure 4-3, (Note 1)
Propagation Delay	t _{D4}	—	23	31	ns	V _{DD} = 18V, V _{EN} = 5V, see Figure 4-3, (Note 1)
Output						
High Output Voltage	V _{OH}	V _{DD} - 0.025	—	—	V	I _{OUT} = 0A
Low Output Voltage	V _{OL}	—	—	0.025	V	I _{OUT} = 0A
Output Resistance, High	R _{OH}	—	12.5	17	Ω	I _{OUT} = 10 mA, V _{DD} = 18V
Output Resistance, Low	R _{OL}	—	7.5	10	Ω	I _{OUT} = 10 mA, V _{DD} = 18V
Peak Output Current	I _{PK}	—	0.5	—	A	V _{DD} = 18V (Note 1)
Latch-Up Protection Withstand Reverse Current	I _{REV}	0.5	—	—	A	Duty cycle ≤ 2%, t ≤ 300 μs (Note 1)
Switching Time (Note 1)						
Rise Time	t _R	—	40	51	ns	V _{DD} = 18V, C _L = 1000 pF, see Figure 4-1, Figure 4-2 (Note 1)
Fall Time	t _F	—	28	39	ns	V _{DD} = 18V, C _L = 1000 pF, see Figure 4-1, Figure 4-2 (Note 1)

Note 1: Tested during characterization, not production tested.

MCP14A0051/2

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $T_A = +25^\circ\text{C}$, with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Delay Time	t_{D1}	—	33	41	ns	$V_{DD} = 18\text{V}$, $V_{IN} = 5\text{V}$, see Figure 4-1 , Figure 4-2 , (Note 1)
Delay Time	t_{D2}	—	24	32	ns	$V_{DD} = 18\text{V}$, $V_{IN} = 5\text{V}$, see Figure 4-1 , Figure 4-2 , (Note 1)
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_{DD}	—	330	560	μA	$V_{IN} = 3\text{V}$, $V_{EN} = 3\text{V}$
	I_{DD}	—	360	580	μA	$V_{IN} = 0\text{V}$, $V_{EN} = 3\text{V}$
	I_{DD}	—	360	580	μA	$V_{IN} = 3\text{V}$, $V_{EN} = 0\text{V}$
	I_{DD}	—	375	600	μA	$V_{IN} = 0\text{V}$, $V_{EN} = 0\text{V}$

Note 1: Tested during characterization, not production tested.

DC CHARACTERISTICS (OVER OPERATING TEMP. RANGE) ([Note 1](#))

Electrical Specifications: Unless otherwise indicated, over the operating range with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Input Voltage Range	V_{IN}	GND - 0.3V	—	$V_{DD} + 0.3$	V	
Logic '1' High Input Voltage	V_{IH}	2.0	1.6	—	V	
Logic '0' Low Input Voltage	V_{IL}	—	1.2	0.8	V	
Input Voltage Hysteresis	$V_{HYST(IN)}$	—	0.4	—	V	
Input Current	I_{IN}	-10	—	+10	μA	$0\text{V} \leq V_{IN} \leq V_{DD}$
Enable						
Enable Voltage Range	V_{EN}	GND - 0.3V	—	$V_{DD} + 0.3$	V	
Logic '1' High Enable Voltage	V_{EH}	2.0	1.6	—	V	
Logic '0' Low Enable Voltage	V_{EL}	—	1.2	0.8	V	
Enable Voltage Hysteresis	$V_{HYST(EN)}$	—	0.4	—	V	
Enable Input Current	I_{EN}	—	12	—	μA	$V_{DD} = 18\text{V}$, $ENB = A_{GND}$
Propagation Delay	t_{D3}	—	33	41	ns	$V_{DD} = 18\text{V}$, $V_{EN} = 5\text{V}$, $T_A = +125^\circ\text{C}$, see Figure 4-3
Propagation Delay	t_{D4}	—	25	33	ns	$V_{DD} = 18\text{V}$, $V_{EN} = 5\text{V}$, $T_A = +125^\circ\text{C}$, see Figure 4-3
Output						
High Output Voltage	V_{OH}	$V_{DD} - 0.025$	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	—	24	Ω	$I_{OUT} = 10\text{ mA}$, $V_{DD} = 18\text{V}$
Output Resistance, Low	R_{OL}	—	—	15	Ω	$I_{OUT} = 10\text{ mA}$, $V_{DD} = 18\text{V}$

Note 1: Tested during characterization, not production tested.

DC CHARACTERISTICS (OVER OPERATING TEMP. RANGE) (Note 1) (CONTINUED)

Electrical Specifications: Unless otherwise indicated, over the operating range with $4.5V \leq V_{DD} \leq 18V$.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Switching Time (Note 1)						
Rise Time	t_R	—	45	56	ns	$V_{DD} = 18V$, $C_L = 1000$ pF, $T_A = +125^\circ C$, see Figure 4-1, Figure 4-2
Fall Time	t_F	—	34	45	ns	$V_{DD} = 18V$, $C_L = 1000$ pF, $T_A = +125^\circ C$, see Figure 4-1, Figure 4-2
Delay Time	t_{D1}	—	32	40	ns	$V_{DD} = 18V$, $V_{IN} = 5V$, $T_A = +125^\circ C$, see Figure 4-1, Figure 4-2
Delay Time	t_{D2}	—	27	35		$V_{DD} = 18V$, $V_{IN} = 5V$, $T_A = +125^\circ C$, see Figure 4-1, Figure 4-2
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_{DD}	—	—	760	μA	$V_{IN} = 3V$, $V_{EN} = 3V$
	I_{DD}	—	—	780	μA	$V_{IN} = 0V$, $V_{EN} = 3V$
	I_{DD}	—	—	780	μA	$V_{IN} = 3V$, $V_{EN} = 0V$
	I_{DD}	—	—	800	μA	$V_{IN} = 0V$, $V_{EN} = 0V$

Note 1: Tested during characterization, not production tested.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with $4.5V \leq V_{DD} \leq 18V$						
Parameter	Sym.	Min.	Typ.	Max.	Units	Comments
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	$^\circ C$	
Maximum Junction Temperature	T_J	—	—	+150	$^\circ C$	
Storage Temperature Range	T_A	-65	—	+150	$^\circ C$	
Package Thermal Resistances						
Thermal Resistance, 6LD 2x2 DFN	θ_{JA}	—	91	—	$^\circ C/W$	
Thermal Resistance, 6LD SOT-23	θ_{JA}	—	192	—	$^\circ C/W$	

MCP14A0051/2

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

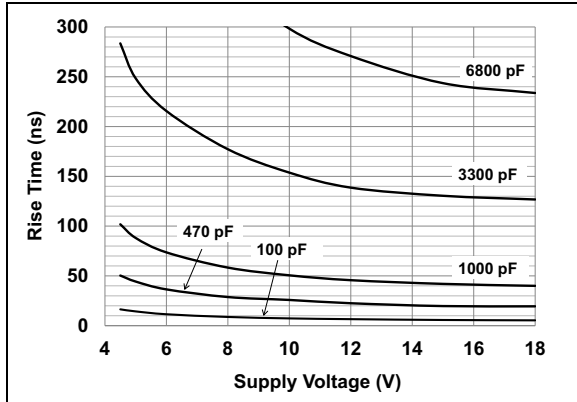


FIGURE 2-1: Rise Time vs. Supply Voltage.

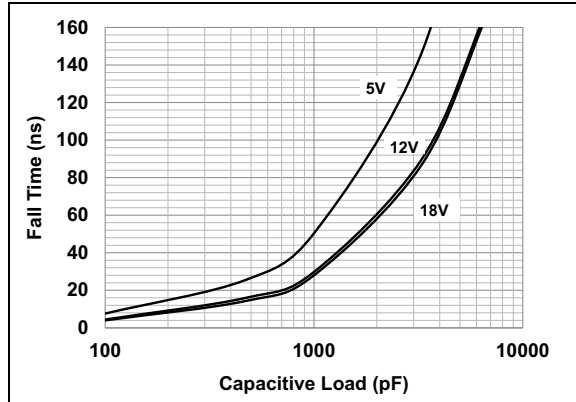


FIGURE 2-4: Fall Time vs. Capacitive Load.

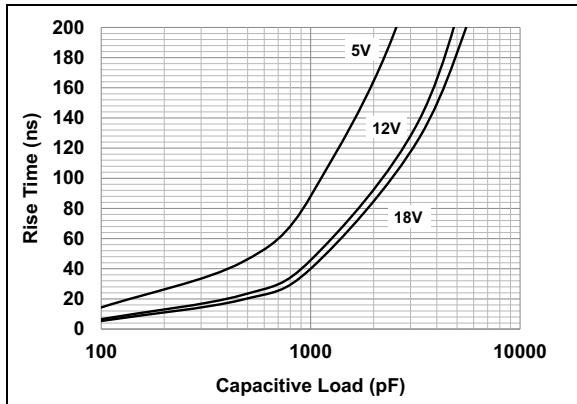


FIGURE 2-2: Rise Time vs. Capacitive Load.

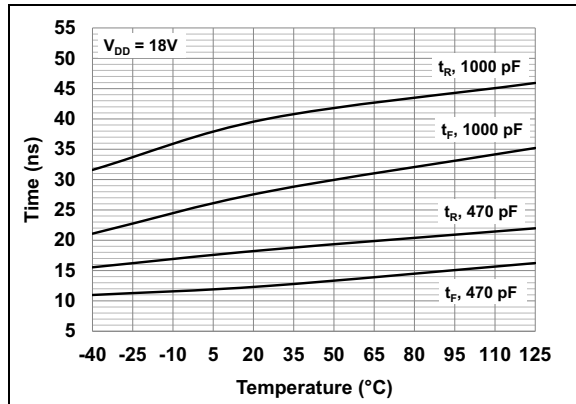


FIGURE 2-5: Rise and Fall Time vs. Temperature.

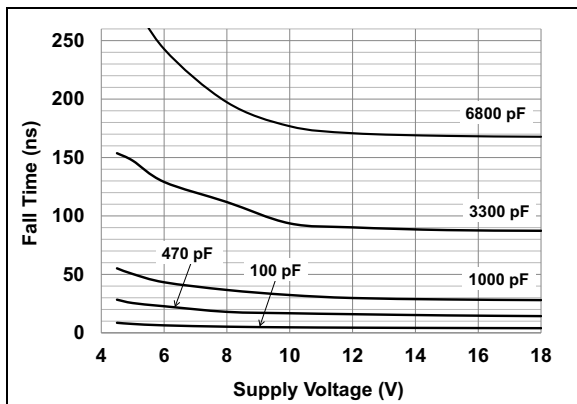


FIGURE 2-3: Fall Time vs. Supply Voltage.

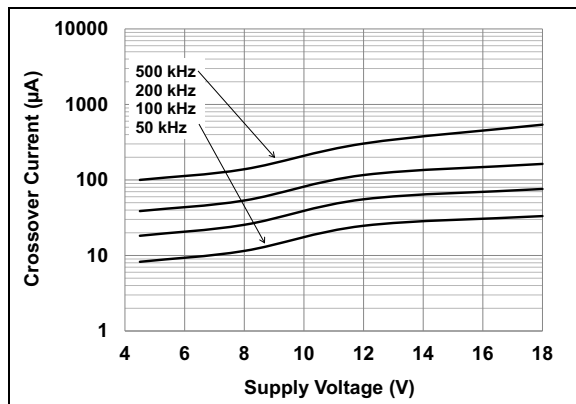


FIGURE 2-6: Crossover Current vs. Supply Voltage.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

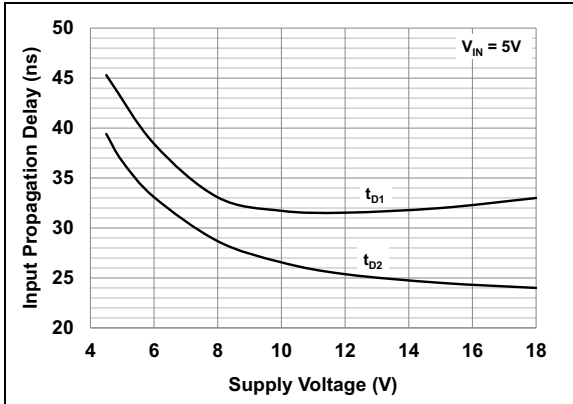


FIGURE 2-7: Input Propagation Delay vs. Supply Voltage.

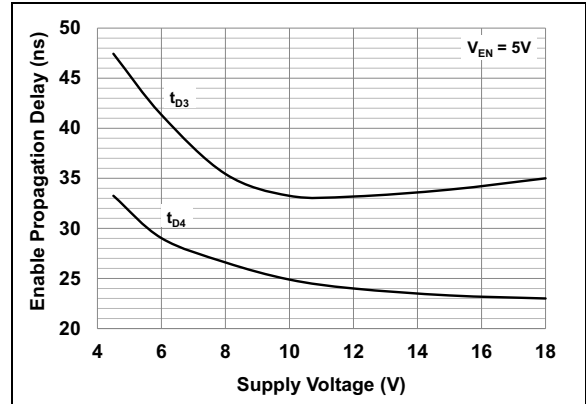


FIGURE 2-10: Enable Propagation Delay vs. Supply Voltage.

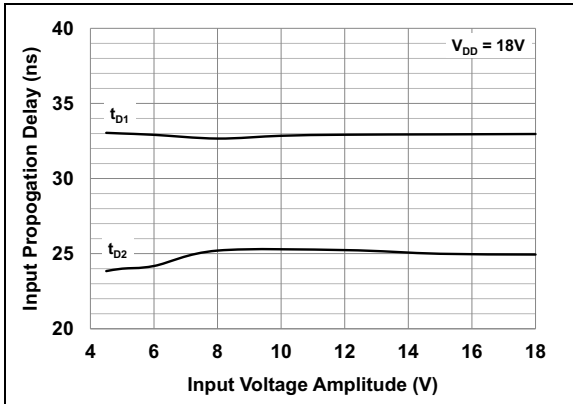


FIGURE 2-8: Input Propagation Delay Time vs. Input Amplitude.

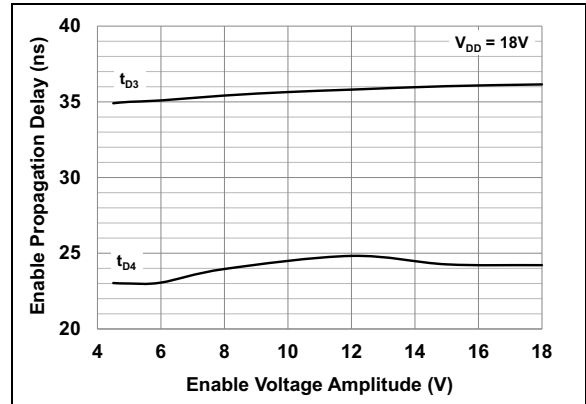


FIGURE 2-11: Enable Propagation Delay Time vs. Enable Voltage Amplitude.

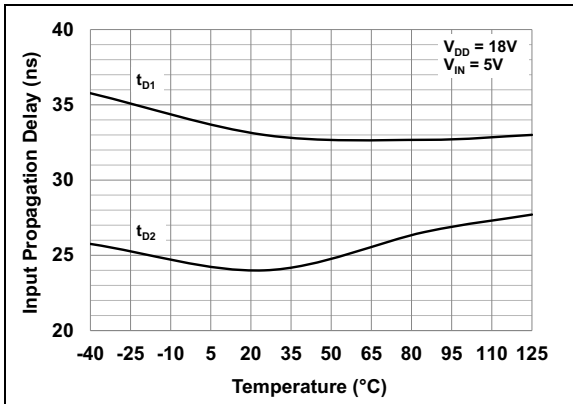


FIGURE 2-9: Input Propagation Delay vs. Temperature.

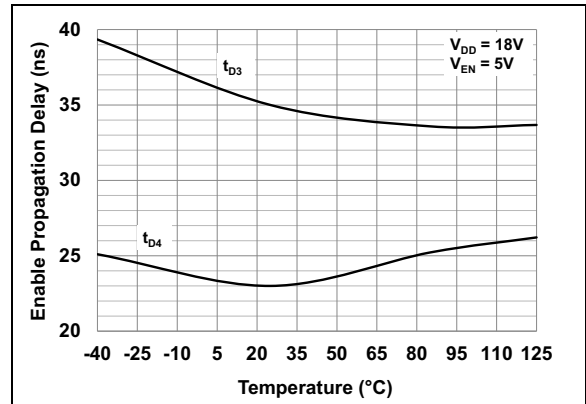


FIGURE 2-12: Enable Propagation Delay vs. Temperature.

MCP14A0051/2

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

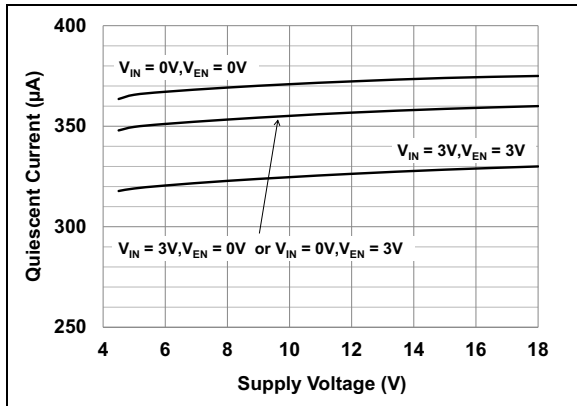


FIGURE 2-13: Quiescent Supply Current vs. Supply Voltage.

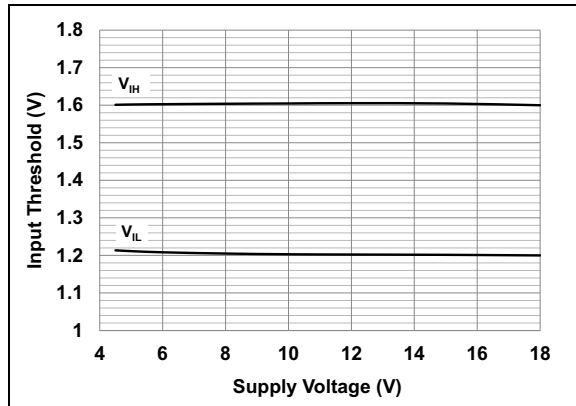


FIGURE 2-16: Input Threshold vs. Supply Voltage.

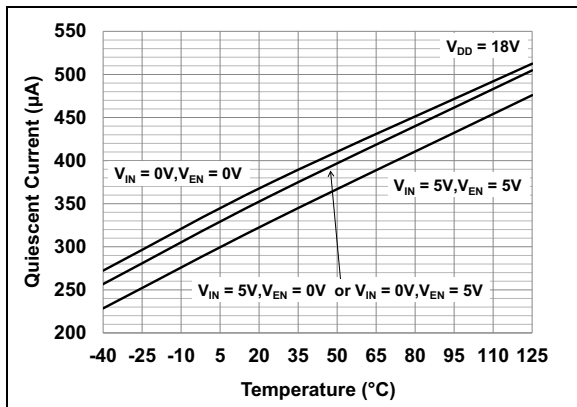


FIGURE 2-14: Quiescent Supply Current vs. Temperature.

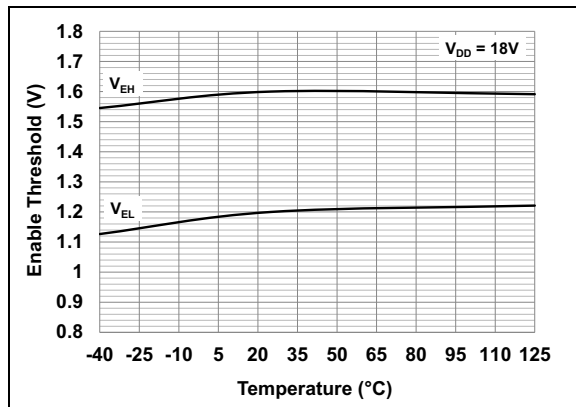


FIGURE 2-17: Enable Threshold vs. Temperature.

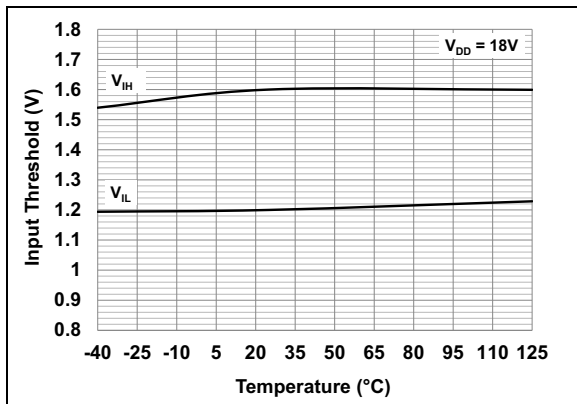


FIGURE 2-15: Input Threshold vs. Temperature.

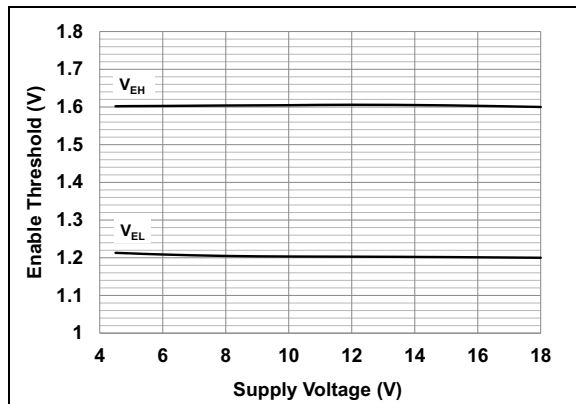


FIGURE 2-18: Enable Threshold vs. Supply Voltage.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

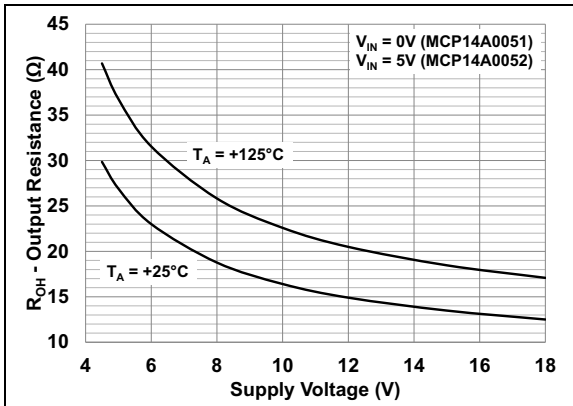


FIGURE 2-19: Output Resistance (Output High) vs. Supply Voltage.

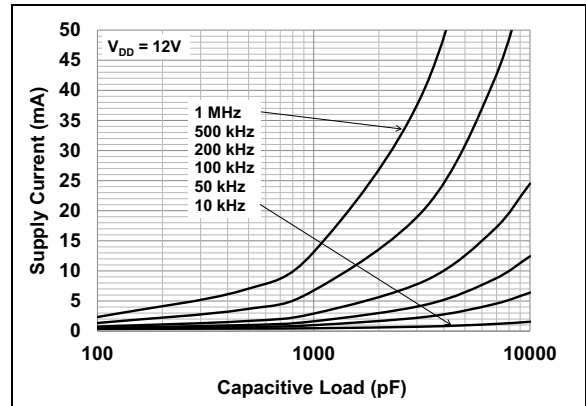


FIGURE 2-22: Supply Current vs. Capacitive Load ($V_{DD} = 12\text{V}$).

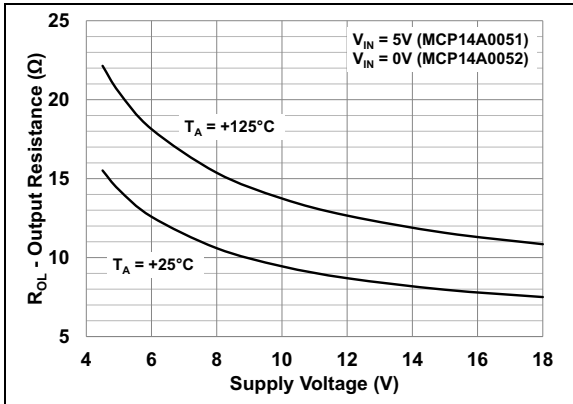


FIGURE 2-20: Output Resistance (Output Low) vs. Supply Voltage.

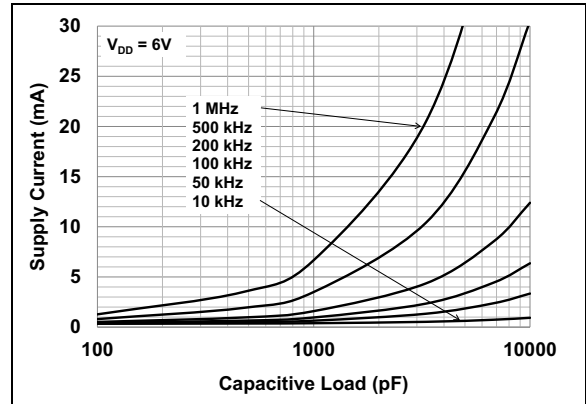


FIGURE 2-23: Supply Current vs. Capacitive Load ($V_{DD} = 6\text{V}$).

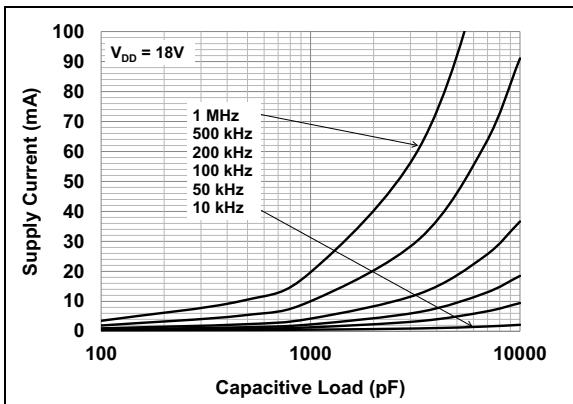


FIGURE 2-21: Supply Current vs. Capacitive Load ($V_{DD} = 18\text{V}$).

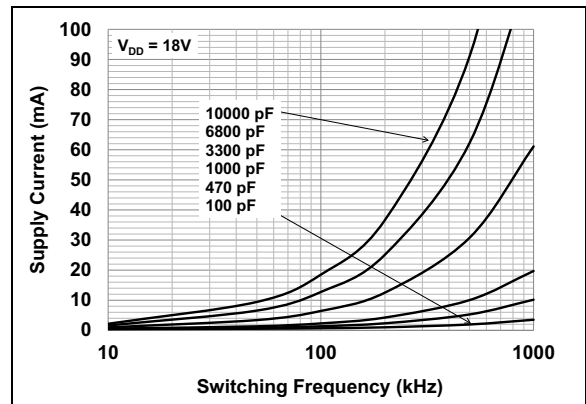


FIGURE 2-24: Supply Current vs. Frequency ($V_{DD} = 18\text{V}$).

MCP14A0051/2

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

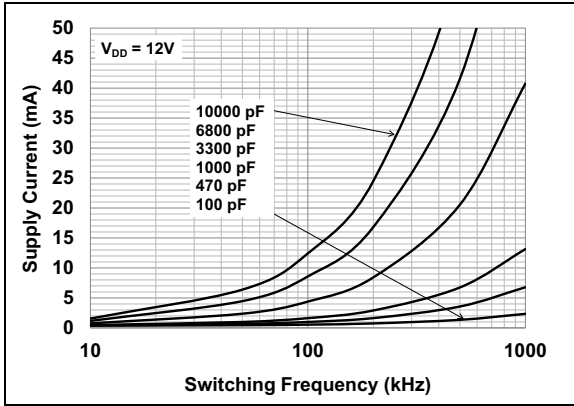


FIGURE 2-25: Supply Current vs. Frequency ($V_{DD} = 12\text{V}$).

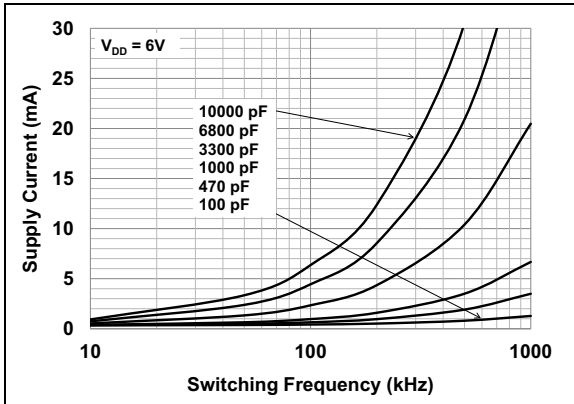


FIGURE 2-26: Supply Current vs. Frequency ($V_{DD} = 6\text{V}$).

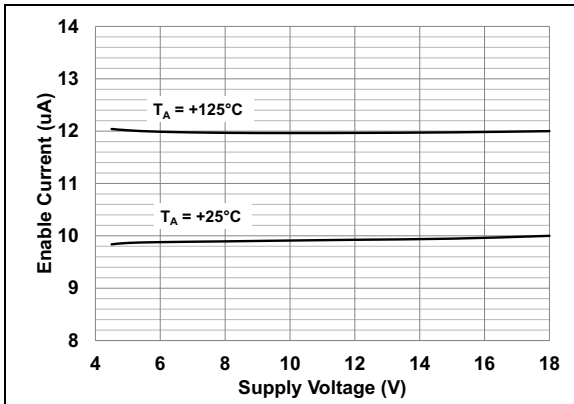


FIGURE 2-27: Enable Current vs. Supply Voltage.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin No.		Symbol	Description
6L 2x2 DFN	6L SOT-23		
1	6	OUT/OUT	Push-Pull Output
2	5	GND	Power Ground
3	4	EN	Device Enable
4	2	A _{GND}	Analog Ground
5	3	IN	Control Input
6	1	V _{DD}	Supply Input
EP	—	EP	Exposed Thermal Pad (GND)

3.1 Output Pin (OUT, $\overline{\text{OUT}}$)

The Output is a CMOS push-pull output that is capable of sourcing and sinking 0.5A of peak current ($V_{DD} = 18V$). The low output impedance ensures the gate of the external MOSFET stays in the intended state even during large transients. This output also has a reverse current latch-up rating of 500 mA.

3.2 Power Ground Pin (GND)

GND is the device return pin for the output stage. The GND pin should have a low-impedance connection to the bias supply source return. When the capacitive load is being discharged, high peak currents will flow out of the ground pin.

3.3 Device Enable Pin (EN)

The MOSFET driver Device Enable is a high-impedance, TTL/CMOS compatible input. The Enable input also has hysteresis between the high and low-input levels, allowing them to be driven from slow rising and falling signals and to provide noise immunity. Driving the Enable pin below the threshold will disable the output of the device, pulling $\overline{\text{OUT}}/\text{OUT}$ low, regardless of the status of the Input pin. Driving the Enable pin above the threshold allows normal operation of the $\overline{\text{OUT}}/\text{OUT}$ pin based on the status of the Input pin. The Enable pin utilizes an internal pull up resistor, allowing the pin to be left floating for standard driver operation.

3.4 Analog Ground Pin (A_{GND})

AGND is the device return pin for the input and enable stages of the MOSFET driver. The AGND pin should be connected to an electrically “quiet” ground node to provide a low noise reference for the input and enable pins.

3.5 Control Input Pin (IN)

The MOSFET driver Control Input is a high-impedance, TTL/CMOS compatible input. The Input also has hysteresis between the high and low-input levels, allowing them to be driven from slow rising and falling signals and to provide noise immunity.

3.6 Supply Input Pin (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are provided to the load.

3.7 Exposed Metal Pad Pin (EP)

The exposed metal pad of the DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane, or other copper plane on a printed circuit board, to aid in heat removal from the package.

MCP14A0051/2

4.0 APPLICATION INFORMATION

4.1 General Information

MOSFET drivers are high-speed, high-current devices which are intended to source/sink high peak currents to charge/discharge the gate capacitance of external MOSFETs or Insulated-Gate Bipolar Transistors (IGBTs). In high-frequency switching power supplies, the Pulse-Width Modulation (PWM) controller may not have the drive capability to directly drive the power MOSFET. A MOSFET driver such as the MCP14A0051/2 family can be used to provide additional source/sink current capability.

4.2 MOSFET Driver Timing

The ability of a MOSFET driver to transition from a fully-off state to a fully-on state is characterized by the driver's rise time (t_R), fall time (t_F) and propagation delays (t_{D1} and t_{D2}). Figure 4-1 and Figure 4-2 show the test circuit and timing waveform used to verify the MCP14A0051/2 timing.

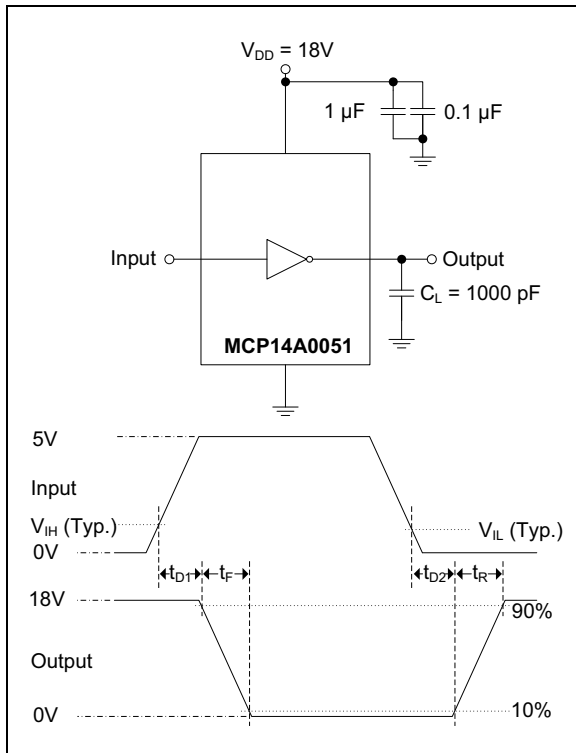


FIGURE 4-1: *Inverting Driver Timing Waveform.*

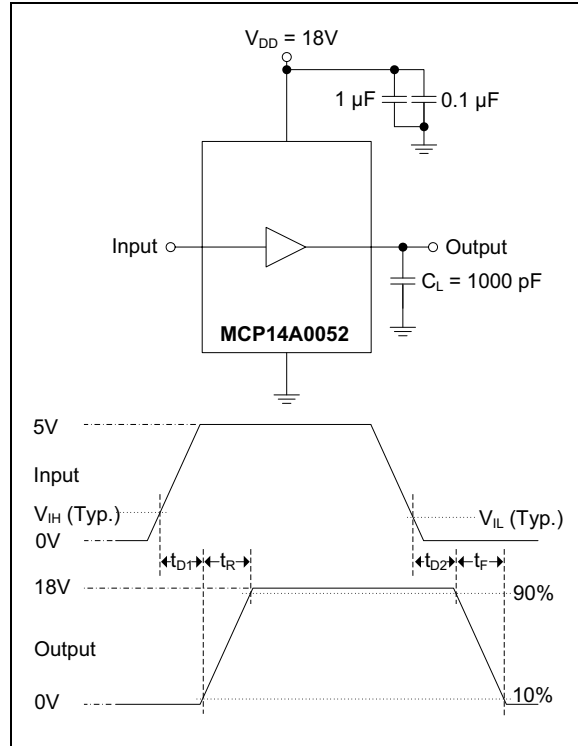


FIGURE 4-2: *Non-Inverting Driver Timing Waveform.*

4.3 Enable Function

The enable pin (EN) provides additional control of the output pin (OUT). This pin is active high and is internally pulled up to V_{DD} so that the pin can be left floating to provide standard MOSFET driver operation.

When the enable pin's voltage is above the Enable pin high-voltage threshold, (V_{EN_H}), the output is enabled and allowed to react to the status of the Input pin. However, when the voltage applied to the Enable pin falls below the low threshold voltage (V_{EN_L}), the driver output is disabled and doesn't respond to changes in the status of the Input pin. When the driver is disabled, the output is pulled down to a low state. Refer to Table 4-1 for enable pin logic. The threshold voltage levels for the Enable pin are similar to the threshold voltage levels of the Input pin, and are TTL and CMOS compatible. Hysteresis is provided to help increase the noise immunity of the enable function, avoiding false triggers of the enable signal during driver switching.

There are propagation delays associated with the driver receiving an enable signal and the output reacting. These propagation delays, t_{D3} and t_{D4} , are graphically represented in Figure 4-3.

TABLE 4-1: ENABLE PIN LOGIC

ENB	IN	MCP14A0051 OUT	MCP14A0052 OUT
H	H	L	H
H	L	H	L
L	X	L	L

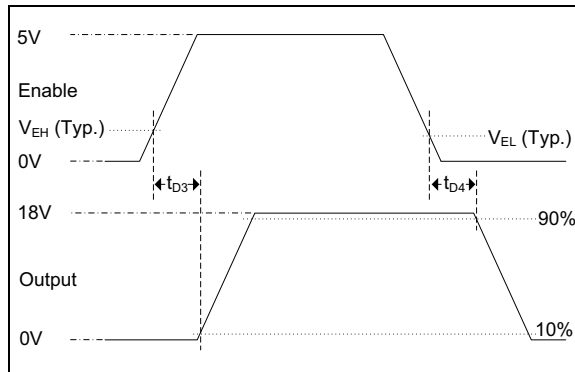


FIGURE 4-3: Enable Timing Waveform.

4.4 Decoupling Capacitors

Careful PCB layout and decoupling capacitors are required when using power MOSFET drivers. Large current is required to charge and discharge capacitive loads quickly. For example, approximately 720 mA are needed to charge a 1000 pF load with 18V in 25 ns.

To operate the MOSFET driver over a wide frequency range with low supply impedance, it is recommended to place 1.0 μ F and 0.1 μ F low ESR ceramic capacitors in parallel between the driver V_{DD} and GND. These capacitors should be placed close to the driver to minimize circuit board parasitics and provide a local source for the required current.

4.5 PCB Layout Considerations

Proper Printed Circuit Board (PCB) layout is important in high-current, fast switching circuits to provide proper device operation and robustness of design. Improper component placement may cause errant switching, excessive voltage ringing or circuit latch-up. The PCB trace loop length and inductance should be minimized by the use of ground planes or traces under the MOSFET gate drive signal, separate analog and power grounds, and local driver decoupling.

Placing a ground plane beneath the MCP14A0051/2 devices will help as a radiated noise shield, as well as providing some heat sinking for power dissipated within the device.

4.6 Power Dissipation

The total internal power dissipation in a MOSFET driver is the summation of three separate power dissipation elements, as shown in Equation 4-1.

EQUATION 4-1:

$$P_T = P_L + P_Q + P_{CC}$$

Where:

- P_T = Total power dissipation
- P_L = Load power dissipation
- P_Q = Quiescent power dissipation
- P_{CC} = Operating power dissipation

4.6.1 CAPACITIVE LOAD DISSIPATION

The power dissipation caused by a capacitive load is a direct function of the frequency, total capacitive load and supply voltage. The power lost in the MOSFET driver for a complete charging and discharging cycle of a MOSFET is shown in Equation 4-2.

EQUATION 4-2:

$$P_L = f \times C_T \times V_{DD}^2$$

Where:

- f = Switching frequency
- C_T = Total load capacitance
- V_{DD} = MOSFET driver supply voltage

4.6.2 QUIESCENT POWER DISSIPATION

The power dissipation associated with the quiescent current draw depends on the state of the Input and Enable pins. Refer to Section 1.0 “Electrical Characteristics” for typical quiescent current draw values in different operating states. The quiescent power dissipation is shown in Equation 4-3.

EQUATION 4-3:

$$P_Q = (I_{QH} \times D + I_{QL} \times (1 - D)) \times V_{DD}$$

Where:

- I_{QH} = Quiescent current in the High state
- D = Duty cycle
- I_{QL} = Quiescent current in the Low state
- V_{DD} = MOSFET driver supply voltage

MCP14A0051/2

4.6.3 OPERATING POWER DISSIPATION

The operating power dissipation occurs each time the MOSFET driver output transitions because, for a very short period of time, both MOSFETs in the output stage are on simultaneously. This cross-conduction current leads to a power dissipation described in [Equation 4-4](#).

EQUATION 4-4:

$$P_{CC} = CC \times f \times V_{DD}$$

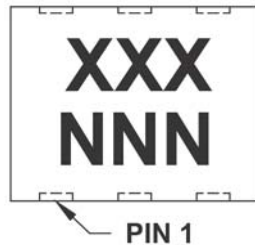
Where:

- CC = Cross-Conduction constant
(Ampere x second)
- f = Switching frequency
- V_{DD} = MOSFET driver supply voltage

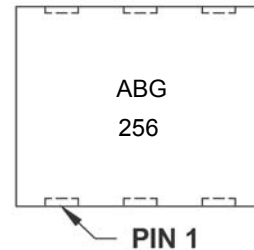
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

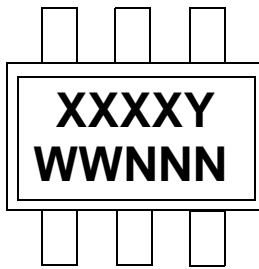
6-Lead DFN (2x2x0.9 mm)



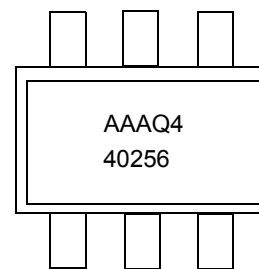
Example



6-Lead SOT-23



Example



Standard Markings for SOT-23

Part Number	Code
MCP14A0051T-E/MAY	ABG
MCP14A0052T-E/MAY	ABH
MCP14A0051T-E/CH	AAAQY
MCP14A0052T-E/CH	AAARY

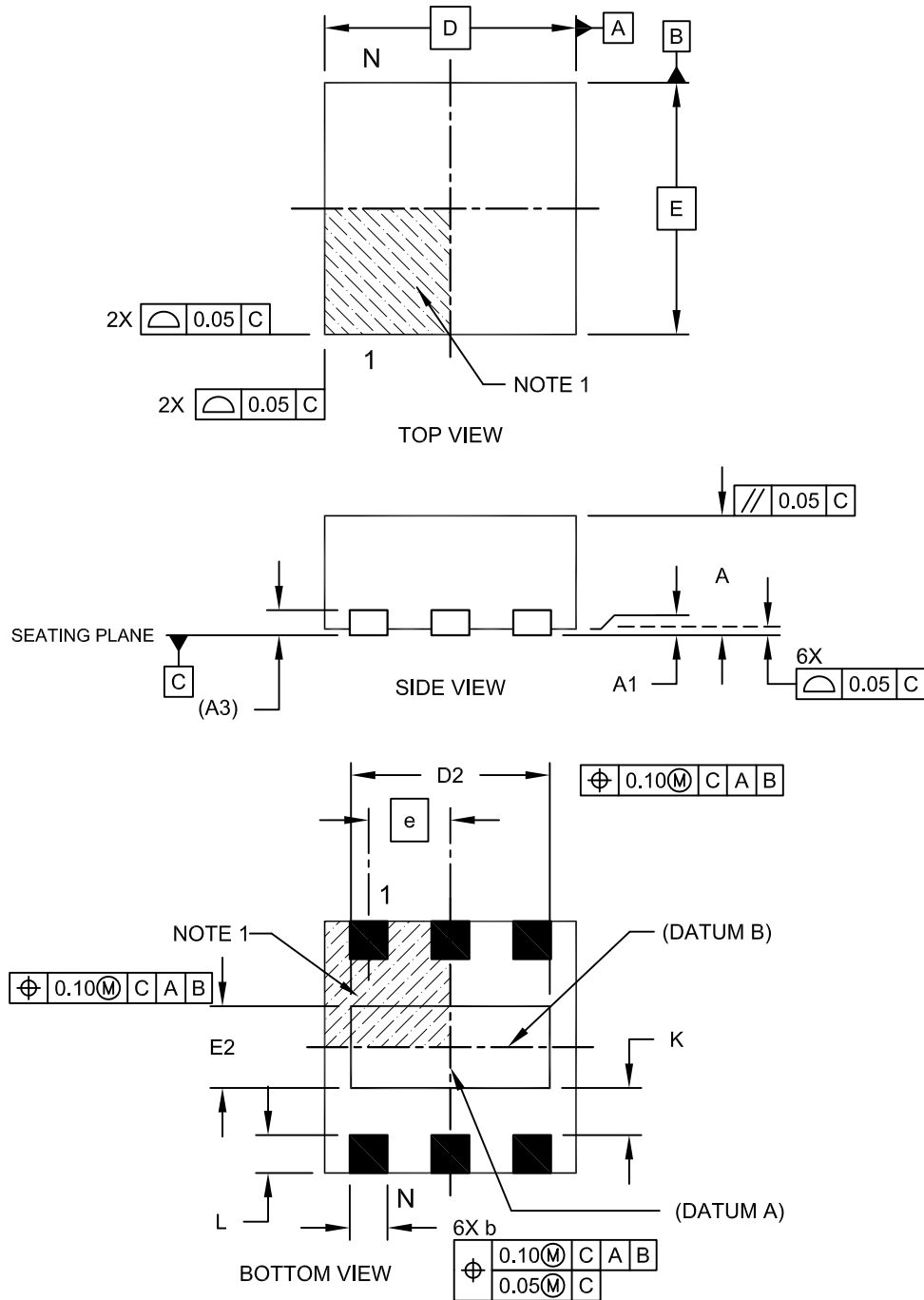
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

MCP14A0051/2

6-Lead Plastic Dual Flat, No Lead Package (MA[Y]) - 2x2x0.9mm Body [DFN]

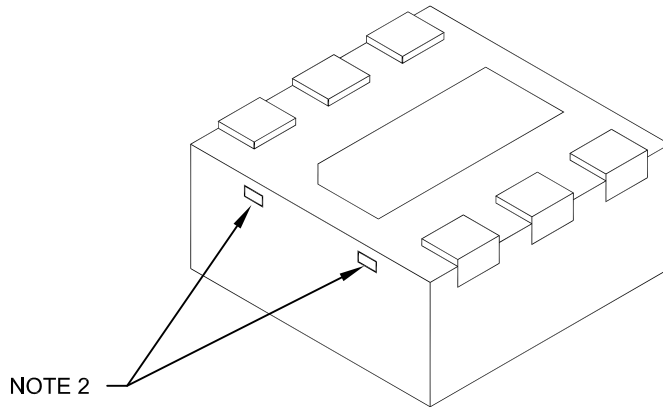
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-120C Sheet 1 of 2

6-Lead Plastic Dual Flat, No Lead Package (MA[Y]) - 2x2x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	6		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	2.00 BSC		
Exposed Pad Length	D2	1.50	1.60	1.70
Exposed Pad Width	E2	0.90	1.00	1.10
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

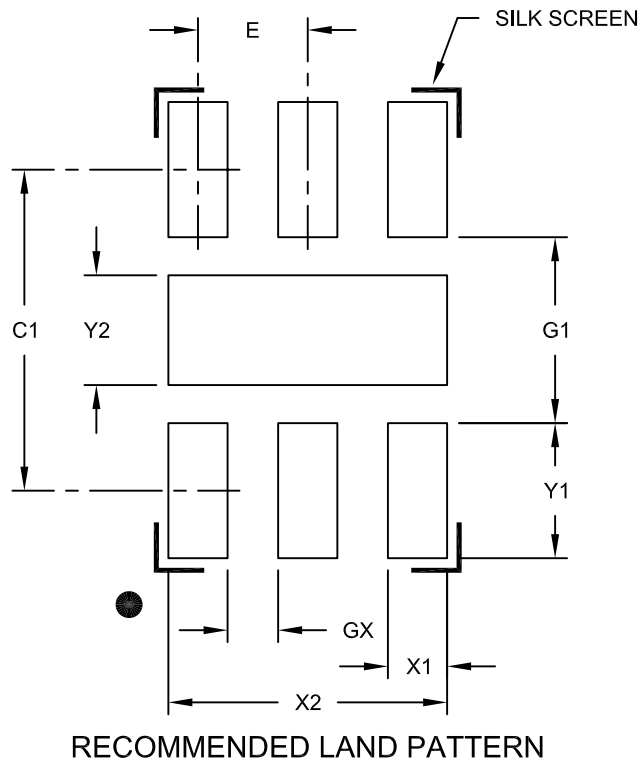
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-120C Sheet 2 of 2

MCP14A0051/2

6-Lead Plastic Dual Flat, No Lead Package (MA) - 2x2x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	Y2			1.00
Optional Center Pad Length	X2			1.70
Contact Pad Spacing	C1		2.10	
Contact Pad Width (X6)	X1			0.35
Contact Pad Length (X6)	Y1			0.65
Distance Between Pads	GX	0.20		
Distance Between Pads	G1	1.10		

Notes:

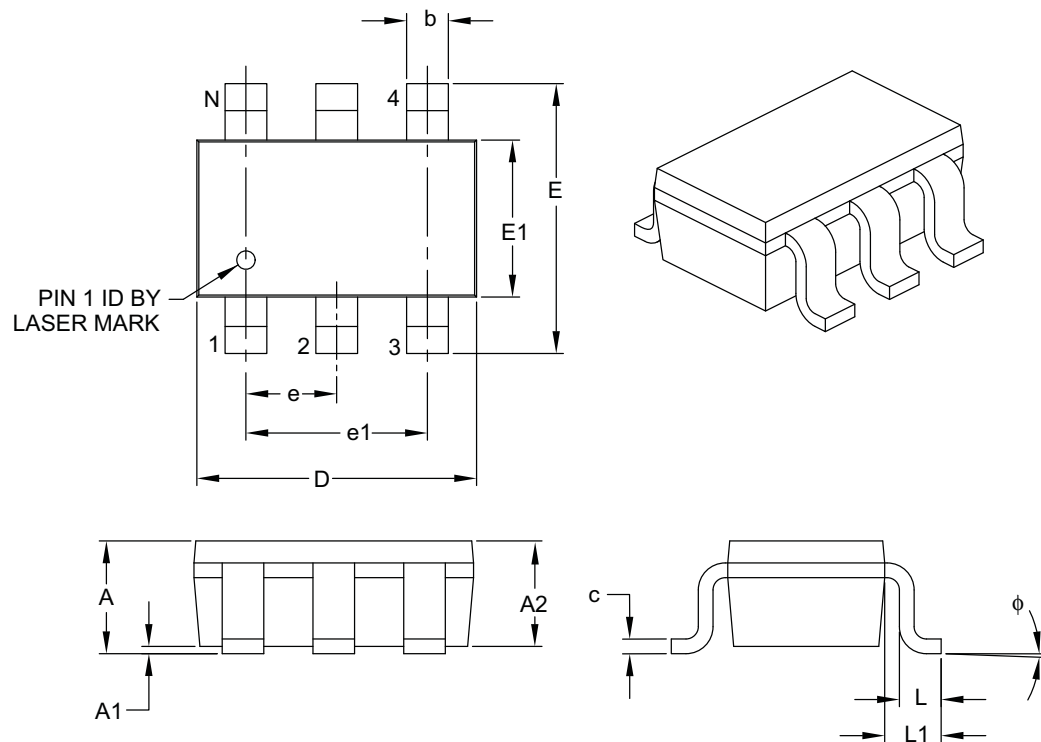
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2120A

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	6		
Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

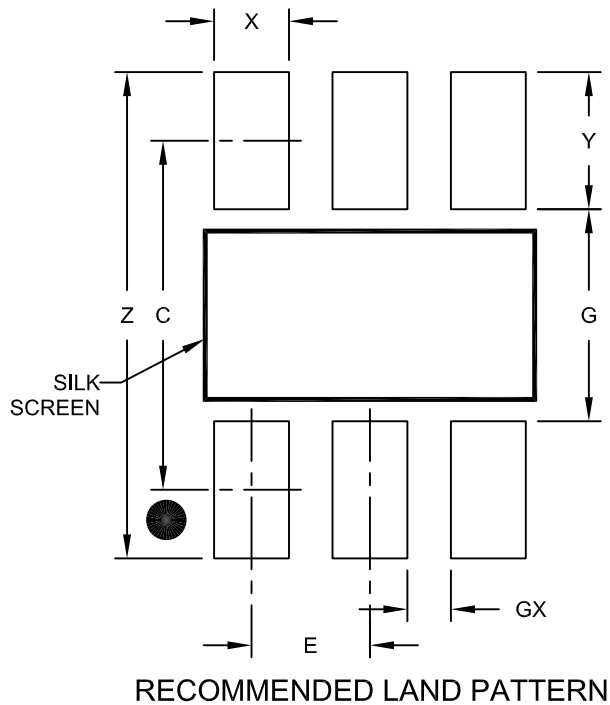
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

MCP14A0051/2

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

APPENDIX A: REVISION HISTORY

Revision A (December 2014)

- Original Release of this Document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>/X</u> ⁽¹⁾	<u>-X</u>	<u>/XX</u>
Device	Tape and Reel	Temperature Range	Package
<p>Device:</p> <p>MCP14A0051T: High-Speed MOSFET Driver (Tape and Reel)</p> <p>MCP14A0052T: High-Speed MOSFET Driver (Tape and Reel)</p>			
<p>Temperature Range: E = -40°C to +125°C (Extended)</p>			
<p>Package:</p> <p>CH = Plastic Small Outline Transistor (SOT-23), 6-lead</p> <p>MAY = Plastic Dual Flat, No Lead Package - 2 x 2 x 0.9 mm Body (DFN) 6-lead</p>			
			<p>Examples:</p> <p>a) MCP14A0051T-E/CH: Tape and Reel, Extended temperature, 6LD SOT-23 package</p> <p>a) MCP14A0052T-E/MAY: Tape and Reel, Extended temperature, 6LD DFN package</p>
			<p>Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.</p>

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, flexPWR, JukeBlox, KEELOQ, KEELOQ logo, Klear, LANCheck, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC³² logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

The Embedded Control Solutions Company and mTouch are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, ECAN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, KlearNet, KlearNet logo, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, RightTouch logo, REAL ICE, SQI, Serial Quad I/O, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2014, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-63276-908-4

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC[®] MCUs and dsPIC[®] DSCs, KEELOQ[®] code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880-3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Pforzheim
Tel: 49-7231-424750

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

03/25/14

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [Gate Drivers](#) category:

Click to view products by [Microchip](#) manufacturer:

Other Similar products are found below :

[89076GBEST](#) [00053P0231](#) [56956](#) [57.404.7355.5](#) [LT4936](#) [57.904.0755.0](#) [5882900001](#) [00600P0005](#) [00-9050-LRPP](#) [00-9090-RDPP](#)
[5951900000](#) [01-1003W-10/32-15](#) [0131700000](#) [00-2240](#) [LTP70N06](#) [LVP640](#) [5J0-1000LG-SIL](#) [LY1D-2-5S-AC120](#) [LY2-US-AC240](#) [LY3-](#)
[UA-DC24](#) [00576P0020](#) [00600P0010](#) [LZN4-UA-DC12](#) [LZNQ2M-US-DC5](#) [LZNQ2-US-DC12](#) [LZP40N10](#) [00-8196-RDPP](#) [00-8274-RDPP](#)
[00-8275-RDNP](#) [00-8722-RDPP](#) [00-8728-WHPP](#) [00-8869-RDPP](#) [00-9051-RDPP](#) [00-9091-LRPP](#) [00-9291-RDPP](#) [0207100000](#) [0207400000](#)
[01312](#) [0134220000](#) [60713816](#) [M15730061](#) [61161-90](#) [61278-0020](#) [6131-204-23149P](#) [6131-205-17149P](#) [6131-209-15149P](#) [6131-218-17149P](#)
[6131-220-21149P](#) [6131-260-2358P](#) [6131-265-11149P](#)