MCP1722

High Voltage LDO with Dual Output and Extended Temperature Range

Key Features

- AEC-Q100, Grade 0 Qualified, PPAP Capable
- Input Voltage Range: 4.5V to 55V
  - Undervoltage Lock Out (UVLO) 2.7V Typical
- 65V Load Dump Protected (ISO 7637-2/2004)
- Extended Junction Temperature Range: -40°C to +150°C
- Standard Output Regulated Voltages (V_R):
  - V_{OUT1}: 10V or 12V
  - V_{OUT2}: 3.3V or 5.0V
  - Tolerance +/- 2% for each LDO Output
- Output Current Capability Typical:
  - V_{OUT1}: 50 mA
  - V_{OUT2}: 100 mA
- Open-Drain Power Good Pins for Both LDO Outputs
- Low Quiescent Supply Current: 50 µA
- Low Shutdown Quiescent Supply Current: 4 µA
- Stable with Ceramic Output Capacitor: 3.3 µF
- Short Circuit Current Foldback Protection
- Thermal Shutdown Protection: 178°C Typical
- High PSRR:
  - -80 dB @ 100Hz typical
- Available in the Following Packages:
  - VDFN 8-Lead 3x3 mm Body with 2.40x1.60 mm Exposed Pad
  - SOIC 8-Lead 3.90 mm Body with 2.2x3.0 mm Exposed Pad

Applications

- Battery Powered Tools
- Handheld Vacuum
- Startup Bias for PWM Controllers

Description

MCP1722 is a dual output, high voltage, low dropout (LDO) regulator, designed to supply a µProcessor with either 3.3V or 5.0V. It has a current capability of 100 mA, while also providing 10V or 12V to a motor driver with a current capability of 50 mA. These specifications make it ideal for handheld power tools with 20V battery packs.

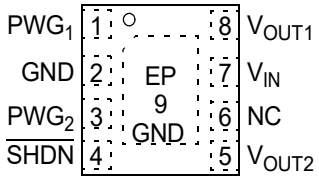
MCP1722 comes with Power Good indicators (two pins, PWG_1 and PWG_2) for both outputs and shutdown functionality (a single $\overline{SHDN}$ pin) that places the part in a low current consumption state, of only 4 µA.

The device comes in two 8-lead VDFN or SOIC packages, both with exposed pads, for improved thermal dissipation. While in operation, MCP1722 is fully protected by thermal shutdown protection and current foldback limiting.

Package Types

MCP1722

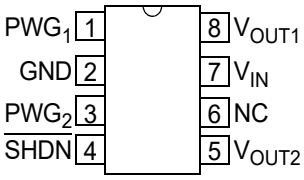
8-Lead 3x3 mm
VDFN*



* Includes Exposed Thermal Pad (EP); see Table 3-1.

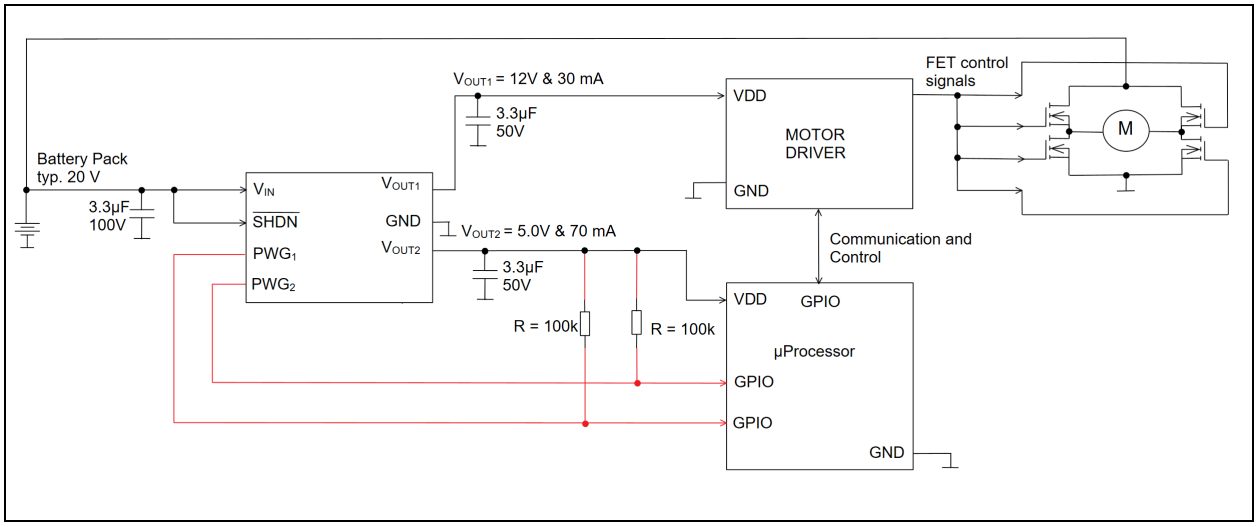
MCP1722

8-Lead 3.90 mm
SOIC*



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage ..... +70.0V
Maximum Voltage on V_{IN}, $\overline{SHDN}$ ..... (GND - 0.3V) to (V_{IN}+0.3V)
Maximum Voltage on V_{OUT1} ..... (GND - 0.3V) to 22V
Maximum Voltage on V_{OUT2} ..... (GND - 0.3V) to 5.5V
Maximum Voltage on PWG_1, PWG_2 ..... (GND-0.3V) to 5.5V
Output Short-Circuit Duration ..... Unlimited **(Note 2)**
Storage Temperature ..... –55°C to +175°C
ESD protection on all pins:
HBM ..... ≥ 4 kV
MM ..... ≥ 300V
CDM 8L SOIC ..... ≥ 1000V
CDM 8L VDFN ..... ≥ 2000V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{R1} + 1V$ **(Note 1)**, $I_{OUT1} = I_{OUT2} = 1$ mA, $C_{IN} = C_{OUT1} = C_{OUT2} = 3.3$ µF ceramic (X7R), $T_A = +25°C$, $\overline{SHDN} > 2.4V$. **Boldface** type applies for ambient temperatures T_A of –40°C to +150°C

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Voltage Supply						
Input Operating Voltage	V_{IN}	**4.5**	–	**55**	V	
UVLO Input Threshold	$UVLOV_{IN}$	–	2.7	–	V	Rising V_{IN}
UVLO Input Hysteresis		–	0.4	–	V	Falling V_{IN}
Quiescent Current	I_Q	–	50	**80**	µA	$I_{OUT1} = I_{OUT2} = 0$ mA
Quiescent Current for $\overline{SHDN}$ mode	$I_{Q\_\overline{SHDN}}$	–	4	**14**	µA	$\overline{SHDN}$ = GND, V_{IN} = 55V
Ground Current	I_{GND}	–	90	**190**	µA	I_{OUT1} = 50 mA, I_{OUT2} = 100 mA
Ground Current in Dropout	I_{DROP}	–	90	**200**	µA	$V_{OUT} \le 90\%$ of V_R, I_{OUT1} = 0 to 50 mA, I_{OUT2} = 0 to 100 mA

Note 1: V_{R1} is the nominal output voltage for LDO_1 the min input voltage is $V_{IN} = V_{R1} + 1V$ or $V_{IN} = V_{IN\_MIN}$ whichever is greater.

2: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

3: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_{R1} + 1V$ or $V_{IN} = V_{IN\_MIN}$ which ever is greater.

4: Characterized, not Production Tested.

5: PSRR measurement is carried out with C_{IN} = 0 µF, V_{IN} = 14.5V, V_{INAC} = 0.4 V_{pkpk}. For LDO_1 measurement I_{OUT1} = 30 mA and I_{OUT2} = 1 mA and for LDO_2 measurement I_{OUT2} = 70 mA and I_{OUT1} = 1 mA.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{R1} + 1V$ (**Note 1**), $I_{OUT1} = I_{OUT2} = 1$ mA, $C_{IN} = C_{OUT1} = C_{OUT2} = 3.3$ µF ceramic (X7R), $T_A = +25°C$, $\overline{SHDN} > 2.4V$. **Boldface** type applies for ambient temperatures T_A of –40°C to +150°C

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
LDO_1						
Maximum Output Current	I_{OUT1}	**50**	–	–	mA	
Line Regulation from V_{IN}	$\Delta V_{OUT1}/(\Delta V_{IN} x V_{OUT1})$	-0.05	0.0002	+0.05	% /V	V_{IN} = 13V to $V_{IN(MAX)}$ V_{OUT1} = 1 mA V_{OUT2} = 1 mA
Load Regulation LDO_1	$\Delta V_{OUT1}/V_{OUT1}$	**-0.1**	0.01	**+0.1**	%	$V_{IN} = V_{R1} + 1V$ V_{OUT1} = 1 to 50 mA V_{OUT2} = 1 mA
Output Voltage Accuracy	–	**V_{R1} - 2**	–	**V_{R1} + 2**	%	
Dropout Voltage	V_{DROP1}	–	–	**0.75**	V	I_{OUT1} = 50 mA (**Note 3**)
LDO_2						
Maximum Output Current	I_{OUT2}	**100**	–	–	mA	
Line Regulation from V_{IN}	$\Delta V_{OUT2}/(\Delta V_{IN} x V_{OUT2})$	**-0.05**	0.0002	**+0.05**	% /V	$V_{IN} = V_{R1} + 1$ to $V_{IN(MAX)}$ V_{OUT1} = 1 mA V_{OUT2} = 1 mA
Load Regulation LDO_2	$\Delta V_{OUT2}/V_{OUT2}$	**-0.5**	0.01	**+0.5**	%	$V_{IN} = V_{R1} + 1V$ V_{OUT1} = 1 mA V_{OUT2} = 1 to 100 mA
Output Voltage Accuracy	–	**V_{R2} - 2**	–	**V_{R2} + 2**	%	
Dropout Voltage	V_{DROP2}	–	–	**0.75**	V	I_{OUT2} = 100 mA (**Note 3**)
Shutdown Voltage Input						
Logic High Input	$V_{\overline{SHDN}\text{-HIGH}}$	**2.4**	–	–	V	
Logic High low	$V_{\overline{SHDN}\text{-HIGH}}$	–	–	**0.75**	V	
$\overline{SHDN}$ Input Leakage Current	$\overline{SHDN}_{ILK}$	–	–	**0.2**	µA	$\overline{SHDN}$ = 55V
Power Good						
PWRGD Input Voltage Range	V_{PG_VIN}	–	–	**5**	V	I_{PWRGD_SINK} = 5 mA

Note 1: V_{R1} is the nominal output voltage for LDO_1 the min input voltage is $V_{IN} = V_{R1} + 1V$ or $V_{IN} = V_{IN\_MIN}$ whichever is greater.

2: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

3: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_{R1} + 1V$ or $V_{IN} = V_{IN\_MIN}$ which ever is greater.

4: Characterized, not Production Tested.

5: PSRR measurement is carried out with C_{IN} = 0 µF, V_{IN} = 14.5V, V_{INAC} = 0.4 V_{pkpk}. For LDO_1 measurement I_{OUT1} = 30 mA and I_{OUT2} = 1 mA and for LDO_2 measurement I_{OUT2} = 70 mA and I_{OUT1} = 1 mA.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{R1} + 1V$ **(Note 1)**, $I_{OUT1} = I_{OUT2} = 1$ mA, $C_{IN} = C_{OUT1} = C_{OUT2} = 3.3$ µF ceramic (X7R), $T_A = +25°C$, $\overline{SHDN} > 2.4V$. **Boldface** type applies for ambient temperatures T_A of –40°C to +150°C

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
PWRGD Threshold VS V_{OUT} voltage	V_{PG_TH}	**90**	92	**94**	%Vout	Falling Edge of V_{OUT}
PWRGD Threshold Hysteresis VS V_{OUT} Voltage	V_{PG_HYS}	**1**	2.0	**3**	$\%V_{OUT}$	Rising Edge of V_{OUT}
PWRGD Output Voltage Low	V_{PG_LOW}	–	0.2	**0.45**	V	I_{PWRGD_SINK}= 5 mA, V_{OUT} = 0V
PWRGD Output Sink Current	I_{PWRGD_SINK}	**5**	–	–	mA	$V_{PWRGD} \leq 0.45V$
PWRGD Output Leakage	$PWRGD_{LKG}$	–	–	**0.2**	µA	$V_{PWRGD} = 5.5V$
PWRGD Time Delay	T_{PWG}	–	115	–	µs	**Rising Edge, (Note 4)**
Detect Threshold to PWRGD Active Time Delay	T_{VDET_PWG}	–	115	–	µs	V_{OUT} goes from V_{OUT} below V_{OUT} - V_{PWRGD_TH} - 50 mV, (Note 4)
Output Discharge Transistor						
Discharge Resistance LDO1	R_{DS_LDO1}	–	90	–	Ω	Note 4
Discharge Resistance LDO2	R_{DS_LDO2}	–	90	–	Ω	Note 4
Protection Features						
FoldBack Current Corner V_{OUT1}	I_{SC1_LIMIT}	–	170	–	mA	Note 4
FoldBack Current Limit V_{OUT1}	I_{LIMIT1}	–	10	–	mA	
FoldBack Current Corner V_{OUT2}	I_{SC2_LIMIT}	–	230	–	mA	
FoldBack Current Limit V_{OUT2}	I_{LIMIT2}	–	10	–	mA	
Transient Performance						
Startup Delay	T_{DELAY}	–	1200	**2500**	µs	
AC Performance						

Note 1: V_{R1} is the nominal output voltage for LDO_1 the min input voltage is $V_{IN} = V_{R1} + 1V$ or $V_{IN} = V_{IN\_MIN}$ whichever is greater.

2: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

3: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_{R1} + 1V$ or $V_{IN} = V_{IN\_MIN}$ which ever is greater.

4: Characterized, not Production Tested.

5: PSRR measurement is carried out with C_{IN} = 0 µF, V_{IN} = 14.5V, V_{INAC} = 0.4 V_{pkpk}. For LDO_1 measurement I_{OUT1} = 30 mA and I_{OUT2} = 1 mA and for LDO_2 measurement I_{OUT2} = 70 mA and I_{OUT1} = 1 mA.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{R1} + 1V$ **(Note 1)**, $I_{OUT1} = I_{OUT2} = 1$ mA, $C_{IN} = C_{OUT1} = C_{OUT2} = 3.3$ µF ceramic (X7R), $T_A = +25°C$, $\overline{SHDN} > 2.4V$. **Boldface** type applies for ambient temperatures T_A of –40°C to +150°C

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Noise LDO1	e_{N1}	–	550	–	μV_{RMS}	f = 10 Hz to 10 MHz, I_{OUT1} = 30 mA, V_{IN} = 16V, (**Note 4**)
Output Noise LDO2	e_{N2}	–	300	–		f = 10 Hz to 10 MHz, I_{OUT} = 70 mA, V_{IN} = 16V, (**Note 4**)
Power Supply Ripple Rejection Ratio	PSRR	–	-80	–	dB	f = 100 Hz **(Note 4, Note 5)**

Note 1: V_{R1} is the nominal output voltage for LDO_1 the min input voltage is $V_{IN} = V_{R1} + 1V$ or $V_{IN} = V_{IN\_MIN}$ whichever is greater.

2: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

3: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_{R1} + 1V$ or $V_{IN} = V_{IN\_MIN}$ which ever is greater.

4: Characterized, not Production Tested.

5: PSRR measurement is carried out with C_{IN} = 0 µF, V_{IN} = 14.5V, V_{INAC} = 0.4 V_{pkpk}. For LDO_1 measurement I_{OUT1} = 30 mA and I_{OUT2} = 1 mA and for LDO_2 measurement I_{OUT2} = 70 mA and I_{OUT1} = 1 mA.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Thermal Shutdown	T_{SD}	–	178	182	°C	Rising Temperature, (**Note 4**)
Thermal Shutdown Hysteresis	ΔT_{SD}	–	18	–	°C	Falling Temperature, (**Note 4**)
Operating Junction Temperature	T_J	-40	–	150	°C	
Package Thermal Resistances						
Thermal Resistances, VDFN 8L with Exposed Pad	θ_{JA}	–	72	–	°C/W	Simulated values, natural convection method, per EIA/JEDEC JESD51-751-7 4 layer board (**Note 2**)
	θ_{JC}	–	85	–	°C/W	Simulated values, top cold plate, per EIA/JEDEC JESD51-751-7 4 layer board (**Note 2**)
	θ_{JB}	–	23	–	°C/W	Simulated values, ring cold plate, per EIA/JEDEC JESD51-751-7 4 layer board (**Note 2**)
	Ψ_{JT}	–	4.02	–	°C/W	Simulated values, natural convection method, per EIA/JEDEC JESD51-751-7 4 layer board (**Note 2**)

TEMPERATURE SPECIFICATIONS (CONTINUED)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Thermal Resistances, SOIC 8L with Exposed Pad	θ_{JA}	–	53	–	°C/W	Simulated values, natural convection method, per EIA/JEDEC JESD51-751-7 4 layer board (**Note 2**)
	θ_{JC}	–	67	–	°C/W	Simulated values, top cold plate, per EIA/JEDEC JESD51-751-7 4 layer board (**Note 2**)
	θ_{JB}	–	27	–	°C/W	Simulated values, ring cold plate, per EIA/JEDEC JESD51-751-7 4 layer board (**Note 2**)
	Ψ_{JT}	–	7.41	–	°C/W	Simulated values, natural convection method, per EIA/JEDEC JESD51-751-7 4 layer board (**Note 2**)

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (for example, outside the specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $C_{IN} = C_{OUT1} = C_{OUT2}$ = 3.3 µF ceramic (X7R), $I_{OUT1} = I_{OUT2}$ = 1 mA, T_A = +25°C, $V_{IN} = V_{R1}$ + 1V, SHDN = 1 MΩ pull-up to V_{IN}.

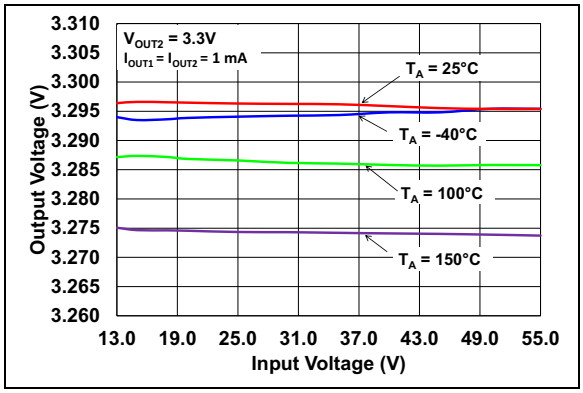


FIGURE 2-1: *Output Voltage vs. Input Voltage (V_R = 3.3V).*

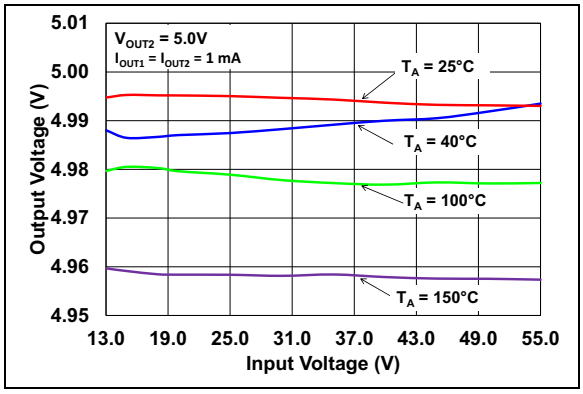


FIGURE 2-2: *Output Voltage vs Input Voltage (V_R = 5.0V).*

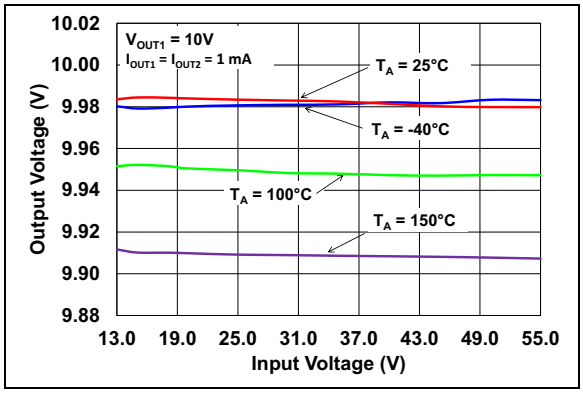


FIGURE 2-3: *Output Voltage vs Input Voltage (V_R = 10V).*

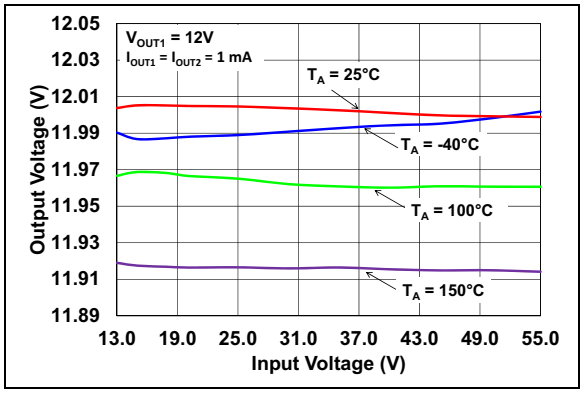


FIGURE 2-4: *Output Voltage vs Input voltage (V_R = 12V).*

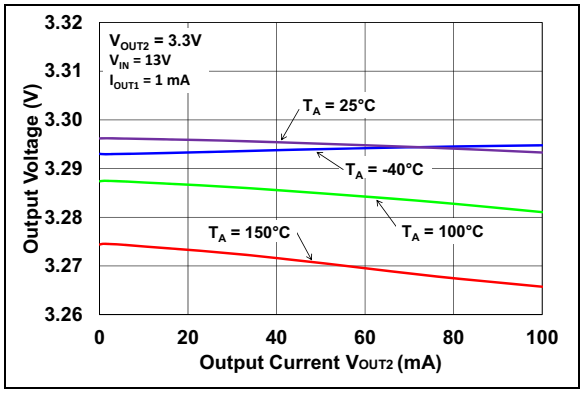


FIGURE 2-5: *Output Voltage vs. Load Current (V_R = 3.3V).*

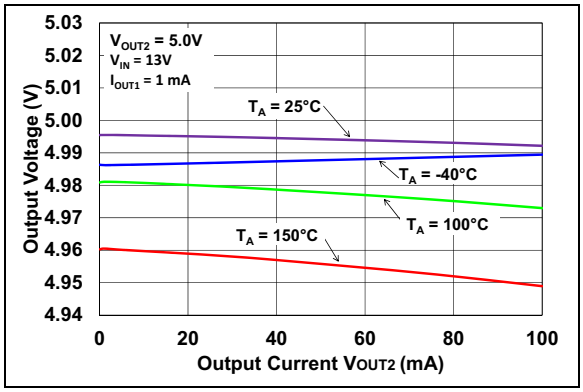


FIGURE 2-6: *Output Voltage vs. Load Current (V_R = 5.0V).*

Note: Unless otherwise indicated, $C_{IN} = C_{OUT1} = C_{OUT2}$ = 3.3 µF ceramic (X7R), $I_{OUT1} = I_{OUT2}$ = 1 mA, T_A = +25°C, $V_{IN} = V_{R1}$ + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

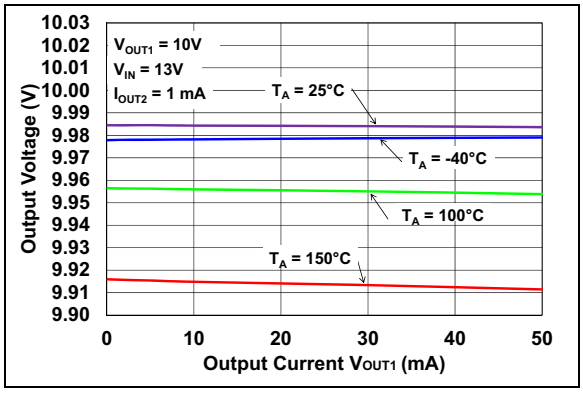


FIGURE 2-7: *Output Voltage vs. Load Current (V_R = 10V).*

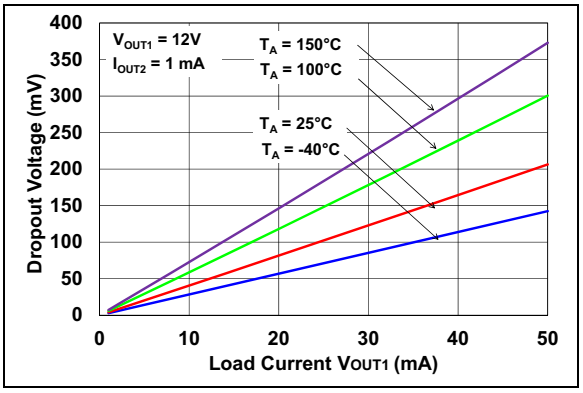


FIGURE 2-10: *Dropout Voltage vs. Load Current (V_R = 12V).*

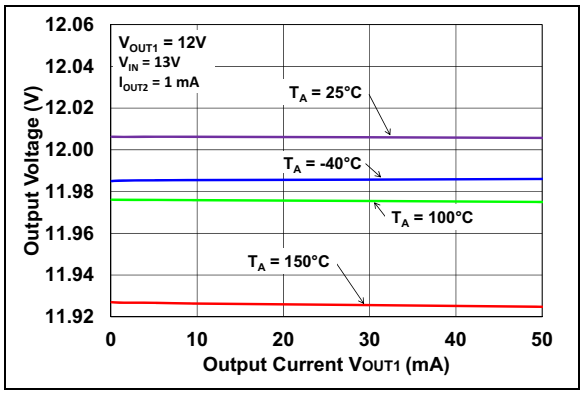


FIGURE 2-8: *Output Voltage vs. Load Current (V_R = 12V).*

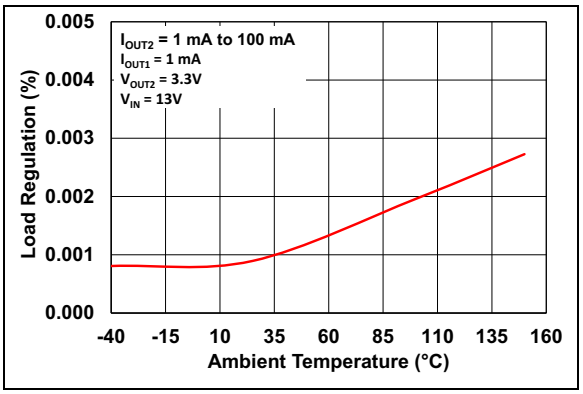


FIGURE 2-11: *Load Regulation vs. Ambient Temperature (V_R = 3.3V).*

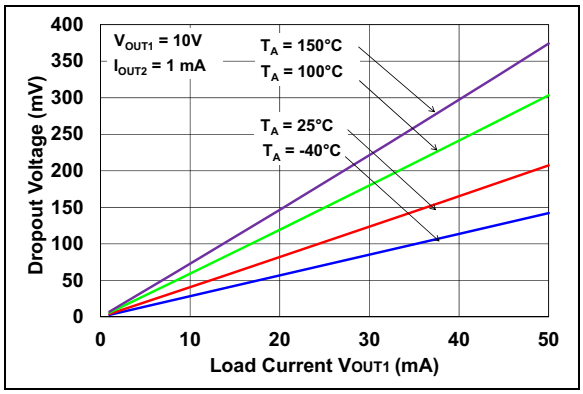


FIGURE 2-9: *Dropout Voltage vs. Load Current (V_R = 10V).*

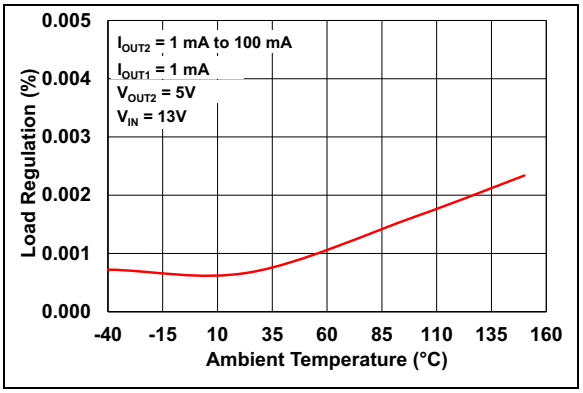


FIGURE 2-12: *Load Regulation vs. Ambient Temperature (V_R = 5.0V).*

Note: Unless otherwise indicated, $C_{IN} = C_{OUT1} = C_{OUT2}$ = 3.3 µF ceramic (X7R), $I_{OUT1} = I_{OUT2}$ = 1 mA, T_A = +25°C, $V_{IN} = V_{R1}$ + 1V, SHDN = 1 MΩ pull-up to V_{IN}.

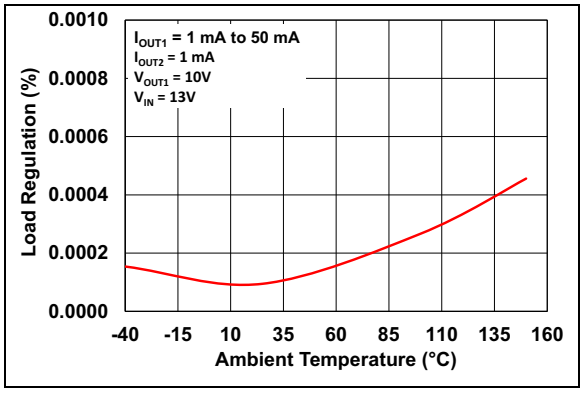


FIGURE 2-13: *Load Regulation vs. Ambient Temperature (V_R = 10V).*

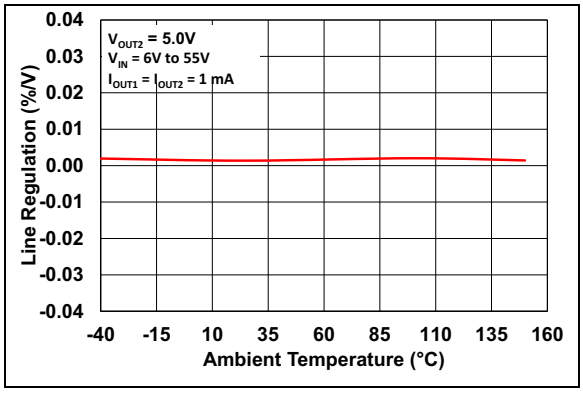


FIGURE 2-16: *Line Regulation vs. Ambient Temperature (V_R = 5.0V).*

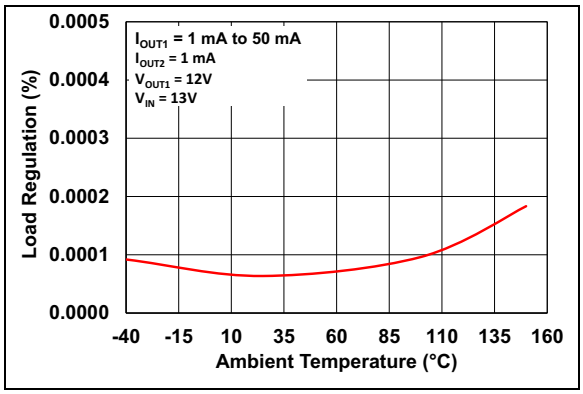


FIGURE 2-14: *Load Regulation vs. Ambient Temperature (V_R = 12V).*

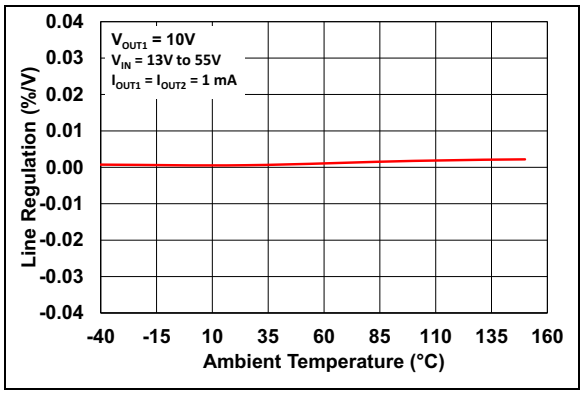


FIGURE 2-17: *Line Regulation vs. Ambient Temperature (V_R = 10V).*

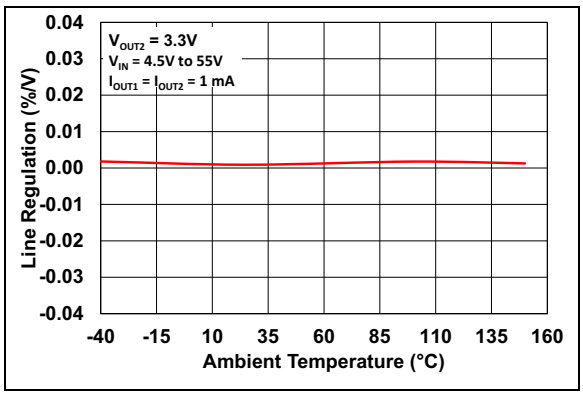


FIGURE 2-15: *Line Regulation vs. Ambient Temperature (V_R = 3.3V).*

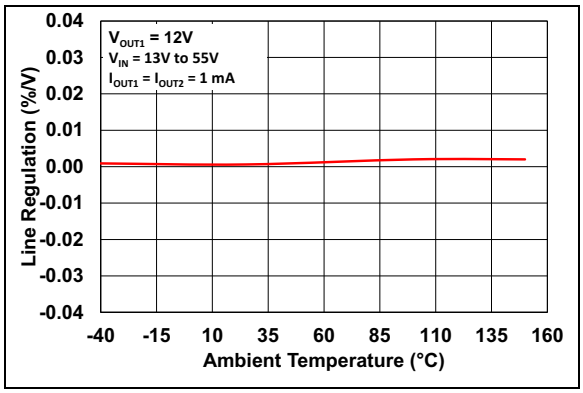


FIGURE 2-18: *Line Regulation vs. Ambient Temperature (V_R = 12V).*

Note: Unless otherwise indicated, $C_{IN} = C_{OUT1} = C_{OUT2}$ = 3.3 µF ceramic (X7R), $I_{OUT1} = I_{OUT2}$ = 1 mA, T_A = +25°C, $V_{IN} = V_{R1}$ + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

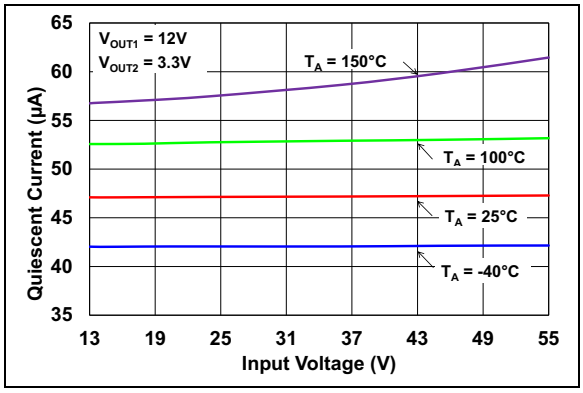


FIGURE 2-19: *Quiescent Current vs. Input voltage (V_R = 3.3V & V_R = 12V).*

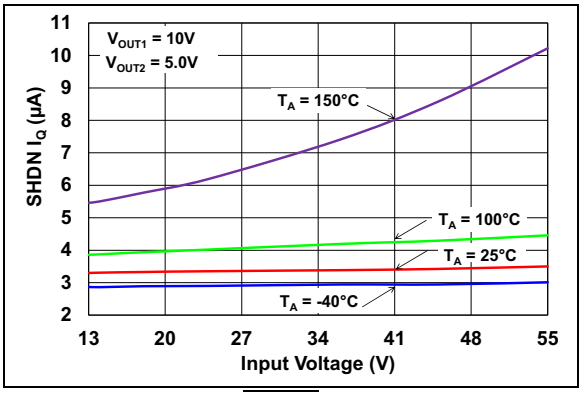


FIGURE 2-22: *$\overline{SHDN}$ Quiescent Current vs. Input voltage (V_R = 5.0V & V_R = 10V).*

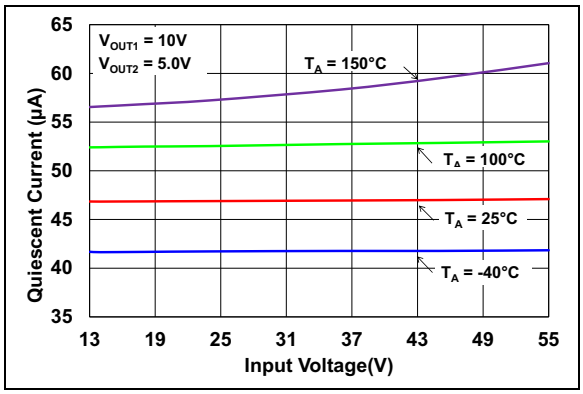


FIGURE 2-20: *Quiescent Current vs. Input Voltage (V_R = 5.0V & V_R = 10V).*

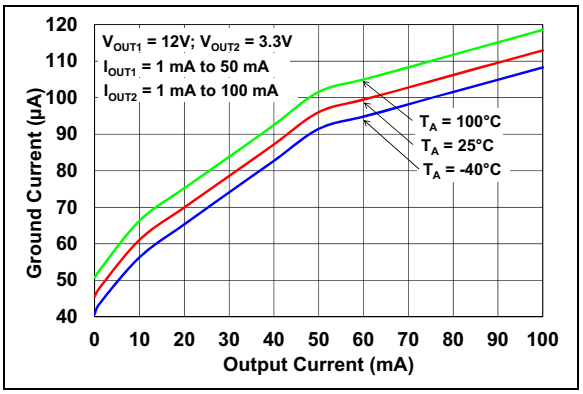


FIGURE 2-23: *Ground Current vs. Load Current (V_R = 3.3V & V_R = 12V).*

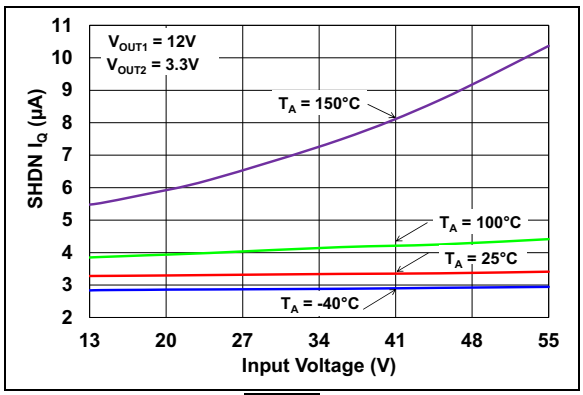


FIGURE 2-21: *$\overline{SHDN}$ Quiescent Current vs. Input voltage (V_R = 3.3V & V_R = 12V).*

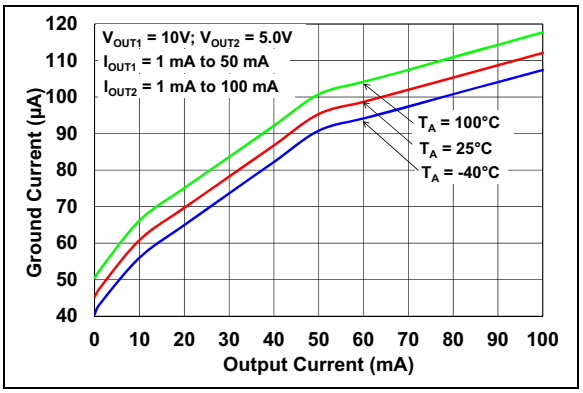


FIGURE 2-24: *Ground Current vs. Load Current (V_R = 5.0V & V_R = 10V).*

Note: Unless otherwise indicated, $C_{IN} = C_{OUT1} = C_{OUT2}$ = 3.3 µF ceramic (X7R), $I_{OUT1} = I_{OUT2}$ = 1 mA, T_A = +25°C, $V_{IN} = V_{R1}$ + 1V, SHDN = 1 MΩ pull-up to V_{IN}.

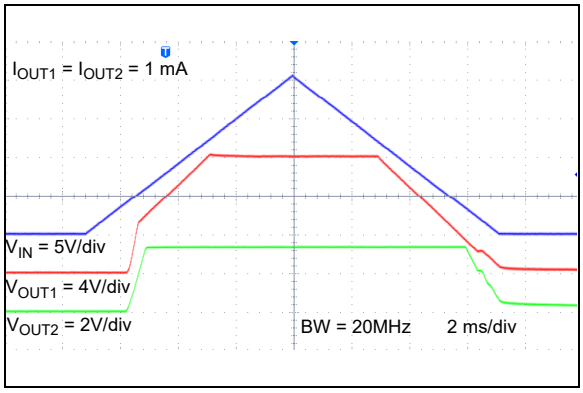


FIGURE 2-25: *UVLO (V_R = 3.3V & V_R = 12V).*

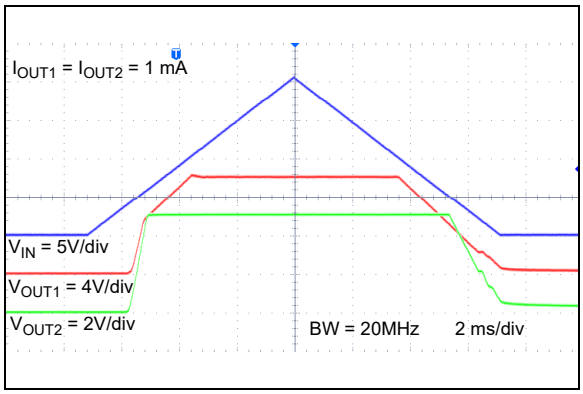


FIGURE 2-26: *UVLO (V_R = 5.0V & V_R = 10V).*

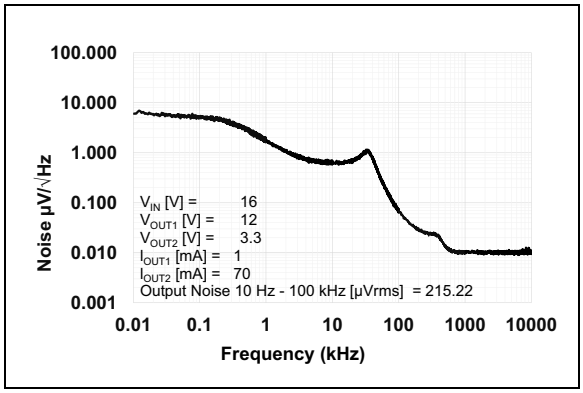


FIGURE 2-27: *Noise vs. Frequency (V_R = 3.3V).*

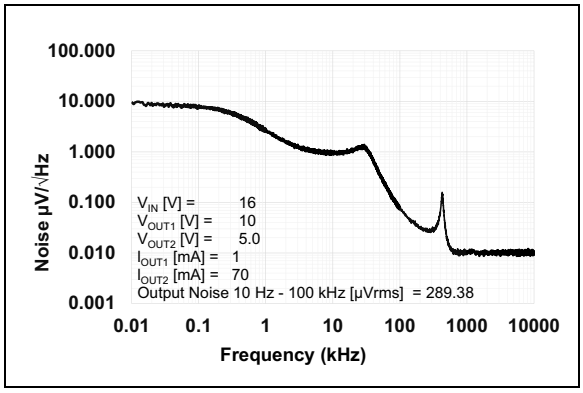


FIGURE 2-28: *Noise vs. Frequency (V_R = 5.0V).*

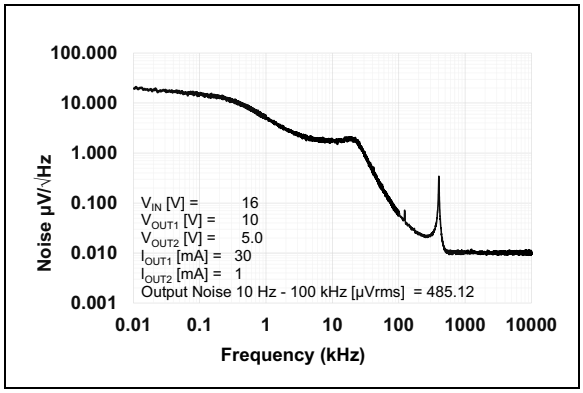


FIGURE 2-29: *Noise vs. Frequency (V_R = 10V).*

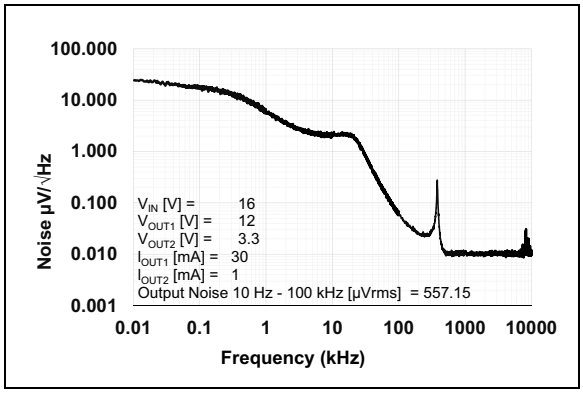


FIGURE 2-30: *Noise vs. Frequency (V_R = 12V).*

Note: Unless otherwise indicated, $C_{IN} = C_{OUT1} = C_{OUT2}$ = 3.3 µF ceramic (X7R), $I_{OUT1} = I_{OUT2}$ = 1 mA, T_A = +25°C, $V_{IN} = V_{R1}$ + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

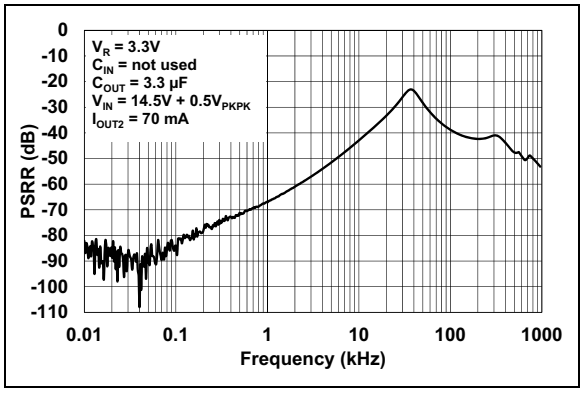


FIGURE 2-31: *PSRR vs. Frequency (V_R = 3.3V).*

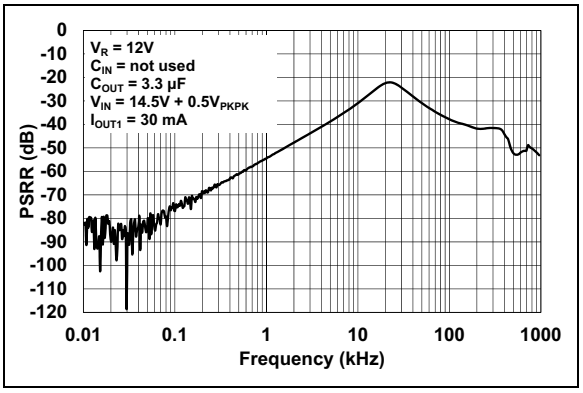


FIGURE 2-34: *PSRR vs. Frequency (V_R = 12V).*

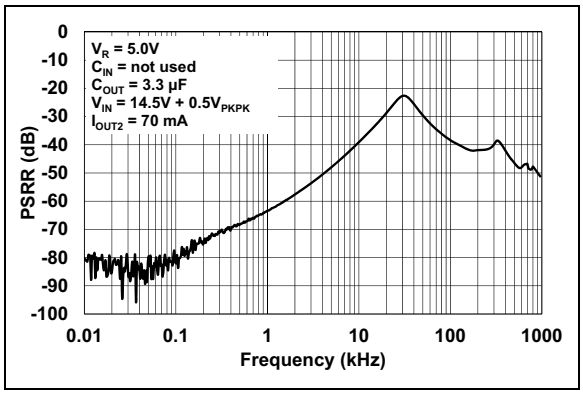


FIGURE 2-32: *PSRR vs. Frequency (V_R = 5.0V).*

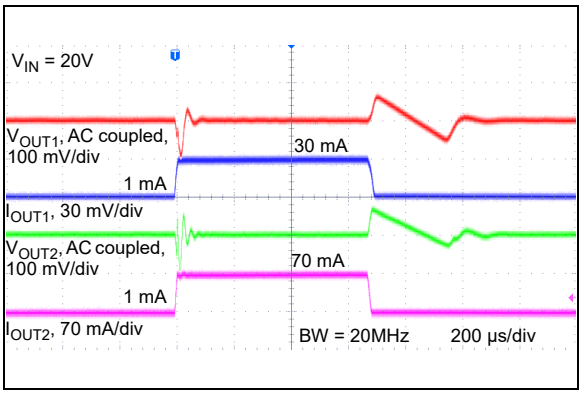


FIGURE 2-35: *Dynamic Load Step (V_R = 3.3V & V_R = 12V).*

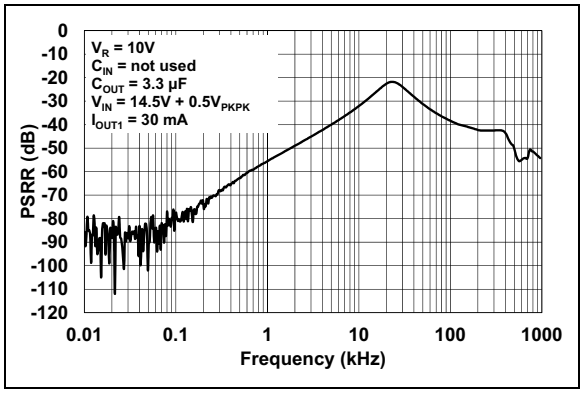


FIGURE 2-33: *PSRR vs. Frequency (V_R = 10V).*

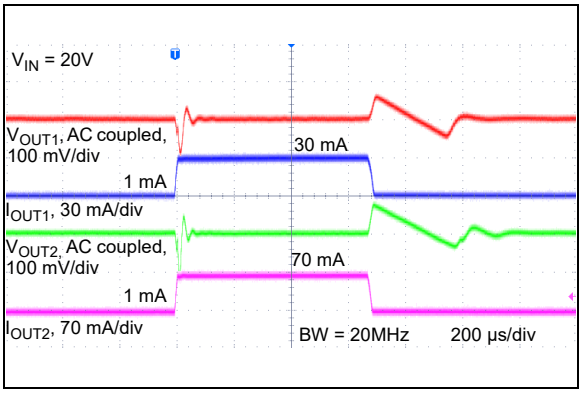


FIGURE 2-36: *Dynamic Load Step (V_R = 5.0V & V_R = 10V).*

Note: Unless otherwise indicated, $C_{IN} = C_{OUT1} = C_{OUT2} = 3.3\ \mu F$ ceramic (X7R), $I_{OUT1} = I_{OUT2} = 1$ mA, $T_A = +25°C$, $V_{IN} = V_{R1} + 1V$, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

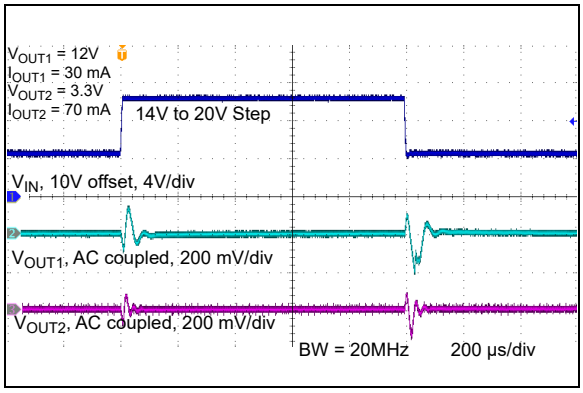


FIGURE 2-37: *Dynamic Line Step (V_R = 3.3V & V_R = 12V).*

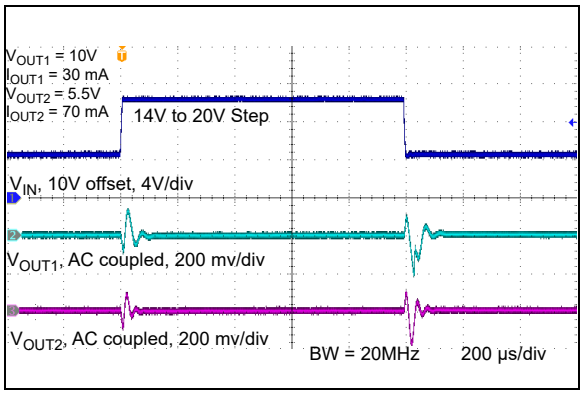


FIGURE 2-38: *Dynamic Line Step (V_R = 3.3V & V_R = 12V).*

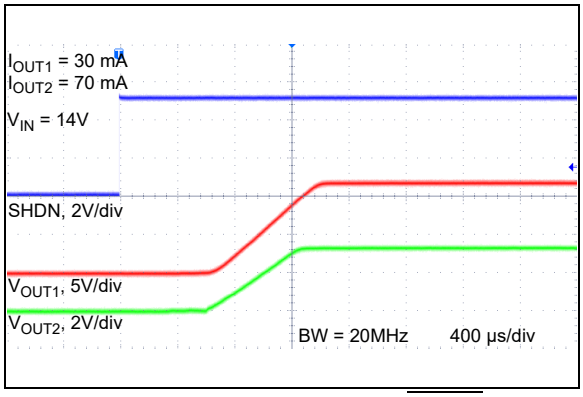


FIGURE 2-39: *Start-up from $\overline{SHDN}$ (0V to 5V) (V_R = 3.3V & V_R = 12V)*

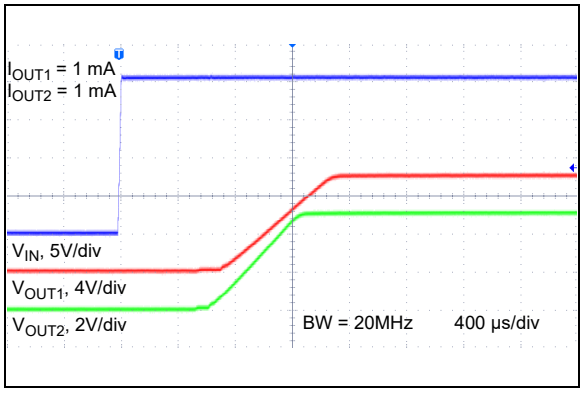


FIGURE 2-40: *Start-up from V_{IN} (0V to 14V) (V_R = 5V & V_R = 10V)*

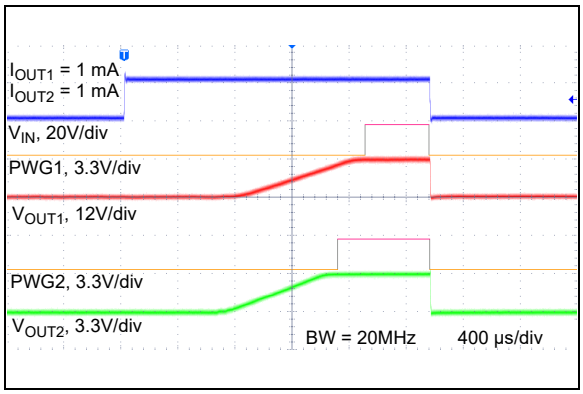


FIGURE 2-41: *Power Good Transition (VR=3.3V & VR=12V).*

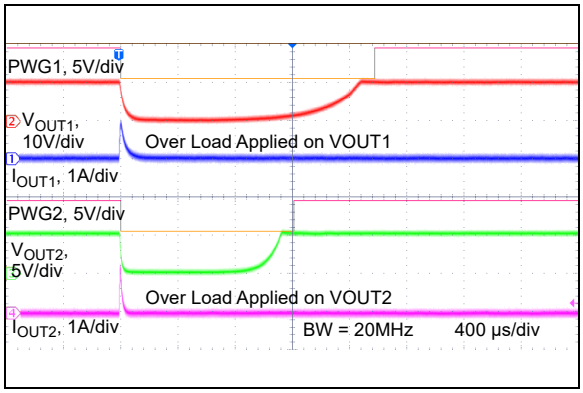


FIGURE 2-42: *Power Good Fault Trigger (VR=5V & VR=10V).*

NOTES:

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

8 Lead DFN	8 Lead SOIC	Symbol	Description
1	1	PWG_1	Open Drain Power Good V_{OUT1}
2	2	GND	Ground
3	3	PWG_2	Open Drain Power Good V_{OUT2}
4	4	$\overline{SHDN}$	Shutdown Control Input (active-low). Do not leave this pin floating.
5	5	V_{OUT2}	Regulated Output Voltage V_{R2} for Second LDO
6	6	NC	Not Connected Pins (should either be left floated or connected to ground)
7	7	V_{IN}	Input Voltage Supply
8	8	V_{OUT1}	Regulated Output Voltage V_{R1} for First LDO
9	9	EP	Exposed Pad - Connect to GND

3.1 Ground Pin (GND)

For optimal noise and Power Supply Rejection Ratio (PSRR) performance, the GND pin of the LDO should be tied to an electrically “quiet” circuit ground. This ensures the LDO power supply rejection ratio and noise device performance. The GND pin of the LDO conducts only ground current, so a wide trace is not required. For applications that have switching or noisy inputs, tie the GND pin to the return of the output capacitor. Ground planes help to lower the inductance and thus reduce the effect of fast current transients.

3.2 Regulated Output Voltage Pin (V_{OUT1} & V_{OUT2})

The V_{OUT1} or V_{OUT2} pins are the regulated output voltage V_R of the respective LDOs. A minimum output capacitance of 3.3 µF is required for each LDO to ensure the stability in all typical applications.

MCP1722 is stable with ceramic capacitors. For more information on output capacitor selection guidance, see **4.1 “Device Overview”**.

3.3 Input Voltage Supply Pin (V_{IN})

Connect the input voltage source to V_{IN}. If the input voltage source is located several inches away from the LDO, or the input source is a battery, it is recommended that an input capacitor be used. A typical input capacitance value of 3.3 µF to 10 µF should be sufficient for most applications. The type of capacitor used is ceramic. However, the low ESR characteristics of the ceramic capacitor will yield better noise and PSRR performance at high frequency.

3.4 Shutdown Control Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is used to turn the LDO output voltage off. Consequently, when the $\overline{SHDN}$ input is at a logic high level, the LDO output voltage is enabled and, when the $\overline{SHDN}$ input is pulled to a logic low level, the LDO output voltage is disabled.

Furthermore, when the $\overline{SHDN}$ input is pulled to a logic-low level, the LDO enters a low-quiescent current shutdown state, where the typical quiescent current is 4 µA.

3.5 Power Good Output (PWG_1 & PWG_2)

PWG_1 and PWG_2 are open drain outputs that can be connected to either 3.3V or 5.0V with a pull-up resistor, to monitor the status of the LDO regulated output voltages. PWG_1 monitors the state for $VOUT_1$ and PWG_2 for $VOUT_2$, respectively.

When the regulated output voltages are above 94%, typically, the power good pins will indicate a logic high state. Similarly if the value drops below 94%, the pins will transition to a logic low state.

3.6 Exposed Pad (EP)

To help with the part's thermal dissipation, both packages have an exposed pad tied internally to GND. It is recommended to connect the Exposed Pad to a solid GND plane with multiple vias, to help dissipate excess heat.

4.0 DETAILED DESCRIPTION

4.1 Device Overview

MCP1722 is a dual output LDO, where LDO_1 has a V_R of 10V or 12V and LDO_2, a V_R of 3.3V or 5.0V. This output combination can be used for powering both a MOSFET driver and a µProcessor.

The LDO also comes with high voltage $\overline{SHDN}$ input and low voltage Power Good feedback for regulated output voltages, thus allowing the µProcessor to monitor the state of the power supply and safely shutdown the application, in the case of a power fail.

The LDO requires a 3.3 µF output capacitor for each output in order to maintain stability. The capacitors will be discharged by the internal discharge blocks, which have a typical resistance of 90Ω and are activated when the part enters a shutdown state.

The device also features a good PSRR of typ -80 dB for low frequencies.

MCP1722 has a temperature range of -40°C to +150°C and is AEC-Q100 qualified grade 0 capable and has passed 65V Load Dump testing, per ISO 7637-2/2004.

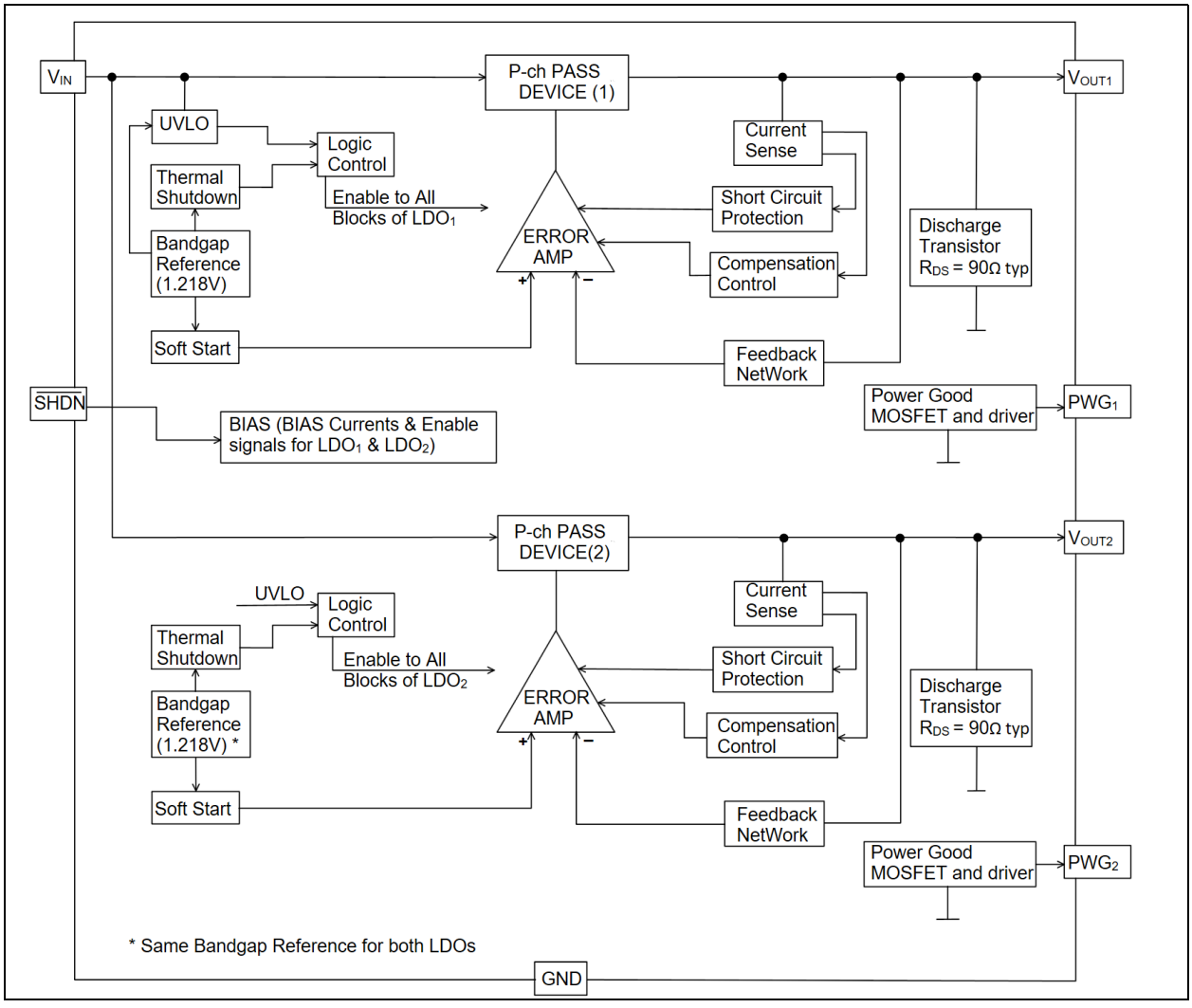


FIGURE 4-1: *Functional Block Diagram.*

4.2 Output Capacitance Requirements

MCP1722 requires a minimum output capacitance of 3.3 µF which can be increased up to 33 µF for output voltage stability. The output capacitor should be located as close to the LDO output as is practical. The device was designed to work with low ESR ceramic capacitors. Ceramic materials X8R\L or X7R have low temperature coefficients and are well within the acceptable ESR range required. A typical 3.3 µF X7R 0805 capacitor has an ESR of 50 mΩ.

4.3 Input Capacitance Requirements

For the LDO output to operate correctly, a low input-source impedance is required. When operating using battery power, or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 3.3 µF to 10 µF of capacitance is recommended for most applications. Given the high input voltage capability of the part (of up to 55V DC), it is recommended to use appropriate voltage rating capacitor, and the de-rating of the capacitance as a function of voltage needs to be taken into account; similar with the output capacitor the ceramic materials need to be X7R or X8R\L because these dielectrics are rated for use with temperatures between -40°C to +125°C or respectively -55°C to +150°C.

4.4 Circuit Protection

MCP1722 features current foldback protection during an output short circuit event, that occurs in normal operation. The foldback current protection is independent for each LDO. When the current foldback block detects an increase in load current, over the typical value of each LDO (see **Section 1.0 "Electrical Characteristics"**), the output current and output voltage will start to decrease until the output current reaches a value of typically 10 mA.

If a short circuit is present during power up the part will enter current limit protection.

MCP1722 was tested using the AEC-Q100 test set-up outlined in Figure 4-2. The testing conditions require the use of very high parasitic inductances on the input and output. For cases such as this, it is required to prevent the output voltage from going below ground by more than 1V (the VOUT pin can withstand a maximum of -0.3VDC). For more information, see **Section "Absolute Maximum Ratings †"**. This can be achieved by placing a diode with the cathode to V_{OUT} and anode to ground.

The thermal shutdown functionality is present on the device and adds to the part's protection features. Typically, thermal shutdown is triggered when the part reaches 178°C and has a typical hysteresis of 18°C.

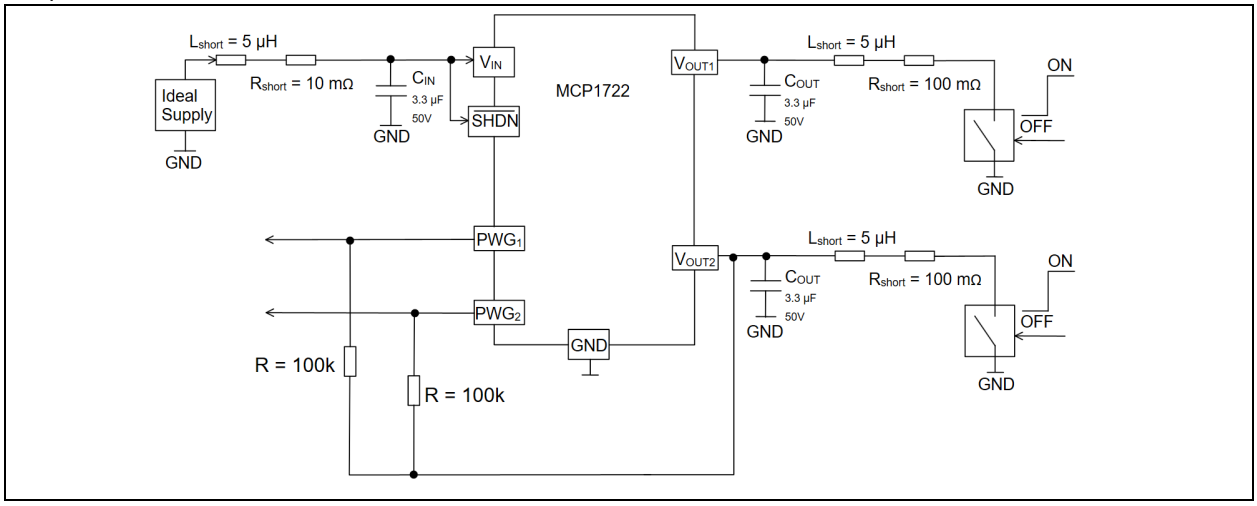


FIGURE 4-2: *Short Circuit Test Set-Up.*

4.5 Dropout Operation

For LDO1, the part can be found operating in a dropout condition when considering the minimum input voltage of 4.5V. Until the supply voltage reaches a value that is equal to V_{R1} + 750 mV, LDO_1 will be tracking the input supply voltage. It is preferred to make sure that the part does not operate in dropout during DC operation so that the AC performance is maintained. The same conditions apply to LDO_2.

The device has a dropout voltage of approximately 250 mV at full load and room temperature, but because of the extended temperature range of 150°C, due to increased leakage, it reaches up to 750 mV.

4.6 Shutdown Input ($\overline{SHDN}$) and Input UVLO

The $\overline{SHDN}$ input is an active-low input signal that turns the LDO on or off. The $\overline{SHDN}$ threshold has a logic HIGH level of minimum 2.4V and a logic LOW level of maximum 0.75V.

The $\overline{SHDN}$ pin ignores low-going pulses that are up to 30 µs. This blanking window helps to reject any system noise spikes on the $\overline{SHDN}$ input signal. Then, on the rising edge of the $\overline{SHDN}$ input, the shutdown circuitry adds 1.2 ms delay before allowing the regulator output to turn on. This delay helps to reject any false turn-on signals or noise on the $\overline{SHDN}$ input signal. After the typical 1.2 ms delay, the regulator start charging the load capacitor as the output rises from 0V to its

regulated value. The charging current will be limited by the current limit value of the device. If the $\overline{SHDN}$ input signal is pulled low during the 1.2 ms delay period, the timer will be reset and the delay time will start over again on the next rising edge of the $\overline{SHDN}$ input. Figure 4-3 shows a timing diagram of the $\overline{SHDN}$ input.

The UVLO block helps prevent false start-ups, during power up sequence, until the input voltage reaches a value of 2.7V.

4.7 Power Good

The Power Good function is available for both LDO_1 and LDO_2, as they are both low voltage open drain outputs which can be used to monitor the output of the LDOs in relation with the Power Good Threshold level (V_{PWG_TH}), which is typically 92%.

During a normal start up sequence the open drain output is held low until the monitored regulated output voltage reaches the value of V_{PWG_TH} plus the hysteresis value. After which the power good time delay (T_{PWG}) will start, and after 115 µs typically the PWG pin will become inactive and can be pulled high by the external pull up resistor connected to V_{OUT2} or a separate supply rail that is below 5.5V.

For those cases in which the power good is referenced to other external supply rails, when the part is powered up it is required to wait the typical start up delay of 1.2 ms before monitoring the power good pins, in order to prevent false readings.

During transient events, false triggering of the Power Good signals is prevented by means of time delay (T_{VDET_PWG}), typically, of 115 µs. After the internal circuitry detects the regulated output falling below the V_{PWG_TH} the open drained output won't be pulled low until the time delay pases. When the $\overline{SHDN}$ is pulled low, if the requirements for a valid signal are met, then the Power Good open drained will be pulled low. The output will be discharged by the output discharge block by means of 90Ω resistor pulled down to GND.

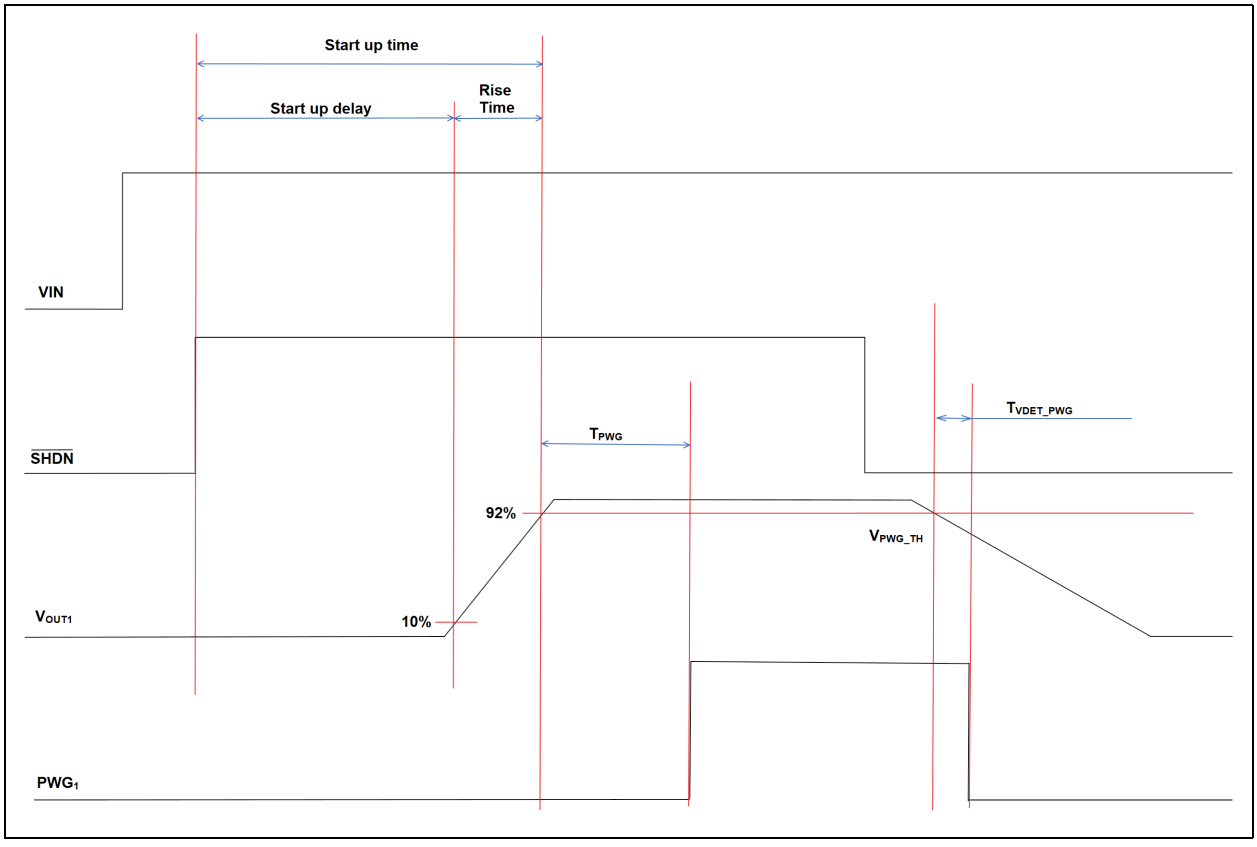


FIGURE 4-3: *Timing Diagram.*

4.8 Package and Device Qualifications

The Devices are AEC-Q100, grade 0 qualified, which allows the MCP1722 to be used within an extended temperature range, from -40°C to +150°C.

Additionally, both packages have a moisture sensitivity level (MSL) of 1.

5.0 APPLICATION INFORMATION

5.1 Typical Application

MCP1722 is used for applications that require medium input voltage and are prone to high input transient voltages.

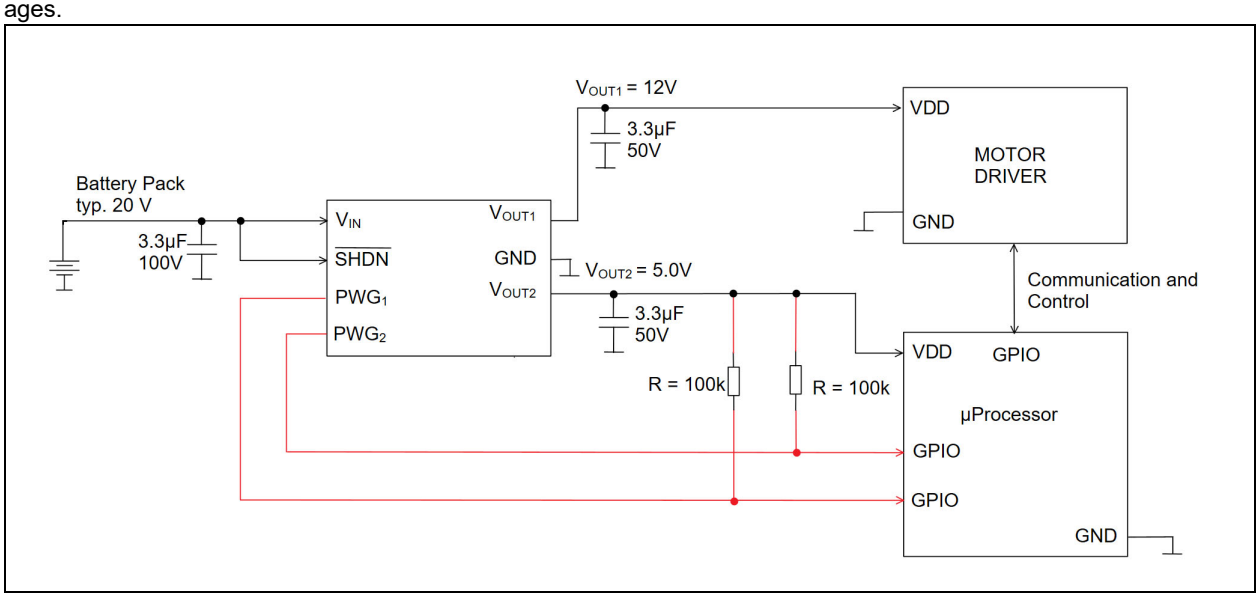


FIGURE 5-1: *Typical Application Circuit II.*

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation within the MCP1722 is a function of input voltage, output voltage, output current and quiescent current. Equation 5-2 can be used to calculate the internal power dissipation for one of the LDOs, while the total power dissipation is the sum of the power dissipated by LDO_1 and LDO_2 Equation 5-1.

EQUATION 5-1:

$$P_{LDO} = P_{LDO1} + P_{LDO2}$$

Where:

P_{LDO} = Total internal power dissipation of the LDO

P_{LDO1} = Internal power dissipation of the LDO_1 pass device

P_{LDO2} = Internal power dissipation of the LDO_2 pass device

EQUATION 5-2:

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

Where:

P_{LDO} = Internal power dissipation of the LDO pass device

$V_{IN(MAX)}$ = Maximum input voltage

$V_{OUT(MIN)}$ = LDO minimum output voltage

$I_{OUT(MAX)}$ = Maximum output current

In addition to the power dissipation due to the LDO P-ch pass device, additional power dissipation also occurs within MCP1722 as a result of quiescent or ground current. The power dissipation due to the ground current can be calculated using Equation 5-3:

EQUATION 5-3:

$$P_{I(GND)} = V_{IN(MAX)} \times I_{GND}$$

Where:

$P_{I(GND)}$ = Power dissipation due to the ground current of the LDO

$V_{IN(MAX)}$ = Maximum input voltage

I_{GND} = Current flowing into the GND pin

The total power dissipated within the MCP1722 is the sum of the power dissipated in the LDO pass device and the P(I_{GND}) term. Because of the CMOS construction, the typical I_{GND} for the MCP1722 is typical 90 µA at full load. Operating at a maximum V_{IN} of 55V results in a power dissipation of 5 mW for. For most applications, this is small compared to the LDO pass device power dissipation, and can be neglected.

The maximum continuous operating junction temperature specified for the MCP1722 is +150°C. To estimate the internal junction temperature of the MCP1722, the total internal power dissipation is multiplied by the thermal resistance from junction-to-ambient (θ_{JA}) of the device. For example, the thermal resistance from junction to ambient for the 8-Lead SOIC with exposed pad package is estimated at 53°C/W.

EQUATION 5-4:

$$T_{J(MAX)} = P_{LDO} \times \theta_{JA} + T_{A(MAX)}$$

Where:

$T_{J(MAX)}$ = Maximum continuous junction temperature

P_{LDO} = Total power dissipation of the device

θ_{JA} = Thermal resistance from junction to ambient

$T_{A(MAX)}$ = Maximum ambient temperature

The maximum power dissipation capabilities for a package can be calculated using the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. Equation 5-5 can be used to determine the package maximum internal power dissipation.

EQUATION 5-5:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{\theta_{JA}}$$

Where:

$P_{D(MAX)}$ = Maximum power dissipation of the device

$T_{J(MAX)}$ = Maximum continuous junction temperature

$T_{A(MAX)}$ = Maximum ambient temperature

θ_{JA} = Thermal resistance from junction to ambient

EQUATION 5-6:

$$T_{J(RISE)} = P_{D(MAX)} \times \theta_{JA}$$

Where:

$T_{J(RISE)}$ = Rise in the device junction temperature over the ambient temperature

$P_{D(MAX)}$ = Maximum power dissipation of the device

θ_{JA} = Thermal resistance from junction to ambient

EQUATION 5-7:

$$T_J = T_{J(RISE)} + T_A$$

Where:

T_J = Junction temperature

$T_{J(RISE)}$ = Rise in the device junction temperature over the ambient temperature

T_A = Ambient temperature

5.3 Typical Application Examples

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are all calculated in the example below. In this particular example, the power dissipation as a result of ground current is small enough to be negligible.

5.3.1 POWER DISSIPATION EXAMPLE

Package

Package Type = 8 Lead SOIC with Exposed Pad

Input Voltage

V_{IN} = 20V ± 5%

LDO Output Voltage and Current

V_{OUT1} = 12V

V_{OUT2} = 5.0V

I_{OUT2} = 30 mA

I_{OUT2} = 70 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = +60°C

Internal Power Dissipation

$P_{LDO1} = (V_{IN(MAX)} - V_{OUT1(MIN)}) \times I_{OUT1}$

P_{LDO1} = ((20V x 1.05) – (12 x 0.98)) x 30 mA

P_{LDO1} = 0.27W

$P_{LDO2} = (V_{IN(MAX)} - V_{OUT2(MIN)}) \times I_{OUT2}$

P_{LDO2} = ((20V x 1.05) – (5.0V x 0.98)) x 70 mA

$P_{LDO(2)}$= 1.12W
P_{LDO} = P_{LDO1} + P_{LDO2}
P_{LDO} = 0.27 + 1.12
P_{LDO} = 1.39W

5.3.2 DEVICE JUNCTION TEMPERATURE RISE EXAMPLE

The internal junction temperature rise is a function of internal power dissipation and of the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient (θ_{JA}) is derived from EIA/JEDEC standards for measuring thermal resistance. The EIA/JEDEC specification is JESD51. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors such as copper area and thickness. Refer to Application Note AN792, *"A Method to Determine How Much Power a SOT23 Can Dissipate in an Application"* (DS00792), for more information regarding this subject.

EXAMPLE 5-1:

$T_{J(RISE)}$ = P_{TOTAL} x θ_{JA}
$T_{J(RISE)}$ = 1.39W x 53°C/W
$T_{J(RISE)}$ = 74°C

5.3.3 JUNCTION TEMPERATURE ESTIMATE EXAMPLE

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below:

EXAMPLE 5-2:

T_J = $T_{J(RISE)}$ + $T_{A(MAX)}$
T_J = 74°C + 60.0°C
T_J = 134°C

5.3.4 MAXIMUM PACKAGE POWER DISSIPATION AT +60°C AMBIENT TEMPERATURE EXAMPLE

EXAMPLE 5-3:

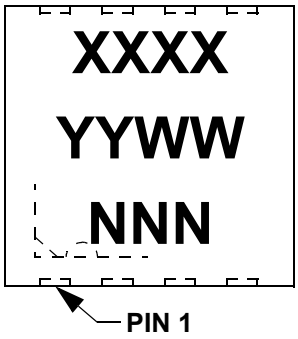
8 Lead SOIC (θ_{JA} = 53°C/W):
$P_{D(MAX)}$ = (150°C – 60°C)/53°C/W
$P_{D(MAX)}$ = 1.69W

NOTES:

6.0 PACKAGING INFORMATION

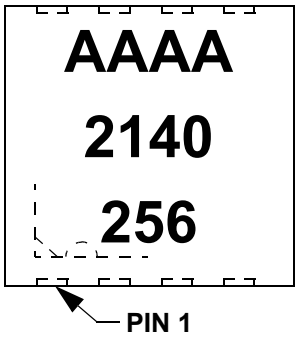
6.1 Package Marking Information

8-Lead VDFN (3x3 mm)

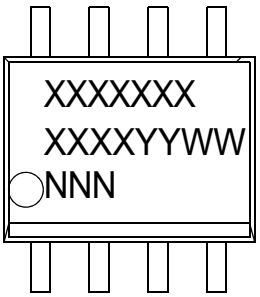


Part Number	Code
MCP1722-3310H/Q8B	AAAA
MCP1722T-3310H/Q8B	
MCP1722-3312H/Q8B	AAAB
MCP1722T-3312H/Q8B	
MCP1722-5010H/Q8B	AAAC
MCP1722T-5010H/Q8B	
MCP1722-5012H/Q8B	AAAD
MCP1722T-5012H/Q8B	

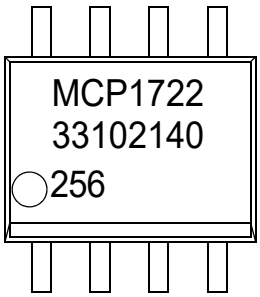
Example MCP1722



8-Lead SOIC (3.90 mm)



Example MCP1722

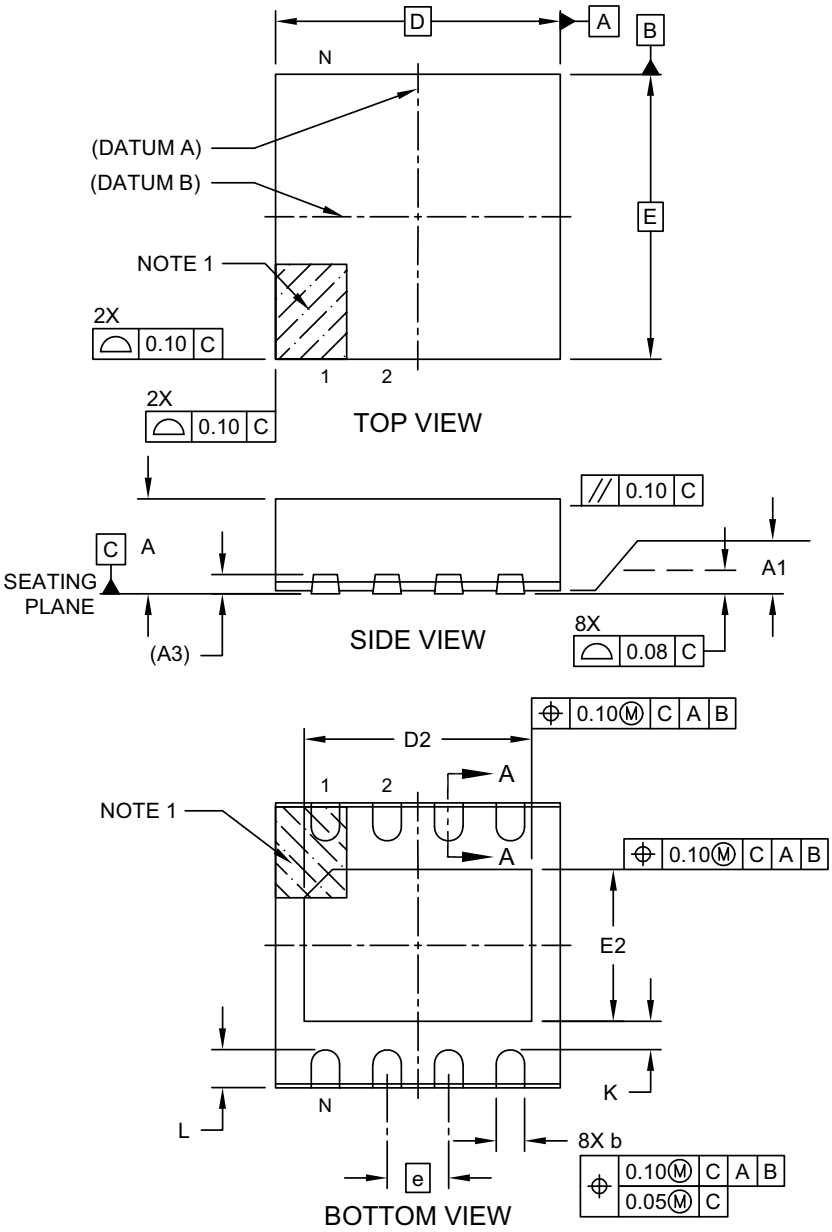


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3x1 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy YCL

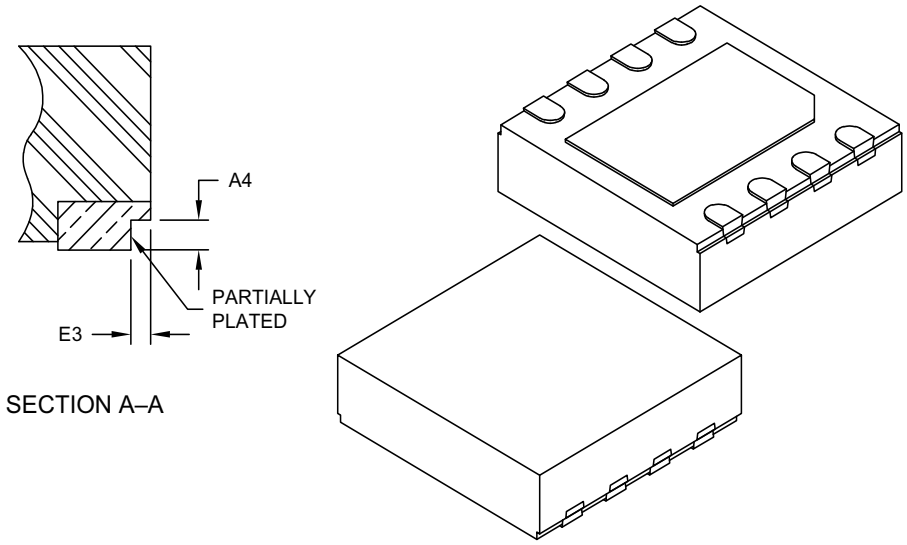
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21358 Rev D Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3x1 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy YCL

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.30	2.40	2.50
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Depth	A4	0.10	-	0.19
Wettable Flank Step Cut Width	E3	-	-	0.085

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

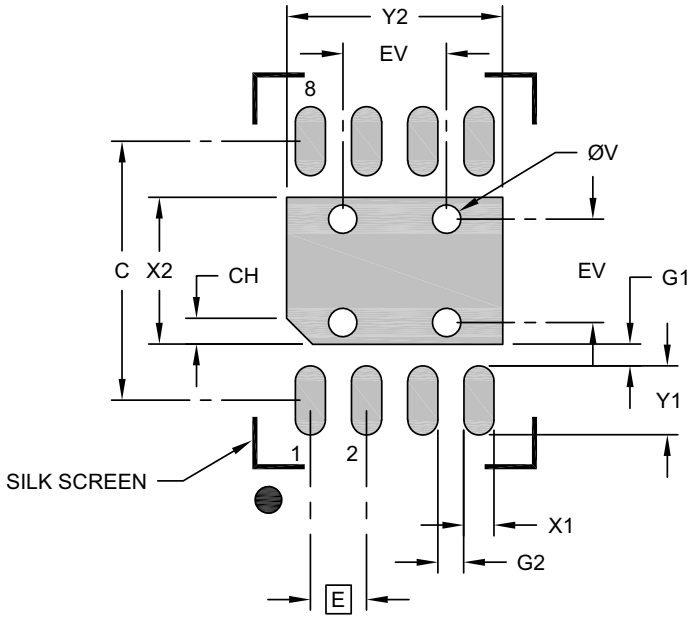
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21358 Rev D Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3x1 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			2.50
Contact Pad Spacing	C		3.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.20		
Pin 1 Index Chamfer	CH	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

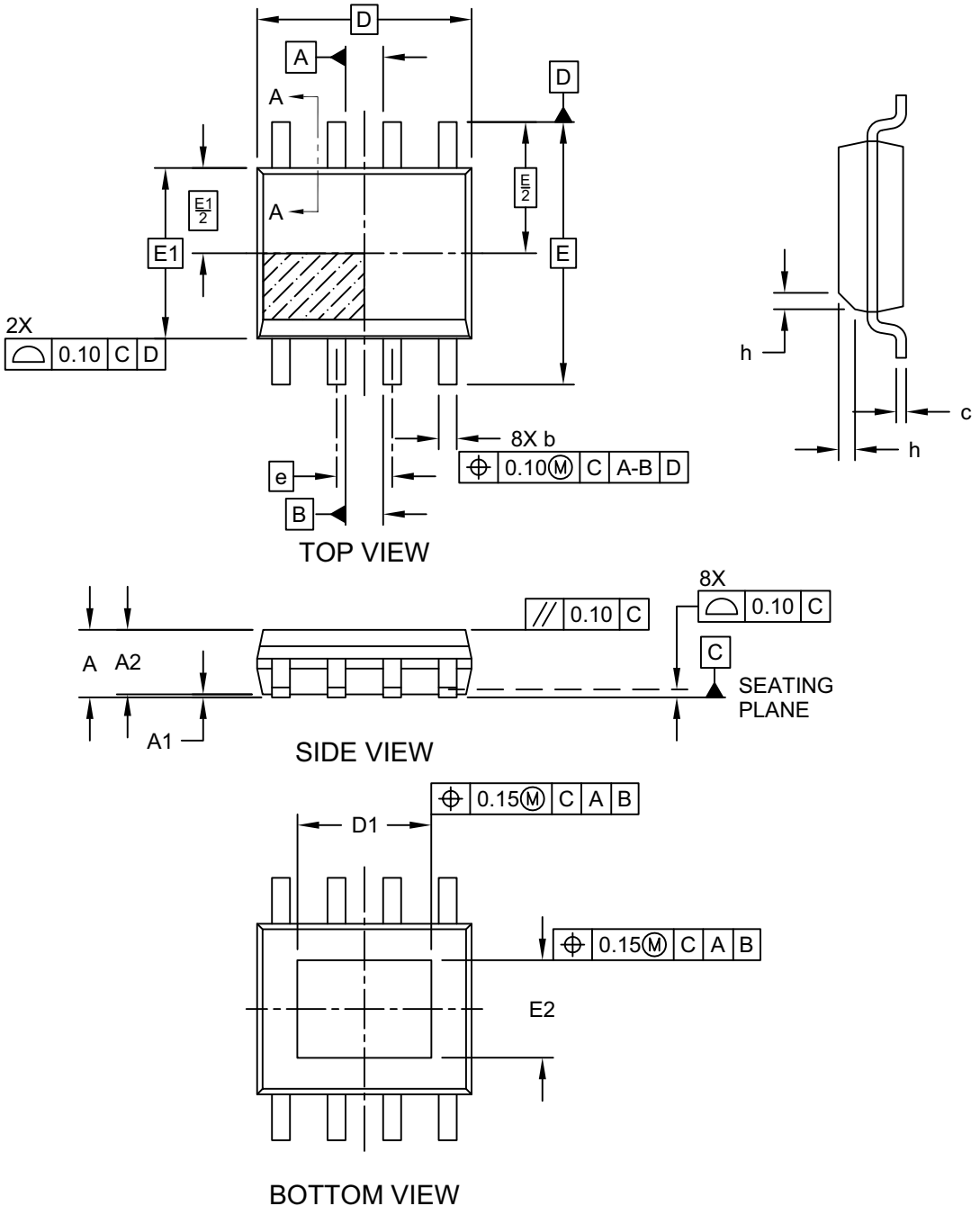
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23358 Rev D

8-Lead Thermally Enhanced Plastic Small Outline (SE) - Narrow, 3.90 mm Body [SOIC] With 2.2 x 3.0 mm Exposed Pad

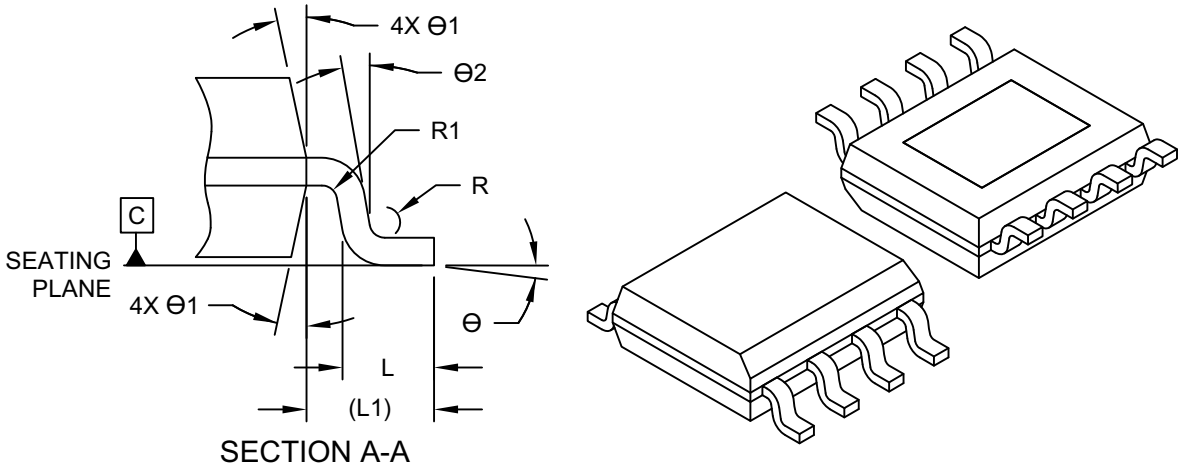
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-162 Rev C Sheet 1 of 2

8-Lead Thermally Enhanced Plastic Small Outline (SE) - Narrow, 3.90 mm Body [SOIC] With 2.2 x 3.0 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.00	-	0.15
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Exposed Pad Width	E2	2.05	2.23	2.41
Exposed Pad Length	D1	2.81	3.06	3.30
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Lead Bend Radius	R	0.07	-	-
Lead Bend Radius	R1	0.07	-	-
Foot Angle	Θ	0°	-	8°
Lead Angle	Θ2	0°	-	-
Mold Draft Angle Top and Bottom	Θ1	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

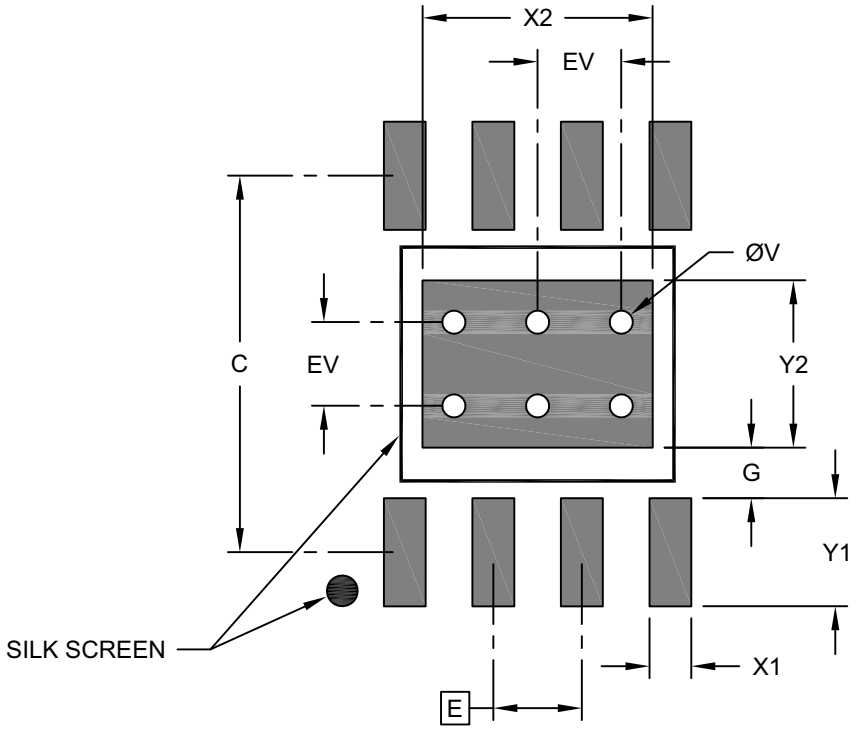
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-163 Rev C Sheet 2 of 2

8-Lead Thermally Enhanced Plastic Small Outline (SE) - Narrow, 3.90 mm Body [SOIC] With 2.2 x 3.0 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Center Pad Width	X2			3.30
Center Pad Length	Y2			2.40
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55
Contact Pad to Center Pad (X8)	G1	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2162 Rev C

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (June 2021)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, such as on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-3310/3312 -5010/5012	X	/XXX
Device	Tape and Reel Option	Voltage Output Option	Temperature Range	Package

Device:	MCP1722:	High Voltage LDO with Dual Output
	MCP1722T:	High Voltage LDO with Dual Output (Tape and Reel)
Tape and Reel Option:	T =	Tape and Reel(1)
Voltage Output Option	3310 =	Dual Output Voltage: 3.3V LDO_2 / 10V LDO_1
	3312 =	Dual Output Voltage: 3.3V LDO_2 / 12V LDO_1
	5010 =	Dual Output Voltage: 5.0V LDO_2 / 10V LDO_1
	5012 =	Dual Output Voltage: 5.0V LDO_2 / 12V LDO_1
Temperature Range:	H =	-40°C to +150°C (Extended)
Package:	Q8B =	Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks (Atmel Legacy YCL), 8-Lead
	S7X =	Thermally Enhanced Plastic Small Outline (SE) - Narrow, 3.90 mm Body [SOIC] With 2.2 x 3.0 mm Exposed Pad, 8-Lead

Examples:

a) MCP1722-3310H/Q8B: 3.3V and 10V Outputs, Extended Temperature, 8-Lead VDFN package

b) MCP1722-3312H/Q8B: 3.3V and 12V Outputs, Extended Temperature, 8-Lead VDFN package

c) MCP1722-5010H/Q8B: 5.0V and 10V Outputs, Extended Temperature, 8-Lead VDFN package

d) MCP1722-5012H/Q8B: 5.0V and 12V Outputs, Extended Temperature, 8-Lead VDFN package

e) MCP1722-3310H/S7X: 3.3V and 10V Outputs, Extended Temperature, 8-Lead SOIC package

f) MCP1722-3312H/S7X: 3.3V and 12V Outputs, Extended Temperature, 8-Lead SOIC package

g) MCP1722-5010H/S7X: 5.0V and 10V Outputs, Extended Temperature, 8-Lead SOIC package

h) MCP1722-5012H/S7X: 5.0V and 12V Outputs, Extended Temperature, 8-Lead SOIC package

i) MCP1722T-3310H/Q8B: Tape and Reel, 3.3V and 10V Outputs, Extended Temperature, 8-Lead VDFN package

j) MCP1722T-3312H/Q8B: Tape and Reel, 3.3V and 12V Outputs, Extended Temperature, 8-Lead VDFN package

k) MCP1722T-5010H/Q8B: Tape and Reel, 5.0V and 10V Outputs, Extended Temperature, 8-Lead VDFN package

l) MCP1722T-5012H/Q8B: Tape and Reel, 5.0V and 12V Outputs, Extended Temperature, 8-Lead VDFN package

m) MCP1722T-3310H/S7X: Tape and Reel, 3.3V and 10V Outputs, Extended Temperature, 8-Lead SOIC package

n) MCP1722T-3312H/S7X: Tape and Reel, 3.3V and 12V Outputs, Extended Temperature, 8-Lead SOIC package,

o) MCP1722T-5010H/S7X: Tape and Reel, 5.0V and 10V Outputs, Extended Temperature, 8-Lead SOIC package

p) MCP1722T-5012H/S7X: Tape and Reel, 5.0V and 12V Outputs, Extended Temperature, 8-Lead SOIC package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
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