MCP2517FD

External CAN FD Controller with SPI Interface

Features

General

- External CAN FD Controller with SPI Interface
- Arbitration Bit Rate up to 1 Mbps
- Data Bit Rate up to 8 Mbps
- CAN FD Controller modes
  - Mixed CAN 2.0B and CAN FD mode
  - CAN 2.0B mode
- Conforms to ISO 11898-1:2015

Message FIFOs

- 31 FIFOs, configurable as transmit or receive FIFOs
- One Transmit Queue (TXQ)
- Transmit Event FIFO (TEF) with 32 bit time stamp

Message Transmission

- Message transmission prioritization:
  - Based on priority bit field, and/or
  - Message with lowest ID gets transmitted first using the Transmit Queue (TXQ)
- Programmable automatic retransmission attempts: unlimited, 3 attempts or disabled

Message Reception

- 32 Flexible Filter and Mask Objects
- Each object can be configured to filter either:
  - Standard ID + first 18 data bits, or
  - Extended ID
- 32-bit Time Stamp

Special Features

- VDD: 2.7 to 5.5V
- Active current: max. 20 mA at 5.5 V, 40 MHz CAN clock
- Sleep current: 10 µA, typical
- Message objects are located in RAM: 2 KB
- Up to 3 configurable interrupt pins
- Bus Health Diagnostics and Error counters
- Transceiver standby control
- Start of frame pin for indicating the beginning of messages on the bus
- Temperature ranges:
  - High (H): –40°C to +150°C

Oscillator Options

- 40, 20 or 4 MHz crystal, or ceramic resonator; or external clock input
- Clock output with prescaler

SPI Interface

- Up to 20 MHz SPI clock speed
- Supports SPI modes 0,0 and 1,1
- Registers and bit fields are arranged in a way to enable efficient access via SPI

Safety Critical Systems

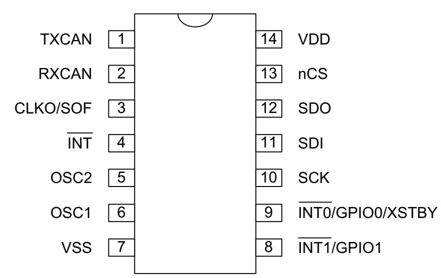
- SPI commands with CRC to detect noise on SPI interface
- Error Correction Code (ECC) protected RAM

Additional Features

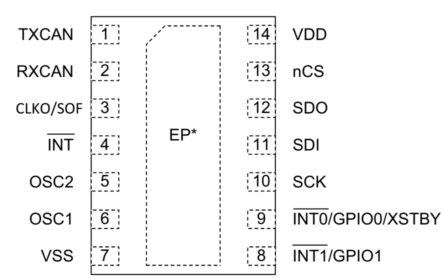
- GPIO pins: $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be configured as general purpose I/O
- Open drain outputs: TXCAN, $\overline{\text{INT}}$, $\overline{\text{INT0}}$, and $\overline{\text{INT1}}$ pins can be configured as push/pull or open drain outputs

Package Types

MCP2517FD
SOIC14



MCP2517FD
VDFN14 with wettable flanks*



*VDFN14 includes an Exposed Thermal Pad (EP); see Table 1-1

1.0 DEVICE OVERVIEW

The MCP2517FD is a cost-effective and small-footprint CAN FD controller that can be easily added to a microcontroller with an available SPI interface. Therefore, a CAN FD channel can be easily added to a microcontroller that is either lacking a CAN FD peripheral, or that doesn't have enough CAN FD channels.

The MCP2517FD supports both, CAN frames in the Classical format (CAN2.0B) and CAN Flexible Data Rate (CAN FD) format, as specified in ISO 11898-1:2015.

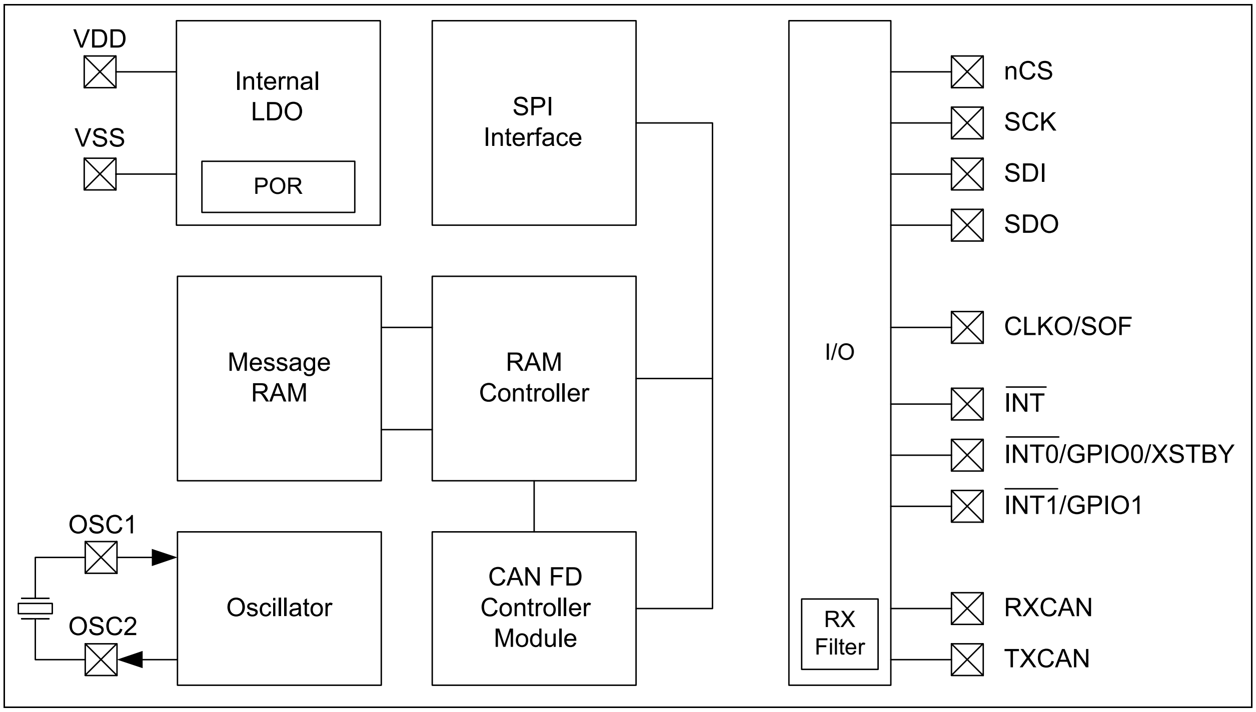
1.1 Block Diagram

Figure 1.1 shows the block diagram of the MCP2517FD. The MCP2517FD contains the following main blocks:

- The CAN FD Controller module implements the CAN FD protocol and contains the FIFOs, and Filters.
- The SPI interface is used to control the device by accessing SFRs and RAM.
- The RAM controller arbitrates the RAM accesses between the SPI and CAN FD Controller module.
- The Message RAM is used to store the data of the Message Objects.
- The oscillator generates the CAN clock.
- The Internal LDO and POR circuit.
- The I/O control.

Note 1:	This data sheet summarizes the features of the MCP2517FD. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "MCP25xxFD Family Reference Manual".

FIGURE 1-1: MCP2517FD BLOCK DIAGRAM



1.2 Pin Out Description

Table 1-1 describes the functions of the pins.

TABLE 1-1: MCP2517FD STANDARD PINOUT VERSION

Pin Name	SOIC	VDFN	Pin Type	Description
TXCAN	1	1	O	Transmit output to CAN FD transceiver
RXCAN	2	2	I	Receive input from CAN FD transceiver
CLKO/SOF	3	3	O	Clock output/Start of Frame output
$\overline{\text{INT}}$	4	4	O	Interrupt output (active low)
OSC2	5	5	O	External oscillator output
OSC1	6	6	I	External oscillator input
VSS	7	7	P	Ground
$\overline{\text{INT1}}$/GPIO1	8	8	I/O	RX Interrupt output (active low)/GPIO
$\overline{\text{INT0}}$/GPIO0/ XSTBY	9	9	I/O	TX Interrupt output (active low)/GPIO/ Transceiver Standby output
SCK	10	10	I	SPI clock input
SDI	11	11	I	SPI data input
SDO	12	12	O	SPI data output
nCS	13	13	I	SPI chip select input
VDD	14	14	P	Positive Supply
EP	-	15	P	Exposed Pad; connect to VSS

Legend: P = Power, I = Input, O = Output

1.3 Typical Application

Figure 1-2 shows an example of a typical application of the MCP2517FD. In this example, the microcontroller operates at 3.3V.

The MCP2517FD interfaces directly with microcontrollers operating at 2.7V to 5.5V. In addition, the MCP2517FD connects directly to high-speed CAN FD transceivers. There are no external level shifters required when connecting VDD of the MCP2517FD and the microcontroller to VIO of the transceiver.

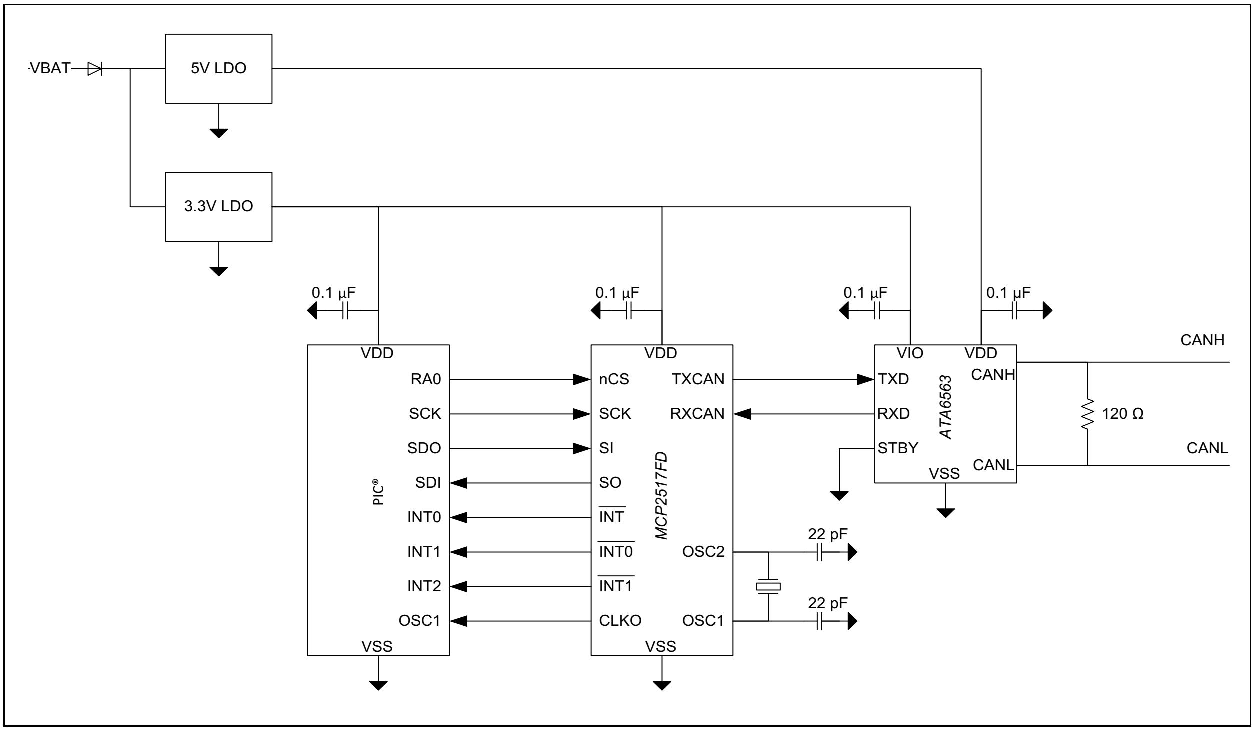
The VDD of the CAN FD transceiver is connected to 5V.

The SPI interface is used to configure and control the CAN FD controller.

The MCP2517FD signals interrupts to the microcontroller using $\overline{INT}$, $\overline{INT0}$ and $\overline{INT1}$. Interrupts need to be cleared by the microcontroller through SPI.

The CLKO pin provides the clock to the microcontroller.

FIGURE 1-2: MCP2517FD INTERFACING WITH A 3.3V MICROCONTROLLER



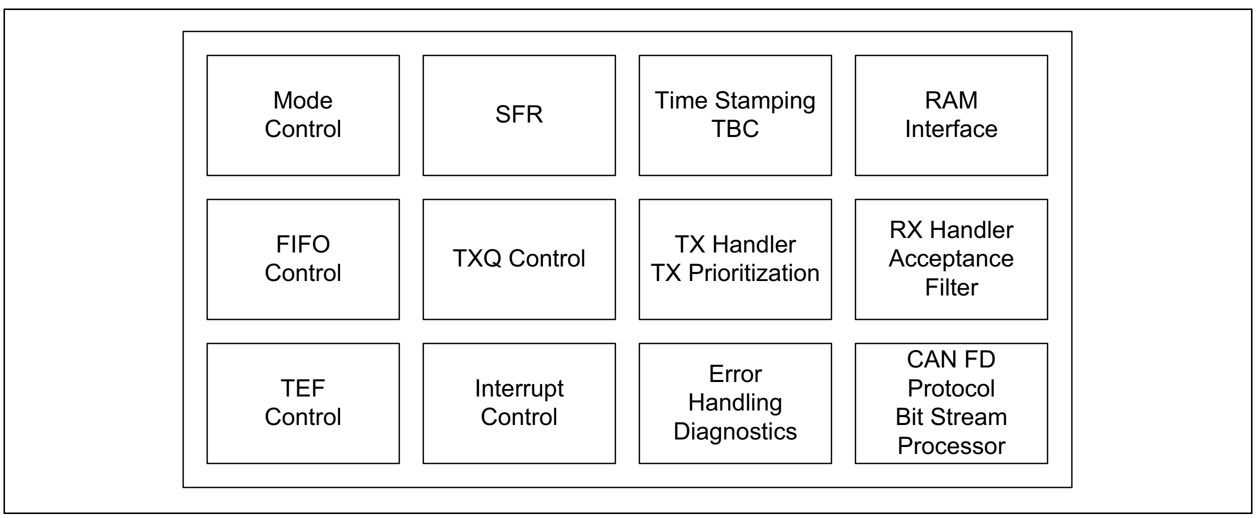
2.0 CAN FD CONTROLLER MODULE

Figure 2-1 shows the main blocks of the CAN FD Controller module:

- The CAN FD Controller module has multiple modes:
  - Configuration
  - Normal CAN FD
  - Normal CAN 2.0
  - Sleep
  - Listen Only
  - Restricted Operation
  - Internal and External Loop back modes
- The CAN FD Bit Stream Processor (BSP) implements the Medium Access Control of the CAN FD protocol described in ISO 11898-1:2015. It serializes and de-serializes the bit stream, encodes and decodes the CAN FD frames, manages the medium access, acknowledges frames, and detects and signals errors.
- The TX Handler prioritizes the messages that are requested for transmission by the Transmit FIFOs. It uses the RAM Interface to fetch the transmit data from RAM and provides it to the BSP for transmission.
- The BSP provides received messages to the RX Handler. The RX Handler uses the Acceptance Filter to filter out messages that shall be stored into Receive FIFOs. It uses the RAM Interface to store received data into RAM.
- Each FIFO can be configured either as a Transmit or Receive FIFO. The FIFO Control keeps track of the FIFO Head and Tail, and calculates the User Address. For a TX FIFO, the User Address points to the address in RAM where the data for the next transmit message shall be stored. For a RX FIFO, the User Address points to the address in RAM where the data of the next receive message shall be read. The User notifies the FIFO that a message was written to or read from RAM by incrementing the Head/Tail of the FIFO.
- The Transmit Queue (TXQ) is a special transmit FIFO that transmits the messages based on the ID of the messages stored in the queue.
- The Transmit Event FIFO (TEF) stores the message IDs of the transmitted messages.
- A free-running Time Base Counter is used to time stamp received messages. Messages in the TEF can also be time stamped.
- The CAN FD Controller module generates interrupts when new messages are received or when messages were transmitted successfully.
- The Special Function Registers (SFR) are used to control and to read the status of the CAN FD Controller module.

Note 1:	This data sheet summarizes the features of the CAN FD Controller module. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "MCP25xxFD Family Reference Manual".

FIGURE 2-1: CAN FD CONTROLLER MODULE BLOCK DIAGRAM



NOTES:

3.0 MEMORY ORGANIZATION

Figure 3-1 illustrates the main sections of the memory and its address ranges:

- MCP2517FD Special Function Registers (SFR)
- CAN FD Controller Module SFR
- Message Memory (RAM)

The SFR are 32 bit wide. The LSB is located at the lower address, e.g., the LSB of C1CON is located at address 0x000, while its MSB is located at address 0x003.

Table 3-1 lists the MCP2517FD specific registers. The first column contains the address of the SFR.

Table 3-2 lists the registers of the CAN FD Controller Module. The first column contains the address of the SFR.

FIGURE 3-1: MEMORY MAP

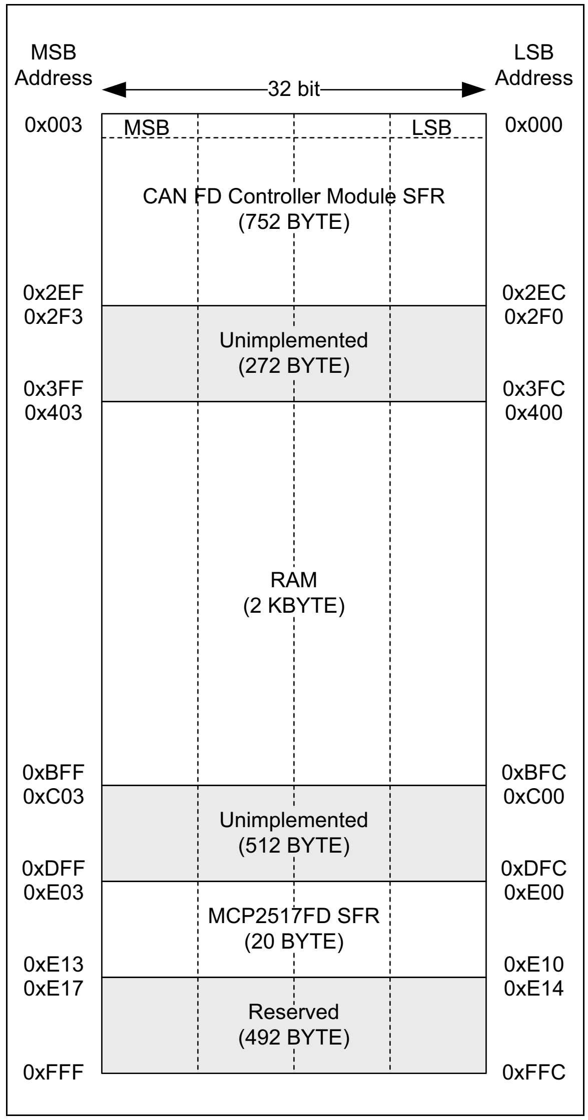


TABLE 3-1: MCP2517FD REGISTER SUMMARY

Address	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
E03	OSC	31:24	—	—	—	—	—	—	—	—
E02		23:16	—	—	—	—	—	—	—	—
E01		15:8	—	—	—	SCLKRDY	—	OSCRDY	—	PLLRDY
E00[1]		7:0	—	CLKODIV<1:0>		SCLKDIV	—	OSCDIS	—	PLLEN
	IOCON	31:24	—	INTOD	SOF	TXCANOD	—	—	PM1	PM0
		23:16	—	—	—	—	—	—	GPIO1	GPIO0
		15:8	—	—	—	—	—	—	LAT1	LAT0
E04		7:0	—	XSTBYEN	—	—	—	—	TRIS1	TRIS0
	CRC	31:24	—	—	—	—	—	—	FERRIE	CRCERRIE
		23:16	—	—	—	—	—	—	FERRIF	CRCERRIF
		15:8	CRC<15:8>							
E08		7:0	CRC<7:0>							
	ECCCON	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	—	PARITY<6:0>						
E0C		7:0	—	—	—	—	—	DEDIE	SECIE	ECCEN
	ECCSTAT	31:24	—	—	—	—	ERRADDR<11:8>			
		23:16	ERRADDR<7:0>							
		15:8	—	—	—	—	—	—	—	—
E10		7:0	—	—	—	—	—	DEDIF	SECIF	—

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
03	C1CON	31:24	TXBWS<3:0>				ABAT	REQOP<2:0>		
02		23:16	OPMOD<2:0>			TXQEN	STEF	SERR2LOM	ESIGM	RTXAT
01		15:8	—	—	—	BRSDIS	BUSY	WFT<1:0>		WAKFIL
00[1]		7:0	—	PXEDIS	ISOCRCEN	DNCNT<4:0>				
	C1NBTCFG	31:24	BRP<7:0>							
		23:16	TSEG1<7:0>							
		15:8	—	TSEG2<6:0>						
04		7:0	—	SJW<6:0>						
	C1DBTCFG	31:24	BRP<7:0>							
		23:16	—	—	—	TSEG1<4:0>				
		15:8	—	—	—	—	TSEG2<3:0>			
08		7:0	—	—	—	—	SJW<3:0>			
	C1TDC	31:24	—	—	—	—	—	—	EDGFLTEN	SID11EN
		23:16	—	—	—	—	—	—	TDCMOD<1:0>	
		15:8	—	TDCO<6:0>						
0C		7:0	—	—	TDCV<5:0>					
	C1TBC	31:24	TBC<31:24>							
		23:16	TBC<23:16>							
		15:8	TBC<15:8>							
10		7:0	TBC<7:0>							
	C1TSCON	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	TSRES	TSEOF	TBCEN
		15:8	—	—	—	—	—	—	TBCPRE<9:8>	
14		7:0	TBCPRE<7:0>							
	C1VEC	31:24	—	RXCODE<6:0>						
		23:16	—	TXCODE<6:0>						
		15:8	—	—	—	FILHIT<4:0>				
18		7:0	—	ICODE<6:0>						
	C1INT	31:24	IVMIE	WAKIE	CERRIE	SERRIE	RXOVIE	TXATIE	SPICRCIE	ECCIE
		23:16	—	—	—	TEFIE	MODIE	TBCIE	RXIE	TXIE
		15:8	IVMIF	WAKIF	CERRIF	SERRIF	RXOVIF	TXATIF	SPICRCIF	ECCIF
1C		7:0	—	—	—	TEFIF	MODIF	TBCIF	RXIF	TXIF
	C1RXIF	31:24	RFIF<31:24>							
		23:16	RFIF<23:16>							
		15:8	RFIF<15:8>							
20		7:0	RFIF<7:1>							—
	C1TXIF	31:24	TFIF<31:24>							
		23:16	TFIF<23:16>							
		15:8	TFIF<15:8>							
24		7:0	TFIF<7:0>							
	C1RXOVIF	31:24	RFOVIF<31:24>							
		23:16	RFOVIF<23:16>							
		15:8	RFOVIF<15:8>							
28		7:0	RFOVIF<7:1>							—
	C1TXATIF	31:24	TFATIF<31:24>							
		23:16	TFATIF<23:16>							
		15:8	TFATIF<15:8>							
2C		7:0	TFATIF<7:0>							

Note 1: The lower order byte of the 32-bit register resides at the low-order address.
2: Reserved register reads 0.

TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	C1TXREQ	31:24	TXREQ<31:24>							
		23:16	TXREQ<23:16>							
		15:8	TXREQ<15:8>							
30		7:0	TXREQ<7:0>							
	C1TREC	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
		15:8	TEC<7:0>							
34		7:0	REC<7:0>							
	C1BDIAG0	31:24	DTERRCNT<7:0>							
		23:16	DRERRCNT<7:0>							
		15:8	NTERRCNT<7:0>							
38		7:0	NRERRCNT<7:0>							
	C1BDIAG1	31:24	DLCMM	ESI	DCRCERR	DSTUFERR	DFORMERR	—	DBIT1ERR	DBIT0ERR
		23:16	TXBOERR	—	NCRCERR	NSTUFERR	NFORMERR	NACKERR	NBIT1ERR	NBIT0ERR
		15:8	EFMSGCNT<15:8>							
3C		7:0	EFMSGCNT<7:0>							
	C1TEFCON	31:24	—	—	—	FSIZE<4:0>				
		23:16	—	—	—	—	—	—	—	—
		15:8	—	—	—	—	—	FRESET	—	UINC
40		7:0	—	—	TEFTSEN	—	TEFOVIE	TEFFIE	TEFHIE	TEFNEIE
	C1TEFSTA	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	—	—	—	—	—	—	—	—
44		7:0	—	—	—	—	TEFOVIF	TEFFIF	TEFHIF	TEFNEIF
	C1TEFUA	31:24	TEFUA<31:24>							
		23:16	TEFUA<23:16>							
		15:8	TEFUA<15:8>							
48		7:0	TEFUA<7:0>							
	Reserved(2)	31:24	Reserved<31:24>							
		23:16	Reserved<23:16>							
		15:8	Reserved<15:8>							
4C		7:0	Reserved<7:0>							
	C1TXQCON	31:24	PLSIZE<2:0>			FSIZE<4:0>				
		23:16	—	TXAT<1:0>		TXPRI<4:0>				
		15:8	—	—	—	—	—	FRESET	TXREQ	UINC
50		7:0	TXEN	—	—	TXATIE	—	TXQEIE	—	TXQNIE
	C1TXQSTA	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	—	—	—	TXQCI<4:0>				
54		7:0	TXABT	TXLARB	TXERR	TXATIF	—	TXQEIF	—	TXQNIF
	C1TXQUA	31:24	TXQUA<31:24>							
		23:16	TXQUA<23:16>							
		15:8	TXQUA<15:8>							
58		7:0	TXQUA<7:0>							

Note 1: The lower order byte of the 32-bit register resides at the low-order address.
2: Reserved register reads 0.

TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	C1FIFOCON1	31:24	PLSIZE<2:0>			FSIZE<4:0>				
		23:16	—	TXAT<1:0>		TXPRI<4:0>				
		15:8	—	—	—	—	—	FRESET	TXREQ	UINC
5C		7:0	TXEN	RTREN	RXTSEN	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
	C1FIFOSTA1	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	—	—	—	FIFOCI<4:0>				
60		7:0	TXABT	TXLARB	TXERR	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
	C1FIFOUA1	31:24	FIFOUA<31:24>							
		23:16	FIFOUA<23:16>							
		15:8	FIFOUA<15:8>							
64		7:0	FIFOUA<7:0>							
68	C1FIFOCON2	31:0	same as C1FIFOCON1							
6C	C1FIFOSTA2	31:0	same as C1FIFOSTA1							
70	C1FIFOUA2	31:0	same as C1FIFOUA1							
74	C1FIFOCON3	31:0	same as C1FIFOCON1							
78	C1FIFOSTA3	31:0	same as C1FIFOSTA1							
7C	C1FIFOUA3	31:0	same as C1FIFOUA1							
80	C1FIFOCON4	31:0	same as C1FIFOCON1							
84	C1FIFOSTA4	31:0	same as C1FIFOSTA1							
88	C1FIFOUA4	31:0	same as C1FIFOUA1							
8C	C1FIFOCON5	31:0	same as C1FIFOCON1							
90	C1FIFOSTA5	31:0	same as C1FIFOSTA1							
94	C1FIFOUA5	31:0	same as C1FIFOUA1							
98	C1FIFOCON6	31:0	same as C1FIFOCON1							
9C	C1FIFOSTA6	31:0	same as C1FIFOSTA1							
A0	C1FIFOUA6	31:0	same as C1FIFOUA1							
A4	C1FIFOCON7	31:0	same as C1FIFOCON1							
A8	C1FIFOSTA7	31:0	same as C1FIFOSTA1							
AC	C1FIFOUA7	31:0	same as C1FIFOUA1							
B0	C1FIFOCON8	31:0	same as C1FIFOCON1							
B4	C1FIFOSTA8	31:0	same as C1FIFOSTA1							
B8	C1FIFOUA8	31:0	same as C1FIFOUA1							
BC	C1FIFOCON9	31:0	same as C1FIFOCON1							
C0	C1FIFOSTA9	31:0	same as C1FIFOSTA1							
C4	C1FIFOUA9	31:0	same as C1FIFOUA1							
C8	C1FIFOCON10	31:0	same as C1FIFOCON1							
CC	C1FIFOSTA10	31:0	same as C1FIFOSTA1							
D0	C1FIFOUA10	31:0	same as C1FIFOUA1							
D4	C1FIFOCON11	31:0	same as C1FIFOCON1							
D8	C1FIFOSTA11	31:0	same as C1FIFOSTA1							
DC	C1FIFOUA11	31:0	same as C1FIFOUA1							
E0	C1FIFOCON12	31:0	same as C1FIFOCON1							
E4	C1FIFOSTA12	31:0	same as C1FIFOSTA1							
E8	C1FIFOUA12	31:0	same as C1FIFOUA1							
EC	C1FIFOCON13	31:0	same as C1FIFOCON1							
F0	C1FIFOSTA13	31:0	same as C1FIFOSTA1							
F4	C1FIFOUA13	31:0	same as C1FIFOUA1							
F8	C1FIFOCON14	31:0	same as C1FIFOCON1							
FC	C1FIFOSTA14	31:0	same as C1FIFOSTA1							
100	C1FIFOUA14	31:0	same as C1FIFOUA1							

Note 1: The lower order byte of the 32-bit register resides at the low-order address.
2: Reserved register reads 0.

TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
104	C1FIFOCON15	31:0	same as C1FIFOCON1							
108	C1FIFOSTA15	31:0	same as C1FIFOSTA1							
10C	C1FIFOUA15	31:0	same as C1FIFOUA1							
110	C1FIFOCON16	31:0	same as C1FIFOCON1							
114	C1FIFOSTA16	31:0	same as C1FIFOSTA1							
118	C1FIFOUA16	31:0	same as C1FIFOUA1							
11C	C1FIFOCON17	31:0	same as C1FIFOCON1							
120	C1FIFOSTA17	31:0	same as C1FIFOSTA1							
124	C1FIFOUA17	31:0	same as C1FIFOUA1							
128	C1FIFOCON18	31:0	same as C1FIFOCON1							
12C	C1FIFOSTA18	31:0	same as C1FIFOSTA1							
130	C1FIFOUA18	31:0	same as C1FIFOUA1							
134	C1FIFOCON19	31:0	same as C1FIFOCON1							
138	C1FIFOSTA19	31:0	same as C1FIFOSTA1							
13C	C1FIFOUA19	31:0	same as C1FIFOUA1							
140	C1FIFOCON20	31:0	same as C1FIFOCON1							
144	C1FIFOSTA20	31:0	same as C1FIFOSTA1							
148	C1FIFOUA20	31:0	same as C1FIFOUA1							
14C	C1FIFOCON21	31:0	same as C1FIFOCON1							
150	C1FIFOSTA21	31:0	same as C1FIFOSTA1							
154	C1FIFOUA21	31:0	same as C1FIFOUA1							
158	C1FIFOCON22	31:0	same as C1FIFOCON1							
15C	C1FIFOSTA22	31:0	same as C1FIFOSTA1							
160	C1FIFOUA22	31:0	same as C1FIFOUA1							
164	C1FIFOCON23	31:0	same as C1FIFOCON1							
168	C1FIFOSTA23	31:0	same as C1FIFOSTA1							
16C	C1FIFOUA23	31:0	same as C1FIFOUA1							
170	C1FIFOCON24	31:0	same as C1FIFOCON1							
174	C1FIFOSTA24	31:0	same as C1FIFOSTA1							
178	C1FIFOUA24	31:0	same as C1FIFOUA1							
17C	C1FIFOCON25	31:0	same as C1FIFOCON1							
180	C1FIFOSTA25	31:0	same as C1FIFOSTA1							
184	C1FIFOUA25	31:0	same as C1FIFOUA1							
188	C1FIFOCON26	31:0	same as C1FIFOCON1							
18C	C1FIFOSTA26	31:0	same as C1FIFOSTA1							
190	C1FIFOUA26	31:0	same as C1FIFOUA1							
194	C1FIFOCON27	31:0	same as C1FIFOCON1							
198	C1FIFOSTA27	31:0	same as C1FIFOSTA1							
19C	C1FIFOUA27	31:0	same as C1FIFOUA1							
1A0	C1FIFOCON28	31:0	same as C1FIFOCON1							
1A4	C1FIFOSTA28	31:0	same as C1FIFOSTA1							
1A8	C1FIFOUA28	31:0	same as C1FIFOUA1							
1AC	C1FIFOCON29	31:0	same as C1FIFOCON1							
1B0	C1FIFOSTA29	31:0	same as C1FIFOSTA1							
1B4	C1FIFOUA29	31:0	same as C1FIFOUA1							
1B8	C1FIFOCON30	31:0	same as C1FIFOCON1							
1BC	C1FIFOSTA30	31:0	same as C1FIFOSTA1							
1C0	C1FIFOUA30	31:0	same as C1FIFOUA1							
1C4	C1FIFOCON31	31:0	same as C1FIFOCON1							
1C8	C1FIFOSTA31	31:0	same as C1FIFOSTA1							
1CC	C1FIFOUA31	31:0	same as C1FIFOUA1							

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

2: Reserved register reads 0.

TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
1D0	C1FLTCON0	31:24	FLTEN3	—	—	F3BP<4:0>				
		23:16	FLTEN2	—	—	F2BP<4:0>				
		15:8	FLTEN1	—	—	F1BP<4:0>				
		7:0	FLTEN0	—	—	F0BP<4:0>				
1D4	C1FLTCON1	31:24	FLTEN7	—	—	F7BP<4:0>				
		23:16	FLTEN6	—	—	F6BP<4:0>				
		15:8	FLTEN5	—	—	F5BP<4:0>				
		7:0	FLTEN4	—	—	F4BP<4:0>				
1D8	C1FLTCON2	31:24	FLTEN11	—	—	F11BP<4:0>				
		23:16	FLTEN10	—	—	F10BP<4:0>				
		15:8	FLTEN9	—	—	F9BP<4:0>				
		7:0	FLTEN8	—	—	F8BP<4:0>				
1DC	C1FLTCON3	31:24	FLTEN15	—	—	F15BP<4:0>				
		23:16	FLTEN14	—	—	F14BP<4:0>				
		15:8	FLTEN13	—	—	F13BP<4:0>				
		7:0	FLTEN12	—	—	F12BP<4:0>				
1E0	C1FLTCON4	31:24	FLTEN19	—	—	F19BP<4:0>				
		23:16	FLTEN18	—	—	F18BP<4:0>				
		15:8	FLTEN17	—	—	F17BP<4:0>				
		7:0	FLTEN16	—	—	F16BP<4:0>				
1E4	C1FLTCON5	31:24	FLTEN23	—	—	F23BP<4:0>				
		23:16	FLTEN22	—	—	F22BP<4:0>				
		15:8	FLTEN21	—	—	F21BP<4:0>				
		7:0	FLTEN20	—	—	F20BP<4:0>				
1E8	C1FLTCON6	31:24	FLTEN27	—	—	F27BP<4:0>				
		23:16	FLTEN26	—	—	F26BP<4:0>				
		15:8	FLTEN25	—	—	F25BP<4:0>				
		7:0	FLTEN24	—	—	F24BP<4:0>				
1EC	C1FLTCON7	31:24	FLTEN31	—	—	F31BP<4:0>				
		23:16	FLTEN30	—	—	F30BP<4:0>				
		15:8	FLTEN29	—	—	F29BP<4:0>				
		7:0	FLTEN28	—	—	F28BP<4:0>				
1F0	C1FLTOBJ0	31:24	—	EXIDE	SID11	EID<17:6>				
		23:16	EID<12:5>							
		15:8	EID<4:0>					SID<10:8>		
		7:0	SID<7:0>							
1F4	C1MASK0	31:24	—	MIDE	MSID11	MEID<17:6>				
		23:16	MEID<12:5>							
		15:8	MEID<4:0>					MSID<10:8>		
		7:0	MSID<7:0>							
1F8	C1FLTOBJ1	31:0	same as C1FLTOBJ0							
1FC	C1MASK1	31:0	same as C1MASK0							
200	C1FLTOBJ2	31:0	same as C1FLTOBJ0							
204	C1MASK2	31:0	same as C1MASK0							
208	C1FLTOBJ3	31:0	same as C1FLTOBJ0							
20C	C1MASK3	31:0	same as C1MASK0							
210	C1FLTOBJ4	31:0	same as C1FLTOBJ0							
214	C1MASK4	31:0	same as C1MASK0							
218	C1FLTOBJ5	31:0	same as C1FLTOBJ0							
21C	C1MASK5	31:0	same as C1MASK0							

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

2: Reserved register reads 0.

TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
220	C1FLTOBJ6	31:0	same as C1FLTOBJ0							
224	C1MASK6	31:0	same as C1MASK0							
228	C1FLTOBJ7	31:0	same as C1FLTOBJ0							
22C	C1MASK7	31:0	same as C1MASK0							
230	C1FLTOBJ8	31:0	same as C1FLTOBJ0							
234	C1MASK8	31:0	same as C1MASK0							
238	C1FLTOBJ9	31:0	same as C1FLTOBJ0							
23C	C1MASK9	31:0	same as C1MASK0							
240	C1FLTOBJ10	31:0	same as C1FLTOBJ0							
244	C1MASK10	31:0	same as C1MASK0							
248	C1FLTOBJ11	31:0	same as C1FLTOBJ0							
24C	C1MASK11	31:0	same as C1MASK0							
250	C1FLTOBJ12	31:0	same as C1FLTOBJ0							
254	C1MASK12	31:0	same as C1MASK0							
258	C1FLTOBJ13	31:0	same as C1FLTOBJ0							
25C	C1MASK13	31:0	same as C1MASK0							
260	C1FLTOBJ14	31:0	same as C1FLTOBJ0							
264	C1MASK14	31:0	same as C1MASK0							
268	C1FLTOBJ15	31:0	same as C1FLTOBJ0							
26C	C1MASK15	31:0	same as C1MASK0							
270	C1FLTOBJ16	31:0	same as C1FLTOBJ0							
274	C1MASK16	31:0	same as C1MASK0							
278	C1FLTOBJ17	31:0	same as C1FLTOBJ0							
27C	C1MASK17	31:0	same as C1MASK0							
280	C1FLTOBJ18	31:0	same as C1FLTOBJ0							
284	C1MASK18	31:0	same as C1MASK0							
288	C1FLTOBJ19	31:0	same as C1FLTOBJ0							
28C	C1MASK19	31:0	same as C1MASK0							
290	C1FLTOBJ20	31:0	same as C1FLTOBJ0							
294	C1MASK20	31:0	same as C1MASK0							
298	C1FLTOBJ21	31:0	same as C1FLTOBJ0							
29C	C1MASK21	31:0	same as C1MASK0							
2A0	C1FLTOBJ22	31:0	same as C1FLTOBJ0							
2A4	C1MASK22	31:0	same as C1MASK0							
2A8	C1FLTOBJ23	31:0	same as C1FLTOBJ0							
2AC	C1MASK23	31:0	same as C1MASK0							
2B0	C1FLTOBJ24	31:0	same as C1FLTOBJ0							
2B4	C1MASK24	31:0	same as C1MASK0							
2B8	C1FLTOBJ25	31:0	same as C1FLTOBJ0							
2BC	C1MASK25	31:0	same as C1MASK0							
2C0	C1FLTOBJ26	31:0	same as C1FLTOBJ0							
2C4	C1MASK26	31:0	same as C1MASK0							
2C8	C1FLTOBJ27	31:0	same as C1FLTOBJ0							
2CC	C1MASK27	31:0	same as C1MASK0							
2D0	C1FLTOBJ28	31:0	same as C1FLTOBJ0							
2D4	C1MASK28	31:0	same as C1MASK0							
2D8	C1FLTOBJ29	31:0	same as C1FLTOBJ0							
2DC	C1MASK29	31:0	same as C1MASK0							
2E0	C1FLTOBJ30	31:0	same as C1FLTOBJ0							
2E4	C1MASK30	31:0	same as C1MASK0							
2E8	C1FLTOBJ31	31:0	same as C1FLTOBJ0							
2EC	C1MASK31	31:0	same as C1MASK0							

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

2: Reserved register reads 0.

3.1 MCP2517FD Specific Registers

- Register 3-1: OSC
- Register 3-2: IOCON
- Register 3-3: CRC
- Register 3-4: ECCCON
- Register 3-5: ECCSTAT

TABLE 3-3: REGISTER LEGEND

Symbol	Description	Symbol	Description
R	Readable bit	HC	Cleared by Hardware only
W	Writable bit	HS	Set by Hardware only
U	Unimplemented bit, read as ‘0’	1	Bit is set at Reset
S	Settable bit	0	Bit is cleared at Reset
C	Clearable bit	x	Bit is unknown at Reset

EXAMPLE 3-1:

R/W - 0 indicates the bit is both readable and writable, and reads ‘0’ after a Reset.

REGISTER 3-1: OSC – MCP2517FD OSCILLATOR CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	R-0	U-0	R-0	U-0	R-0
—	—	—	SCLKRDY	—	OSCRDY	—	PLLRDY
bit 15							bit 8

U-0	R/W-1	R/W-1	R/W-0	U-0	HS/C-0	U-0	R/W-0
—	CLKODIV<1:0>		SCLKDIV(1)	—	OSCDIS(2)	—	PLLEN(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12 **SCLKRDY:** Synchronized SCLKDIV bit
1 = SCLKDIV 1
0 = SCLKDIV 0

bit 11 **Unimplemented:** Read as ‘0’

bit 10 **OSCRDY:** Clock Ready
1 = Clock is running and stable
0 = Clock not ready or off

bit 9 **Unimplemented:** Read as ‘0’

bit 8 **PLLRDY:** PLL Ready
1 = PLL Locked
0 = PLL not ready

bit 7 **Unimplemented:** Read as ‘0’

bit 6-5 **CLKODIV<1:0>:** Clock Output Divisor
11 =CLKO is divided by 10
10 =CLKO is divided by 4
01 =CLKO is divided by 2
00 =CLKO is divided by 1

bit 4 **SCLKDIV:** System Clock Divisor(1)
1 = SCLK is divided by 2
0 = SCLK is divided by 1

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **OSCDIS:** Clock (Oscillator) Disable(2)
1 = Clock disabled, the device is in Sleep mode.
0 = Enable Clock

Note 1: This bit can only be modified in Configuration mode.
2: Clearing OSCDIS while in Sleep mode will wake-up the device and put it back in Configuration mode.

REGISTER 3-1: OSC – MCP2517FD OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 1	**Unimplemented:** Read as '0'
bit 0	**PLLEN:** PLL Enable(1) 1 = System Clock from 10x PLL 0 = System Clock comes directly from XTAL oscillator

Note 1: This bit can only be modified in Configuration mode.

2: Clearing OSCDIS while in Sleep mode will wake-up the device and put it back in Configuration mode.

REGISTER 3-2: IOCON – INPUT/OUTPUT CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-1	R/W-1
—	INTOD	SOF	TXCANOD	—	—	PM1	PM0
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x
—	—	—	—	—	—	GPIO1	GPIO0
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x
—	—	—	—	—	—	LAT1	LAT0
bit 15							bit 8

U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1
—	XSTBYEN	—	—	—	—	TRIS1[1]	TRIS0[1]
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as ‘0’

bit 30 **INTOD:** Interrupt pins Open Drain Mode
1 = Open Drain Output
0 = Push/Pull Output

bit 29 **SOF:** Start-Of-Frame signal
1 = SOF signal on CLKO pin
0 = Clock on CLKO pin

bit 28 **TXCANOD:** TXCAN Open Drain Mode
1 = Open Drain Output
0 = Push/Pull Output

bit 27-26 **Unimplemented:** Read as ‘0’

bit 25 **PM1:** GPIO Pin Mode
1 = Pin is used as GPIO1
0 = Interrupt Pin $\overline{INT1}$, asserted when CiINT.RXIF and RXIE are set

bit 24 **PM0:** GPIO Pin Mode
1 = Pin is used as GPIO0
0 = Interrupt Pin $\overline{INT0}$, asserted when CiINT.TXIF and TXIE are set

bit 23-18 **Unimplemented:** Read as ‘0’

bit 17 **GPIO1:** GPIO1 Status
1 = $V_{GPIO1} > V_{IH}$
0 = $V_{GPIO1} < V_{IL}$

bit 16 **GPIO0:** GPIO0 Status
1 = $V_{GPIO0} > V_{IH}$
0 = $V_{GPIO0} < V_{IL}$

bit 15-10 **Unimplemented:** Read as ‘0’

Note 1: If PMx = 0, TRISx will be ignored and the pin will be an output.

REGISTER 3-2: IOCON – INPUT/OUTPUT CONTROL REGISTER (CONTINUED)

bit 9	**LAT1:** GPIO1 Latch 1 = Drive Pin High 0 = Drive Pin Low
bit 8	**LAT0:** GPIO0 Latch 1 = Drive Pin High 0 = Drive Pin Low
bit 7	**Unimplemented:** Read as '0'
bit 6	**XSTBYEN:** Enable Transceiver Standby Pin Control 1 = XSTBY control enabled 0 = XSTBY control disabled
bit 5-2	**Unimplemented:** Read as '0'
bit 1	**TRIS1:** GPIO1 Data Direction(1) 1 = Input Pin 0 = Output Pin
bit 0	**TRIS0:** GPIO0 Data Direction(1) 1 = Input Pin 0 = Output Pin

Note 1: If PMx = 0, TRISx will be ignored and the pin will be an output.

REGISTER 3-3: CRC – CRC REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	FERRIE	CRCERRIE
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	HS/C-0	HS/C-0
—	—	—	—	—	—	FERRIF	CRCERRIF
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CRC<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CRC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25 **FERRIE:** CRC Command Format Error Interrupt Enable

bit 24 **CRCERRIE:** CRC Error Interrupt Enable

bit 23-18 **Unimplemented:** Read as ‘0’

bit 17 **FERRIF:** CRC Command Format Error Interrupt Flag
1 = Number of Bytes mismatch during “SPI with CRC” command occurred
0 = No SPI CRC command format error occurred

bit 16 **CRCERRIF:** CRC Error Interrupt Flag
1 = CRC mismatch occurred
0 = No CRC error has occurred

bit 15-0 **CRC<15:0>:** Cycle Redundancy Check from last CRC mismatch

REGISTER 3-4: ECCCON – ECC CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PARITY<6:0>						
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	DEDIE	SECIE	ECCEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as ‘0’

bit 14-8 **PARITY<6:0>:** Parity bits used during write to RAM when ECC is disabled

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2 **DEDIE:** Double Error Detection Interrupt Enable Flag

bit 1 **SECIE:** Single Error Correction Interrupt Enable Flag

bit 0 **ECCEN:** ECC Enable
1 = ECC enabled
0 = ECC disabled

REGISTER 3-5: ECCSTAT – ECC STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ERRADDR<11:8>			
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ERRADDR<7:0>							
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	HS/C-0	HS/C-0	U-0
—	—	—	—	—	DEDIF	SECIF	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as ‘0’

bit 27-16 **ERRADDR<11:0>:** Address where last ECC error occurred

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2 **DEDIF:** Double Error Detection Interrupt Flag
1 = Double Error was detected
0 = No Double Error Detection occurred

bit 1 **SECIF:** Single Error Correction Interrupt Flag
1 = Single Error was corrected
0 = No Single Error occurred

bit 0 **Unimplemented:** Read as ‘0’

3.2 CAN FD Controller Module Registers

Configuration Registers

- Register 3-6: CiCON
- Register 3-7: CiNBTCFG
- Register 3-8: CiDBTCFG
- Register 3-9: CiTDC
- Register 3-10: CiTBC
- Register 3-11: CiTSCON

Interrupt and Status Registers

- Register 3-12: CiVEC
- Register 3-13: CiINT
- Register 3-14: CiRXIF
- Register 3-15: CiRXOVIF
- Register 3-16: CiTXIF
- Register 3-17: CiTXATIF
- Register 3-18: CiTXREQ

Error and Diagnostic Registers

- Register 3-19: CiTREC
- Register 3-20: CiBDIAG0
- Register 3-21: CiBDIAG1

Fifo Control and Status Registers

- Register 3-22: CiTEFCON
- Register 3-23: CiTEFSTA
- Register 3-24: CiTEFUA
- Register 3-25: CiTXQCON
- Register 3-26: CiTXQSTA
- Register 3-27: CiTXQUA
- Register 3-28: CiFIFOCONm – m = 1 to 31
- Register 3-29: CiFIFOSTAm – m = 1 to 31
- Register 3-30: CiFIFOUAm – m = 1 to 31

Filter Configuration and Control Registers

- Register 3-31: CiFLTCONm – m = 0 to 7
- Register 3-32: CiFLTOBJm – m = 0 to 31
- Register 3-33: CiMASKm – m = 0 to 31

Note: The 'i' shown in the register identifier denotes CANi, e.g., C1CON. The MCP2517FD contains one CAN FD Controller Module.

TABLE 3-4: REGISTER LEGEND

Sym	Description	Sym	Description
R	Readable bit	HC	Cleared by Hardware only
W	Writable bit	HS	Set by Hardware only
U	Unimplemented bit, read as '0'	1	Bit is set at Reset
S	Settable bit	0	Bit is cleared at Reset
C	Clearable bit	x	Bit is unknown at Reset

EXAMPLE 3-2:

R/W - 0 indicates the bit is both readable and writable, and reads '0' after a Reset.

REGISTER 3-6: CiCON – CAN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
TXBWS<3:0>				ABAT	REQOP<2:0>		
bit 31							bit 24

R-1	R-0	R-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
OPMOD<2:0>			TXQEN(1)	STEF(1)	SERR2LOM(1)	ESIGM(1)	RTXAT(1)
bit 23							bit 16

U-0	U-0	U-0	R/W-0	R-0	R/W-1	R/W-1	R/W-1
—	—	—	BRSDIS	BUSY	WFT<1:0>		WAKFIL(1)
bit 15							bit 8

U-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PXEDIS(1)	ISOCRCEN(1)	DNCNT<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **TXBWS<3:0>**: Transmit Bandwidth Sharing bits
Delay between two consecutive transmissions (in arbitration bit times)
`0000` = No delay
`0001` = 2
`0010` = 4
`0011` = 8
`0100` = 16
`0101` = 32
`0110` = 64
`0111` = 128
`1000` = 256
`1001` = 512
`1010` = 1024
`1011` = 2048
`1111-1100 = 4096`

bit 27 **ABAT**: Abort All Pending Transmissions bit
`1` = Signal all transmit FIFOs to abort transmission
`0` = Module will clear this bit when all transmissions were aborted

bit 26-24 **REQOP<2:0>**: Request Operation Mode bits
`000` = Set Normal CAN FD mode; supports mixing of CAN FD and Classic CAN 2.0 frames
`001` = Set Sleep mode
`010` = Set Internal Loopback mode
`011` = Set Listen Only mode
`100` = Set Configuration mode
`101` = Set External Loopback mode
`110` = Set Normal CAN 2.0 mode; possible error frames on CAN FD frames
`111` = Set Restricted Operation mode

Note 1: These bits can only be modified in Configuration mode.

REGISTER 3-6: CiCON – CAN CONTROL REGISTER (CONTINUED)

bit 23-21 **OPMOD<2:0>**: Operation Mode Status bits
000 = Module is in Normal CAN FD mode; supports mixing of CAN FD and Classic CAN 2.0 frames
001 = Module is in Sleep mode
010 = Module is in Internal Loopback mode
011 = Module is in Listen Only mode
100 = Module is in Configuration mode
101 = Module is in External Loopback mode
110 = Module is Normal CAN 2.0 mode; possible error frames on CAN FD frames
111 = Module is Restricted Operation mode

bit 20 **TXQEN**: Enable Transmit Queue bit(1)
1 = Enables TXQ and reserves space in RAM
0 = Don't reserve space in RAM for TXQ

bit 19 **STEF**: Store in Transmit Event FIFO bit(1)
1 = Saves transmitted messages in TEF and reserves space in RAM
0 = Don't save transmitted messages in TEF

bit 18 **SERR2LOM**: Transition to Listen Only Mode on System Error bit(1)
1 = Transition to Listen Only Mode
0 = Transition to Restricted Operation Mode

bit 17 **ESIGM**: Transmit ESI in Gateway Mode bit(1)
1 = ESI is transmitted recessive when ESI of message is high or CAN controller error passive
0 = ESI reflects error status of CAN controller

bit 16 **RTXAT**: Restrict Retransmission Attempts bit(1)
1 = Restricted retransmission attempts, CiFIFOCONm.TXAT is used
0 = Unlimited number of retransmission attempts, CiFIFOCONm.TXAT will be ignored

bit 15-13 **Unimplemented**: Read as '0'

bit 12 **BRSDIS**: Bit Rate Switching Disable bit
1 = Bit Rate Switching is Disabled, regardless of BRS in the Transmit Message Object
0 = Bit Rate Switching depends on BRS in the Transmit Message Object

bit 11 **BUSY**: CAN Module is Busy bit
1 = The CAN module is transmitting or receiving a message
0 = The CAN module is inactive

bit 10-9 **WFT<1:0>**: Selectable Wake-up Filter Time bits
00 = T00FILTER
01 = T01FILTER
10 = T10FILTER
11 = T11FILTER

Note: Please refer to Table 7-5.

bit 8 **WAKFIL**: Enable CAN Bus Line Wake-up Filter bit(1)
1 = Use CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 7 **Unimplemented**: Read as '0'

bit 6 **PXEDIS**: Protocol Exception Event Detection Disabled bit(1)
A recessive "res bit" following a recessive FDF bit is called a Protocol Exception.
1 = Protocol Exception is treated as a Form Error.
0 = If a Protocol Exception is detected, the CAN FD Controller Module will enter Bus Integrating state.

bit 5 **ISOCRCEN**: Enable ISO CRC in CAN FD Frames bit(1)
1 = Include Stuff Bit Count in CRC Field and use Non-Zero CRC Initialization Vector according to ISO 11898-1:2015
0 = Do NOT include Stuff Bit Count in CRC Field and use CRC Initialization Vector with all zeros

Note 1: These bits can only be modified in Configuration mode.

REGISTER 3-6: CiCON – CAN CONTROL REGISTER (CONTINUED)

bit 4-0 **DNCNT<4:0>**: Device Net Filter Bit Number bits
`10011-11111` = Invalid Selection (compare up to 18-bits of data with EID)
`10010` = Compare up to data byte 2 bit 6 with EID17
...
`00001` = Compare up to data byte 0 bit 7 with EID0
`00000` = Do not compare data bytes

Note 1: These bits can only be modified in Configuration mode.

REGISTER 3-7: CiNBTCFG – NOMINAL BIT TIME CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BRP<7:0>							
bit 31							bit 24

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0
TSEG1<7:0>							
bit 23							bit 16

U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
—	TSEG2<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
—	SJW<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **BRP<7:0>**: Baud Rate Prescaler bits
`1111 1111` = TQ = 256/Fsys
...
`0000 0000` = TQ = 1/Fsys

bit 23-16 **TSEG1<7:0>**: Time Segment 1 bits (Propagation Segment + Phase Segment 1)
`1111 1111` = Length is 256 x TQ
...
`0000 0000` = Length is 1 x TQ

bit 15 **Unimplemented**: Read as ‘0’

bit 14-8 **TSEG2<6:0>**: Time Segment 2 bits (Phase Segment 2)
`111 1111` = Length is 128 x TQ
...
`000 0000` = Length is 1 x TQ

bit 7 **Unimplemented**: Read as ‘0’

bit 6-0 **SJW<6:0>**: Synchronization Jump Width bits
`111 1111` = Length is 128 x TQ
...
`000 0000` = Length is 1 x TQ

Note 1: This register can only be modified in Configuration mode.

REGISTER 3-8: CiDBTCFG – DATA BIT TIME CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BRP<7:0>							
bit 31							bit 24

U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0
—	—	—	TSEG1<4:0>				
bit 23							bit 16

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1	R/W-1
—	—	—	—	TSEG2<3:0>			
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1	R/W-1
—	—	—	—	SJW<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **BRP<7:0>**: Baud Rate Prescaler bits
`1111 1111` = TQ = 256/Fsys
...
`0000 0000` = TQ = 1/Fsys

bit 23-21 **Unimplemented**: Read as ‘0’

bit 20-16 **TSEG1<4:0>**: Time Segment 1 bits (Propagation Segment + Phase Segment 1)
`1 1111` = Length is 32 x TQ
...
`0 0000` = Length is 1 x TQ

bit 15-12 **Unimplemented**: Read as ‘0’

bit 11-8 **TSEG2<3:0>**: Time Segment 2 bits (Phase Segment 2)
`1111` = Length is 16 x TQ
...
`0000` = Length is 1 x TQ

bit 7-4 **Unimplemented**: Read as ‘0’

bit 3-0 **SJW<3:0>**: Synchronization Jump Width bits
`1111` = Length is 16 x TQ
...
`0000` = Length is 1 x TQ

Note 1: This register can only be modified in Configuration mode.

REGISTER 3-9: CiTDC – TRANSMITTER DELAY COMPENSATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	EDGFLTEN	SID11EN
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
—	—	—	—	—	—	TDCMOD<1:0>	
bit 23							bit 16

U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
—	TDCO<6:0>						
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TDCV<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented**: Read as ‘0’

bit 25 **EDGFLTEN**: Enable Edge Filtering during Bus Integration state bit
1 = Edge Filtering enabled, according to ISO 11898-1:2015
0 = Edge Filtering disabled

bit 24 **SID11EN**: Enable 12-Bit SID in CAN FD Base Format Messages bit
1 = RRS is used as SID11 in CAN FD base format messages: SID<11:0> = {SID<10:0>, SID11}
0 = Don’t use RRS; SID<10:0> according to ISO 11898-1:2015

bit 23-18 **Unimplemented**: Read as ‘0’

bit 17-16 **TDCMOD<1:0>**: Transmitter Delay Compensation Mode bits; Secondary Sample Point (SSP)
10-11 = Auto; measure delay and add TDCO.
01 = Manual; Don’t measure, use TDCV + TDCO from register
00 = TDC Disabled

bit 15 **Unimplemented**: Read as ‘0’

bit 14-8 **TDCO<6:0>**: Transmitter Delay Compensation Offset bits; Secondary Sample Point (SSP)
Two’s complement; offset can be positive, zero, or negative.
011 1111 = 63 x TSYSCLK
...
000 0000 = 0 x TSYSCLK
...
111 1111 = –64 x TSYSCLK

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **TDCV<5:0>**: Transmitter Delay Compensation Value bits; Secondary Sample Point (SSP)
11 1111 = 63 x TSYSCLK
...
00 0000 = 0 x TSYSCLK

Note 1: This register can only be modified in Configuration mode.

REGISTER 3-10: CiTBC – TIME BASE COUNTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<31:24>							
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<23:16>							
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **TBC<31:0>**: Time Base Counter bits
This is a free running timer that increments every TBCPRE clocks when TBCEN is set

Note 1: The TBC will be stopped and reset when TBCEN = 0.
2: The TBC prescaler count will be reset on any write to CiTBC (CiTSCON.TBCPRE will be unaffected).

REGISTER 3-11: CiTSCON – TIME STAMP CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	TSRES	TSEOF	TBCEN
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	TBCPRE<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TBCPRE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-19 **Unimplemented**: Read as ‘0’

bit 18 **TSRES**: Time Stamp res bit (FD Frames only)
1 = at sample point of the bit following the FDF bit.
0 = at sample point of SOF

bit 17 **TSEOF**: Time Stamp EOF bit
1 = Time Stamp when frame is taken valid:
- RX no error until last but one bit of EOF
- TX no error until the end of EOF
0 = Time Stamp at “beginning” of Frame:
- Classical Frame: at sample point of SOF
- FD Frame: see TSRES bit.

bit 16 **TBCEN**: Time Base Counter Enable bit
1 = Enable TBC
0 = Stop and reset TBC

bit 15-10 **Unimplemented**: Read as ‘0’

bit 9-0 **TBCPRE<9:0>**: Time Base Counter Prescaler bits
1023 = TBC increments every 1024 clocks
...
0 = TBC increments every 1 clock

REGISTER 3-12: CiVEC – INTERRUPT CODE REGISTER

U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
—	RXCODE<6:0>[1]						
bit 31							bit 24

U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
—	TXCODE<6:0>[1]						
bit 23							bit 16

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	FILHIT<4:0>[1]				
bit 15							bit 8

U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
—	ICODE<6:0>[1]						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented**: Read as '0'

bit 30-24 **RXCODE<6:0>**: Receive Interrupt Flag Code bits[1]
1000001-1111111 = Reserved
1000000 = No interrupt
0100000-0111111 = Reserved

0011111 = FIFO 31 Interrupt (RFIF<31> set)
...
0000010 = FIFO 2 Interrupt (RFIF<2> set)
0000001 = FIFO 1 Interrupt (RFIF<1> set)
0000000 = Reserved. FIFO 0 can't receive.

bit 23 **Unimplemented**: Read as '0'

bit 22-16 **TXCODE<6:0>**: Transmit Interrupt Flag Code bits[1]
1000001-1111111 = Reserved
1000000 = No interrupt
0100000-0111111 = Reserved

0011111 = FIFO 31 Interrupt (TFIF<31> set)
...
0000001 = FIFO 1 Interrupt (TFIF<1> set)
0000000 = TXQ Interrupt (TFIF<0> set)

bit 15-13 **Unimplemented**: Read as '0'

bit 12-8 **FILHIT<4:0>**: Filter Hit Number bits[1]
11111 = Filter 31
11110 = Filter 30
...
00001 = Filter 1
00000 = Filter 0

bit 7 **Unimplemented**: Read as '0'

Note 1: If multiple interrupts are pending, the interrupt with the highest number will be indicated.

REGISTER 3-12: CiVEC – INTERRUPT CODE REGISTER (CONTINUED)

bit 6-0 **ICODE[6:0]**: Interrupt Flag Code bits[1]

`1001011`-`1111111` = Reserved
`1001010` = Transmit Attempt Interrupt (any bit in CiTXATIF set)
`1001001` = Transmit Event FIFO Interrupt (any bit in CiTEFIF set)
`1001000` = Invalid Message Occurred (IVMIF/IE)
`1000111` = Operation Mode Change Occurred (MODIF/IE)
`1000110` = TBC Overflow (TBCIF/IE)
`1000101` = RX/TX MAB Overflow/Underflow (RX: message received before previous message was saved to memory; TX: can't feed TX MAB fast enough to transmit consistent data.) (SERRIF/IE)
`1000100` = Address Error Interrupt (illegal FIFO address presented to system) (SERRIF/IE)
`1000011` = Receive FIFO Overflow Interrupt (any bit in CiRXOVIF set)
`1000010` = Wake-up interrupt (WAKIF/WAKIE)
`1000001` = Error Interrupt (CERRIF/IE)
`1000000` = No interrupt
`0100000`-`0111111` = Reserved
`0011111` = FIFO 31 Interrupt (TFIF<31> or RFIF<31> set)
...
`0000001` = FIFO 1 Interrupt (TFIF<1> or RFIF<1> set)
`0000000` = TXQ Interrupt (TFIF<0> set)

Note 1: If multiple interrupts are pending, the interrupt with the highest number will be indicated.

REGISTER 3-13: CiINT – INTERRUPT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IVMIE	WAKIE	CERRIE	SERRIE	RXOVIE	TXATIE	SPICRCIE	ECCIE
bit 31							bit 24

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TEFIE	MODIE	TBCIE	RXIE	TXIE
bit 23							bit 16

HS/C-0	HS/C-0	HS/C-0	HS/C-0	R-0	R-0	R-0	R-0
IVMIF(1)	WAKIF(1)	CERRIF(1)	SERRIF(1)	RXOVIF	TXATIF	SPICRCIF	ECCIF
bit 15							bit 8

U-0	U-0	U-0	R-0	HS/C-0	HS/C-0	R-0	R-0
—	—	—	TEFIF	MODIF(1)	TBCIF(1)	RXIF	TXIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **IVMIE**: Invalid Message Interrupt Enable bit

bit 30 **WAKIE**: Bus Wake Up Interrupt Enable bit

bit 29 **CERRIE**: CAN Bus Error Interrupt Enable bit

bit 28 **SERRIE**: System Error Interrupt Enable bit

bit 27 **RXOVIE**: Receive FIFO Overflow Interrupt Enable bit

bit 26 **TXATIE**: Transmit Attempt Interrupt Enable bit

bit 25 **SPICRCIE**: SPI CRC Error Interrupt Enable bit

bit 24 **ECCIE**: ECC Error Interrupt Enable bit

bit 23-21 **Unimplemented**: Read as '0'

bit 20 **TEFIE**: Transmit Event FIFO Interrupt Enable bit

bit 19 **MODIE**: Mode Change Interrupt Enable bit

bit 18 **TBCIE**: Time Base Counter Interrupt Enable bit

bit 17 **RXIE**: Receive FIFO Interrupt Enable bit

bit 16 **TXIE**: Transmit FIFO Interrupt Enable bit

bit 15 **IVMIF**: Invalid Message Interrupt Flag bit(1)

bit 14 **WAKIF**: Bus Wake Up Interrupt Flag bit(1)

bit 13 **CERRIF**: CAN Bus Error Interrupt Flag bit(1)

bit 12 **SERRIF**: System Error Interrupt Flag bit(1)
1 = A system error occurred
0 = No system error occurred

bit 11 **RXOVIF**: Receive Object Overflow Interrupt Flag bit
1 = Receive FIFO overflow occurred
0 = No receive FIFO overflow has occurred

bit 10 **TXATIF**: Transmit Attempt Interrupt Flag bit

bit 9 **SPICRCIF**: SPI CRC Error Interrupt Flag bit

Note 1: Flags are set by hardware and cleared by application.

REGISTER 3-13: CiINT – INTERRUPT REGISTER (CONTINUED)

bit 8	**ECCIF**: ECC Error Interrupt Flag bit
bit 7-5	**Unimplemented**: Read as ‘0’
bit 4	**TEFIF**: Transmit Event FIFO Interrupt Flag bit 1 = TEF interrupt pending 0 = No TEF interrupts pending
bit 3	**MODIF**: Operation Mode Change Interrupt Flag bit(1) 1 = Operation mode change occurred (OPMOD has changed) 0 = No mode change occurred
bit 2	**TBCIF**: Time Base Counter Overflow Interrupt Flag bit(1) 1 = TBC has overflowed 0 = TBC didn’t overflow
bit 1	**RXIF**: Receive FIFO Interrupt Flag bit 1 = Receive FIFO interrupt pending 0 = No receive FIFO interrupts pending
bit 0	**TXIF**: Transmit FIFO Interrupt Flag bit 1 = Transmit FIFO interrupt pending 0 = No transmit FIFO interrupts pending

Note 1: Flags are set by hardware and cleared by application.

REGISTER 3-14: CiRXIF – RECEIVE INTERRUPT STATUS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RFIF<31:24>							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RFIF<23:16>							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RFIF<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	U-0
RFIF<7:1>							—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-1 **RFIF<31:1>**: Receive FIFO Interrupt Pending bits[1]
1 = One or more enabled receive FIFO interrupts are pending
0 = No enabled receive FIFO interrupts are pending

bit 0 **Unimplemented**: Read as ‘0’

Note 1: RFIF = ‘or’ of enabled RXFIFO flags; flags will be cleared when the condition of the FIFO terminates.

REGISTER 3-15: CiRXOVIF – RECEIVE OVERFLOW INTERRUPT STATUS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RFOVIF<31:24>							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RFOVIF<23:16>							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RFOVIF<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	U-0
RFOVIF<7:1>							—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-1 **RFOVIF<31:1>**: Receive FIFO Overflow Interrupt Pending bits
1 = Interrupt is pending
0 = Interrupt not pending

bit 0 **Unimplemented**: Read as ‘0’

Note 1: Flags need to be cleared in FIFO register

REGISTER 3-16: CiTXIF – TRANSMIT INTERRUPT STATUS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TFIF<31:24>							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TFIF<23:16>(1)							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TFIF<15:8>(1)							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TFIF<7:0>(1)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **TFIF<31:0>**: Transmit FIFO/TXQ (2) Interrupt Pending bits(1)
`1` = One or more enabled transmit FIFO/TXQ interrupts are pending
`0` = No enabled transmit FIFO/TXQ interrupt are pending

Note 1: TFIF = ‘or’ of the enabled TXFIFO flags; flags will be cleared when the condition of the FIFO terminates.
2: TFIF<0> is for the Transmit Queue.

REGISTER 3-17: CiTXATIF – TRANSMIT ATTEMPT INTERRUPT STATUS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TFATIF<31:24>[1]							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TFATIF<23:16>[1]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TFATIF<15:8>[1]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TFATIF<7:0>[1]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **TFATIF<31:0>**: Transmit FIFO/TXQ [2] Attempt Interrupt Pending bits[1]
`1` = Interrupt is pending
`0` = Interrupt not pending

Note 1: Flags need to be cleared in FIFO register.
2: TFATIF<0> is for the Transmit Queue.

REGISTER 3-18: CiTXREQ – TRANSMIT REQUEST REGISTER

S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0
TXREQ<31:24>							
bit 31							bit 24

S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0
TXREQ<23:16>							
bit 23							bit 16

S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0
TXREQ<15:8>							
bit 15							bit 8

S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0
TXREQ<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-1 **TXREQ<31:1>**: Message Send Request bits
TXEN= 1 (Object configured as a Transmit Object)
Setting this bit to ‘1’ requests sending a message.
The bit will automatically clear when the message(s) queued in the object is (are) successfully sent.
This bit can NOT be used for aborting a transmission.
TXEN= 0 (Object configured as a Receive Object)
This bit has no effect

bit 0 **TXREQ<0>**: Transmit Queue Message Send Request bit
Setting this bit to ‘1’ requests sending a message.
The bit will automatically clear when the message(s) queued in the object is (are) successfully sent.
This bit can NOT be used for aborting a transmission.

REGISTER 3-19: CiTREC – TRANSMIT/RECEIVE ERROR COUNT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

U-0	U-0	R-1	R-0	R-0	R-0	R-0	R-0
—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TEC<7:0>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
REC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-22	**Unimplemented**: Read as ‘0’
bit 21	**TXBO**: Transmitter in Bus Off State bit (TEC > 255) In Configuration mode, TXBO is set, since the module is not on the bus.
bit 20	**TXBP**: Transmitter in Error Passive State bit (TEC > 127)
bit 19	**RXBP**: Receiver in Error Passive State bit (REC > 127)
bit 18	**TXWARN**: Transmitter in Error Warning State bit (128 > TEC > 95)
bit 17	**RXWARN**: Receiver in Error Warning State bit (128 > REC > 95)
bit 16	**EWARN**: Transmitter or Receiver is in Error Warning State bit
bit 15-8	**TEC<7:0>**: Transmit Error Counter bits
bit 7-0	**REC<7:0>**: Receive Error Counter bits

REGISTER 3-20: CiBDIAG0 – BUS DIAGNOSTIC REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTERRCNT<7:0>							
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DRERRCNT<7:0>							
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NTERRCNT<7:0>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NRERRCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **DTERRCNT<7:0>**: Data Bit Rate Transmit Error Counter bits

bit 23-16 **DRERRCNT<7:0>**: Data Bit Rate Receive Error Counter bits

bit 15-8 **NTERRCNT<7:0>**: Nominal Bit Rate Transmit Error Counter bits

bit 7-0 **NRERRCNT<7:0>**: Nominal Bit Rate Receive Error Counter bits

REGISTER 3-21: CiBDIAG1 – BUS DIAGNOSTICS REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
DLCMM	ESI	DCRCERR	DSTUFERR	DFORMERR	—	DBIT1ERR	DBIT0ERR
bit 31							bit 24

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXBOERR	—	NCRCERR	NSTUFERR	NFORMERR	NACKERR	NBIT1ERR	NBIT0ERR
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EFMSGCNT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EFMSGCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31	**DLCMM**: DLC Mismatch bit During a transmission or reception, the specified DLC is larger than the PLSIZE of the FIFO element.
bit 30	**ESI**: ESI flag of a received CAN FD message was set.
bit 29	**DCRCERR**: Same as for nominal bit rate (see below).
bit 28	**DSTUFERR**: Same as for nominal bit rate (see below).
bit 27	**DFORMERR**: Same as for nominal bit rate (see below).
bit 26	**Unimplemented**: Read as ‘0’
bit 25	**DBIT1ERR**: Same as for nominal bit rate (see below).
bit 24	**DBIT0ERR**: Same as for nominal bit rate (see below).
bit 23	**TXBOERR**: Device went to bus-off (and auto-recovered).
bit 22	**Unimplemented**: Read as ‘0’
bit 21	**NCRCERR**: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data.
bit 20	**NSTUFERR**: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.
bit 19	**NFORMERR**: A fixed format part of a received frame has the wrong format.
bit 18	**NACKERR**: Transmitted message was not acknowledged.
bit 17	**NBIT1ERR**: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value ‘1’), but the monitored bus value was dominant.
bit 16	**NBIT0ERR**: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value ‘0’), but the monitored bus value was recessive.
bit 15-0	**EFMSGCNT<15:0>**: Error Free Message Counter bits

REGISTER 3-22: CiTEFCON – TRANSMIT EVENT FIFO CONTROL REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FSIZE<4:0>(1)				
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	S/HC-1	U-0	S/HC-0
—	—	—	—	—	FRESET	—	UINC
bit 15							bit 8

U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TEFTSEN(1)	—	TEFOVIE	TEFFIE	TEFHIE	TEFNEIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-24 **FSIZE<4:0>:** FIFO Size bits(1)
0_0000 = FIFO is 1 Message deep
0_0001 = FIFO is 2 Messages deep
0_0010 = FIFO is 3 Messages deep
...
1_1111 = FIFO is 32 Messages deep

bit 23-11 **Unimplemented:** Read as ‘0’

bit 10 **FRESET**: FIFO Reset bit
1 = FIFO will be reset when bit is set, cleared by hardware when FIFO was reset. The user should wait for this bit to clear before taking any action.
0 = No effect

bit 9 **Unimplemented:** Read as ‘0’

bit 8 **UINC**: Increment Tail bit
When this bit is set, the FIFO tail will increment by a single message.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **TEFTSEN**: Transmit Event FIFO Time Stamp Enable bit(1)
1 = Time Stamp objects in TEF
0 = Don’t Time Stamp objects in TEF

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **TEFOVIE**: Transmit Event FIFO Overflow Interrupt Enable bit
1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 2 **TEFFIE**: Transmit Event FIFO Full Interrupt Enable bit
1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

Note 1: These bits can only be modified in Configuration mode.

REGISTER 3-22: CiTEFCON – TRANSMIT EVENT FIFO CONTROL REGISTER (CONTINUED)

bit 1	**TEFHIE**: Transmit Event FIFO Half Full Interrupt Enable bit 1 = Interrupt enabled for FIFO half full 0 = Interrupt disabled for FIFO half full
bit 0	**TEFNEIE**: Transmit Event FIFO Not Empty Interrupt Enable bit 1 = Interrupt enabled for FIFO not empty 0 = Interrupt disabled for FIFO not empty

Note 1: These bits can only be modified in Configuration mode.

REGISTER 3-23: CiTEFSTA – TRANSMIT EVENT FIFO STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	HS/C-0	R-0	R-0	R-0
—	—	—	—	TEFOVIF	TEFFIF(1)	TEFHIF(1)	TEFNEIF(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as ‘0’

bit 3 **TEFOVIF**: Transmit Event FIFO Overflow Interrupt Flag bit
1 = Overflow event has occurred
0 = No overflow event occurred

bit 2 **TEFFIF**: Transmit Event FIFO Full Interrupt Flag bit(1)
1 = FIFO is full
0 = FIFO is not full

bit 1 **TEFHIF**: Transmit Event FIFO Half Full Interrupt Flag bit(1)
1 = FIFO is ≥ half full
0 = FIFO is < half full

bit 0 **TEFNEIF**: Transmit Event FIFO Not Empty Interrupt Flag bit(1)
1 = FIFO is not empty, contains at least one message
0 = FIFO is empty

Note 1: This bit is read only and reflects the status of the FIFO.

REGISTER 3-24: CiTEFUA – TRANSMIT EVENT FIFO USER ADDRESS REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
TEFUA<31:24>							
bit 31							bit 24

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
TEFUA<23:16>							
bit 23							bit 16

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
TEFUA<15:8>							
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
TEFUA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **TEFUA<31:0>:** Transmit Event FIFO User Address bits

A read of this register will return the address where the next object is to be read (FIFO tail).

Note 1: This register is not guaranteed to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

REGISTER 3-25: CiTXQCON – TRANSMIT QUEUE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLSIZE<2:0>[1]			FSIZE<4:0>[1]				
bit 31							bit 24

U-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TXAT<1:0>		TXPRI<4:0>				
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	S/HC-1	R/W/HC-0	S/HC-0
—	—	—	—	—	FRESET[3]	TXREQ[2]	UINC
bit 15							bit 8

R-1	U-0	U-0	R/W-0	U-0	R/W-0	U-0	R/W-0
TXEN	—	—	TXATIE	—	TXQEIE	—	TXQNIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **PLSIZE<2:0>**: Payload Size bits[1]
000 = 8 data bytes
001 = 12 data bytes
010 = 16 data bytes
011 = 20 data bytes
100 = 24 data bytes
101 = 32 data bytes
110 = 48 data bytes
111 = 64 data bytes

bit 28-24 **FSIZE<4:0>**: FIFO Size bits[1]
0_0000 = FIFO is 1 Message deep
0_0001 = FIFO is 2 Messages deep
0_0010 = FIFO is 3 Messages deep
...
1_1111 = FIFO is 32 Messages deep

bit 23 **Unimplemented:** Read as ‘0’

bit 22-21 **TXAT<1:0>**: Retransmission Attempts bits
This feature is enabled when CiCON.RTXAT is set.
00 = Disable retransmission attempts
01 = Three retransmission attempts
10 = Unlimited number of retransmission attempts
11 = Unlimited number of retransmission attempts

bit 20-16 **TXPRI<4:0>**: Message Transmit Priority bits
00000 = Lowest Message Priority
...
11111 = Highest Message Priority

Note 1: These bits can only be modified in Configuration mode.
2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.
3: FRESET is set while in Configuration mode and is automatically cleared in Normal mode.

REGISTER 3-25: CiTXQCON – TRANSMIT QUEUE CONTROL REGISTER (CONTINUED)

bit 15-11	**Unimplemented:** Read as '0'
bit 10	**FRESET**: FIFO Reset bit(3) 1 = FIFO will be reset when bit is set; cleared by hardware when FIFO was reset. User should wait until this bit is clear before taking any action. 0 = No effect
bit 9	**TXREQ**: Message Send Request bit(2) 1 = Requests sending a message; the bit will automatically clear when all the messages queued in the TXQ are successfully sent. 0 = Clearing the bit to '0' while set ('1') will request a message abort.
bit 8	**UINC**: Increment Head bit When this bit is set, the FIFO head will increment by a single message.
bit 7	**TXEN**: TX Enable 1 = Transmit Message Queue. This bit always reads as '1'.
bit 6-5	**Unimplemented:** Read as '0'
bit 4	**TXATIE**: Transmit Attempts Exhausted Interrupt Enable bit 1 = Enable interrupt 0 = Disable interrupt
bit 3	**Unimplemented:** Read as '0'
bit 2	**TXQEIE**: Transmit Queue Empty Interrupt Enable bit 1 = Interrupt enabled for TXQ empty 0 = Interrupt disabled for TXQ empty
bit 1	**Unimplemented:** Read as '0'
bit 0	**TXQNIE**: Transmit Queue Not Full Interrupt Enable bit 1 = Interrupt enabled for TXQ not full 0 = Interrupt disabled for TXQ not full

Note 1: These bits can only be modified in Configuration mode.

2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.

3: FRESET is set while in Configuration mode and is automatically cleared in Normal mode.

REGISTER 3-26: CiTXQSTA – TRANSMIT QUEUE STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	TXQCI<4:0>[1]				
bit 15							bit 8

HS/C-0	HS/C-0	HS/C-0	HS/C-0	U-0	R-1	U-0	R-1
TXABT[2][3]	TXLARB[2][3]	TXERR[2][3]	TXATIF	—	TXQEIF	—	TXQNIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 3-13 **Unimplemented:** Read as ‘0’

bit 12-8 **TXQCI<4:0>:** Transmit Queue Message Index bits[1]
A read of this register will return an index to the message that the FIFO will next attempt to transmit.

bit 7 **TXABT**: Message Aborted Status bit[2][3]
1 = Message was aborted
0 = Message completed successfully

bit 6 **TXLARB**: Message Lost Arbitration Status bit[2][3]
1 = Message lost arbitration while being sent
0 = Message did not loose arbitration while being sent

bit 5 **TXERR**: Error Detected During Transmission bit[2][3]
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 4 **TXATIF**: Transmit Attempts Exhausted Interrupt Pending bit
1 = Interrupt pending
0 = Interrupt Not pending

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **TXQEIF**: Transmit Queue Empty Interrupt Flag bit
1 = TXQ is empty
0 = TXQ is not empty, at least 1 message queued to be transmitted

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **TXQNIF**: Transmit Queue Not Full Interrupt Flag bit
1 = TXQ is not full
0 = TXQ is full

Note 1: TXQCI<4:0> gives a zero-indexed value to the message in the TXQ. If the TXQ is 4 messages deep (FSIZE=5’h03) TXQCI will take on a value of 0 to 3 depending on the state of the TXQ.
2: This bit is cleared when TXREQ is set or by writing a 0 using the SPI.
3: This bit is updated when a message completes (or aborts) or when the TXQ is reset.

REGISTER 3-27: CiTXQUA – TRANSMIT QUEUE USER ADDRESS REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
TXQUA<31:24>							
bit 31							bit 24

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
TXQUA<23:16>							
bit 23							bit 16

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
TXQUA<15:8>							
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
TXQUA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **TXQUA<31:0>:** TXQ User Address bits
A read of this register will return the address where the next message is to be written (TXQ head).

Note 1: This register is not guaranteed to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

REGISTER 3-28: CiFIFOCONm – FIFO CONTROL REGISTER m, (m = 1 TO 31)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLSIZE<2:0>(1)			FSIZE<4:0>(1)				
bit 31							bit 24

U-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TXAT<1:0>		TXPRI<4:0>				
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	S/HC-1	R/W/HC-0	S/HC-0
—	—	—	—	—	FRESET(3)	TXREQ(2)	UINC
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXEN(1)	RTREN	RXTSEN(1)	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **PLSIZE<2:0>:** Payload Size bits(1)
000 = 8 data bytes
001 = 12 data bytes
010 = 16 data bytes
011 = 20 data bytes
100 = 24 data bytes
101 = 32 data bytes
110 = 48 data bytes
111 = 64 data bytes

bit 28-24 **FSIZE<4:0>:** FIFO Size bits(1)
0_0000 = FIFO is 1 Message deep
0_0001 = FIFO is 2 Messages deep
0_0010 = FIFO is 3 Messages deep
...
1_1111 = FIFO is 32 Messages deep

bit 23 **Unimplemented:** Read as ‘0’

bit 22-21 **TXAT<1:0>:** Retransmission Attempts bits
This feature is enabled when CiCON.RTXAT is set.
00 = Disable retransmission attempts
01 = Three retransmission attempts
10 = Unlimited number of retransmission attempts
11 = Unlimited number of retransmission attempts

bit 20-16 **TXPRI<4:0>:** Message Transmit Priority bits
00000 = Lowest Message Priority
...
11111 = Highest Message Priority

Note 1: These bits can only be modified in Configuration mode.
2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.
3: FRESET is set while in Configuration mode and is automatically cleared in Normal mode.

REGISTER 3-28: CiFIFOCONm – FIFO CONTROL REGISTER m, (m = 1 TO 31) (CONTINUED)

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **FRESET:** FIFO Reset bit(3)

1 = FIFO will be reset when bit is set; cleared by hardware when FIFO was reset. User should wait until this bit is clear before taking any action.

0 = No effect

bit 9 **TXREQ:** Message Send Request bit(2)

TXEN = 1 (FIFO configured as a Transmit FIFO)

1 = Requests sending a message; the bit will automatically clear when all the messages queued in the FIFO are successfully sent.

0 = Clearing the bit to '0' while set ('1') will request a message abort.

TXEN = 0 (FIFO configured as a Receive FIFO)

This bit has no effect.

bit 8 **UINC:** Increment Head/Tail bit

TXEN = 1 (FIFO configured as a Transmit FIFO)
When this bit is set, the FIFO head will increment by a single message.
TXEN = 0 (FIFO configured as a Receive FIFO)
When this bit is set, the FIFO tail will increment by a single message.

bit 7 **TXEN:** TX/RX FIFO Selection bit(1)

1 = Transmit FIFO
0 = Receive FIFO

bit 6 **RTREN**: Auto RTR Enable bit
1 = When a remote transmit is received, TXREQ will be set.
0 = When a remote transmit is received, TXREQ will be unaffected.

bit 5 **RXTSEN**: Received Message Time Stamp Enable bit(1)
1 = Capture time stamp in received message object in RAM.
0 = Don't capture time stamp.

bit 4 **TXATIE**: Transmit Attempts Exhausted Interrupt Enable bit
1 = Enable interrupt
0 = Disable interrupt

bit 3 **RXOVIE**: Overflow Interrupt Enable bit
1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 2 **TFERFFIE**: Transmit/Receive FIFO Empty/Full Interrupt Enable bit
TXEN = 1 (FIFO configured as a Transmit FIFO)
Transmit FIFO Empty Interrupt Enable
1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty
TXEN = 0 (FIFO configured as a Receive FIFO)
Receive FIFO Full Interrupt Enable
1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 1 **TFHRFHIE**: Transmit/Receive FIFO Half Empty/Half Full Interrupt Enable bit
TXEN = 1 (FIFO configured as a Transmit FIFO)
Transmit FIFO Half Empty Interrupt Enable
1 = Interrupt enabled for FIFO half empty
0 = Interrupt disabled for FIFO half empty
TXEN = 0 (FIFO configured as a Receive FIFO)
Receive FIFO Half Full Interrupt Enable
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

Note 1: These bits can only be modified in Configuration mode.
2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.
3: FRESET is set while in Configuration mode and is automatically cleared in Normal mode.

REGISTER 3-28: CiFIFOCONm – FIFO CONTROL REGISTER m, (m = 1 TO 31) (CONTINUED)

bit 0 **TFNRFNIE**: Transmit/Receive FIFO Not Full/Not Empty Interrupt Enable bit
TXEN = 1 (FIFO configured as a Transmit FIFO)
Transmit FIFO Not Full Interrupt Enable
1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full
TXEN = 0 (FIFO configured as a Receive FIFO)
Receive FIFO Not Empty Interrupt Enable
1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

Note 1: These bits can only be modified in Configuration mode.
2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.
3: FRESET is set while in Configuration mode and is automatically cleared in Normal mode.

REGISTER 3-29: CiFIFOSTAm – FIFO STATUS REGISTER m, (m = 1 TO 31)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	FIFOCI<4:0>(1)				
bit 15							bit 8

HS/C-0	HS/C-0	HS/C-0	HS/C-0	HS/C-0	R-0	R-0	R-0
TXABT(2)(3)	TXLARB(2)(3)	TXERR(2)(3)	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12-8 **FIFOCI<4:0>:** FIFO Message Index bits(1)

TXEN = 1 (FIFO is configured as a Transmit FIFO)
A read of this bit field will return an index to the message that the FIFO will next attempt to transmit.
TXEN = 0 (FIFO is configured as a Receive FIFO)
A read of this bit field will return an index to the message that the FIFO will use to save the next message

bit 7 **TXABT:** Message Aborted Status bit(2)(3)

1 = Message was aborted
0 = Message completed successfully

bit 6 **TXLARB:** Message Lost Arbitration Status bit(2)(3)

1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 5 **TXERR:** Error Detected During Transmission bit(2)(3)

1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 4 **TXATIF:** Transmit Attempts Exhausted Interrupt Pending bit

TXEN = 1 (FIFO is configured as a Transmit FIFO)
1 = Interrupt pending
0 = Interrupt not pending
TXEN = 0 (FIFO is configured as a Receive FIFO)
Read as ‘0’

Note 1: FIFOCI<4:0> gives a zero-indexed value to the message in the FIFO. If the FIFO is 4 messages deep (FSIZE=5’h03) FIFOCI will take on a value of 0 to 3 depending on the state of the FIFO.

2: This bit is cleared when TXREQ is set or by writing a 0 using the SPI.

3: This bit is updated when a message completes (or aborts) or when the FIFO is reset.

REGISTER 3-29: CiFIFOSTAm – FIFO STATUS REGISTER m, (m = 1 TO 31) (CONTINUED)

bit 3 **RXOVIF:** Receive FIFO Overflow Interrupt Flag bit
TXEN = 1 (FIFO is configured as a Transmit FIFO)
Unused, Read as '0'
TXEN = 0 (FIFO is configured as a Receive FIFO)
1 = Overflow event has occurred
0 = No overflow event has occurred

bit 2 **TFERFFIF:** Transmit/Receive FIFO Empty/Full Interrupt Flag bit
TXEN = 1 (FIFO is configured as a Transmit FIFO)
Transmit FIFO Empty Interrupt Flag
1 = FIFO is empty
0 = FIFO is not empty; at least one message queued to be transmitted
TXEN = 0 (FIFO is configured as a Receive FIFO)
Receive FIFO Full Interrupt Flag
1 = FIFO is empty
0 = FIFO is not full

bit 1 **TFHRFHIF:** Transmit/Receive FIFO Half Empty/Half Full Interrupt Flag bit
TXEN = 1 (FIFO is configured as a Transmit FIFO)
Transmit FIFO Half Empty Interrupt Flag
1 = FIFO is ≤ half full
0 = FIFO is > half full
TXEN = 0 (FIFO is configured as a Receive FIFO)
Receive FIFO Half Full Interrupt Flag
1 = FIFO is ≥ half full
0 = FIFO is < half full

bit 0 **TFNRFNIF:** Transmit/Receive FIFO Not Full/Not Empty Interrupt Flag bit
TXEN = 1 (FIFO is configured as a Transmit FIFO)
Transmit FIFO Not Full Interrupt Flag
1 = FIFO is not full
0 = FIFO is full
TXEN = 0 (FIFO is configured as a Receive FIFO)
Receive FIFO Not Empty Interrupt Flag
1 = FIFO is not empty, contains at least one message
0 = FIFO is empty

Note 1: FIFOCI<4:0> gives a zero-indexed value to the message in the FIFO. If the FIFO is 4 messages deep (FSIZE=5'h03) FIFOCI will take on a value of 0 to 3 depending on the state of the FIFO.
2: This bit is cleared when TXREQ is set or by writing a 0 using the SPI.
3: This bit is updated when a message completes (or aborts) or when the FIFO is reset.

REGISTER 3-30: CiFIFOUAm – FIFO USER ADDRESS REGISTER m, (m = 1 TO 31)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<31:24>							
bit 31							bit 24

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<23:16>							
bit 23							bit 16

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<15:8>							
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FIFOUA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **FIFOUA<31:0>:** FIFO User Address bits

TXEN = 1 (FIFO is configured as a Transmit FIFO)
A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0 (FIFO is configured as a Receive FIFO)
A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This bit is not guaranteed to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

REGISTER 3-31: CiFLTCONm – FILTER CONTROL REGISTER m, (m = 0 TO 7)

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTEN3	—	—	F3BP<4:0>[1]				
bit 31							bit 24

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTEN2	—	—	F2BP<4:0>[1]				
bit 23							bit 16

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTEN1	—	—	F1BP<4:0>[1]				
bit 15							bit 8

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTEN0	—	—	F0BP<4:0>[1]				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN3:** Enable Filter 3 to Accept Messages bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **Unimplemented:** Read as ‘0’

bit 28-24 **F3BP<4:0>:** Pointer to FIFO when Filter 3 hits bits[1]
1_1111 = Message matching filter is stored in FIFO 31
1_1110 = Message matching filter is stored in FIFO 30
....
0_0010 = Message matching filter is stored in FIFO 2
0_0001 = Message matching filter is stored in FIFO 1
0_0000 = Reserved FIFO 0 is the TX Queue and can’t receive messages

bit 23 **FLTEN2>:** Enable Filter 2 to Accept Messages bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **Unimplemented:** Read as ‘0’

bit 20-16 **F2BP<4:0>:** Pointer to FIFO when Filter 2 hits bits[1]
1_1111 = Message matching filter is stored in FIFO 31
1_1110 = Message matching filter is stored in FIFO 30
....
0_0010 = Message matching filter is stored in FIFO 2
0_0001 = Message matching filter is stored in FIFO 1
0_0000 = Reserved FIFO 0 is the TX Queue and can’t receive messages

bit 15 **FLTEN1:** Enable Filter 1 to Accept Messages bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **Unimplemented:** Read as ‘0’

Note 1: This bit can only be modified if the corresponding filter is disabled (FLTEN = 0).

REGISTER 3-31: CiFLTCONm – FILTER CONTROL REGISTER m, (m = 0 TO 7) (CONTINUED)

bit 12-8 **F1BP<4:0>:** Pointer to FIFO when Filter 1 hits bits[1]

1_1111 = Message matching filter is stored in FIFO 31
1_1110 = Message matching filter is stored in FIFO 30
....
0_0010 = Message matching filter is stored in FIFO 2
0_0001= Message matching filter is stored in FIFO 1
0_0000 = Reserved FIFO 0 is the TX Queue and can't receive messages

bit 7 **FLTEN0:** Enable Filter 0 to Accept Messages bit

1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 4-0 **F0BP<4:0>:** Pointer to FIFO when Filter 0 hits bits[1]

1_1111 = Message matching filter is stored in FIFO 31
1_1110 = Message matching filter is stored in FIFO 30
....
0_0010 = Message matching filter is stored in FIFO 2
0_0001 = Message matching filter is stored in FIFO 1
0_0000 = Reserved FIFO 0 is the TX Queue and can't receive messages

Note 1: This bit can only be modified if the corresponding filter is disabled (FLTEN = 0).

REGISTER 3-32: CiFLTOBJm – FILTER OBJECT REGISTER m,(m = 0 TO 31)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	EXIDE	SID11	EID<17:13>				
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EID<12:5>							
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EID<4:0>					SID<10:8>		
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as ‘0’

bit 30 **EXIDE:** Extended Identifier Enable bit
If MIDE = 1:
1 = Match only messages with extended identifier
0 = Match only messages with standard identifier

bit 29 **SID11:** Standard Identifier filter bit

bit 28-11 **EID<17:0>:** Extended Identifier filter bits
In DeviceNet mode, these are the filter bits for the first 18 data bits

bit 10-0 **SID<10:0>:** Standard Identifier filter bits

Note 1: This register can only be modified when the filter is disabled(CiFLTCON.FLTENm = 0).

REGISTER 3-33: CiMASKm – MASK REGISTER m, (m = 0 TO 31)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MIDE	MSID11	MEID<17:13>				
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MEID<12:5>							
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MEID<4:0>					MSID<10:8>		
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MSID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as ‘0’

bit 30 **MIDE:** Identifier Receive mode bit
1 = Match only message types (standard or extended ID) that correspond to EXIDE bit in filter
0 = Match both standard and extended message frames if filters match

bit 29 **MSID11:** Standard Identifier Mask bit

bit 28-11 **MEID<17:0>:** Extended Identifier Mask bits
In DeviceNet mode, these are the mask bits for the first 18 data bits

bit 10-0 **MSID<10:0>:** Standard Identifier Mask bits

NOTES:

3.3 Message Memory

The MCP2517FD contains a 2 KB RAM that is used to store message objects. There are three different kinds of message objects:

- Table 3-5: Transmit Message Objects used by the TXQ and by TX FIFOs.
- Table 3-6: Receive Message Objects used by RX FIFOs.
- Table 3-7: TEF objects.

Figure 3-2 illustrates how message objects are mapped into RAM. The number of message objects for the TEF, the TXQ, and for each FIFO is configurable. Only the message objects for FIFO2 are shown in detail. The number of data bytes per message object (payload) is individually configurable for the TXQ and each FIFO.

FIFOs and message objects can only be configured in Configuration mode.

The TEF objects are allocated first. Space in RAM will only be reserved if CiCON.STEF = 1.

Next the TXQ objects are allocated. Space in RAM will only be reserved if CiCON.TXQEN = 1.

Next the message objects for FIFO1 through FIFO31 are allocated.

This highly flexible configuration results in an efficient usage of the RAM.

The addresses of the message objects depend on the selected configuration. The application doesn't have to calculate the addresses. The User Address field provides the address of the next message object to read from or write to.

3.3.1 RAM ECC

The RAM is protected with an Error Correction Code (ECC). The ECC logic supports Single Error Correction (SEC), and Double Error Detection (DED).

SEC/DED requires seven parity bits in addition to the 32 data bits.

Figure 3-3 shows the block diagram of the ECC logic.

3.3.1.1 ECC Enable and Disable

The ECC logic can be enabled by setting ECCCON.ECCEN. When ECC is enabled, the data written to the RAM is encoded, and the data read from RAM is decoded.

When the ECC logic is disabled, the data is written to RAM, the parity bits are taken from ECCCON.PARITY. This enables the testing of the ECC logic by the user. During a read the parity bits are stripped out and the data is read back unchanged.

3.3.1.2 RAM Write

During a RAM write, the Encoder calculates the parity bits and adds the parity bits to the input data.

3.3.1.3 RAM READ

During a RAM read, the Decoder checks the output data from RAM for consistency and removes the parity bits. It corrects single bit errors and detects double bit errors.

FIGURE 3-2: MESSAGE MEMORY ORGANIZATION

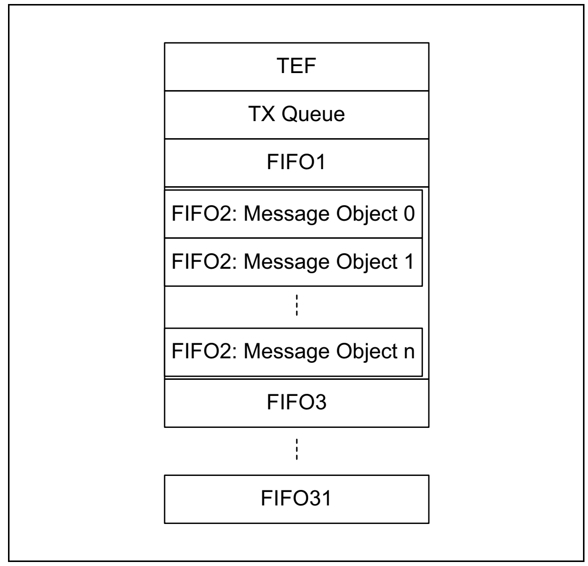


FIGURE 3-3: ECC LOGIC

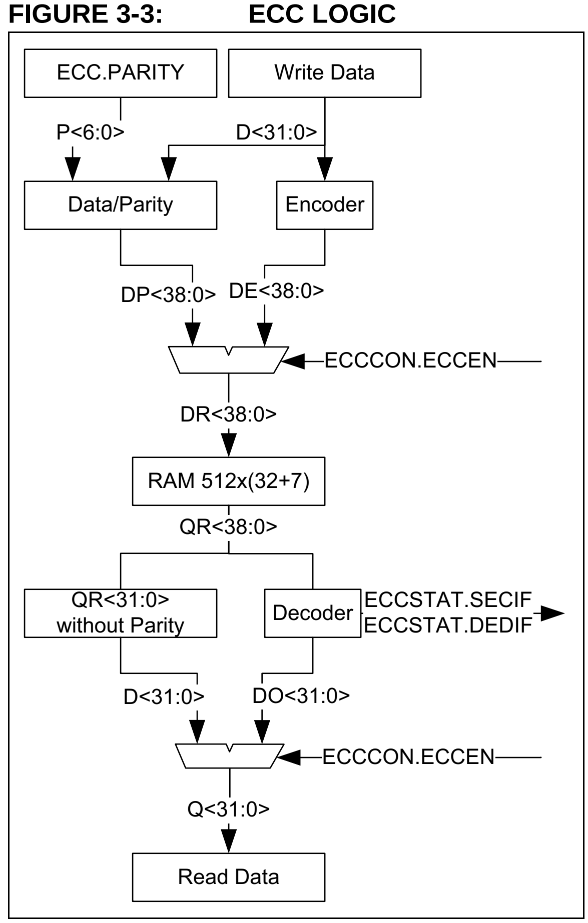


TABLE 3-5: TRANSMIT MESSAGE OBJECT (TXQ AND TX FIFO)

Word		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
T0	31:24	—	—	SID11	EID<17:6>				
	23:16	EID<12:5>							
	15:8	EID<4:0>					SID<10:8>		
	7:0	SID<7:0>							
T1	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	SEQ<6:0>							ESI
	7:0	FDF	BRS	RTR	IDE	DLC<3:0>			
T2 (1)	31:24	Transmit Data Byte 3							
	23:16	Transmit Data Byte 2							
	15:8	Transmit Data Byte 1							
	7:0	Transmit Data Byte 0							
T3	31:24	Transmit Data Byte 7							
	23:16	Transmit Data Byte 6							
	15:8	Transmit Data Byte 5							
	7:0	Transmit Data Byte 4							
Ti	31:24	Transmit Data Byte n							
	23:16	Transmit Data Byte n-1							
	15:8	Transmit Data Byte n-2							
	7:0	Transmit Data Byte n-3							

bit T0.31-30 **Unimplemented:** Read as 'x'

bit T0.29 **SID11:** In FD mode the standard ID can be extended to 12 bit using r1

bit T0.28-11 **EID<17:0>:** Extended Identifier

bit T0.10-0 **SID<10:0>:** Standard Identifier

bit T1.31-16 **Unimplemented:** Read as 'x'

bit T1.15-9 **SEQ<6:0>:** Sequence to keep track of transmitted messages in Transmit Event FIFO

bit T1.8 **ESI:** Error Status Indicator

In CAN to CAN gateway mode (CiCON.ESIGM=1), the transmitted ESI flag is a "logical OR" of T1.ESI and error passive state of the CAN controller;

In normal mode ESI indicates the error status

1 = Transmitting node is error passive

0 = Transmitting node is error active

bit T1.7 **FDF:** FD Frame; distinguishes between CAN and CAN FD formats

bit T1.6 **BRS:** Bit Rate Switch; selects if data bit rate is switched

bit T1.5 **RTR:** Remote Transmission Request; not used in CAN FD

bit T1.4 **IDE:** Identifier Extension Flag; distinguishes between base and extended format

bit T1.3-0 **DLC<3:0>:** Data Length Code

Note 1: Data Bytes 0-n: payload size is configured individually in control register (CiFIFOCONm.PLSIZE<2:0>).

TABLE 3-6: RECEIVE MESSAGE OBJECT

Word		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
R0	31:24	—	—	SID11	EID<17:6>				
	23:16	EID<12:5>							
	15:8	EID<4:0>					SID<10:8>		
	7:0	SID<7:0>							
R1	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	FILHIT<4:0>					—	—	ESI
	7:0	FDF	BRS	RTR	IDE	DLC<3:0>			
R2 (2)	31:24	RXMSGTS<31:24>							
	23:16	RXMSGTS<23:16>							
	15:8	RXMSGTS<15:8>							
	7:0	RXMSGTS<7:0>							
R3 (1)	31:24	Receive Data Byte 3							
	23:16	Receive Data Byte 2							
	15:8	Receive Data Byte 1							
	7:0	Receive Data Byte 0							
R4	31:24	Receive Data Byte 7							
	23:16	Receive Data Byte 6							
	15:8	Receive Data Byte 5							
	7:0	Receive Data Byte 4							
Ri	31:24	Receive Data Byte n							
	23:16	Receive Data Byte n-1							
	15:8	Receive Data Byte n-2							
	7:0	Receive Data Byte n-3							

bit R0.31-30 **Unimplemented:** Read as ‘x’

bit R0.29 **SID11:** In FD mode the standard ID can be extended to 12 bit using r1

bit R0.28-11 **EID<17:0>:** Extended Identifier

bit R0.10-0 **SID<10:0>:** Standard Identifier

bit R1.31-16 **Unimplemented:** Read as ‘x’

bit R1.15-11 **FILTHIT<4:0>:** Filter Hit, number of filter that matched

bit R1.10-9 **Unimplemented:** Read as ‘x’

bit R1.8 **ESI:** Error Status Indicator
1 = Transmitting node is error passive
0 = Transmitting node is error active

bit R1.7 **FDF:** FD Frame; distinguishes between CAN and CAN FD formats

bit R1.6 **BRS:** Bit Rate Switch; indicates if data bit rate was switched

bit R1.5 **RTR:** Remote Transmission Request; not used in CAN FD

bit R1.4 **IDE:** Identifier Extension Flag; distinguishes between base and extended format

bit R1.3-0 **DLC<3:0>:** Data Length Code

bit R2.31-0 **RXMSGTS<31:0>:** Receive Message Time Stamp

Note 1: RXMOBJ: Data Bytes 0-n: payload size is configured individually in the FIFO control register (CiFIFOCONm.PLSIZE<2:0>).
2: R2 (RXMSGTS) only exits in objects where CiFIFOCONm.RXTSEN is set.

TABLE 3-7: TRANSMIT EVENT FIFO OBJECT

Word		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
TE0	31:24	—	—	SID11	EID<17:6>				
	23:16	EID<12:5>							
	15:8	EID<4:0>					SID<10:8>		
	7:0	SID<7:0>							
TE1	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	SEQ<6:0>							ESI
	7:0	FDF	BRS	RTR	IDE	DLC<3:0>			
TE2 [(1)]	31:24	TXMSGTS<31:24>							
	23:16	TXMSGTS<23:16>							
	15:8	TXMSGTS<15:8>							
	7:0	TXMSGTS<7:0>							

bit TE0.31-30 **Unimplemented:** Read as ‘x’

bit TE0.29 **SID11:** In FD mode the standard ID can be extended to 12 bit using r1

bit TE0.28-11 **EID<17:0>:** Extended Identifier

bit TE0.10-0 **SID<10:0>:** Standard Identifier

bit TE1.31-16 **Unimplemented:** Read as ‘x’

bit TE1.15-9 **SEQ<6:0>:** Sequence to keep track of transmitted messages

bit TE1.8 **ESI:** Error Status Indicator

1 = Transmitting node is error passive
0 = Transmitting node is error active

bit TE1.7 **FDF:** FD Frame; distinguishes between CAN and CAN FD formats

bit TE1.6 **BRS:** Bit Rate Switch; selects if data bit rate is switched

bit TE1.5 **RTR:** Remote Transmission Request; not used in CAN FD

bit TE1.4 **IDE:** Identifier Extension Flag; distinguishes between base and extended format

bit TE1.3-0 **DLC<3:0>:** Data Length Code

bit TE2.31-0 **TXMSGTS<31:0>:** Transmit Message Time Stamp [(1)]

Note 1: TE2 (TXMSGTS) only exits in objects where CiTEFCON.TEFTSEN is set.

4.0 SPI INTERFACE

The MCP2517FD is designed to interface directly with an Serial Peripheral Interface (SPI) port available on most microcontrollers. The SPI in the microcontroller must be configured in mode 0,0 or 1,1 in 8-bit operating mode.

SFR and Message Memory (RAM) are accessed using SPI instructions. Figure 4-1 illustrates the generic format of the SPI instructions (SPI mode 0,0). Each instruction starts with driving nCS low (falling edge on nCS). The 4-bit command and the 12-bit address are shifted into SDI on the rising edge of SCK. During a write instruction, data bits are shifted into SDI on the rising edge of SCK. During a read instruction, data bits are shifted out of SDO on the falling edge of SCK. One or more data bytes are transfered with one instruction. Data bits are updated on the falling edge of SCK and must be valid on the rising edge of SCK. Each instruction ends with driving nCS high (rising edge on nCS).

Refer to Figure 7-1 for detailed input and output timing for both mode 0,0 and mode 1,1.

Table 4-1 lists the SPI instructions and their format.

> **Note 1:** The frequency of SCK has to be less than or equal to half the frequency of SYSCLK. This ensures that the synchronization between SCK and SYSCLK works correctly.
>
> **2:** In order to minimize the Sleep current, the SDO pin of the MCP2517FD must not be left floating while the device is in Sleep mode. This can be achieved by enabling a pull-up or pull-down resistor inside the MCU on the pin that is connected to the SDO pin of the MCP2517FD, while the MCP2517FD is in Sleep mode.

FIGURE 4-1: SPI INSTRUCTION FORMAT

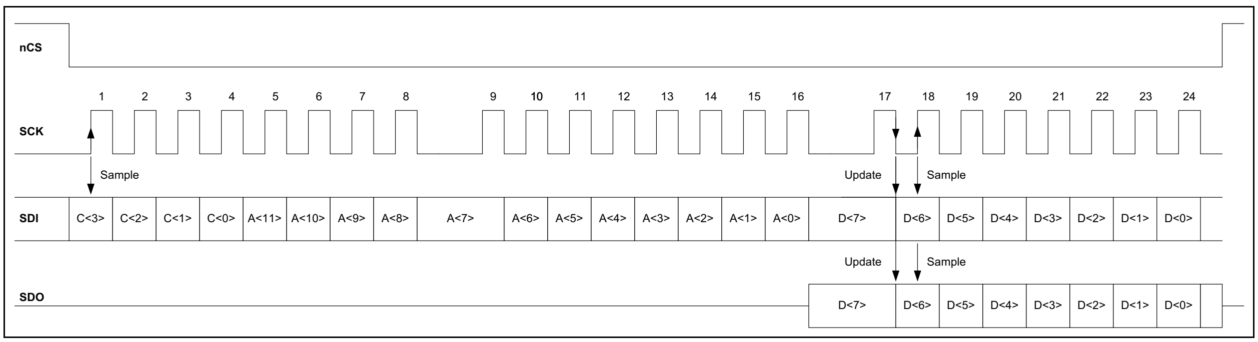


TABLE 4-1: SPI INSTRUCTIONS

Name	Format	Description
RESET	C = 0b0000; A = 0x000	Resets internal registers to default state; selects Configuration mode.
READ	C = 0b0011; A; D = SDO	Read SFR/RAM from address A.
WRITE	C = 0b0010; A; D = SDI	Write SFR/RAM to address A.
READ_CRC	C = 0b1011; A; N; D = SDO; CRC = SDO	Read SFR/RAM from address A. N data bytes. Two bytes CRC. CRC is calculated on C, A, N and D.
WRITE_CRC	C = 0b1010; A; N; D = SDI; CRC = SDI	Write SFR/RAM to address A. N data bytes. Two bytes CRC. CRC is calculated on C, A, N and D.
WRITE_SAFE	C = 0b1100; A; D = SDI; CRC = SDI	Write SFR/RAM to address A. Check CRC before write. CRC is calculated on C, A and D.

Legend: C = Command (4 bit), A = Address (12 bit), D = Data (1 to n bytes), N = Number of Bytes (1 byte), CRC (2 bytes)

4.1 SFR Access

The SFR access is byte-oriented. Any number of data bytes can be read or written with one instruction. The address is incremented by one automatically after every data byte. The address rolls over from 0x3FF to 0x000 and from 0xFFF to 0xE00.

The following SPI instructions only show the different fields and their values. Every instruction follows the generic format illustrated in Figure 4-1.

4.1.1 RESET

Figure 4-2 illustrates the RESET instruction. The instruction starts with nCS going low. The Command (C<3:0> = 0b0000) is followed by the Address (A<11:0> = 0x000). The instruction ends when nCS goes high.

The RESET instruction should only be issued after the device has entered Configuration mode. All SFR and State Machines are reset just like during a Power-on Reset (POR), and the device transitions immediately to Configuration mode.

The Message Memory is not changed.

The actual reset happens at the end of the instruction when nCS goes high.

4.1.2 SFR READ - READ

Figure 4-3 illustrates the READ instruction, while accessing SFR. The instruction starts with nCS going low. The Command (C<3:0> = 0b0011), is followed by the Address (A<11:0>). Afterwards, the data byte from address A (DB[A]) is shifted out, followed by data byte from address A+1 (DB[A+1]). Any number of data bytes can be read. The instruction ends when nCS goes high.

4.1.3 SFR WRITE - WRITE

Figure 4-4 illustrates the WRITE instruction, while accessing SFR. The instruction starts with nCS going low. The Command (C<3:0> = 0b0010), is followed by the Address (A<11:0>). Afterwards, the data byte is shifted into address A (DB[A]), next into address A+1 (DB[A+1]). Any number of data bytes can be written. The instruction ends when nCS goes high.

Data bytes are written to the register with the falling edge on SCK following the 8th data bit.

FIGURE 4-2: RESET INSTRUCTION

nCS Low	0b0000	0x000	nCS High

FIGURE 4-3: SFR READ INSTRUCTION

nCS Low	0b0011	A<11:0>	DB[A]	DB[A+1]	- - - - -	DB[A+n-1]	nCS High

FIGURE 4-4: SFR WRITE INSTRUCTION

nCS Low	0b0010	A<11:0>	DB[A]	DB[A+1]	- - - - -	DB[A+n-1]	nCS High

4.2 Message Memory Access

The Message Memory (RAM) access is Word-oriented (4 bytes at a time). Any multiple of 4 data bytes can be read or written with one instruction. The address is incremented by one automatically after every data byte. The address rolls over from 0xBFF to 0x400.

The following SPI instructions only show the different fields and their values. Every instruction follows the generic format illustrated in Figure 4-1.

4.2.1 MESSAGE MEMORY READ - READ

Figure 4-5 illustrates the READ instruction, while accessing RAM. The instruction starts with nCS going low. The Command (C<3:0> = 0b0011), is followed by the Address (A<11:0>). Afterwards, the data byte from address A (DB[A]) is shifted out, followed by data byte from address A+1 (DB[A+1]). The instruction ends when nCS goes high.

Read commands from RAM must always read a multiple of 4 data bytes. A word is internally read from RAM after the address field, and after every fourth data byte read on the SPI. In case nCS goes high before a multiple of 4 data bytes is read on SDO, the incomplete read should be discarded by the microcontroller.

4.2.2 MESSAGE MEMORY WRITE - WRITE

Figure 4-6 illustrates the WRITE instruction, while accessing RAM. The instruction starts with nCS going low. The Command (C<3:0> = 0b0010), is followed by the Address (A<11:0>). Afterwards, the data byte is shifted into address A (DB[A]), next into address A+1 (DB[A+1]). The instruction ends when nCS goes high.

Write commands must always write a multiple of 4 data bytes. After every fourth data byte, with the falling edge on SCK, the RAM Word gets written. In case nCS goes high before a multiple of 4 data bytes is received on SDI, the data of the incomplete Word will not be written to RAM.

FIGURE 4-5: MESSAGE MEMORY READ INSTRUCTION

nCS Low	0b0011	A<11:0>	DW[A]				nCS High
			DB[A]	DB[A+1]	DB[A+2]	DB[A+3]	

FIGURE 4-6: MESSAGE MEMORY WRITE INSTRUCTION

nCS Low	0b0010	A<11:0>	DW[A]				nCS High
			DB[A]	DB[A+1]	DB[A+2]	DB[A+3]	

4.3 SPI Commands with CRC

In order to detect or avoid bit errors during SPI communication, SPI commands with CRC are available.

4.3.1 CRC CALCULATION

In parallel with the SPI shift register, the CRC is calculated, see Figure 4-7.

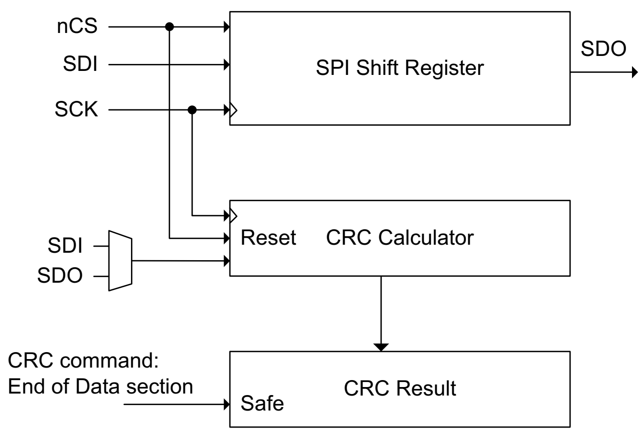
When nCS is asserted, the CRC calculator is reset to 0xFFFF.

The result of the CRC calculation is available after the Data section of a CRC command. The result of the CRC calculation is written to the CRC register in case a CRC mismatch is detected. In case of a CRC mismatch, CRC.CRCERRIF is set.

The MCP2517FD uses the following generator polynomial: CRC-16/USB (0x8005). CRC-16 detects all single and double-bit errors, all errors with an odd number of bits, all burst errors of length 16 or less, and most errors for longer bursts. This allows an excellent detection of SPI communication errors that can happen in the system, and heavily reduces the risk of miscommunication, even under noisy environments.

The maximum number of data bits is used while reading and writing TX or RX Message Objects. A RX Message Object with 64 Bytes of data + 12 Bytes ID and Time Stamp contains 76 Bytes or 608 bits. In comparison, USB data packets contain up to 1024 bits. CRC-16 has a Hamming Distance of 4 up to 1024 bits.

FIGURE 4-7: CRC CALCULATION



4.3.2 SFR READ WITH CRC - READ_CRC

Figure 4-8 illustrates the READ_CRC instruction, while accessing SFR. The instruction starts with nCS going low. The Command (C<3:0> = 0b1011), is followed by the Address (A<11:0>), and the number of data bytes (N<7:0>). Afterwards, the data byte from address A (DB[A]) is shifted out, followed by the data byte from address A+1 (DB[A+1]). Any number of data bytes can be read. Next the CRC is shifted out (CRC<15:0>). The instruction ends when nCS goes high.

The CRC is provided to the microcontroller. The microcontroller checks the CRC. No interrupt is generated on CRC mismatch during a READ_CRC command inside the MCP2517FD.

If nCS goes high before the last byte of the CRC is shifted out, a CRC Form Error interrupt is generated: CRC.FERRIF.

4.3.3 SFR WRITE WITH CRC - WRITE_CRC

Figure 4-9 illustrates the WRITE_CRC instruction, while accessing SFR. The instruction starts with nCS going low. The Command (C<3:0> = 0b1010), is followed by the Address (A<11:0>), and the number of data bytes (N<7:0>). Afterwards, the data byte is shifted into address A (DB[A]), next into address A+1 (DB[A+1]). Any number of data bytes can be written. Next the CRC is shifted in (CRC<15:0>). The instruction ends when nCS goes high.

The SFR is written to the register after the data byte was shifted in on SDI, with the falling edge on SCK. Data bytes are written to the register before the CRC is checked.

The CRC is checked at the end of the write access. In case of a CRC mismatch, a CRC Error interrupt is generated: CRC.CRCERRIF.

If nCS goes high before the last byte of the CRC is shifted in, a CRC Form Error interrupt is generated: CRC.FERRIF.

FIGURE 4-8: SFR READ WITH CRC INSTRUCTION

nCS Low	0b1011	A<11:0>	N<7:0>	DB[A]	DB[A+1]	-----	DB[A+n-1]	CRC<15:8>	CRC<7:0>	nCS High

FIGURE 4-9: SFR WRITE WITH CRC INSTRUCTION

nCS Low	0b1010	A<11:0>	N<7:0>	DB[A]	DB[A+1]	-----	DB[A+n-1]	CRC<15:8>	CRC<7:0>	nCS High

4.3.4 SFR WRITE SAFE WITH CRC - WRITE_SAFE

This instruction ensures that only correct data is written to the SFR.

Figure 4-10 illustrates the WRITE_SAFE instruction, while accessing SFR. The instruction starts with nCS going low. The Command (C<3:0> = 0b1100), is followed by the Address (A<11:0>). Afterwards, one data byte is shifted into address A (DB[A]). Next the CRC (CRC<15:0>) is shifted in. The instruction ends when nCS goes high.

The data byte is only written to the SFR after the CRC is checked and if it matches.

If the CRC mismatches, the data byte is not written to the SFR and a CRC Error interrupt is generated: CRC.CRCERRIF.

If nCS goes high before the last byte of the CRC is shifted in, a CRC Form Error interrupt is generated: CRC.FERRIF.

FIGURE 4-10: SFR WRITE SAFE WITH CRC INSTRUCTION

nCS Low	0b1100	A<11:0>	DB[A]	CRC<15:8>	CRC<7:0>	nCS High

4.3.5 MESSAGE MEMORY READ WITH CRC- READ_CRC

Figure 4-11 illustrates the READ_CRC instruction, while accessing RAM. The instruction starts with nCS going low. The Command (C<3:0> = 0b1011), is followed by the Address (A<11:0>), and the number of data Words (N<7:0>). Afterwards, the data byte from address A (DB[A]) is shifted out, followed by data byte from address A+1 (DB[A+1]). Next the CRC (CRC<15:0>) is shifted out. The instruction ends when nCS goes high.

Read commands should always read a multiple of 4 data bytes. A word is internally read from RAM after the “N” field, and after every fourth data byte read on the SPI. In case nCS goes high before a multiple of 4 data bytes are read on SDO, the incomplete read should be discarded by the microcontroller.

The CRC is provided to the microcontroller. The microcontroller checks the CRC. No interrupt is generated on CRC mismatch during a READ_CRC command inside the MCP2517FD.

If nCS goes high before the last byte of the CRC is shifted out, a CRC Form Error interrupt is generated: CRC.FERRIF.

4.3.6 MESSAGE MEMORY WRITE WITH CRC - WRITE_CRC

Figure 4-12 illustrates the WRITE instruction, while accessing RAM. The instruction starts with nCS going low. The Command (C<3:0> = 0b1010), is followed by the Address (A<11:0>), and the number of data Words (N<7:0>). Afterwards, the data byte is shifted into address A (DB[A]), next into address A+1 (DB[A+1]). Next the CRC (CRC<15:0>) is shifted in. The instruction ends when nCS goes high.

Write commands must always write a multiple of 4 data bytes. After every fourth data byte, with the falling edge on SCK, the RAM gets written. In case nCS goes high before a multiple of 4 data bytes is received on SDI, the data of the incomplete Word will not be written to RAM.

The CRC is checked at the end of the write access. In case of a CRC mismatch, a CRC interrupt is generated: CRC.CRCERRIF.

If nCS goes high before the last byte of the CRC is shifted in, a CRC interrupt is generated: CRC.FERRIF.

FIGURE 4-11: MESSAGE MEMORY READ WITH CRC INSTRUCTION

nCS Low	0b1011	A<11:0>	N<7:0>	DW[A]				CRC<15:8>	CRC<7:0>	nCS High
				DB[A]	DB[A+1]	DB[A+2]	DB[A+3]			

FIGURE 4-12: MESSAGE MEMORY WRITE WITH CRC INSTRUCTION

nCS Low	0b1010	A<11:0>	N<7:0>	DW[A]				CRC<15:8>	CRC<7:0>	nCS High
				DB[A]	DB[A+1]	DB[A+2]	DB[A+3]			

4.3.7 MESSAGE MEMORY WRITE SAFE WITH CRC - WRITE_SAFE

This instruction ensures that only correct data is written to RAM.

Figure 4-10 illustrates the WRITE_SAFE instruction, while accessing RAM. The instruction starts with nCS going low. The Command (C<3:0> = 0b1100), is followed by the Address (A<11:0>). Afterwards, the data byte is shifted into address A (DB[A]), next into address A+1 (DB[A+1]), A+2 (DB[A+2]), and A+3 (DB[A+3]). Next the CRC (CRC<15:0>) is shifted in. The instruction ends when nCS goes high.

The data word is only written to RAM after the CRC is checked and if it matches.

If the CRC mismatches, the data word is not written to RAM and a CRC Error interrupt is generated: CRC.CRCERRIF.

If nCS goes high before the last byte of the CRC is shifted in, a CRC interrupt is generated: CRC.FERRIF.

FIGURE 4-13: MESSAGE MEMORY WRITE SAFE WITH CRC INSTRUCTION

nCS Low	0b1100	A<11:0>	DW[A]				CRC<15:8>	CRC<7:0>	nCS High
			DB[A]	DB[A+1]	DB[A+2]	DB[A+3]			

5.0 OSCILLATOR

Figure 5-1 shows the block diagram of the oscillator in the MCP2517FD. The oscillator system generates the SYSCLK, which is used in the CAN FD Controller Module and for RAM accesses. It is recommended by the CAN FD community to use either a 40 or 20 MHz SYSCLK.

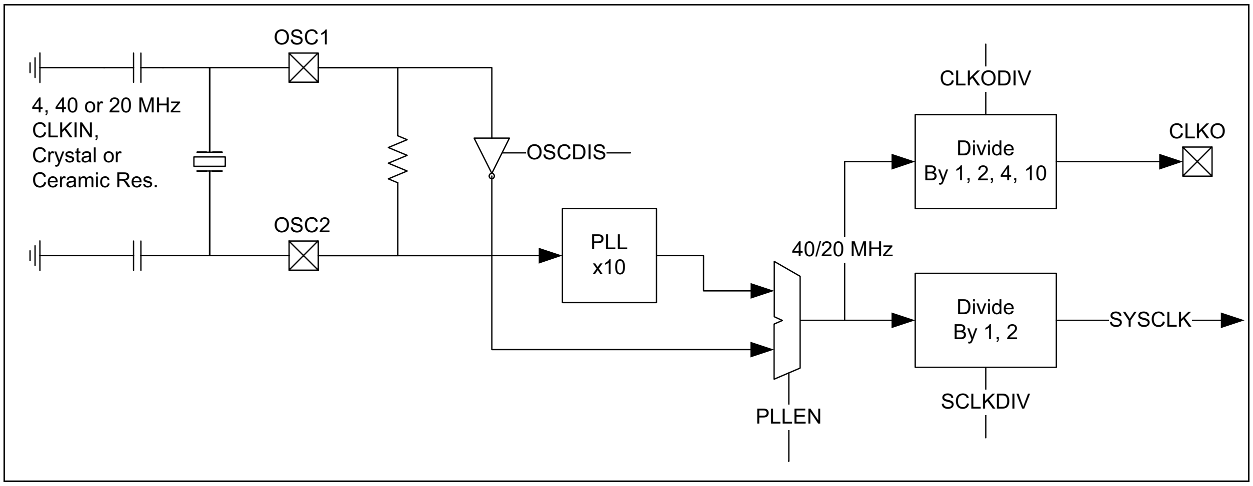
The time reference for clock generation can be an external 40, 20 or 4 MHz crystal, ceramic resonator or external clock.

The OSC register controls the oscillator. The PLL can be enabled to multiply the 4 MHz clock by 10.

The internal 40/20 MHz can be divided by two.

The internally generated clock can be divided and provided on the CLKO pin.

FIGURE 5-1: MCP2517FD OSCILLATOR BLOCK DIAGRAM



6.0 I/O CONFIGURATION

The IOCON register is used to configure the I/O pins:

- CLKO/SOF: select Clock Output or Start of Frame.
- TXCANOD: TXCAN can be configured as Push-Pull or as Open Drain output. Open Drain outputs allows the user to connect multiple controllers together to build a CAN network without using a transceiver.
- $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be configured as GPIO with similar registers as in the PIC microcontrollers or as Transmit and Receive interrupts.
- $\overline{\text{INT0}}$/GPIO0/XSTBY can also be used to automatically control the standby pin of the transceiver.
- INTOD: The interrupt pins can be configured as open-drain or push/pull outputs.

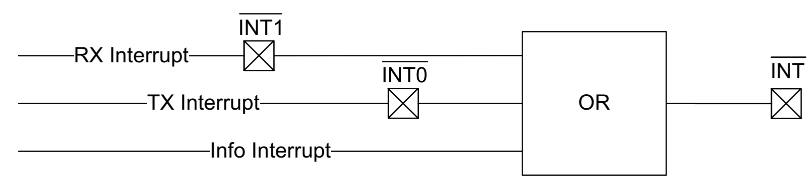
6.1 Interrupt Pins

The MCP2517FD contains three different interrupt pins, see Figure 6-1:

- $\overline{\text{INT}}$ is asserted on any interrupt in the CiINT register (xIF & xIE), including the RX and TX interrupts.
- $\overline{\text{INT1}}$/GPIO1 can be configured as GPIO or RX interrupt pin (CiINT.RXIF & RXIE).
- $\overline{\text{INT0}}$/GPIO0 can be configured as GPIO or TX interrupt pin (CiINT.TXIF & TXIE).

All interrupt pins are active low.

FIGURE 6-1: INTERRUPT PINS



7.0 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings†

V_{DD} .... –0.3V to 6.0V

DC Voltage at all I/O w.r.t GND .... –0.3V to VDD + 0.3V

Virtual Junction Temperature, T_{VJ} (IEC60747-1) .... –40°C to +165°C

Soldering temperature of leads (10 seconds) .... +300°C

ESD protection on all pins (IEC 801; Human Body Model) .... ±4 kV

ESD protection on all pins (IEC 801; Machine Model) .... ±400V

ESD protection on all pins (IEC 801; Charge Device Model) .... ±750V

† **NOTICE:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 7-1: DC CHARACTERISTICS

DC Specifications		Electrical Characteristics: High (H): TAMB = –40°C to +150°C; VDD = 2.7V to 5.5V				
Sym.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
VDD Pin						
VDD	Voltage Range	2.7		5.5	V	RAM data retention guaranteed
VPORH	Power-on Reset Voltage			2.65	V	Highest voltage on VDD before device releases POR
VPORL	Power-on Reset Voltage	2.2			V	Lowest voltage on VDD before device asserts POR
SVDD	VDD Rise Rate to ensure POR	0.05			V/ms	**Note 1**
IDD	Supply Current		15	20	mA	40 MHz SYSCLK, 20 MHz SPI activity
IDDS	Sleep Current		10	60	µA	Clock is stopped TAMB ≤ +85°C (**Note 1**)
				550		Clock is stopped TAMB ≤ +150°C
Digital Input Pins:						
VIH	High-Level Input Voltage	0.7 VDD		VDD + 0.3	V	
VIL	Low-Level Input Voltage	–0.3		0.3 VDD	V	
VOSCPP	OSC1 detection Voltage	0.5			V	Minimum peak-to-peak voltage on OSC1 pin (**Note 1**)
ILI	Input Leakage Current					
	OSC1	–5		+5	µA	
	All other	–1		+1	µA	
Digital Output Pins:						
VOH	High-Level Output Voltage	VDD – 0.7			V	IOH = –2 mA, VDD = 2.7V
VOL	Low-Level Output Voltage					
	TXCAN			0.6	V	IOL = 8 mA, VDD = 2.7V
	All other			0.6	V	IOL = 2 mA, VDD = 2.7V

Note 1: Characterized; not 100% tested.

TABLE 7-2: CLKOUT AND SOF AC CHARACTERISTICS

AC Specifications		Electrical Characteristics: High (H): TAMB = -40°C to +150°C; VDD = 2.7V to 5.5V				
Sym.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
TCLKOH	CLKO Output High	8			ns	@ 40 MHz (**Note 1**)
TCLKOL	CLKO Output Low	8			ns	**Note 1**
TCLKOR	CLKO Output Rise			5	ns	**Note 1**
TCLKOF	CLKO Output Fall			5	ns	**Note 1**
TSOFH	SOF Output High		31 TOSC		ns	**Note 2**
TSOFPD	SOF Propagation Delay: RXCAN falling edge to SOF rising edge		1 TOSC		ns	**Note 2**

Note 1: Characterized; not 100% tested.
2: Design guidance only.

TABLE 7-3: CRYSTAL OSCILLATOR AC CHARACTERISTICS

AC Specifications		Electrical Characteristics: High (H): T_{AMB} = –40°C to +150°C; V_{DD} = 2.7V to 5.5V				
Sym.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
$F_{OSC1,CLKI}$	OSC1 Input Frequency	2	40	40	MHz	External digital clock
$F_{OSC1,4M}$	OSC1 Input Frequency	4 – 0.5%	4	4+0.5%	MHz	4 MHz crystal/resonator (**Note 1**)
F_{DRIFT}	SYSCLK frequency drift			10	ppm	Additional frequency drift of SYSCLK due to internal PLL @ 4 MHz (**Note 1**)
$F_{OSC1,20M}$	OSC1 Input Frequency	20 – 0.5%	20	20+0.5%	MHz	20 MHz crystal/resonator (**Note 1**)
$F_{OSC1,40M}$	OSC1 Input Frequency	40 – 0.5%	40	40+0.5%	MHz	40 MHz crystal/resonator (**Note 1**)
T_{OSC1}	T_{OSC1}=1/$F_{OSC1,x}$	25			ns	
T_{OSC1H}	OSC1 Input High	0.45 * T_{OSC}		0.55 * T_{OSC}	ns	**Note 1**
T_{OSC1L}	OSC1 Input Low	0.45 * T_{OSC}		0.55 * T_{OSC}	ns	**Note 1**
T_{OSC1R}	OSC1 Input Rise			20	ns	**Note 2**
T_{OSC1F}	OSC1 Input Fall			20	ns	**Note 2**
DC_{OSC1}	Duty Cycle on OSC1	45	50	55	%	External clock duty cycle requirement (**Note 1**)
$T_{OSCSTAB}$	Oscillator stabilization period			3	ms	From POR to final frequency (**Note 1**)
$T_{OSCSLEEP}$	Oscillator stabilization from Sleep			3	ms	From Sleep to final frequency (**Note 1**)
$G_{M,4M}$	Transconductance	1470		2210	µA/V	4 MHz crystal (**Note 2**)
$G_{M,40M}$	Transconductance	2040		3060	µA/V	40 MHz crystal (**Note 2**)

Note 1: Characterized; not 100% tested.
2: Design guidance only.

TABLE 7-4: CAN BIT RATE

AC Specifications		Electrical Characteristics: High (H): T_{AMB} = –40°C to +150°C; V_{DD} = 2.7V to 5.5V				
Sym.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
BR_{NOM}	Nominal Bit Rate	0.125	0.5	1	Mbps	
BR_{DATA}	Data Bit Rate	0.5	2	8	Mbps	$BR_{DATA} \geq BR_{NOM}$

Note 1: Tested bit rates. Device allows the configuration of more bit rates, including slower bit rates than the minimum stated.

TABLE 7-5: CAN RX FILTER AC CHARACTERISTICS

AC Specifications		Electrical Characteristics: High (H): TAMB = –40°C to +150°C; VDD = 2.7V to 5.5V				
Sym.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
TPROP	Filter propagation delay		1		ns	Note 2
TFILTER	Filter time (Note 3)	40 70 125 225		75 120 215 390	ns	T00FILTER T01FILTER T10FILTER T11FILTER
TREVO-CERY	Minimum high time on input for output to go high again	5			ns	Note 2

Note 1: Characterized; not 100% tested.
2: Design guidance only.
3: Pulses on RXCAN shorter than the minimum TFILTER time will be ignored; pulses longer than the maximum TFILTER time will wake-up the device.

TABLE 7-6: SPI AC CHARACTERISTICS

AC Specifications			Electrical Characteristics: High (H): TAMB = –40°C to +150°C; VDD = 2.7V to 5.5V				
Param.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
	FSCK	SCK Input Frequency			20	MHz	Note 3
	TSCK	SCK Period, TSCK=1/FSCK	50			ns	Note 3
1	TSCKH	SCK High Time	20			ns	
2	TSCKL	SCK Low Time	20			ns	
3	TSCKR	SCK Rise Time			100	ns	Note 2
4	TSCKF	SCK Fall Time			100	ns	Note 2
5	TCS2SCK	nCS ↓ to SCK ↑	TSCK/2			ns	
6	TSCK2CS	SCK ↑ to nCS ↑	TSCK			ns	
7	TSDI2SCK	SDI Setup: SDI ↕ to SCK ↑	5			ns	
8	TSCK2SDI	SDI Hold: SCK ↑ to SDI ↕	5			ns	
9	TSCK2SDO	SDO Valid: SCK ↓ to SDO ↕			20	ns	CLOAD = 50 pF
10	TCS2SDOZ	SDO High Z: nCS ↑ to SDO Z			2 TSCK	ns	CLOAD = 50 pF
11	TCSD	nCS ↑ to nCS ↓	TSCK			ns	Note 2

Note 1: Characterized; not 100% tested.
2: Design guidance only.
3: FSCK must be less than or equal to FSYSCLK/2.

FIGURE 7-1: SPI I/O TIMING

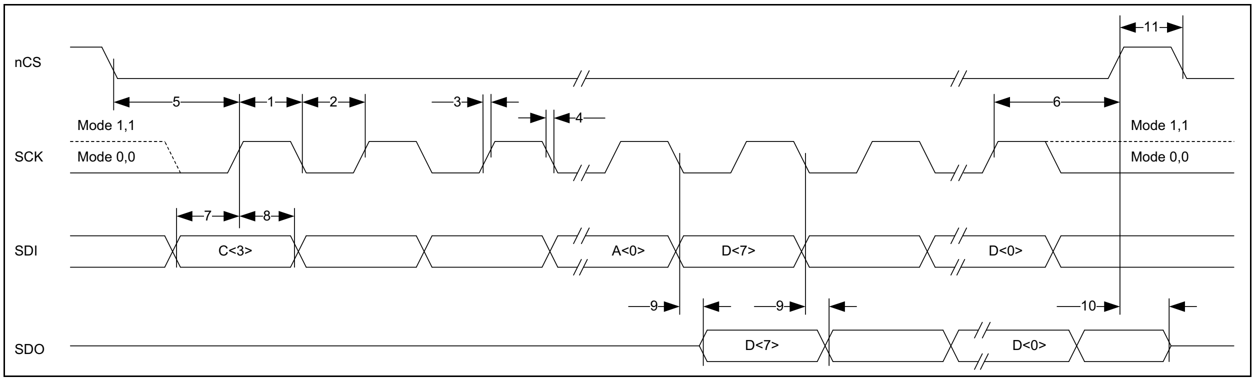


TABLE 7-7: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	–40		+150	°C	
Storage Temperature Range	T_A	–55		+150	°C	
Thermal Package Resistance						
Thermal Resistance for SOIC-14	θ_{JA}	—	+149.5	—	°C/W	
Thermal Resistance for DFN-14	θ_{JA}	—	+64.1	—	°C/W	

NOTES:

8.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

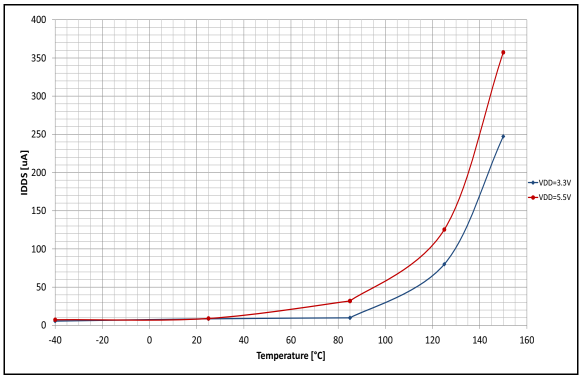


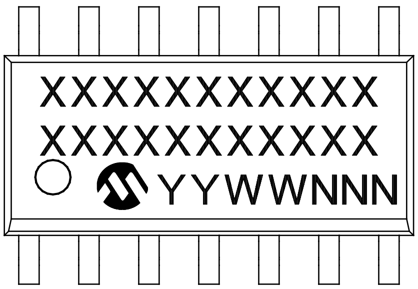
FIGURE 8-1: *Average IDDS vs. Temperature*

NOTES:

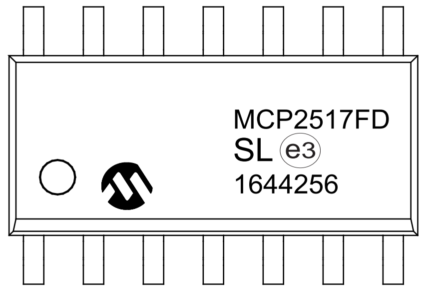
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

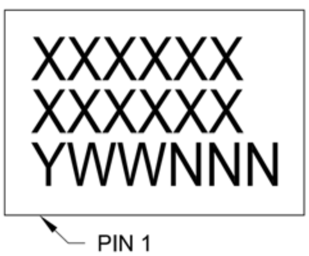
14-Lead SOIC



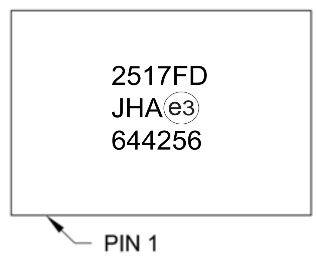
Example:



14-Lead VDFN



Example:

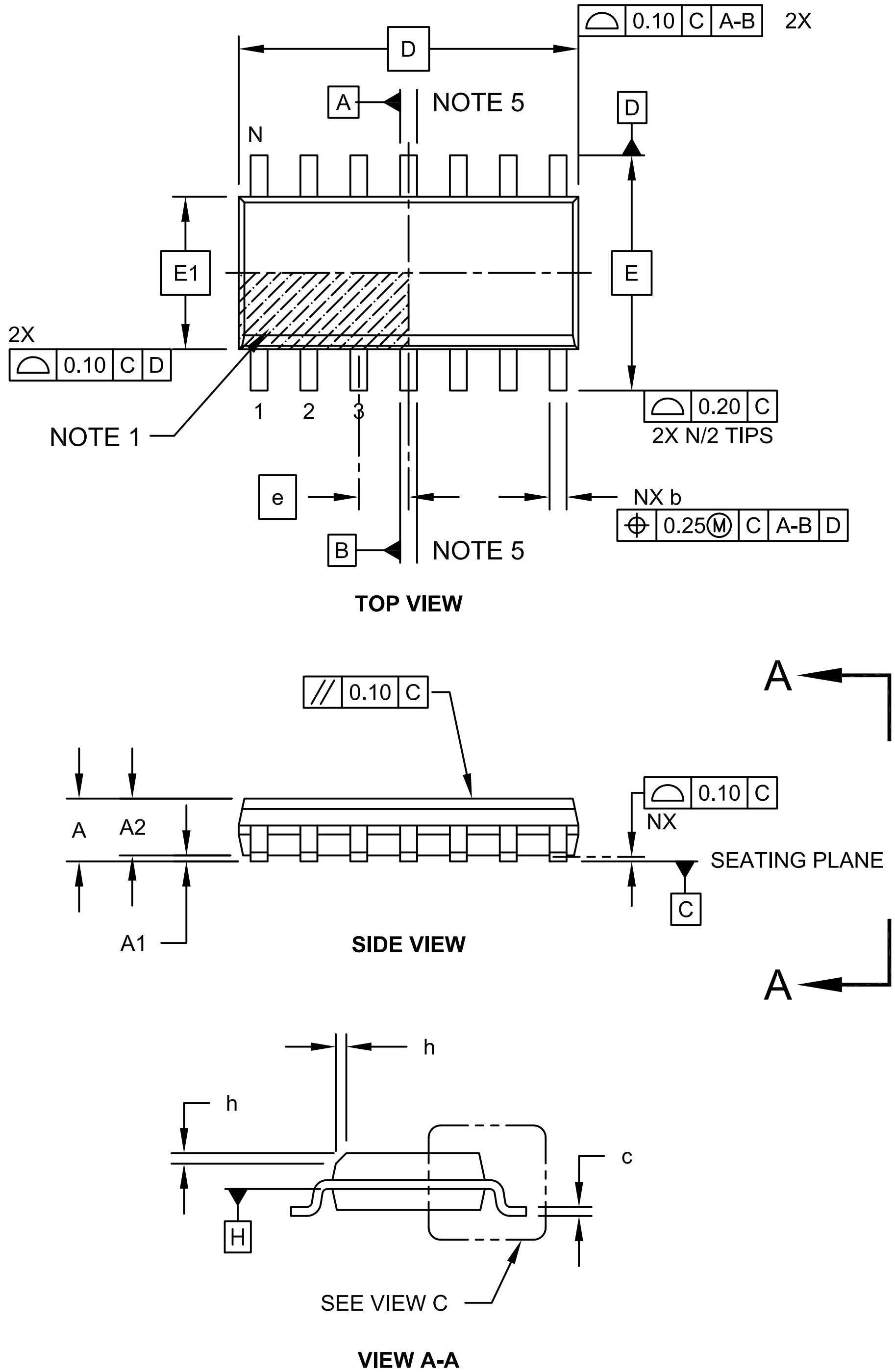


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

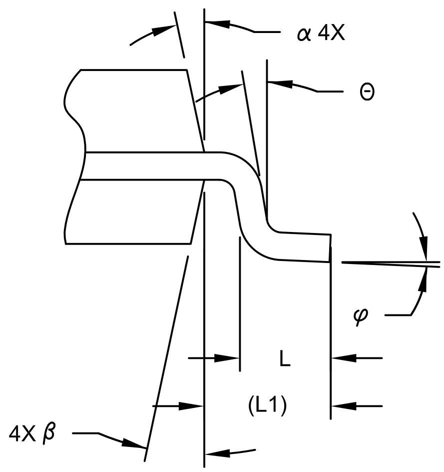
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



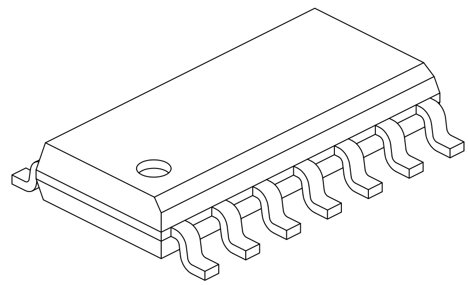
Microchip Technology Drawing No. C04-065C Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

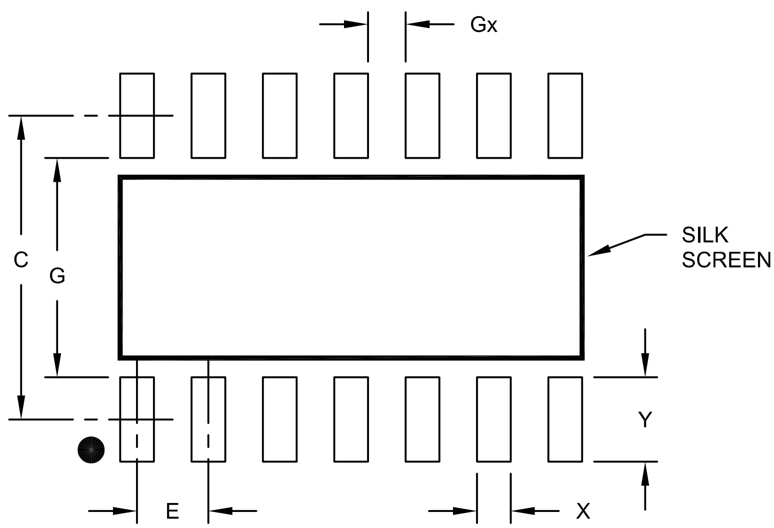
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

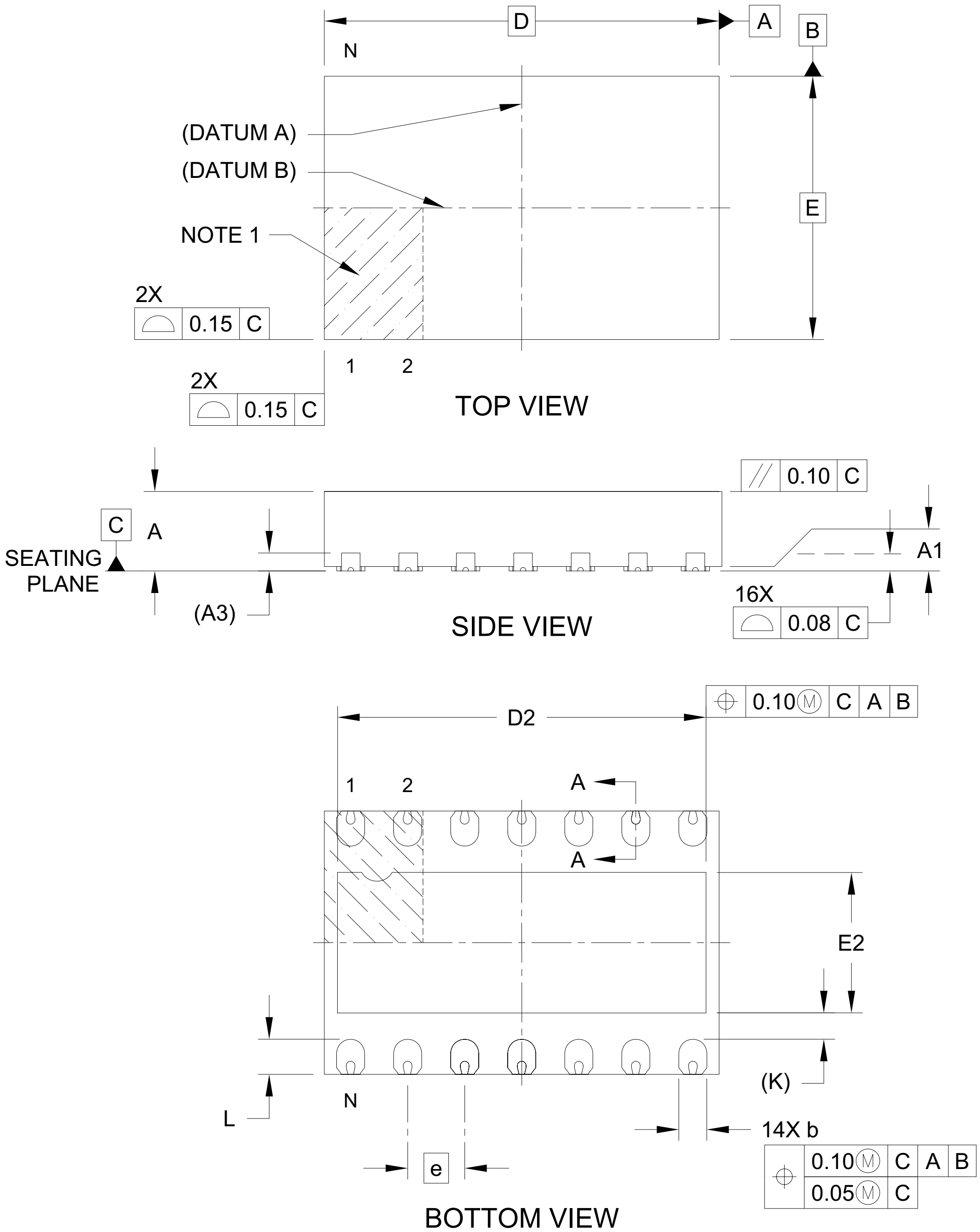
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Very Thin Plastic Quad Flat, No Lead Package (JHA) - 4.5x3.0 mm Body [VDFN] With Dimpled Wettable Flanks

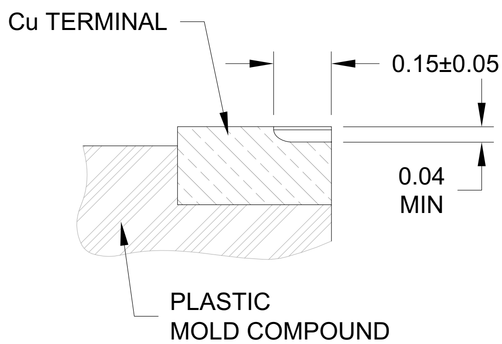
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



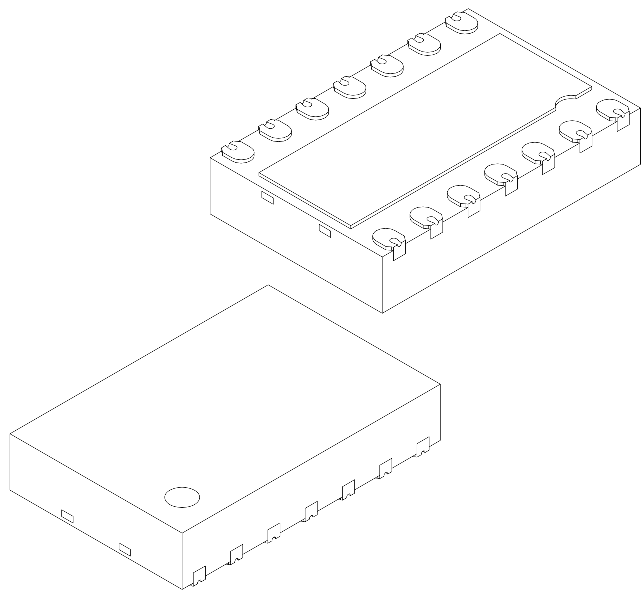
Microchip Technology Drawing C04-1198A Sheet 1 of 2

14-Lead Very Thin Plastic Quad Flat, No Lead Package (JHA) - 4.5x3.0 mm Body [VDFN] With Dimpled Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		4.50 BSC	
Exposed Pad Length	D2	4.15	4.20	4.25
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.55	1.60	1.65
Terminal Width	b	0.29	0.32	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.30 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

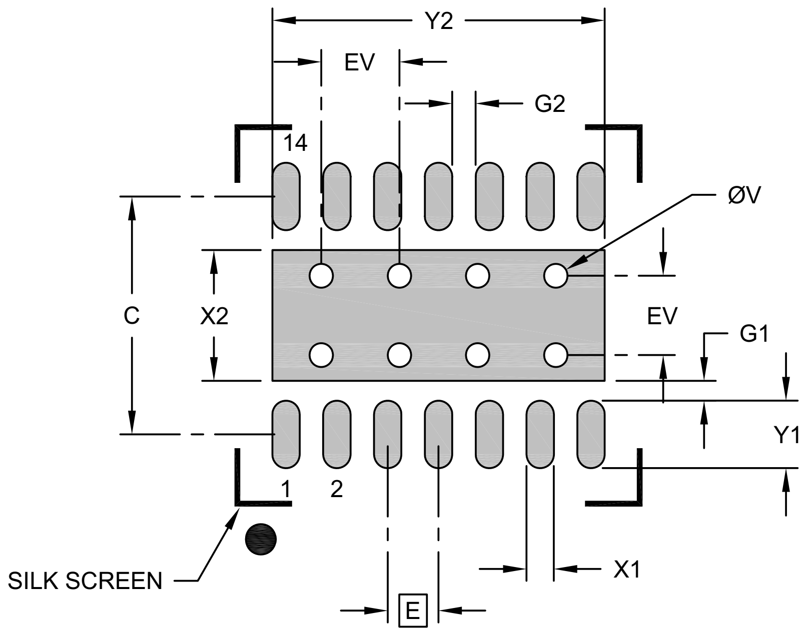
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1198A Sheet 2 of 2

14-Lead Very Thin Plastic Quad Flat, No Lead Package (JHA) - 4.5x3.0 mm Body [VDFN] With Dimpled Wettable Flanks

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			1.65
Optional Center Pad Length	Y2			4.25
Contact Pad Spacing	C		3.00	
Contact Pad Width (X14)	X1			0.35
Contact Pad Length (X14)	Y1			0.85
Contact Pad to Center Pad (X14)	G1	0.25		
Spacing Between Contacts (X12)	G1	0.30		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3198A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (May 2018)

The following is the list of modifications:

1. Updated the Active Current value in the **Features** section.
2. Updated **Register 3-28**, **Register 3-29** and **Register 3-32**.
3. Updated **Section 6.1 "Interrupt Pins"**.
4. Updated **Table 7-4**.

Revision A (August 2017)

- Original Release of this Document.

NOTES:

APPENDIX B: CAN FD CONFORMANCE

The MCP2517FD passed the CAN FD conformance tests specified in ISO 16845-1:2016.

ISO 11898-1:2015 lists non-mandatory features. Table B-1 clarifies which optional features are implemented.

TABLE B-1: ISO OPTIONAL FEATURES

No.	Optional Feature	Implemented
1	FD frame format	Yes
2	Disabling of frame formats	Yes. Classical CAN frame format.
3	Limited LLC frames	No. Full range of IDs and DLCs implemented.
4	No transmission of frames including padding bytes	N/A. See No. 3.
5	LLC Abort interface	Yes
6	ESI and BRS bit values	Yes
7	Method to provide MAC data consistency	Yes
8	Time and time triggering	Start of Frame output.
9	Time stamping	Yes. 32 bit TBC.
10	Bus monitoring mode	Yes
11	Handle	Yes
12	Restricted operation	Yes
13	Separate prescalers for nominal bits and for data bits	Yes
14	Disabling of automatic retransmission	Yes
15	Maximum number of retransmissions	Yes. One, 3, or unlimited.
16	Disabling of protocol exception event on res bit detected recessive	Yes. Selectable.
17	PCS_Status	No
18	Edge filtering during the bus integration state	Yes. Selectable.
19	Time resolution for SSP placement	Yes. 128 TQ. Measured, manual or disabled.
20	FD_T/R message	TX and RX interrupts.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][(1)]	–X	/XX
Device	Tape and Reel	Temperature Range	Package

Device:	MCP2517FD: CAN FD Controller
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel [(1)]
Temperature Range:	H = -40°C to +150°C (High)
Package:	SL = Plastic SOIC (150 mil Body), 14-Lead JHA = Plastic VDFN (4.5x3 mm Body), 14-Lead with Dimpled Wettable Flanks

Examples:

a) MCP2517FD-H/SL: High Temperature, Plastic SOIC (150 mil Body), 14-Lead

b) MCP2517FDT-H/SL: Tape and Reel, High Temperature, Plastic SOIC (150 mil Body), 14-Lead

c) MCP2517FD-H/JHA: High Temperature, VDFN (4.5x3 mm Body), 14-Lead with Dimpled Wettable Flanks

d) MCP2517FDT-H/JHA: Tape and Reel, High Temperature, VDFN (4.5x3 mm Body), 14-Lead with Dimpled Wettable Flanks

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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