MCP33151/41-XX

1 Msps/500 ksps, 14/12-Bit Single-Ended Input SAR ADC

Features

- Sample Rate (Throughput):
  - MCP33151/41-10: 1 Msps
  - MCP33151/41-05: 500 ksps
- 14/12-Bit Resolution with No Missing Codes
- No Latency Output
- Wide Operating Voltage Range:
  - Analog supply voltage (AV_{DD}): 1.8V
  - Digital input/output interface voltage (DV_{IO}): 1.7 - 5.5V
  - External reference (V_{REF}): AV_{DD}-5.1V
- Pseudodifferential Input Operation with Single-Ended Configuration:
  - Input full-scale range: 0V to +V_{REF}
- Ultra-Low Current Consumption (typical):
  - During input acquisition (standby): ~1.5 µA
  - During conversion:

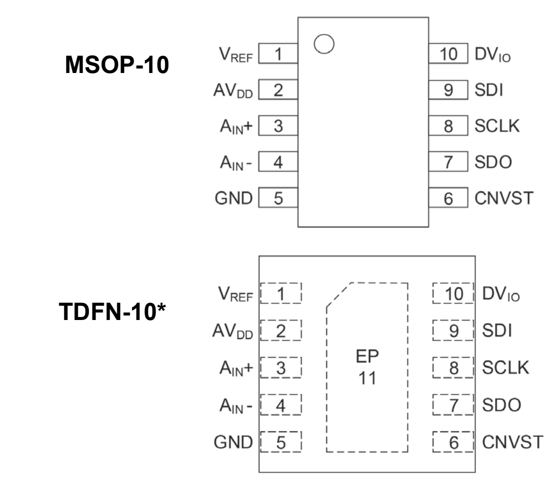
    MCP33151/41-10: ~0.66 mA

    MCP33151/41-05: ~0.33 mA
- SPI-Compatible Serial Communication:
  - SCLK clock rate: up to 100 MHz
- 3-Wire with Optional BUSY Indicator
- ADC Self-Calibration for Offset, Gain, and Linearity Errors:
  - During power-up (automatic)
  - On-Demand via user's command during normal operation
- Built-In Data Accumulator
  - Integrate up to 1024 consecutive converted samples
  - Increase ENOB up to 18 bits by automatically averaging conversion results
- AEC-Q100 Qualified:
  - Temperature grade 1: -40°C to +125°C
- Package Options: MSOP-10 and TDFN-10

Typical Applications

- High-Precision Data Acquisition
- Medical Instruments
- Test Equipment
- Electric Vehicle Battery Management Systems
- Motor Control Applications
- Switch-Mode Power Supply Applications
- Battery-Powered Equipment

Package Types



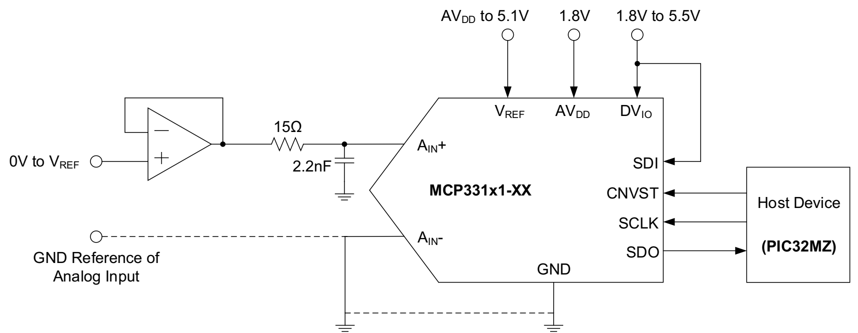
* Includes Exposed Thermal Pad (EP); see Table 4-1.

MCP331X1-XX Device Offering (Note 1)

Part Number	Resolution	Sample Rate	Input Type	Input Range	Performance (Typical)				
					SNR (dBFS)	SFDR (dB)	THD (dB)	INL (LSB)	DNL (LSB)
MCP33151-10	14-bit	1 Msps	Single-Ended	0V to 5.1V	80.4	103.9	-102.5	±0.39	±0.11
MCP33141-10	12-bit	1 Msps	Single-Ended	0V to 5.1V	73.3	102.0	-100.4	±0.09	±0.05
MCP33151-05	14-bit	500 kSPS	Single-Ended	0V to 5.1V	80.4	102.7	-100.9	±0.39	±0.11
MCP33141-05	12-bit	500 kSPS	Single-Ended	0V to 5.1V	73.3	99.9	-99.2	±0.09	±0.05

Note 1: SNR, SFDR, and THD are measured with f_{IN} = 10 kHz, V_{IN} = -1 dBFS, V_{REF} = 5.1V.

Typical Application Diagram



Description

The MCP33151/41-10 and MCP33151/41-05 are single-ended, 14-bit and 12-bit, single-channel 1 Msps and 500 kSPS ADC family devices, respectively, featuring low-power consumption and high performance, using a successive approximation register (SAR) architecture.

The device operates with an external voltage reference (V_{REF}) from AV_{DD} to 5.1V, which supports a wide range of input full-scale range from 0V to V_{REF}. The reference voltage setting is independent of the analog supply voltage (AV_{DD}) and is higher than AV_{DD}. The conversion output is available through an easy-to-use simple SPI-compatible 3-wire interface.

The device requires a 1.8V analog supply voltage (AV_{DD}) and a 1.7V to 5.5V digital I/O interface supply voltage (DV_{IO}). The wide digital I/O interface supply (DV_{IO}) range (1.7V-5.5V) allows the device to interface with most host devices (Master) available in the current industry, such as the PIC32 microcontrollers, without using external voltage level shifters.

Once all supply voltages are connected, the device will power-up and perform an automatic calibration to minimize offset, gain and linearity errors. The automatic calibration takes place approximately 40 ms following power-up, and it is necessary to ensure that all power supplies are fully settled and stable after this time. See **Section 4.1.1, Power-Up Sequence and Auto-Calibration** for more details. The device performance stays stable across the specified temperature range. However, when extreme changes in the operating environment, such as in the reference voltage, are made with respect to the initial conditions (e.g. the reference voltage did not fully settle during the initial power-up sequence), the user may send a recalibrate command anytime to initiate another self-calibration to restore optimum performance.

When the initial power-up sequence is completed, the device enters a low-current input acquisition mode, where sampling capacitors are connected to the input pins. This mode is called Standby.

During Standby mode, most of the internal analog circuitry is shut down in order to reduce current consumption. Typically, the device consumes approximately 1.5 µA during Standby. A new conversion is started on the rising edge of CNVST. When the conversion is complete and the host lowers CNVST, the output data is presented on SDO, and the device enters Standby mode to begin acquiring the next input sample. The user can clock out the ADC output data using the SPI-compatible serial clock during Standby.

The ADC system clock is generated by an internal on-chip clock, therefore the conversion is performed independent of the SPI serial clock (SCLK).

This device can be used for various high-speed and high-accuracy analog-to-digital data conversion applications, where design simplicity, low power, and no output latency are needed.

The device is AEC-Q100 qualified for automotive applications and operates over the extended temperature range of -40°C to +125°C. The available package options are Pb-free TDFN-10 and MSOP-10.

1.0 KEY ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings†

External Analog Supply Voltage (AV_{DD}) .... -0.3V to 2.0V
External Digital Supply Voltage (DV_{IO}).......... -0.3V to 5.8V
External Reference Voltage (V_{REF}).......... -0.3V to 5.8V
Analog Inputs w.r.t GND .... -0.3V to V_{REF} + 0.3V
Current at Input Pins ....±2 mA
Current at Output and Supply Pins ....±250 mA
Storage Temperature ....-65°C to +150°C
Maximum Junction Temperature (T_J) .... +150°C
ESD Protection on all Pins ....≤4 kV HBM, ≤2 kV CDM

†Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.2 Electrical Specifications

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Analog Input (V_{IN}) = -1 dBFS sine wave, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF, +25°C is applied for typical values.
MCP331X1-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP331X1-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Requirements						
Analog Supply Voltage Range	AV_{DD}	1.7	1.8	1.9	V	Note 3
Digital Input/Output Interface Voltage Range	DV_{IO}	1.7	—	5.5	V	Note 3
Analog Supply Current at AV_{DD} Pin:						
During Conversion	I_{DDAN}	—	660	900	µA	f_s = 1 Msps (MCP331X1-10)
		—	330	600	µA	f_s = 500 ksps (MCP331X1-05)
During Standby	I_{DDAN_STBY}	—	1.5	—	µA	During input acquisition (t_{ACQ})
Average Digital Supply Current At DV_{IO} Pin:						
During Data Transfer	I_{IO_DATA}	—	400	—	µA	f_s = 1 Msps (MCP33151-10)
		—	343	—	µA	f_s = 1 Msps (MCP33141-10)
		—	200	—	µA	f_s = 500 ksps (MCP33151-05)
		—	171	—	µA	f_s = 500 ksps (MCP33141-05)
During Standby	I_{IO_STBY}	—	120	—	nA	During input acquisition (t_{ACQ})

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: Decoupling capacitor is recommended on the following pins:
(a) AV_{DD} pin: 1 µF ceramic capacitor, (b) DV_{IO} pin: 0.1 µF ceramic capacitor, (c) V_{REF} pin: 10 µF tantalum capacitor.
4: PSRR (dB) = -20 log (D_{VOUT}/AV_{DD}), where D_{VOUT} = change in conversion result.
5: ENOB = (SINAD – 1.76)/6.02

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Analog Input (V_{IN}) = -1 dBFS sine wave, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF, +25°C is applied for typical values. MCP331X1-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz. MCP331X1-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
External Reference Voltage Input						
Reference Voltage	V_{REF}	AV_{DD}	—	5.1	V	Note 2, Note 3
Reference Load Current at V_{REF} Pin:						
During Conversion	I_{REF}	—	220	290	µA	f_s = 1 Msps (MCP331X1-10)
		—	110	180	µA	f_s = 500 ksps (MCP331X1-05)
During Standby	I_{REF_STBY}	—	40	—	nA	During input acquisition (t_{ACQ})
Total Power Consumption (Including AV_{DD}, DV_{IO}, V_{REF} Pins)						
MCP331X1-10						
at 1 Msps	P_{DISS_TOTAL}	—	3.6	—	mW	Averaged power for t_{ACQ} + t_{CNV}
at 500 ksps		—	1.8	—	mW	
at 100 ksps		—	0.4	—	mW	
During Standby	P_{DISS_STBY}	—	3.3	—	µW	During input acquisition (t_{ACQ})
MCP331X1-05						
at 500 ksps	P_{DISS_TOTAL}	—	1.8	—	mW	Averaged power for t_{ACQ} + t_{CNV}
at 100 ksps		—	0.4	—	mW	
During Standby	P_{DISS_STBY}	—	3.3	—	µW	During input acquisition (t_{ACQ})
Analog Inputs						
Input Voltage Range	V_{IN+}	-0.1	—	V_{REF} + 0.1	V	Note 2
Input Full-Scale Voltage Range	FSR	0	—	$+V_{REF}$	V_{PP}	Note 2
Input Sampling Capacitance	C_S	—	10	—	pF	Note 1
-3 dB Input Bandwidth	BW_{-3dB}	—	45	—	MHz	Note 1
Aperture Delay		—	2.5	—	ns	Time delay between CNVST rising edge and when input is sampled, Note 1
Leakage Current at Analog Input Pin	$I_{LEAK\_AN\_INPUT}$	—	±2.2	±200	nA	During input acquisition (t_{ACQ})
System Performance						
Sample Rate (Throughput Rate)	f_s	—	—	1	Msps	MCP331X1-10
		—	—	500	ksps	MCP331X1-05
Resolution (No Missing Codes)		14	—	—	Bits	MCP33151-10 and MCP33151-05
		12	—	—	Bits	MCP33141-10 and MCP33141-05

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: Decoupling capacitor is recommended on the following pins:
(a) AV_{DD} pin: 1 µF ceramic capacitor, (b) DV_{IO} pin: 0.1 µF ceramic capacitor, (c) V_{REF} pin: 10 µF tantalum capacitor.
4: PSRR (dB) = -20 log (D_{VOUT}/AV_{DD}), where D_{VOUT} = change in conversion result.
5: ENOB = (SINAD – 1.76)/6.02

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Analog Input (V_{IN}) = -1 dBFS sine wave, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF, +25°C is applied for typical values.
MCP331X1-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP331X1-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Integral Nonlinearity	INL	-1.5	±0.39	+1.5	LSB	MCP33151-10 and MCP33151-05
		—	±0.09	—	LSB	MCP33141-10 and MCP33141-05
Differential Nonlinearity	DNL	-0.8	±0.11	+0.8	LSB	MCP33151-10 and MCP33151-05
		-0.3	±0.05	+0.3	LSB	MCP33141-10 and MCP33141-05
Offset Error		-1.62	±0.4	+1.62	mV	MCP33151-10 and MCP33151-05
		-1.33	±0.4	+1.33	mV	MCP33141-10 and MCP33141-05
Offset Error Drift with Temperature		—	±0.1	—	µV/°C	
Gain Error	G_{ER}	—	±2	—	LSB	MCP33151-10 and MCP33151-05
		—	±0.5	—	LSB	MCP33141-10 and MCP33141-05
Gain Error Drift with Temperature		—	±8	—	µV/°C	
Input Common-mode Rejection Ratio	CMRR	—	84	—	dB	
Power Supply Rejection Ratio	PSRR	—	75	—	dB	(**Note 4**)
Dynamic Performance						
Signal-to-Noise Ratio	SNR	**MCP33151-10 and MCP33151-05: 14-bit ADC**				
		—	80.4	—	dBFS	V_{REF} = 5V, f_{IN} = 1 kHz
		—	73.5	—		V_{REF} = 1.8V, f_{IN} = 1 kHz
		78.7	80.4	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	73.5	—		V_{REF} = 1.8V, f_{IN} = 10 kHz
		MCP33141-10 and MCP33141-05: 12-bit ADC				
		—	73.3	—	dBFS	V_{REF} = 5V, f_{IN} = 1 kHz
		—	70.9	—		V_{REF} = 1.8V, f_{IN} = 1 kHz
		72.8	73.3	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	70.8	—		V_{REF} = 1.8V, f_{IN} = 10 kHz

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: Decoupling capacitor is recommended on the following pins:
(a) AV_{DD} pin: 1 µF ceramic capacitor, (b) DV_{IO} pin: 0.1 µF ceramic capacitor, (c) V_{REF} pin: 10 µF tantalum capacitor.
4: PSRR (dB) = -20 log (D_{VOUT}/AV_{DD}), where D_{VOUT} = change in conversion result.
5: ENOB = (SINAD – 1.76)/6.02

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Analog Input (V_{IN}) = -1 dBFS sine wave, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF, +25°C is applied for typical values.
MCP331X1-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP331X1-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Signal-to-Noise and Distortion Ratio (Note 5)	SINAD	**MCP33151-10 and MCP33151-05: 14-bit ADC**				
		—	80.4	—	dBFS	V_{REF} = 5V, f_{IN} = 1 kHz
		—	73.6	—		V_{REF} = 1.8V, f_{IN} = 1 kHz
		—	80.3	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	73.3	—		V_{REF} = 1.8V, f_{IN} = 10 kHz
		MCP33141-10 and MCP33141-05: 12-bit ADC				
		—	73.3	—	dBFS	V_{REF} = 5V, f_{IN} = 1 kHz
		—	70.9	—		V_{REF} = 1.8V, f_{IN} = 1 kHz
		—	73.3	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	70.8	—		V_{REF} = 1.8V, f_{IN} = 10 kHz
Spurious Free Dynamic Range	SFDR	**MCP33151-10 and MCP33151-05: 14-bit ADC**				
		—	103.5	—	dBc	V_{REF} = 5V, f_{IN} = 1 kHz
		—	101.3	—		V_{REF} = 1.8V, f_{IN} = 1 kHz
		—	103.7	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	98.1	—		V_{REF} = 1.8V, f_{IN} = 10 kHz
		MCP33141-10 and MCP33141-05: 12-bit ADC				
		—	101.0	—	dBc	V_{REF} = 5V, f_{IN} = 1 kHz
		—	98.8	—		V_{REF} = 1.8V, f_{IN} = 1 kHz
		—	101.4	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	97.5	—		V_{REF} = 1.8V, f_{IN} = 10 kHz
Total Harmonic Distortion (first five harmonics)	THD	**MCP33151-10 and MCP33151-05: 14-bit ADC**				
		—	-102.0	—	dBc	V_{REF} = 5V, f_{IN} = 1 kHz
		—	-97.0	—		V_{REF} = 1.8V, f_{IN} = 1 kHz
		—	-101.5	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	-95.5	—		V_{REF} = 1.8V, f_{IN} = 10 kHz
		MCP33141-10 and MCP33141-05: 12-bit ADC				
		—	-98.9	—	dBc	V_{REF} = 5V, f_{IN} = 1 kHz
		—	-95.0	—		V_{REF} = 1.8V, f_{IN} = 1 kHz
		—	-98.6	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	-94.5	—		V_{REF} = 1.8V, f_{IN} = 10 kHz
System Self-Calibration						
Self-Calibration Time	t_{CAL}	—	500	650	ms	Note 2
Number of SCLK Clocks for Recalibrate Command	$ReCal_{NSCLK}$	—	1024	—	clocks	Includes clocks for data bits
Serial Interface Timing Information, see						

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: Decoupling capacitor is recommended on the following pins:
(a) AV_{DD} pin: 1 µF ceramic capacitor, (b) DV_{IO} pin: 0.1 µF ceramic capacitor, (c) V_{REF} pin: 10 µF tantalum capacitor.
4: PSRR (dB) = -20 log (D_{VOUT}/AV_{DD}), where D_{VOUT} = change in conversion result.
5: ENOB = (SINAD – 1.76)/6.02

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Analog Input (V_{IN}) = -1 dBFS sine wave, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF, +25°C is applied for typical values.
MCP331X1-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP331X1-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Digital Inputs/Outputs						
High-Level Input Voltage	V_{IH}	0.7 x DV_{IO}	—	DV_{IO} + 0.3	V	$DV_{IO} \geq$ 2.3V
		0.9 x DV_{IO}	—	DV_{IO} + 0.3	V	DV_{IO} < 2.3V
Low-Level Input Voltage	V_{IL}	-0.3	—	0.3 x DV_{IO}	V	$DV_{IO} \geq$ 2.3V
		-0.3	—	0.2 x DV_{IO}	V	DV_{IO} < 2.3V
Hysteresis of Schmitt Trigger Inputs	V_{HYST}	—	0.2 x DV_{IO}	—	V	All digital inputs
Low-Level Output Voltage	V_{OL}	—	—	0.2 x DV_{IO}	V	I_{OL} = 500 µA (source)
High-Level Output Voltage	V_{OH}	0.8 x DV_{IO}	—	—	V	I_{OH} = - 500 µA (sink)
Input Leakage Current	I_{LI}	—	—	±1	µA	CNVST/SDI/SCLK = GND or DV_{IO}
Output Leakage Current	I_{LO}	—	—	±1	µA	Output is high-Z, SDO = GND or DV_{IO}
Internal Capacitance (all digital inputs and outputs)	C_{INT}	—	7	—	pF	T_A = +25°C (**Note 1**)

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: Decoupling capacitor is recommended on the following pins:
(a) AV_{DD} pin: 1 µF ceramic capacitor, (b) DV_{IO} pin: 0.1 µF ceramic capacitor, (c) V_{REF} pin: 10 µF tantalum capacitor.
4: PSRR (dB) = -20 log (D_{VOUT}/AV_{DD}), where D_{VOUT} = change in conversion result.
5: ENOB = (SINAD – 1.76)/6.02

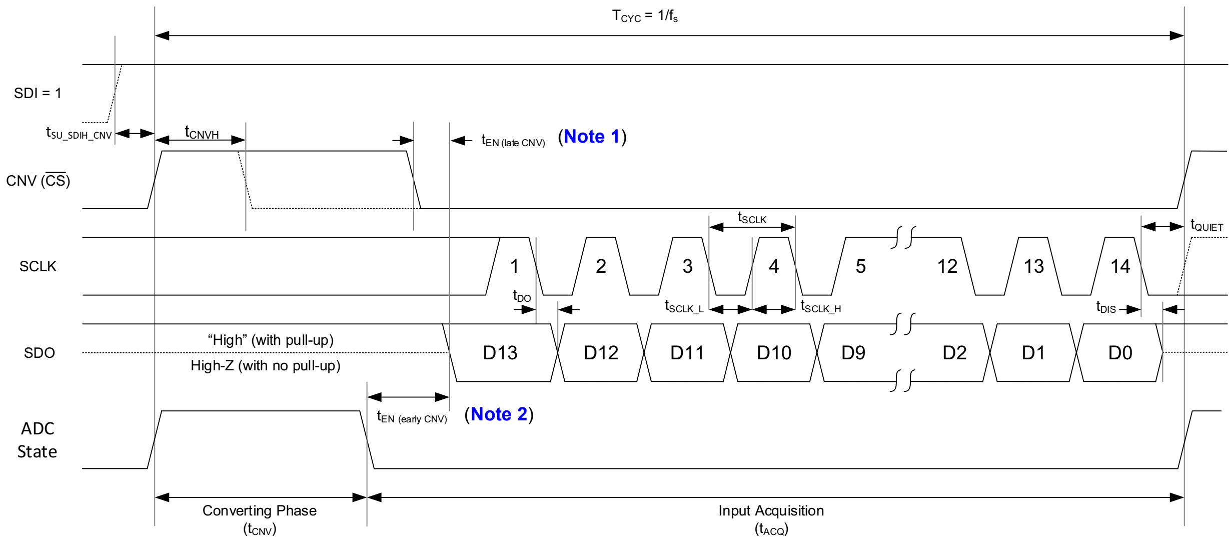
TABLE 1-2: SERIAL INTERFACE TIMING SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, GND = 0V,
Analog Input (A_{IN}) = -1 dBFS sine wave, Resolution = 16-bit (MCP33151-10), f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF, +25°C is applied for typical values. All timings are measured at 50%. See Figure 2.0 for timing diagram.

- MCP331X1-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
- MCP331X1-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Serial Clock Frequency	f_{SCLK}	—	—	100	MHz	See t_{SCLK} specification
SCLK Period	t_{SCLK}	10	—	—	ns	DV_{IO} ≥ 3.3V, f_{SCLK} = 100 MHz (Max.)
		12	—	—	ns	DV_{IO} ≥ 2.3V, f_{SCLK} = 83.3 MHz (Max.)
		16	—	—	ns	DV_{IO} ≥ 1.7V, f_{SCLK} = 62.5 MHz (Max.)
SCLK Low Time	t_{SCLK_L}	3	—	—	ns	DV_{IO} ≥ 2.3V
		4.5	—	—	ns	DV_{IO} ≥ 1.7V
SCLK High Time	t_{SCLK_H}	3	—	—	ns	DV_{IO} ≥ 2.3V
		4.5	—	—	ns	DV_{IO} ≥ 1.7V
Output Valid from SCLK Low	t_{DO}	—	—	10	ns	DV_{IO} ≥ 3.3V
		—	—	12	ns	DV_{IO} ≥ 2.3V
		—	—	16	ns	DV_{IO} ≥ 1.7V
Quiet Time	t_{QUIET}	10	—	—	ns	**Note 2**
3-Wire Operation:						
SDI Valid Setup Time	$t_{SU\_SDIH\_CNV}$	5	—	—	ns	SDI High to CNVST Rising Edge
CNVST Pulse Width High Time	t_{CNVH}	10	—	—	ns	
Output Enable Time	t_{EN}	—	—	10	ns	DV_{IO} ≥ 2.3V
		—	—	15	ns	DV_{IO} ≥ 1.7V
Output Disable Time	t_{DIS}	—	—	15	ns	**Note 2**
MCP331X1-10						
Sample Rate	f_s	—	—	1	Msps	Throughput rate
Input Acquisition Time (**Note 2**)	t_{ACQ}	250	490	—	ns	
Data Conversion Time	t_{CNV}	—	510	750	ns	
Time Between Conversions	t_{CYC}	1	—	—	µs	$t_{CYC} = t_{ACQ} + t_{CNV}$, f_S = 1 Msps
MCP331X1-05						
Sample Rate	f_s	—	—	500	ksps	Throughput rate
Input Acquisition Time (**Note 2**)	t_{ACQ}	600	800	—	ns	
Data Conversion Time	t_{CNV}	—	1200	1400	ns	
Time Between Conversions	t_{CYC}	2	—	—	µs	$t_{CYC} = t_{ACQ} + t_{CNV}$, f_S = 500 ksps

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.



Note 1: t_{EN} when CNVST is lowered before t_{CNV} (MAX).

2: t_{EN} when CNVST is lowered after t_{CNV} (MAX).

FIGURE 1-1: *Interface Timing Diagram (14-bit Device). CNVST is Used as Chip Select (CS). See **Section 6.0, Digital Serial Interface**.*

TABLE 1-3: TEMPERATURE CHARACTERISTICS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	Note 1
Storage Temperature Range	T_A	-65	—	+150	°C	Note 1
Thermal Package Resistance						
Thermal Resistance, MSOP-10	θ_{JA}	—	202	—	°C/W	
Thermal Resistance, TDFN-10	θ_{JA}	—	68	—	°C/W	

Note 1: The internal junction temperature (T_j) must not exceed the absolute maximum specification of +150°C.

NOTES:

2.0 TYPICAL PERFORMANCE CURVES FOR 14-BIT DEVICES (MCP33151-XX)

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33151-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33151-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

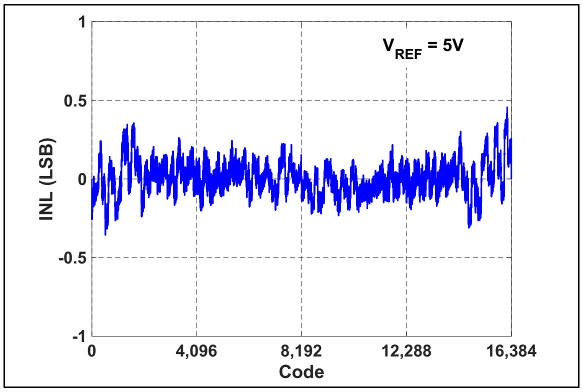


FIGURE 2-1: *INL vs. Output Code: V_{REF} = 5V.*

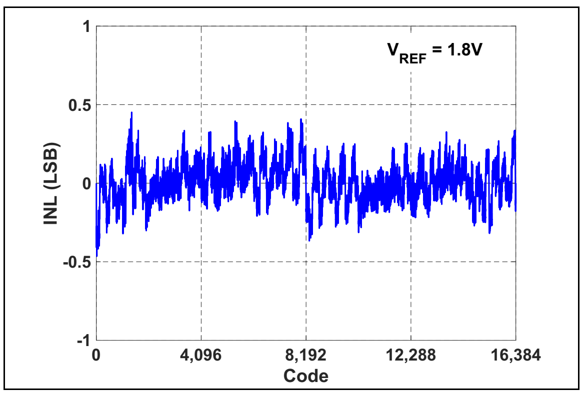


FIGURE 2-2: *INL vs. Output Code: V_{REF} = 1.8V.*

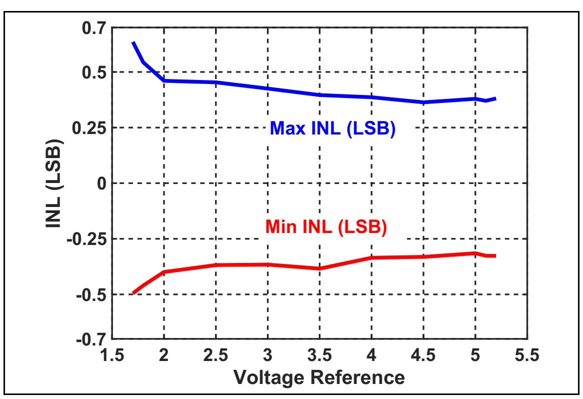


FIGURE 2-3: *INL vs. Reference Voltage.*

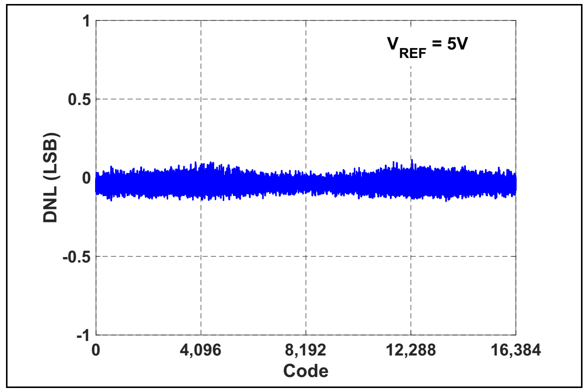


FIGURE 2-4: *DNL vs. Output Code: V_{REF} = 5V.*

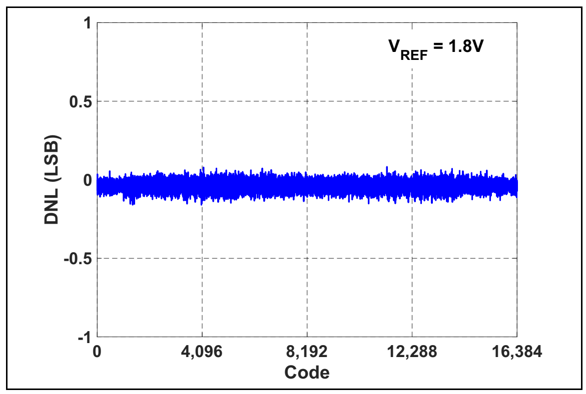


FIGURE 2-5: *DNL vs. Output Code: V_{REF} = 1.8V.*

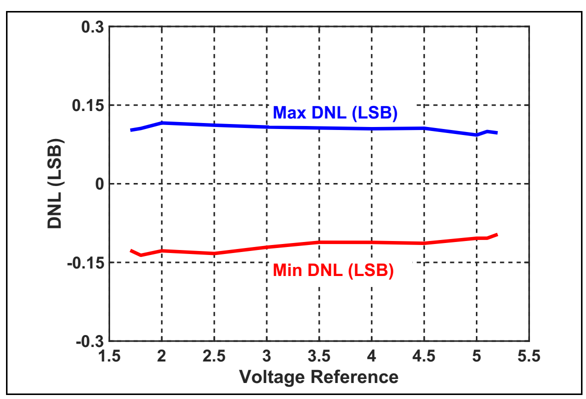


FIGURE 2-6: *DNL vs. Reference Voltage.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33151-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33151-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

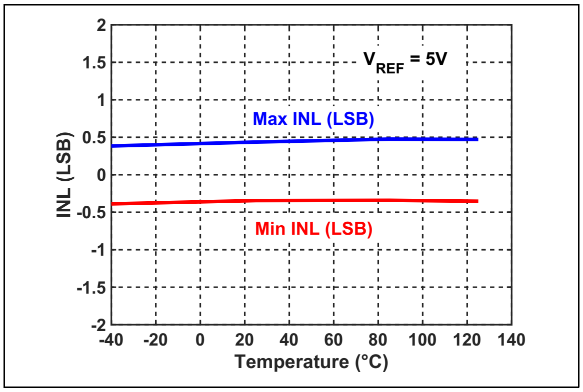


FIGURE 2-7: *INL vs. Temperature.*

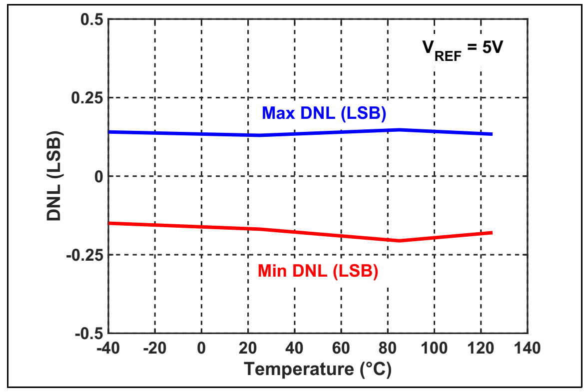


FIGURE 2-10: *DNL vs. Temperature.*

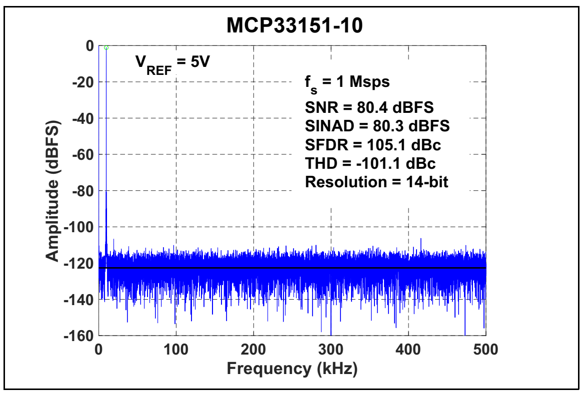


FIGURE 2-8: *FFT for 10 kHz Input Signal: f_S = 1 Msps, V_{IN} = -1 dBFS, V_{REF} = 5V.*

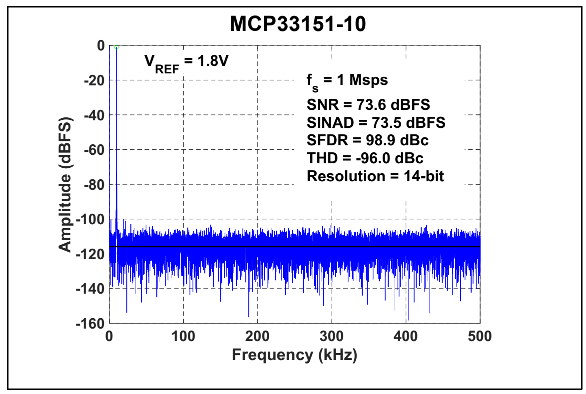


FIGURE 2-11: *FFT for 10 kHz Input Signal: f_S = 1 Msps, V_{IN} = -1 dBFS, V_{REF} = 1.8V.*

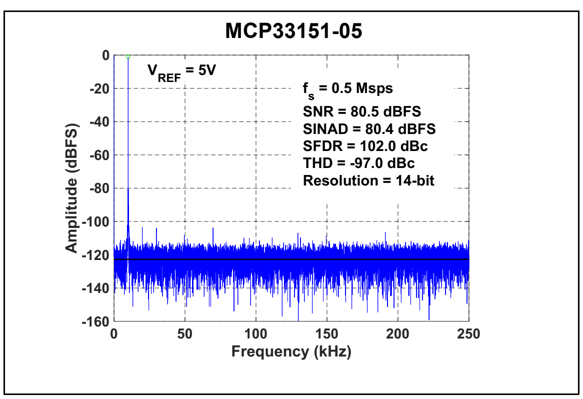


FIGURE 2-9: *FFT for 10 kHz Input Signal: f_S = 500 ksps, V_{IN} = -1 dBFS, V_{REF} = 5V.*

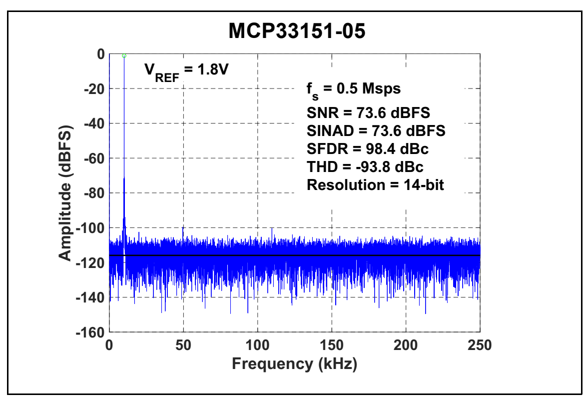


FIGURE 2-12: *FFT for 10 kHz Input Signal: f_S = 500 ksps, V_{IN} = -1 dBFS, V_{REF} = 1.8V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33151-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33151-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

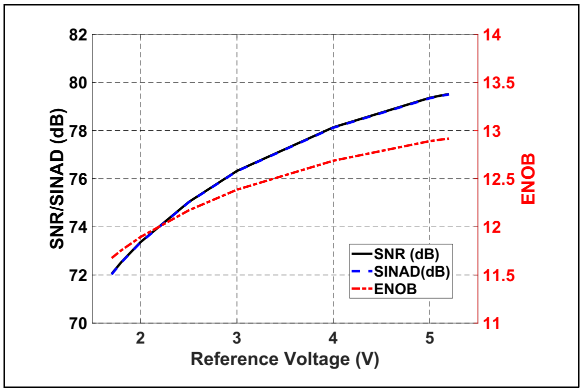


FIGURE 2-13: *SNR/SINAD/ENOB vs. Reference Voltage.*

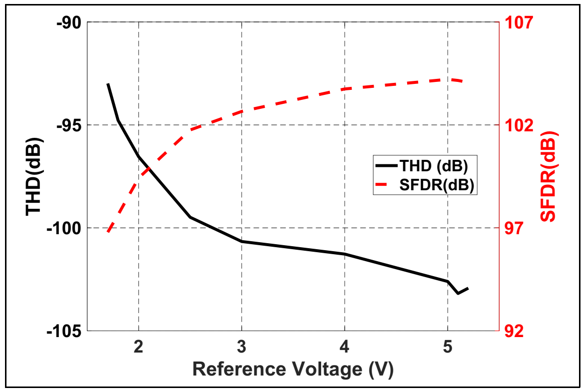


FIGURE 2-16: *THD/SFDR vs. Reference Voltage.*

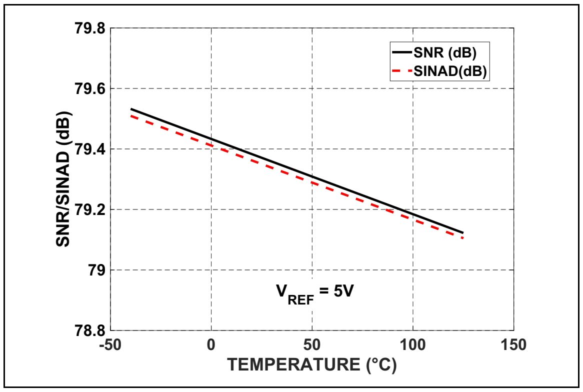


FIGURE 2-14: *SNR/SINAD vs. Temperature: V_{REF} = 5V.*

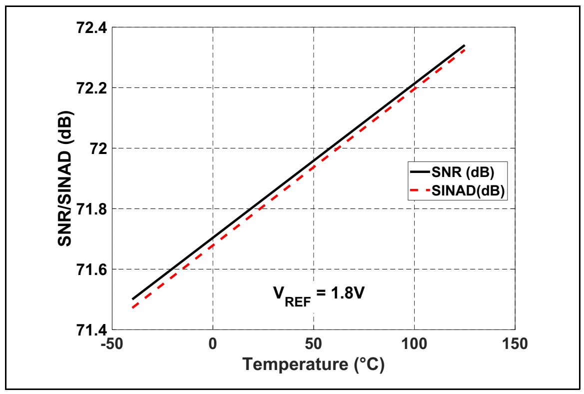


FIGURE 2-17: *SNR/SINAD vs. Temperature: V_{REF} = 1.8V.*

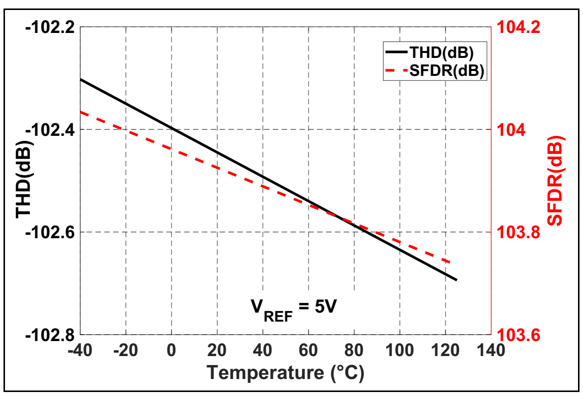


FIGURE 2-15: *THD/SFDR vs. Temperature: V_{REF} = 5V.*

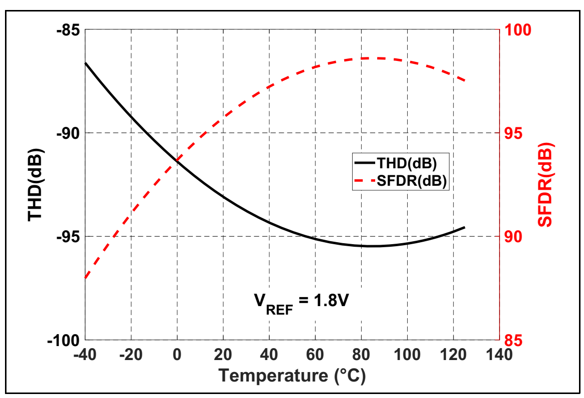


FIGURE 2-18: *THD/SFDR vs. Temperature: V_{REF} = 1.8V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33151-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33151-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

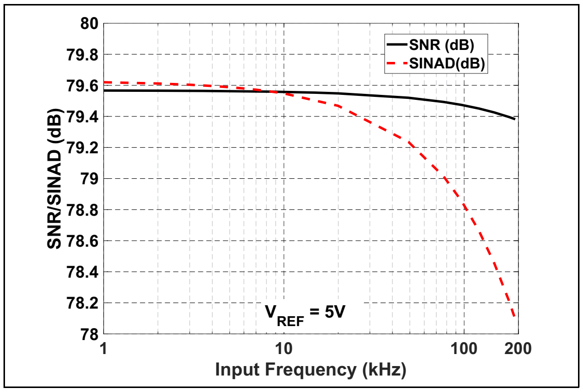


FIGURE 2-19: *SNR/SINAD vs.Input Frequency: V_{REF} = 5V.*

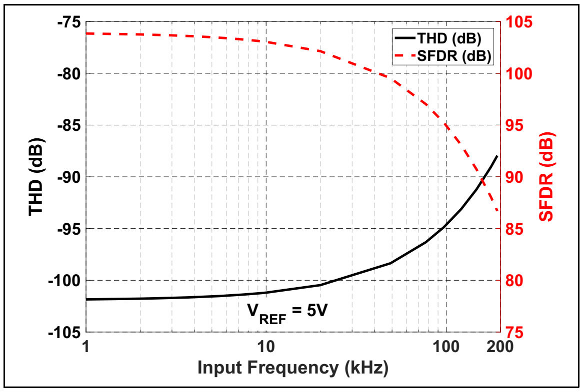


FIGURE 2-20: *THD/SFDR vs. Input Frequency: V_{REF} = 5V.*

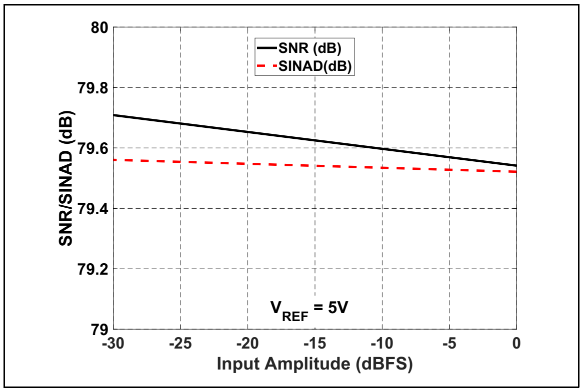


FIGURE 2-21: *SNR/SINAD vs. Input Amplitude: V_{REF} = 5V.*

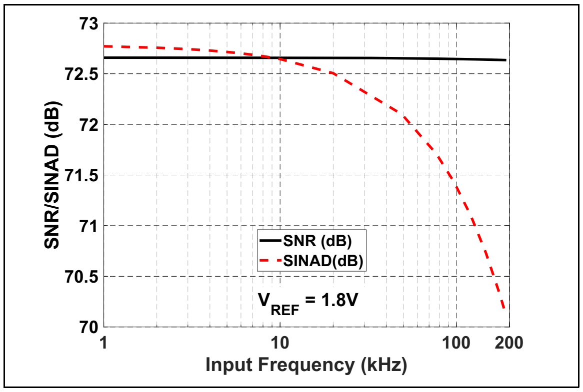


FIGURE 2-22: *SNR/SINAD vs.Input Frequency: V_{REF} = 1.8V.*

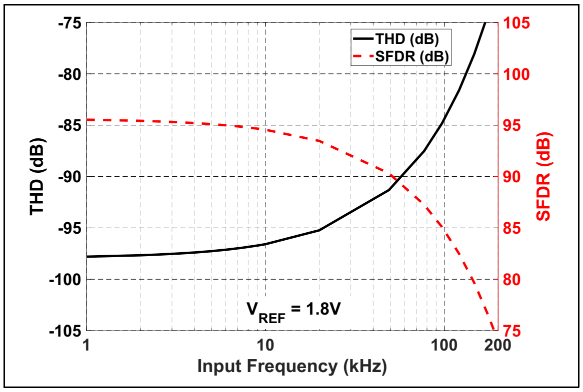


FIGURE 2-23: *THD/SFDR vs. Input Frequency: V_{REF} = 1.8V.*

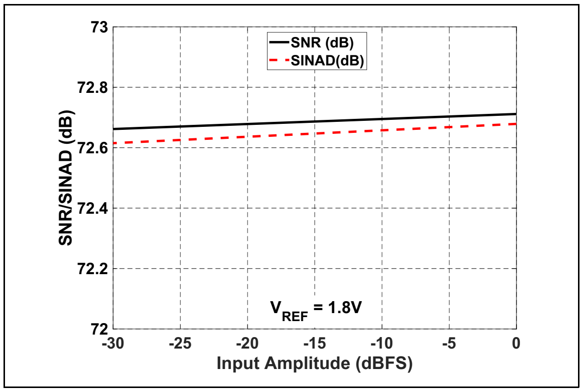


FIGURE 2-24: *SNR/SINAD vs. Input Amplitude: V_{REF} = 1.8V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33151-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33151-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

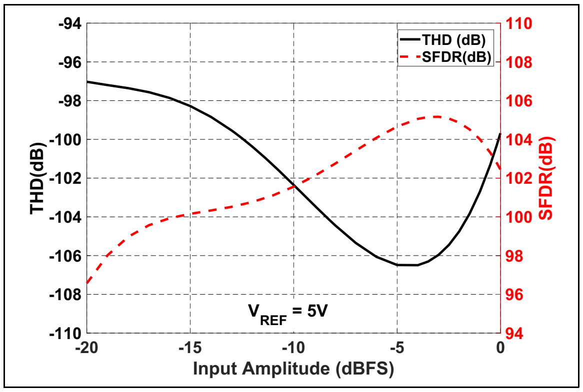


FIGURE 2-25: *THD/SFDR vs. Input Amplitude: V_{REF} = 5V.*

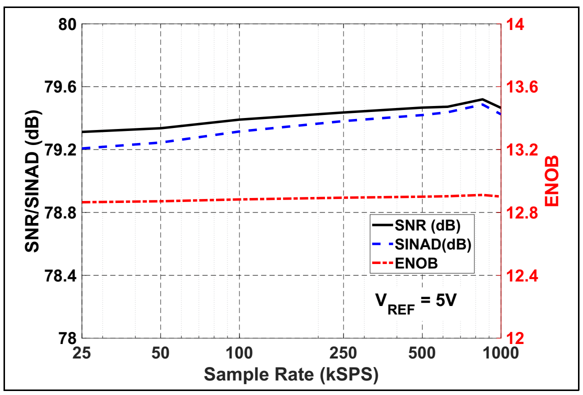


FIGURE 2-26: *SNR/SINAD/ENOB vs. Sample Rate: V_{REF} = 5V.*

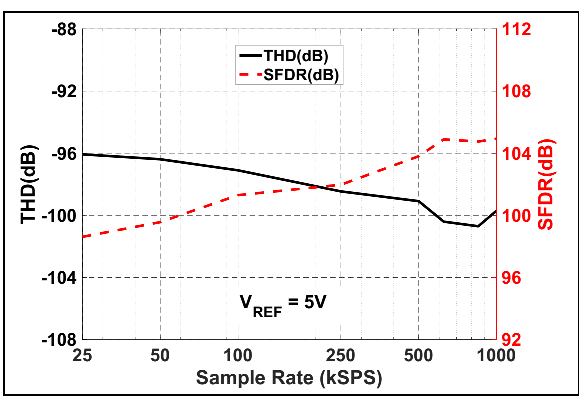


FIGURE 2-27: *THD/SFDR vs. Sample Rate: V_{REF} = 5V.*

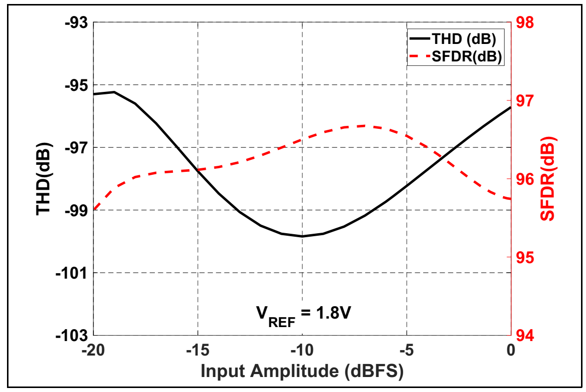


FIGURE 2-28: *THD/SFDR vs. Input Amplitude: V_{REF} = 1.8V.*

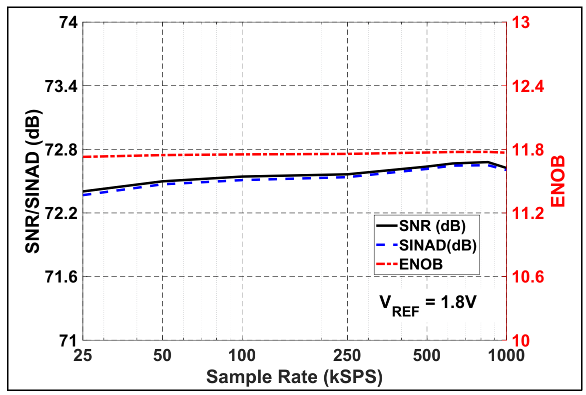


FIGURE 2-29: *SNR/SINAD/ENOB vs. Sample Rate: V_{REF} = 1.8V.*

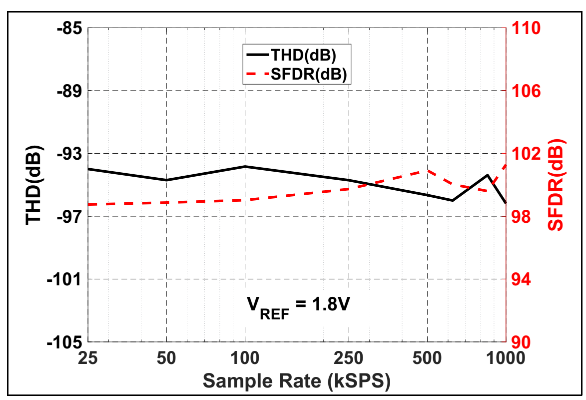


FIGURE 2-30: *THD/SFDR vs. Sample Rate: V_{REF} = 1.8V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33151-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33151-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

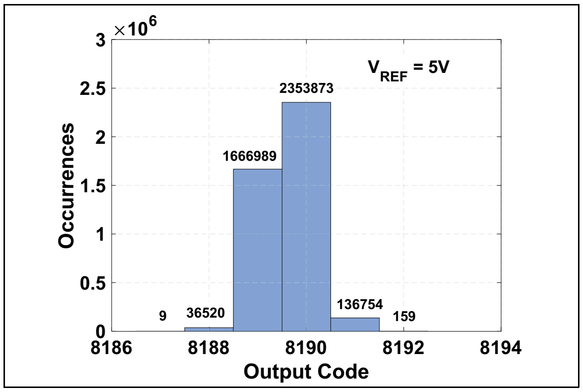


FIGURE 2-31: *Shorted Input Histogram: VREF = 5V.*

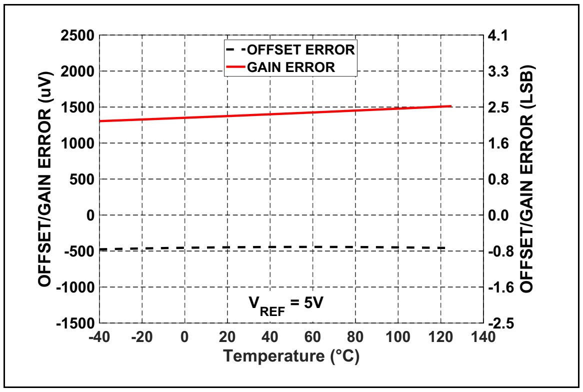


FIGURE 2-32: *Offset and Gain Error vs. Temperature: V_{REF} = 5V.*

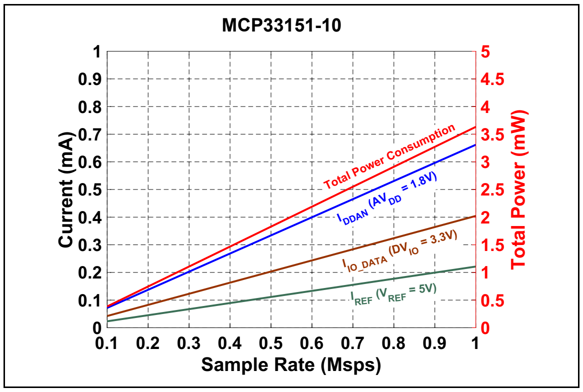


FIGURE 2-33: *Power Consumption vs. Sample Rate: MCP33151-10, C_{LOAD_SDO} = 20 pF.*

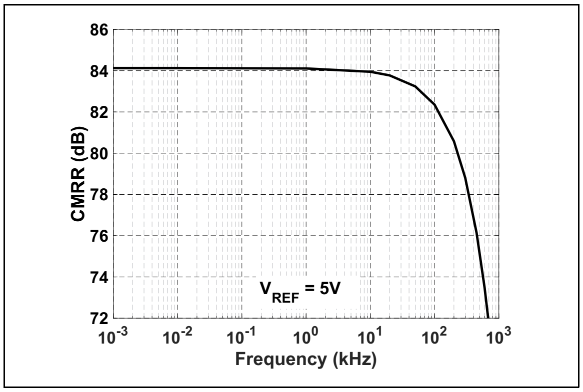


FIGURE 2-34: *CMRR vs. Input Frequency: $5V_{REF}$*

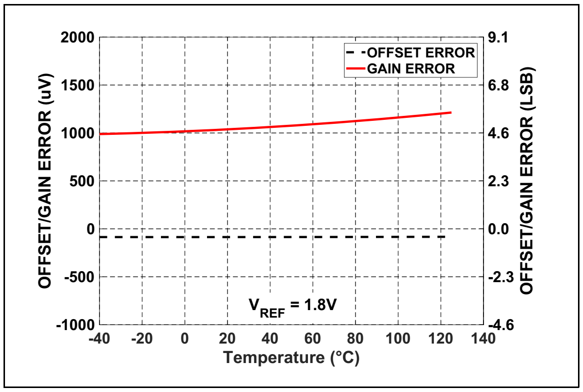


FIGURE 2-35: *Offset and Gain Error vs. Temperature: V_{REF} = 1.8V.*

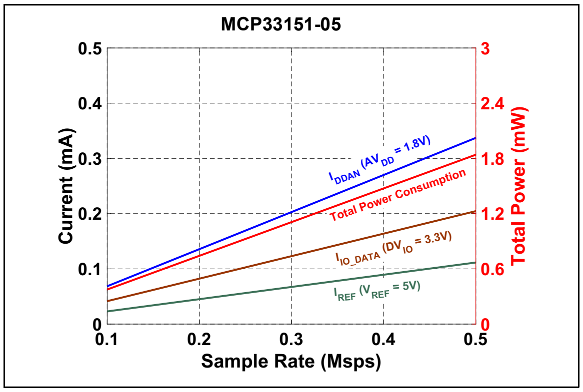


FIGURE 2-36: *Power Consumption vs. Sample Rate: MCP33151-05, C_{LOAD_SDO} = 20 pF.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33151-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33151-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

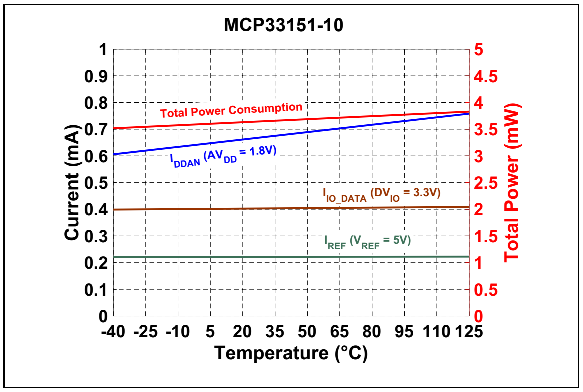


FIGURE 2-37: *Power Consumption vs. Temperature: MCP33151-10, C_{LOAD_SDO} = 20 pF.*

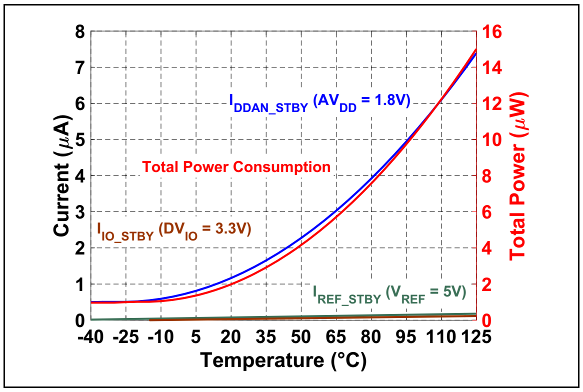


FIGURE 2-38: *Power Consumption vs. Temperature during Shutdown (Standby).*

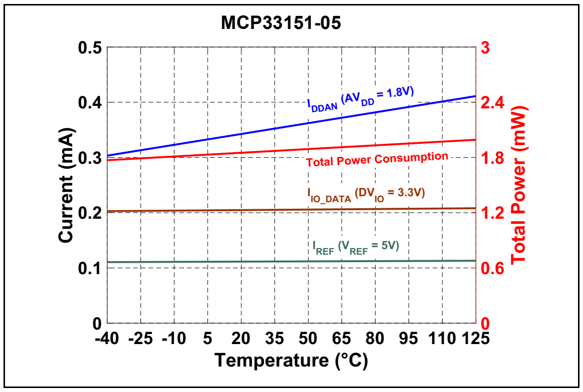


FIGURE 2-39: *Power Consumption vs. Temperature: MCP33151-05, C_{LOAD_SDO} = 20 pF.*

3.0 TYPICAL PERFORMANCE CURVES FOR 12-BIT DEVICES (MCP33141-XX)

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33141-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33141-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

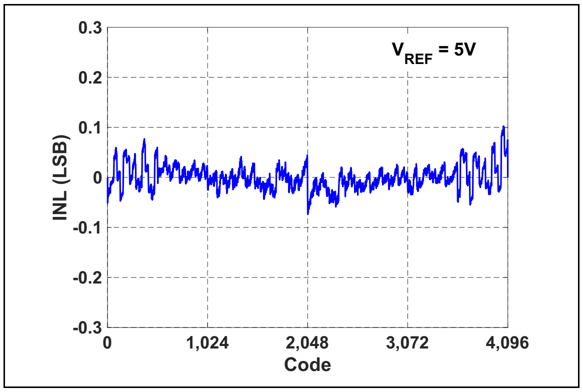


FIGURE 3-1: *INL vs. Output Code: V_{REF} = 5V.*

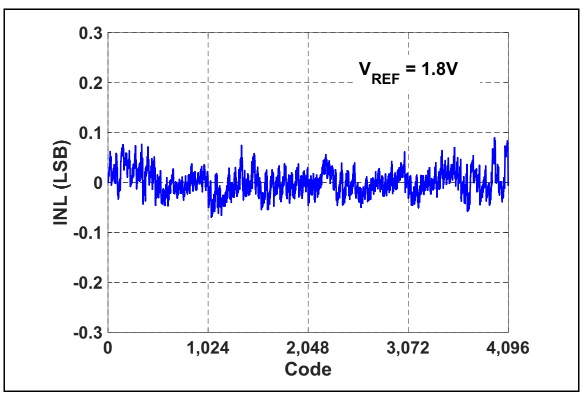


FIGURE 3-2: *INL vs. Output Code: V_{REF} = 1.8V.*

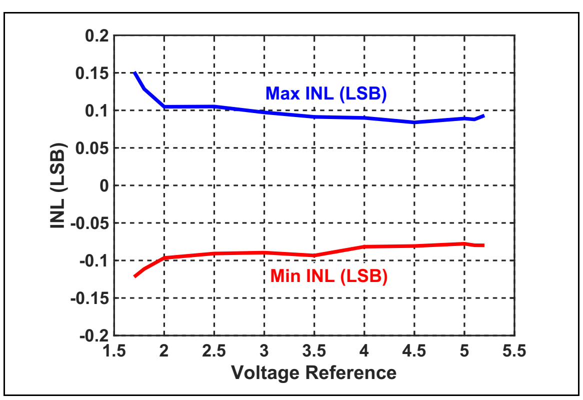


FIGURE 3-3: *INL vs. Reference Voltage.*

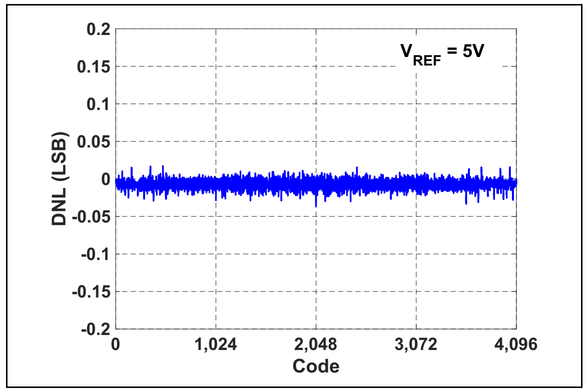


FIGURE 3-4: *DNL vs. Output Code: V_{REF} = 5V.*

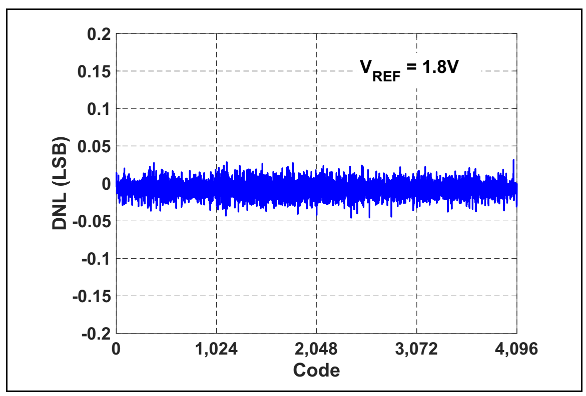


FIGURE 3-5: *DNL vs. Output Code: V_{REF} = 1.8V.*

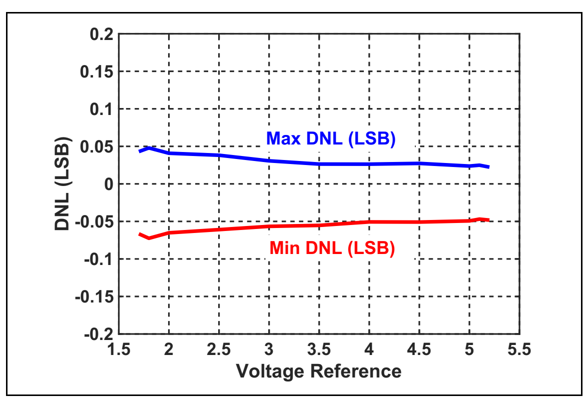


FIGURE 3-6: *DNL vs. Reference Voltage.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33141-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33141-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

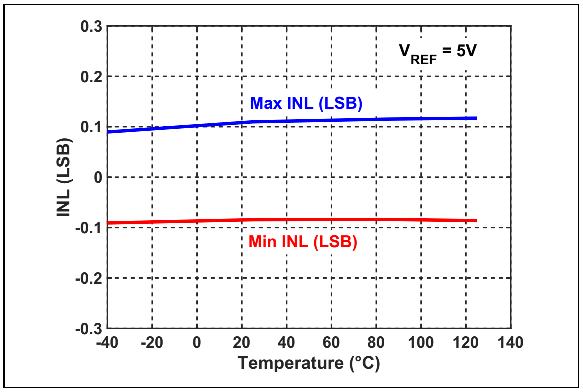


FIGURE 3-7: *INL vs. Temperature.*

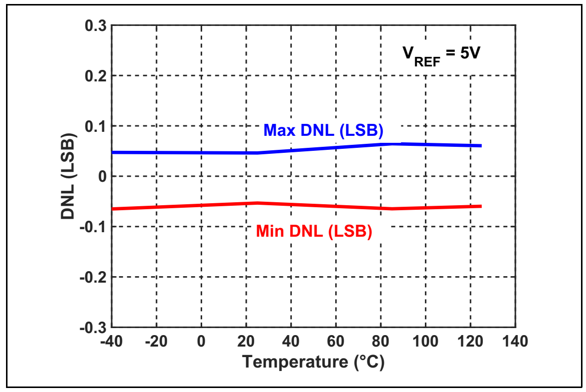


FIGURE 3-10: *DNL vs. Temperature.*

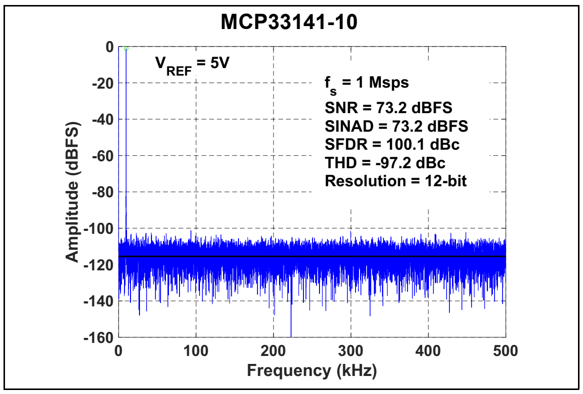


FIGURE 3-8: *FFT for 10 kHz Input Signal: f_S = 1 Msps, V_{IN} = -1 dBFS, V_{REF} = 5V.*

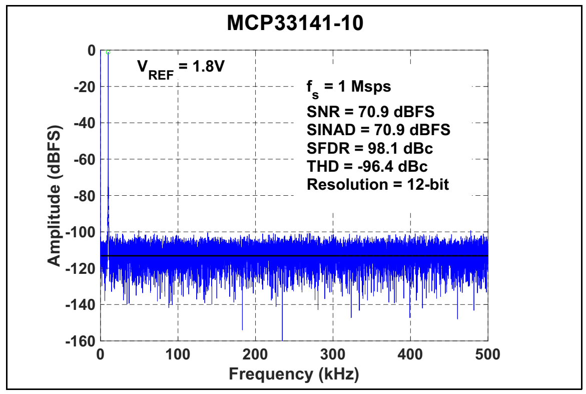


FIGURE 3-11: *FFT for 10 kHz Input Signal: f_S = 1 Msps, V_{IN} = -1 dBFS, V_{REF} = 1.8V.*

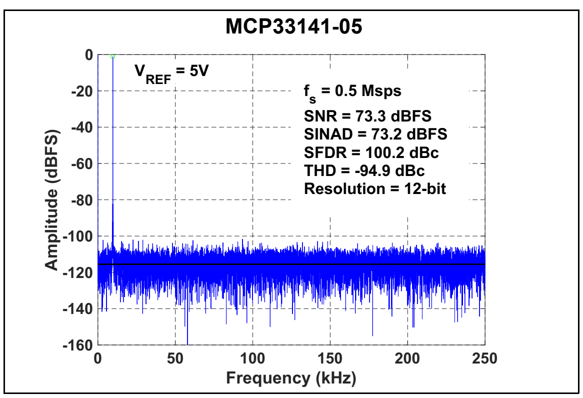


FIGURE 3-9: *FFT for 10 kHz Input Signal: f_S = 500 ksps, V_{IN} = -1 dBFS, V_{REF} = 5V.*

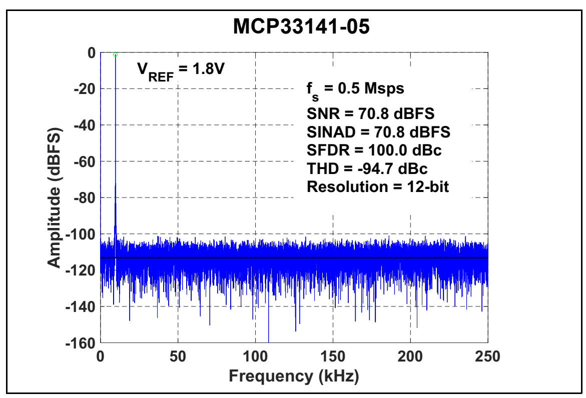


FIGURE 3-12: *FFT for 10 kHz Input Signal: f_S = 500 ksps, V_{IN} = -1 dBFS, V_{REF} = 1.8V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33141-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33141-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

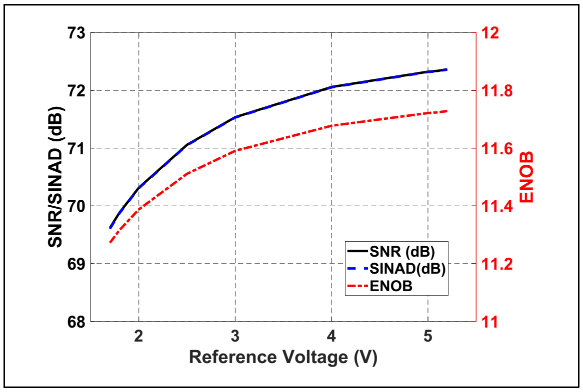


FIGURE 3-13: *SNR/SINAD/ENOB vs. Reference Voltage.*

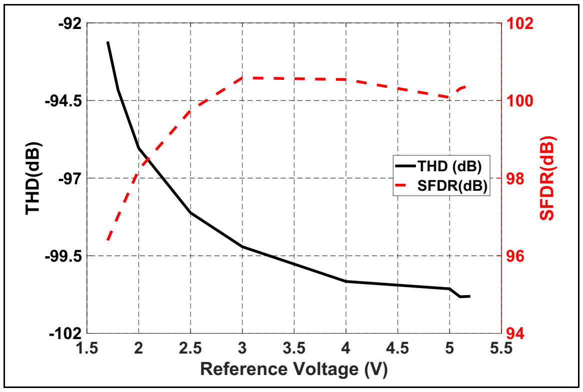


FIGURE 3-16: *THD/SFDR vs. Reference Voltage.*

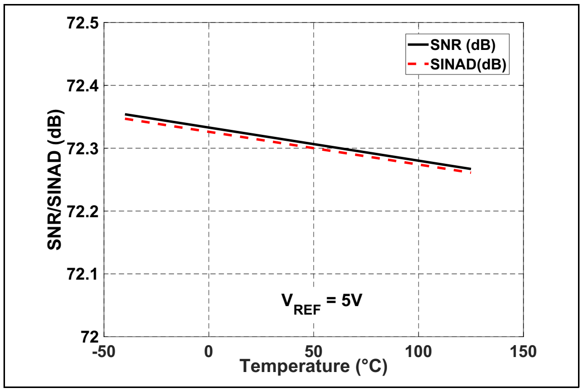


FIGURE 3-14: *SNR/SINAD vs. Temperature: V_{REF} = 5V.*

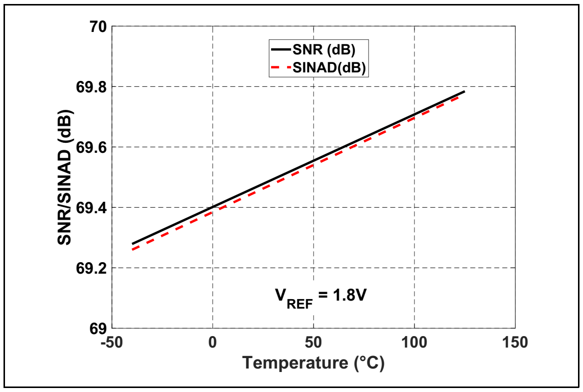


FIGURE 3-17: *SNR/SINAD vs. Temperature: V_{REF} = 1.8V.*

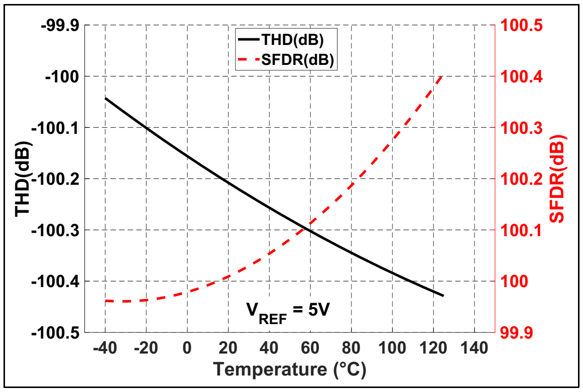


FIGURE 3-15: *THD/SFRD vs. Temperature: V_{REF} = 5V.*

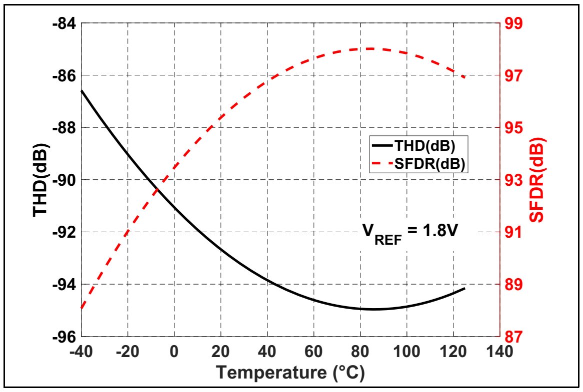


FIGURE 3-18: *THD/SFDR vs. Temperature: V_{REF} = 1.8V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33141-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33141-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

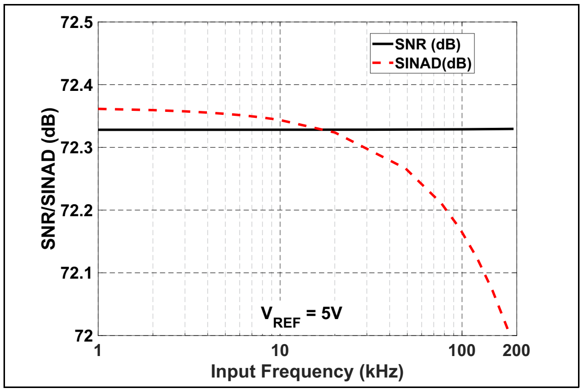


FIGURE 3-19: *SNR/SINAD vs. Input Frequency: V_{REF} = 5V.*

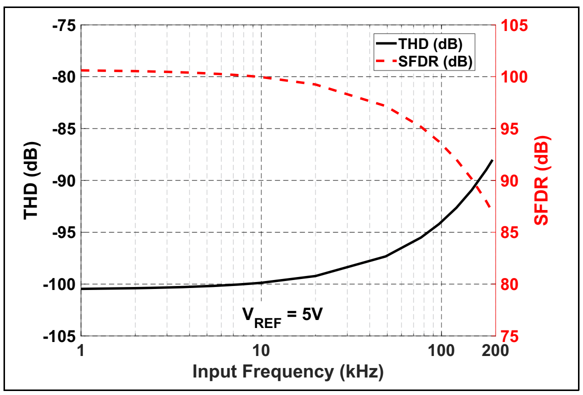


FIGURE 3-20: *THD/SFDR vs. Input Frequency: V_{REF} = 5V.*

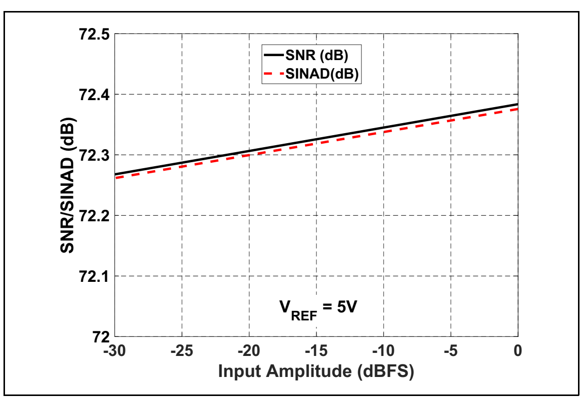


FIGURE 3-21: *SNR/SINAD vs. Input Amplitude: V_{REF} = 5V.*

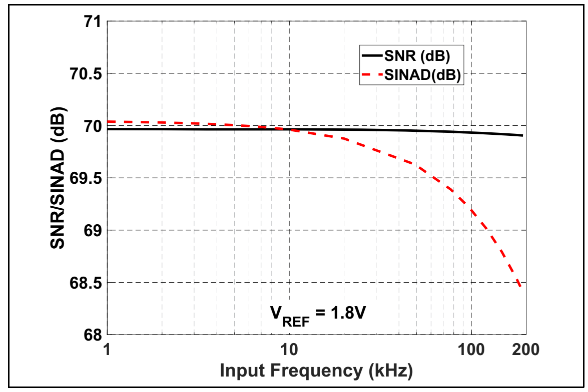


FIGURE 3-22: *SNR/SINAD vs. Input Frequency: V_{REF} = 1.8V.*

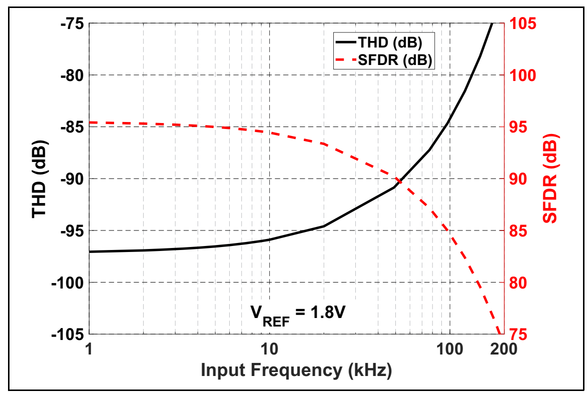


FIGURE 3-23: *THD/SFDR vs. Input Frequency: V_{REF} = 1.8V.*

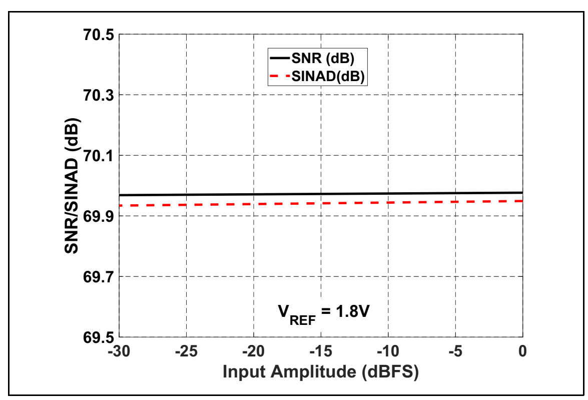


FIGURE 3-24: *SNR/SINAD vs. Input Amplitude: V_{REF} = 1.8V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33141-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33141-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

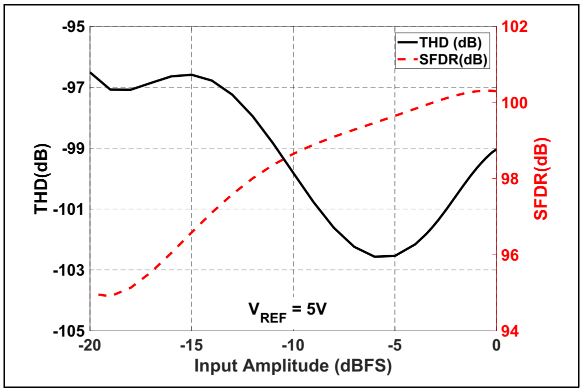


FIGURE 3-25: *THD/SFDR vs. Input Amplitude: V_{REF} = 5V.*

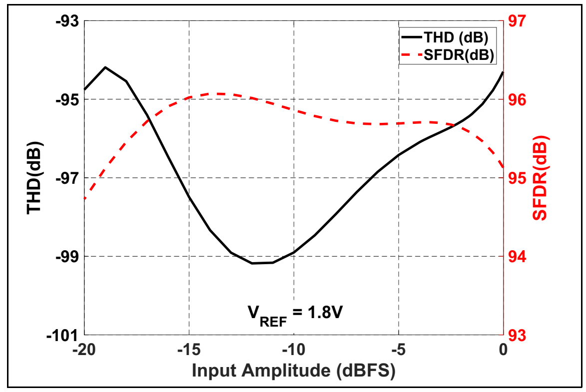


FIGURE 3-28: *THD/SFDR vs. Input Amplitude: V_{REF} = 1.8V.*

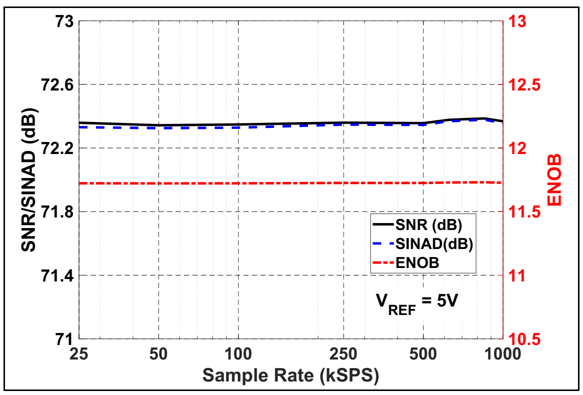


FIGURE 3-26: *SNR/SINAD/ENOB vs. Sample Rate: V_{REF} = 5V.*

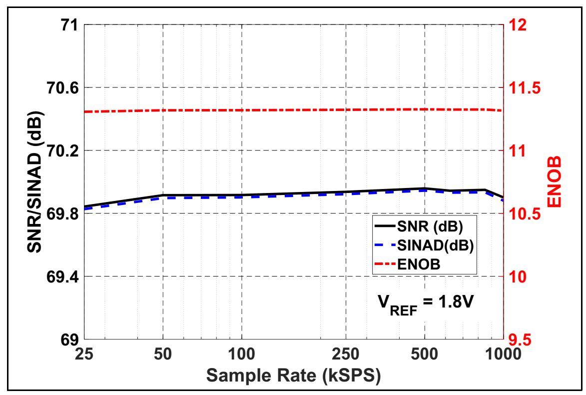


FIGURE 3-29: *SNR/SINAD/ENOB vs. Sample Rate: V_{REF} = 1.8V.*

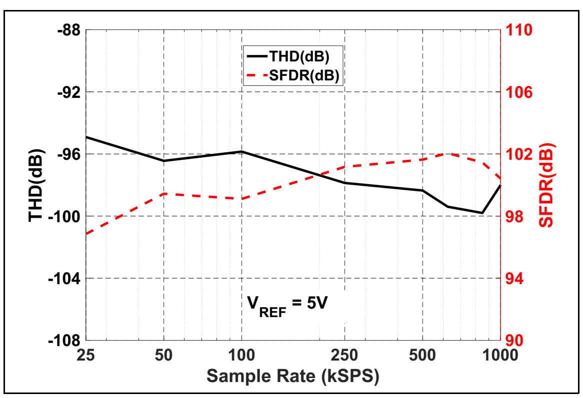


FIGURE 3-27: *THD/SFDR vs. Sample Rate: V_{REF} = 5V.*

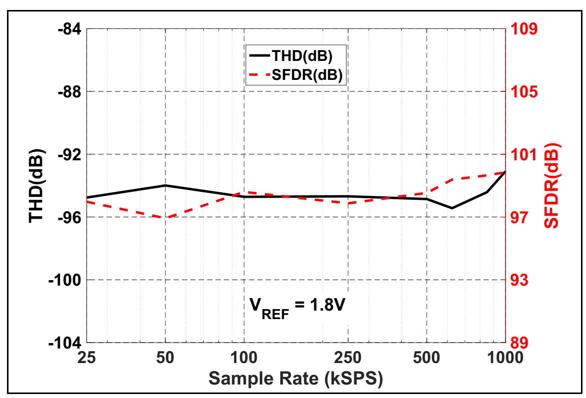


FIGURE 3-30: *THD/SFDR vs. Sample Rate: V_{REF} = 18V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33141-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33141-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

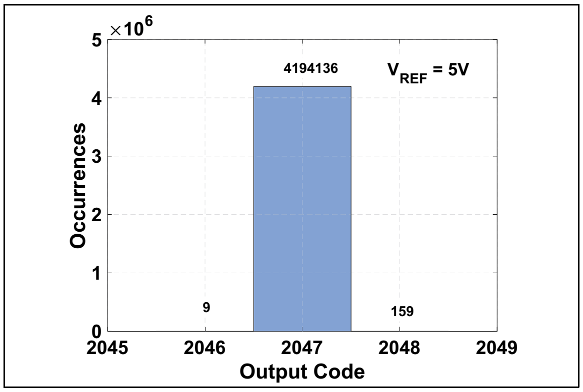


FIGURE 3-31: *Shorted Input Histogram: V_{REF} = 5V.*

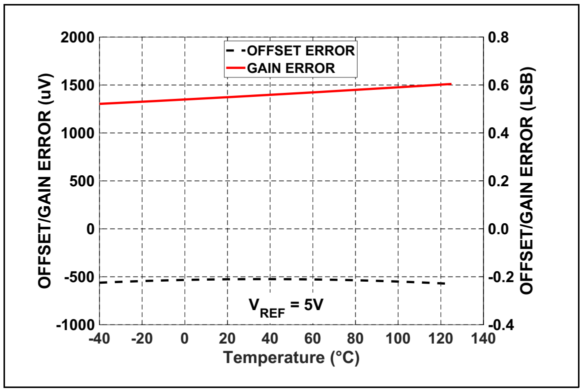


FIGURE 3-32: *Offset and Gain Error vs. Temperature: V_{REF} = 5V.*

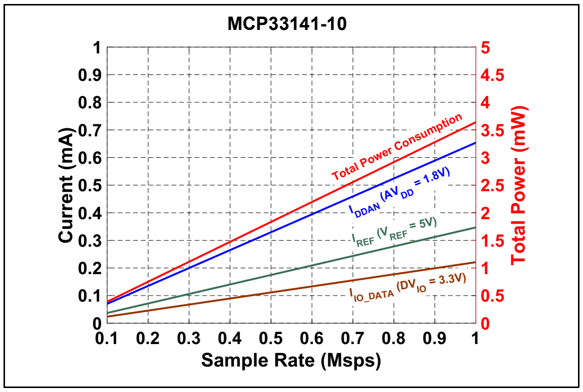


FIGURE 3-33: *Power Consumption vs. Sample Rate: MCP33141-10, C_{LOAD_SDO} = 20 pF.*

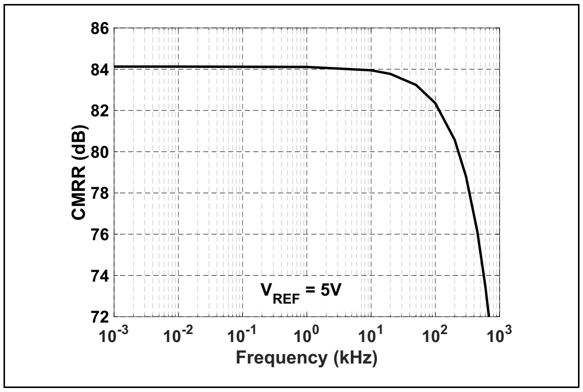


FIGURE 3-34: *CMRR vs. Input Frequency: 5V_{REF}*

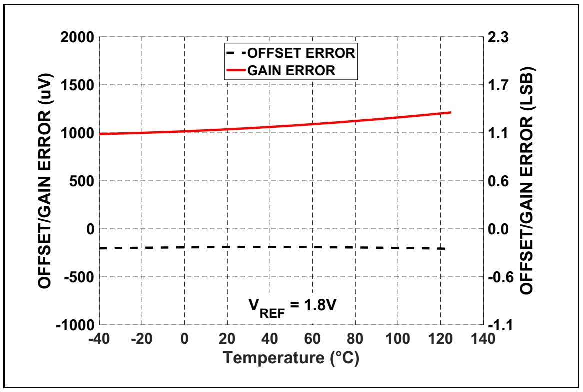


FIGURE 3-35: *Offset and Gain Error vs. Temperature: V_{REF} = 1.8V.*

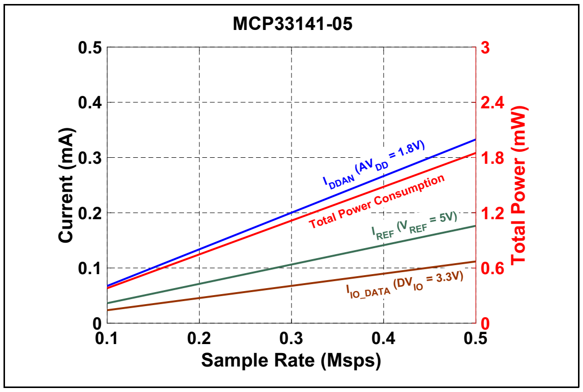


FIGURE 3-36: *Power Consumption vs. Sample Rate: MCP33141-05, C_{LOAD_SDO} = 20 pF.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33141-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33141-05: Sample Rate (f_S) = 500 ksps, SPI Clock Input (SCLK) = 30 MHz.

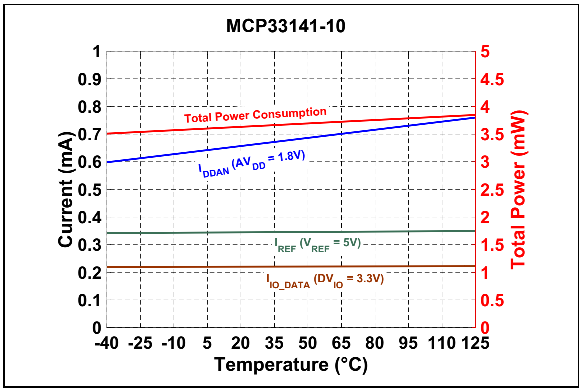


FIGURE 3-37: *Power Consumption vs. Temperature: MCP33141-10, C_{LOAD_SDO} = 20 pF.*

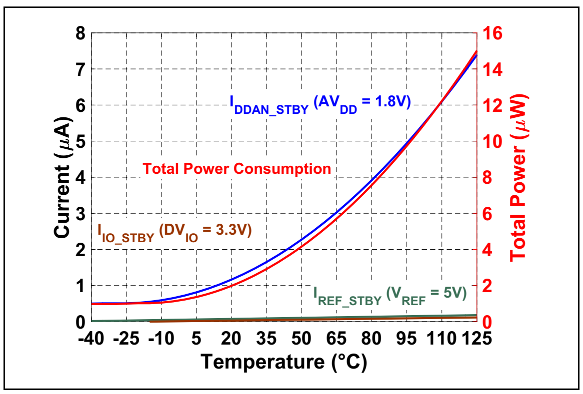


FIGURE 3-38: *Power Consumption vs. Temperature during Shutdown (Standby).*

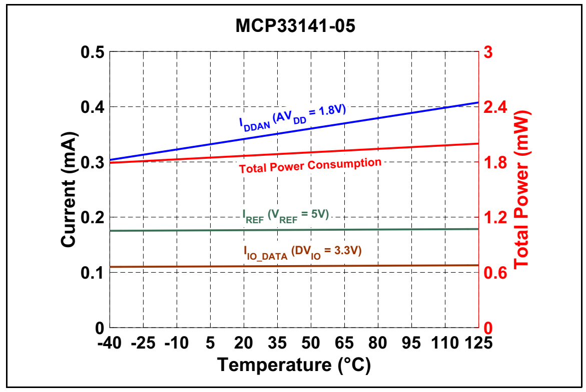


FIGURE 3-39: *Power Consumption vs. Temperature: MCP33141-05, C_{LOAD_SDO} = 20 pF.*

4.0 PIN DESCRIPTIONS

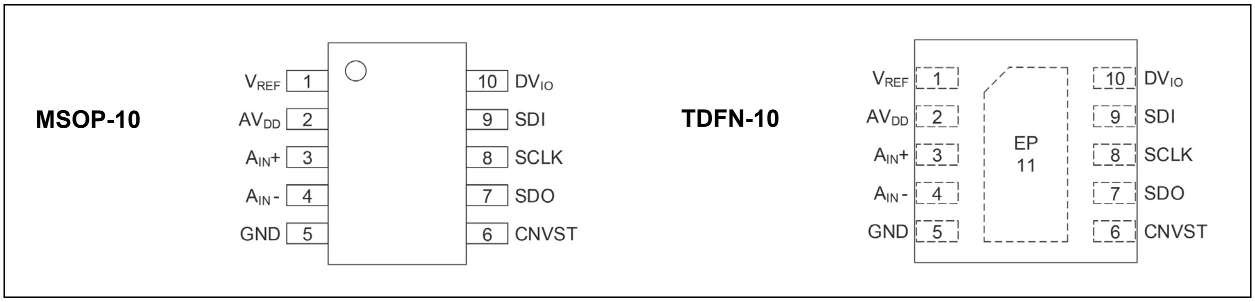


FIGURE 4-1: Pin Configurations.

TABLE 4-1: PIN FUNCTION TABLE

MSOP-10	TDFN-10	Symbol	Description
1	1	V_{REF}	Reference Voltage Input Pin (AV_{DD}-5.1V). This pin should be decoupled with a 10 µF tantalum capacitor.
2	2	AV_{DD}	DC Supply Voltage Input for Analog Section Pin (1.8V). This pin should be decoupled with a 1 µF ceramic capacitor.
3	3	$A_{IN}+$	Analog Input Pin
4	4	$A_{IN}-$	Ground Reference Pin for Analog Input. Connect this pin to the ground reference of the analog input.
5	5	GND	Power Supply Ground Reference Pin. This pin is a common ground for both the analog power supply (AV_{DD}) and digital I/O supply (DV_{IO}).
6	6	CNVST	Conversion Start Control and Active-Low SPI $\overline{CS}$ Digital Input Pin. A new conversion is started on the rising edge of CNVST. When the conversion is complete, output data is available at SDO by lowering CNVST.
7	7	SDO	SPI-Compatible Serial Digital Data Output Pin. ADC conversion data is shifted out by SCLK clock, with MSB first.
8	8	SCLK	SPI-Compatible Serial Data Clock Digital Input Pin. The ADC output is synchronously shifted out by this clock.
9	9	SDI	SPI-Compatible Serial Data Digital Input Pin. Tie to DV_{IO} for normal operation.
10	10	DV_{IO}	DC Supply Voltage for Digital Input/Output Interface Pin (1.7V-5.5V). This pin should be decoupled with a 0.1 µF ceramic capacitor.
—	11	EP	Exposed Thermal Pad. Not internally bonded (NC).

4.1 Supply Voltages (AV_{DD}, DV_{IO})

The device has two power supply pins:

- Analog power supply (AV_{DD}): 1.8V
- Digital input/output interface power supply (DV_{IO}): 1.7V to 5.5V.

The large supply voltage range of DV_{IO} allows the device to interface with various host devices that operate with different supply voltages. See **TABLE 1-2: Serial Interface Timing Specifications** for timing specifications for I/O interface signal parameters depending on DV_{IO} voltage.

Note:	Proper decoupling capacitors (1 µF to AV_{DD}, 0.1 µF to DV_{IO}) should be mounted as close as possible to the respective pins. See Figure 5-1 for an example circuit.

4.2 Reference Voltage (V_{REF})

The device requires a single-ended external reference voltage (V_{REF}). The external input reference range is from AV_{DD} to 5.1V. This reference voltage sets the input full-scale range from 0V to V_{REF}. See Figure 5-2 and Figure 5-3 for an example application circuit and reference voltage settings.

Note:	The reference pin needs a tantalum decoupling capacitor (10 µF, 10V rating). Additional multiple ceramic capacitors can be added in parallel to decouple high-frequency noise.

4.2.1 VOLTAGE REFERENCE SELECTION

The performance of the voltage reference has a large impact on the accuracy of high-precision data acquisition systems. The voltage reference should have high-accuracy, low-noise, and low-temperature drift. A ±0.1% output accuracy of the reference directly corresponds to ±0.1% absolute accuracy of the ADC output. The RMS output noise voltage of the reference must be less than 1/2 LSB of the ADC.

4.3 Power-Up Sequence and Auto-Calibration

The device will perform an automatic calibration on power-up approximately 40 ms after all three power rails (AV_{DD}, DV_{IO}, and V_{REF}) are powered by their respective voltage supplies. The calibration process will take approximately 400 ms to complete before the device will be ready for acquisition. To avoid potential auto-calibration issues, all supplies must be fully stabilized < 40 ms from the moment power is initially supplied. All digital activity must be avoided prior to and during device calibration. At higher operating temperatures (>85°C) it may be necessary to provide additional time for the device to complete calibration (up to 55 ms at 125°C).Therefore it is advisable to wait at least 450-500 ms following power-on before initiating any other activity. Otherwise, it may be necessary to send a manual recalibration command to ensure proper operation. See Figure 4-2 for example power-on operation timing, and refer to Section 6.2, Recalibrate Command for more details regarding initiating manual recalibration. Once the device finishes calibration it will automatically enter Acquisition (ACQ) mode.

Note:	Unlike manual recalibration, there will be no activity on SDO to indicate completion of auto-calibration. See **Section 6.2, Recalibrate Command** for more details.

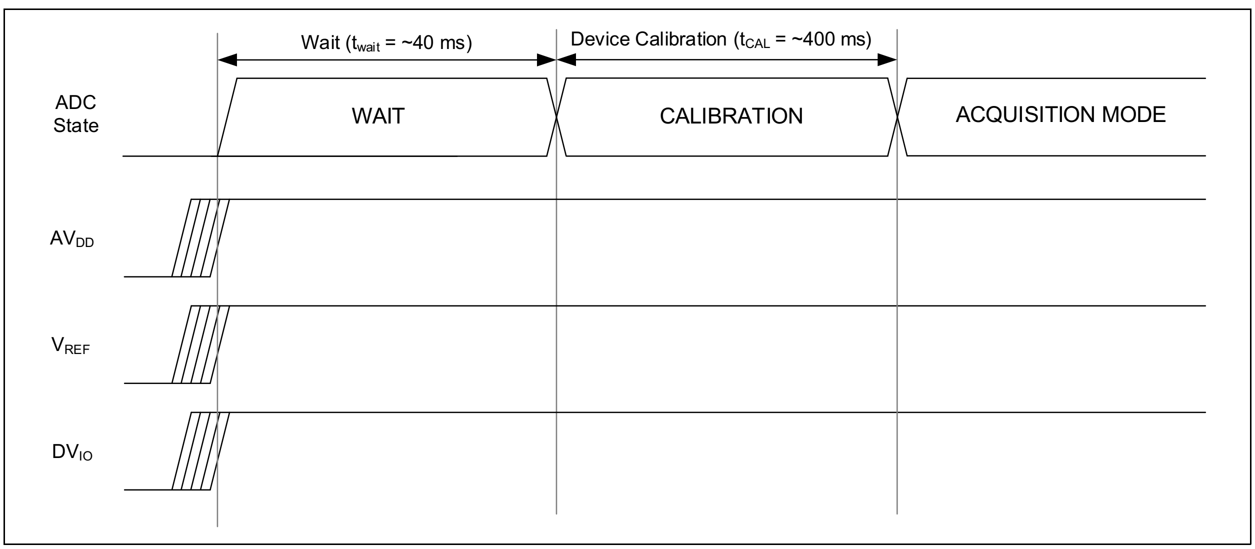


FIGURE 4-2: *Power-Up Sequence and Auto-Calibration Timing Diagram.*

5.0 DEVICE OVERVIEW

The device converts unipolar single-ended analog input into unipolar straight binary codes.

When the MCP33151/41-XX is first powered-up, it performs a self-calibration and enters a low current input acquisition mode (Standby) by itself.

The external reference voltage (V_{REF}) ranging from AV_{DD} to 5.1V sets the input full-scale range (FSR) from 0V to $+V_{REF}$.

During input acquisition (Standby), the internal input sampling capacitors are connected to the input signal, while most of the internal analog circuits are shut down to save power. During this input acquisition time (t_{ACQ}), the device consumes a typical current of 1.5 µA.

The user can operate the device with an easy-to-use SPI-compatible 3-wire interface.

The device initiates data conversion on the rising edge of the conversion start control (CNVST). The data conversion time (t_{CNV}) is set by the internal clock. Once the conversion is complete, the device starts the next input acquisition. During this input acquisition time (t_{ACQ}), the user can clock out the output data by providing the external SPI serial clock (SCLK).

The device provides conversion data with no missing codes. This ADC device family has a large input full-scale range, high precision, high throughput with no output latency, and is an ideal choice for various ADC applications.

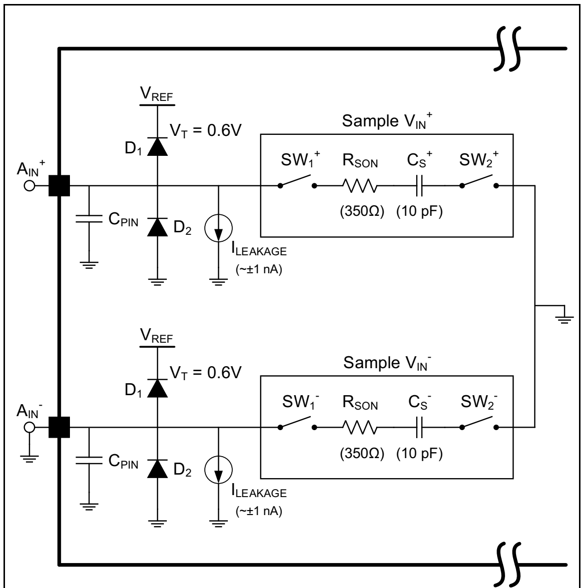
5.1 Analog Input

Figure 5-1 shows a simplified equivalent circuit of the input architecture with a switched capacitor input stage. The input sampling capacitor (C_S+) is about 10 pF. The back-to-back diodes (D_1 – D_2) at each input pin are ESD protection diodes. Note that these ESD diodes are tied to V_{REF}, so that each input signal can swing from 0V to V_{REF}.

The input sampling and hold circuit in A_{IN}+ path is also repeated in A_{IN}- path. This allows the device to perform a pseudodifferential conversion of the input signal. Therefore, the Common-mode signal presented at both input pins is rejected. In applications, A_{IN}+ pin is for the input signal and A_{IN}- pin is for the ground reference of the input signal. The user must connect the A_{IN}- pin to a clean ground plane of the input signal externally.

During input acquisition phase (Standby), the sampling switches are closed and each input sees the sampling capacitor (≈ 10 pF) in series with the on-resistance of the sampling switch, R_{SON} (≈ 350Ω).

For high-precision data conversion applications, the input voltage needs to be fully settled within 1/2 LSB during t_{ACQ}. The settling time is directly related to the source impedance: a lower impedance source results in a faster input settling time. Although the device can be driven directly with a low impedance source, using a low noise input driver is highly recommended.



Where:

C_S+, C_S-	=	Input sample and hold capacitor ≈ 10 pF
R_{SON}	=	On-resistance of the sampling switch ≈ 350Ω
C_{PN}	=	Package pin + ESD capacitor ≈ 2 pF
A_{IN}+	=	Analog input
A_{IN}-	=	Ground reference of analog input

FIGURE 5-1: *Simplified Equivalent Analog Input Circuit.*

Note: The ESD diodes at the analog input pins are biased from V_{REF}. Any input voltage outside the absolute maximum range can turn on the input ESD protection diodes and results in input leakage current which may cause conversion errors and permanent damage to the device. Care must be taken in setting the input voltage ranges so that the input voltage does not exceed the absolute maximum input voltage range.

5.1.1 INPUT VOLTAGE RANGE

The device has two analog input pins: $A_{IN}+$ and $A_{IN}-$ pins. The analog input signal is applied to the $A_{IN}+$ pin, and the ground reference of the input signal is tied to the $A_{IN}-$ pin.

The voltage difference between $A_{IN}+$ and $A_{IN}-$ is the ADC input (V_{IN}) and needs to be between 0V and $+V_{REF}$ to produce unsaturated output codes. Equation 5-1 shows the input full-scale range (FSR) and input range.

EQUATION 5-1: FSR AND INPUT RANGE

$$\text{Input Full-Scale Range (FSR)} = V_{REF}$$

Input Range: $0V \le V_{IN} \le (V_{REF} - 1\ LSB)$

Where:

$V_{IN} = AIN^{+} - AIN^{-}$

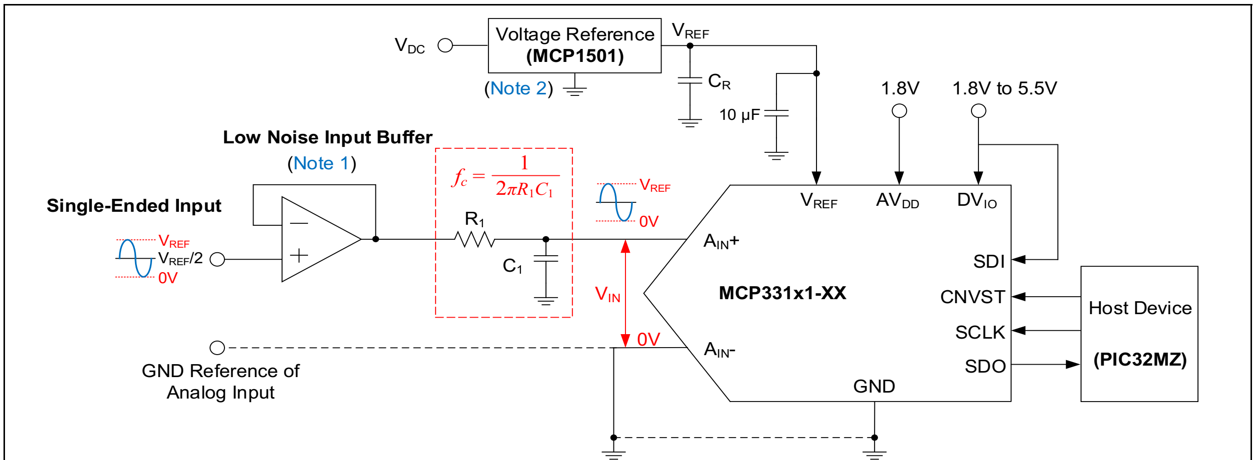
The device will output unipolar straight binary codes for the analog input. If the input (V_{IN}) is greater than the reference voltage (V_{REF}), the output code will be saturated (all 1's). If the input (V_{IN}) is less than or equal to 0V, the output will be all 0's.

5.2 Analog Input Conditioning Circuit

The MCP33151/41-XX can be driven directly when the source impedance of the input driver is low.

A large source impedance of the input signal may affect the ADC's performance. In general, the source impedance is less sensitive to the ADC's DC performances such as INL and DNL. However, it affects significantly the dynamic performances, such as THD, SFDR and SNR.

Therefore, it is a good design practice to isolate the ADC input from the high-impedance source using a low-noise input driver amplifier. Figure 5-2 shows an input configuration example using a low-noise OP amplifier such as MCP6286 and Figure 5-3 shows the transfer function of the MCP33151/41-XX.



Note 1: Contact Microchip Technology Inc. for more selections of the low-noise input driver amplifiers.

2: Contact Microchip Technology Inc. for the MCP1501 application circuit.

FIGURE 5-2: *Unipolar Input Application Example.*

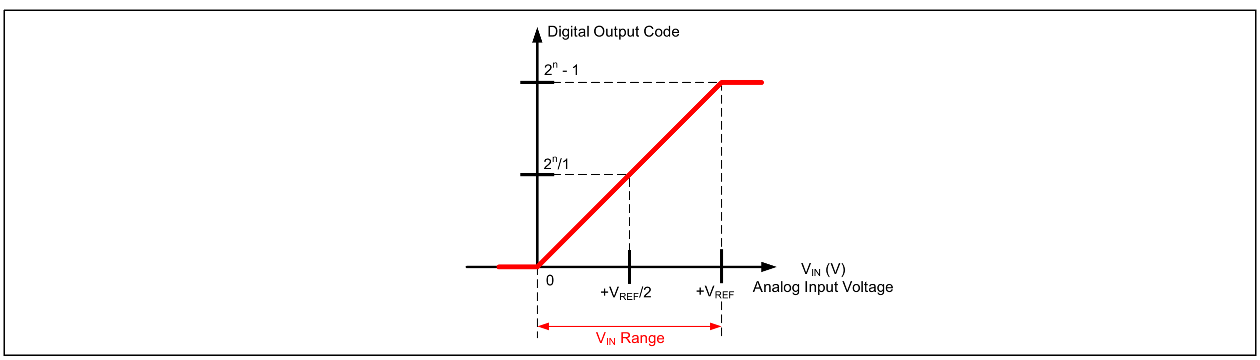


FIGURE 5-3: *Transfer Function for Figure 5-2.*

5.3 ADC Input Driver Selection

The noise and distortion of the ADC input driver can degrade the dynamic performance (SNR, SFDR, and THD) of the overall ADC application system. Therefore, the ADC input driver needs better performance specifications than the ADC itself. The data sheet of the driver typically shows the output noise voltage and harmonic distortion parameters.

Figure 5-4 shows a simplified system noise presentation block diagram for the front-end driver and ADC.

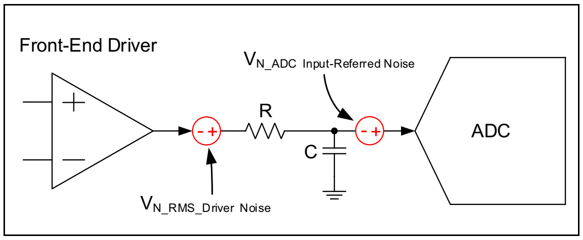


FIGURE 5-4: Simplified System Noise Representation.

- **Unity Gain Bandwidth:**

An input driver with higher bandwidth usually results in better overall linearity performance. Typically, the driver should have the unity gain bandwidth greater than 5 times the -3 dB cutoff frequency of the anti-aliasing filter:

EQUATION 5-2: BANDWIDTH REQUIREMENT FOR ADC INPUT DRIVER

$$BW_{Input\ Driver} \geq 5 \times f_B \quad \text{(Hz)}$$

$$\geq \frac{5}{2\pi RC} \quad \text{for a single-pole RC filter}$$

Where:

f_B = -3 dB bandwidth of RC anti-aliasing filter as shown in Figure 5-4.

- **Distortion:**

The nonlinearity characteristics of the input driver cause distortions in the ADC output. Therefore, the input driver should have less distortion than the ADC itself. The recommended THD of the driver is at least 10 dB less than that of the ADC:

EQUATION 5-3: RECOMMENDED THD FOR ADC INPUT DRIVER

$$THD_{Input\ Buffer} \leq THD_{ADC} - 10 \quad \text{(dB)}$$

- **ADC Input Referred Noise:**

When the ADC operates with a full-scale input range, the ADC input-referred RMS noise for a single-ended input configuration is approximated as shown in Equation 5-4.

EQUATION 5-4: ADC INPUT-REFERRED NOISE

$$V_{N\_ADC\ Input\text{-}Referred\ Noise} = \frac{V_{REF}}{2\sqrt{2}} 10^{-\frac{SNR}{20}} \quad \text{(V)}$$

- **Noise Contribution from the Front-End Driver:**

The noise from the input driver can degrade the ADC's SNR performance. Therefore, the selected input driver must have the lowest possible broadband noise density and 1/f noise. When an anti-aliasing filter is used after the input driver, the output noise density of the input driver is integrated over the -3 dB bandwidth of the filter.

Equation 5-5 shows the RMS output noise voltage calculation using the RC filter's bandwidth and noise density (e_N) of the input driver. G_N in Equation 5-5 is the noise gain of the driver amplifier and becomes 1 for a unity gain buffer driver.

EQUATION 5-5: NOISE FROM FRONT-END DRIVER AMPLIFIER

$$V_{N\_RMS\_Driver\ Noise} \approx G_N \frac{e_N}{\sqrt{2}} \sqrt{\pi f_B} \quad \text{(V)}$$

Where e_N is the broadband noise density (V/√Hz) of the front-end driver amplifier and is typically given in its data sheet.

In Equation 5-5, 1/f noise ($e_{NFlicker}$) is ignored assuming it is very small compared to the broadband noise (e_N).

For high-precision ADC applications, the noise contribution from the front-end input driver amplifier is typically constrained to be less than about 20% (or 1/5 times) of the ADC input-referred noise as shown in Equation 5-6:

EQUATION 5-6: RECOMMENDED ADC INPUT DRIVER NOISE

$$V_{N\_RMS\_Driver\ Noise} \leq \frac{1}{5} V_{N\_ADC\ Input\text{-}Referred\ Noise}$$

Using Equation 5-4 and Equation 5-6, the recommended noise voltage density (e_N) limit of the ADC input driver is expressed in Equation 5-7:

EQUATION 5-7: NOISE DENSITY FOR ADC INPUT DRIVER

$$G_N \frac{e_N}{\sqrt{2}} \sqrt{\pi f_B} \leq \frac{1}{5} V_{N\_ADC\ Input\text{-}Referred\ Noise}$$

$$e_N \leq \frac{1}{10} \frac{1}{G_N \sqrt{\pi f_B}} V_{REF} 10^{-\frac{SNR}{20}} \quad \left(\frac{V}{\sqrt{Hz}}\right)$$

Using Equation 5-7, the recommended maximum noise voltage density limit for unity gain input driver for single-ended input ADC can be estimated. Table 5-1 and Table 5-2 show a few example results with $G_N = 1$. The user has these tables as a reference when selecting the ADC input driver amplifier.

TABLE 5-1: NOISE VOLTAGE DENSITY (E_N) OF INPUT DRIVER FOR MCP33151-XX

ADC (Note 1)			RC Filter	ADC Input Driver Amplifier (G_N = 1)
V_{REF}	SNR (dBFS)	ADC Input-Referred Noise	f_B (Note 2)	Noise Voltage Density (e_N)
1.8V	71.9	161.7 µV	3 MHz	14.9 nV/√Hz
			4 MHz	12.9 nV/√Hz
			5 MHz	11.5 nV/√Hz
3V	76.0	168.1 µV	3 MHz	15.5 nV/√Hz
			4 MHz	13.4 nV/√Hz
			5 MHz	12.0 nV/√Hz
5V	79.3	190.7 µV	3 MHz	17.6 nV/√Hz
			4 MHz	15.2 nV/√Hz
			5 MHz	13.6 nV/√Hz

Note 1: See Equation 5-4 for the ADC input-referred noise calculation for single-ended input.

2: f_B is -3 dB bandwidth of the RC anti-aliasing filter.

TABLE 5-2: NOISE VOLTAGE DENSITY (E_N) OF INPUT DRIVER FOR MCP33141-XX

ADC (Note 1)			RC Filter	ADC Input Driver Amplifier (G_N = 1)
V_{REF}	SNR (dBFS)	ADC Input-Referred Noise	f_B (Note 2)	Noise Voltage Density (e_N)
1.8V	69.5	213.2 µV	3 MHz	19.6 nV/√Hz
			4 MHz	17.0 nV/√Hz
			5 MHz	15.2 nV/√Hz
3V	71.4	285.5 µV	3 MHz	26.3 nV/√Hz
			4 MHz	22.8 nV/√Hz
			5 MHz	20.4 nV/√Hz
5V	72.3	429.0 µV	3 MHz	39.5 nV/√Hz
			4 MHz	34.2 nV/√Hz
			5 MHz	30.6 nV/√Hz

Note 1: See Equation 5-4 for the ADC input-referred noise calculation for single-ended input.

2: f_B is -3dB bandwidth of the RC anti-aliasing filter.

5.4 Device Operation

When the MCP33151/41-XX is first powered-up, it self-calibrates internal systems and automatically enters Input Acquisition mode. The device operates in two phases: input acquisition (Standby) and data conversion. Figure 5-5 shows the ADC operating sequence.

5.4.1 INPUT ACQUISITION PHASE (STANDBY)

During the input acquisition phase (t_{ACQ}), also called Standby, the two input sampling capacitors, C_S+ and C_S-, are connected to the A_{IN}+ and A_{IN}- pins, respectively. The input voltage is sampled until a rising edge on CNVST is detected. The input voltage should be fully settled within 1/2 LSB during t_{ACQ}.

The acquisition time (t_{ACQ}) is user-controllable. This acquisition time (t_{ACQ}) can be increased as long as needed for additional power savings.

5.4.2 DATA CONVERSION PHASE

The start of the conversion is controlled by CNVST. On the rising edge of CNVST, the sampled charge is locked (sample switches are opened) and the ADC performs the conversion. Once a conversion is started, it will not stop until the current conversion is complete. The data conversion time (t_{CNV}) is not user-controllable. After the conversion is complete and the host lowers CNVST, the output data is presented on SDO.

Any noise injection during the conversion phase may affect the accuracy of the conversion. To reduce environment noise, minimize I/O events and running clocks during the conversion time.

The output data is clocked out MSB first. While the output data is being transferred, the device enters the next input acquisition phase.

Note:	Transferring output data during the acquisition phase can disturb the next input sample. It is highly recommended to allow at least t_{QUIET} (10 ns, typical) between the last edge on the SPI interface and the rising edge on CNVST. See Figure 2.0 for t_{QUIET}.

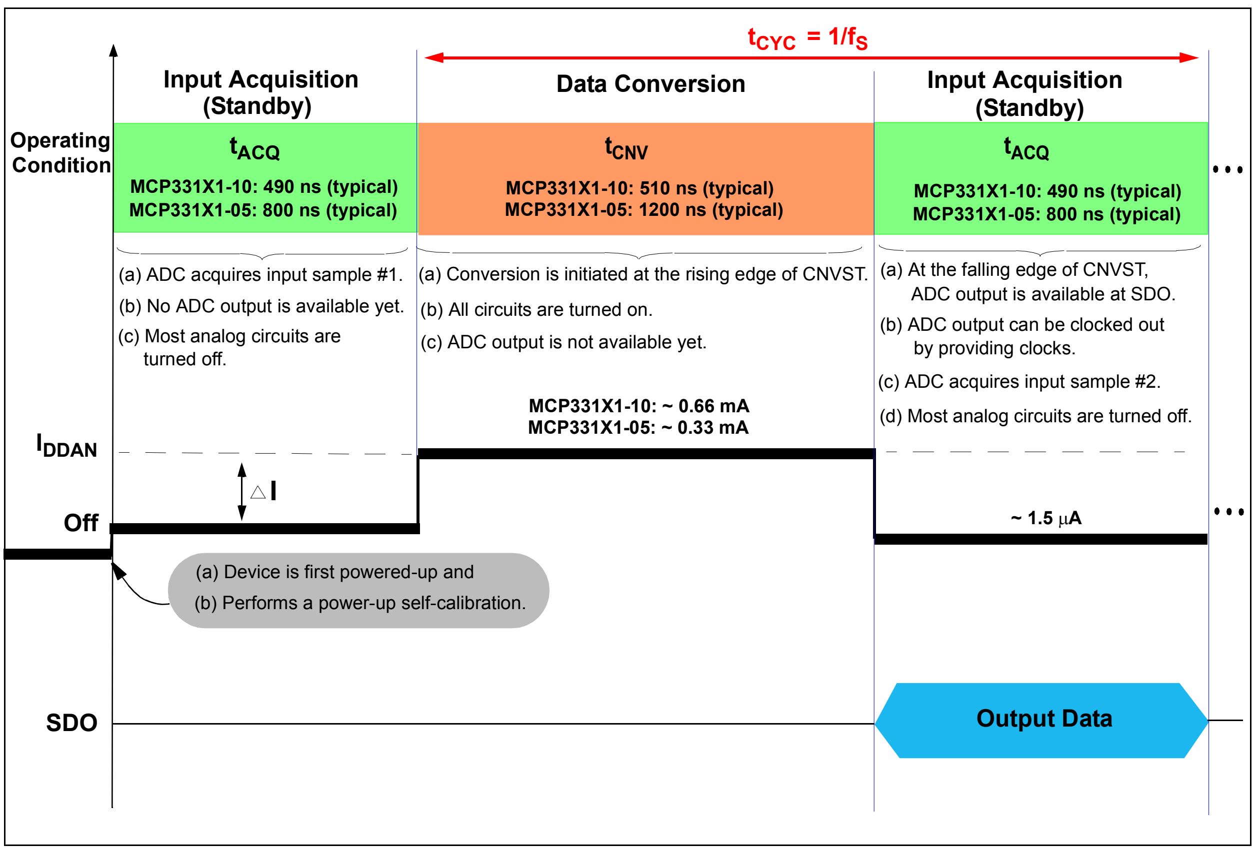


FIGURE 5-5: Device Operating Sequence.

5.4.3 SAMPLE (THROUGHPUT) RATE

The device completes data conversion within the maximum specification of the data conversion time (t_{CNV}). The continuous input sample rate is the inverse of the sum of input acquisition time (t_{ACQ}) and data conversion time (t_{CNV}). Equation 5-8 shows the continuous sample rate calculation using the minimum and maximum specifications of the input acquisition time (t_{ACQ}) and data conversion time (t_{CNV}).

EQUATION 5-8: SAMPLE RATE

$$Sample\ Rate = \frac{1}{(t_{ACQ} + t_{CNV})}$$

(a) MCP331X1-10:

$$Sample\ Rate = \frac{1}{(250\ ns + 750\ ns)} = 1\ Msps$$

(b) MCP331X1-05:

$$Sample\ Rate = \frac{1}{(600\ ns + 1400\ ns)} = 500\ kSPS$$

5.4.4 SERIAL SPI CLOCK FREQUENCY REQUIREMENT

The ADC output is collected during the input acquisition time. For continuous input sampling and data conversion sequence, the SPI clock frequency should be fast enough to clock out all output data bits during t_{ACQ}. For the continuous sampling rate (f_S), the minimum SPI clock frequency requirement is determined by Equation 5-9.

EQUATION 5-9: SPI CLOCK FREQUENCY REQUIREMENT

$$t_{ACQ} = N \times T_{SCLK} + t_{QUIET} + t_{EN}$$

$$f_{SCLK} = \frac{1}{T_{SCLK}} = \frac{N}{t_{ACQ} - (t_{QUIET} + t_{EN})}$$

Where:

f_{SCLK}	=	Minimum SPI serial clock frequency required to transfer all N-bits of output data during t_{ACQ}
	=	f_{SCLK} = minimum SPI serial clock frequency required to transfer all N-bits of output data during t_{ACQ}
N	=	Number of output data bits
T_{SCLK}	=	Period of SPI clock
$N \times T_{SCLK}$	=	Output data window
t_{QUIET}	=	Quiet time between the last output bit and beginning of the next conversion start
	=	10 ns (min.)

Note: Refer to **TABLE 1-2: Serial Interface Timing Specifications** for relevant timing information and see Figure 2-1 for the digital interface timing diagram.

5.5 Transfer Function

The pseudodifferential analog input is:
$V_{IN} = (V_{IN}+) - (V_{IN}-)$, where $V_{IN}+$ is the analog input voltage at $A_{IN}+$ pin with respect to the ground reference (GND), and $V_{IN}-$ is the voltage at $A_{IN}-$ pin, which is 0V when tied to the analog input ground reference (GND).

The LSB size is given by Equation 5-10. and an example of LSB size vs. reference voltage is summarized in Table 5-3.

EQUATION 5-10: LSB SIZE - EXAMPLE

$$LSB = \frac{V_{REF}}{2^N}$$

Where N is the resolution of the ADC in bits.

TABLE 5-3: LSB SIZE VS REFERENCE

Reference Voltage (V_{REF})	LSB Size	
	MCP33151-XX (14-bit)	MCP33141-XX (12-bit)
1.8V	109.9 µV	439.5 µV
2V	122.1 µV	488.3 µV
2.5V	152.6 µV	0.6104 mV
3V	183.1 µV	0.7324 mV
3.3V	201.4 µV	0.8057 mV
3.5V	213.6 µV	0.8545 mV
4V	244.1 µV	0.9766 mV
4.5V	274.7 µV	1.0986 mV
5V	305.2 µV	1.2207 mV
5.1	311.3 µV	1.2451 mV

Figure 5-6 shows the ideal transfer function and Table 5-4 shows the digital output codes for the MCP33151/41-XX.

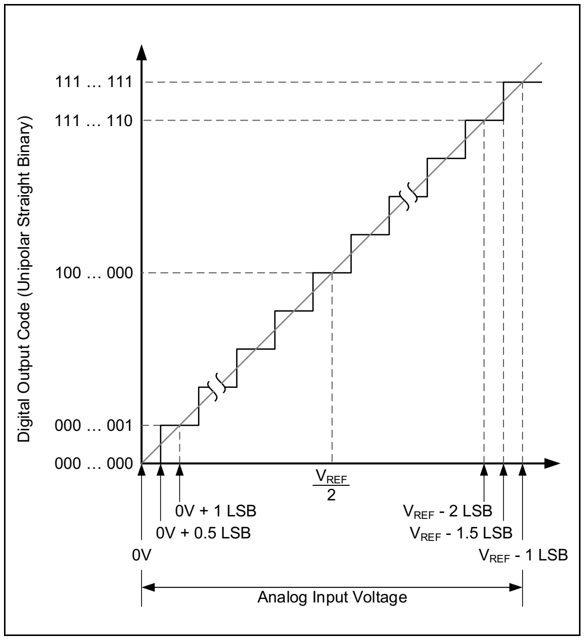


FIGURE 5-6: *Ideal Transfer Function.*

5.6 Digital Output Code

The digital output code is proportional to the input voltage. The output data is in unipolar straight binary format. The following is an example of the output code:

- for a zero or negative input:

  Analog Input: $V_{IN} \le 0$ (V)

  Output Code: `0000...0000`

- for a mid-scale input:

  Analog Input: $V_{IN} = +V_{REF}/2$ (V)

  Output Code: `1000...0000`

- for a positive full-scale input:

  Analog Input: $V_{IN} = +V_{REF}$ (V)

  Output Code: `1111...1111`

The code will be locked at `1111...11` for all voltages greater than (V_{REF} – 1 LSB) and `0000...00` for voltages less than 0V. Table 5-4 shows an example of output codes of various input levels.

TABLE 5-4: DIGITAL OUTPUT CODE

Input Voltage (V)	Digital Output Codes	
	MCP33151-XX (14-bit)	MCP33141-XX (12-bit)
V_{REF}	`11-1111-1111-1111`	`1111-1111-1111`
V_{REF} - 1 LSB	`11-1111-1111-1111`	`1111-1111-1111`
. .	. .	. .
$V_{REF}/2$	`10-0000-0000-0000`	`1000-0000-0000`
. .	. .	. .
2 LSB	`00-0000-0000-0010`	`0000-0000-0010`
1 LSB	`00-0000-0000-0001`	`0000-0000-0001`
≤ 0V	`00-0000-0000-0000`	`0000-0000-0000`

5.7 Data Accumulator

The MCP33151/41-XX devices feature an internal integrator capable of accumulating consecutive sample data and transmitting the accumulated data directly from the ADC, without requiring any special SPI settings to operate. This enables the user to achieve a higher ENOB through consecutive sample integration utilizing the ADC hardware, without requiring any external computational resources and reducing the amount of data transmitted on the serial bus. See Figure 5-7 for an example FFT performance plot after 1024 integrated samples while sampling a 75Hz input signal with a 5V reference voltage. Refer to Figure 5-8 for an example of FFT performance across possible integration lengths.

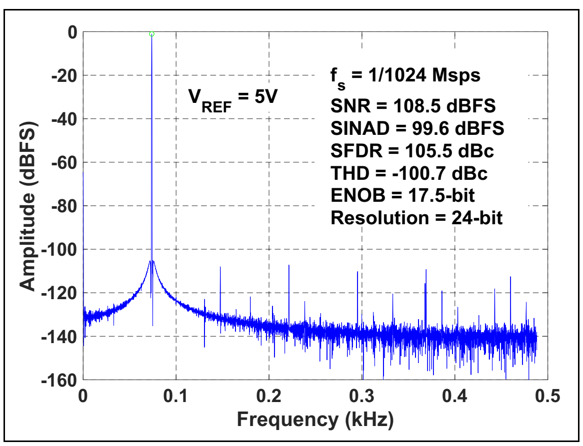


FIGURE 5-7: FFT with 1024 Integrated Samples: Input Freq = 75Hz.

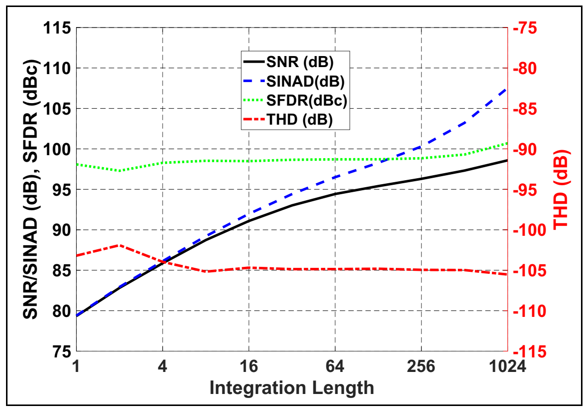


FIGURE 5-8: FFT Performance vs Integration Length: Input Freq = 75Hz.

5.7.1 DATA ACCUMULATOR USAGE

Data accumulation is performed automatically within the device between each sequential Conversion/ Acquisition cycle (TCYC) whenever the current conversion results are not read out, up to a total of 1024 consecutive conversions for an ENOB increase of up to 5 bits above typical. To begin data accumulation, the user simply avoids transmitting any SCLK pulses during each sequential conversion cycle.

Note: If a sample has been converted but not read out, the sample can be discarded by providing at least 1 SCLK pulse before initiating the next conversion. Providing at least 1 SCLK will reset the system for single acquisition. Otherwise all consecutive conversions without an SCLK pulse will automatically be integrated with the previous conversion results.

After completing the desired number of conversions to achieve the target ENOB, the user can begin transferring the total accumulated data by transmitting the necessary number of SCLK pulses to transfer all stored bits. Refer to Table 5-5 for number of conversions, bit size and ENOB relationship. See Figure 6-5 and Figure 6-8 for example Conversion/ Acquisition control and SPI timing operation.

Consecutive sample integration increases the bit size of the output data, up to the maximum output size of the ADC (24-bits/18.5 ENOB at 1024 samples for a 14-bit ADC).

Because the addition of two binary values can produce a sum with an increased bit size, the ADC will need to output data proportional to the amount of samples being integrated. See Table 5-5 for an estimate of the data size and ENOB capability depending on the number of conversions the user chooses to integrate.

When using the accumulator, it is important to consider the frequency content of the input signal being sampled. Because the accumulator is averaging all consecutive conversions over the accumulated time period, the input frequency must be low enough to ensure that no signal information is being filtered out. This means that there is a performance trade-off between sample integration length (and resulting ENOB improvement) and the maximum input frequency that can be sampled. Refer to Table 5-6 to understand the roll-off frequencies for various integration lengths, and refer to Figure 5-9 for an example of the dB attenuation across integration lengths.

TABLE 5-5: ACCUMULATED DATA SIZE AND ENOB FOR 14-BIT ADC

Number of Conversions	ADC transmission size (bits)	Effective Number of bits (ENOB) (1)
1	14	13
2	15	13.5
3 - 4	16	13.5 - 14
5 - 8	17	14 - 14.5
9 - 16	18	14.5 - 15
17 - 32	19	15 - 15.5
33 - 64	20	15.5 - 16
65 - 128	21	16 - 16.5
129 - 256	22	16.5 - 17
257 - 512	23	17 - 17.5
513 - 1024	24	17.5 - 18

Note 1: ENOB values based on typical 14-bit device characteristics under nominal conditions and setting N to the maximum value in the corresponding row.

Note: The discrepancy between the output data size and the actual ENOB is a result of sample integration doubling both the signal amplitude and the noise power for each factor of two that the samples are integrated. By integrating 2 samples, the signal amplitude increases SNR by 6 dB, and the noise power decreases SNR by 3 dB, resulting in an overall SNR increase of 3 dB (+0.5 ENOB).

TABLE 5-6: INPUT SIGNAL ROLL-OFF FREQUENCY VS INTEGRATION LENGTH

Integration Length	Roll-Off (Hz @ 1MSPS)		
	0.1 dB	0.01 dB	0.001 dB
2	41781.9	13226.3	4183.0
4	20890.9	6613.2	2091.5
8	10445.5	3306.6	1045.7
16	5222.7	1653.3	522.9
32	2611.4	826.6	261.4
64	1305.7	413.3	130.7
128	652.8	206.7	65.4
256	326.4	103.3	32.7
512	163.2	51.7	16.3
1024	81.6	25.8	8.2

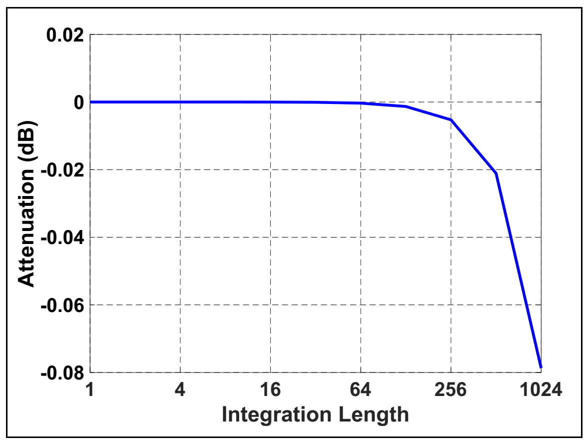


FIGURE 5-9: *Measured Attenuation of Fundamental Frequency (dB) vs Integration Length: Input Freq = 75 Hz.*

6.0 DIGITAL SERIAL INTERFACE

The device has an SPI compatible serial digital interface using four digital interface pins: CNV, SDI, SDO and SCLK.

The following sections describe the operation of the MCP33151/41-XX using the digital serial interface.

Table 6-1 summarizes the descriptions of both digital interface pins and interface options. The communication is always started by the host device (Master).

> **Note:** This device supports a standard SPI Mode 0,0 only. **SPI MODE 0,0:** in this mode, the SCLK idle state is Low. Data is clocked out on the SDO pin on the falling edge of the SCLK pin. For the MCP33151/41-XX, this means that there will be a rising edge before there is a falling edge.

6.1 Serial Interface Options and Serial Communications

The device offers a $\overline{CS}$ mode with a 3-wire interface, and can operate either with or without a BUSY indicator status output. This BUSY status output bit is followed by the conversion output bits, and can be used as an interrupt request ($\overline{IRQ}$) input for the digital host device.

The 3-wire $\overline{CS}$ mode (using CNV, SCLK, SDO) interface is simple and useful when the host device handles a single MCP33151/41-XX device.

The following sections detail the serial communication of the 3-wire $\overline{CS}$ modes with or without a BUSY output bit.

TABLE 6-1: INTERFACE MODE SELECTION SUMMARY

Interface Mode	SDI Pin		CNV Pin at t_{CNV} (recommended)	SCLK at CNV Rising Edge	BUSY bit at SDO
	at CNV Rising Edge	after CNV Rising Edge			
3-wire $\overline{CS}$ mode without BUSY output bit	"High"		Transition from "High" to "Low" after t_{CNV} (Max.)	—	No
3-wire $\overline{CS}$ mode with BUSY output bit	"Low"		Transition from "High" to "Low" before t_{CNV} (Max.)	—	Yes

6.1.1 $\overline{CS}$ MODES

> **Note:** The timing diagram examples in the following subsections are given with 14-bit mode only. The examples are applicable for the 12-bit mode in the same way with reduced bits.

6.1.1.1 3-Wire $\overline{CS}$ Mode Without BUSY Output Bit

This interface option is most useful when a single MCP33151/41-XX is connected to an SPI-compatible digital host. Figure 6-1 shows the connection diagram with the host device. In this mode, CNV functions as both conversion control and $\overline{CS}$.

To enable this interface option, SDI can either be tied to V_{IO}, or permanently held in a Logic = 1 state. By doing so, the device will never output a BUSY status bit.

As shown in Figure 6-2, at the rising edge of CNV, the conversion is initiated. The SDO pin becomes High-Z state (if no external pull-up is used). Once the conversion is initiated, it continues and completes the conversion regardless of the CNV pin condition. This means the CNV pin can be used for other SPI devices after the conversion is initiated.

When the conversion is complete, the device enters the acquisition phase (Power-Down state), and SDO comes out of the High-Z state when CNV is lowered. The device exits the acquisition phase when CNV goes high. SDO returns to a High-Z state after the 14th SCLK falling edge or when CNV goes high, whichever occurs first.

The device will output the MSB on the SDO pin following the falling edge of CNV, or once the converting phase (t_{CNV}) completes, whichever happens later. The remaining data bits are then clocked out on the subsequent SCLK falling edges. Data are valid on both edges of SCLK and can be captured on either edge. However, a digital host capturing data on the SCLK falling edge can achieve a faster read out rate.

> **Note:** It is recommended to use this mode only when the ADC converting phase (t_{CNV}) will complete before the falling edge of CNV.

Figure 6-2 and Figure 6-3 show the timing diagrams for both early and late CNV lowering scenarios.

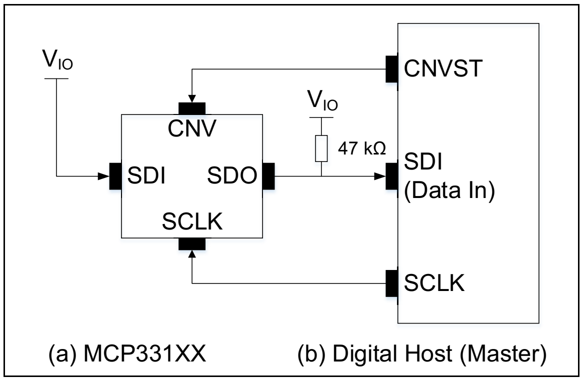


FIGURE 6-1: *Connection Diagram for 3-Wire CS Mode without BUSY Status Indicator Output Bit.*

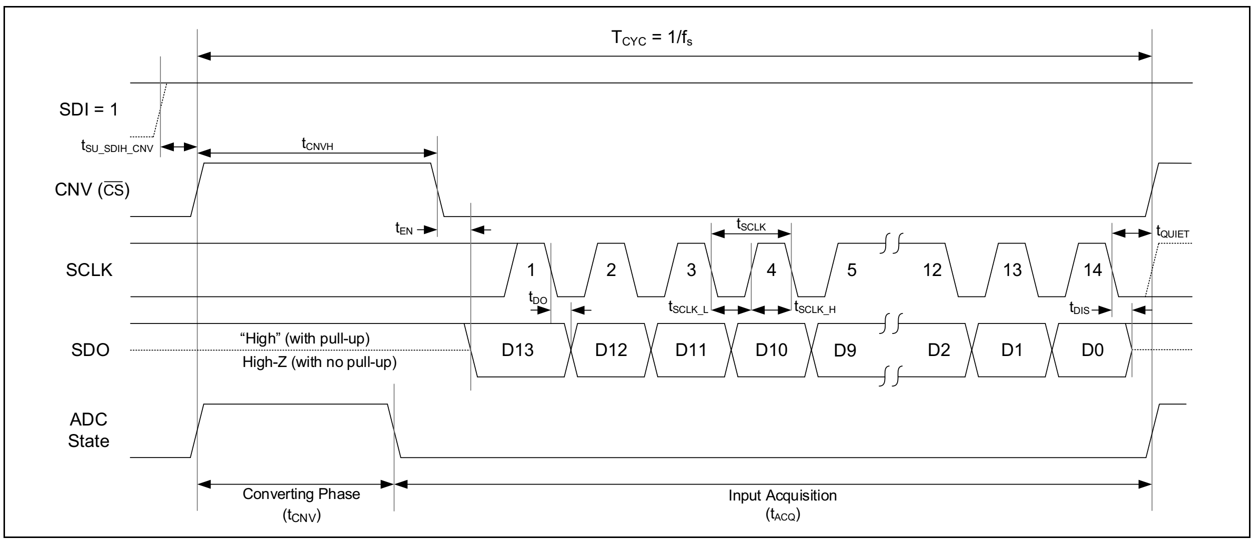


FIGURE 6-2: *Interface Timing Diagram for 3-Wire CS Mode without BUSY Status Indicator Output Bit, Late CNV (Recommended).*

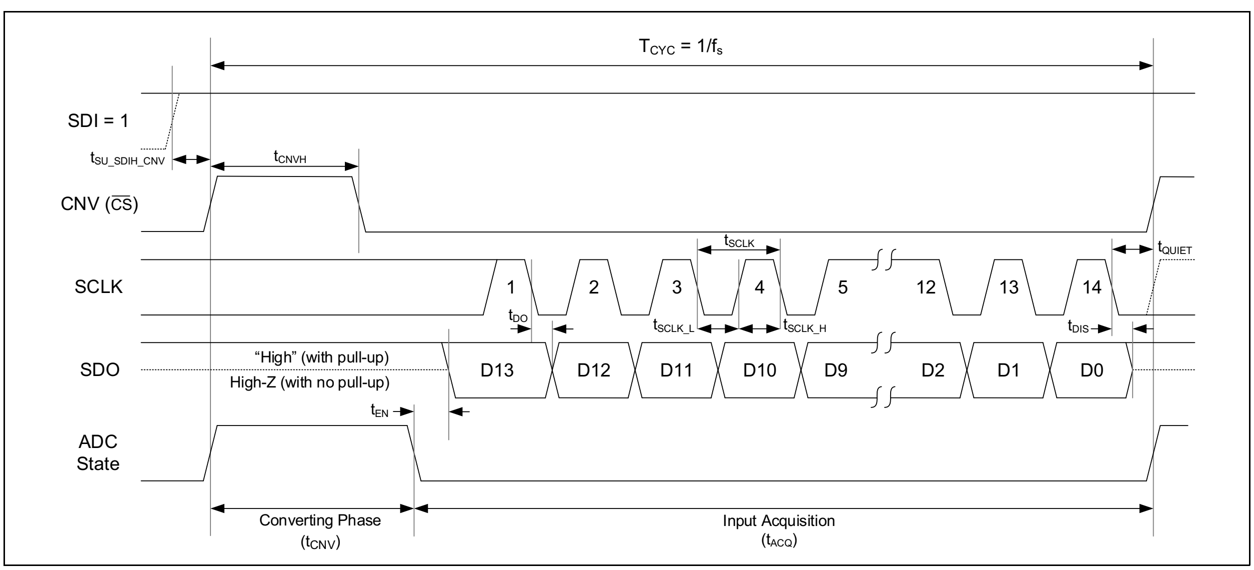


FIGURE 6-3: *Interface Timing Diagram for 3-Wire CS Mode without BUSY Status Indicator Output Bit, Early CNV.*

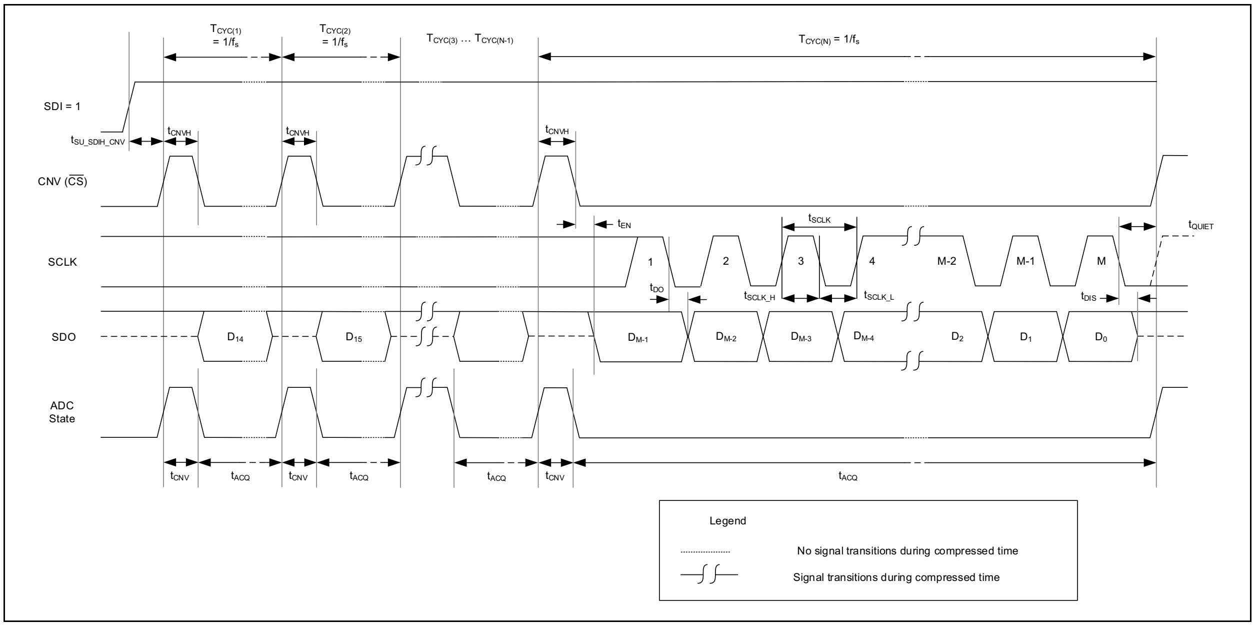


FIGURE 6-4: *Interface Timing Diagram for Accumulator Operation in 3-Wire CS Mode, Without BUSY Status Indicator Output Bit.*

Note:	See **Section 5.7, Data Accumulator** for more details about using the data accumulator feature.

6.1.1.2 3-Wire $\overline{CS}$ Mode with BUSY Output Bit

This interface option is typically used when a single MCP33151/41-XX is connected to an SPI-compatible digital host that has an interrupt ($\overline{IRQ}$) input.

Figure 6-5 shows the connection diagram with the host device. In this mode, CNV functions as both conversion control and $\overline{CS}$.

To enable this interface option, SDI can either be tied to GND, or permanently held in a Logic = 0 state. By doing so, the device will always output a BUSY status bit.

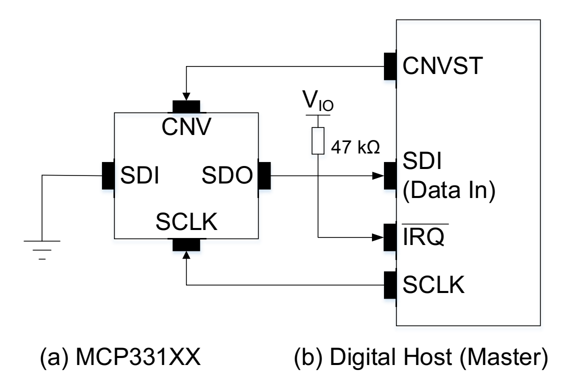
As shown in Figure 6-6, at the rising edge of CNV, conversion is initiated. The SDO pin becomes High-Z state (if no external pull-up is used). Once the conversion is initiated, it continues and completes the conversion regardless of the CNV pin condition. This means the CNV pin can be used for other SPI devices after the conversion is initiated.

When conversion is complete, the device enters an acquisition phase and Power-Down state, SDO comes out of the High-Z state, and outputs a BUSY status indicator bit (Low level). The device exits the acquisition phase when CNV once again returns to a High state. SDO then returns to a High-Z state after the 15th SCLK falling edge or when CNV goes High, whichever occurs first.

Note:	It is recommended that CNV be driven Low before the minimum conversion time (t_{CNV}) expires, and remain Low until the maximum possible conversion time (t_{CONV}) expires. A Low level on the CNV input at the end of a conversion ensures the device generates a BUSY status indicator bit when the ADC has finished converting.

This configuration provides a high-to-low transition on the $\overline{IRQ}$ pin of the digital host by the BUSY bit. The data bits are clocked out, MSB first, on the subsequent SCLK falling edges. Data are valid on both edges of SCLK and can be captured on either edge. However, a digital host capturing data on the SCLK falling edge can achieve a faster reading rate.

Figure 6-6 and Figure 6-7 show the timing diagrams for both early and late CNV lowering scenarios.



Note: This connection can also monitor the calibration status indicator output using $\overline{IRQ}$ pin.

FIGURE 6-5: *Connection Diagram for 3-Wire $\overline{CS}$ Mode with BUSY Status Indicator Output Bit. $\overline{IRQ}$ Pin in the Host Device Is Used for Interrupt Event.*

Note: The pull-up resistor on the SDO pin is highly recommended in this mode as it ensures that the $\overline{IRQ}$ pin of the digital host is held high when SDO goes to High-Z state.

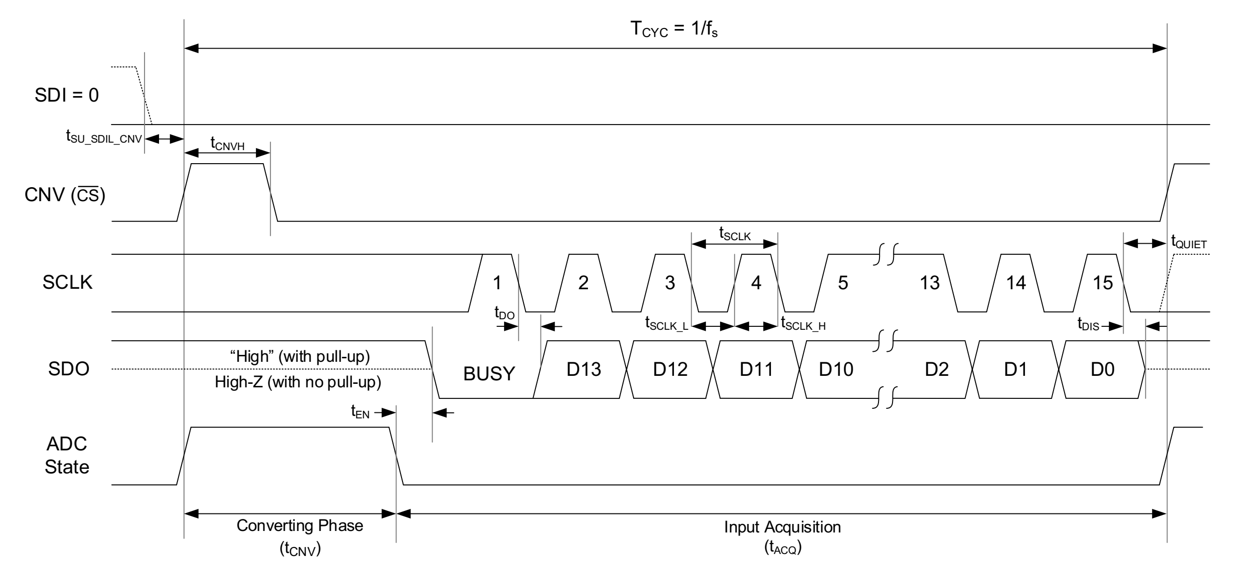


FIGURE 6-6: *Timing Diagram for 3-Wire $\overline{CS}$ Mode with BUSY Status Indicator Output Bit, Early CNV (Recommended).*

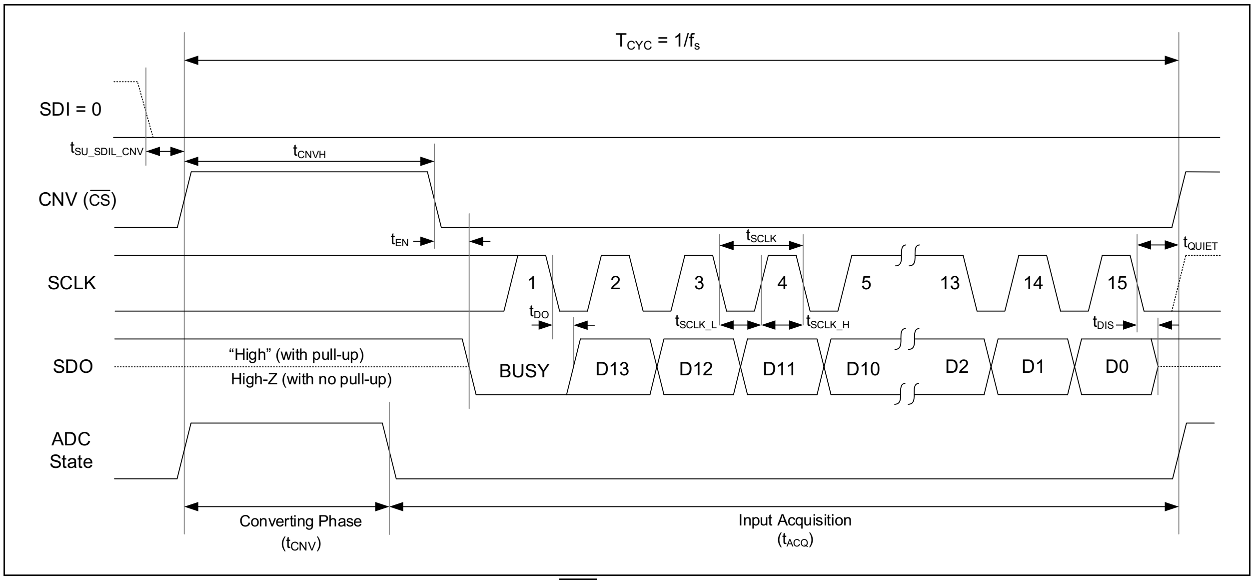


FIGURE 6-7: *Timing Diagram for 3-Wire $\overline{CS}$ Mode with BUSY Status Indicator Output Bit, Late CNV.*

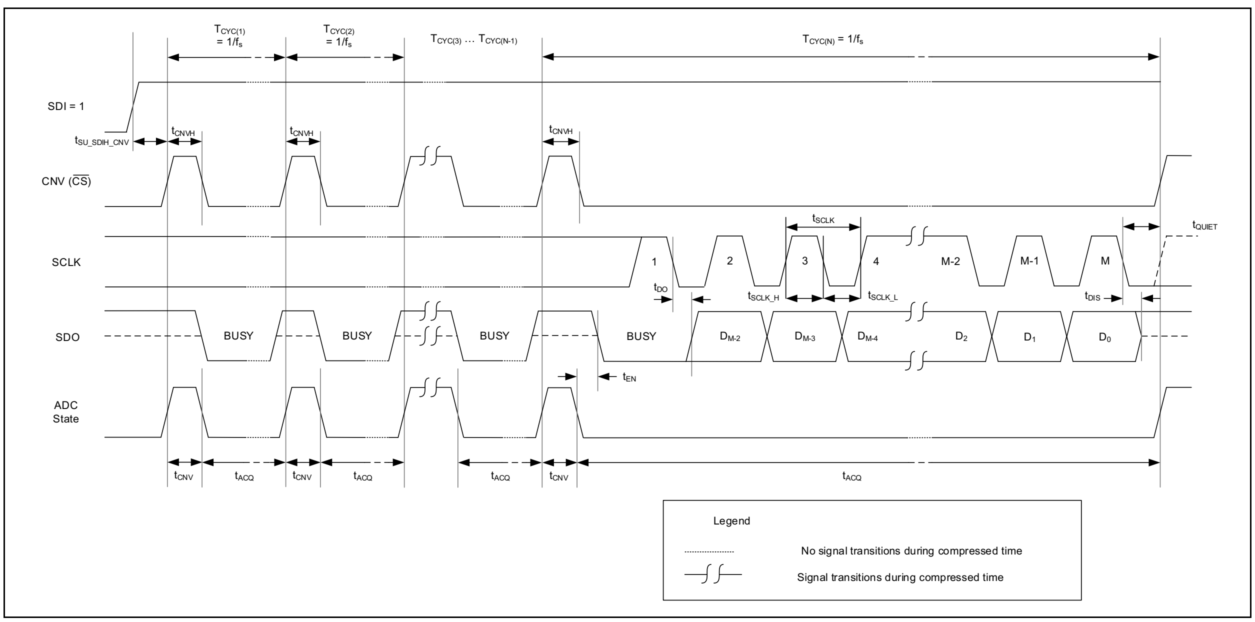


FIGURE 6-8: *Interface Timing Diagram for Accumulator Operation in 3-Wire CS Mode, with BUSY Status Indicator Output Bit.*

Note:	See **Section 5.7, Data Accumulator** for more details about using the data accumulator feature.

6.2 Recalibrate Command

The recalibrate command applies to the following cases:

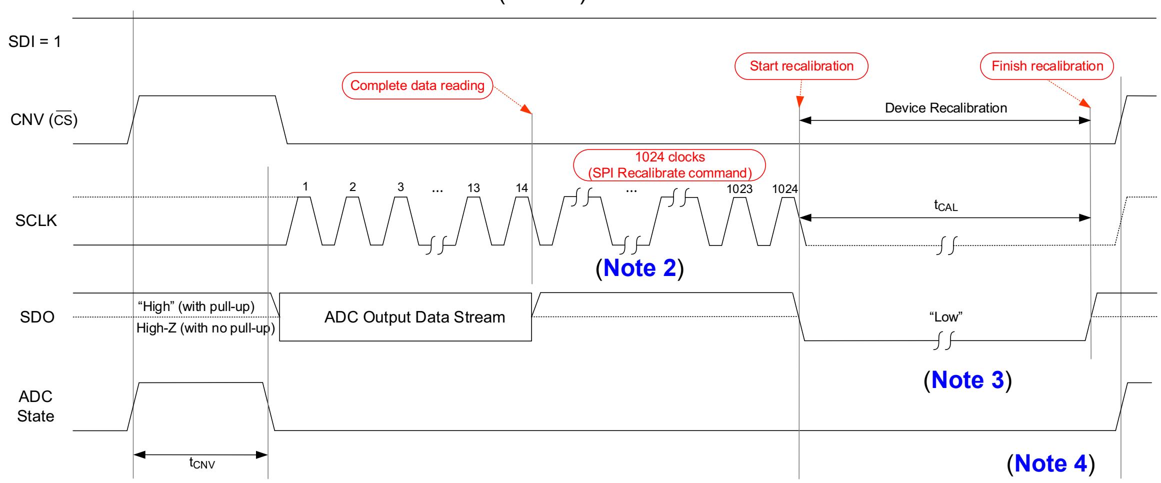
- When the reference voltage was not fully settled during the initial power-on sequence.
- During operation, to ensure optimum performance across varying environment conditions, such as reference voltage and temperature.

A self-calibration is initiated by sending the recalibrate command. The host device sends a recalibrate command by transmitting 1024 SCLK pulses (including the clocks for data bits) while the device is in the acquisition phase (Standby).

The device drives SDO Low during the recalibration procedure, and returns to High-Z once completed. The status of the recalibration procedure can be monitored by placing a pull-up on SDO, so that SDO goes High when the recalibration is complete.

Figure 6-9 shows the recalibrate command timing diagram. The calibration takes approximately 500 ms (t_{CAL}).

(Note 1)



Note 1: SDI must remain High during the entire recalibration cycle.
2: The 1024 clocks include the clocks for data bits.
3: SDO outputs Low during calibration and High-Z when exiting the calibration.
4: After finishing the recalibration procedure, the device is ready for a new input sampling immediately.

FIGURE 6-9: Recalibrate Command Timing Diagram.

Note: When the device performs a calibration, it is important to note that the analog supply voltage (AV_{DD}), the reference voltage (V_{REF}) and the digital I/O interface supply voltage (DV_{IO}) must be stabilized for a correct calibration. This is particularly relevant during the initial power-on sequence. See **Section 4.1.1, Power-Up Sequence and Auto-Calibration** for more details.

7.0 TERMINOLOGY

Analog Input Bandwidth (Full-Power Bandwidth)

The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay or Sampling Delay

This is the time delay between the rising edge of the CNVST input and when the input signal is held for a conversion.

Differential Nonlinearity (DNL, No Missing Codes)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. No missing codes to 16-bit resolution indicates that all 65,536 codes (16,384 codes for 14-bit, 4096 codes for 12-bit) must be present over all the operating conditions.

Integral Nonlinearity (INL)

INL is the maximum deviation of each individual code from an ideal straight line drawn from negative full scale through positive full scale.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), below the Nyquist frequency and excluding the power at DC and the first nine harmonics.

EQUATION 7-1:

$$SNR = 10\log\left(\frac{P_S}{P_N}\right)$$

SNR is either given in units of dBc (dB to carrier), when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale), when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D) below the Nyquist frequency, but excluding DC:

EQUATION 7-2:

$$SINAD = 10\log\left(\frac{P_S}{P_D + P_N}\right) = -10\log\left[10^{-\frac{SNR}{10}} - 10^{-\frac{THD}{10}}\right]$$

SINAD is either given in units of dBc (dB to carrier), when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale), when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB)

The effective number of bits for a sine wave input at a given input frequency can be calculated directly from its measured SINAD using the following formula:

EQUATION 7-3:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Gain Error

Gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error is usually expressed in LSB or as a percentage of full-scale range (%FSR).

Offset Error

Offset error is the difference between the ideal voltage (0V + 0.5 LSB) that produces the first code transition ("`000... 000`" to "`000... 001`") and the actual voltage producing that code.

Temperature Drift

The temperature drift for offset error and gain error specifies the maximum change from the initial (+25°C) value to the value at across the T_{MIN} to T_{MAX} range. The value is normalized by the reference voltage and expressed in µV/°C or ppm/°C.

Maximum Conversion Rate

The maximum clock rate at which parametric testing is performed.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier) or dBFS.

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the summed power of the first 13 harmonics (P_D).

EQUATION 7-4:

$$THD = 10log\left(\frac{P_S}{P_D}\right)$$

THD is typically given in units of dBc (dB to carrier). THD is also shown by:

EQUATION 7-5:

$$THD = -20log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2}}{V_1^2}$$

Where:

V_1 = RMS amplitude of the fundamental frequency

V_1 through V_n = Amplitudes of the second through n^{th} harmonics

Common-Mode Rejection Ratio (CMRR)

Common-mode rejection is the ability of a device to reject a signal that is common to both sides of a differential or pseudodifferential input pair. The Common-mode signal can be an AC or DC signal or a combination of the two. CMRR is measured using the ratio of the differential signal gain to the Common-mode signal gain and expressed in dB with the following equation:

EQUATION 7-6:

$$CMRR = 20log\left(\frac{A_{DIFF}}{A_{CM}}\right)$$

Where:

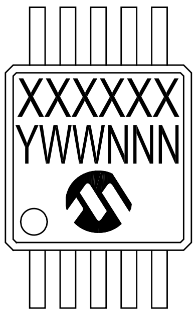
A_{DIFF} = ∆Output Code/∆Differential Voltage

A_{DIFF} = ∆Output Code/∆Common-Mode Voltage

8.0 PACKAGING INFORMATION

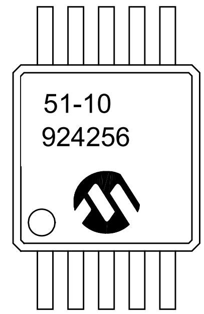
8.1 Package Marking Information

10-Lead MSOP (3 mm x 3 mm)

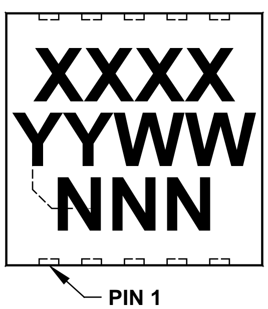


Part Number	Code
MCP33151-10	51-10
MCP33151-05	51-05
MCP33141-10	41-10
MCP33141-05	41-05

Example

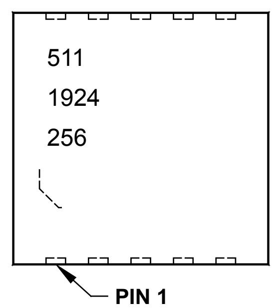


10-Lead TDFN (3 mm x 3 mm x 0.8 mm)



Part Number	Code
MCP33151-10	511
MCP33151-05	510
MCP33141-10	411
MCP33141-05	410

Example

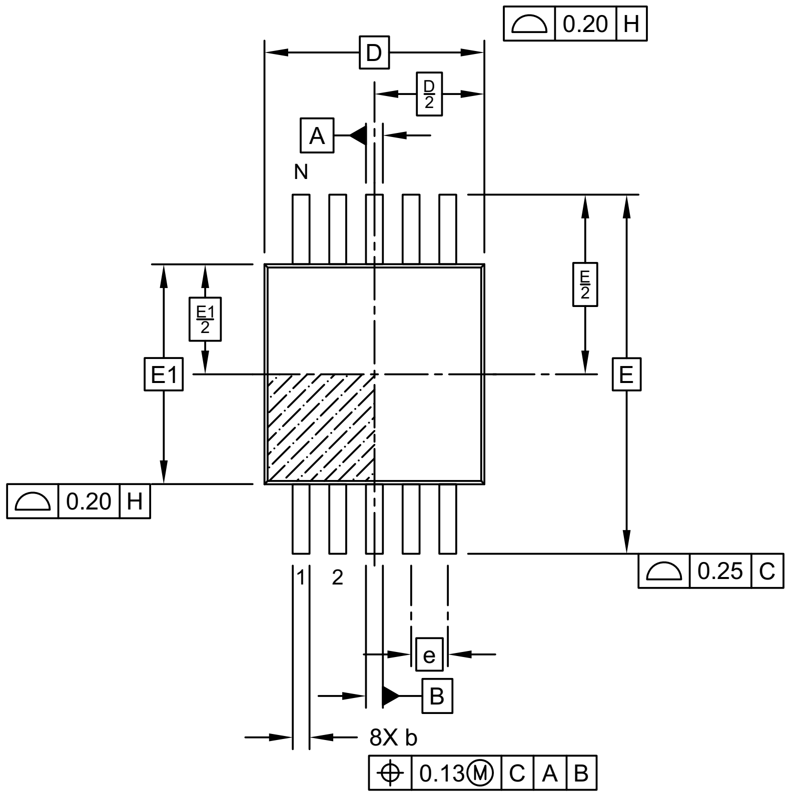


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

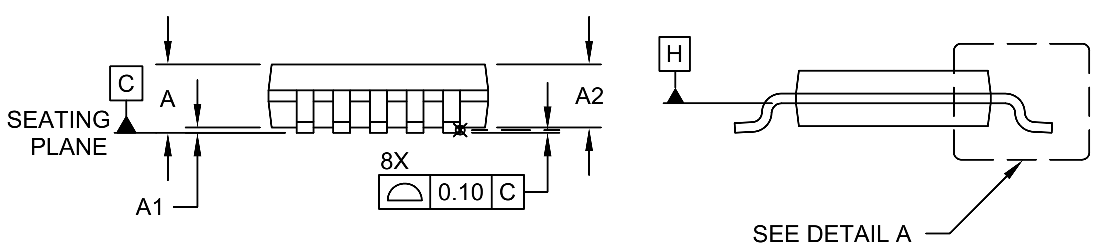
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



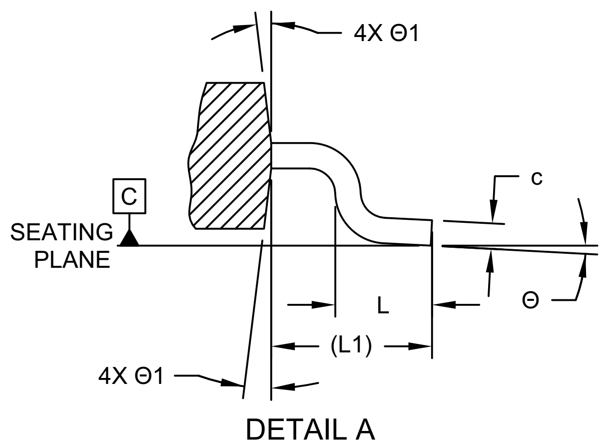
SIDE VIEW

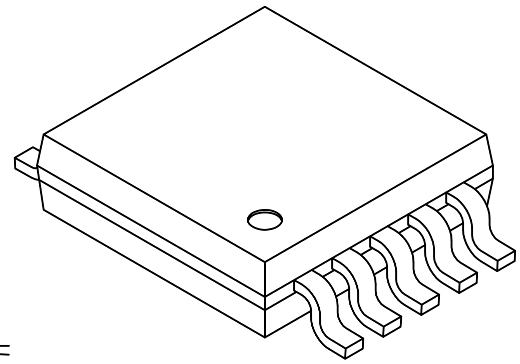
END VIEW

Microchip Technology Drawing C04-021D Sheet 1 of 2

10-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	10		
Pitch	e	0.50 BSC		
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Mold Draft Angle	Θ	0°	-	8°
Foot Angle	Θ1	5°	-	15°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.15	-	0.33

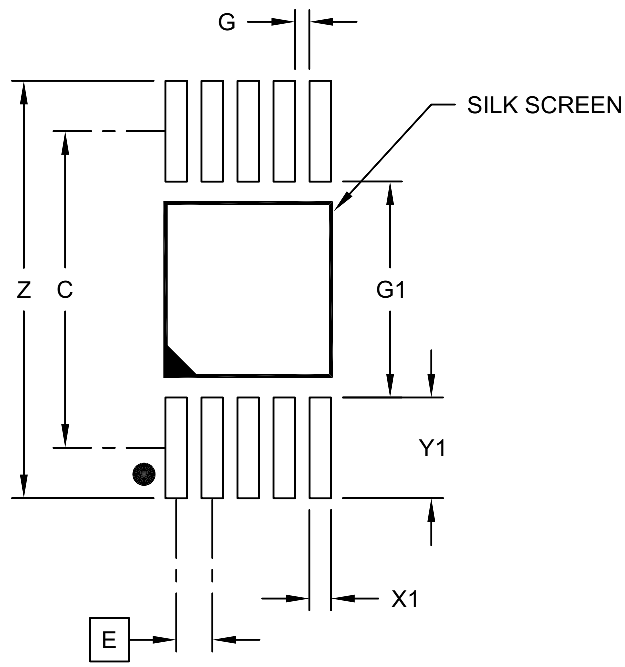
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021D Sheet 2 of 2

10-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.80
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			1.40
Distance Between Pads (X5)	G1	3.00		
Distance Between Pads (X8)	G	0.20		

Notes:

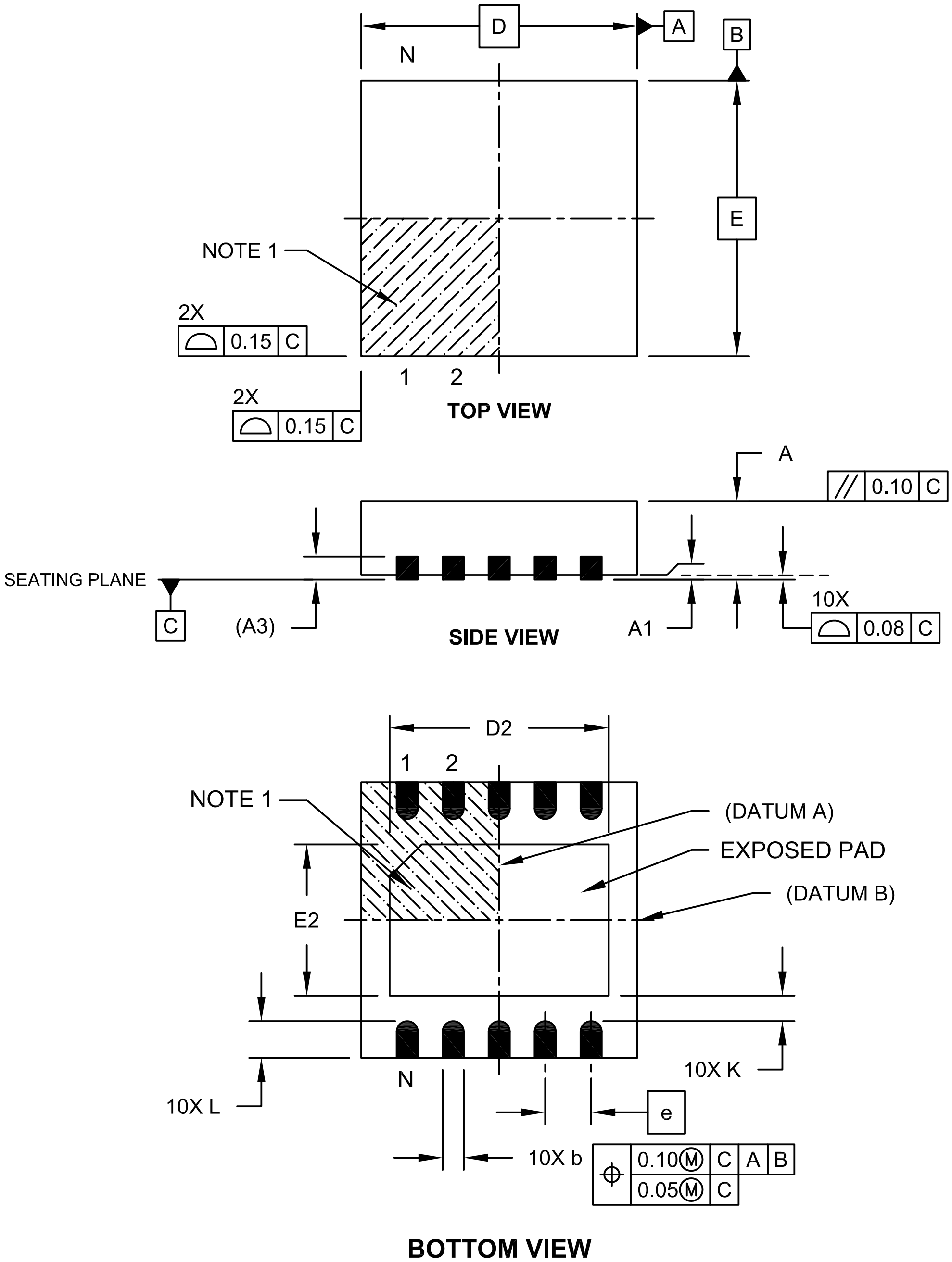
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2021B

10-Lead Thin Plastic Dual Flat, No Lead Package (MN) - 3x3x0.8mm Body [TDFN]

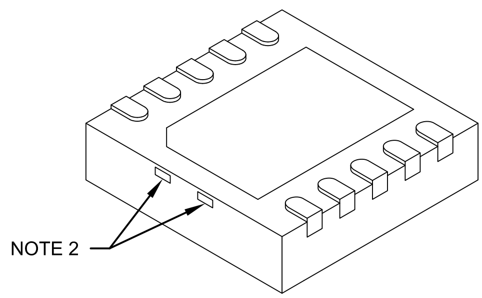
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-185A Sheet 1 of 2

10-Lead Thin Plastic Dual Flat, No Lead Package (MN) - 3x3x0.8mm Body [TDFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.20	2.30	2.35
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.55	1.65	1.70
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-0185A Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision A (June 2019)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	–XX	X	–X	/XX
Device	Input Type	Sample Rate	Tape and Reel	Temperature Range	Package

Device:	MCP33151-10:	1 Msps, 14-Bit Single-Ended Input SAR ADC
	MCP33141-10:	1 Msps, 12-Bit Single-Ended Input SAR ADC
	MCP33151-05:	500 ksps, 14-Bit Single-Ended Input SAR ADC
	MCP33141-05:	500 ksps, 12-Bit Single-Ended Input SAR ADC
Input Type	Blank	=Single-Ended Input
Sample Rate:	10	= 1 Msps
	05	= 500 kSPS
Tape and Reel Option:	Blank	= Standard packaging (tube or tray)
	T	= Tape and Reel
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	MS	= Plastic Micro Small Outline Package (MSOP), 10-Lead
	MN	= Thin Plastic Dual Flat No, Lead Package (TDFN), 10-Lead

Examples:

a) MCP33151-10-E/MS: 1 Msps, 14-bit device, 10-LD MSOP

b) MCP33151-10T-E/MS: 1 Msps, 14-bit device, 10-LD MSOP, Tape and Reel

c) MCP33151-10-E/MN: 1 Msps, 14-bit device, 10-LD TDFN

d) MCP33151-10T-E/MN: 1 Msps, 14-bit device, 10-LD TDFN, Tape and Reel

e) MCP33141-10-E/MS: 1 Msps, 12-bit device, 10-LD MSOP

f) MCP33141-10T-E/MS: 1 Msps, 12-bit device, 10-LD MSOP, Tape and Reel

g) MCP33141-10-E/MN: 1 Msps, 12-bit device, 10-LD TDFN

h) MCP33141-10T-E/MN: 1 Msps, 12-bit device, 10-LD TDFN, Tape and Reel

i) MCP33151-05-E/MS: 500 ksps, 14-bit device, 10-LD MSOP

j) MCP33151-05T-E/MS: 500 ksps, 14-bit device, 10-LD MSOP, Tape and Reel

k) MCP33151-05-E/MN: 500 ksps, 14-bit device, 10-LD TDFN

l) MCP33151-05T-E/MN: 500 ksps, 14-bit device, 10-LD TDFN, Tape and Reel

m) MCP33141-05-E/MS: 500 ksps, 12-bit device, 10-LD MSOP

n) MCP33141-05T-E/MS: 500 ksps, 12-bit device, 10-LD MSOP, Tape and Reel

o) MCP33141-05-E/MN: 500 ksps, 12-bit device, 10-LD TDFN

p) MCP33141-05T-E/MN: 500 ksps, 12-bit device, 10-LD TDFN, Tape and Reel

Note 1: Tape and Reel identifier appears only in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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