MICROCHIP

MCP6496/6R/6U/7/9

30 MHz Operational Amplifier with EMI Filtering

Features

- Low-Input Offset Voltage:
  - ±1.6 mV (maximum)
- Quiescent Current: 2.5 mA (maximum)/amplifier
- Enhanced EMI Protection
- Supply Voltage Range: 1.8V to 5.5V
- Gain Bandwidth Product: 30 MHz (typical)
- Rail-to-Rail Input/Output
- Unity Gain Stable
- No Phase Reversal
- Quick Start-up Time: 2 µs typical
- Small Packages:
  - Singles in SC70-5, SOT-23-5
  - Dual in SOIC-8, MSOP-8
  - Quad in SOIC-14, TSSOP-14
- Extended Temperature Range:-40°C to +125°C
- AEC Q100 qualified

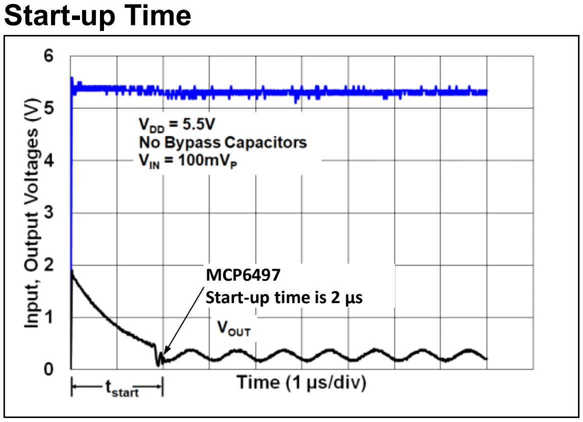
Applications

- Automotive
- Portable Equipment
- Medical Diagnostic Equipment
- Active Filters
- Sensor Conditioning

Design Aids

- SPICE Macro Models
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Start-up Time



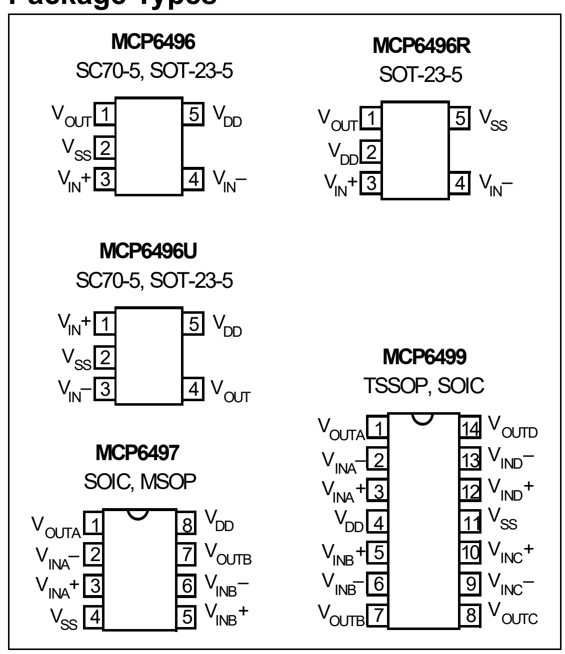
Description

The Microchip Technology Inc. MCP6496/6R/6U/7/9 operational amplifier operates with a single supply voltage as low as 1.8V, while drawing low quiescent current (2.5 mA, maximum per amplifier). This op amp also has low-input offset voltage (±1.6 mV, maximum) and rail-to-rail input and output operation. In addition, the MCP6496/6R/6U/7/9 is unity gain stable and has a gain bandwidth product of 30 MHz (typical).

The MCP6496/6R/6U/7/9 has EMI protection to minimize the effects of electromagnetic interference from external sources. This feature makes it suited for EMI sensitive applications such as power lines, radio stations and mobile communications.

This family is offered in single (MCP6496), dual (MCP6497) and quad (MCP6499) packages. All devices are designed using an advanced CMOS process and fully specified in the extended temperature range from -40°C to +125°C.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} – V_{SS}$ 6V
Current at Analog Input Pins (V_{IN}+, V_{IN}-) ....±5 mA
Analog Inputs (V_{IN}+, V_{IN}-)†† .... V_{SS} – 0.5V to V_{DD} + 0.5V
Analog Outputs (V_{OUT}).................... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage .... $|V_{DD} – V_{SS}|$
Output Short-Circuit Current (Note 1)....................Continuous
Storage Temperature....................-65°C to +150°C
Maximum Junction Temperature (T_J) ....+150°C
ESD Protection on All Pins (HBM; CDM; MM) ....≥ 4 kV; 2 kV; 200V

Note 1: Short-circuit to ground, one amplifier per package

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage Limits"**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Electrical Characteristics: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/4, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF.						
Input Offset						
Input Offset Voltage	V_{OS}	-1.6	—	1.6	mV	
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±0.6	—	µV/°C	T_A= -40°C to +125°C
Power Supply Rejection Ratio	PSRR	82	100	—	dB	
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1	—	pA	
		—	19	—	pA	T_A = +85°C
		—	200	—	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||2	—	Ω||pF	
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS} - 0.3	—	V_{DD} + 0.3	V	
		V_{SS} - 0.1	—	V_{DD} + 0.1		T_A= -40°C to +125°C, Guaranteed by Characterization.
Common Mode Rejection Ratio	CMRR	—	125	—	dB	V_{DD} = 5.5V V_{CM} = -0.1V to 4.1V
		66	92	—	dB	V_{DD} = 5.5V V_{CM} = -0.3V to 5.8V
		—	75	—	dB	V_{DD} = 1.8V V_{CM} = -0.3V to 2.1V

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/4, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	105	130	—	dB	0.2 < V_{OUT} < (V_{DD} -0.2V)
Output						
High-Level Output Voltage	V_{OH}	V_{DD} - 10	V_{DD} - 3.5	—	mV	V_{DD} = 5.5V, R_L = 10 kΩ
		V_{DD} - 50	V_{DD} - 30	—		V_{DD} = 5.5V, R_L = 1 kΩ
Low-Level Output Voltage	V_{OL}	—	V_{SS} + 3.5	V_{SS} + 10	mV	V_{DD} = 5.5V, R_L = 10 kΩ
		—	V_{SS} + 30	V_{SS} + 50		V_{DD} = 5.5V, R_L = 1 kΩ
Output Short-Circuit Current	I_{SC}	—	±15.5	—	mA	V_{DD} = 1.8V, source
		—	±8.5	—	mA	V_{DD} = 1.8V, sink
		—	±55	—	mA	V_{DD} = 5.5V, source
		—	±45	—	mA	V_{DD} = 5.5V, sink
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Amplifier	I_Q	—	2.0	2.5	mA	I_O = 0
Startup Time	t_{start}	—	2	—	µs	V_{DD} = 0V to 5.5V
Crosstalk		—	122	—	dB	

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/4, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
AC Response						
Gain Bandwidth Product	GBWP	—	30	—	MHz	
Phase Margin	PM	—	53	—	°	G = +1 V/V
Slew Rate	SR	—	40	—	V/µs	V_{DD} = 5.5V
Settling Time	t_s	—	0.4	—	µs	To 0.1%, V_{DD} = 5V, 2V step, G = +1
		—	0.5	—		To 0.01%, V_{DD} = 5V, 2V step, G = +1
Total Harmonic Distortion + Noise	THD+N	—	0.002	—	%	V_{DD} = 5V, V_o = 1V_{RMS}, G = +1, f = 1 kHz, 80 kHz measurement BW
Noise						
Input Noise Voltage	E_{ni}	—	3.3	—	µV_{P-P}	f = 0.1 Hz to 100 Hz
Input Noise Voltage Density	e_{ni}	—	12	—	nV/√Hz	f = 1 kHz
		—	4.8	—	nV/√Hz	f = 100 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz
Electromagnetic Interference Rejection Ratio	EMIRR	—	30	—	dB	V_{IN} = 100 mV_{PK}, 400 MHz
		—	42	—		V_{IN} = 100 mV_{PK}, 900 MHz
		—	49	—		V_{IN} = 100 mV_{PK},1800 MHz
		—	51	—		V_{IN} = 100 mV_{PK}, 2400 MHz
		—	52	—		V_{IN} = 100 mV_{PK}, 5800 MHz

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V and V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	221	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	150	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/4, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF.

2.1 DC Inputs

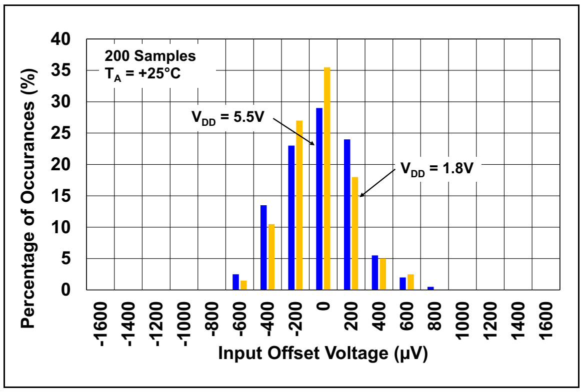


FIGURE 2-1: *Input Offset Voltage Histogram.*

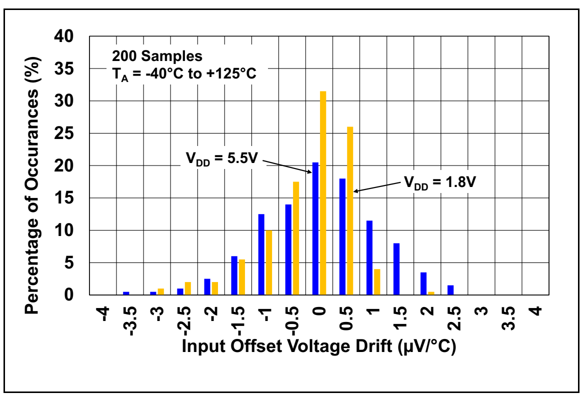


FIGURE 2-2: *Input Offset Voltage Drift Histogram.*

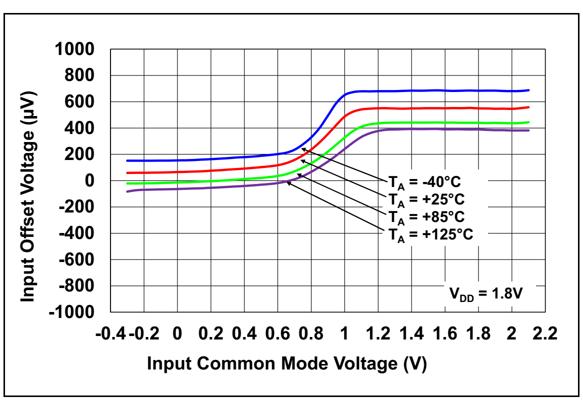


FIGURE 2-3: *Input Offset Voltage vs. Common-Mode Input Voltage.*

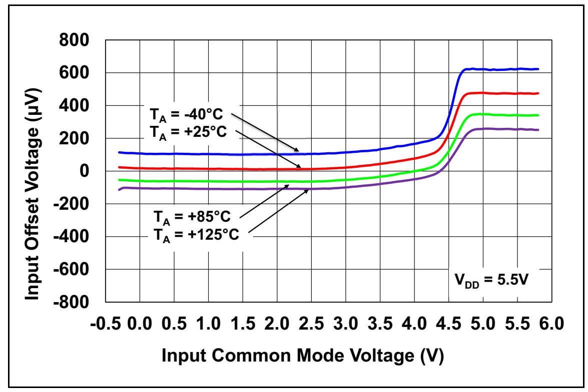


FIGURE 2-4: *Input Offset Voltage vs. Common-Mode Input Voltage.*

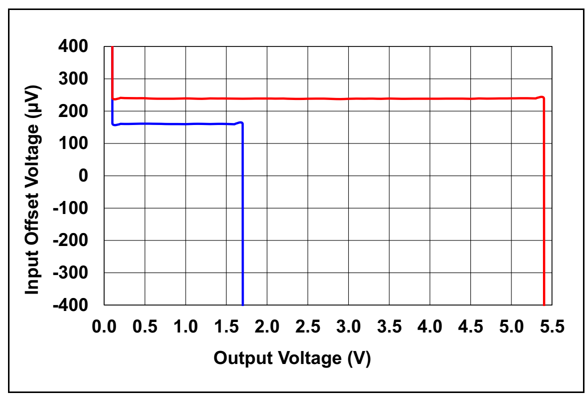


FIGURE 2-5: *Input Offset Voltage vs. Output Voltage.*

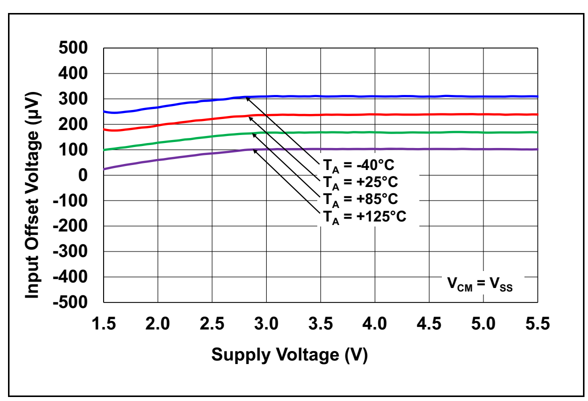


FIGURE 2-6: *Input Offset Voltage vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/4, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF.

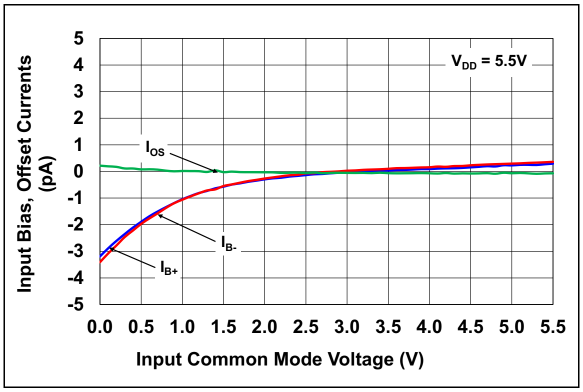


FIGURE 2-7: *Input Bias, Offset Current vs. Common-Mode Input Voltage.*

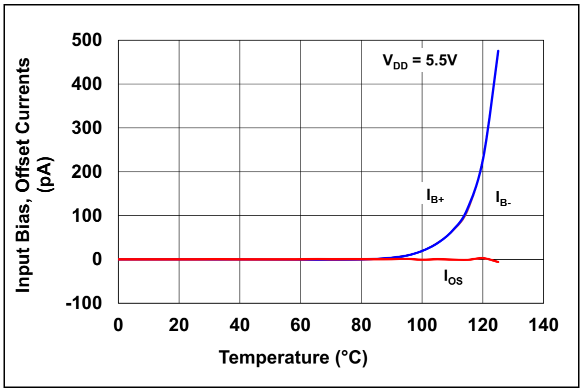


FIGURE 2-8: *Input Bias, Offset Currents vs. Common Mode Input Voltage.*

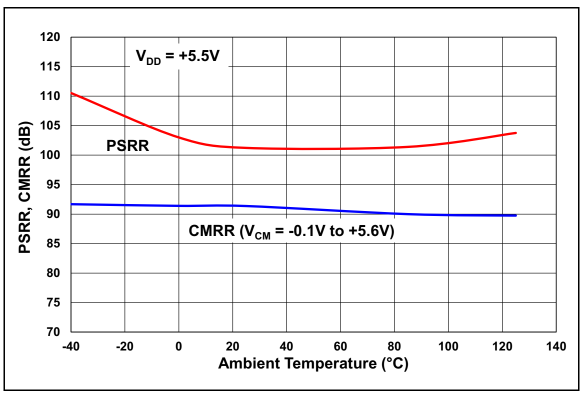


FIGURE 2-9: *CMRR, PSRR vs. Ambient Temperature.*

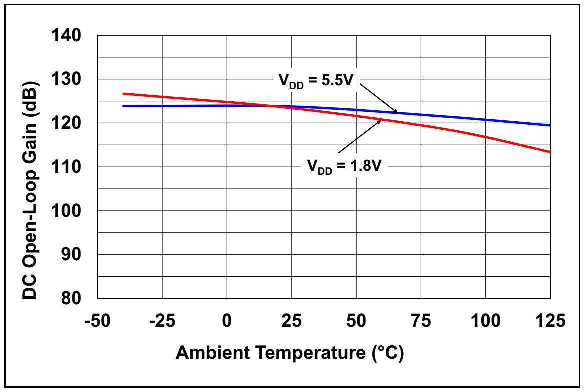


FIGURE 2-10: *DC Open-Loop Gain vs. Ambient Temperature.*

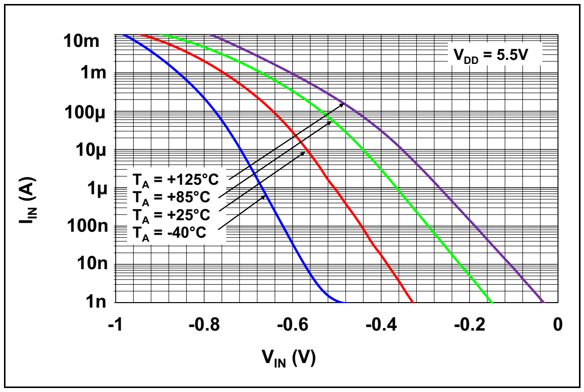


FIGURE 2-11: *Measured Input Current vs. Input Voltage (below V_{SS}).*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/4, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF.

2.2 Other DC Voltages and Currents

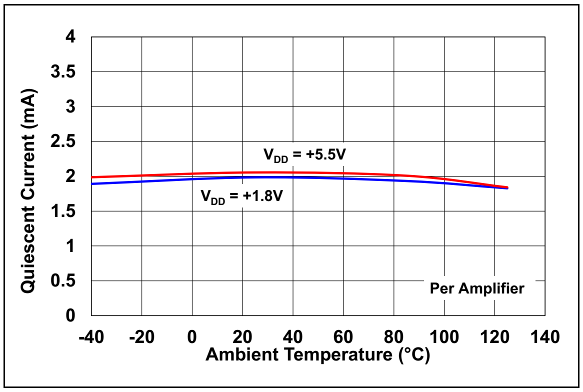


FIGURE 2-12: *Quiescent Current vs. Ambient Temperature.*

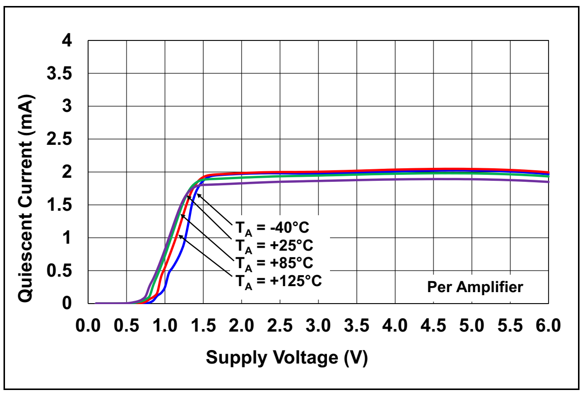


FIGURE 2-13: *Quiescent Current vs. Power Supply Voltage.*

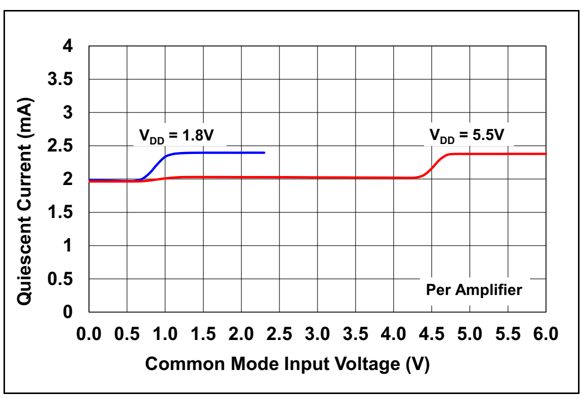


FIGURE 2-14: *Quiescent Current vs. Common-Mode Input Voltage.*

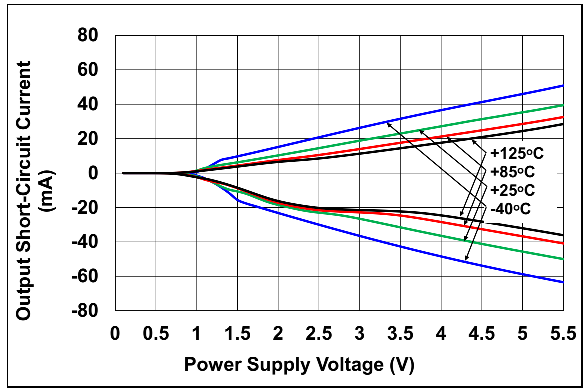


FIGURE 2-15: *Output Short-Circuit Current vs. Power Supply Voltage.*

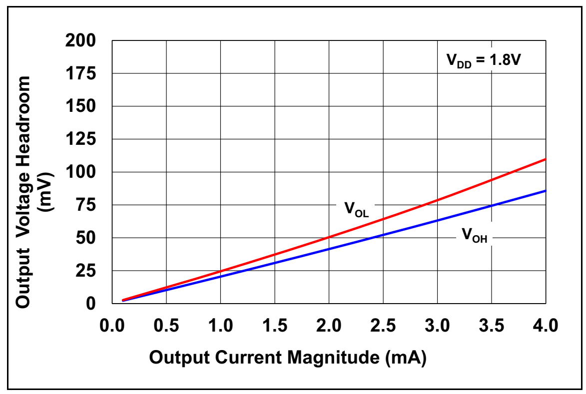


FIGURE 2-16: *Output Voltage Headroom vs. Output Current.*

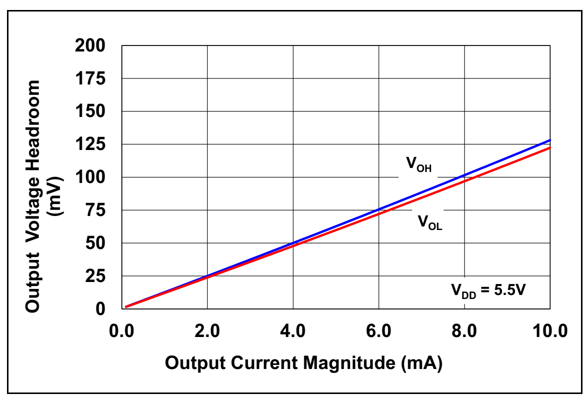


FIGURE 2-17: *Output Voltage Headroom vs. Output Current.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/4$, V_{OUT} = $V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 30 pF.

2.3 Frequency Response

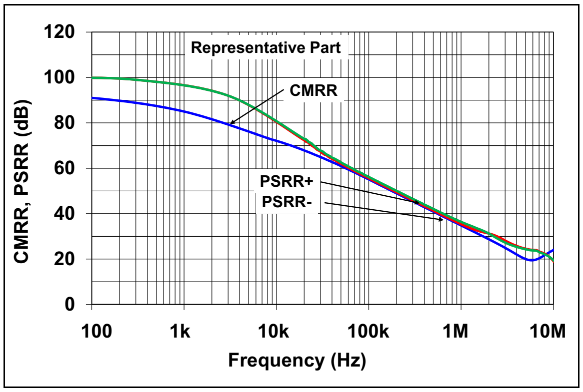


FIGURE 2-18: *CMRR, PSRR vs. Frequency.*

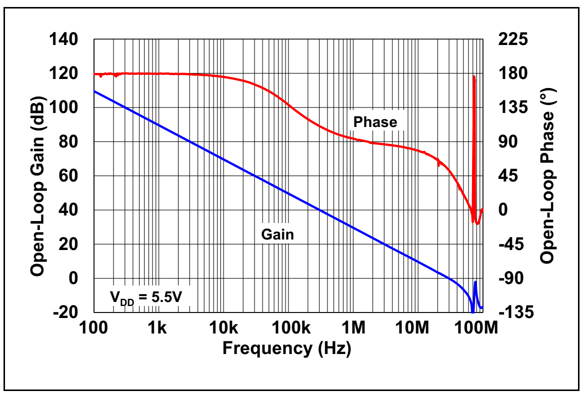


FIGURE 2-19: *Open-Loop Gain, Phase vs. Frequency.*

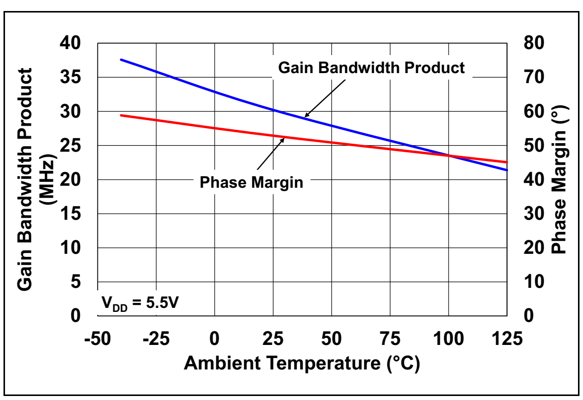


FIGURE 2-20: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

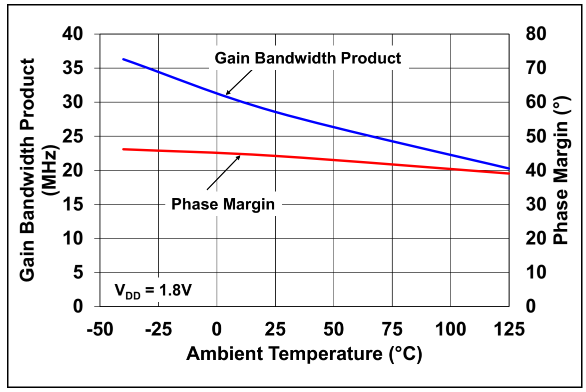


FIGURE 2-21: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

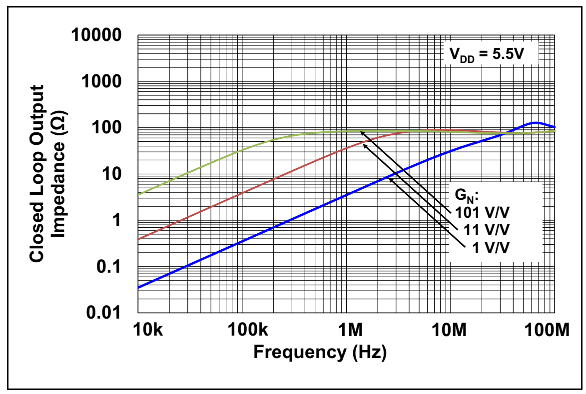


FIGURE 2-22: *Closed-Loop Output Impedance vs. Frequency.*

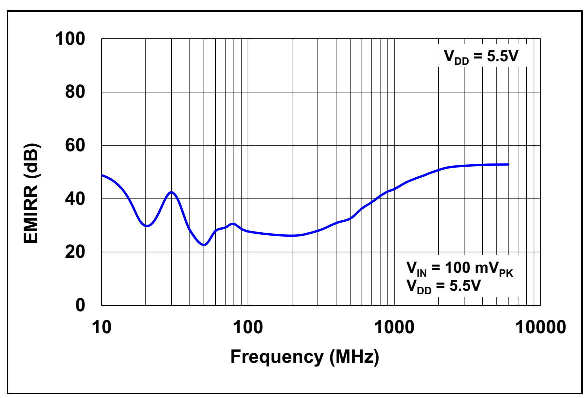


FIGURE 2-23: *EMIRR vs. Frequency.*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/4, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF.

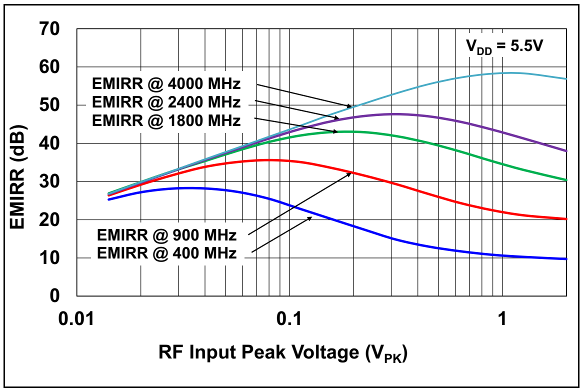


FIGURE 2-24: *EMIRR vs. RF Input Peak-to-Peak Voltage.*

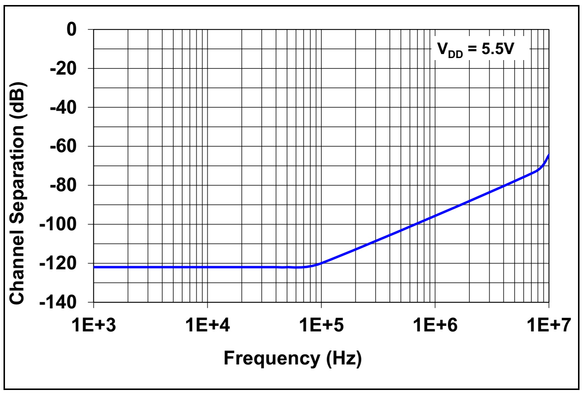


FIGURE 2-25: *Channel Separation vs. Frequency.*

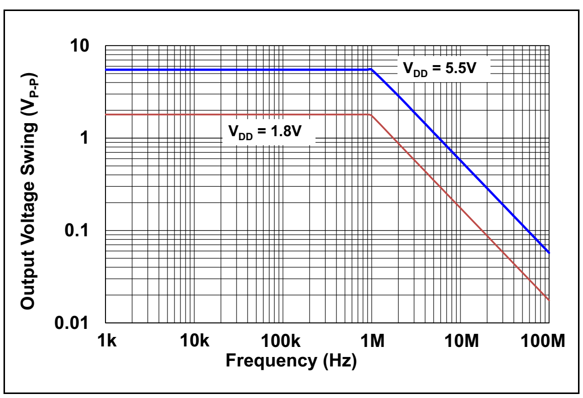


FIGURE 2-26: *Maximum Output Voltage Swing vs. Frequency.*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/4, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF.

2.4 Input Noise

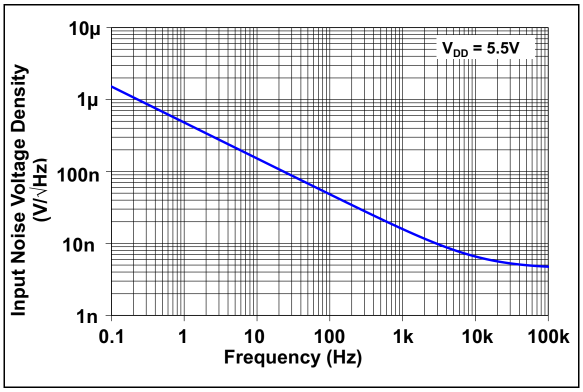


FIGURE 2-27: *Input Noise Voltage Density vs. Frequency.*

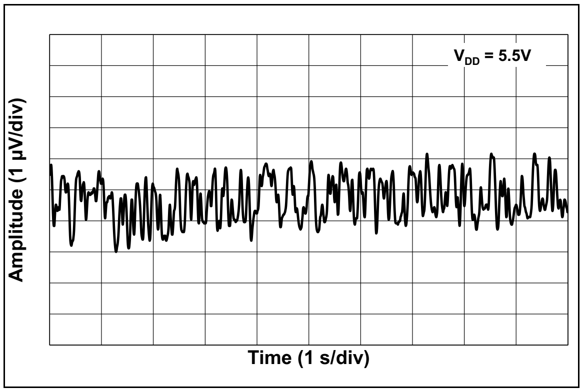


FIGURE 2-28: *0.1 Hz to 10 Hz Voltage Noise.*

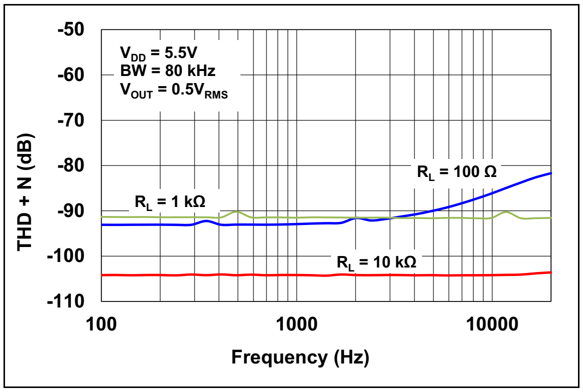


FIGURE 2-29: *THD + N vs. Frequency.*

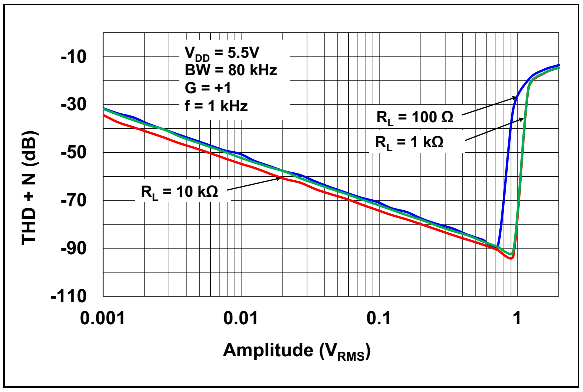


FIGURE 2-30: *THD + N vs. Amplitude.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/4$, V_{OUT} = $V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 30 pF.

2.5 Time Response

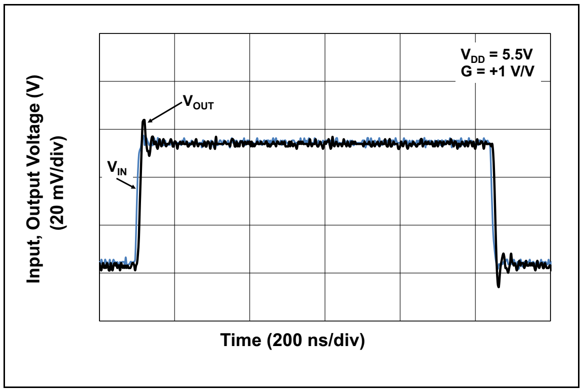


FIGURE 2-31: *Small Signal Noninverting Pulse Response.*

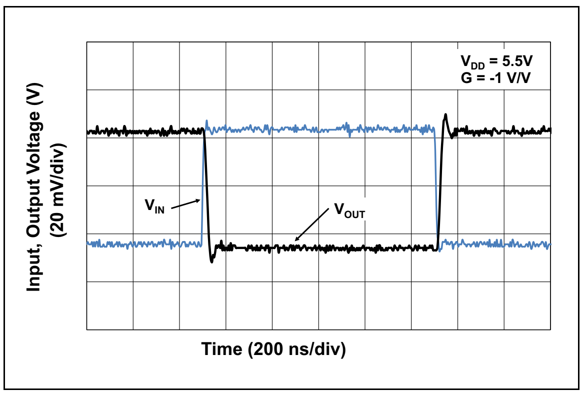


FIGURE 2-32: *Small Signal Inverting Pulse Response.*

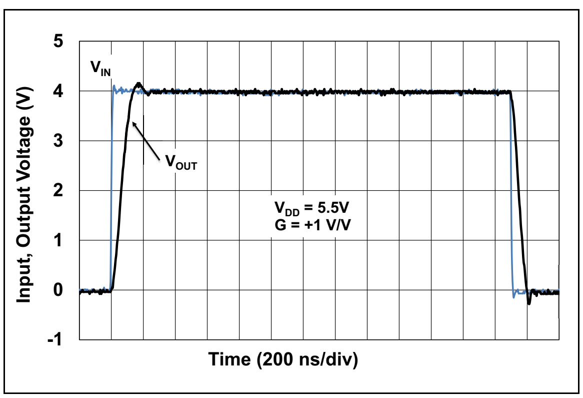


FIGURE 2-33: *Large Signal Noninverting Pulse Response.*

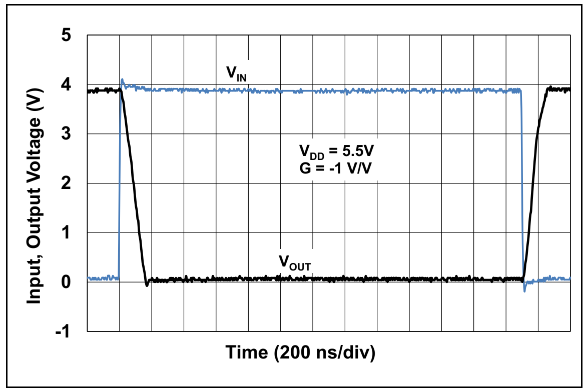


FIGURE 2-34: *Large Signal Inverting Pulse Response.*

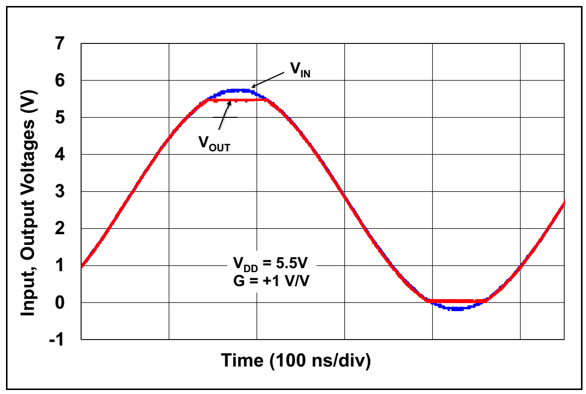


FIGURE 2-35: *The MCP6496/6R/6U/7/9 Device Shows No Phase Reversal.*

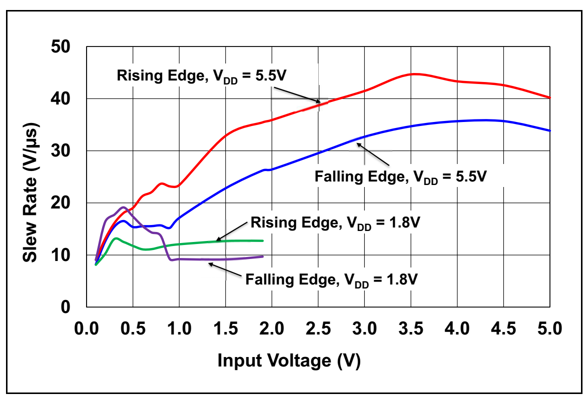


FIGURE 2-36: *Slew Rate vs. Input Voltage.*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/4, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 30 pF.

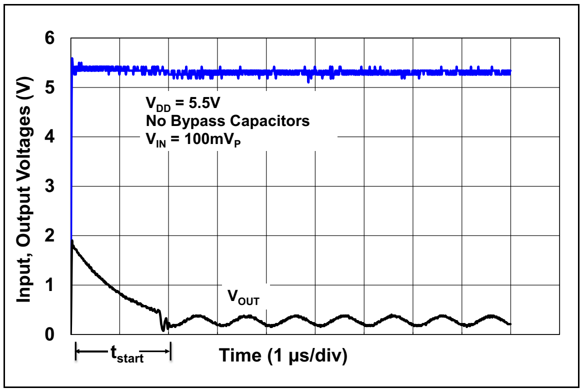


FIGURE 2-37: *Start-up Time.*

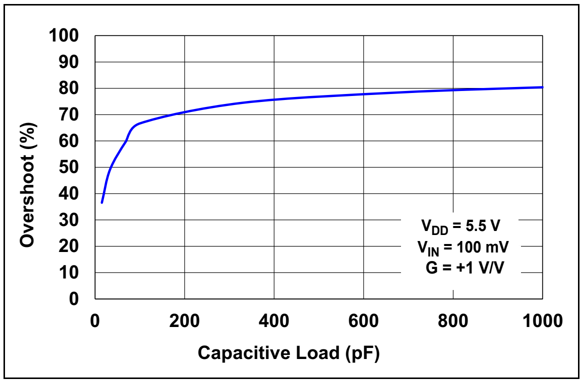


FIGURE 2-38: *Overshoot vs. Capacitive Load.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1, Table 3-2, and Table 3-3.

TABLE 3-1: PIN FUNCTION TABLE - SINGLES

MCP6496	MCP6496R	MCP6496U	Symbol	Description
5-Lead SC70, SOT-23	5-Lead SOT-23	5-Lead SC70, SOT-23		
1	1	4	V_{OUT}	Analog Output
2	5	2	V_{SS}	Negative Power Supply
3	3	1	$V_{IN}+$	Noninverting Input
4	4	3	$V_{IN}-$	Inverting Input
5	2	5	V_{DD}	Positive Power Supply

TABLE 3-2: PIN FUNCTION TABLE - DUALS

MCP6497	Symbol	Description
8-Lead MSOP, SOIC		
1	V_{OUTA}	Analog Output; Op Amp A
2	$V_{INA}-$	Inverting Input; Op Amp A
3	$V_{INA}+$	Noninverting Input; Op Amp A
4	V_{SS}	Negative Power Supply
5	$V_{INB}+$	Noninverting Input; Op Amp B
6	$V_{INB}-$	Inverting Input; Op Amp B
7	V_{OUTB}	Analog Output; Op Amp B
8	V_{DD}	Positive Power Supply

TABLE 3-3: PIN FUNCTION TABLE - QUADS

MCP6499	Symbol	Description
14-Lead TSSOP, SOIC		
1	V_{OUTA}	Analog Output; Op Amp A
2	$V_{INA}-$	Inverting Input; Op Amp A
3	$V_{INA}+$	Noninverting Input; Op Amp A
4	V_{DD}	Positive Power Supply
5	$V_{INB}+$	Noninverting Input; Op Amp B
6	$V_{INB}-$	Inverting Input; Op Amp B
7	V_{OUTB}	Analog Output; Op Amp B
8	V_{OUTC}	Analog Output; Op Amp C
9	$V_{INC}-$	Inverting Input; Op Amp C
10	$V_{INC}+$	Noninverting Input; Op Amp C
11	V_{SS}	Negative Power Supply
12	$V_{IND}+$	Noninverting Input; Op Amp D
13	$V_{IND}-$	Inverting Input; Op Amp D
14	V_{OUTD}	Analog Output; Op Amp D

3.1 Analog Outputs

The analog output pins (V_{OUTx}) are low-impedance voltage sources.

3.2 Analog Inputs

The noninverting and inverting inputs (V_{INx}+, V_{INx}-) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins (V_{SS}, V_{DD})

The positive power supply (V_{DD}) is 1.8V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} needs bypass capacitors.

4.0 APPLICATION INFORMATION

The MCP6496/6R/6U/7/9 operational amplifier is unity gain stable and suitable for a wide range of general-purpose applications.

4.1 Rail-to-Rail Input

4.1.1 PHASE REVERSAL

The MCP6496/6R/6U/7/9 op amp is designed to prevent phase reversal, when the input pins exceed the supply voltages. Figure 2-35 shows the input voltage exceeding the supply voltage with no phase reversal.

4.1.2 INPUT VOLTAGE LIMITS

In order to prevent damage and/or improper operation of the amplifier, the circuit must limit the voltages at the input pins (see **Section 1.1, Absolute Maximum Ratings †**).

The Electrostatic Discharge (ESD) protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors against many, but not all, overvoltage conditions, and to minimize the input bias current (I_B).

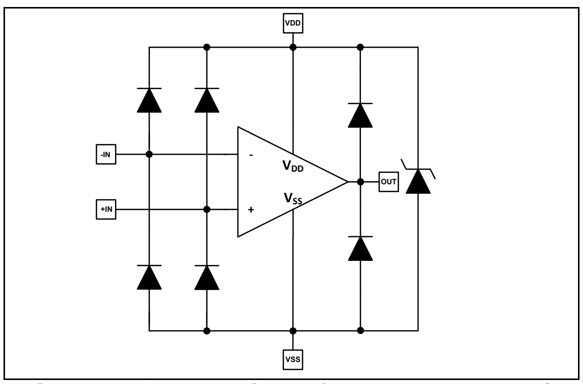


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go well above V_{DD}; their breakdown voltage is high enough to allow normal operation. At 0.5V above V_{DD} or below V_{SS}, the input currents are typically less than 5 mA. Very fast ESD events that meet the specifications are limited so that damage does not occur.

4.1.3 INPUT CURRENT LIMITS

In order to prevent damage and/or improper operation of the amplifier, the circuit must limit the currents into the input pins (see **Section 1.1, Absolute Maximum Ratings †**).

Figure 4-2 shows one approach to protecting these inputs. The resistors R_1 and R_2 limit the possible currents in or out of the input pins through the ESD diodes to either V_{DD} or V_{SS}.

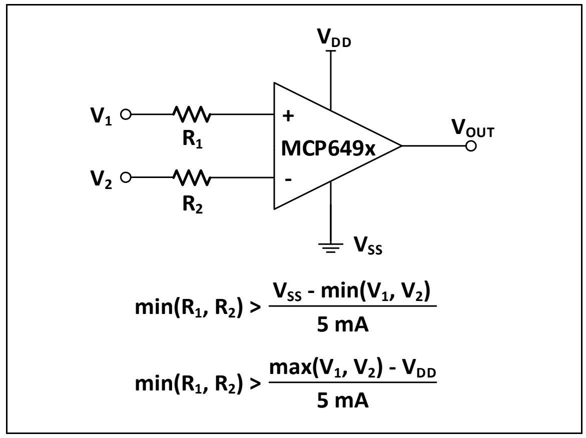


FIGURE 4-2: *Protecting the Analog Inputs.*

4.1.4 NORMAL OPERATION

The input stage of the MCP6496/6R/6U/7/9 op amp uses two differential input stages in parallel. One operates at a low common mode input voltage (V_{CM}), while the other operates at a high V_{CM}. With this topology, the device operates with a V_{CM} up to 300 mV above V_{DD} and 300 mV below V_{SS}. The input offset voltage is measured at $V_{CM} = V_{SS} - 0.3V$ and $V_{DD} + 0.3V$ to ensure proper operation.

The transition between the input stages occurs when V_{CM} is near $V_{DD} - 0.9V$ (see Figures 2-3 and 2-4). For the best distortion performance and gain linearity, with noninverting gains, avoid this region of operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6496/6R/6U/7/9 op amp is 0.003V (typical) and 5.497V (typical) when $R_L = 10\ k\Omega$ is connected to $V_{DD}/2$ and $V_{DD} = 5.5V$. Refer to Figures 2-16 and 2-17 for more information.

4.3 Start-up

The MCP6496/6R/6U/7/9 family of parts quickly controls the output when power (V_{DD}) is initially applied to the device (start-up). Bypass capacitors are removed during the start-up testing to minimize the inrush currents (see Figure 4-3). When the op amp is controlled and is off, the output impedance is high and V_{OUT} is the input sine wave; this is used as the start-up time.

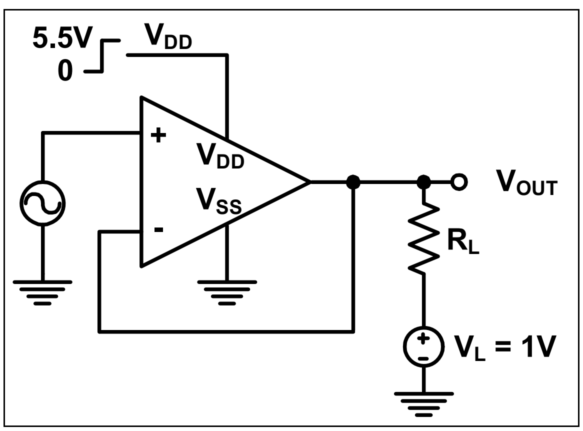


FIGURE 4-3: *Start-up Test Circuit*

Figure 4-4 shows the input voltage (blue line) for the MCP6497 and the output voltage (black line). When power is first applied to the MCP6497, the output is turned off (Point A) and is driven by the load. After 2 µs (typical), the output is turned on (Point B) and V_{OUT} follows the input sine wave.

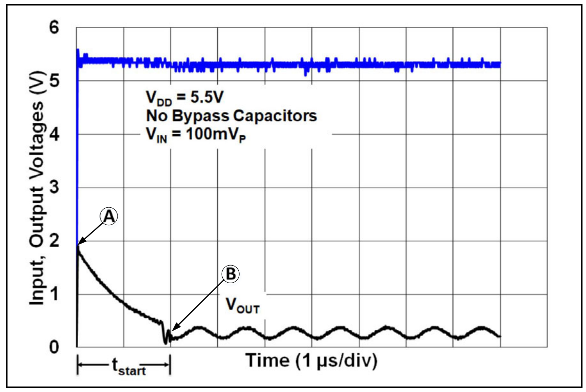


FIGURE 4-4: *Start-Up Test Waveforms.*

4.4 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1 V/V) is the most sensitive to the capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with the MCP6496/6R/6U/7/9 op amp, a small series resistor at the output (R_{ISO} in Figure 4-5) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

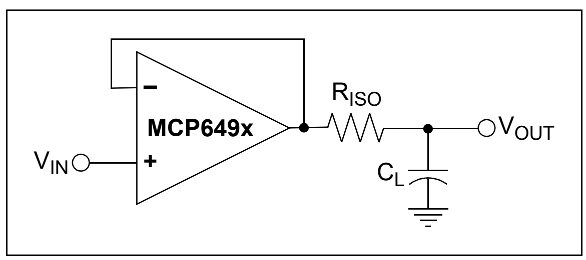


FIGURE 4-5: *Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.*

4.5 Supply Bypass

The MCP6496/6R/6U/7/9 op amp's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6496/6R/6U/7/9's bias current at +25°C (±1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-6.

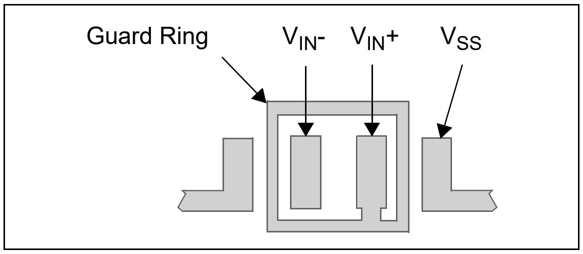


FIGURE 4-6: *Example Guard Ring Layout for Inverting Gain.*

1. Noninverting Gain and Unity-Gain Buffer:
   a) Connect the noninverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}-). This biases the guard ring to the Common mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the noninverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b) Connect the inverting pin (V_{IN}-) to the input with a wire that does not touch the PCB surface.

4.7 Unused Op Amps

An unused op amp in a dual (MCP6497) or quad (MCP6499) package should be configured as in shown in Figure 4-7. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components.

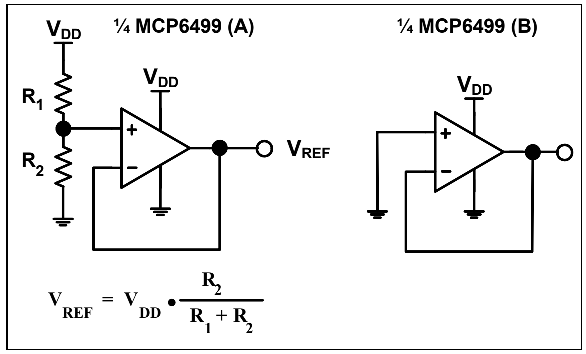


FIGURE 4-7: *Unused Op Amps.*

4.8 Electromagnetic Interference Rejection Ratio (EMIRR) Definitions

The electromagnetic interference (EMI) is the disturbance that affects an electrical circuit due to either electromagnetic induction or electromagnetic radiation emitted from an external source.

The parameter which describes the EMI robustness of an op amp is the Electromagnetic Interference Rejection Ratio (EMIRR). It quantitatively describes the effect that an RF interfering signal has on op amp performance. Internal passive filters make EMIRR better compared with older parts. This means that, with good PCB layout techniques, your EMC performance should be better.

EMIRR is defined in Equation 4-1.

EQUATION 4-1:

$$EMIRR(dB) = 20 \bullet \log\left(\frac{V_{RF}}{\Delta V_{OS}}\right)$$

Where:

V_{RF} = Peak Amplitude of RF Interfering Signal (V_{PK})

ΔV_{OS} = Input Offset Voltage Shift (V)

4.9 Application Circuits

4.9.1 MULTIPLE FEEDBACK LOW-PASS FILTER

The MCP6496/6R/6U/7/9 op amp can be used in active-filter applications. Figure 4-8 shows an inverting, third-order, multiple feedback low-pass filter that can be used as an anti-aliasing filter.

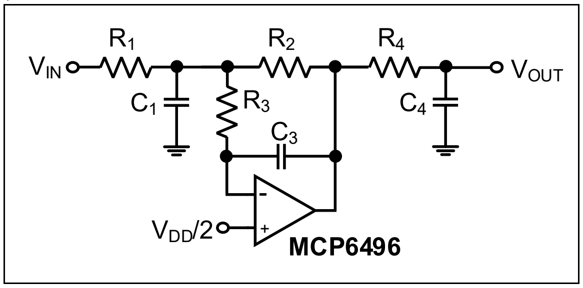


FIGURE 4-8: *Multiple Feedback Low-Pass Filter.*

4.9.2 PHOTODIODE AMPLIFIER

Figure 4-9 shows a photodiode biased in the photovoltaic mode for high precision. The resistor R converts the diode current to the voltage V_{OUT}. The capacitor is used to limit the bandwidth or to stabilize the circuit against the diode's capacitance.

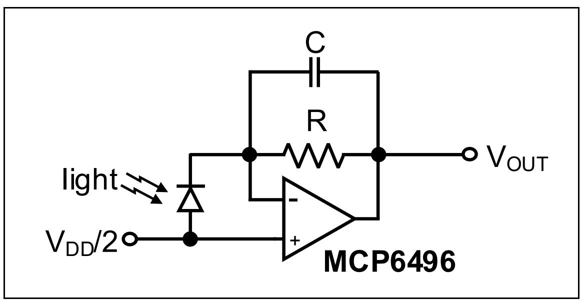


FIGURE 4-9: *Photodiode Amplifier.*

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6496/6R/6U/7/9 op amp.

5.1 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify the Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchase and sampling of Microchip parts.

5.2 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip website at www.microchipdirect.com.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 2 (P/N DS51668)
- MCP6XXX Amplifier Evaluation Board 3 (P/N DS51673)
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board (P/N SOIC8EV)
- 5/6-Pin SOT-23 Evaluation Board (P/N VSUEV2)
- 14-Pin SOIC/TSSOP/DIP Evaluation Board (P/N SOIC14EV)

5.3 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip website at www.microchip.com/appnotes, and are recommended as supplemental reference resources.

- **ADN003 –** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
- **AN722 –** *"Operational Amplifier Topologies and DC Specifications",* DS00722
- **AN723 –** *"Operational Amplifier AC Specifications and Applications",* DS00723
- **AN884 –** *"Driving Capacitive Loads With Op Amps",* DS00884
- **AN990 –** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990
- **AN1177 –** *"Op Amp Precision Design: DC Errors",* DS01177
- **AN1228 –** *"Op Amp Precision Design: Random Noise",* DS01228
- **AN1258 –** *"Op Amp Precision Design: PCB Layout Techniques",* DS01258

These application notes and others are listed in the design guide:

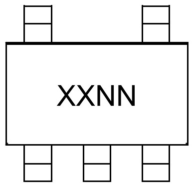
- *"Signal Chain Design Guide",* DS21825

NOTES:

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

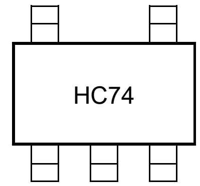
5-Lead SC-70 (**MCP6496/6U**)



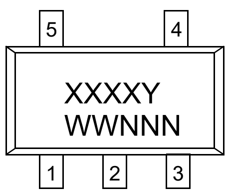
Device	Marking
MCP6496	HCNN
MCP6496U	HDNN

Note: Applies to 5-Lead SC-70.

Example:



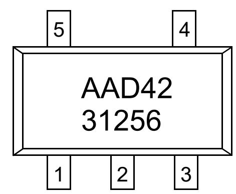
5-Lead SOT-23 (**MCP6496/6R/6U**)



Device	Marking
MCP6496	AAD4Y
MCP6496R	AAD6Y
MCP6496U	AAD5Y

Note: Applies to 5-Lead SOT-23.

Example:

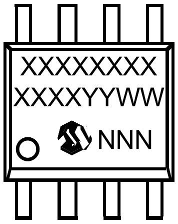


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

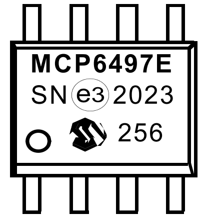
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

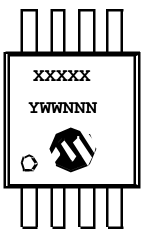
8-Lead SOIC (150 mil) **(MCP6497)**



Example:

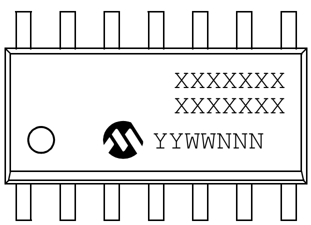


8-Lead MSOP

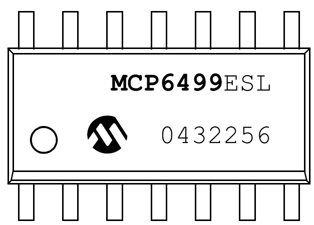


Example:

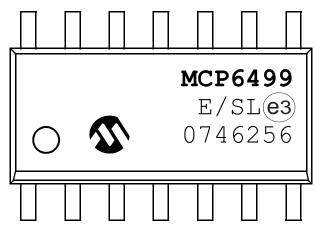
14-Lead SOIC (150 mil) (**MCP6499**)



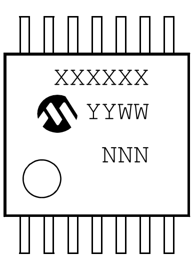
Example:



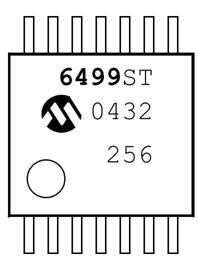
OR



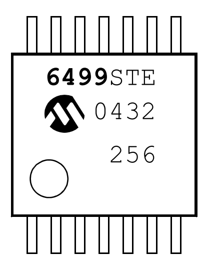
14-Lead TSSOP (**MCP6499**)



Example:

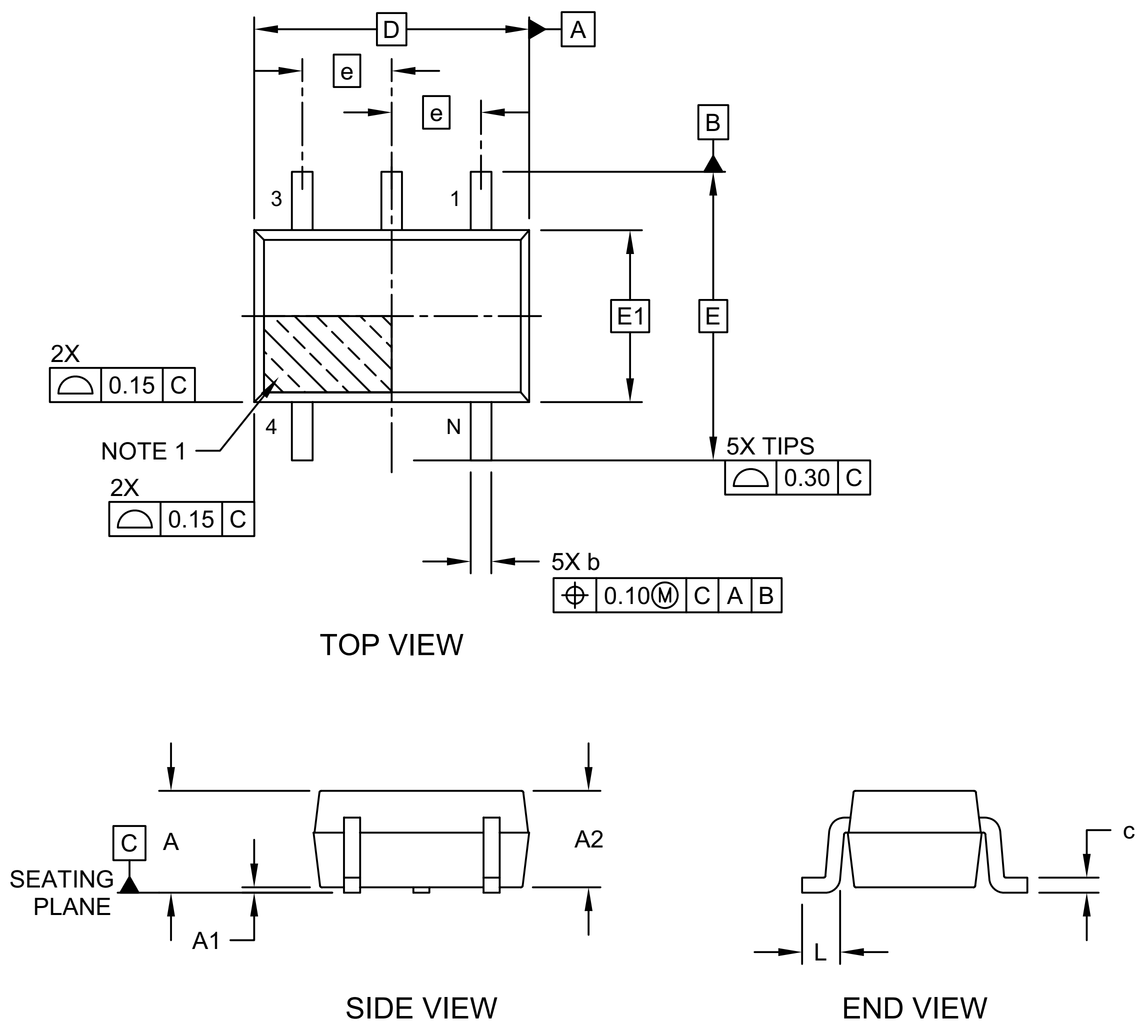


OR



5-Lead Plastic Small Outline Transistor (LT) [SC70]

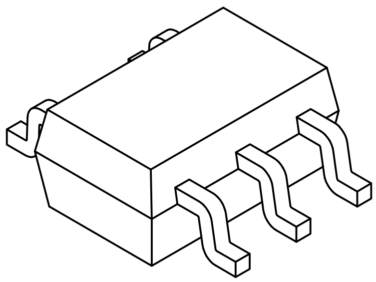
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-061-LT Rev E Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D		2.00 BSC	
Overall Width	E		2.10 BSC	
Molded Package Width	E1		1.25 BSC	
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.26

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

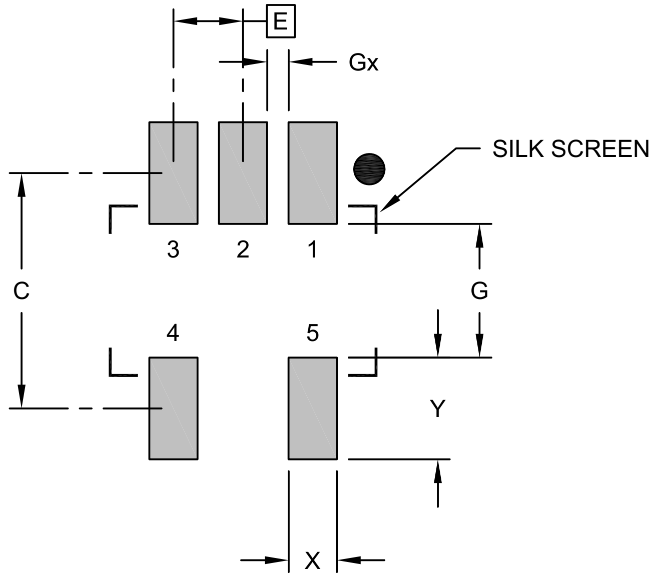
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-061-LT Rev E Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

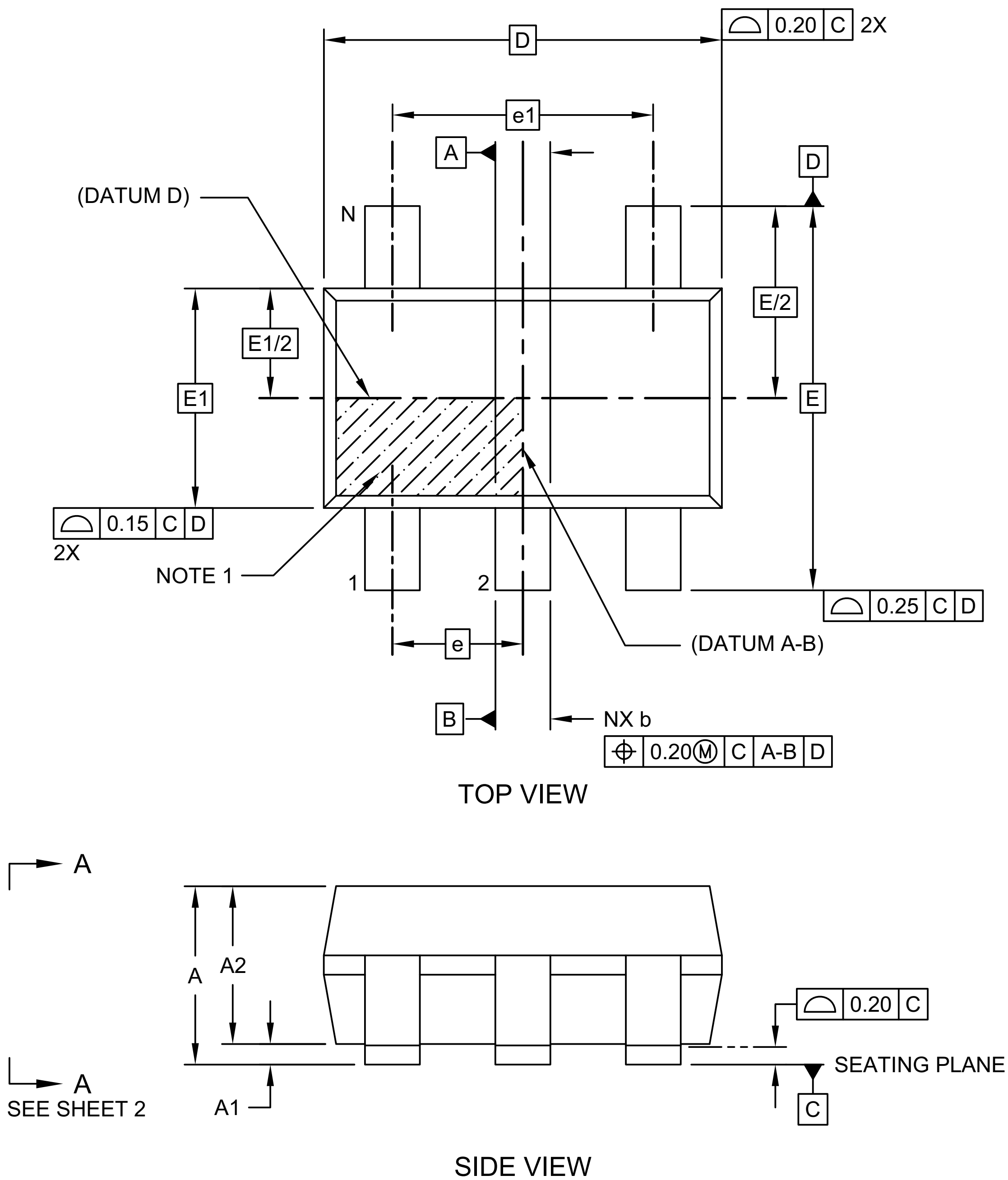
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061-LT Rev E

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

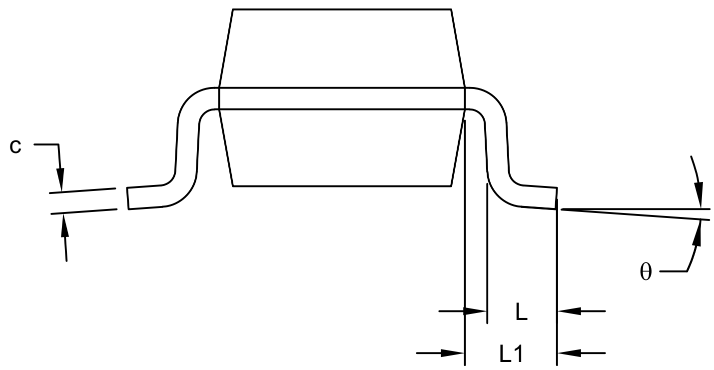
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



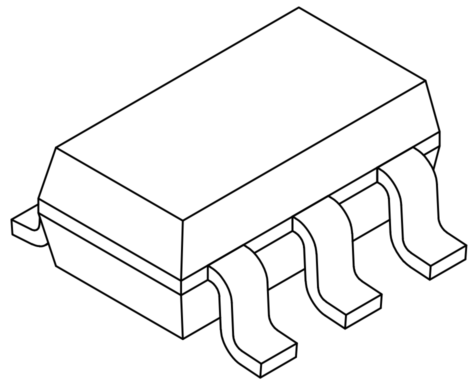
Microchip Technology Drawing C04-091-OT Rev H Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	-	0.60
Footprint	L1	0.60 REF		
Foot Angle	θ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

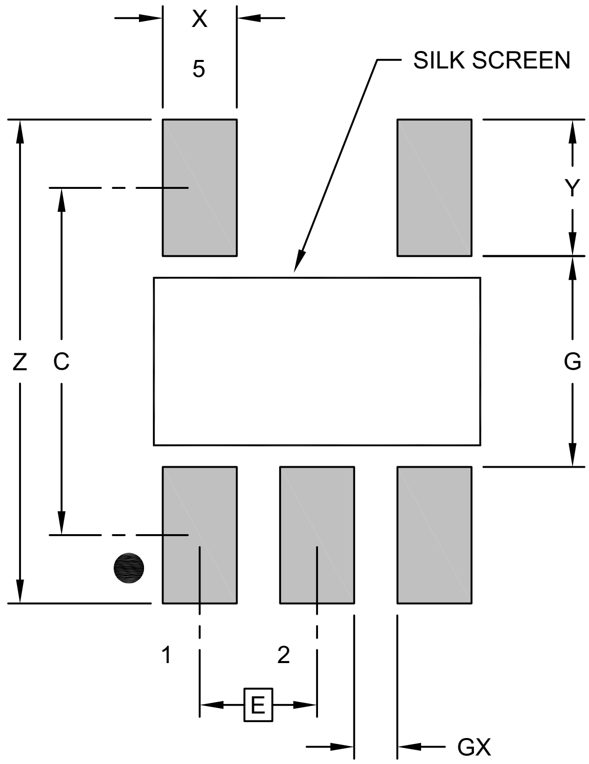
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev H Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (CT) [SOT-23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

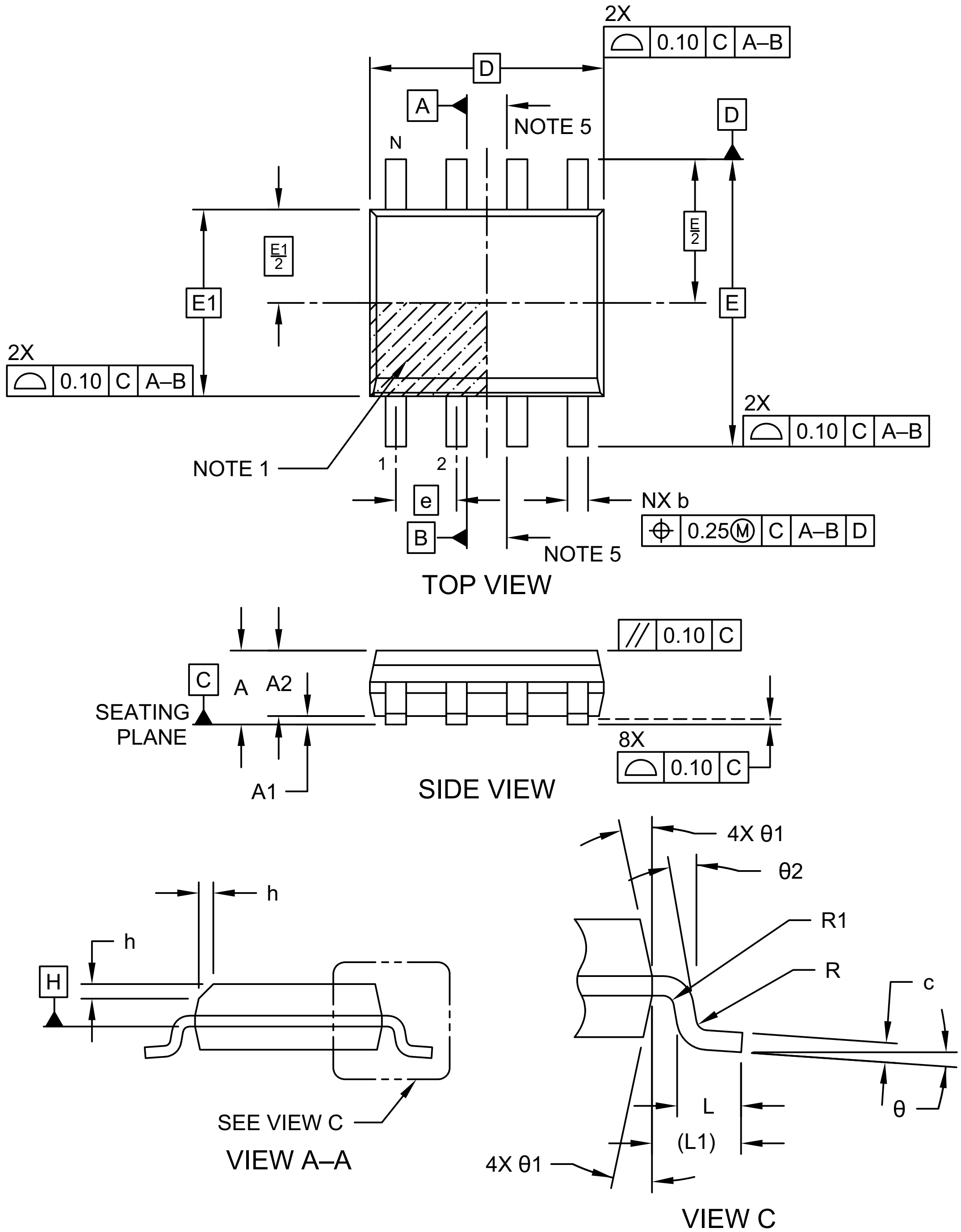
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-CT Rev H

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

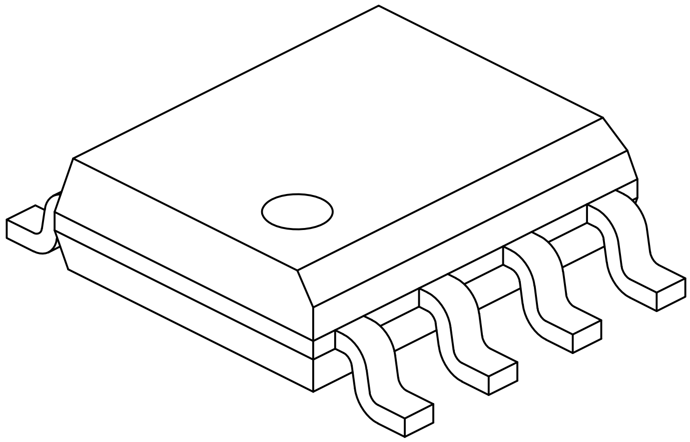
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

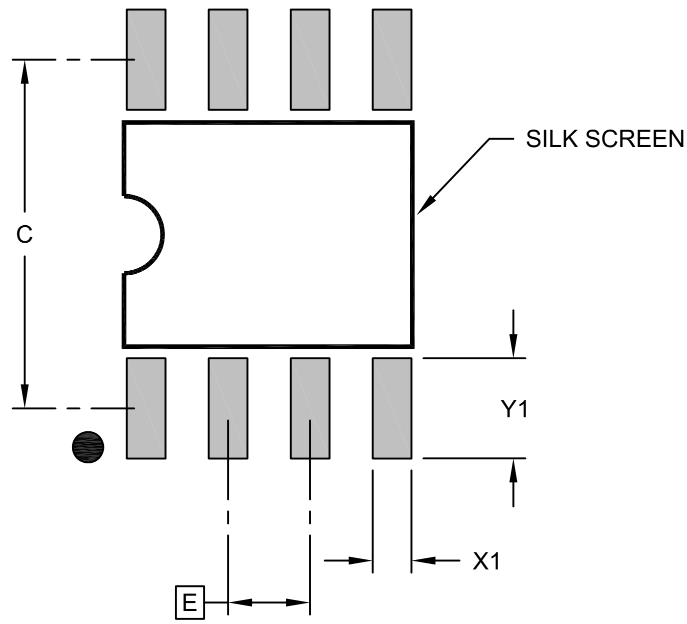
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

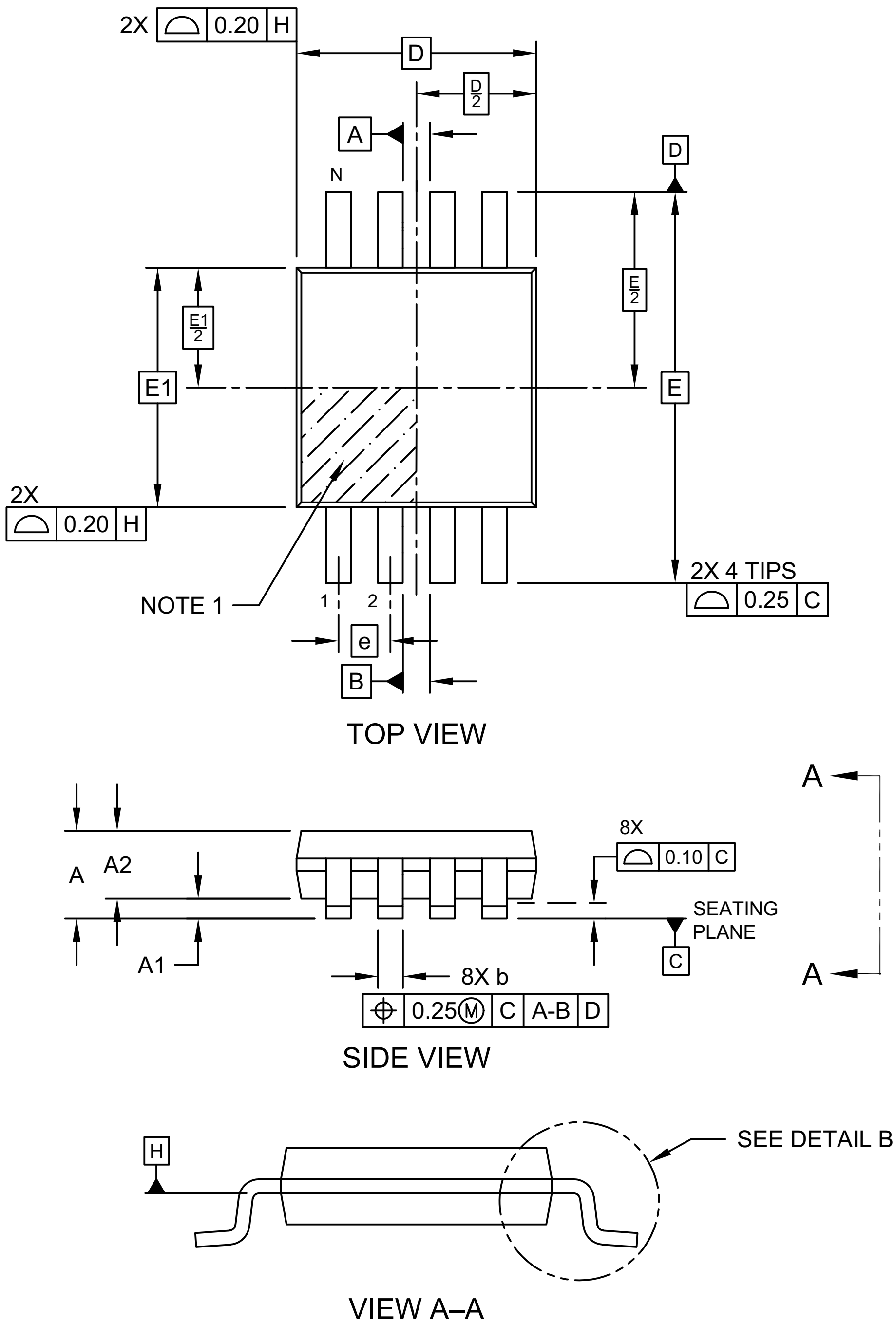
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev K

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

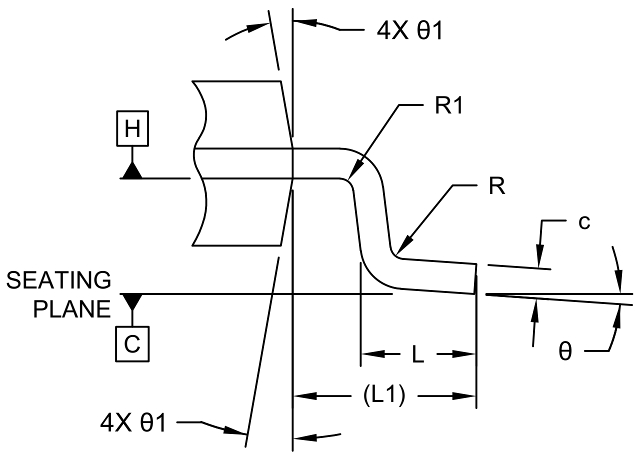
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



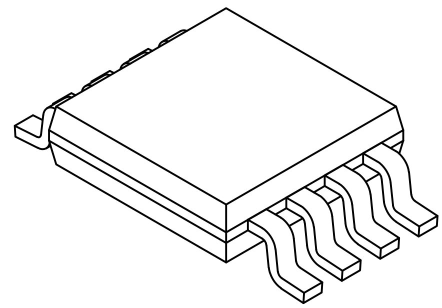
Microchip Technology Drawing C04-111-MS Rev F Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D	3.00 BSC		
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

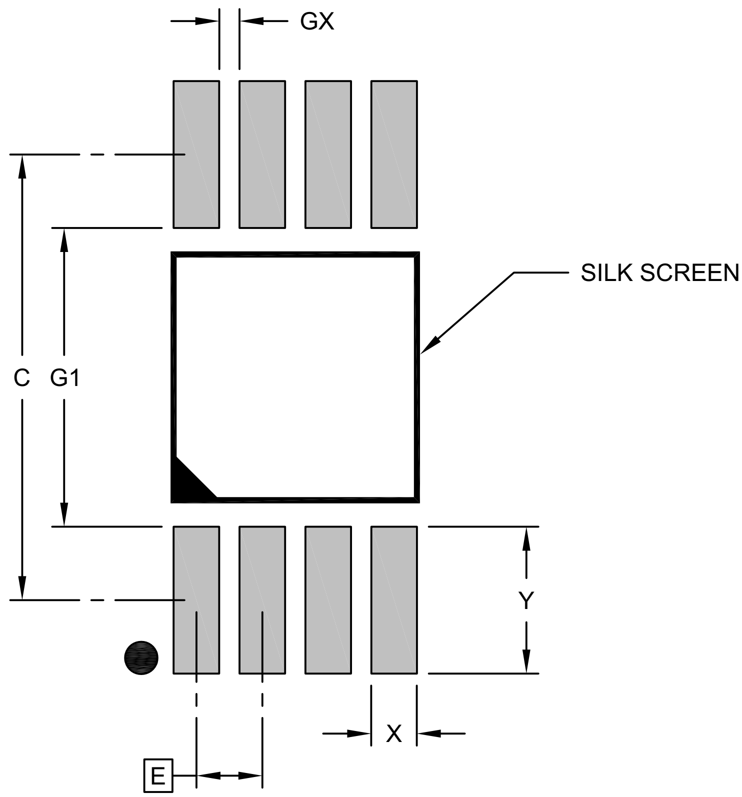
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev F Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

Notes:

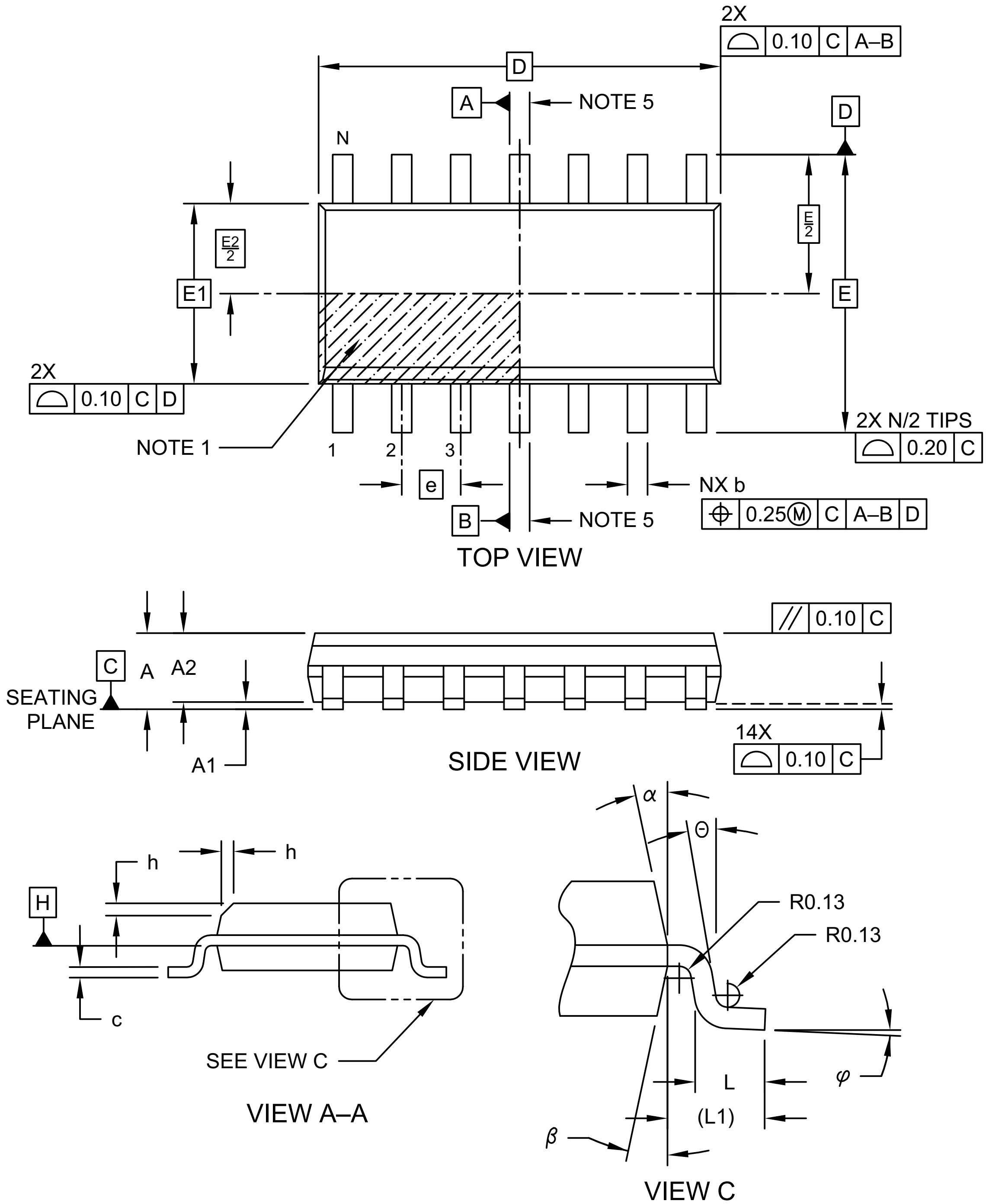
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-MS Rev F

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

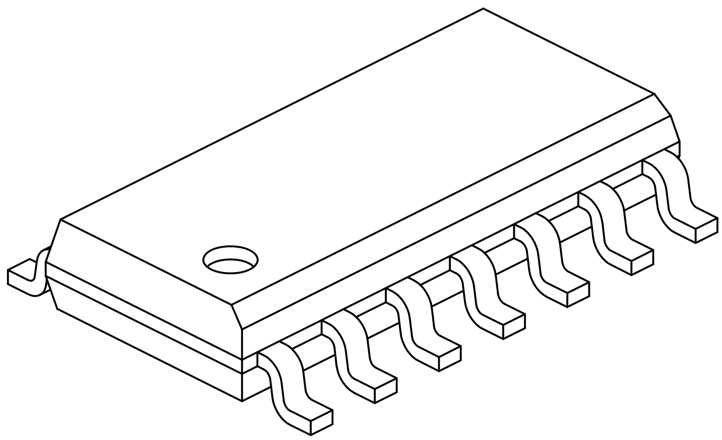
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

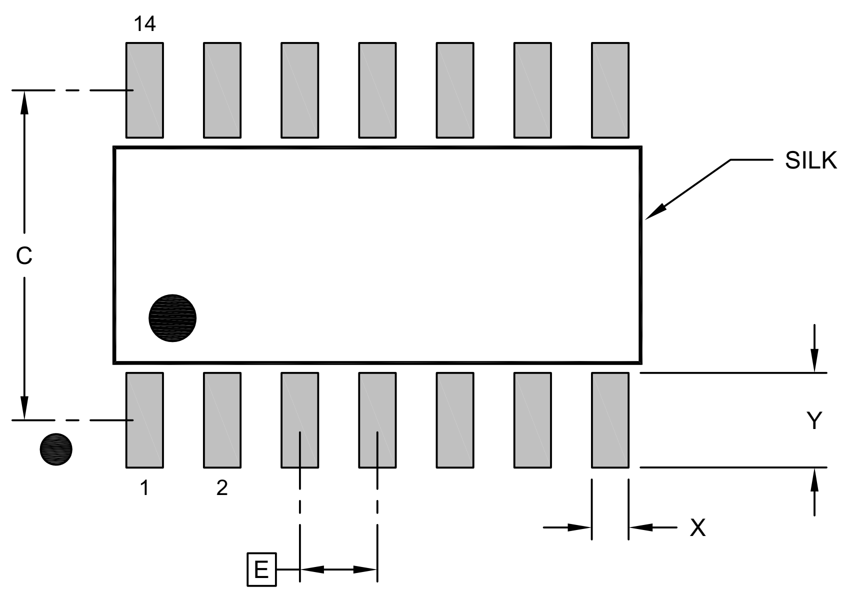
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Contact Pitch	E			1.27 BSC	
Contact Pad Spacing	C			5.40	
Contact Pad Width (X14)	X				0.60
Contact Pad Length (X14)	Y				1.55

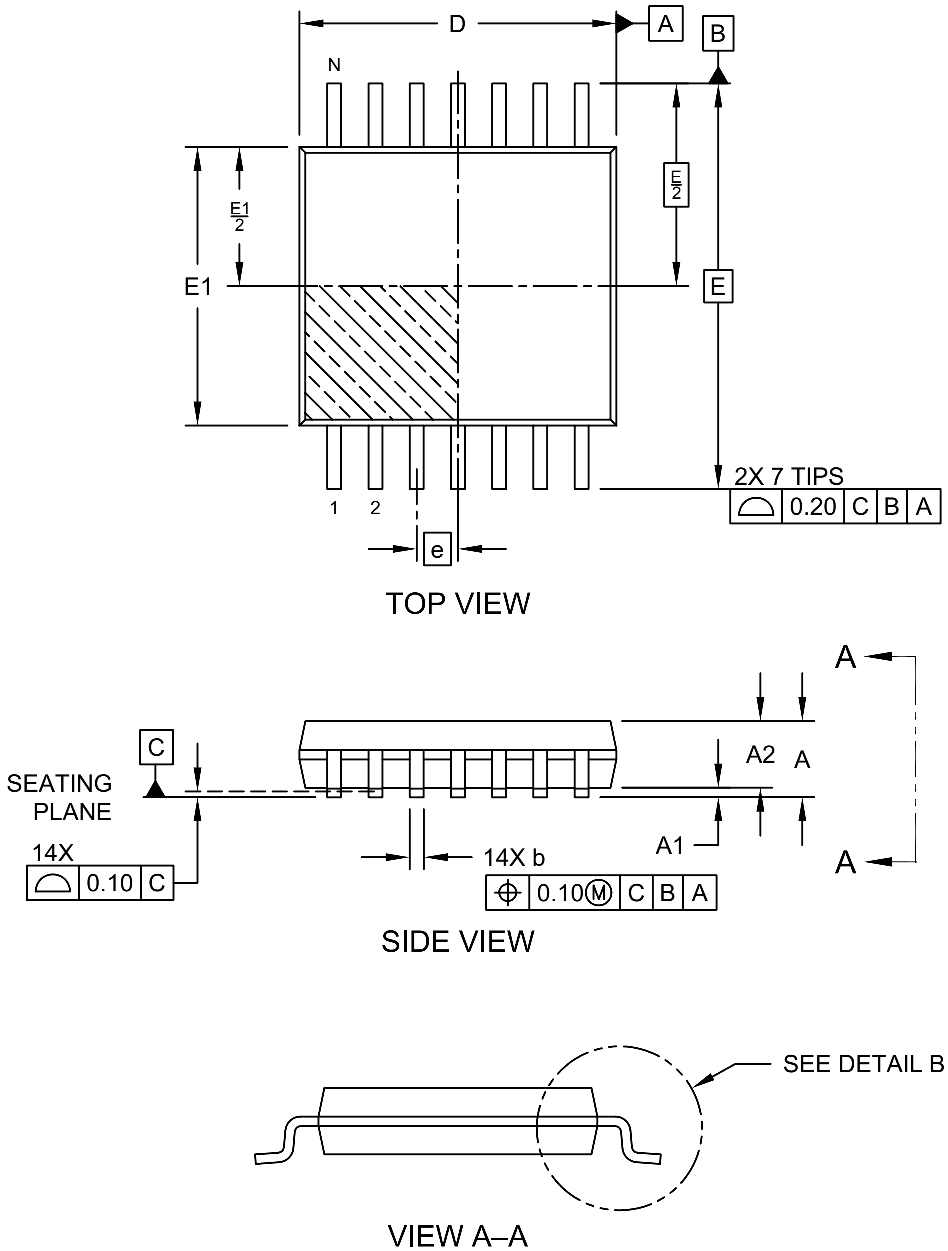
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

14-Lead Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

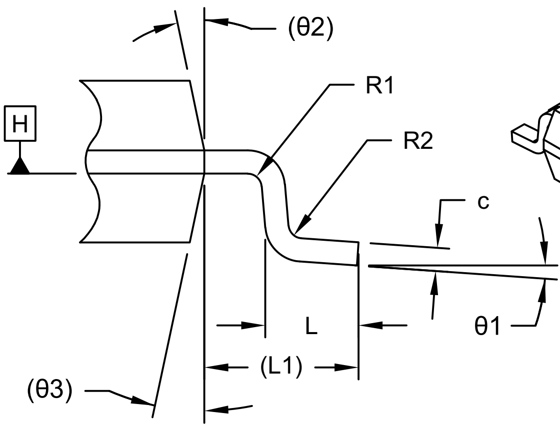
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



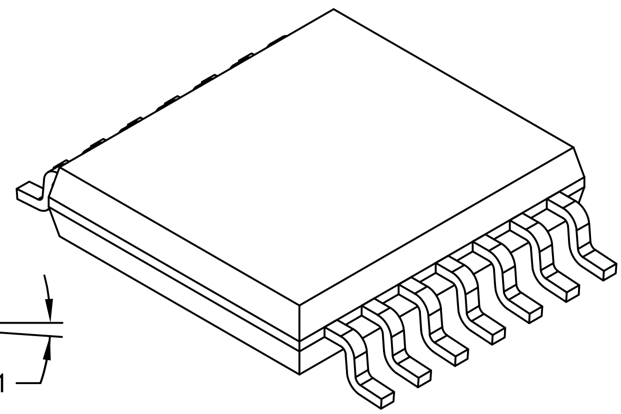
Microchip Technology Drawing C04-087 Rev E Sheet 1 of 2

14-Lead Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	14		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Standoff	A1	0.05	–	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	–	0.30
Terminal Thickness	c	0.09	–	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Lead Bend Radius	R1	0.09	–	–
Lead Bend Radius	R2	0.09	–	–
Foot Angle	θ1	0°	–	8°
Mold Draft Angle	θ2	–	12° REF	–
Mold Draft Angle	θ3	–	12° REF	–

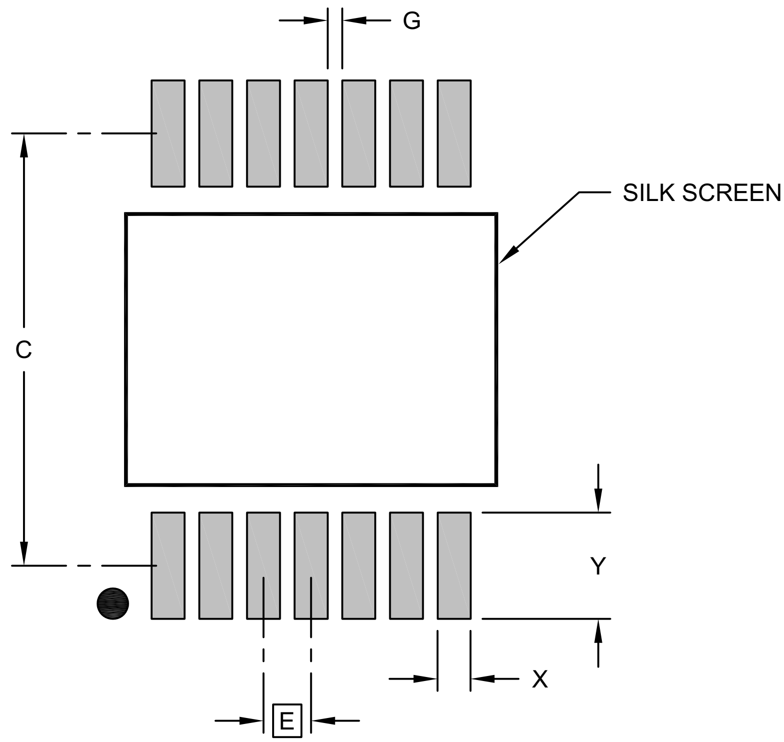
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087 Rev E Sheet 2 of 2

14-Lead Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS		
		Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.65 BSC		
Contact Pad Spacing	C			5.90	
Contact Pad Width (Xnn)	X				0.45
Contact Pad Length (Xnn)	Y				1.45
Contact Pad to Contact Pad (Xnn)	G		0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2087 Rev E

APPENDIX A: REVISION HISTORY

Revision A (December 2022)

- Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X(1)	-X	/XX	XXX(2)
Device	Tape and Reel Option	Temperature Range	Package	CLASS

Device:	MCP6496	Single Op Amp
	MCP6496T	Single Op Amp (Tape and Reel) (SC-70, SOT-23)
	MCP6496RT	Single Op Amp (Tape and Reel) (SOT-23)
	MCP6496UT	Single Op Amp (Tape and Reel) (SC-70, SOT-23)
	MCP6497	Dual Op Amp
	MCP6497T	Dual Op Amp (Tape and Reel for SOIC, MSOP)
	MCP6499	Quad Op Amp
	MCP6499T	Quad Op Amp (Tape and Reel for TSSOP and SOIC)

Temperature Range: E = -40°C to +125°C

Package:	LT	=	Plastic Package (SC-70), 5-lead (MCP6496 only)
	OT	=	Plastic Small Outline transistor (SOT-23), 5-lead (MCP6496 only)
	SN	=	Plastic Small Outline, (3.90 mm), 8-lead (MCP6497 only)
	MS	=	Plastic MSOP, 8-lead (MCP6497 only)
	ST	=	Plastic Thin Shrink Small Outline (4.4 mm), 14-lead (MCP6499 only)
	SL	=	Plastic Small Outline, (3.90 mm), 14-lead (MCP6499 only)
Class:	(Blank)	=	Non-Automotive
	VAO	=	Automotive

Note 1: The Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Automotive parts are AEC-Q100 qualified. Grade 1.

Examples:

a) MCP6496T-E/LT:	Tape and Reel, Extended temperature, 5LD SC-70 package
b) MCP6496T-E/OT:	Tape and Reel, Extended temperature, 5LD SOT-23 package
c) MCP6496RT-E/OT:	Tape and Reel, Extended temperature, 5LD SOT-23 package
d) MCP6496UT-E/LT:	Tape and Reel, Extended temperature, 5LD SC-70 package
e) MCP6496UT-E/OT:	Tape and Reel, Extended temperature, 5LD SOT-23 package
a) MCP6497-E/SN:	Extended temperature, 8LD SOIC package
b) MCP6497-E/MS:	Extended temperature, 8LD MSOP package
c) MCP6497T-E/SN:	Tape and Reel, Extended temperature, 8LD SOIC package
d) MCP6497T-E/MS:	Tape and Reel, Extended temperature, 8LD MSOP package
a) MCP6499-E/ST:	Extended temperature, 14LD TSSOP package
b) MCP6499-E/SL:	Extended temperature, 14LD SOIC package
c) MCP6499T-E/SL:	Tape and Reel, Extended temperature, 14LD SOIC package
d) MCP6499T-E/ST:	Tape and Reel, Extended temperature, 14LD TSSOP package

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office
.\

PART NO.	X(1)	-X	/XX	XXX(2)
Device	Tape and Reel Option	Temperature Range	Package	CLASS

Device:	MCP6496	Single Op Amp
	MCP6496T	Single Op Amp (Tape and Reel) (SC-70, SOT-23)
	MCP6496RT	Single Op Amp (Tape and Reel) (SOT-23)
	MCP6496UT	Single Op Amp (Tape and Reel) (SC-70, SOT-23)
	MCP6497	Dual Op Amp
	MCP6497T	Dual Op Amp (Tape and Reel for SOIC, MSOP)
	MCP6499	Quad Op Amp
	MCP6499T	Quad Op Amp (Tape and Reel for TSSOP and SOIC)

Temperature Range: E = -40°C to +125°C

Package:	LT	= Plastic Package (SC-70), 5-lead (MCP6496 only)
	OT	= Plastic Small Outline transistor (SOT-23), 5-lead (MCP6496 only)
	SN	= Plastic Small Outline, (3.90 mm), 8-lead (MCP6497 only)
	MS	= Plastic MSOP, 8-lead (MCP6497 only)
	ST	= Plastic Thin Shrink Small Outline (4.4 mm), 14-lead (MCP6499 only)
	SL	= Plastic Small Outline, (3.90 mm), 14-lead (MCP6499 only)
Class:	(Blank)	= Non-Automotive
	VAO	= Automotive

Note 1: The Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Automotive parts are AEC-Q100 qualified. Grade 1.

Examples:

a) MCP6496T-E/LTVAO: Tape and Reel, Automotive, Extended temperature, 5LD SC-70 package

b)MCP6496T-E/OTVAO: Tape and Reel, Automotive, Extended temperature, 5LD SOT-23 package

c)MCP6496RT-E/OTVAO: Tape and Reel, Automotive, Extended temperature, 5LD SOT-23 package

d)MCP6496UT-E/LTVAO: Tape and Reel, Automotive, Extended temperature, 5LD SC-70 package

e)MCP6496UT-E/OTVAO: Tape and Reel, Automotive, Extended temperature, 5LD SOT-23 package

a)MCP6497T-E/SNVAO: Tape and Reel, Extended temperature, Automotive, 8LD SOIC package

b)MCP6497T-E/MSVAO: Tape and Reel, Extended temperature, Automotive, 8LD MSOP package

a)MCP6499T-E/STVAO: Tape and Reel, Extended temperature, Automotive, 14LD TSSOP package

b)MCP6499T-E/SLVAO: Tape and Reel, Extended temperature, Automotive, 14LD SOIC package

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- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

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