MCP87018

High-Speed N-Channel Power MOSFET

Features:

- Low Drain-to-Source On Resistance ($R_{DS(ON)}$)
- Low Total Gate Charge (Q_G) and Gate-to-Drain Charge (Q_{GD})
- Low Series Gate Resistance (R_G)
- Fast Switching
- Capable of Short Dead-Time Operation
- RoHS Compliant

Applications:

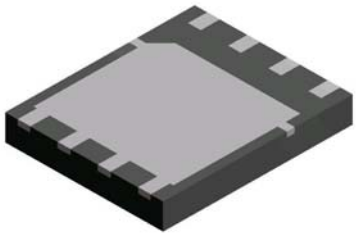
- Point-of-Load DC-DC Converters
- High-Efficiency Power Management in Servers, Networking and Automotive Applications

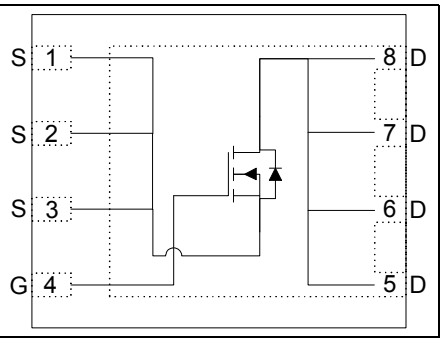
Description:

The MCP87018 is an N-Channel power MOSFET in a popular PDFN 5 mm x 6 mm package. Advanced packaging and silicon processing technologies allow the MCP87018 to achieve a low Q_G for a given $R_{DS(on)}$ value, resulting in a low Figure of Merit (FOM). Combined with low R_G, the low FOM of the MCP87018 allows high-efficiency power conversion with reduced switching and conduction losses.

Package Type

PDFN 5 x 6





Product Summary Table: Unless otherwise indicated, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Operating Characteristics						
Drain-to-Source Breakdown Voltage	BV_{DSS}	25	—	—	V	V_{GS} = 0V, I_D = 250 µA
Gate-to-Source Threshold Voltage	$V_{GS(TH)}$	1	1.3	1.6	V	V_{DS} = V_{GS}, I_D = 250 µA
Drain-to-Source On Resistance	$R_{DS(ON)}$	—	1.8	2.2	mΩ	V_{GS} = 4.5V, I_D = 25A
		—	1.5	1.9	mΩ	V_{GS} = 10V, I_D = 25A
Total Gate Charge	Q_G	—	32.5	37	nC	V_{DS} = 12.5V, I_D = 25A, V_{GS} = 4.5V
Gate-to-Drain Charge	Q_{GD}	—	13	—	nC	V_{DS} = 12.5V, I_D = 25A
Series Gate Resistance	R_G	—	1.5	—	Ω	—
Thermal Characteristics						
Thermal Resistance Junction-to-X	$R_{\theta JX}$	—	—	55	°C/W	**Note 1**
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	—	—	1.0	°C/W	**Note 2**

Note 1: $R_{\theta JX}$ is determined with the device surface mounted on a 4-Layer FR4 PCB, with a 1" x 1" mounting pad of 2 oz. copper. This characteristic is dependent on user's board design.

2: $R_{\theta JC}$ is determined using JEDEC 51-14 Method. This characteristic is determined by design.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DS} .....+25V

V_{GS} ..... +10.0V / -8V

$I_{D,}$ Continuous ..... 100A, T_C = +25°C

P_D .....2.2W, T_A = +25°C

T_J, T_{STG}.....-55°C to +150°C

E_{AS} Avalanche Energy ..... 612.5 mJ

I_D = 35A, L = 1 mH, R_G = 25Ω

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Static Characteristics						
Drain-to-Source Breakdown Voltage	BV_{DSS}	25	—	—	V	V_{GS} = 0V, I_D = 250 µA
Drain-to-Source Leakage Current	I_{DSS}	—	—	1	µA	V_{GS} = 0V, V_{DS} = 20V
Gate-to-Source Leakage Current	I_{GSS}	—	—	100	nA	V_{DS} = 0V, V_{GS} = 10V/-8V
Gate-to-Source Threshold Voltage	$V_{GS(TH)}$	1	1.3	1.6	V	V_{DS} = V_{GS}, I_D = 250 µA
Drain-to-Source On Resistance	$R_{DS(ON)}$	—	2.2	—		V_{GS} = 3.3V, I_D = 25A
		—	1.8	2.2	mΩ	V_{GS} = 4.5V, I_D = 25A
		—	1.5	1.9	mΩ	V_{GS} = 10V, I_D = 25A
Transconductance	g_{fs}	—	162	—	S	V_{DS} = 12.5V, I_D = 25A
Dynamic Characteristics						
Input Capacitance	C_{ISS}	—	2925	—	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1 MHz
Output Capacitance	C_{OSS}	—	1305	—	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1 MHz
Reverse Transfer Capacitance	C_{RSS}	—	330	—	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1 MHz
Total Gate Charge	Q_G	—	32.5	37	nC	V_{DS} = 12.5V, I_D = 25A, V_{GS} = 4.5V
Gate-to-Drain Charge	Q_{GD}	—	13	—	nC	V_{DS} = 12.5V, I_D = 25A
Gate-to-Source Charge	Q_{GS}	—	5.3	—	nC	V_{DS} = 12.5V, I_D = 25A
Gate Charge at $V_{GS(TH)}$	$Q_{G(TH)}$	—	3.8	—	nC	V_{DS} = 12.5V, I_D = 25A
Output Charge	Q_{OSS}	—	26	—	nC	V_{DS} = 12.5V, V_{GS} = 0
Turn-On Delay Time	$t_{d(on)}$	—	6.53	—	ns	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 25A, R_G = 2Ω
Rise Time	t_r	—	28.3	—	ns	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 25A, R_G = 2Ω
Turn-Off Delay Time	$t_{d(off)}$	—	26.35	—	ns	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 25A, R_G = 2Ω
Fall Time	t_f	—	28.05	—	ns	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 25A, R_G = 2Ω
Series Gate Resistance	R_G	—	1.5	—	Ω	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Diode Characteristics						
Diode Forward Voltage	V_{FD}	—	0.8	1	V	I_S = 25A, V_{GS} = 0V
Reverse Recovery Charge	Q_{RR}	—	47	—	nC	I_S = 25A, di/dt = 300 A/µs
Reverse Recovery Time	t_{rr}	—	28	—	ns	I_S = 25A, di/dt = 300 A/µs
Avalanche Characteristics						
Avalanche Energy	E_{AS}	200	—	—	mJ	I_D = 20A, L = 1 mH, R_G = 25Ω

TEMPERATURE CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Junction Temperature Range	T_J	-55	—	150	°C	
Storage Temperature Range	T_A	-55	—	150	°C	
Package Thermal Resistances						
Thermal Resistance Junction-to-X, 8L 5x6-PDFN	$R_{\theta JX}$	—	—	55	°C/W	**Note 1**
Thermal Resistance Junction-to-Case, 8L 5x6-PDFN	$R_{\theta JC}$	—	—	1.0	°C/W	**Note 2**

Note 1: $R_{\theta JX}$ is determined with the device surface mounted on a 4-Layer FR4 PCB, with a 1" x 1" mounting pad of 2 oz. copper. This characteristic is dependent on user's board design.

2: $R_{\theta JC}$ is determined using JEDEC 51-14 Method. This characteristic is determined by design.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C.

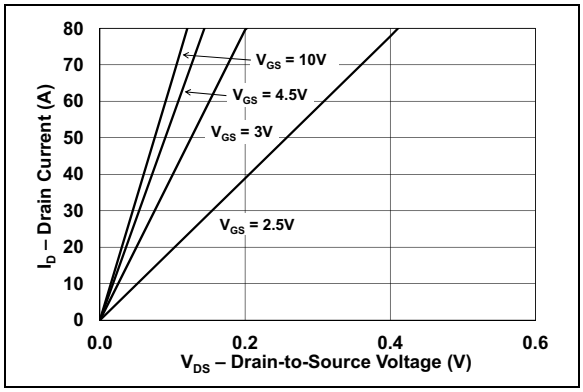


FIGURE 2-1: *Typical Output Characteristics.*

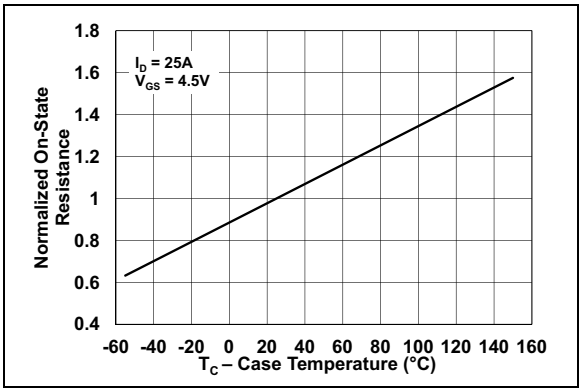


FIGURE 2-4: *Normalized On-State Resistance vs. Temperature.*

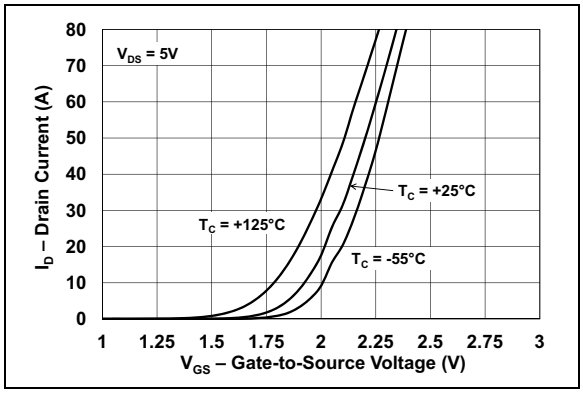


FIGURE 2-2: *Typical Transfer Characteristics.*

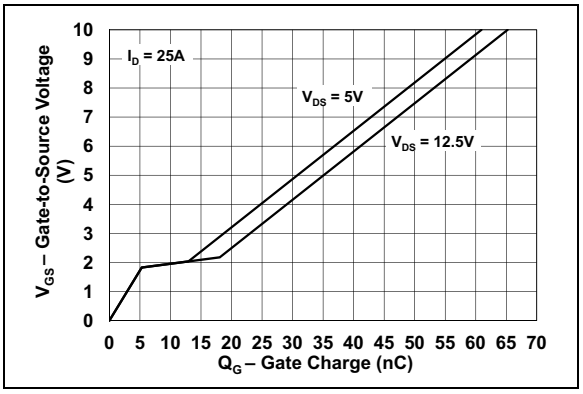


FIGURE 2-5: *Gate-to-Source Voltage vs. Gate Charge.*

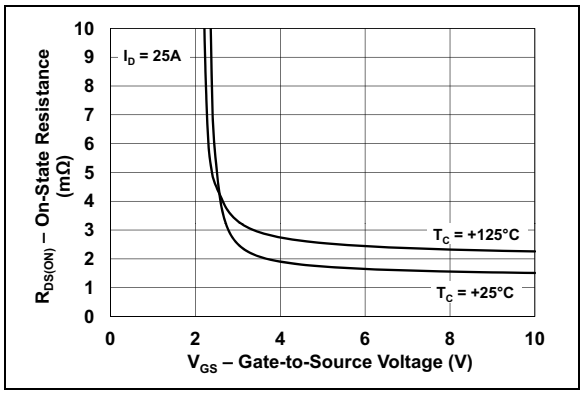


FIGURE 2-3: *On-State Resistance vs. Gate-to-Source Voltage.*

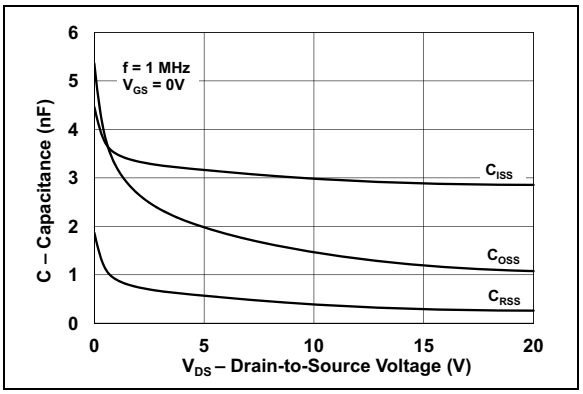


FIGURE 2-6: *Capacitance vs. Drain-to-Source Voltage.*

Note: Unless otherwise indicated, T_A = +25°C.

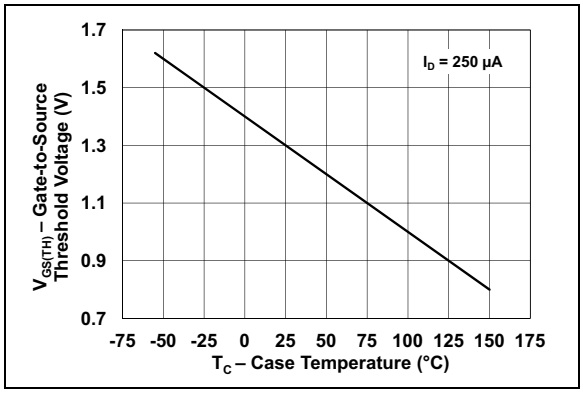


FIGURE 2-7: *Gate-to-Source Threshold Voltage vs. Temperature.*

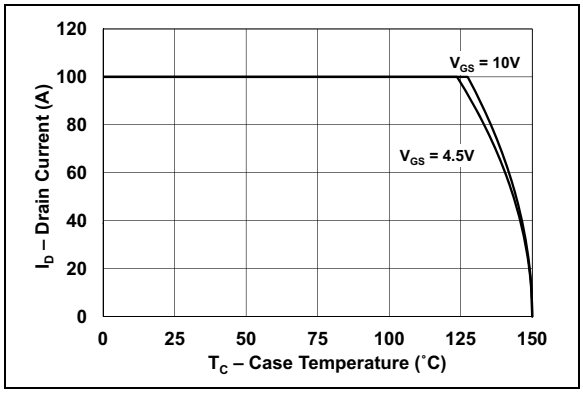


FIGURE 2-10: *Maximum Drain Current vs. Temperature.*

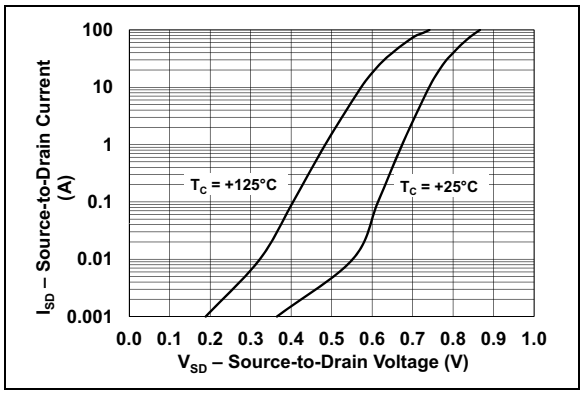


FIGURE 2-8: *Source-to-Drain Current vs. Source-to-Drain Voltage.*

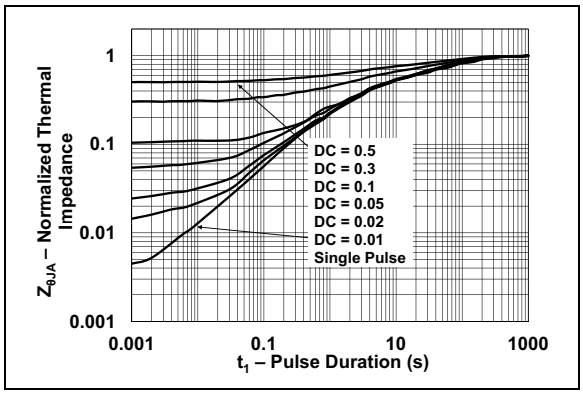


FIGURE 2-11: *Transient Thermal Impedance.*

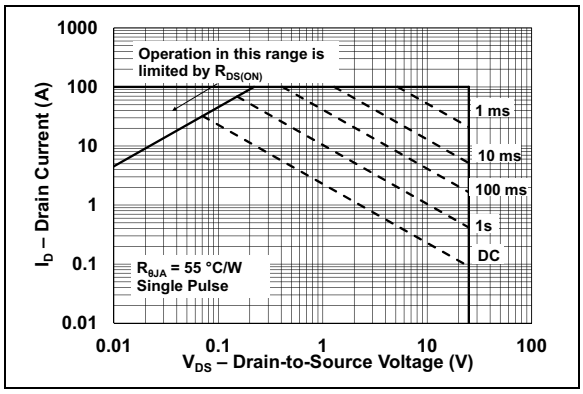


FIGURE 2-9: *Maximum Safe Operating Area.*

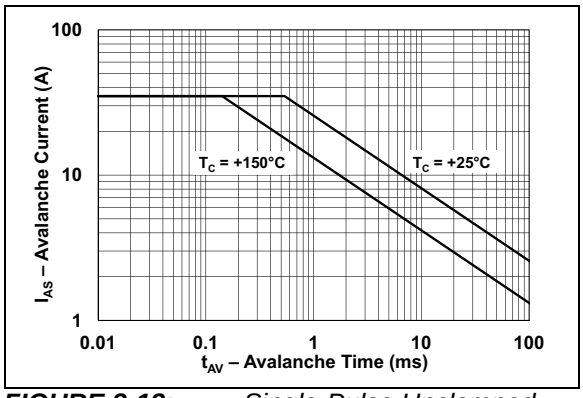


FIGURE 2-12: *Single-Pulse Unclamped Inductive Switching.*

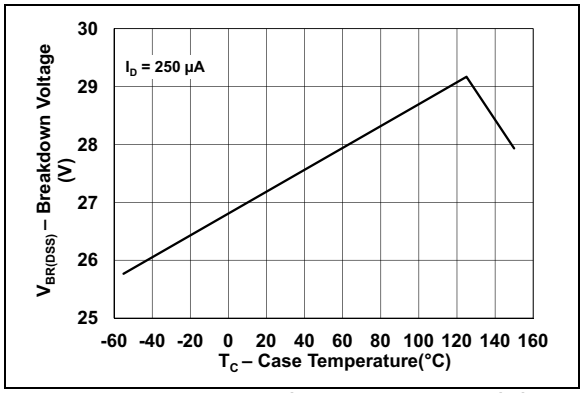


FIGURE 2-13: *Drain-to-Source Breakdown Voltage vs. Temperature.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

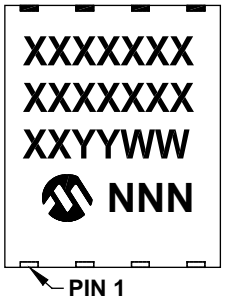
TABLE 3-1: PIN FUNCTION TABLE

MCP87018 5x6 PDFN	**Symbol**	**Description**
1, 2, 3	S	Source pin
4	G	Gate pin
5, 6, 7, 8	D	Drain pin, including exposed thermal pad

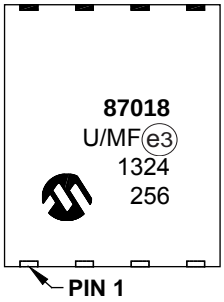
4.0 PACKAGING INFORMATION

4.1 Package Marking Information*

8-Lead PDFN (5x6x1.0 mm)



Example



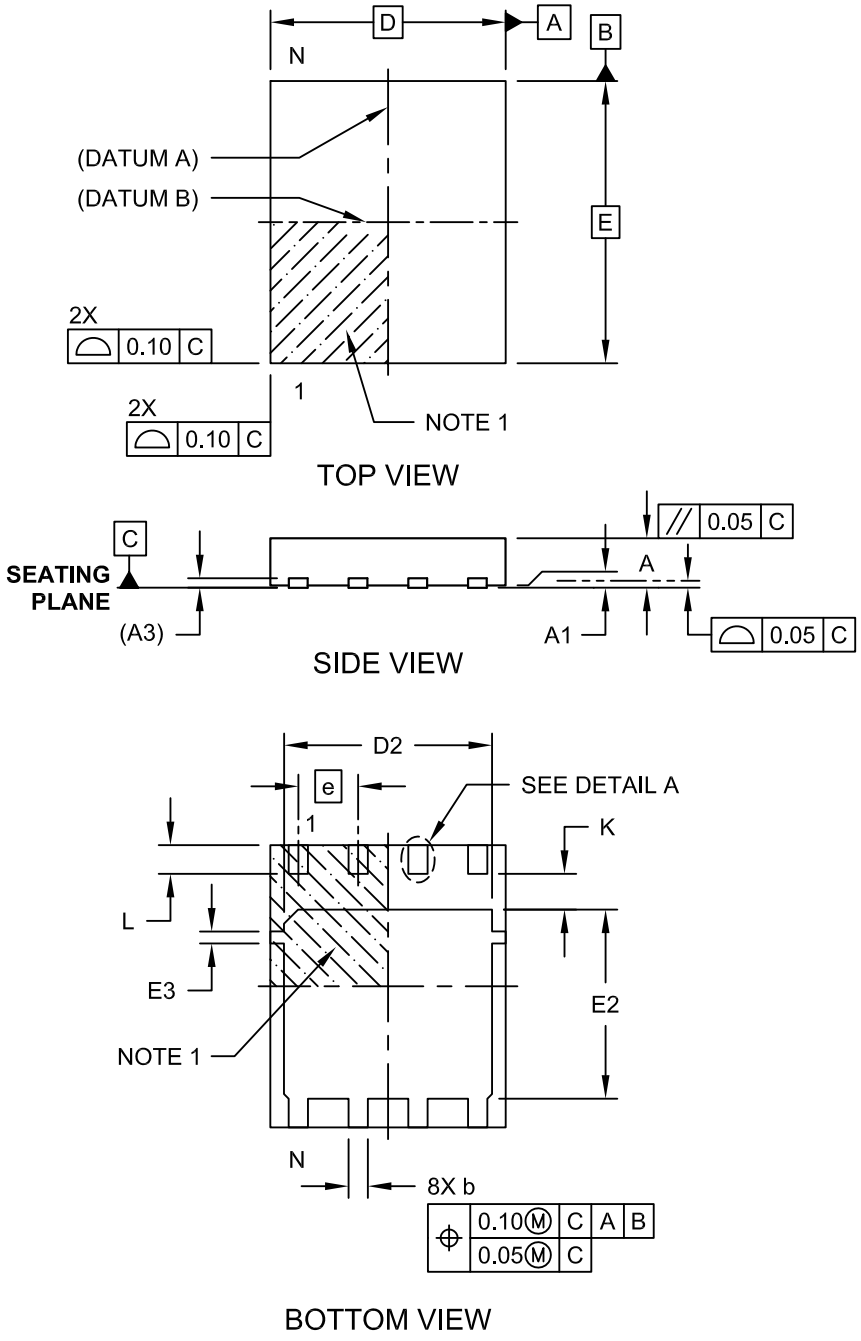
*RoHS compliant using EU-RoHS exemption: 7(a) – Lead in high-melting-temperature-type solders (i.e., lead-based alloys containing 85% by weight or more lead) can be found on the outer packaging for this package.

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Power Dual Flatpack No Lead Package (MF) – 5x6x1.0 mm Body [PDFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-188B Sheet 1 of 2

8-Lead Power Dual Flatpack No Lead Package (MF) – 5x6x1.0 mm Body [PDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

DETAIL A
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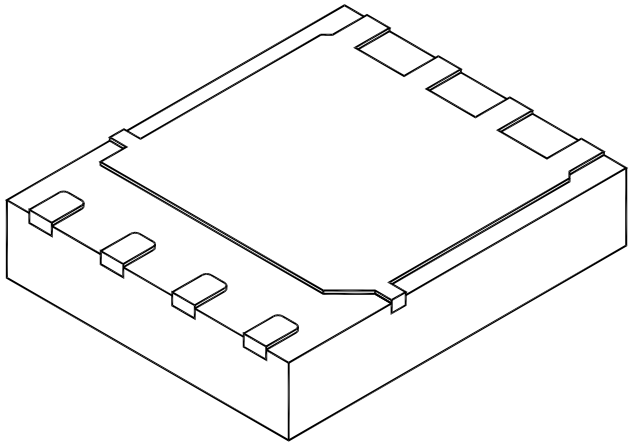


	Units	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.80	1.00	1.03
Standoff	A1	0.00	-	0.05
Terminal Thickness	(A3)		0.20 REF	
Overall Length	D		5.00 BSC	
Overall Width	E		6.00 BSC	
Exposed Pad length	D2	4.27	4.42	4.52
Exposed Pad Width	E2	3.87	4.02	4.12
Tab Width	E3	0.20	0.25	0.30
Terminal Width	b	0.36	0.41	0.46
Terminal Length	L	0.51	0.61	0.71
Terminal to Exposed Pad	K	0.71	0.76	0.81

Notes:

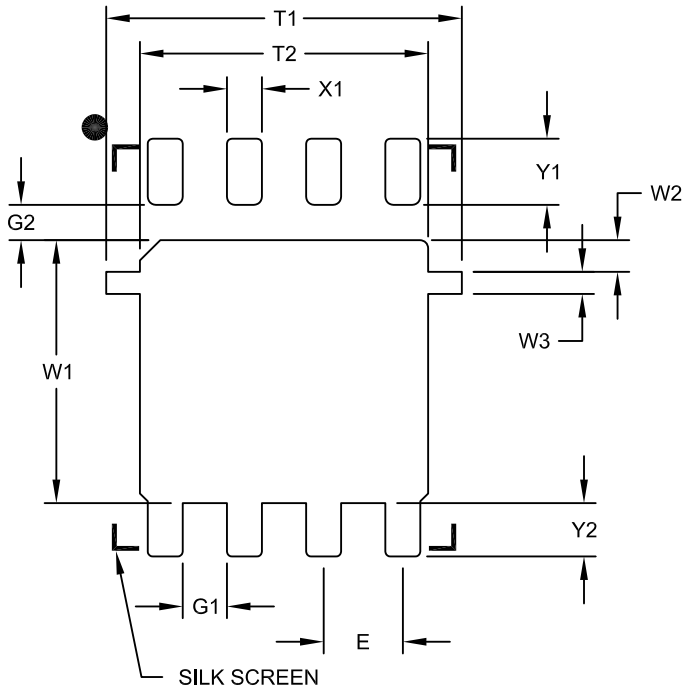
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Package dimension does not include mold flash, protrusions, burrs or metal smearing.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-188B Sheet 2 of 2

8-Lead Power Dual Flatpack No Lead Package (MF) – 5x6x1.0 mm Body [PDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Center Pad Width	W1			4.22
Pad Edge to Tab	W2		0.51	
Tab Width	W3		0.35	
Center Pad Length With Tabs	T1			5.70
Center Pad Length	T2			4.62
Distance Between Terminals	G1	0.71		
Terminal To Center Pad (X4)	G2	0.57		
Terminal Pad Width (X8)	X1			0.56
Terminal Pad Length (X4)	Y1			1.06
Terminal Pad Length (X8)	Y2			0.86

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2188A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (July 2013)

The following is the list of modifications:

1. Updated the thermal resistance junction-to-X and junction-to-case values in Product Summary Table and Temperature Characteristics.
2. Added Figures 2-9 and 2-11 in Section 2.0, Typical Performance Curves.
3. Updated Figure 2-10 in Section 2.0, Typical Performance Curves.

Revision A (January 2013)

- Original Release of this Document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP87018T:	N-Channel Power MOSFET (Tape and Reel)
Temperature Range:	U =	-55°C to +150°C (Ultra High)
Package:	MF =	8-Lead High Power Dual Flatpack, No Lead Package (5x6x1.0 mm Body) (PDFN), 8-lead

Examples:

a) MCP87018T-U/MF: Tape and Reel, Ultra High Temperature, 8LD PDFN package

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ISBN: 978-1-62077-338-3

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