

High-Speed Integrated Ultrasound Driver IC

Features

- Drives Two Ultrasound Transducer Channels
- Generates a Five-Level Waveform
- Drives 12 High-Voltage MOSFETs
- $\pm 2A$ Source-and-Sink Peak Currents
- Up to 20 MHz Output Frequency
- 12 V/ns Slew Rate
- ± 3 ns Matched Delay Times
- Less than -40 dB Second Harmonic
- Two Separate Gate Drive Voltages
- 1.8V to 3.3V CMOS Logic Interface

Applications

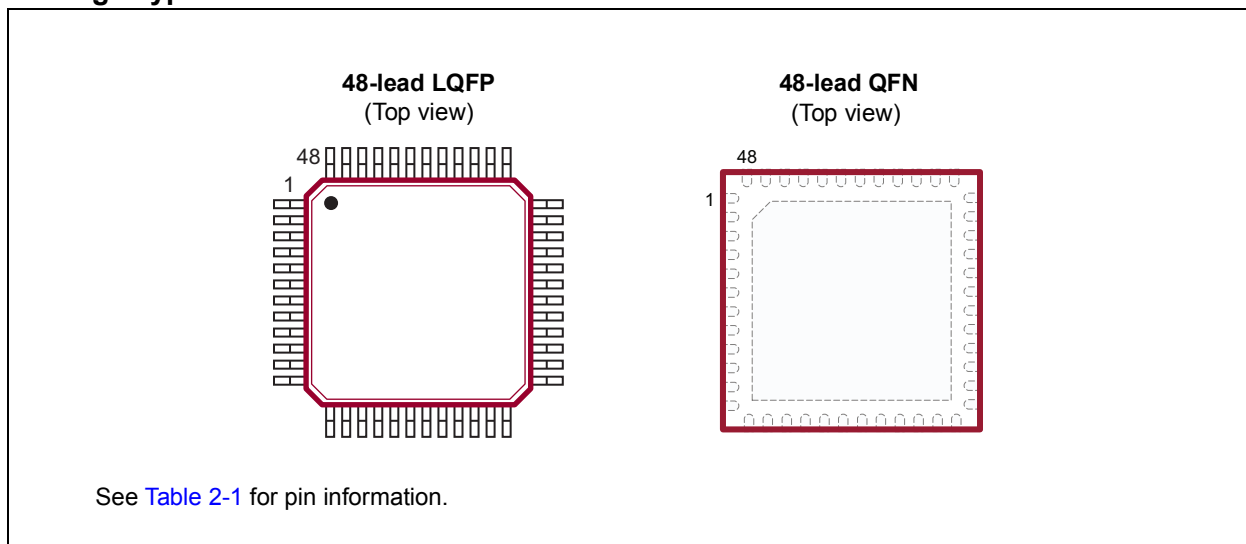
- Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Non-Destructive Testing (NDT)
- Metal Flaw Detection
- Sonar Transmitter

General Description

The MD1711 is a two-channel logic controller circuit with low-impedance MOSFET gate drivers. It is intended to be used with external FETs as a five-level high-voltage and high-speed transmitter. The MD1711 is designed for medical ultrasound imaging applications but can also be used for metal flaw detection, NDT and for driving piezoelectric transducers.

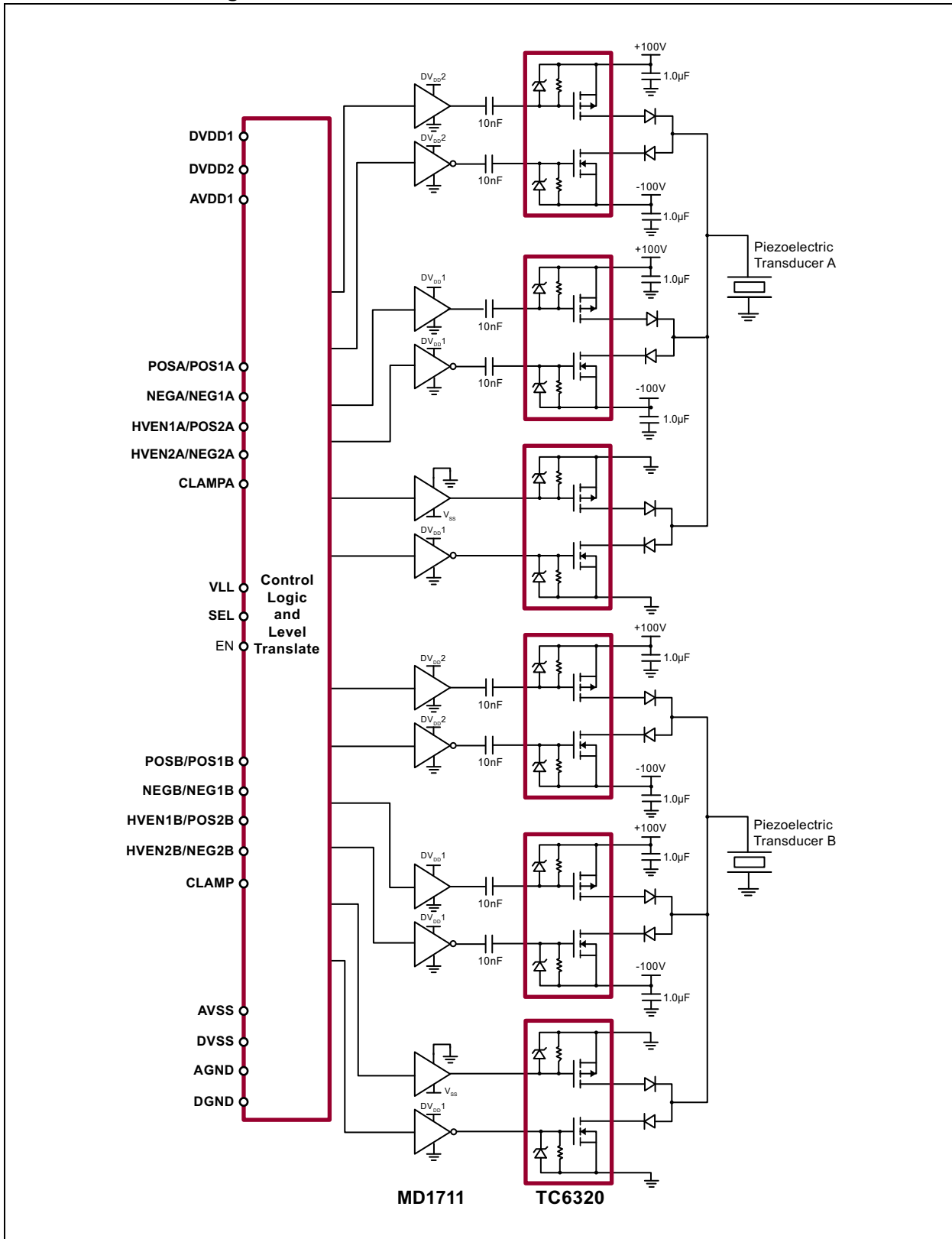
The MD1711 has two sets of control logic inputs, one for Channel A and one for Channel B. Each channel consists of three pairs of MOSFET gate drivers. These drivers are designed to match the drive requirements of the TC6320. One MD1711 drives six TC6320s. Each driver consists of an N-channel and a P-channel MOSFET. They are designed to have the same impedance and can provide peak currents of 2 amps.

Package Types

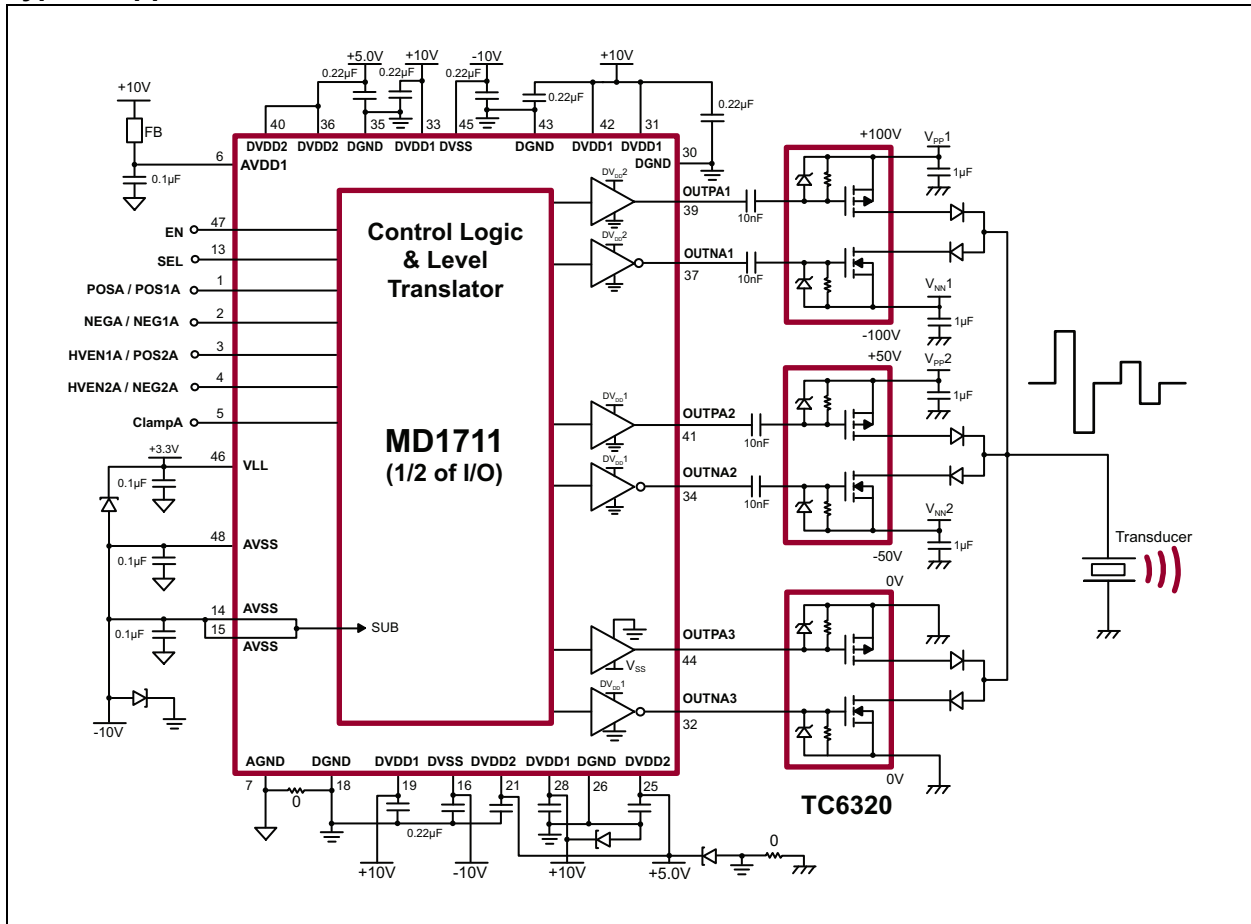


MD1711

Functional Block Diagram



Typical Application Circuit



MD1711

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

| | |
|------------------------------------------------------------------------|-----------------|
| Logic Supply Voltage, V_{LL} | -0.5V to +5.5V |
| Positive Gate Drive Supply, AV_{DD1} , DV_{DD1} , DV_{DD2} | -0.5V to +15V |
| Negative Gate Drive Supply, AV_{SS} , DV_{SS} | -15V to +0.5V |
| Operating Junction Temperature, T_J | 0°C to +125°C |
| Storage Temperature, T_S | -65°C to +150°C |
| Power Dissipation (48-lead LQFP) | 1.92W |
| Power Dissipation (48-lead QFN) | 5.55W |

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

OPERATING SUPPLY VOLTAGES AND CURRENTS

Electrical Specifications: Over operating conditions unless otherwise specified, $AV_{DD1} = DV_{DD1} = DV_{DD2} = 10V$, $AV_{SS} = DV_{SS} = -10V$, $V_{LL} = 3.3V$, $T_A = 25^\circ C$.

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|-----------------------------------------|-------------------------|------|------|------|---------|-----------------------------------------------------|
| Logic Supply | V_{LL} | 1.8 | 3.3 | 5 | V | |
| Positive Drive Bias Supply | AV_{DD1} | 8 | 10 | 12.6 | V | |
| Positive Gate Drive Supply | DV_{DD1} | 4.75 | — | 12.6 | V | |
| Positive Gate Drive Supply | DV_{DD2} | 4.75 | — | 12.6 | V | |
| Negative Gate Drive and Bias Supply | AV_{SS} , DV_{SS} | -12 | -10 | -8 | V | |
| Logic Supply Current | I_{VLL} | — | 2 | — | mA | All channels on at 5 MHz, no load |
| Positive Bias Current | I_{AVDD1} | — | 5 | — | mA | |
| Negative Drive and Bias Supply Currents | I_{AVSS} , I_{DVSS} | — | 20 | — | mA | |
| Positive Drive Current 1 | I_{DVDD1} | — | 55 | — | mA | |
| Positive Drive Current 2 | I_{DVDD2} | — | 13 | — | mA | All channels on at 5 MHz, $DV_{DD2} = 5V$, no load |
| V_{AVDD1} Quiescent Current | I_{AVDD1Q} | — | 2 | — | mA | EN = low, all inputs low or high |
| V_{AVSS} Quiescent Current | I_{AVSSQ} | — | 0.75 | — | mA | |
| V_{DVDD1} Quiescent Current | I_{DVDD1Q} | — | — | 10 | μA | |
| V_{DVDD2} Quiescent Current | I_{DVDD2Q} | — | — | 10 | μA | |
| Logic Supply Current | I_{VLLQ} | — | 1 | — | mA | |

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise specified, $AV_{DD1} = DV_{DD1} = DV_{DD2} = 10V$, $AV_{SS} = DV_{SS} = -10V$, $V_{LL} = 3.3V$, $T_A = 0^\circ C$ to $70^\circ C$.

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions | |
|----------------------------------------------------|-----------|--------------|------|--------------|---------|------------|------------------------------|
| P-CHANNEL AND N-CHANNEL GATE DRIVER OUTPUTS | | | | | | | |
| Output Sink Resistance | P-Channel | R_{SINK} | — | — | 6 | Ω | $I_{SINK} = 100\text{ mA}$ |
| | N-Channel | | — | — | 10 | Ω | $I_{SINK} = 100\text{ mA}$ |
| Output Source resistance | P-Channel | R_{SOURCE} | — | — | 6 | Ω | $I_{SOURCE} = 100\text{ mA}$ |
| | N-Channel | | — | — | 10 | Ω | $I_{SOURCE} = 100\text{ mA}$ |
| Peak Output Sink Current | P-Channel | I_{SINK} | — | 2 | — | A | |
| | N-Channel | | — | 1.5 | — | A | |
| Peak Output Source Current | P-Channel | I_{SOURCE} | — | 2 | — | A | |
| | N-Channel | | — | 1.5 | — | A | |
| LOGIC INPUTS | | | | | | | |
| Input Logic High Voltage | V_{IH} | $0.8 V_{LL}$ | — | V_{LL} | V | | |
| Input Logic Low Voltage | V_{IL} | 0 | — | $0.2 V_{LL}$ | V | | |
| Input Logic High Current | I_{IH} | — | — | 1 | μA | | |
| Input Logic Low Current | I_{IL} | -1 | — | — | μA | | |

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise specified, $AV_{DD1} = DV_{DD1} = DV_{DD2} = 10V$, $AV_{SS} = DV_{SS} = -10V$, $V_{LL} = 3.3V$, $T_A = 0^\circ C$ to $70^\circ C$.

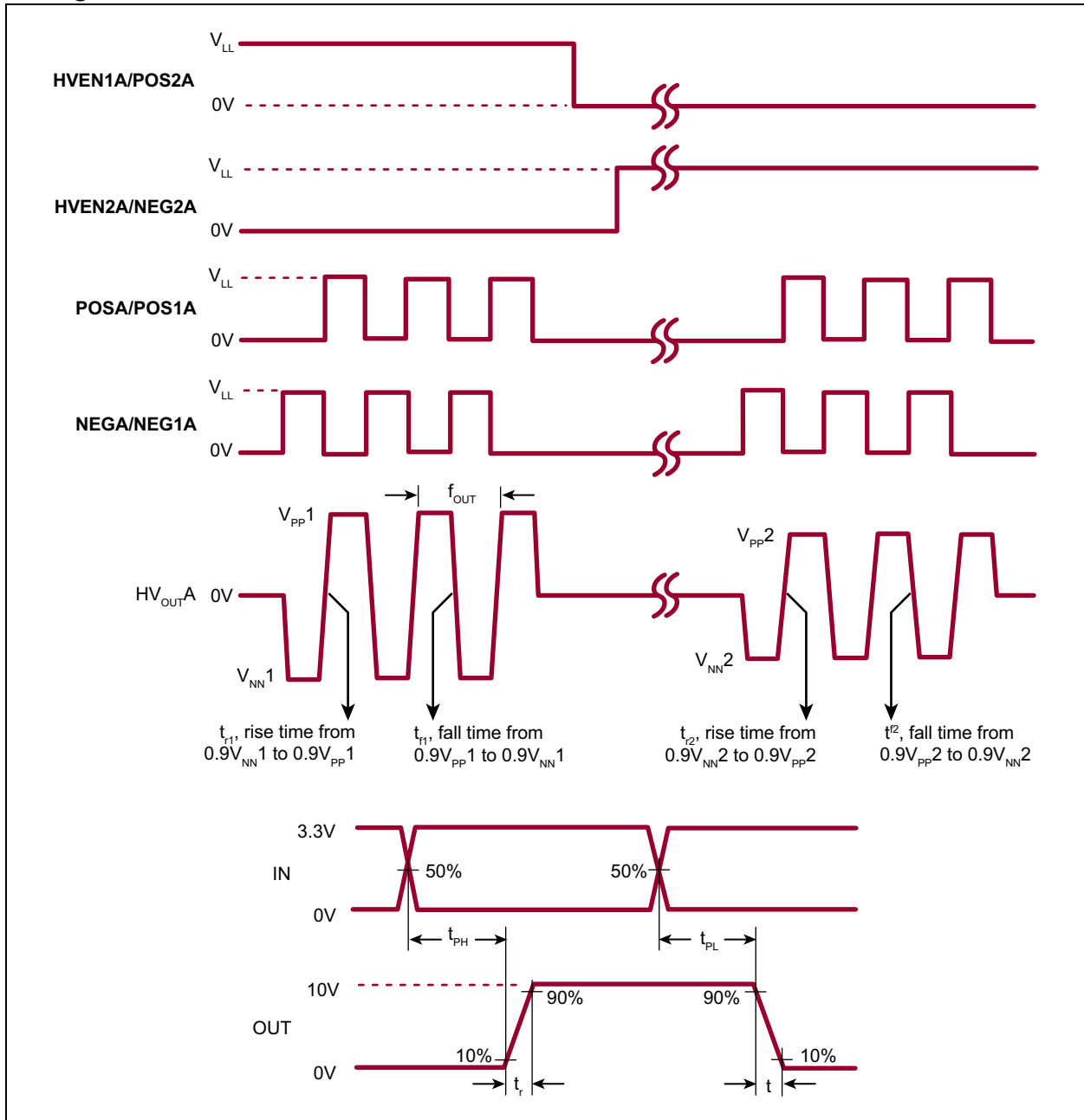
| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---------------------------------------------------|-------------------|------|------|---------|------|----------------------------------------------------------|
| Output Frequency Range | f_{OUT} | — | — | 20 | MHz | |
| Propagation Delay when Output is from Low to High | t_{PH} | — | 19 | — | ns | No load (See Timing Waveforms.) |
| Propagation Delay when Output is from High to Low | t_{PL} | — | 19 | — | ns | No load (See Timing Waveforms.) |
| Output Rise Time | t_r | — | 8 | — | ns | 1000 pF load (See Timing Waveforms.) |
| Output Fall Time | t_f | — | 8 | — | ns | 1000 pF load (See Timing Waveforms.) |
| Delay Time Matching | Δt_{DM} | — | — | ± 3 | ns | No load, from device to device |
| Output Jitter | Δt_{DLAY} | — | 30 | — | ps | Standard deviation of t_D samples (1 kHz) |
| Output Slew Rate | SR | — | 12 | — | V/ns | Measured at TC6320 output with 100 Ω load |
| Second Harmonic Distortion | HD2 | — | -40 | — | dB | |

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TEMPERATURE SPECIFICATIONS

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|-----------------------------------|---------------|------|------|------|------|------------|
| TEMPERATURE RANGE | | | | | | |
| Operating Junction Temperature | T_J | 0 | — | +125 | °C | |
| Storage Temperature | T_S | -65 | — | +150 | °C | |
| PACKAGE THERMAL RESISTANCE | | | | | | |
| 48-lead LQFP | θ_{JA} | — | 52 | — | °C/W | |
| 48-lead QFN | θ_{JA} | — | 18 | — | °C/W | |

Timing Waveforms



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2.0 PIN DESCRIPTION

Functional descriptions for the pins are listed in [Table 2-1](#). See [Package Types](#) for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

| Pin Number | Pin Name | Description |
|------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | POSA/POS1A | Logic input control for Channel A. When SEL = L, the pin is POSA. When SEL = H, the pin is POS1A. |
| 2 | NEGA/NEG1A | Logic input control for Channel A. When SEL = L, the pin is NEGA. When SEL = H, the pin is NEG1A. |
| 3 | HVEN1A/POS2A | Logic input control for Channel A. When SEL = L, the pin is HVEN1A. When SEL = H, the pin is POS2A. |
| 4 | HVEN2A/NEG2A | Logic input control for Channel A. When SEL = L, the pin is HVEN2A. When SEL = H, the pin is NEG2A. |
| 5 | CLAMPA | Used with SEL = H. Logic input control for OUT-PA3 and OUT-NA3. Connect to ground when SEL = L. |
| 6 | AVDD1 | Supplies analog circuitry portion of the gate driver. Should be at the same potential as DVDD1. |
| 7 | AGND | Analog Ground |
| 8 | CLAMPB | Used with SEL = H. Logic input control for OUT-PB3 and OUT-NB3. Connect to ground when SEL = L. |
| 9 | HVEN2B/NEG2B | Logic input control for Channel B. When SEL = L, the pin is HVEN2B. When SEL = H, the pin is NEG2B. |
| 10 | HVEN1B/POS2B | Logic input control for Channel B. When SEL = L, the pin is HVEN1B. When SEL = H, the pin is POS2B. |
| 11 | NEGB/NEG1B | Logic input control for Channel B. When SEL = L, the pin is NEGB. When SEL = H, the pin is NEG1B. |
| 12 | POSB/POS1B | Logic input control for Channel B. When SEL = L, the pin is POSB. When SEL = H, the pin is POS1B. |
| 13 | SEL | Logic input select. See Table 3-2 for SEL = L and Table 3-3 for SEL = H. |
| 14 | AVSS | Negative driver supply for OUT-PA3, OUT-PB3 and bias circuits. It is also connected to the IC substrate. It should be connected to the most negative potential. |
| 15 | | |
| 16 | DVSS | Gate drive supply voltage for OUT-PA3 and OUT-PB3. Supplies digital circuitry portion and the main output stage. Should be at the same potential as AVSS. |
| 17 | OUT-PB3 | Output P-channel gate driver for Channel B |
| 18 | DGND | Digital Ground |
| 19 | DVDD1 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA2, OUT-NA2, OUT-NA3, OUT-PB2, OUT-NB2 and OUT-NB3. Should be at the same potential as AVDD1. |
| 20 | Out-PB2 | Output P-channel gate driver for Channel B |
| 21 | DVDD2 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA1, OUT-NA1, OUT-PB1 and OUT-NB1. Can be at a different potential compared to DVDD1. |
| 22 | Out-PB1 | Output P-channel gate driver for Channel B |
| 23 | N/C | No connect |
| 24 | Out-NB1 | Output N-channel gate driver for Channel B |

TABLE 2-1: PIN FUNCTION TABLE

| Pin Number | Pin Name | Description |
|------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25 | DVDD2 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA1, OUT-NA1, OUT-PB1 and OUT-NB1. Can be at a different potential compared to DVDD1. |
| 26 | DGND | Digital Ground |
| 27 | Out-NB2 | Output N-channel gate driver for Channel B |
| 28 | DVDD1 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA2, OUT-NA2, OUT-NA3, OUT-PB2, OUT-NB2 and OUT-NB3. Should be at the same potential as AVDD1. |
| 29 | Out-NB3 | Output N-channel gate driver for Channel B |
| 30 | DGND | Digital Ground |
| 31 | DVDD1 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA2, OUT-NA2, OUT-NA3, OUT-PB2, OUT-NB2 and OUT-NB3. Should be at the same potential as AVDD1. |
| 32 | OUT-NA3 | Output N-channel gate drivers for Channel A |
| 33 | DVDD1 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA2, OUT-NA2, OUT-NA3, OUT-PB2, OUT-NB2 and OUT-NB3. Should be at the same potential as AVDD1. |
| 34 | Out-NA2 | Output N-Channel gate drivers for Channel A |
| 35 | DGND | Digital Ground |
| 36 | DVDD2 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA1, OUT-NA1, OUT-PB1 and OUT-NB1. Can be at a different potential compared to DVDD1. |
| 37 | Out-NA1 | Output N-channel gate drivers for Channel A |
| 38 | N/C | No connect |
| 39 | Out-PA1 | Output P-channel gate drivers for Channel A |
| 40 | DVDD2 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA1, OUT-NA1, OUT-PB1 and OUT-NB1. Can be at a different potential compared to DVDD1. |
| 41 | OUT-PA2 | Output P-channel gate drivers for Channel A |
| 42 | DVDD1 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA2, OUT-NA2, OUT-NA3, OUT-PB2, OUT-NB2 and OUT-NB3. Should be at the same potential as AVDD1. |
| 43 | DGND | Digital Ground |
| 44 | Out-PA3 | Output P-channel gate drivers for Channel A |
| 45 | DVSS | Gate drive supply voltage for OUT-PA3 and OUT-PB3. Supplies digital circuitry portion and the main output stage. Should be at the same potential as AVSS. |
| 46 | VLL | Logic supply voltage |
| 47 | EN | Logic input enable control. When EN = L, all P-channel output drivers are high and all N-channel output drivers are low. |
| 48 | AVSS | Negative driver supply for OUT-PA3, OUT-PB3 and bias circuits. It is also connected to the IC substrate. It should be connected to the most negative potential. |
| Center Pad | AVSS | For the QFN package, the center pad is at AVSS potential. It should be externally connected to AVSS. |

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3.0 DETAILED DESCRIPTION

TABLE 3-1: POWER-UP SEQUENCE

| Step | Connection | Description |
|------|-------------------------------------------------------------------------------|---------------------------------------------------|
| 1 | AV _{SS} , DV _{SS} | Negative gate drive supply and substrate bias |
| 2 | V _{LL} , AV _{DD1} , DV _{DD1} and DV _{DD2} | Logic supply, positive gate drive supply and bias |

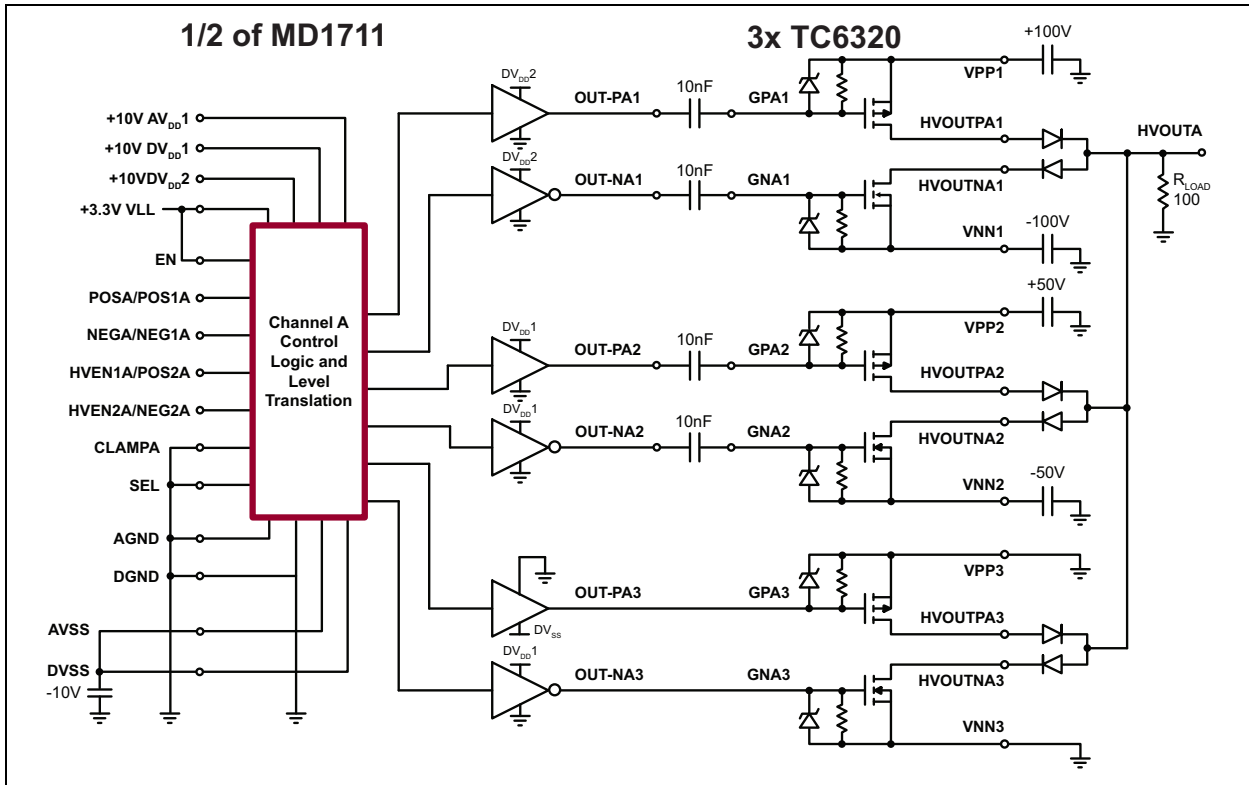


FIGURE 3-1: Test Circuit for Channel A.

TABLE 3-2: TRUTH FUNCTION TABLE FOR CHANNELS A AND B (FOR SEL = L)

| Logic Control Inputs | | | | | | | V _{pp1} to V _{NN1} Output | | V _{pp2} to V _{NN2} Output | | V _{pp3} to V _{NN3} Output | |
|----------------------|----|----------------|----------------|-------|--------------|--------------|---------------------------------------------|----------------------|---------------------------------------------|----------------------|---------------------------------------------|----------------------|
| SEL | EN | HVEN1/ POS2 | HVEN2/ NEG2 | Clamp | POS/ POS1 | NEG/ NEG1 | HV _{OUT} P1 | HV _{OUT} N1 | HV _{OUT} P2 | HV _{OUT} N2 | HV _{OUT} P3 | HV _{OUT} N3 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | OFF | | OFF | | ON | ON |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | | | | | ON | ON |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | | | | | ON | ON |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | | | | | OFF | OFF |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | OFF | OFF | OFF | OFF | OFF | |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | | | | | | |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | | | | | | |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | | | | | | |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | OFF | OFF | OFF | ON | ON | |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | | OFF | ON | OFF | OFF | |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | | ON | OFF | OFF | OFF | |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | | OFF | OFF | OFF | OFF | |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | OFF | OFF | OFF | OFF | OFF | |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | | | | | | |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | | | | | | |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | | | | | | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | OFF | OFF | OFF | | ON | ON |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | OFF | ON | | | OFF | OFF |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | ON | OFF | | | OFF | OFF |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | OFF | OFF | | | OFF | OFF |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | OFF | OFF | OFF | OFF | OFF | |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | | | | | | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | | | | | | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | | | | | | |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | OFF | OFF | OFF | OFF | OFF | |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | | | | | | |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | | | | | | |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | OFF | OFF | OFF | OFF | OFF | |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | | | | | | |
| 0 | 0 | X | X | X | X | X | OFF | | OFF | | OFF | |

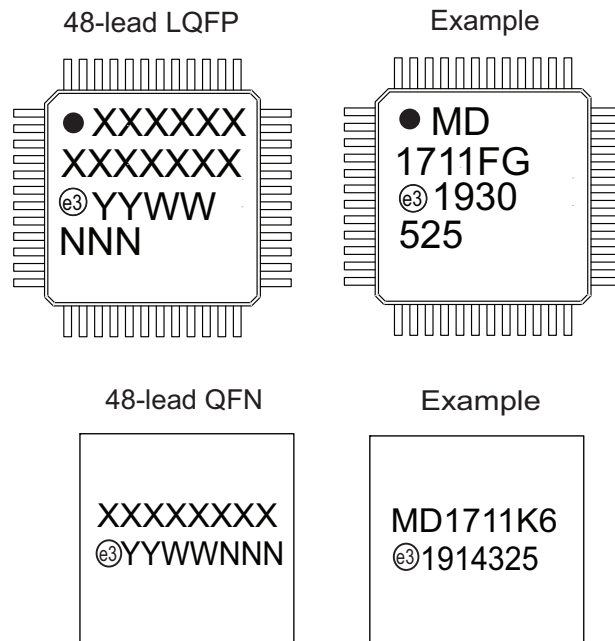
MD1711

TABLE 3-3: TRUTH FUNCTION TABLE FOR CHANNELS A AND B (FOR SEL = H)

| Logic Control Inputs | | | | | | | V _{PP1} to V _{NN1} Output | | V _{PP2} to V _{NN2} Output | | V _{PP3} to V _{NN3} Output | |
|----------------------|----|----------------|----------------|-------|--------------|--------------|---------------------------------------------|----------------------|---------------------------------------------|----------------------|---------------------------------------------|----------------------|
| SEL | EN | HVEN1/ POS2 | HVEN2/ NEG2 | Clamp | POS/ POS1 | NEG/ NEG1 | HV _{OUT} P1 | HV _{OUT} N1 | HV _{OUT} P2 | HV _{OUT} N2 | HV _{OUT} P3 | HV _{OUT} N3 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | OFF | OFF | OFF | OFF | OFF | |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | OFF | OFF | OFF | ON | OFF | |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | OFF | OFF | ON | OFF | OFF | |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | OFF | OFF | ON | ON | OFF | |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | OFF | OFF | OFF | OFF | ON | |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | OFF | OFF | OFF | ON | ON | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | OFF | OFF | ON | OFF | ON | |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | OFF | OFF | ON | ON | ON | |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | OFF | OFF | ON | ON | ON | |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | ON | ON | OFF | OFF | OFF | OFF |

4.0 PACKAGING INFORMATION

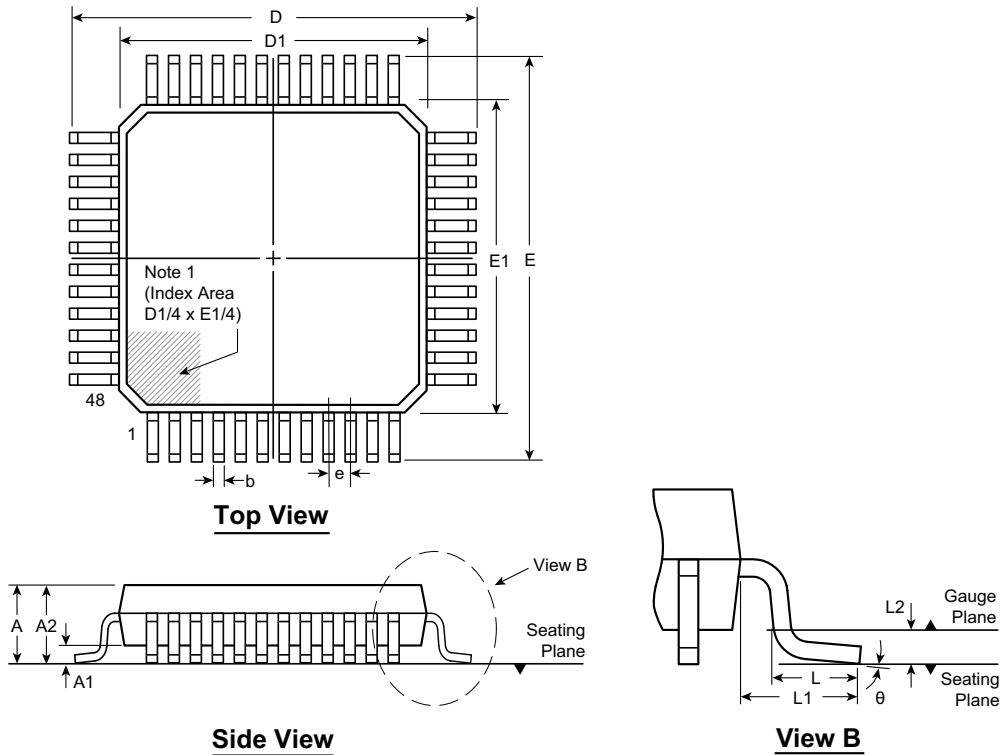
4.1 Package Marking Information



| | | |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| Legend: | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |
| Note: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo. | |

MD1711

48-Lead LQFP Package Outline (FG) 7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

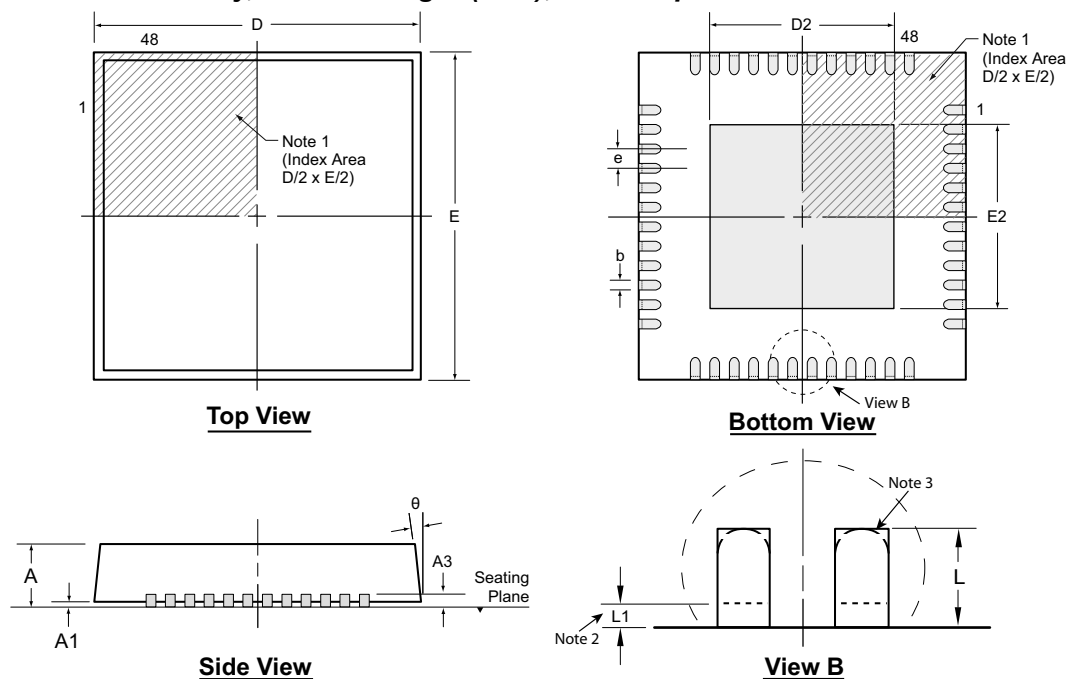
| Symbol | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | θ | |
|----------------|-----|-------|------|------|------|-------|-------|-------|-------|-------------|-------------|-------------|----------|------|
| Dimension (mm) | MIN | 1.40* | 0.05 | 1.35 | 0.17 | 8.80* | 6.80* | 8.80* | 6.80* | 0.50 BSC | 1.00 REF | 0.25 BSC | 0° | |
| | NOM | - | - | 1.40 | 0.22 | 9.00 | 7.00 | 9.00 | 7.00 | | | | 0.45 | 3.5° |
| | MAX | 1.60 | 0.15 | 1.45 | 0.27 | 9.20* | 7.20* | 9.20* | 7.20* | | | | 0.60 | 7° |

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

48-Lead QFN Package Outline (K6) 7.00x7.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

| Symbol | A | A1 | A3 | b | D | D2 | E | E2 | e | L | L1 | θ | |
|----------------|-----|------|------|----------|------|-------|------|-------|------|----------|-------------------|----------|-----|
| Dimension (mm) | MIN | 0.80 | 0.00 | 0.20 REF | 0.18 | 6.85* | 1.25 | 6.85* | 1.25 | 0.50 BSC | 0.30 [†] | 0.00 | 0° |
| | NOM | 0.90 | 0.02 | | 0.25 | 7.00 | - | 7.00 | - | | 0.40 [†] | - | - |
| | MAX | 1.00 | 0.05 | | 0.30 | 7.15* | 5.45 | 7.15* | 5.45 | | 0.50 [†] | 0.15 | 14° |

JEDEC Registration MO-220, Variation VKKD-6, Issue K, June 2006.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings are not to scale.

MD1711

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2019)

- Converted Supertex Doc# DSFP-MD1711 to Microchip DS20005740A
- Changed package marking formats
- Changed the quantity of the 48-lead LQFP FG M931 media type from 3000/Reel to 1000/Reel
- Changed the quantity of the 48-lead VQFN K6 package from 250/Tray to 260/Tray
- Changed the quantity of the 48-lead VQFN K6 M933 media type from 2000/Reel to 3000/Reel
- Made minor text changes throughout the document

MD1711

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| <u>PART NO.</u> | | <u>XX</u> | - | <u>X</u> | - | <u>X</u> |
|-----------------|-----------------|-----------|---|--------------------------------------------|---|------------|
| Device | Package Options | | | Environmental | | Media Type |
| Device: | MD1711 | = | | High-Speed Integrated Ultrasound Driver IC | | |
| Packages: | FG | = | | 48-lead LQFP | | |
| | K6 | = | | 48-lead VQFN | | |
| Environmental: | G | = | | Lead (Pb)-free/RoHS-compliant Package | | |
| Media Types: | (blank) | = | | 250/Tray for an FG Package | | |
| | | = | | 260/Tray for a K6 Package | | |
| | M931 | = | | 1000/Reel for an FG Package | | |
| | M933 | = | | 3000/Reel for a K6 Package | | |

| Examples: | |
|---------------------|---------------------------------------------------------------------|
| a) MD1711FG-G: | High-Speed Integrated Ultrasound Driver IC, 48-lead LQFP, 250/Tray |
| b) MD1711FG-G-M931: | High-Speed Integrated Ultrasound Driver IC, 48-lead LQFP, 1000/Reel |
| c) MD1711K6-G: | High-Speed Integrated Ultrasound Driver IC, 48-lead VQFN, 260/Tray |
| d) MD1711K6-G-M933: | High-Speed Integrated Ultrasound Driver IC, 48-lead VQFN, 3000/Reel |

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