MD1715+TC8020 Demoboard
High Speed ±100V 3.2A Pulser

Features

- Demo dual-transducer ultrasound transmitter
- MD1715 driving TC8020 with 12 MOSFETs
- 5-level voltage pulse waveforms outputs
- ±3.2 A source and sink current capability
- 100MHz frequency clock on board
- Programmable logic waveform generation
- JTAG connection for CPLD programming
- SMA connectors for external clock and signals
- 1.8 to 3.3V CMOS logic interface

Applications

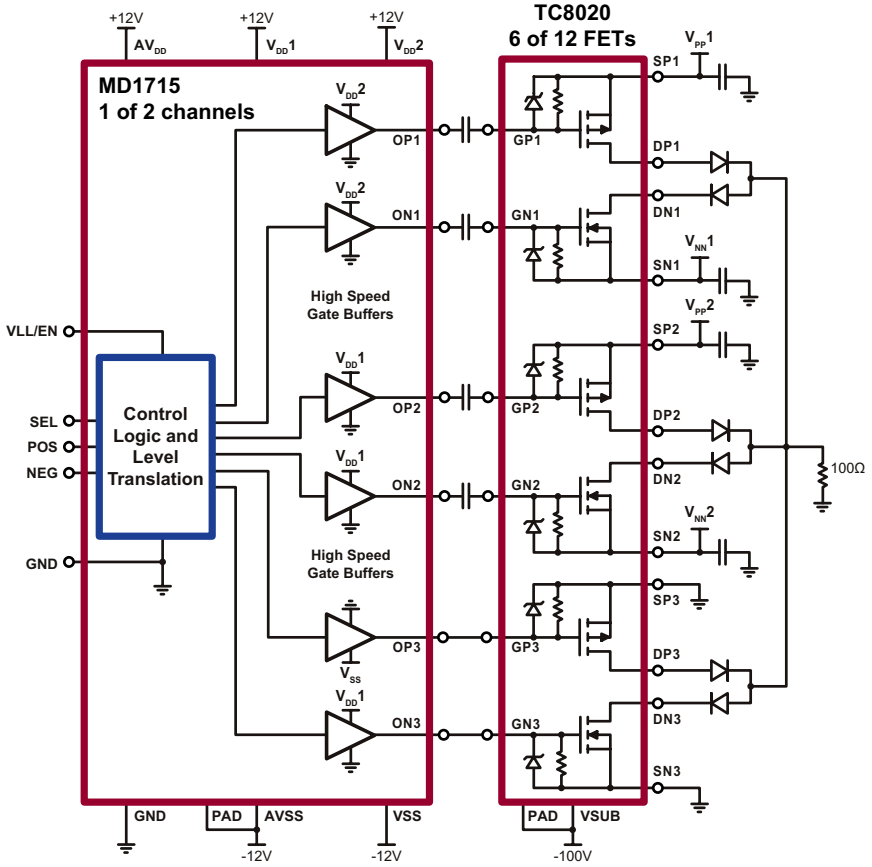
- Medical ultrasound imaging
- Ultrasonic NDT detection
- Piezoelectric transducer drivers
- Capacitive and MEMS sensor driver
- Material flaw detection
- ATE and waveform generator

General Description

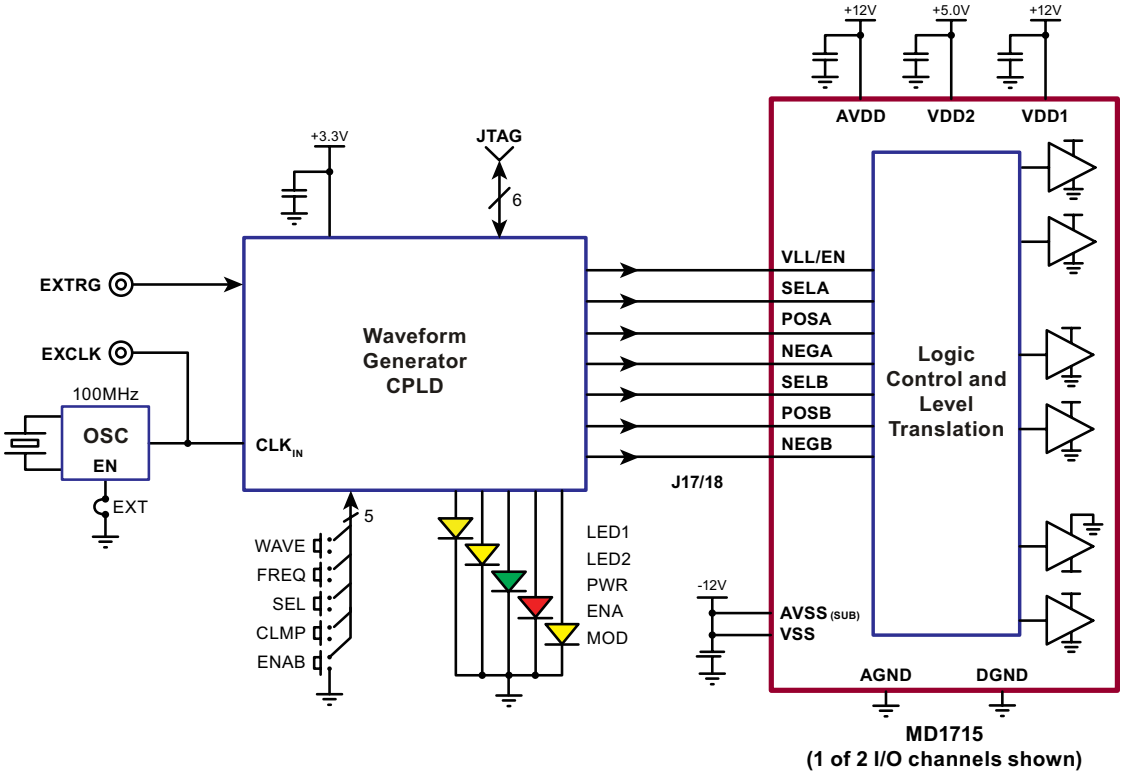
The MD1715DB2 demoboard can drive two transducers as a five-level, two channel transmitter for ultrasound and other applications.

The demoboard consists of one MD1715 in a 6x6mm 40-lead QFN package driving 12 high voltage FETs in six TC8020s in one 8x8mm 56-lead QFN package. The CPLD programmable logic circuit 40MHz crystal oscillator generates accurate timing high-speed waveforms on a separate CPL board. There are multiple frequencie and waveform combinations that can be selected as bipolar pulse waveforms. External clock input can be used if the on board oscillator is disabled. The external trigger input can be used to synchronize the output waveforms. There are five push buttons for selecting the demo waveform, frequency, phase, mode selection functions. Color LEDs indicate the demo selection states. Jumpers on board for select the SMA connector to the external loads or the 220pF//1k on board dummy load.

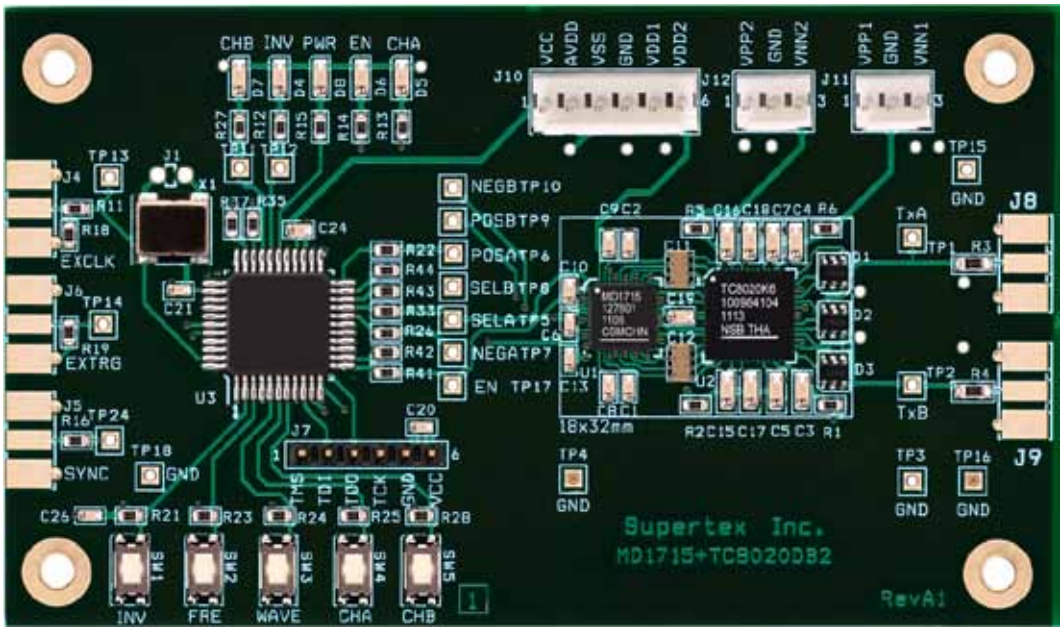
Block Diagram



MD1715/+TC8020DB2 Schematic Block Diagram

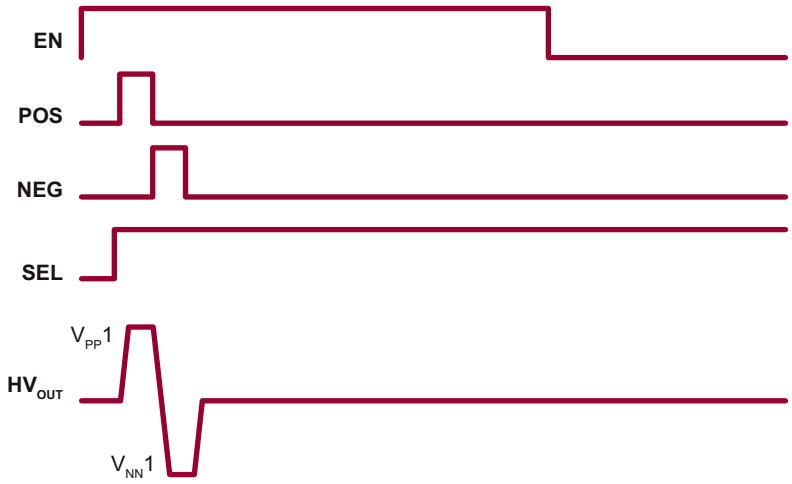


MD1715+TC8020DB2 Demo Board PCB Layout

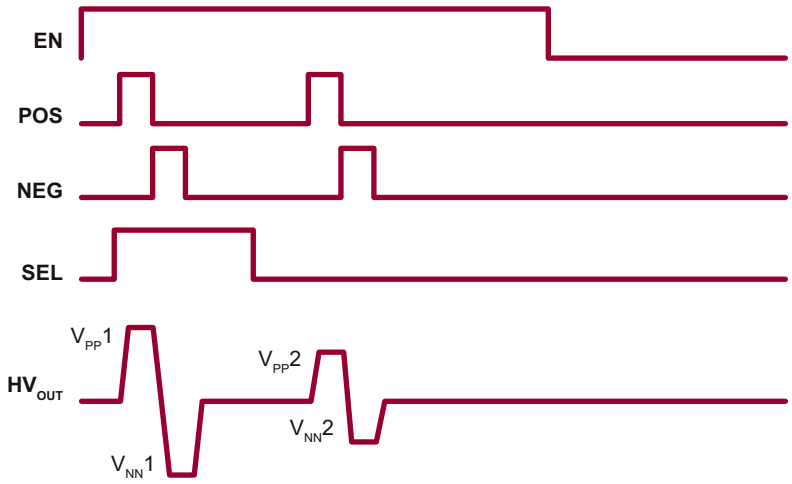


Actual size: 100mm x 60mm

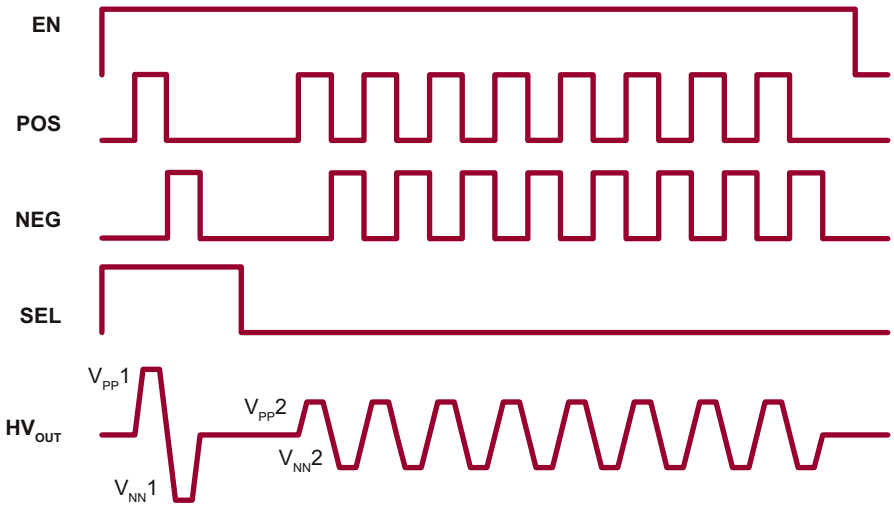
Demo Waveforms (I)



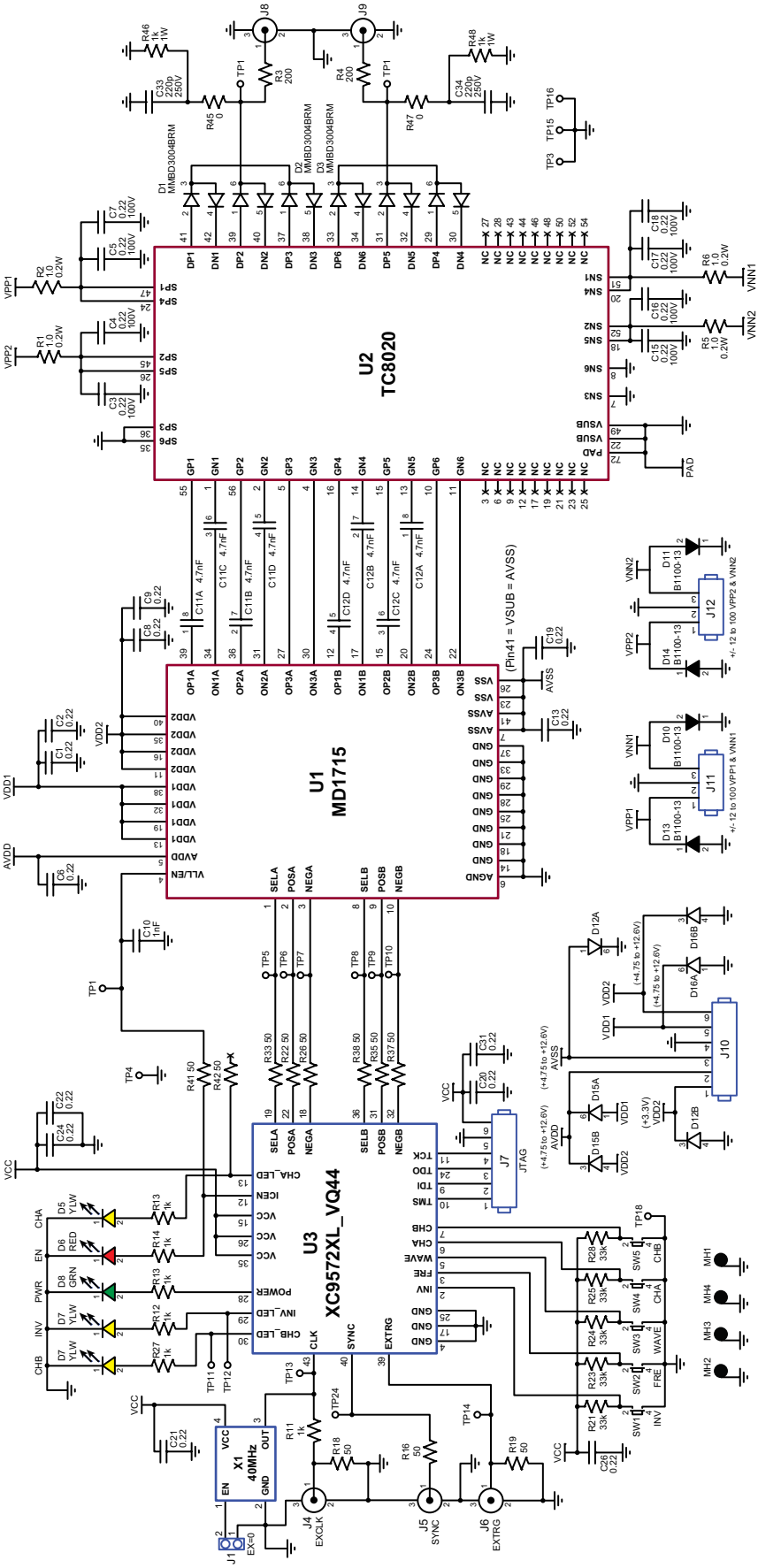
Demo Waveforms (II)



Demo Waveforms (III)



Schematic Diagram



Operating Supply Voltages and Current

Sym	Parameter	Min	Typ	Max	Units	Suggested Current Limit*
VCC/VCC2	Logic Supply	1.8	3.3	3.3	V	150mA
AVDD	Positive Supply Voltage	5.0	10	12	V	10mA
VDD1	Positive Drive Supply	5.0	10	12	V	50mA
VDD2	Positive Drive Supply	5.0	5.0	12	V	25mA
VPP1	TC8020 HV Positive Supply	0	-	100	V	5.0mA
VNN1	TC8020 HV Negative Supply	-100	-	0	V	5.0mA
VPP2	TC8020 HV Positive Supply	0	-	100	V	5.0mA
VNN2	TC8020 HV Negative Supply	-100	-	0	V	5.0mA
AVSS/VSS	TC8020 HV Positive Supply	0	-	-12	V	10mA
VSUB	TC8020 Thermal Pad	-	0	-	V	---
GND	Circuit Ground or 0V	-	0	-	V	---

Note:
** Current limits should change according the testing waveform, frequency and duty cycles.*

Push Button Descriptions

Push Button	Description
INV	Toggles between inverting or non-Inverting
CHA	Toggles between CHA on or off
CHB	Toggles between CHB on or off
FRE	Toggles between 0.3125MHz to 20MHz demo waveforms on Channel-A &B
WAV	Toggles between waveforms on Channel-A and B

Note:
CPLD output signals and push button names are aligned with MD1711 demo board.

LED Descriptions

LED	Description
PWR	Indicates the CPLD board VCC power is connected, LED on = Power on
ENA	Indicates the MD1715 VLL/EN input is High/Low, LED on = CHA or CHB or both ON
INV	Indicates the inverting or non-inverting mode
CHA	Indicates channel-A on/off
CHB	Indicates channel-B on/off

JTAG or Boundary Scan Mode

JTAG or Boundary Scan mode is an industry standard (IEEE 1149.1, or 1532) serial programming mode. External logic from a cable, microprocessor, or other device is used to drive the JTAG specific pins: Test Data Out (TDO), Test Data In (TDI), Test Mode Select (TMS), and Test Clock (TCK). This mode has gained popularity due to its standardization and ability to program CPLD through the same four JTAG pins. The data in this mode is loaded at one bit per TCK.

Testing MD1715DB2 Ultrasound Pulser

Power supply voltages and current limit settings to start the power-up sequence are listed above. Power-down is the reverse of the power-up sequence.

It is important to have the protective Schottky diodes on the MD1715 and the TC8020 pulser circuit PCB on each voltage-rail, just like this demoboard. Only one set of diodes is required per board if multiple pulser channels are on the same PCB. The IC substrate of the MD1715 is internally connected to the AVSS pin. While powering up a multi-voltage rail CMOS chip, one must usually turn one of the substrate bias voltages first, in order to prevent CMOS latch-up. However, with the Schottky diodes on-board, specifically the D9, D12 and D15 diodes, the MD1715 is allowed to power-on the VCC +3.3V first, to establish the CPU and FPGA, etc. and get the digital circuit working first, then power-on the AVSS/DVSS, AVDD/DVDD and VPP/VNN, etc., with the inactive input logic known-state.

Use a ribbon cable to connect the input logic signal connector, J13. Ground pins 3, 5-23 of J13 on the digital logic DGND of the signal generator side. Logic supply voltage V_{CC} must equal the V_{LL} of MD1715. It is usually 1.8, 2.5 or 3.3V DC.

Use a high-impendence oscilloscope probe for all on-board test points. There are two 5:1 voltage attenuators on-board (R6 and R16 are 200Ω) that are designed to connect the high voltage output J3 and J9 SMA connectors via a 50Ω coaxial cable to the oscilloscope (50Ω input) directly. If one needs to connect the J3 or J9 SMA connectors to a testing transducer with a coaxial cable of 50/75Ω, in order to prevent circuit damage due to long cable line reflection, a proper in-series resistor of 40 to 67Ω revise-termination should be considered on R6 or R16, with the impedance matching the cable and transducer load impedances. The TC8020's output impedance is about 8.0Ω.

If an external cable load is used, disconnect the on-board load (220pF // 1.0KΩ) by removing both jumpers on J2 or J8 (1-3) & (2-4), then place one jumper at J2 or J8 (1-2) position. Any overloaded outputs, including shorter pulse duty cycles, longer pulse durations or higher CW voltages (>12V) could damage the IC or MOSFETs.

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