MIC2155

Two-Phase Single-Output PWM Synchronous Buck Control IC

Features

- Synchronous Buck Control IC with Outputs Switching 180 Degrees Out of Phase
- Remote Sensing with Internal Differential Amplifier
- 4.5V-to-14.5V Input Voltage Range
- Adjustable Output Voltages down to 0.7V
- 1% Output Voltage Accuracy
- Starts up into a Pre-biased Output
- 500 kHz PWM Operation
- Adaptive Gate Drive allows Efficiencies of over 95%
- Adjustable Current Limit with no Sense Resistor
- Senses Low-Side MOSFET Current
- Internal Drivers allow 25A per Phase
- Power Good Output allows Simple Sequencing
- Dual Enable Pins with Micro-Power Shutdown and UVLO
- Programmable Soft-Start Pin
- Output Overvoltage Protection
- Works with Ceramic Output Capacitors
- Multi-Input Supply Capability
- Single-Output High-Current Capability with Master/Slave Current Sharing
- External Synchronization
- Small Footprint 32-Pin 5 mm × 5 mm VQFN
- Junction Temperature Range of –40°C to +125°C

Applications

- Multi-Output Power Supplies with Sequencing
- DSP, FPGA, CPU and ASIC Power Supplies
- DSL Modems
- Telecommunications and Networking Equipment
- Servers

General Description

The MIC2155 is a two-phase, single-output synchronous buck control IC that features small size, high efficiency, and a high level of flexibility. The IC implements a 500 kHz Voltage mode PWM control with the outputs switching 180 degrees out of phase. The result of the out-of-phase operation is 1 MHz (or 600 kHz) input ripple with ripple current cancellation, minimizing the required input filter capacitance. A 1% output voltage tolerance allows the maximum level of system performance. Internal drivers with adaptive gate drive allow the highest efficiency with the minimum external components.

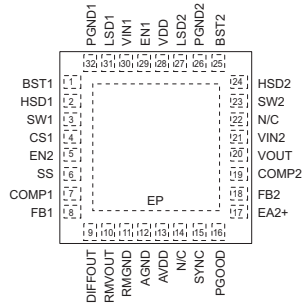
Two independent enable pins and a power good output are provided, allowing a high level of control and sequencing capability.

The MIC2155 has an operating junction temperature ranging from –40°C to +125°C.

Data sheets and support documentation can be found on the Microchip website at www.microchip.com.

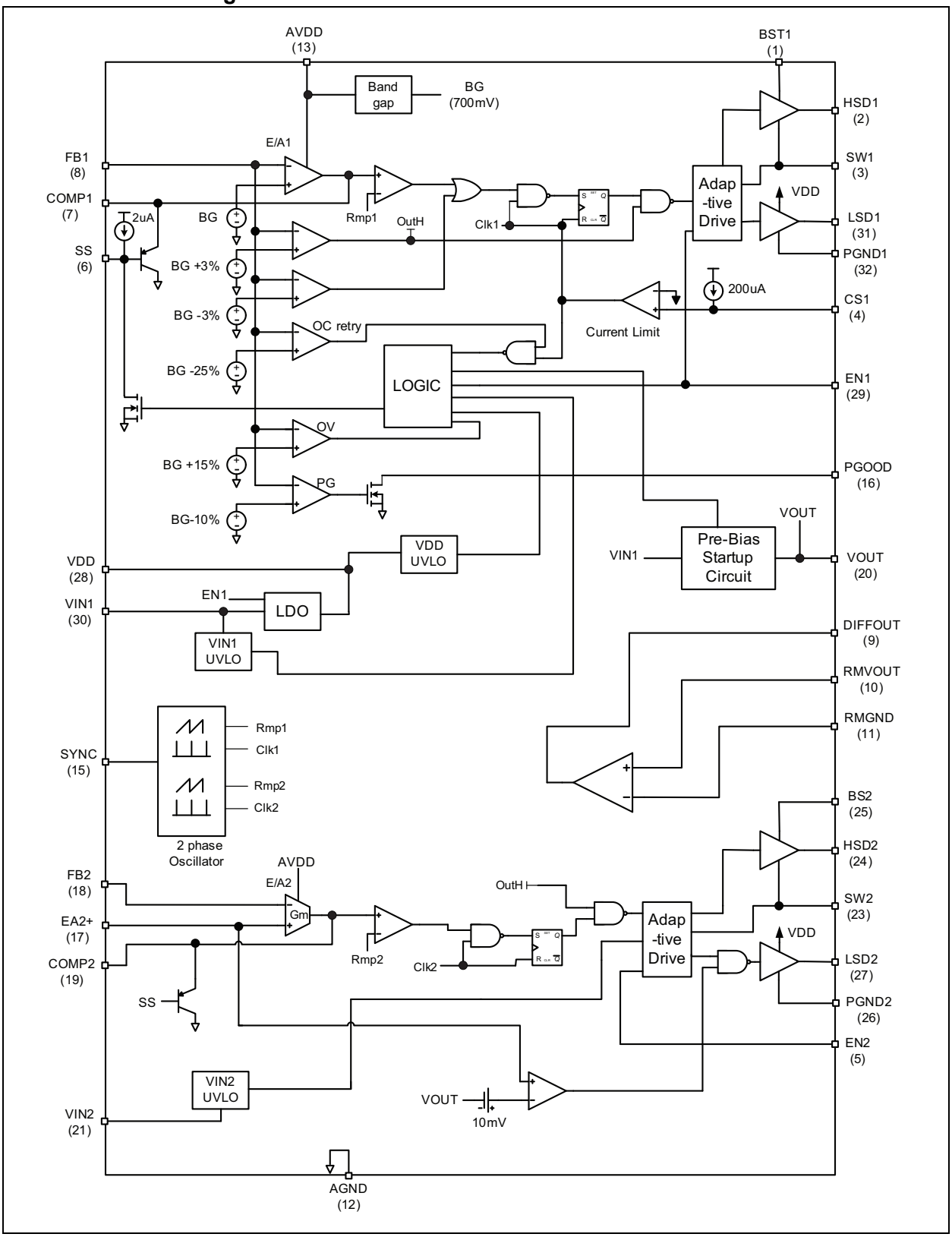
Package Type

32-lead 5 mm x 5 mm VQFN
(Top view)

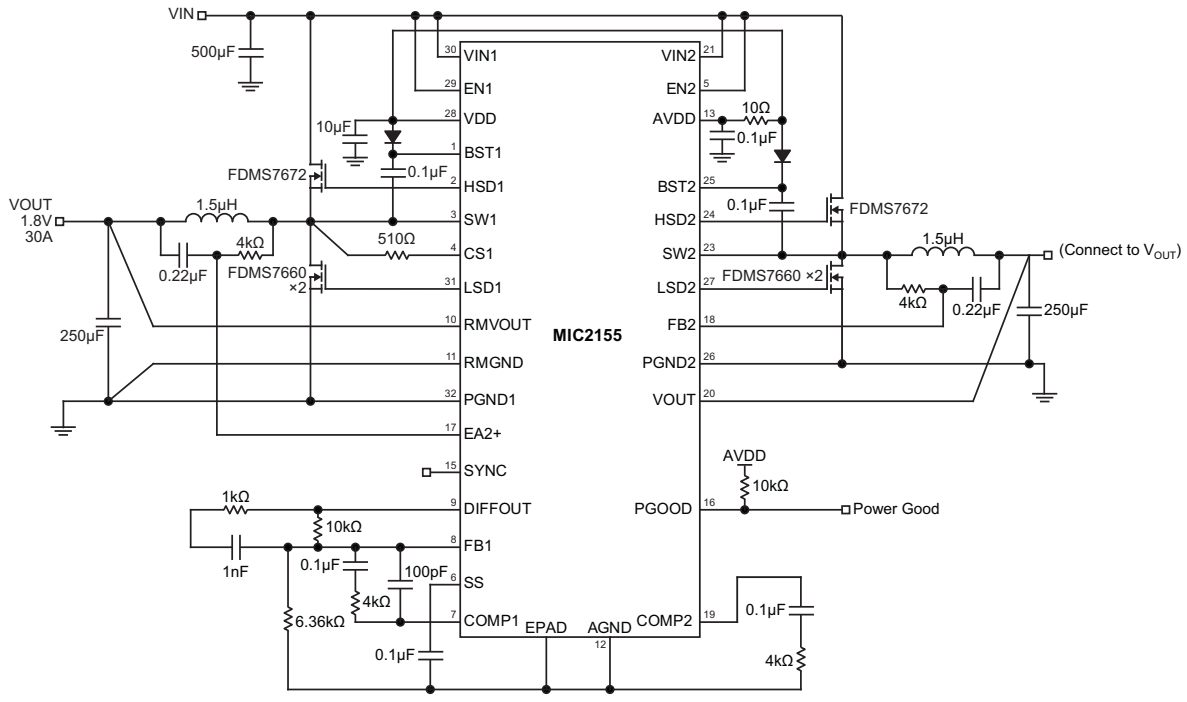


See Table 3-1 for pin information.

Functional Block Diagram



Typical Application Circuit



30A Two-Phase Converter

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage, (V_{IN1},V_{IN2}) ..... –0.3V to 15V
Bootstrapped Voltage, (V_{BST}) ..... V_{IN} +6V
SS, FB1, RMV_{OUT}, RM_{GND}, A_{VDD}, SYNC, EA2+, FB2, V_{OUT} ..... –0.3V to 6V
CS1, EN1, EN2 ..... –0.3V to 15V
Junction Temperature, T_J ..... –40°C to +150°C
Storage Temperature, T_S ..... –65°C to +150°C
ESD, Machine Model 100V
ESD, Human Body Model 1500V
Lead Temperature (Soldering 10 Seconds) ..... 260°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{IN1},V_{IN2}	+4.5	—	+14.5	V	**Note 1**
Output Voltage	V_{OUT}	+0.7	—	+3.6	V	**Note 1**

Note 1: The device is not guaranteed to function outside its operating rating.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_J = 25°C; V_{EN} = V_{IN1} = V_{IN2} =12V; unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ 125°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{IN1},V_{IN2}	+4.5	—	+14.5	V	
Output Voltage	V_{OUT}	+0.7	—	+3.6	V	
V_{IN},V_{DD}, V_{REF} SUPPLY						
Total Quiescent Supply Current, I_{VIN1} + I_{VIN2}	I_{VIN}	—	6	**10**	mA	V_{FB} = 0.8V (both O/Ps; non-switching)
Shutdown Current	I_{SD}	—	210	**300**	µA	V_{EN1} = V_{EN2} = 0V
CH1 V_{IN} UVLO Start Voltage	V_{IN1UV_R}	**3.6**	4	**4.4**	V	V_{DD} = Open
CH1 V_{IN} UVLO Stop Voltage	V_{IN1UV_F}	**3.4**	3.97	**4.2**	V	V_{DD} = Open
CH2 V_{IN} UVLO Start Voltage	V_{IN2UV_R}	**2.5**	2.7	**2.9**	V	V_{DD} = Open
CH2 V_{IN} UVLO Stop Voltage	V_{IN2UV_F}	**2.3**	2.5	**2.7**	V	V_{DD} = Open
V_{DD} UVLO Start Voltage	V_{DDUV_R}	—	3.6	—	V	V_{IN1} = V_{DD} for V_{IN} < 6V
V_{DD} UVLO Stop Voltage	V_{DDUV_F}	—	3.3	—	V	V_{IN1} = V_{DD} for V_{IN} < 6V
V_{IN} UVLO Hysteresis	V_{INUV_HYS}	—	40	—	mV	V_{DD} = open
V_{EN} Shutdown Threshold	V_{EN_SD}	**0.6**	1	**1.6**	V	Each Channel
V_{EN} Hysteresis	V_{EN_HYS}	—	30	—	mV	Each Channel
Internal Bias Voltage	V_{DD}	4.9	5.25	5.6	V	I_{VDD} = –75 mA
		4.9	5	5.6	V	I_{VDD} = –50 mA, V_{IN} = 6V

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Minimum on-time before automatic cycle skipping begins.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_J = 25°C; V_{EN} = V_{IN1} = V_{IN2} =12V; unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ 125°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
OSCILLATOR/PWM SECTION						
PWM Frequency per Channel	f_s	450	510	550	kHz	
Sync Range	f_{SYNC}	860	—	1200	kHz	Sync Input is 2x PWM Frequency
Sync Level	V_{SYNC}	**0.5**	—	**3**	V	
Maximum Duty Cycle	$D_{(MAX)}$	**80**	—	—	%	Each channel
Minimum Headroom between V_{DD} and V_{OUT}	$V_{HR(MIN)}$	—	—	**1.3**	V	Required for remote sense amplifier use
Minimum On-Time	$t_{ON(MIN)}$	—	30	—	ns	Each channel (**Note 2**)
REGULATION						
CH1 Feedback Voltage Reference	V_{FB}	693	697	707	mV	+/–1%
		686	697	**714**	mV	+/–2%
CH1 Feedback Bias Current	I_{FB}	—	30	—	nA	V_{FB} = 0.7V
Output Voltage Line Regulation	ΔV_{OUT_LINE}	—	0.08	—	%	4.5V ≤ V_{IN} ≤ 14.5V
Output Voltage Load Regulation	ΔV_{OUT_LOAD}	—	0.5	—	%	
Output Voltage Total Regulation	ΔV_{OUT_TOTAL}	—	0.6	—	%	4.5V ≤ V_{IN} ≤ 14.5V; 1A ≤ I_{OUT} ≤ 10A (V_{OUT} = 2.5V)
CHANNEL CURRENT BALANCING						
Asynchronous Mode V_{TH} for Slave Output	V_{TH_ASYN}	—	10	—	mV	
ERROR AMPLIFIER (CH1)						
DC Gain	G_{EA1}	—	70	—	dB	
Output Sourcing/Sinking Current	$I_{SNK/SRC}$	—	1	—	mA	
ERROR AMPLIFIER (CH2)						
DC Gain	G_{EA2}	—	70	—	dB	
Transconductance	g_m	—	1.25	—	mS	
DIFFERENTIAL AMPLIFIER						
Voltage Gain	G_{DA}	—	1	—		
Offset Voltage	V_{OS}	**–20**	—	**+20**	mV	
Output Sourcing Current Range	I_{SRC_DA}	0	—	500	µA	
OUTPUT OVERVOLTAGE PROTECTION						
OV Threshold	OV_{TH}	**106**	109	**114**	$\%V_{REF}$	V_{FB} = OV_{TH}, Latch LSD High
Delay Blanking time	t_{BLANK_OV}	—	1	—	µs	
SOFT START						
Internal Soft-Start Source Current	I_{SS}	1.25	2	2.75	µA	T_J = 25°C
		1		**4**	µA	–40°C ≤ T_J ≤ 125°C
CURRENT SENSE						
CS Overcurrent Trip Point Program Current	I_{CL}	180	195	220	µA	
CS Comparator Sense Offset Voltage	V_{CL_OS}	**–10**	0	**+10**	mV	Senses drop across low-side FET
POWER GOOD						
Power Good Threshold	PG_{TH}	**86**	88.5	**91**	$\%V_{REF}$	Sweep V_{FB} from Low to High
Power Good Voltage Low	V_{PG_LOW}	—	0.225	0.3	V	V_{FB} = 0 V; I_{PGOOD} = 1 mA

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Minimum on-time before automatic cycle skipping begins.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_J = 25°C; V_{EN} = V_{IN1} = V_{IN2} =12V; unless otherwise specified. Bold values indicate –40°C ≤ T_J ≤ 125°C.

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
GATE DRIVERS							
Rise/Fall Time	Source	t_{RISE}	—	23	—	ns	Source into 3000 pF
	Sink	t_{FALL}		16		ns	Sink out of 3000 pF
High-Side Drive Resistance	Source	R_{HSD_H}	—	1.6	**3.5**	Ω	V_{DD} = V_{IN} = 5V
	Sink	R_{HSD_L}		1.7	**2.5**	Ω	
Low-Side Drive Resistance	Source	R_{LSD_H}	—	2	**3.5**	Ω	V_{DD} = V_{IN} = 5V
	Sink	R_{LSD_L}	—	1.4	**2.5**	Ω	
Driver Non-Overlap Time (Adaptive)		t_{NON}	—	60	—	ns	

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Minimum on-time before automatic cycle skipping begins.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	–40	—	+125	°C	
Maximum Junction Temperature	$T_{J(ABSMAX)}$	—	—	+150	°C	
Ambient Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
32-lead 5mm × 5mm VQFN	θ_{JA}	—	50	—	°C/W	
	θ_{JC}	—	5	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

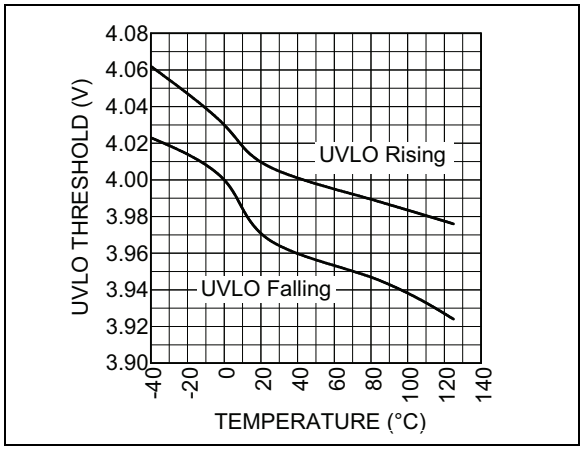


FIGURE 2-1: *VN1 UVLO Threshold.*

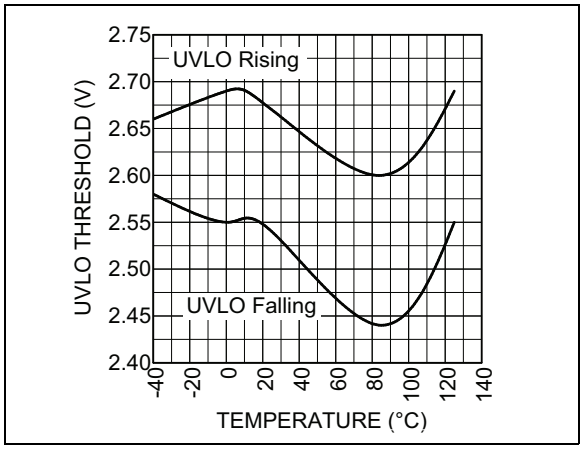


FIGURE 2-2: *VIN2 UVLO Threshold.*

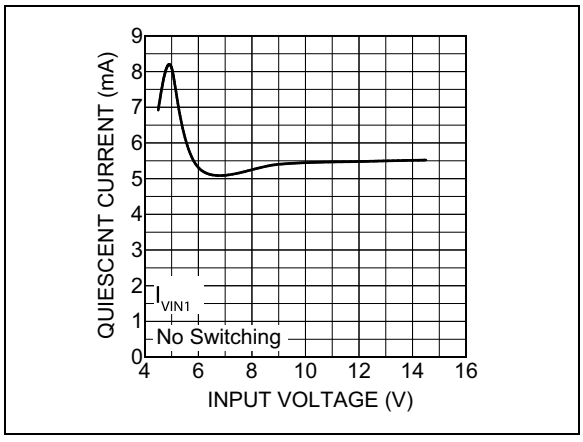


FIGURE 2-3: *Quiescent Current 1 vs. Input Voltage.*

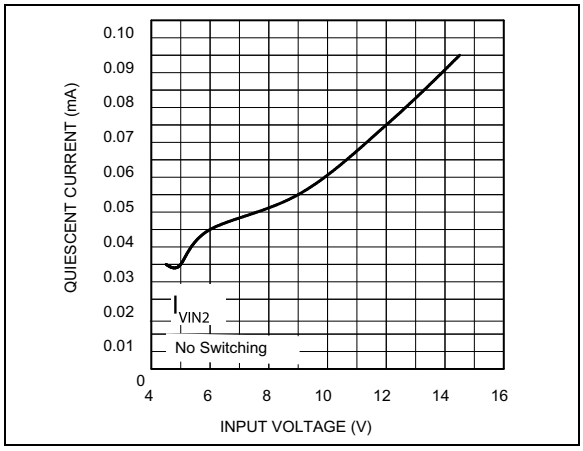


FIGURE 2-4: *Quiescent Current 2 vs. Input Voltage.*

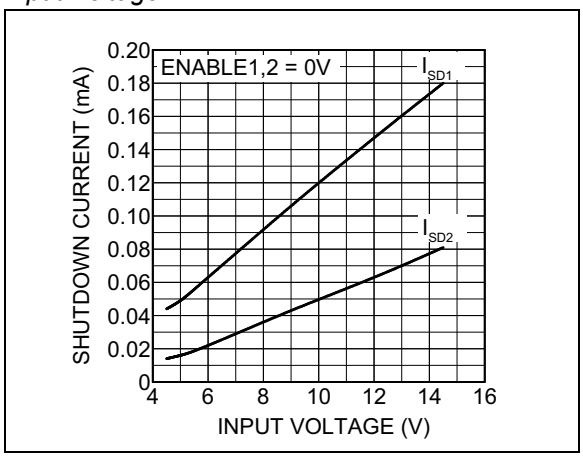


FIGURE 2-5: *Shutdown Current vs. Input Voltage.*

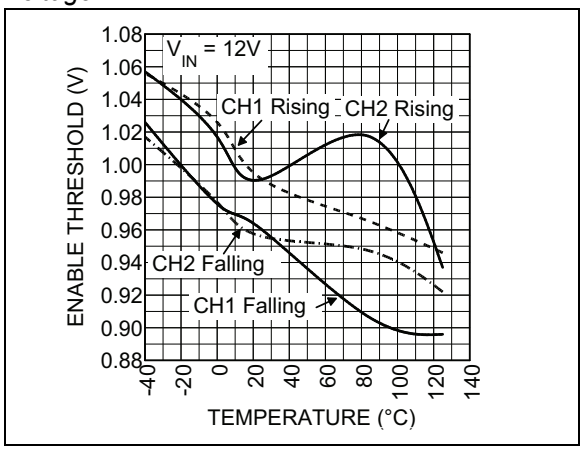


FIGURE 2-6: *Enable Threshold vs Temperature.*

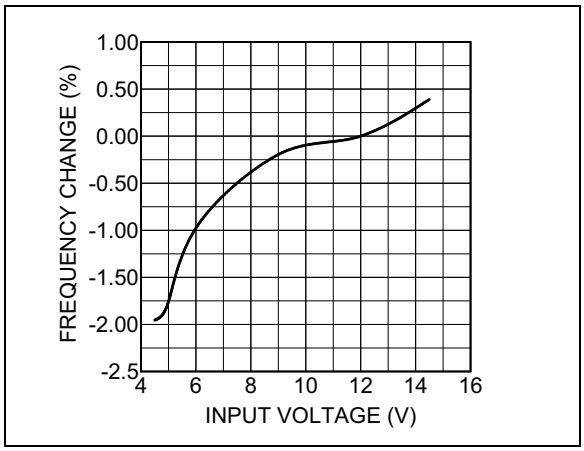


FIGURE 2-7: *Change in Switching Frequency vs. Input Voltage.*

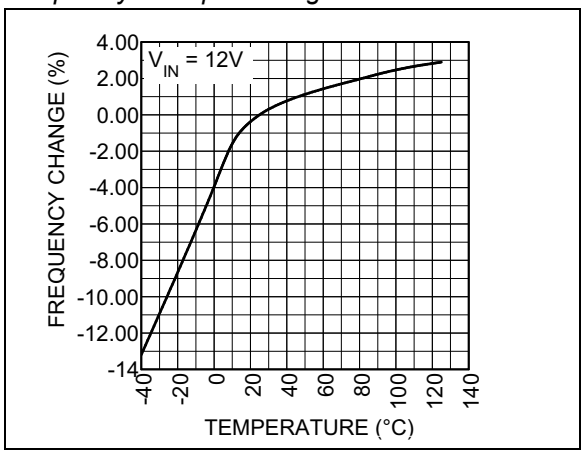


FIGURE 2-8: *Change in Switching Frequency vs. Temperature.*

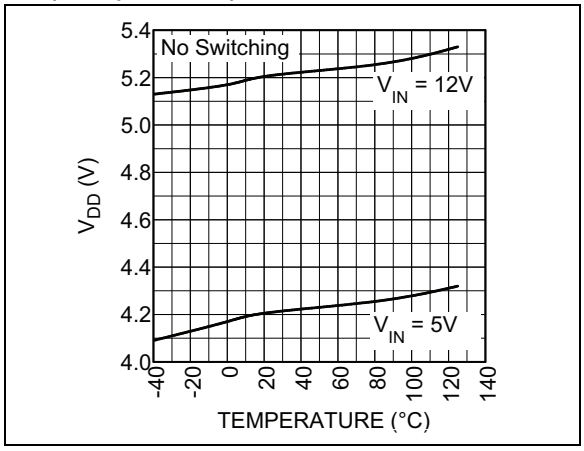


FIGURE 2-9: *V_{DD} vs. Temperature.*

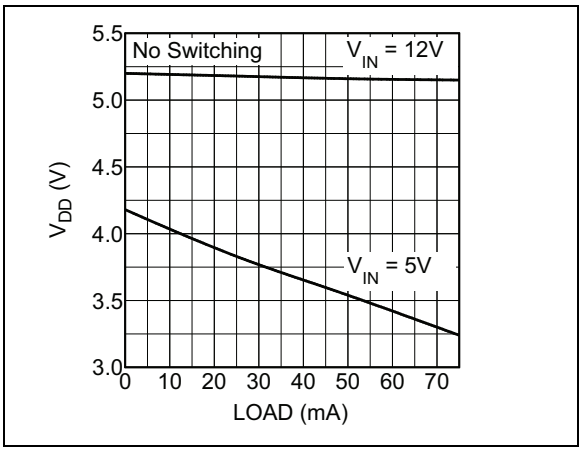


FIGURE 2-10: *V_{DD} vs. Load.*

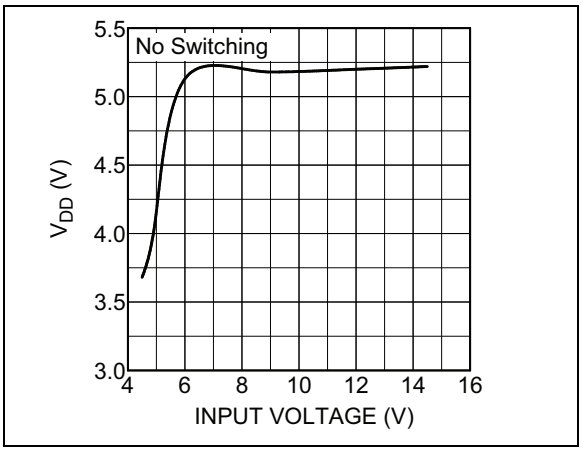


FIGURE 2-11: *V_{DD} vs. Input Voltage.*

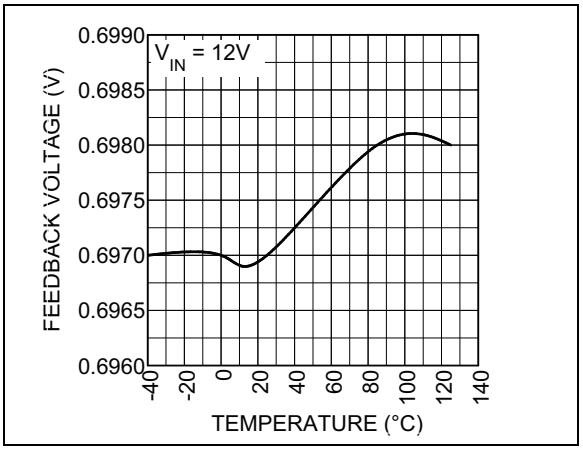


FIGURE 2-12: *Feedback Voltage vs. Temperature.*

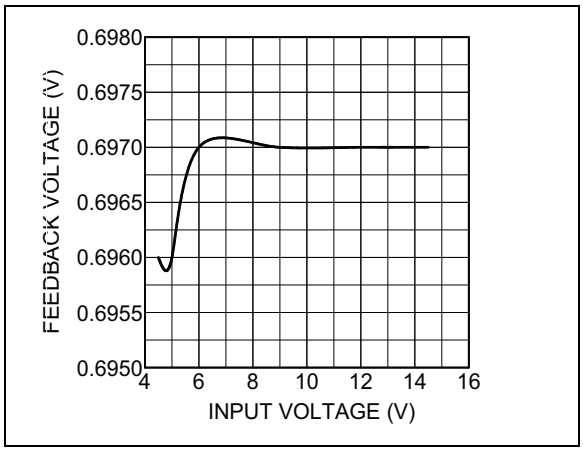


FIGURE 2-13: *Feedback Voltage vs. Input Voltage.*

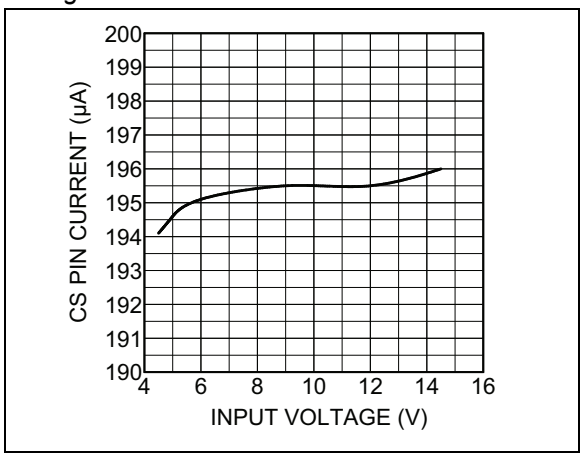


FIGURE 2-14: *CS Pin Current vs. Input Voltage.*

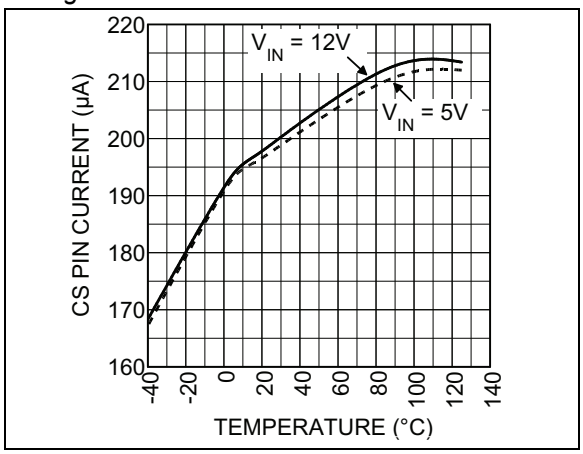


FIGURE 2-15: *CS Pin Current vs. Temperature.*

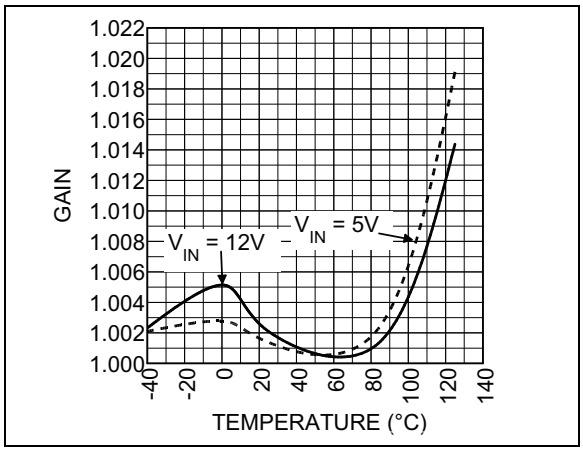


FIGURE 2-16: *Differential Amplifier Gain vs. Temperature.*

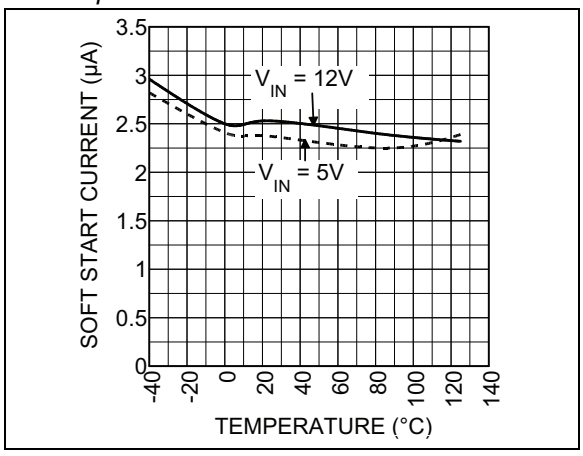


FIGURE 2-17: *Soft-Start Current vs. Temperature.*

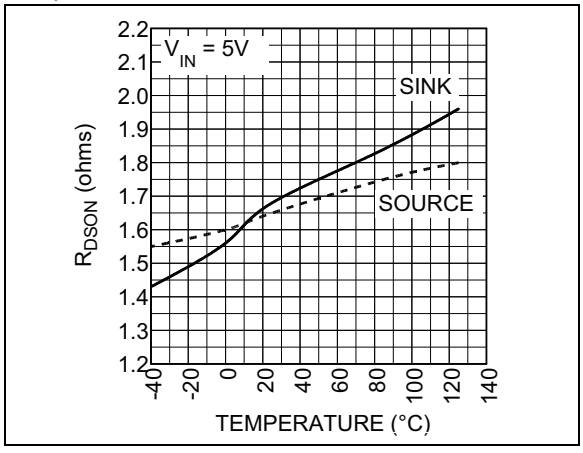


FIGURE 2-18: *R_{DSON} High-Side Drive Source/Sink.*

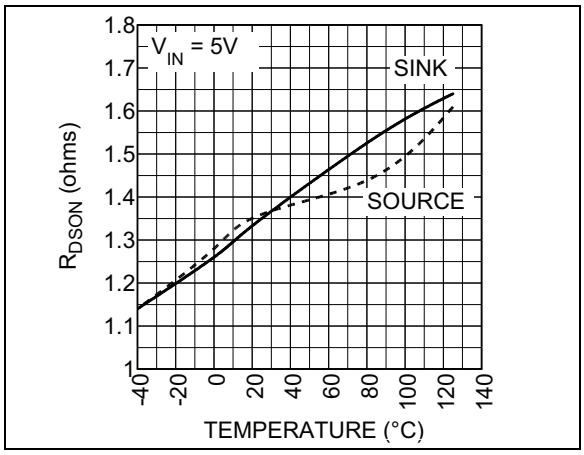


FIGURE 2-19: *R_{DSON} Low-Side Drive Source/Sink.*

3.0 PIN DESCRIPTION

The details on the pins of MIC2155 are listed in Table 3-1. Refer to **Package Type** for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	BST1	Boost 1 (input): Provides voltage for high-side MOSFET Driver 1. The gate drive voltage is higher than the high-side MOSFET source voltage by V_{DD} minus a diode drop.
2	HSD1	High-side Driver 1 (output): High-current driver output for Channel 1 external high-side MOSFET.
3	SW1	Switch Node 1 (output): Return for HSD1
4	CS1	Current Sense 1 (input): Current-limit comparator non-inverting input. Current is sensed across the Channel 1 low-side FET during the off-time. Current limit is set by the resistor between the CS1 pin and drain of the Channel 1 low-side FET.
5	EN2	Enable 2 (input): Channel 2 enable. Pull high to enable. Pull low to disable.
6	SS	Soft Start (input): Controls the turn-on time of the output voltage. Active at Power-up, Enable, and Current limit recovery.
7	COMP1	Compensation 1 (input): Output of the internal error amplifier for Channel 1.
8	FB1	Feedback 1 (input): Negative input to the error amplifier of Channel 1.
9	DIFFOUT	Output of remote sense differential amplifier.
10	RMVOUT	Remote V_{OUT}: Connect to V_{OUT} at the remote sense point. Input to precision differential amplifier.
11	RMGND	Remote Ground: Connect to ground at the remote sense point. Input to precision differential amplifier.
12	AGND	Analog Ground
13	AVDD	Analog Supply Voltage (input): Connect to V_{DD} through an RC filter network.
14	N/C	No connect
15	SYNC	Sync (input): Synchronizes switching to an external source. Leave floating when not used.
16	PGOOD	Power Good (output): Asserts high when voltage on the FB pin rises above Power Good threshold.
17	EA2+	Positive Input to Channel 2 (current-sharing) error amplifier (Input): Connect to Channel 1 current sense.
18	FB2	Negative input to Channel 2 (current sharing) error amplifier (Input): Connect to Channel 2 current sense.
19	COMP2	Compensation 2 (input): Pin for external compensation of Channel 2 error amplifier.
20	VOUT	Output Sense (input): Connect to output side of inductors. Used for current sharing.
21	VIN2	Supply Voltage for Channel 2 (input): Used for Channel 2 UVLO circuit.
22	N/C	No connect
23	SW2	Switch Node 2 (output): Return for HSD2.
24	HSD2	High-side Driver 2 (output): High-current driver output for Channel 2 high-side MOSFET.
25	BST2	Boost 2 (input): Provides voltage for high-side MOSFET driver in Channel 2. The gate drive voltage is higher than the high-side MOSFET source voltage by V_{DD} minus a diode drop.
26	PGND2	Power Ground 2: High current return for Low-Side Driver 2.
27	LSD2	Low-side Driver 2 (output): High-current driver output for Channel 2 low-side external MOSFET.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
28	VDD	5V Internal Linear Regulator from V_{IN1} (output): V_{DD} is the external MOSFET gate driver supply voltage and an internal supply bus for the IC. When V_{IN1} is <5V, this regulator operates in Dropout mode. Connect external bypass capacitor.
29	EN1	Enable 1 (input): Output enable. Turns off both channels. Pull high to enable. Pull low to disable.
30	VIN1	Supply Voltage for Channel 1 (input): Used for UVLO and V_{DD} circuits.
31	LSD1	Low-side Driver 1 (output): High-current driver output for Channel 1 low-side external MOSFET.
32	PGND1	Power Ground 1: High current return for low-side Driver 1.
EP	EPAD	Exposed Pad (power): Must make a full connection to the GND plane to maximize thermal performance of the package.

4.0 FUNCTIONAL DESCRIPTION

The MIC2155 is a two-phase, synchronous buck controller operating at a fixed frequency. The device switches at 500 kHz per phase (1 MHz at the input and output).

The following are some advantages of multi-phase operation:

- Smaller input and output filtering components are required because of current cancellation and higher input and output frequency.
- Faster transient response is possible with smaller output filter component values.
- Load current through each phase is one-half the total output current, which allows for even heat distribution and smaller components.
- Control circuitry forces better current sharing in the MOSFETs than paralleling FETs in a single-phase application.

The controller utilizes a Voltage-mode control scheme (VMC). Lossless current sharing is accomplished by sensing the DC voltage across each inductor winding. Lossless overcurrent protection is performed by sensing the voltage across the low-side MOSFET on-resistance during the off-time.

Other features of the controller are:

- Overvoltage protection
- Soft start
- UVLO
- Enable
- Remote sensing
- Pre-biased output startup
- Multiple input supplies
- Power good signal
- Frequency synchronization

4.1 Startup

A typical startup sequence is shown in Figure 4-1 (also refer to the **Functional Block Diagram**). The enable pins are asserted after V_{IN} is applied. V_{DD} is immediately turned on and an internal FET releases the soft-start pin. The soft-start pin controls the error amplifier voltage. As V_{SS} ramps up, it reaches a threshold where the gate drive is enabled and the MOSFETs start to switch at a very low duty cycle. The rise of the soft-start voltage controls the increase in V_{OUT} by gradually allowing the COMP1 pin voltage to rise. A 10 mV offset in the current controller keeps the Channel 2 low-side drive off when the output current is low to prevent current from circulating between the phases. PGOOD is asserted when V_{OUT} reaches the PGOOD threshold.

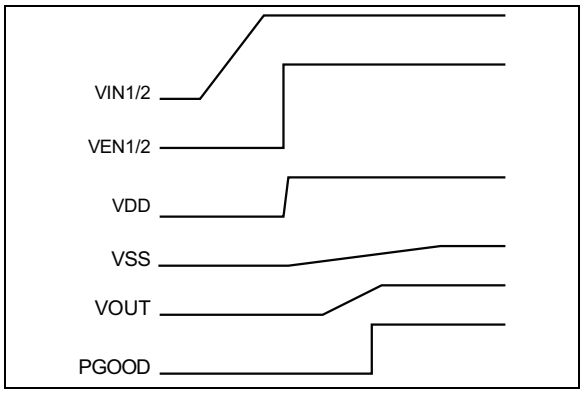


FIGURE 4-1: *Startup Sequence.*

A typical output voltage and inductor current startup waveforms are shown in Figure 4-2.

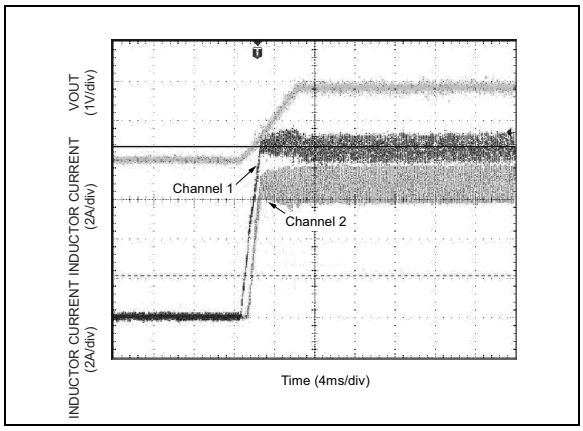


FIGURE 4-2: *Turn on Waveforms.*

4.2 Soft-Start

The soft-start circuitry controls how fast the output voltage rises by controlling the COMP pin rise time. Without soft start, a fast or uncontrolled turn-on requires a higher current from the input source to charge up the output capacitance.

The soft-start circuitry also controls the delay time between the enable pin assertion to when V_{OUT} starts to rise. An internal 2 µA (typical) soft-start current source is used to charge up an external soft-start capacitor. Figure 4-3 and Figure 4-4 show the soft-start circuitry and waveform timing.

The output voltage starts to rise when V_{SS} is approximately 1 diode drop above ground, 0.6V.

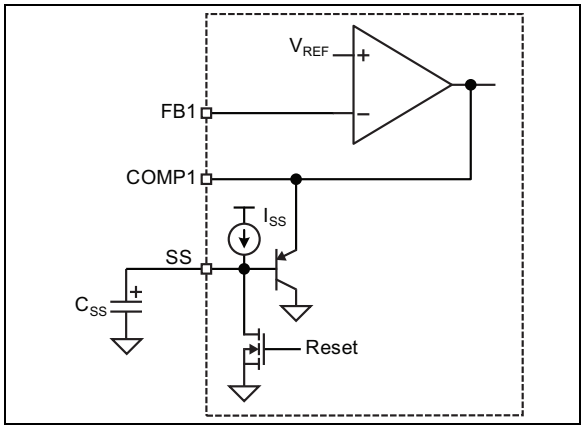


FIGURE 4-3: *Soft-Start Circuit.*

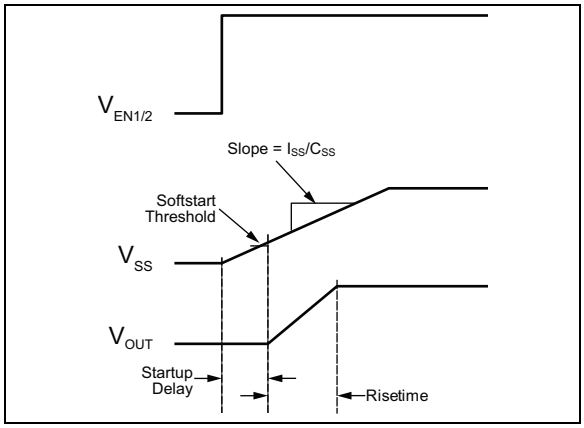


FIGURE 4-4: *Soft-Start Waveforms.*

The startup delay and output voltage rise time can be programmed by the external soft-start capacitor value and approximated using the formula in Equation 4-1 and Equation 4-2, respectively.

EQUATION 4-1:

Delay:

$$t_d = \frac{C_{SS} \times 0.6V}{I_{SS}}$$

EQUATION 4-2:

Rise time:

$$t_R = \frac{C_{SS} \times V_{OUT}}{V_{IN} \times I_{SS}}$$

The soft start pin is pulled to ground and the soft-start capacitor is discharged under the following conditions:

- EN1 pin De-asserted
- UVLO on the V_{IN1} or V_{DD} pins
- Overcurrent
- Overvoltage (latched off)

4.3 Enable

There is an enable pin for each of the two channels. Asserting EN1 enables Channel 1 gate drive and VDD internal 5V LDO as well as releases the soft-start circuit. De-asserting EN1 disables the gate drive, discharges C_{SS}, and disables V_{DD}. It brings the controller into a low-current OFF state.

Enable 2 only controls switching of Channel 2. Disabling Channel 2 stops the switching of the power FETs on Channel 2 which reduces the V_{DD} current draw. This can improve efficiency when operating at low output current, especially when large MOSFETs are used.

4.4 Supply Voltages and Internal Regulator

The MIC2155 is powered from a 4.5V to 14.5V supply. The two input supply pins (VIN1 and VIN2) are connected together in most applications. They are powered separately in configurations with two input supply voltages.

VIN1 supplies an internal LDO, which generates the V_{DD} supply voltage. VDD is used to power the gate drive circuitry and must be externally decoupled to the power ground pins (PGND1 and PGND2). A 10 µF ceramic capacitor is recommended for most applications. The AVDD pin is the supply pin for the Bandgap reference and internal analog circuits. A small RC filter (10Ω, 0.1 µF) connected to AVDD is recommended to help attenuate switching noise from the VDD supply.

The dropout of the internal VDD regulator causes VDD to drop if VIN1 is below 6V. When operating below 6V, VDD may be jumpered to VIN1. This bypasses the internal LDO and prevents VDD from dropping out.

An external LDO or simple series pass regulator can be used to limit the VDD voltage for applications with an input voltage that spans above and below the 6V maximum V_{DD} limit. Figure 4-5 and Figure 4-6 illustrate two examples of regulating VDD with external circuitry.

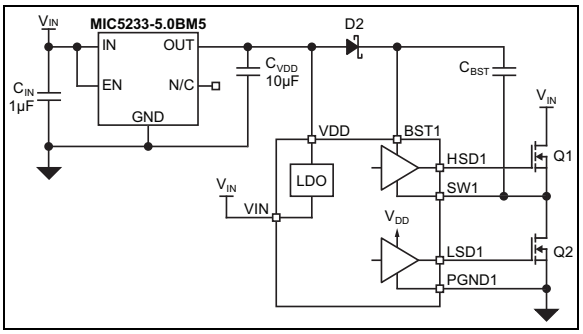


FIGURE 4-5: *LDO Regulator.*

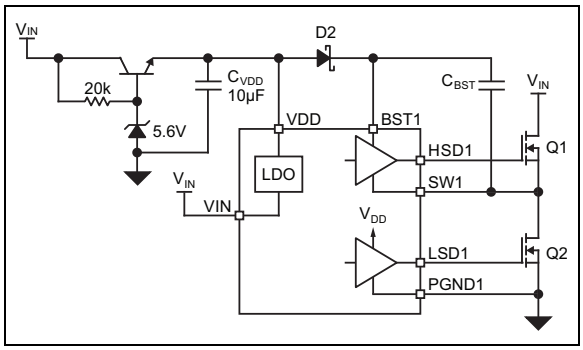


FIGURE 4-6: *Emitter Follower Regulator.*

The internal VDD regulator can supply up to 75 mA of current to drive the external MOSFETs. Power dissipation inside the MIC2155 control IC is divided between power dissipated in the controller's analog circuitry and power dissipated in the drive circuitry. Drive circuitry power is almost always much greater than analog circuitry power. Total regulator power dissipation is calculated using Equation 4-3.

EQUATION 4-3:

$$P_{DISS} = V_{IN} \times I_{IN} = V_{IN} \times (f_S \times Q_G + I_Q)$$

Where:

Q_G = total gate charge of all MOSFETs
f_S = switching frequency of each stage (500 kHz)
I_Q = controller quiescent current (non-switching supply current)

In some instances, power dissipation inside the control IC may limit the controller's maximum operating ambient temperature. An example is when the MIC2155 is powered from a 12V source and is driving 4 FETs. If each FET has a Q_G = 37 nC, the total power dissipation in the MIC2155 is derived approximately with Equation 4-4.

EQUATION 4-4:

$$P_{DISS} = 12V \times (37nc \times 4) \times 500kHz = 0.888W$$

The maximum operating ambient temperature is computed in Equation 4-5.

EQUATION 4-5:

$$T_{A(MAX)} = T_{J(MAX)} - P_{DISS} \times \theta_{JC}$$

$$T_{A(MAX)} = 125°C - 0.888W \times 50°C/W$$

$$T_{A(MAX)} = 81°C$$

Using an external LDO to supply VDD (as in Figure 4-5) can lower power dissipation in the controller and reduce junction temperature by supplying VDD externally. Using an external regulator, the power dissipated in the controller is reduced to the value as calculated in Equation 4-6.

EQUATION 4-6:

$$P_{DISS} = 5V \times (37nC \times 4) \times 500kHz = 0.37W$$

Careful selection and temperature rise calculations of the external LDO should be done to prevent an excessively high LDO junction temperature.

4.5 UVLO

Separate UVLO circuits monitor VIN1, VIN2 and VDD. Switching on Channel 1 is inhibited until the voltages on the VIN1 and VDD pins are greater than their respective UVLO thresholds. The gate drive on Channel 2 is inhibited until the VIN2 pin voltage exceeds its UVLO threshold.

Individual UVLO thresholds are necessary to allow proper operation from separate input supplies. The VIN1 threshold prevents the IC from switching if the input voltage is too low to properly source the VDD voltage. The VIN2 UVLO threshold is lower than VIN1 to allow operation from a low-voltage input.

Channel 1 switches and provides a regulated output voltage even if the VIN2 UVLO prevents Channel 2 from switching.

4.6 Power Good

The power good signal asserts high when the output voltage is greater than the power good threshold. The power good circuit compares a portion of the reference voltage to the voltage on the feedback pin. The output is an open drain FET as shown in Figure 4-7. To assert high, it must be pulled up to AVDD through a resistor.

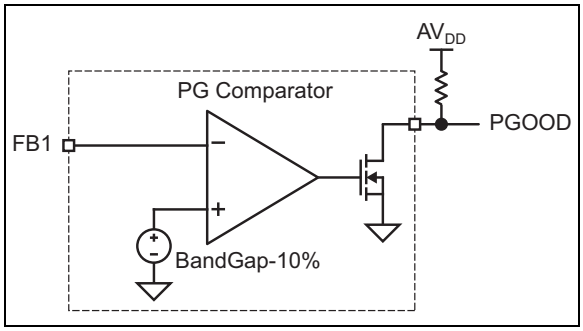


FIGURE 4-7: *Power Good.*

The power good signal may be connected to the enable pin of other power supplies and be used to sequence the other outputs.

4.7 Oscillator and Frequency Synchronization

The internal oscillator free runs at a fixed frequency and requires no external components. The oscillator generates two clock signals that are 180 degrees out of phase with each other. This forces each channel of the controller to switch 180 degrees out of phase, which reduces input and output ripple current.

The internal oscillator generates a clock signal and ramp signal. The clock signal terminates the switching cycle for each channel. The ramp voltage signal for Channel 1 is compared with the output of the Channel 1 error amplifier and regulates the output voltage. The ramp signal for Channel 2 is compared with the Channel 2 error amplifier output and forces the output current of Channel 2 to match that of Channel 1. See Figure 4-8.

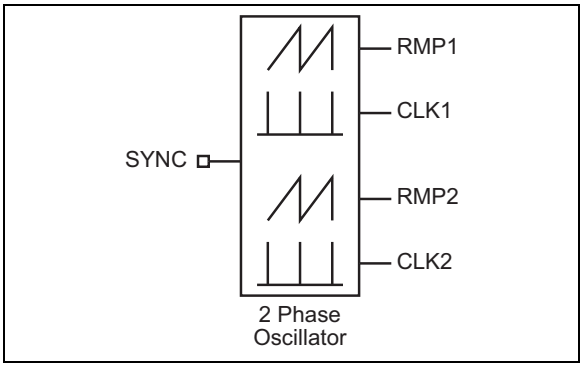


FIGURE 4-8: *Oscillator and Sync Diagram.*

The SYNC input (pin 15) allows the MIC2155 to synchronize to an external clock signal. When synchronized, each channel switches at half of the synchronization frequency. Limitations on the synchronization frequency and signal amplitude are listed in the **Section 1.0 "Electrical Characteristics"**. When not used, the sync pin should be left open (no connect).

4.8 MOSFET Gate-Drive Circuitry

The high-side drive circuit is designed to switch an N-channel MOSFET. Figure 4-9 shows a diagram of the gate drive and bootstrap circuit. D2 and C_{BST} comprise the bootstrap circuit, which is used to supply drive voltage to the high-side FET. Bootstrap capacitor C_{BST} is charged through diode D2 while the low-side MOSFET is on and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to charge the MOSFET gate, turning on the FET. As the MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. V_{CBST} floats up by VIN, diode D2 is reversed biased and V_{BST} is pulled high while continuing to keep the high-side MOSFET on. The high-side drive voltage, which is derived from V_{DD}, is approximately 4.5V due to the voltage drop across D2. When operating at 4.5V $V_{IN,}$ without connecting V_{DD} to V_{IN}, the gate drive voltage to the high-side FET could be as low as 3.2V. MOSFETs with an appropriate V_{GS} threshold should be used in this situation.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge vs. V_{GS}. Based on this information and a recommended ΔV_{CBST} of less than 0.1V, the minimum value of bootstrap capacitance is calculated as shown in Equation 4-7.

EQUATION 4-7:

$$C_{BST} \geq \frac{Q_{GATE}}{\Delta V_{CBST}}$$

Where:
Q_{GATE} = Total Gate Charge of high-side MOSFET
ΔV_{CBST} = Voltage Drop across the C_{BST} capacitor

A minimum value of 0.1 µF is required for each of the bootstrap capacitors, regardless of the MOSFETs being driven. Larger or paralleled MOSFETs may require larger capacitance values for proper operation. Placement is critical. The bootstrap capacitors (C_{BST}) for the BST supply pins must be located close between the BST and SW pins. The etch connections should be short, wide and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to **Section 4.23 "General Layout and Component Placement"** for more details.

A delay between the switching of the two MOSFETs is necessary to prevent both MOSFETs from being on at the same time and shorting V_{IN} to ground. An adaptive gate drive in the controller monitors the switch node (SW1) and low-side driver (LSD1) to minimize dead time while preventing both MOSFETs from being on at the same time. This enables the use of a broad range of MOSFETS without requiring excessive dead time.

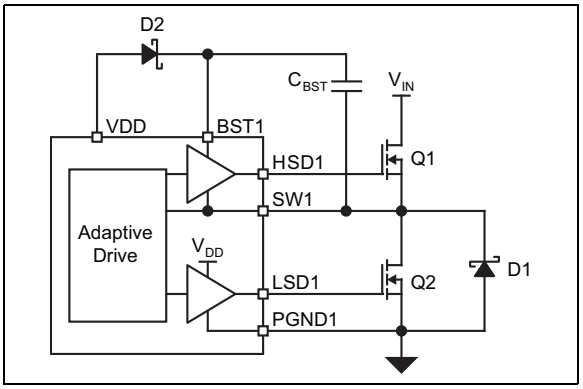


FIGURE 4-9: *Gate Drive.*

4.9 dv/dt-Induced Turn-On of the Low-Side MOSFET

As the high-side MOSFET turns on, the rising dv/dt on the switch-node forces current through C_{GD} of the low-side FET causing a glitch on the FET's gate. Figure 4-10 illustrates the basic mechanism causing this issue. If the glitch on the gate is greater than the FET's turn-on threshold, it may cause an unwanted turn-on of the low-side FET while the high-side FET is on. A short circuit between input and ground would occur. This condition lowers efficiency and increases power dissipation in both FETs. Additionally, turning on the low-side FET during the off-time could interfere with overcurrent sensing.

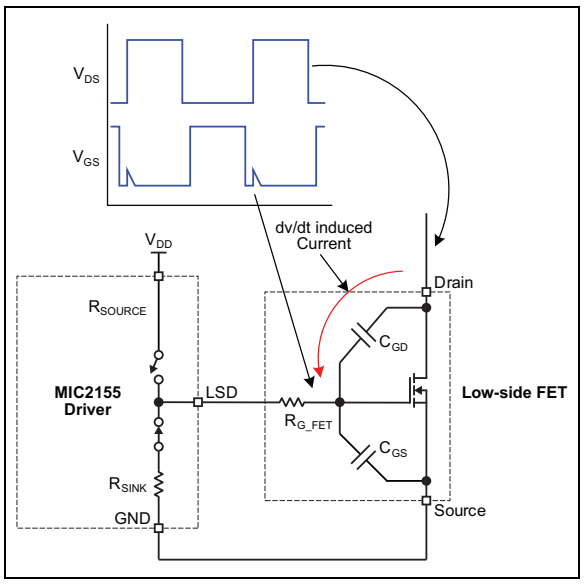


FIGURE 4-10: *dv/dt-Induced Turn-on.*

The following steps can be taken to lower the gate drive impedance, minimize the dv/dt-induced current, and lower the FETs susceptibility to the induced glitch:

1. Choose a low-side MOSFET with:
   - a high C_{GS}/C_{GD} ratio
   - a low internal gate resistance
2. Do not put a resistor between the LSD output and the gate of low-side MOSFET.
3. Ensure both the gate drive and return path PCB traces are short low-inductance connections.
4. Use a 4.5V V_{GS}-rated MOSFET because its higher gate threshold voltage is more immune to glitches than a 2.5V-rated or 3.3V-rated FET.
5. Connect V_{DD} to V_{IN} or a 5V supply if V_{IN} is below 6V. The R_{DSON} of the internal driver will be lower, and a 4.5V rated MOSFET can be used.

4.10 Remote Sense

Remote sensing provides accurate output voltage regulation by sensing at the load. Remote sensing makes up for losses in the power distribution path. It uses a unity gain differential amplifier to overcome voltage drops in both the output and return (ground) paths. The amplifier has a Common mode input range from –0.3V to 3.6V. For proper remote sense operation, V_{IN} must be greater than 6V. If V_{IN} is less than 6V, the V_{DD} pin must be connected to V_{IN} or externally supplied with 5V.

The output of the remote sense amplifier can source up to 500 µA. The voltage divider resistors (R1 and R4 in Figure 4-12) must be chosen to insure the output current of the amplifier does not exceed the maximum of 500 µA. See Equation 4-8.

EQUATION 4-8:

$$R1_{MAX} \geq \frac{V_{OUT} - V_{REF}}{500\,\mu A}$$

Where:
V_{REF} = 0.7V

A gain/phase plot of the remote sense amplifier in Figure 4-11 shows a typical 2 MHz bandwidth. Phase lag is 45 degrees at 1 MHz.

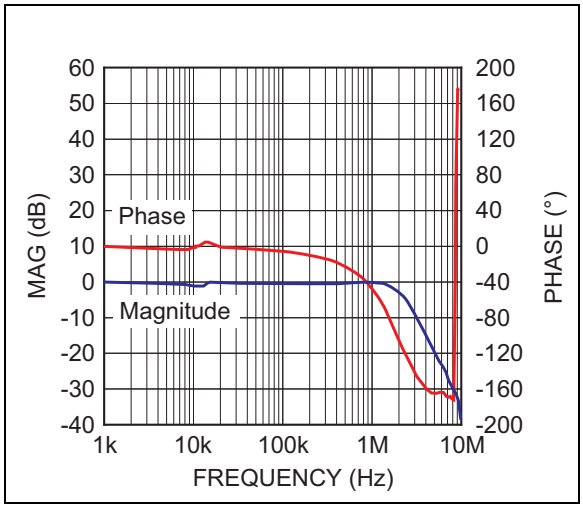


FIGURE 4-11: *Remote Sense Amplifier Gain/Phase Plot.*

A typical remote sense configuration is shown in Figure 4-12. The output of the remote sense amplifier feeds a voltage divider (R1, R4), which is connected to the Channel 1 error amplifier. The divider and compensation network for the remote sense are the same as for a local sense configuration. The 10Ω resistors provide an alternate feedback path if the remote sense connections are removed or opened. The remote sense connections should not be shorted. Otherwise the output voltage will increase close to V_{IN}. The OVP circuit in the controller does not protect against this type of fault when the feedback pin voltage is 0V.

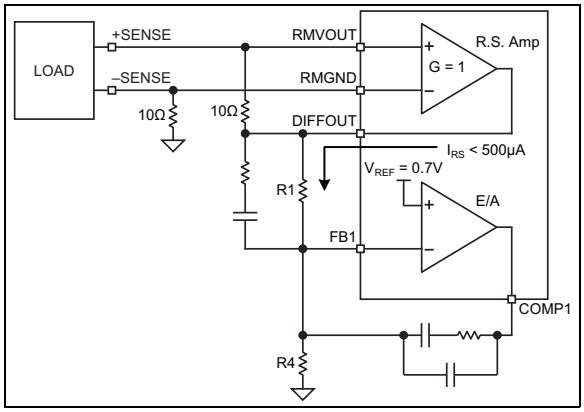


FIGURE 4-12: *Remote Sense.*

4.11 Setting the Output Voltage

Regardless of whether the remote sensing or local output voltage sensing is used, the output voltage is set with voltage divider resistors R1 and R4 (See Figure 4-12.). The equation below is used to calculate V_{OUT}.

EQUATION 4-9:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R4}\right)$$

Where:
V_{REF} = 0.7V

4.12 Current Limit and Overcurrent Protection

The MIC2155 uses the synchronous (low-side) MOSFETs R_{DSON} to sense an over current condition. The low-side MOSFET is used because it displays lower parasitic oscillations after switching than the high-side MOSFET. Additionally, it improves the accuracy and reduces false tripping at lower voltage outputs and narrow duty cycles since the off-time increases as duty cycle decreases. Figure 4-13 shows the overcurrent detection circuit.

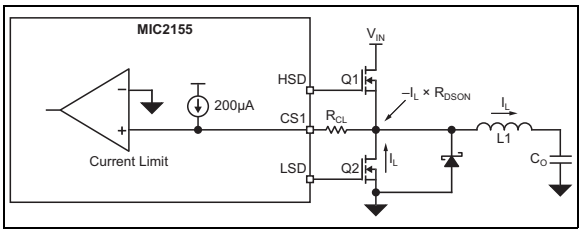


FIGURE 4-13: *Overcurrent Detection Circuit.*

Inductor current flows from the lower MOSFET source to the drain during off-time. The drain voltage becomes negative with respect to ground as the inductor current continues to flow from source to drain. This negative voltage is proportional to instantaneous inductor current times the low-side MOSFET R_{DSON}. The voltage across the low-side FET becomes even more negative as the output current increases. Figure 4-14 shows the inductor current and low-side FET V_{DS} waveforms.The overcurrent detection circuit operates by passing a known fixed current source (about 200 µA typical) through a resistor R_{CL}. This sets up an offset voltage (I_{CL} × R_{CL}) that is compared to the V_{DS} of the low-side FET. When source-to-drain voltage V_{SD} (I_L x R_{DSON}) is equal to this voltage, the MIC2155's over current trigger is set, which disables the next high-side gate drive pulse. After missing the high-side pulse, the overcurrent (OC) trigger is reset. If on the next low-side drive cycle, the current is still too high i.e. V_{CS1} is ≤ 0V, another high-side pulse is missed and so on. This effectively reduces the overall energy transferred to the output and V_{OUT} starts to fall.

The MIC2155 current limit circuit restricts the maximum peak inductor current. If the load tries to draw additional current, the output voltage drops until it is no longer within regulation limits. At this point, (75% of nominal output voltage) a Hiccup Current mode is initiated to protect downstream loads from excessive current during hard short circuits. This helps reduce the overall power dissipation in the PWM converter components during a fault.

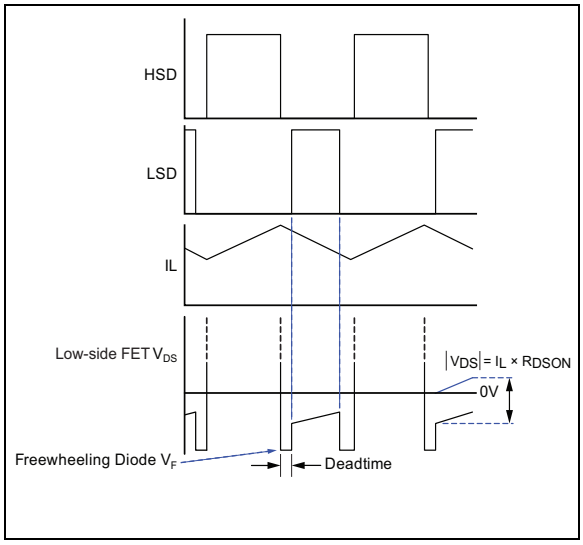


FIGURE 4-14: *Inductor Current and Low-Side FET V_{DS} Waveforms.*

The MIC2155 only senses current across the low-side MOSFET of Channel 1 since both channels operate in parallel. This means the total output current limit is approximately twice the calculated current limit.

4.13 Current Limit Setting

The current limit circuit responds to the peak inductor current flowing through the low-side FET. The value of R_{CL} can be estimated with a simple method or can be more accurately calculated by taking the inductor ripple current into account.

4.13.1 THE SIMPLE METHOD

The current limit setting resistor value can be quickly estimated with Equation 4-10.

EQUATION 4-10:

$$R_{CL} = \frac{I_{OUT(OC)} \times R_{DSON(MAX)}}{2 \times 180\mu A}$$

Where:

$I_{OUT(OC)}$ is the total output current limit at overcurrent.
R_{DSON} is the maximum on-resistance of the low-side FET at the operating junction temperature.

4.13.2 ACCURATE METHOD

For designs where ripple current is significant when compared to I_{OUT} or for low duty cycle operation, calculating the current setting resistor R_{CL} should take into account that we are sensing the peak inductor current and that there is a blanking delay of approximately 100 ns. See Figure 4-15.

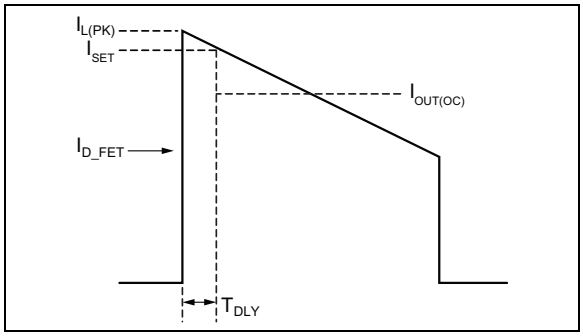


FIGURE 4-15: *Overcurrent Waveform.*

Equation 4-11, Equation 4-12, Equation 4-13 and Equation 4-14 are used to accurately calculate the current limit resistor value.

EQUATION 4-11:

$$I_{L(PK)} = \frac{I_{OUT(OC)}}{2} + \frac{I_{L(PP)}}{2}$$

Where:

$I_{L(PK)}$ = The peak inductor current in each phase
$I_{L(PP)}$ = The ripple inductor current in each phase

EQUATION 4-12:

$$I_{L(PP)} = \frac{V_{OUT} \times (1 - D)}{f_S \times L}$$

Where:
D = Duty cycle
f_S = Switching frequency
L = Power inductor value

EQUATION 4-13:

$$I_{SET} = I_{L(PK)} - \frac{V_{OUT} \times T_{DLY}}{L}$$

Where:
L = Power inductor value
T_{DLY} = Current limit blanking time about 100 ns

EQUATION 4-14:

$$R_{CL} = \frac{I_{SET} \times R_{DSON(MAX)}}{I_{CL(MIN)}}$$

Where:
I_{SET} = Overcurrent setpoint
$I_{CL(MIN)}$ = Minimum overcurrent trip point program current

EQUATION 4-15:

$$D = \frac{V_{OUT}}{V_{IN} \times Efficiency}$$

4.13.3 EXAMPLE

Consider a 12V-to-3.3V converter at a 30A total output current limit with 1.5 µH power inductor and 90% efficiency at full load. Each channel will supply 15A at a 500 kHz switching frequency. The on-resistance of the low side MOSFET is 6 mΩ.

Equation 4-16 shows how to use the simple method and Equation 4-17 illustrates the accurate method.

EQUATION 4-16:

$$R_{CL} = \frac{\frac{30A}{2} \times 6m\Omega}{180\mu A} = 500\Omega$$

EQUATION 4-17:

$$D = \frac{3.3V}{12V \times 0.9} = 0.3$$

$$I_{L(PP)} = \frac{3.3V \times (1 - 0.3)}{500kHz \times 1.5\mu H} = 3.1A$$

$$I_{L(PK)} = \frac{30A}{2} + \frac{3.1A}{2} = 16.55A$$

$$I_{SET} = 16.55A - \frac{3.3V \times 100ns}{1.5\mu H} = 16.33A$$

$$R_{CL} = \frac{16.33A \times 6m\Omega}{180\mu A} = 544\Omega$$

Using the simple method here would result in a current limit point lower than expected.

This equation sets the target maximum current limit point per channel of the converter, but the actual maximum value will depend on the actual inductor value, actual I_{CL} and on resistance of the MOSFET under current limit conditions. This could be in the region of 50% higher and should be considered to ensure that all the power components are within their thermal limits unless thermal protection is implemented separately.

4.14 Inductor Current Sensing

Current sharing between the two phases is achieved by sensing the inductor current in each phase. Lossless inductor current sensing is used, which has the advantages of lower power loss and lower cost —over using a discrete resistor in series with the inductor.

The inductor current sense circuit is shown in Figure 4-16. It extracts the voltage drop across the inductor's DC winding resistance.

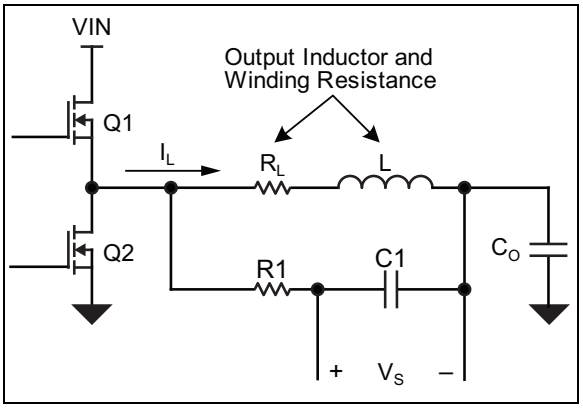


FIGURE 4-16: *Lossless Inductor Current Sense.*

The voltage across capacitor C1 is computed with Equation 4-18.

EQUATION 4-18:

$$V_S = I_L \times \left(R_L \times \frac{\frac{sL}{R_L} + 1}{sC1 \times R1 + 1} \right)$$

If the R1 × C1 time constant is equal to the L/R_L time constant, the voltage across capacitor C1 equals the $R_L \times I_L$. Figure 4-17 is a plot of this equation and shows the results graphically. It assumes an inductance of 1.5 µH, R_L = 0.01Ω, C1 = 0.1 µF, and R1 =1.5k. The time constants are equal and diverge at the same rate. The overall impedance, H(s), equals R_L for all frequencies.

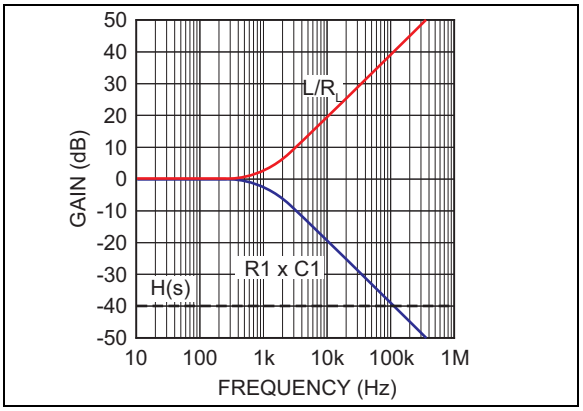


FIGURE 4-17: *Current Sense Gain/Phase Plot.*

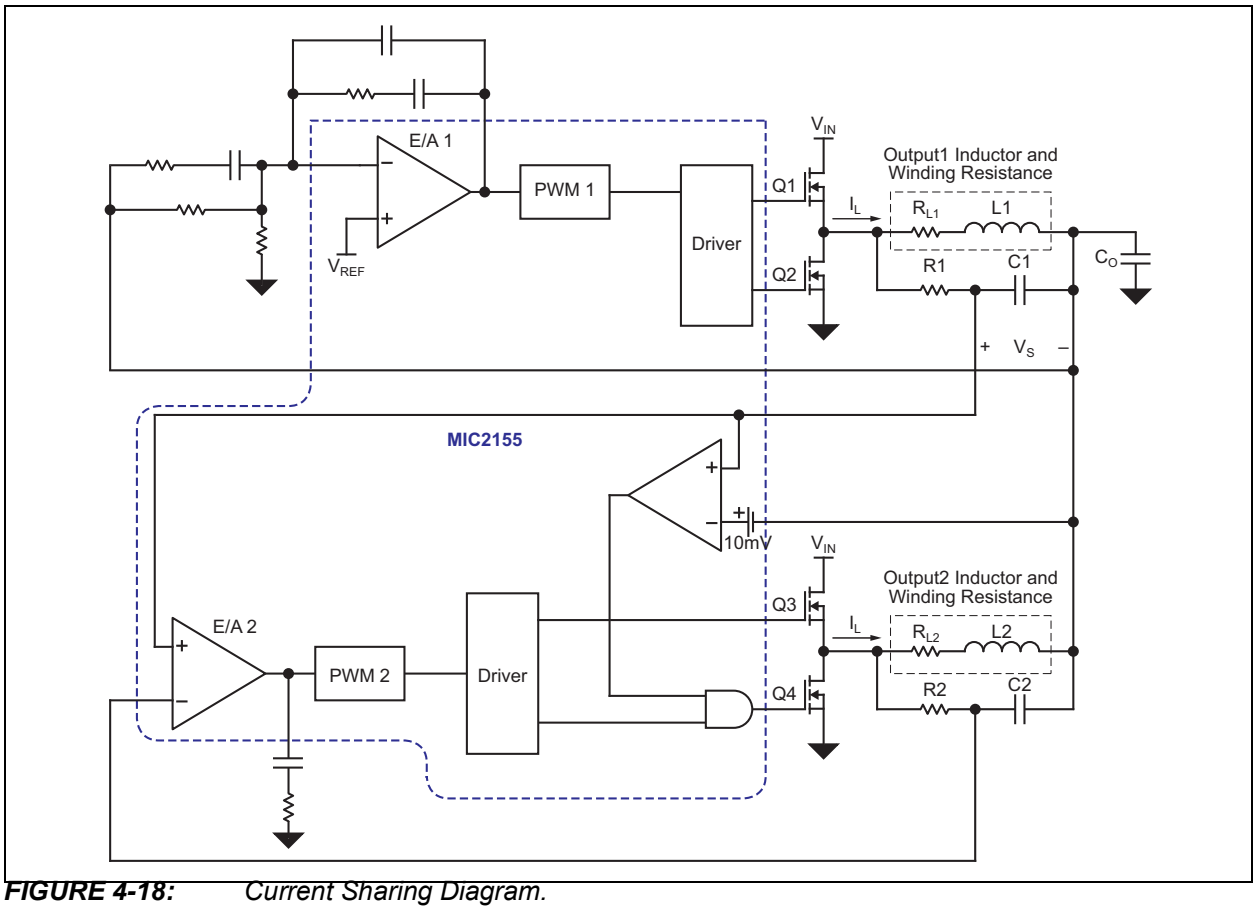


FIGURE 4-18: *Current Sharing Diagram.*

4.15 Current Sharing

The schematic in Figure 4-18 illustrates the current sharing scheme. The error amplifier in Channel 1, E/A 1, monitors the output voltage and adjusts the duty cycle of Channel 1 to regulate that voltage. The inputs of transconductance error amplifier, E/A 2, are connected to the current sense points of each channel. The error amplifier 2 regulates Channel 2 current by monitoring and making reference to the current sense point of Channel 1 and forcing the current sense point of Channel 2 to be equal.

Any offset or difference in current between the two channels is caused by tolerances in the inductance, DCR, and tolerances of R1, C1, R2 and C2. Additionally, voltage offset in E/A 2 may cause variations in output current sharing. At lower currents, these variations may force the current of Channel 2 to be 0.

A nominal 10 mV offset inhibits the Channel 2 low-side MOSFET until the output current increases to the magnitude where the voltage across C1 is 10 mV. This prevents the low-side MOSFET of Channel 2 from sinking current to ground during startup or during low current operation.

4.16 Startup into a Pre-Biased Output

Soft-start circuitry in a conventional synchronous buck regulator forces the regulator to start up by initially operating at a minimum duty cycle and gradually increasing the duty cycle until the output voltage reaches regulation. In a synchronous buck power supply, a narrow duty cycle means the low-side MOSFET is on for most of the switching period. If the output voltage is not 0V, the wide on time of the low-side MOSFET may discharge the output and cause high reverse current to flow in the inductor.

The MIC2155 is designed to turn on into a pre-biased output without discharging the output. Circuitry in the controller monitors the input and output voltage and forces the soft-start circuit to initially operate at the proper duty cycle. This allows the output to turn on in a controlled fashion without discharging the output. The minimum output voltage for proper operation of the pre-bias startup circuitry is 0.6V. If V_{OUT} is less than 0.6V, a partial discharge of V_{OUT} may occur.

4.17 Separate Input Supplies

The MIC2155 can operate from two input supplies with different voltages. Each of the two channels can have a different input voltage and still share current. This allows the buck converter supply input to draw power from more than one supply source.

The controller will force the output currents of the two channels to be equal. Since the output voltage and currents of the two channels are the same, the input power drawn from each supply will approximately be the same. The input currents will be inversely proportional to the input voltages of each of the two supplies. For example, if the total output power is 50W and efficiency is 91%, the total input power from both supplies is calculated based on Equation 4-19.

EQUATION 4-19:

$$P_{IN1} = \frac{P_{OUT}}{\eta} = \frac{50W}{0.91} = 55W$$

Each supply contributes approximately half the power. See Equation 4-20.

EQUATION 4-20:

$$P_{IN1} = P_{IN2} = 27.5W$$

For V_{IN1} = 12V and V_{IN2} = 3.3V, the following formula in Equation 4-21 are used.

EQUATION 4-21:

$$I_{IN1} = \frac{P_{IN1}}{V_{IN1}} = \frac{27.5W}{12V} = 2.3A$$

$$I_{IN2} = \frac{P_{IN2}}{V_{IN2}} = \frac{27.5W}{3.3V} = 8.3A$$

4.18 Component Selection, Guidelines and Design Example

The following section outlines a procedure for designing a two-phase synchronous buck converter using the MIC2155.

This example will use the following parameters:

V_{IN} = 12V
V_{OUT} = 1.8V
I_{OUT} = 30A

Switching frequency (f_S) = 500 kHz/channel

4.18.1 OUTPUT FILTER SELECTION

The output filter is comprised of the output capacitors and the output inductors. The filter is designed to attenuate the output voltage ripple to the desired value. The output filter components also determine how well the buck converter responds to output load current transients. If output transients are significant, the output capacitors should be chosen first to meet the transient specification. The output inductor is then selected to insure the filter attenuates the output ripple to meet the specification.

A second commonly used method of designing the filter is to select the inductor value to keep the ripple current between 20% and 30% of the full load output current for that channel. Then select the output capacitance to meet the output voltage ripple specification and output current transient specification.

Values for inductance, peak and RMS inductor currents are required to choose the output inductors. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Output capacitor selection requires information of transient current, RMS capacitor current and output voltage.

There are several tradeoffs to be made when selecting the output inductor. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger size and more expensive inductor.

Higher switching frequencies allow the use of a small inductance but increase power dissipation in the inductor core and MOSFET switching loss. The MIC2155 switches at 500 kHz/channel and is designed to use a smaller inductor at the expense of higher switching losses and slightly lower efficiency.

The peak output ripple current for a two-phase converter is shown in Figure 4-19. The graph shows that peak ripple current is a function of duty cycle. Since each channel is 180 degrees out of phase with the other, at 50% duty cycle, the output ripple currents from each channel cancel, and the output ripple current is close to zero.

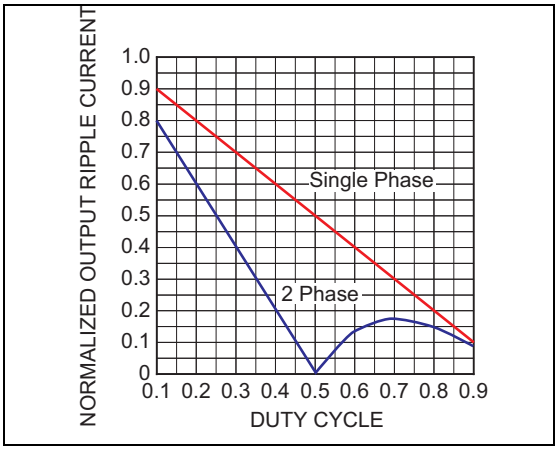


FIGURE 4-19: *Phase Output Ripple Current vs. Duty Cycle.*

For this example, with V_{IN} = 12V, V_{OUT} = 1.8V and efficiency = 88%, the duty cycle is computed as shown in Equation 4-22.

EQUATION 4-22:

$$D = \frac{V_{OUT}}{\eta \times V_{IN}} = \frac{1.8V}{0.88 \times 12V} = 0.17$$

Figure 4-19 shows the peak-to-peak output ripple current normalized by the maximum value, which is indicated in Equation 4-23.

EQUATION 4-23:

$$I_{OPP(MAX)} = \frac{V_{OUT}}{f_S \times L}$$

The two-phase peak-to-peak output ripple current is less than that for a single-phase conversion. If V_{IN} varies, the input voltage that generated the highest ripple current should be used for the calculation.

For this example, assume the output transient loading is small, and the filter design is based on output ripple voltage requirement.

The inductance value is calculated by Equation 4-24.

EQUATION 4-24:

$$L = \frac{V_{OUT} \times (\eta \times V_{IN(MAX)} - V_{OUT})}{\eta \times V_{IN(MAX)} \times f_S \times 0.2 \times I_{O1(MAX)}}$$

Where:

f_S = the switching frequency per channel
0.2 = the ratio of AC ripple current to DC maximum output current of each phase channel
$V_{IN(MAX)}$ = the maximum input voltage
$I_{O1(MAX)}$ is the DC maximum output current per channel or ½ of the maximum total output current ($I_{OUT(MAX)}$)
η is the converter's efficiency

A computation for this example is shown in Equation 4-25.

EQUATION 4-25:

$$L = \frac{1.8V \times (0.88 \times 12V - 1.8V)}{0.88 \times 12V \times 500kHz \times 0.2 \times 15A} = 1\mu H$$

The peak-to-peak ripple current for each channel is calculated with Equation 4-26.

EQUATION 4-26:

$$I_{L(PP)} = \frac{V_{OUT} \times (\eta \times V_{IN(MAX)} - V_{OUT})}{\eta \times V_{IN(MAX)} \times f_S \times L}$$

$$I_{L(PP)} = \frac{1.8V \times (0.88 \times 12V - 1.8V)}{0.88 \times 12V \times 500kHz \times 1\mu H} = 3A$$

The output capacitors see less ripple current than each channel because they are out of phase.

The calculation of the peak-to-peak output ripple current normalizing factor is shown in Equation 4-27.

EQUATION 4-27:

$$I_{OPP(MAX)} = \frac{V_{OUT}}{f_S \times L} = \frac{1.8V}{500kHz \times 1\mu H} = 3.6$$

The approximate output ripple current in the two-phase configuration at 17% duty cycle is determined from the graph in Equation 4-19 and can be computed with Equation 4-28.

EQUATION 4-28:

$$I_{OPP} = 0.65 \times \frac{V_{OUT}}{f_S \times L} = 0.65 \times \frac{1.8V}{500kHz \times 1\mu H} = 2.3A$$

For the input and output voltage in this application, going to a two-phase design decreases the total output ripple current from 3 A_{PP} to 2.3 A_{PP}.

The peak inductor current in each channel is equal to the average maximum output current per channel plus one half of the peak-to -peak inductor ripple current. Refer to Equation 4-29.

EQUATION 4-29:

$$I_{L(PK)} = I_{O1(MAX)} + 0.5 \times I_{L(PP)} = 15A + 0.5 \times 3A = 16.5A$$

The RMS inductor current is used to calculate the $I^2 \times R$ losses in the inductor as shown in Equation 4-30.

EQUATION 4-30:

$$I_{L(RMS)} = I_{O1(MAX)} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{I_{L(PP)}}{I_{O1(MAX)}}\right)^2}$$

$$I_{L(RMS)} = 15A \times \sqrt{1 + \frac{1}{12} \times \left(\frac{3A}{15A}\right)^2} = 15.02A$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC2155 requires the use of ferrite materials for all but the most cost-sensitive applications. Lower-cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the buck converter. This is

especially noticeable at low output power. The inductor winding resistance decreases efficiency more significantly at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor size.

The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor.

For this example, a Cooper HCF1305-1R0 inductor was chosen. Core loss for this application was taken from the data sheet and is 15 mW. Winding resistance is 1.9 mΩ.

Copper loss in the inductor is calculated with Equation 4-31.

EQUATION 4-31:

$$P_{L(Cu)} = (I_{L(RMS)})^2 \times R_{WINDING}$$
$$= (15.02A)^2 \times 1.9m\Omega = 0.43W$$

The resistance of the copper wire, $R_{WINDING}$, increases with temperature. If so desired, a more accurate calculation can be made if the maximum ambient temperature and temperature rise of the inductor is known. The value of the winding resistance at operating temperature is calculated with Equation 4-32.

EQUATION 4-32:

$$R_{WINDING(HT)} = R_{WINDING(20)} \times (1 + 0.0042 \times (Temp_{HT} - T_{20}))$$

Where:

$Temp_{HT}$ = the temperature of the wire under operating load
T_{20} = ambient room temperature
$R_{WINDING(20)}$ = the resistance of the winding at room temperature, usually specified by the manufacturer

For this example, the approximate power dissipation is 0.43W. From the manufacturer's data sheet, this causes a 20°C rise in inductor temperature. Assuming ambient temperature stayed at 20°C, the maximum winding resistance would be increased from 1.9 mΩ to the value calculated with Equation 4-33.

EQUATION 4-33:

$$R_{WINDING(HT)} = 1.9m\Omega \times (1 + 0.0042 \times (40°C - 20°C)) = 2.06m\Omega$$

4.18.2 OUTPUT CAPACITOR SELECTION

In this example, the output capacitors are chosen to keep the output voltage ripple below a specified value. The output ripple voltage is determined by the capacitors' ESR (equivalent series resistance) and capacitance. Voltage rating and RMS current capability are two other important factors in selecting the output capacitors.

Ceramic output capacitors and most polymer capacitors have very low ESR and are recommended for use with the MIC2155. The output capacitance is usually the primary cause of output ripple in ceramic and very low ESR capacitors. The minimum value of C_{OUT} is calculated in Equation 4-34.

EQUATION 4-34:

$$C_{OUT} \geq \frac{I_{OPP}}{8 \times \Delta V_{OPP} \times 2 \times f_S}$$

Where:

ΔV_{OPP} = peak-to-peak output voltage ripple in Steady state
I_{OPP} = peak-to-peak ripple current as see by the capacitors
f_S = per channel switching frequency

Notice the calculation is performed at 2x the switching frequency since the capacitors see ripple current from both phases.

For the example illustrated in Equation 4-35 using ΔV_{OPP} = 10 mV, the minimum C_{OUT} is:

EQUATION 4-35:

$$C_{OUT} \geq \frac{2.3A}{8 \times 10mV \times 2 \times 500kHz} = 29\mu F$$

A capacitance at this low value is usually not used in high current converters because of transient output current requirements.

For load transient requirement consideration, the output voltage drop due to the load transient current step is mainly contributed by the output capacitance discharge to support the load current step. The required output capacitance can be estimated with Equation 4-36.

EQUATION 4-36:

$$C_{OUT} > \frac{\Delta I_{LOAD} \times t_{RES}}{\Delta V_{OUT(LDT)}}$$

Where:

ΔI_{LOAD} = Load transient current step
t_{RES} = Load transient response time
$\Delta V_{OUT(LDT)}$ = Output voltage drop due to the load step

For this example, 500 µF total capacitance is used. It is split up into four 47 µF ceramic capacitors and two 150 µF aluminum polymer capacitors connected in parallel.

The total output ripple is a combination of ripple voltages due to the ESR and the output capacitance. The steady-state total output ripple voltage is calculated in Equation 4-37.

EQUATION 4-37:

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{OPP}}{8 \times C_{OUT} \times 2 \times f_S}\right)^2 + (I_{OPP} \times ESR_{COUT})^2}$$

To increase reliability, the recommended voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for an aluminum electrolytic or ceramic.

The output capacitor RMS current is computed in Equation 4-38.

EQUATION 4-38:

$$I_{COUT(RMS)} = \frac{I_{OPP}}{\sqrt{12}} = \frac{2.3A}{\sqrt{12}} = 0.66A$$

The power dissipated in the output capacitors can be calculated with Equation 4-39.

EQUATION 4-39:

$$P_{DISS(COUT)} = (I_{COUT(RMS)})^2 \times ESR_{COUT}$$

4.18.3 INDUCTOR CURRENT SENSE COMPONENTS

The RC circuit values that sense current across the inductor can be calculated once the inductor is selected. The circuit is shown in Figure 4-20.

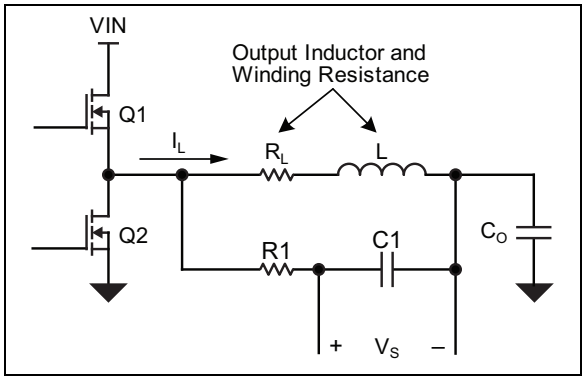


FIGURE 4-20: *Inductor Current Sense.*

For this example, the inductor has the following parametric values:

L = 1 µH

R_L = 1.9 mΩ

Proper sensing of the DC voltage across the inductor requires the L/R_L time constant be equal to the R1 × C1 time constant as shown in Equation 4-40.

EQUATION 4-40:

$$\frac{L}{R_L} = C1 \times R1$$

A good range of values for C1 is 0.1 µF to 1 µF. For this example, C1 is chosen as 0.22 µF. R1 is shown in Equation 4-41.

EQUATION 4-41:

$$R1 = \frac{L}{R_L \times C1} = \frac{1\mu H}{1.9m\Omega \times 0.22\mu F} = 2.39k\Omega$$

4.18.4 INPUT CAPACITOR SELECTION

In addition to high-frequency ceramic capacitors, a larger bulk capacitance, either ceramic or aluminum electrolytic should be used to help attenuate ripple on the input and to supply current to the input during large output current transients. The input capacitors must be rated for the RMS input current of the buck converter. RMS input capacitor current is determined by the maximum output current. The graph in Figure 4-21 shows the normalized RMS input ripple current vs. duty cycle. Data is normalized to the output current.

For a two-phase converter operating at 17% duty cycle, the input RMS current is determined at the graph in Figure 4-21 and can be approximated by Equation 4-42.

EQUATION 4-42:

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times 0.24 = 30A \times 0.24 = 7.2A$$

The power dissipated in the input capacitor is indicated in Equation 4-43.

EQUATION 4-43:

$$P_{DISS(CIN)} = (I_{CIN(RMS)})^2 \times ESR_{CIN}$$

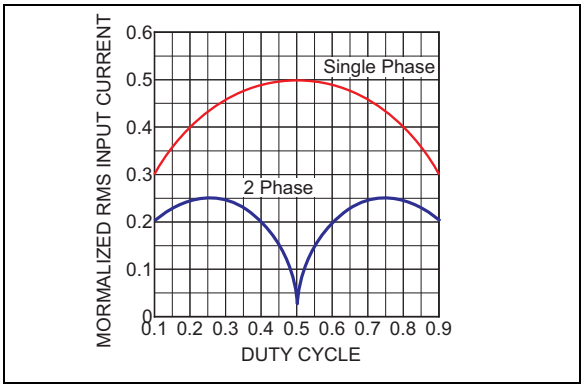


FIGURE 4-21: *RMS Input Current vs. Duty Cycle.*

4.18.5 MOSFET SELECTION

External N-channel logic-level power MOSFETs must be used for the high-side and low-side switches. The MOSFET gate-to-source drive voltage from the MIC2155 is regulated by an internal 5V V_{DD} regulator. Logic level MOSFETs, whose operation is specified at V_{GS} = 4.5V must be used. The MOSFET on-resistance R_{DSON} is used to calculate the losses during the MOSFET's conduction time. If operating at 4.5 V_{IN}, without connecting V_{DD} to V_{IN}, the gate drive voltage to the high-side FET could be as low as 3.2V. MOSFETs with low V_{GS} enhanced gates should be used in this situation.

It is important to note the on-resistance of a MOSFET increases at high junction temperature. A 75°C rise in junction temperature increases the channel resistance of the MOSFET by 40% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation.

Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2155 gate drive circuit. Gate charge can be a significant source of power dissipation in the controller due to the high switching frequencies and generally large MOSFETs that are driven. At low output load this power dissipation is noticeable as a reduction in efficiency.

The average current required to drive the MOSFETs is shown in Equation 4-44.

EQUATION 4-44:

$$I_{DD} = Q_G \times f_S$$

Where:

Q_G is the total gate charge for all high-side and low-side MOSFETs. This information should be obtained from the manufacturer's data sheet with a 5V V_{GS}.

Since the current from the gate drive comes from the input voltage, the power dissipated in the MIC2155 due to gate drive is shown in Equation 4-45.

EQUATION 4-45:

$$P_{GATEDRIVE} = Q_G \times f_S \times V_{IN}$$

A convenient figure of merit for switching MOSFETs is the on-resistance times the total gate charge ($R_{DSON} \times Q_G$). Lower numbers translate into higher efficiency. Low-gate-charge logic-level MOSFETs are a good choice for use with the MIC2155. The internal LDO that supplies V_{DD} is rated for 75 mA. Exceeding this value could damage the regulator or cause excessive power dissipation in the IC. Refer to **Section 4.4 "Supply Voltages and Internal Regulator"** of this for additional information.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On resistance
- Total gate charge

The V_{DS} voltage rating of the MOSFETs is essentially equal to the input voltage. A safety factor of 20% should be added to the $V_{DS(max)}$ of the MOSFETs to account for voltage spikes due to circuit parasitics.

The power dissipated in the switching transistor is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses that occur during the transition times when the MOSFET is turning on and off (P_{AC}). Refer to Equation 4-46 for the calculation of the power dissipation in MOSFET switch.

EQUATION 4-46:

$$P_{DISS(SW)} = P_{CONDUCTION} + P_{AC}$$

Where:

$P_{CONDUCTION} = (I_{SW(RMS)})^2 \times R_{DSON}$
$P_{AC} = P_{AC(ON)} + P_{AC(OFF)}$
R_{DSON} is the on resistance of the MOSFET switch.

Making the assumption that the turn-on and turn-off transition times are equal, the total AC switching loss of the MOSFET switch is calculated based on Equation 4-47.

EQUATION 4-47:

$$P_{AC} = (V_{IN} + V_D) \times I_L \times t_T \times f_S$$

Where:

V_D = freewheeling diode forward voltage
I_L = average inductor current (half I_{OUT})
t_T = the switching transition time (typically 15 ns to 30 ns)
f_S = the switching frequency of each phase

4.18.6 RMS CURRENT AND MOSFET POWER DISSIPATION CALCULATION

Under normal operation, the high-side MOSFET's RMS current is greatest when V_{IN} is low (maximum duty cycle). The low-side MOSFET's RMS current is greatest when V_{IN} is high (minimum duty cycle). However, the MOSFET sees maximum stress during short-circuit conditions, where the output current is equal to the maximum overcurrent level. The calculations below are for normal operation. To calculate the stress under short-circuit conditions, substitute the total output current at overcurrent level ($I_{OUT(OC)}$) for $I_{OUT(max)}$.

The RMS value of the high-side switch current and low-side switch current is computed as shown in Equation 4-48 and Equation 4-49.

EQUATION 4-48:

$$I_{SWHS(RMS)} = \sqrt{D} \times \sqrt{\left(\frac{I_{OUT(MAX)}^2}{4} + \frac{I_{L(PP)}^2}{12}\right)}$$

Where:

$I_{OUT(MAX)}$ = Total maximum output current at normal operation
D = the duty cycle of the converter $D = \frac{V_{OUT}}{\eta \times V_{IN}}$
$I_{L(PP)}$ = the individual inductor ripple current
η = is the efficiency of the converter

EQUATION 4-49:

$$I_{SWLS(RMS)} = \sqrt{(1-D)} \times \sqrt{\left(\frac{I_{OUT(MAX)}^2}{4} + \frac{I_{L(PP)}^2}{12}\right)}$$

Where:

$I_{OUT(MAX)}$ = Total maximum output current at normal operation
D = the duty cycle of the converter $D = \frac{V_{OUT}}{\eta \times V_{IN}}$
$I_{L(PP)}$ = the individual inductor ripple current
η = is the efficiency of the converter

Converter efficiency also depends on other component parameters that have not yet been selected. For design purposes, an efficiency estimate of 85% to 90% can be used. The efficiency can be more accurately calculated once the design is complete. If the assumed efficiency is grossly inaccurate, a second iteration through the design procedure should be made.

For the high-side switch, the maximum DC power dissipation is calculated with Equation 4-50.

EQUATION 4-50:

$$P_{SWHS(DC)} = R_{DSON(HS)} \times (I_{SWHS(RMS)})^2$$

The AC switching loss for each of the high-side MOSFETs is computed in Equation 4-51.

EQUATION 4-51:

$$P_{AC} = (V_{IN} + V_D) \times I_{OUT(MAX)} \times 0.5 \times t_T \times f_S$$

The total power dissipation for each high-side MOSFET is calculated based on Equation 4-52.

EQUATION 4-52:

$$P_{DISS(SWHS)} = P_{SWHS(DC)} + P_{AC}$$

For each low-side MOSFET switch, the total power dissipation is mainly DC power dissipation only, and the AC switching loss is very small and usually can be neglected. It is because the freewheeling diode across the low-side MOSFET turns on first during the switching transition times and the voltage across the low-side MOSFET is small during its turn-on and turn-off transitions. Therefore, the power dissipation of each low-side MOSFET can be approximated by Equation 4-53.

EQUATION 4-53:

$$P_{DISS(SWLS)} \approx P_{SWLS(DC)} = (I_{SWLS(RMS)})^2 \times R_{DSON(LS)}$$

4.18.7 EXTERNAL SCHOTTKY DIODE

A freewheeling diode in parallel with the low-side FET is needed to keep the inductor current flow continuous while both MOSFETs are turned off (dead time). Dead time is necessary to prevent current from flowing unimpeded through both MOSFETs. An external Schottky diode is not necessary for circuit operation since the low-side MOSFET contains a parasitic body diode. An external diode will improve efficiency due to its lower forward voltage drop as compared to the internal parasitic diode in the FET. It may also decrease high-frequency noise because the Schottky diode junction does not suffer from reverse recovery.

If the MOSFET body diode is used, it must be rated to handle the peak and average current. The body diode may have a relatively slow reverse recovery time and a relatively high forward voltage drop. The power lost in the diode is proportional to the forward voltage drop of the diode. As the high-side MOSFET starts to turn on, the body diode becomes a short circuit for the reverse recovery period, dissipating additional power. The diode recovery and the circuit inductance will cause ringing during the high-side MOSFET turn on. If the internal FET diode is used, power dissipated during the dead time should be added to the P_{DISS} of the low-side MOSFET.

An external Schottky diode conducts at a lower forward voltage, preventing the body diode in the MOSFET from turning on. The lower forward voltage drop dissipates less power than the body diode. The lack of a reverse recovery mechanism in a Schottky diode causes less ringing and power loss. Depending on the circuit components and operating conditions, an external Schottky diode may give a ½% to 1% improvement in efficiency.

The average diode forward current is calculated in Equation 4-54.

EQUATION 4-54:

$$I_{D(AVG)} = I_{OUT(MAX)} \times t_{DT} \times f_S$$

Where:
t_{DT} = the dead time when both MOSFETs are off

The reverse voltage requirement of the diode is calculated based as shown in Equation 4-55.

EQUATION 4-55:

$$V_{DIODE(RRM)} = V_{IN}$$

The power dissipated by the diode is computed based on Figure 4-56.

EQUATION 4-56:

$$P_{DIODE} = I_{D(AVG)} \times V_F$$

Where:
V_F = the forward voltage at the peak diode current

4.18.8 SNUBBER DESIGN

A snubber is used to damp out high-frequency ringing caused by parasitic inductance and capacitance in the buck converter circuit. A snubber is needed for each of the two phases in the converter. Figure 4-22 shows a simplified schematic of one of the buck converter phases. Stray capacitance consists mostly of the two MOSFET's output capacitance (C_{OSS}). The stray inductance is mostly package and etch inductance. The arrows show the resonant current path when the high-side MOSFET turns on. This ringing causes stress on the semiconductors in the circuit as well as increased EMI.

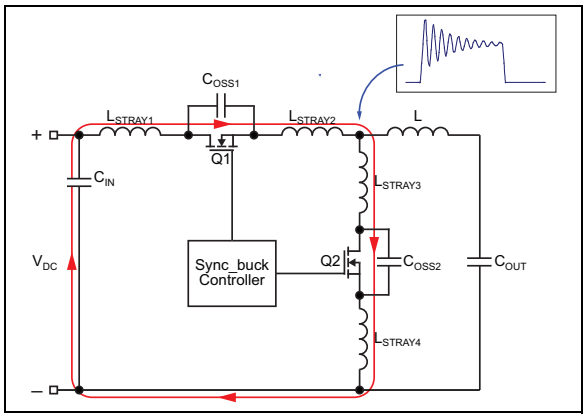


FIGURE 4-22: *Output Parasitics.*

One method of reducing the ringing is to use a resistor and capacitor to lower the Q of the resonant circuit. The circuit in Figure 4-23 shows the resistor in between the switch node and ground. Capacitor, Cs, is used to block DC and minimize the power dissipation in the resistor. This capacitor value should be between 5 and 10 times the parasitic capacitance of the MOSFET C_{OSS}. A capacitor that is too small will have high impedance and prevent the resistor from damping the ringing. A capacitor that is too large causes unnecessary power dissipation in the resistor, which lowers efficiency.

The snubber components should be placed as close as possible to the low-side MOSFET and/or external Schottky diode since it contributes to most of the stray capacitance. Placing the snubber too far from the FET or using etch that is too long or thin will add inductance to the snubber and diminishes its effectiveness.

A proper snubber design requires the parasitic inductance and capacitance be known. A method of determining these values and calculating the damping resistor value is outlined below.

1. Measure the ringing frequency at the switch node which is determined by parasitic L_P and C_P. Define this frequency as f_1.

2. Add a capacitor C_S (normally at least 3 times as big as the C_{OSS} of the FET) from the switch node to ground and measure the new ringing frequency. Define this new (lower) frequency as f_2. L_P and C_P can now be solved using the values of f_1, f_2 and C_S.

3. Add a resistor R_S in series with C_S to generate critical damping.

Step 1: First measure the ringing frequency on the switch node voltage when the high-side MOSFET turns on. This ringing is characterized by Equation 4-57.

EQUATION 4-57:

$$f_1 = \frac{1}{2\pi \times \sqrt{L_P \times C_P}}$$

Where:
C_P and L_P are the parasitic capacitance and inductance.

Step 2: Add a capacitor, C_S, in parallel with the synchronous MOSFET, Q2. The capacitor value should be approximately 3 times the C_{OSS} of Q2. Measure the new ringing frequency f_2 at the switch node. This ringing frequency is characterized by Equation 4-58.

EQUATION 4-58:

$$f_2 = \frac{1}{2\pi \times \sqrt{L_P \times (C_S + C_P)}}$$

f' is defined as shown in Equation 4-59.

EQUATION 4-59:

$$f' = \frac{f_1}{f_2}$$

Combining the equations for f_1, f_2 and f' to derive C_P, the parasitic capacitance is show in Equation 4-60.

EQUATION 4-60:

$$C_P = \frac{C_S}{(f')^2 - 1}$$

L_P is solved by re-arranging the equation for f_1 as shown in Equation 4-61.

EQUATION 4-61:

$$L_P = \frac{1}{(2\pi)^2 \times C_P \times (f_1)^2}$$

Step 3: Calculate the damping resistor. Critical damping occurs at Q = 1 as illustrated in Equation 4-62.

EQUATION 4-62:

$$Q = R_S \times \sqrt{\frac{C_P + C_S}{L_P}}$$

The solution for R_S is shown in Equation 4-63.

EQUATION 4-63:

$$R_S = \sqrt{\frac{L_P}{C_P + C_S}}$$

Figure 4-23 shows the snubber in the circuit and the damped switch node waveform.

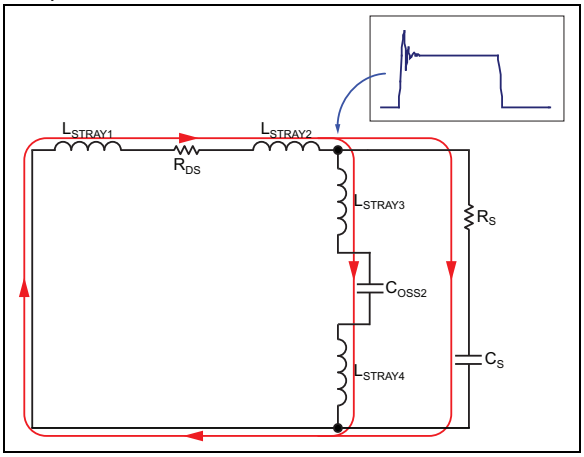


FIGURE 4-23: *Snubber Circuit.*

The snubber capacitor, C_S, is charged and discharged each switching cycle. The energy stored in C_S is dissipated by the snubber resistor, R_S, two times per switching period. This power is calculated in Equation 4-64.

EQUATION 4-64:

$$P_{SNUBBER} = f_S \times C_S \times V_{IN}^2$$

Where:
f_S = the switching frequency for each phase
V_{IN} = the DC input voltage

4.19 Compensation of the Output Voltage Loop

The voltage regulation, filter, and power stage sections are shown in Figure 4-24. The error amplifier for Channel 1 is used to regulate the output voltage and compensate the voltage regulation loop. It is a voltage output op amp that is designed to use Type III (PID) compensation. Type III compensation has two compensating zeros, two poles and a pole at the origin. The figure also shows the transfer function for each section.

For this analysis, the LC filter in the two-phase design is combined into one. The inductances are in parallel and the output capacitance is the total sum of all C_{OUT}. The ESR is the parallel combination of all ESRs. The DCR is the parallel combination all inductor DCRs.The output load is represented by a resistor R.

The output filter contains a complex double pole formed by the capacitor and inductor and a zero from the output capacitor and its ESR. The transfer function of the filter is shown in Equation 4-65.

EQUATION 4-65:

$$G_{FILTER1}(s) = \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{Q \times \omega_o} + \left(\frac{s}{\omega_o}\right)^2}$$

Where:

$$\omega_z = \frac{1}{C_O \times ESR_{CO}}$$

$$\omega_o = \frac{1}{\sqrt{C_O \times L_O}}$$

$$Q = \frac{1}{DCR + ESR_{CO}} \times \sqrt{\frac{L_O}{C_O}}$$

(For R>> ESR_{CO} and R >> DCR)

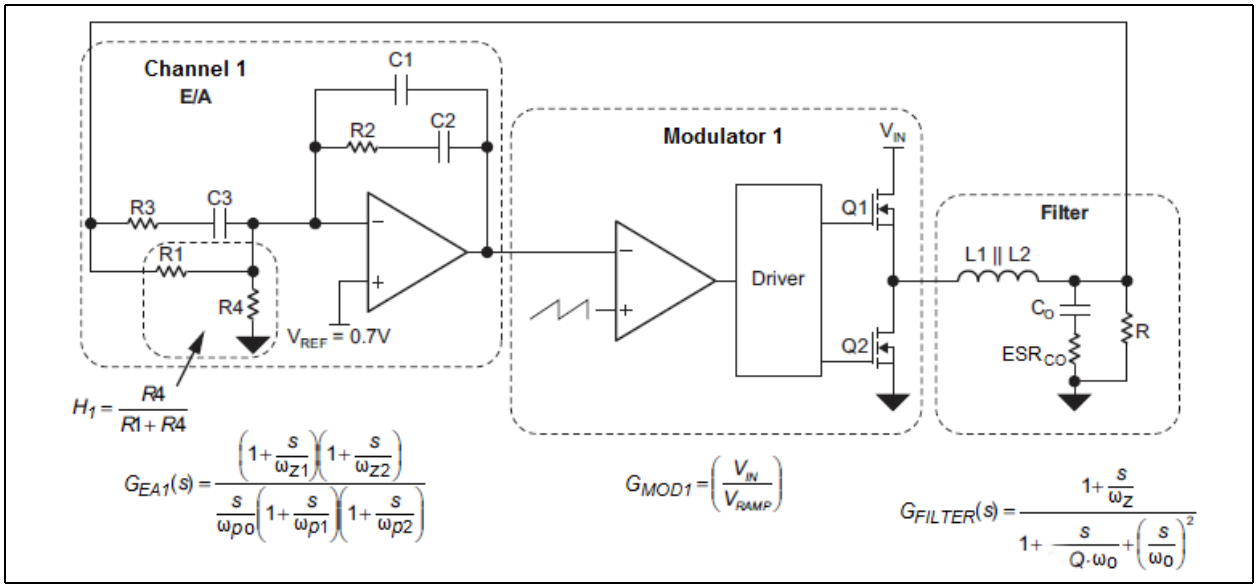


FIGURE 4-24: *Voltage Loop and Transfer Functions.*

Compensation is necessary to ensure the control loop has adequate bandwidth and phase margin to properly respond to input voltage and output current transients.

High gain at DC and low frequencies are needed for accurate output voltage regulation. Attenuation near the switching frequency prevents switching frequency noise from interfering with the control loop.

The Modulator Gain is proportional to the input voltage and inversely proportional to the internal ramp voltage generated by the oscillator. The MIC2155 peak-to-peak ramp voltage is 1V as shown in Equation 4-66.

EQUATION 4-66:

$$G_{MOD1} = \left(\frac{V_{IN}}{V_{RAMP}}\right)$$

The output voltage divider attenuates V_{OUT} and feeds it back to the error amplifier. The divider gain is shown in Equation 4-67.

EQUATION 4-67:

$$H_1 = \frac{R4}{R1 + R4} = \frac{V_{REF}}{V_{OUT}}$$

The modulator, filter and voltage divider gains can be multiplied together to show the open-loop gain of these parts. See Equation 4-68.

EQUATION 4-68:

$$G_{VD}(s) = G_{FILTER1}(s) \times H_1 \times G_{MOD1}$$

This transfer function is plotted in Figure 4-25. At low frequency, the transfer function gain equals the modulator gain times the voltage divider gain. As the frequency increases toward the LC filter resonant frequency, the gain starts to peak. The increase in the gain's amplitude equals Q. Just above the resonant frequency, the gain drops at a –40 db/decade rate. The phase quickly drops from 0° to almost –180 degrees before the phase boost of the zero brings it back up to –90 degrees. Higher values of Q cause the phase to drop quickly. In a well-damped low-Q system the phase changes more slowly.

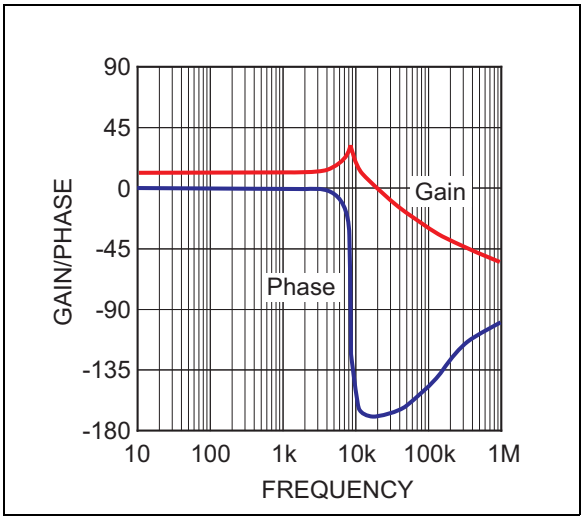


FIGURE 4-25: *G_{VD} Transfer Function.*

As the frequency approaches the zero frequency (Fz), formed by C_O and its ESR, the slope of the gain curve changes from –40 db/decade rate to –20 db/decade rate and the phase increases. The zero causes a 90° phase boost. Ceramic capacitors, with their smaller values of capacitance and ESR, push the zero and its phase boost out to higher frequencies, which allow the

phase lag from the LC filter to drop closer to –180 degrees. The system will be close to being unstable if the overall open-loop gain crosses 0 dB while the phase is close to –180 degrees. If the output capacitance and/or ESR is high, the zero moves lower in frequency and helps to boost the phase, leading to a more stable system.

The error amplifier is a type III compensated which has two zeros, two poles and a pole at the origin. This type of error amplifier works well when Ceramic output capacitors make up the majority of C_{OUT} because it introduces an extra zero that helps improve phase margin. See Equation 4-69.

EQUATION 4-69:

$$G_{EA1}(s) = \frac{\left(1+\frac{s}{\omega_{Z1}}\right)\times\left(1+\frac{s}{\omega_{Z2}}\right)}{\frac{s}{\omega_{PO}}\times\left(1+\frac{s}{\omega_{P1}}\right)\times\left(1+\frac{s}{\omega_{P2}}\right)}$$

Where:

$$\omega_{Z1} = \frac{1}{R2\times C2}$$

$$\omega_{Z2} = \frac{1}{(R1+R3)\times C3}$$

$$\omega_{PO} = \frac{1}{R1\times C1}$$

$$\omega_{P1} = \frac{1}{\frac{C1\times C2}{C1+C2}\times R2}$$

$$\omega_{P2} = \frac{1}{R3\times C3}$$

Figure 4-26 shows the bode plot of the error amplifier transfer function.

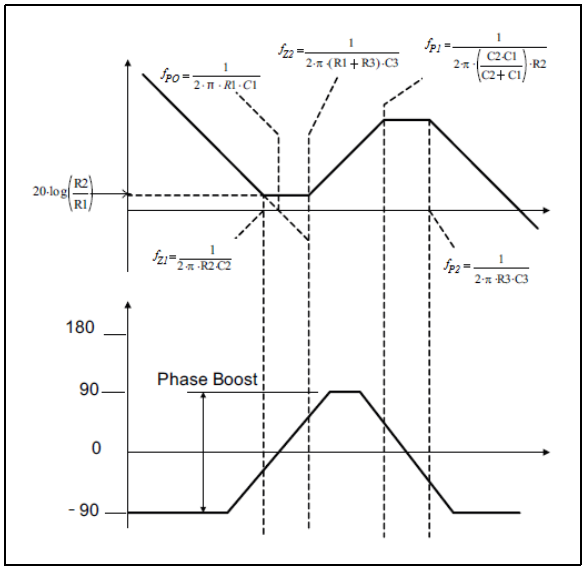


FIGURE 4-26: *Type III Compensated Error Amplifier Gain/Phase.*

4.20 Error Amplifier Design Procedure

Step 1: Decide on the crossover frequency.

To maximize transient response, the open-loop bandwidth should be made reasonably high. Initially, the bandwidth can be selected to be 1/10 of the output switching frequency. This may be improved once the design is built and measurements are made. An initial bandwidth of 100 kHz for the MIC2155 is a good choice.

Step 2: Determine the gain required at the crossover frequency.

G_{Boost} is how much gain boost is needed for the G_{EA1}, so that the open-loop transfer function crosses 0 dB at the pre-determined crossover frequency. This can be measured by plotting the $G_{VD}(s)$ transfer function or can be estimated with Equation 4-70 and Equation 4-71.

EQUATION 4-70:

For $f_C > f_Z$ (when ESR is relatively large),

$$G_{BOOST} = \frac{1}{\frac{H_1\times V_{IN}}{V_M}\times\left(\frac{f_O}{f_Z}\right)^2\times\left(\frac{f_Z}{f_C}\right)}$$

Where:

f_O = LC filter resonant frequency
f_C = open loop bandwidth chosen in Step 1
f_Z = zero formed by C_{OUT} and its ESR
H_1 = voltage divider attenuation
V_M = amplitude of the internal sawtooth ramp (V_M = 1)
V_{IN} = Input voltage to the power supply

EQUATION 4-71:

For $f_C < f_Z$ (when ESR is very small),

$$G_{BOOST} = \frac{1}{\frac{H_1\times V_{IN}}{V_M}\times\left(\frac{f_O}{f_C}\right)^2}$$

Where:

f_O = LC filter resonant frequency
f_C = open loop bandwidth chosen in Step 1
f_Z = zero formed by C_{OUT} and its ESR
H_1 = voltage divider attenuation
V_M = amplitude of the internal sawtooth ramp (V_M = 1)
V_{IN} = Input voltage to the power supply

Step 3: Determine the phase boost needed at the crossover frequency.

Typically, 52 degrees of phase margin can be used for most applications. This is a good trade off between an overdamped system (slower response to transients) and an underdamped system (overshoot or unstable response to transients). It also allows some margin for component tolerances and variations due to ambient temperature changes. The phase margin excluding the error amplifier phase boost at the crossover frequency

(f_C) can be determined by plotting the $G_{VD}(s)$ phase on a bode plot or can be estimated with the formula in Equation 4-72.

EQUATION 4-72:

$$\varphi_{M(XBOOST)} = tan^{-1}\left(\frac{1-\left(\frac{f_C}{f_O}\right)^2}{\frac{f_C}{Q \times f_O}}\right) + tan^{-1}\left(\frac{f_C}{f_Z}\right)$$

The additional phase boost required from the error amplifier is shown in Equation 4-73.

EQUATION 4-73:

$$\varphi_{BOOST} = 52° - \varphi_{M(XBOOST)}$$

Step 4: Determine the frequencies f_{Z2} and f_{P1}.

The frequencies for the zero and pole (f_{Z2} and f_{P1}) are calculated for the desired amount of phase boost at the crossover frequency (f_C). See Equation 4-74.

EQUATION 4-74:

$$f_{Z2} = f_C \times \sqrt{\frac{1-\sin\left[\frac{\varphi_{BOOST}}{2}\right]}{1+\sin\left[\frac{\varphi_{BOOST}}{2}\right]}}$$

$$f_{P1} = f_C \times \sqrt{\frac{1+\sin\left[\frac{\varphi_{BOOST}}{2}\right]}{1-\sin\left[\frac{\varphi_{BOOST}}{2}\right]}}$$

Step 5: Determine the frequency for f_{Z1}.

The low-frequency zero, f_{Z1}, is initially set to one-fifth of the LC resonant frequency. If it is set too low, it forces the low frequency gain to be low and impact transient response. If set too high, it does not add enough phase boost at the LC resonant frequency. This could cause conditional stability, which is when the phase drops below –180 degrees before the gain crosses 0 dB. If the DC gain should drop in this situation, this may lead to an unstable system. Refer to Equation 4-75.

EQUATION 4-75:

$$f_{Z1} = \frac{f_O}{5}$$

Step 6: Determine the frequency for f_{P2}.

This is the high frequency pole, which is useful in additional attenuation of the switching frequency. It should initially be set at half of the switching frequency. If it is set too low, it lowers the phase margin at the crossover frequency, making it difficult to achieve the proper phase margin. If set too high, it does not provide attenuation of the switching frequency, which could lead to jitter of the switching waveform or instability under certain conditions. The f_{P2} can be calculated with Equation 4-76.

EQUATION 4-76:

$$f_{P2} = \frac{f_S}{2}$$

4.21 Calculating Error Amplifier Component Values

Once the pole and zero frequencies have been fixed, the error amplifier's resistor and capacitor values are calculated.

R1: This value is chosen first. All other component values are calculated from R1. A value of 10 kΩ is suggested. If R1 is chosen too high, R2 may be very large and the high impedances could be sensitive to noise. If the remote sense amplifier is used, R1 must be large enough so than not more than 500 µA of current is drawn from the amplifier.

R2: The value of R2 is determined from the mid-band gain of the error amplifier. This gain depends on the frequencies of the poles, zeros and LC filter resonant frequency.

Based on the amount of G_{EA1} gain necessary at the crossover frequency, the error amplifier mid-band gain and R2 values are calculated using the formulas in Equation 4-77.

EQUATION 4-77:

For $f_C > f_Z$ and $f_{P1} = f_Z$,

$$G_{CO} = \frac{V_M}{H_1 \times V_{IN}} \times \left(\frac{f_Z}{f_O}\right)^2 \times \left(\frac{f_C}{f_Z}\right) \times \frac{f_{Z2}}{f_{P1}}$$

$$R2 = R1 \times G_{CO}$$

EQUATION 4-78:

For $f_C < f_Z$ and $f_{P1} = f_Z$,

$$G_{CO} = \frac{V_M}{H_1 \times V_{IN}} \times \left(\frac{f_C}{f_O}\right)^2 \times \frac{f_{Z2}}{f_C}$$

$$R2 = R1 \times G_{CO}$$

The other component values are calculated as indicated in Equation 4-79, Equation 4-80, Equation 4-81 and Equation 4-82.

EQUATION 4-79:

$$C2 = \frac{1}{2 \times \pi \times f_{Z1} \times R2}$$

EQUATION 4-80:

$$C3 = \frac{1}{2 \times \pi \times f_{Z2} \times (R1 + R3)}$$

For R1>> R3,

$$C3 = \frac{1}{2 \times \pi \times f_{Z2} \times R1}$$

EQUATION 4-81:

$$C1 = \frac{C2}{2 \times \pi \times (f_{P1} \times C2 \times R2) - 1}$$

EQUATION 4-82:

$$R3 = \frac{1}{2 \times \pi \times f_{P2} \times C3}$$

4.22 Compensation of the Current Sharing Loop

The control circuitry for Channel 2 forces the channel's output current to match the current in Channel 1. The Channel 2 error amplifier compares the inductor currents in the two channels and adjusts the duty cycle of Channel 2 to control its output current. A block diagram is shown in Figure 4-27.

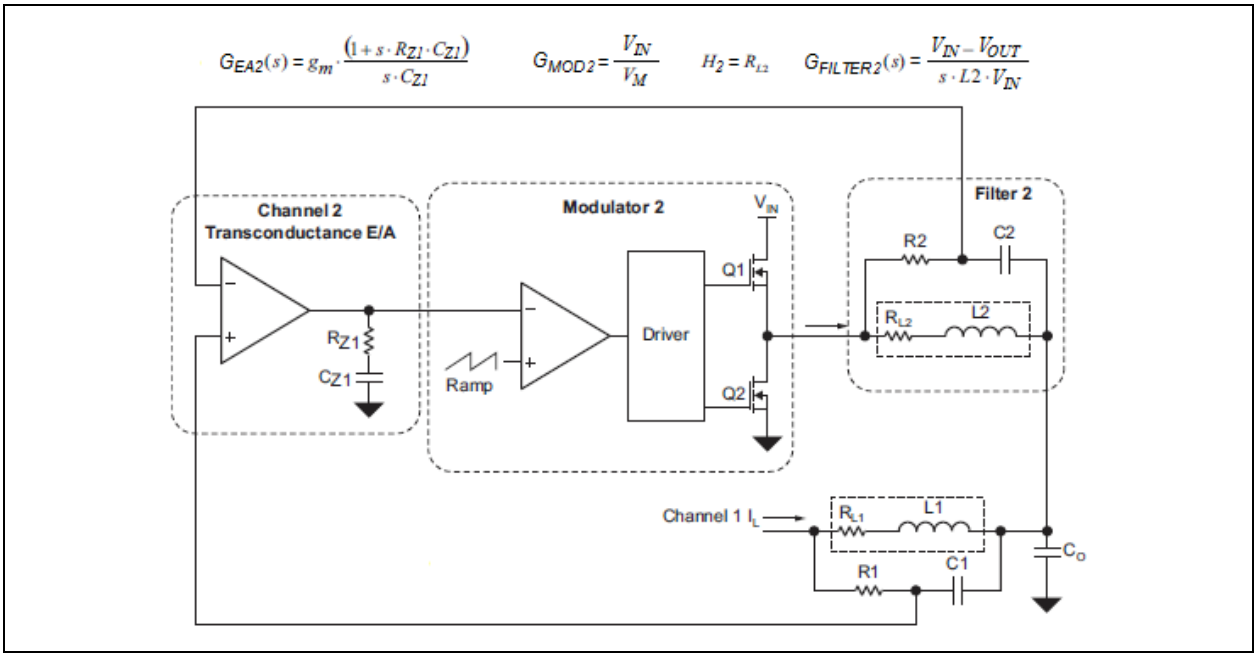


FIGURE 4-27: *Current Sharing Loop and Transfer Functions.*

Unlike the voltage output amplifier used for Channel 1 compensation, a transconductance amplifier is used for the Channel 2 compensation since only a pole/zero combination is required for compensation. The transconductance amplifier transfer function is shown in Equation 4-83.

EQUATION 4-83:

$$G_{EA2}(s) = g_m \times \frac{1 + s \times R_{Z1} \times C_{Z1}}{s \times C_{Z1}}$$

Where:

R_{Z1} and C_{Z1} = the external components connected to the COMP2 pin

g_m = the transconductance of the internal error amplifier 2

The pole and zero frequencies are indicted in Equation 4-84 and Equation 4-85.

EQUATION 4-84:

$$f_{POLE} = \frac{g_m}{2 \times \pi \times C_{Z1}}$$

EQUATION 4-85:

$$f_{ZERO} = \frac{1}{2 \times \pi \times R_{Z1} \times C_{Z1}}$$

The gain of the modulator is indicated in Equation 4-86.

EQUATION 4-86:

$$G_{MOD2} = \frac{V_{IN}}{V_M}$$

Where:
V_M = the peak-to-peak amplitude of the internal sawtooth

The gain H_2 of the feedback circuit is the Channel 2 output current sense voltage divided by Channel 2 output current as shown in Equation 4-87.

EQUATION 4-87:

$$H_2 = R_{L2}$$

The filter transfer function is the output current over the applied voltage. See Equation 4-88.

EQUATION 4-88:

$$G_{FILTER2}(s) = \frac{V_{IN} - V_{OUT}}{s \times L2 \times V_{IN}}$$

The open loop transfer function is indicated in Equation 4-89.

EQUATION 4-89:

$$G_{OL2}(s) = G_{EA2}(s) \times G_{MOD2} \times H_2 \times G_{FILTER2}(s)$$

$$= \frac{g_m \times (1 + s \times R_{Z1} \times C_{Z1}) \times R_{L2} \times (V_{IN} - V_{OUT})}{(s \times C_{Z1}) \times V_m \times (s \times L2)}$$

The loop is inherently stable because the phase shift is only 90 degrees. The error amplifier pole and zero is selected to achieve a desired crossover frequency. In this example, the desired crossover frequency is 50 kHz. The transfer function of the filter, modulator and feedback is plotted in Figure 4-28.

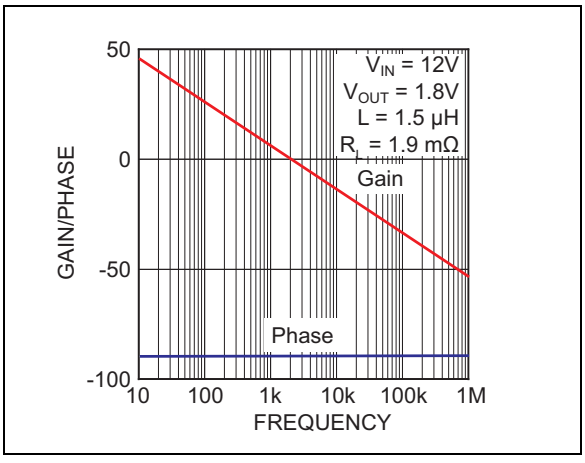


FIGURE 4-28: *Current Sharing Loop $G_{FILTER2}(s)$ x G_{MOD2} x H_2 Gain/Phase.*

The gain boost required at 50 kHz is 28 dB which is a gain of 25. The gain for frequencies above the zero is indicated in Equation 4-90.

EQUATION 4-90:

$$G_{MID} = R_{Z1} \times g_m$$

For a typical g_m = 1.25 mS, use Equation 4-91 in solving for R_{Z1}.

EQUATION 4-91:

$$R_{Z1} = \frac{G_{MID}}{g_m} = \frac{25}{1.25mS} = 20k\Omega$$

Set the zero frequency to be 1/5 of the crossover frequency. See Equation 4-92.

EQUATION 4-92:

$$C_{Z1} = \frac{1}{2 \times \pi \times R_{Z1} \times f_{Z1}}$$

$$= \frac{1}{2 \times \pi \times 20k\Omega \times 10kHz} = 800pF$$

The compensated open-loop gain/phase plot is shown in Figure 4-29.

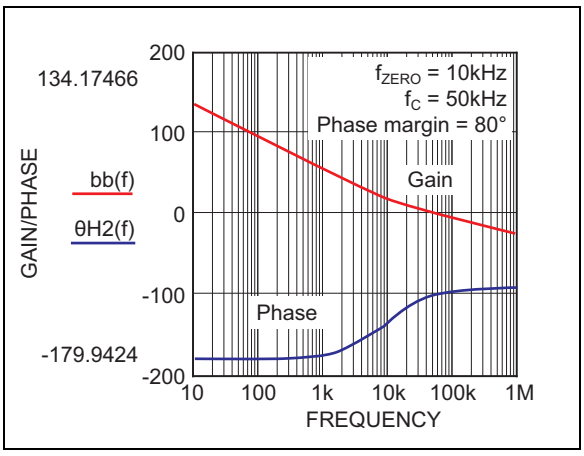


FIGURE 4-29: *Compensated Current Sharing Loop Gain/Phase.*

4.23 General Layout and Component Placement

There are three basic types of currents in a switching power supply—high di/dt, moderate di/dt and DC. Examples of each are shown in Figure 4-30.

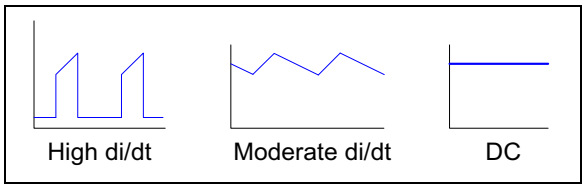


FIGURE 4-30: *Current Diagram.*

In a buck converter, high di/dt currents in the 0.5 A/ns range are generated by MOSFETs switching on and off. These fast switching currents flow in the high-side and low-side MOSFETs, external freewheeling Schottky diode and the input capacitor. Fast-switching currents also flow in the gate drive and return etch between the controller and the power FETs. At that switching speed at a 10 nH piece of etch generates 5V across itself. Therefore, attention to proper layout techniques is essential. Traces that have high di/dt currents must be kept short and wide. Additionally, a power ground plane should be used on an adjacent layer to help minimize etch inductance. Figure 4-31 shows a layout example that minimizes inductance.

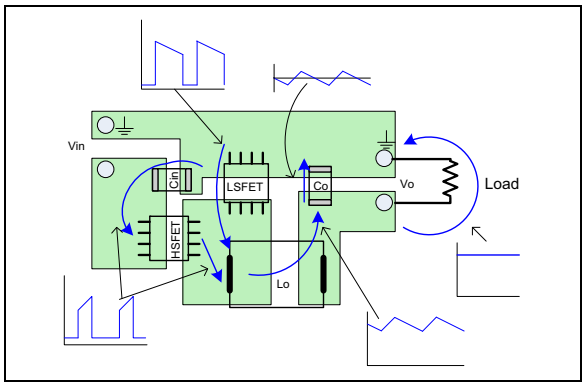


FIGURE 4-31: *Layout.*

Moderate di/dt currents flow in the inductor and output capacitor. Although layout is not as critical, it is still important to minimize inductance by using short, wide traces and a ground plane. Figure 4-31 shows the etch connecting the inductor to the output is shaped to force current to flow past the output capacitor before reaching the output terminal (or output load). This minimizes the series inductance between the inductor and the capacitor, which improves the ability of the capacitor to filter ripple. Additionally, the inductor current has a large DC component and requires a wide trace to minimize voltage drop and power dissipation.

DC currents in a high-current buck converter require wide etch paths to minimize voltage drop and power dissipation. The input and output current are mainly DC. At or near maximum output power, the inductor current is also predominately DC and requires ample etch to reduce copper loss, reduce temperature rise and improve efficiency. Minimizing voltage drops in the output and ground path helps improve output voltage regulation for configurations without remote voltage sensing.

The gate drive connections to both the high-side and low-side MOSFETs must each have their own return current path. The high-side MOSFET's source is connected to the switch node and returns back to the controller's SW1 or SW2 pin. The high-side gate drive and return (switch node) traces should be routed on top of each other on adjacent layers to minimize inductance. These traces swing between V_{IN} and ground and should be routed away from low-voltage and noise-sensitive analog etch or components. The low-side MOSFET return path is power ground. High di/dt currents flow in the low-side gate drive and return paths. These must be kept away from noise sensitive signal traces and signal ground planes.

Ceramic capacitors are recommended for most decoupling and filtering applications because of their low impedance and small size. Depending on the application, most dielectrics (X5R, X7R, NPO) are acceptable, however, Z5U type ceramic capacitor dielectrics are not recommended due to their large change in capacitance over temperature and voltage.

4.24 Design and Layout Checklist

- Ceramic capacitor placed between the high-side FET drain and the low-side FET source.
- MOSFET gate drive traces must be low inductance and routed away from noise-sensitive analog signals, components and ground planes.
- The signal and power ground planes must be separated to prevent high current and fast switching signals from interfering with the low-level, noise-sensitive analog signals. These planes should be connected at only 1 point, next to the MIC2155 controller.
- The following signals and their components should be decoupled or referenced to the power ground plane:VIN1, VIN2, VDD, PGND1, PGND2
- These analog signals should be referenced or decoupled to the analog ground plane: AVDD, SYNC, EN, SS, PGOOD, COMP1, COMP2, FB2, EA2, VOUT, FB1, AGND
- Place the current sharing RC components (that connect across the inductor) and any related filtering components close to the FB2, EA2+ and VOUT pins (18, 17, 20). The traces connecting the inductors and these components should be routed close together to minimize pickup or EMI

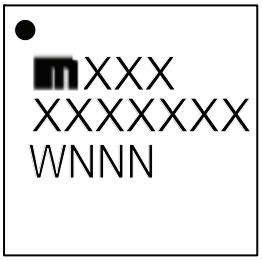
radiation.

- Place the overcurrent setting resistor close to the CS1 pin (pin 4).The switch node to this resistor connection should be connected close to the drain pin of the Channel 1 low-side MOSFET. The trace coming from the switch node to this resistor has high dv/dt and should be routed away from other noise-sensitive components and traces.
- The remote sense traces must be routed close together or on adjacent layers to minimize noise pickup. The traces should be routed away from the switch node, inductors, MOSFETs and other high dv/dt or di/dt sources.

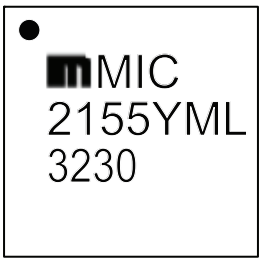
5.0 PACKAGE INFORMATION

5.1 Package Marking Information

32-lead VQFN



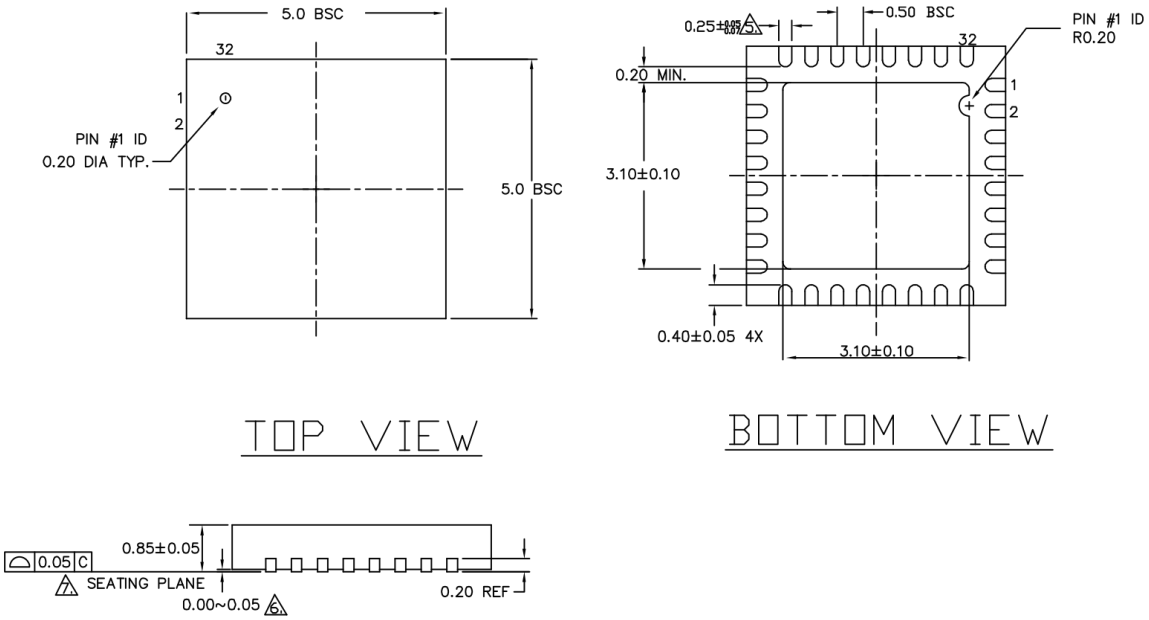
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

5.2 Package Outline Drawing



32-lead 5mm x 5 mm VQFN

APPENDIX A: REVISION HISTORY

Revision A (April 2019)

- Converted Micrel Doc# DSFP-MIC2155 to Microchip DS20006106A. Removed all references to MIC2156.
- Added some sections to comply with the standard Microchip format
- Changed the package marking format
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	XX	-	XX
Device	Junction Temp. Range	Package Options		Media Type

Device:	MIC2155	=	Two-Phase Single-Output PWM Synchronous-Buck-Control IC
Junction Temperature Range:	Y	=	–40°C to +125°C RoHS-Compliant
Package:	ML	=	32-lead (5mm x 5mm) VQFN
Media Type:	TR	=	1000/Reel for an ML Package

Example:

a) MIC2155YML-TR: Two-Phase Single-Output PWM Synchronous-Buck-Control IC, 32-lead VQFN, 1000/Reel

Note: Tape and reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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