MIC5252

150 mA High PSRR, Low Noise µCap CMOS LDO

Features

- Input Voltage Range: 2.7V to 6.0V
- PSRR = 50 dB @ V_O + 0.3V
- Ultra-Low Output Noise: 30 μV_{RMS}
- Stability with Ceramic Output Capacitors
- Ultra-Low Dropout: 135 mV @ 150 mA
- High Output Accuracy:
  - 1.0% Initial Accuracy
  - 2.0% over Temperature
- Low Quiescent Current: 90µA
- Tight Load and Line Regulation
- TTL Logic-Controlled Enable Input
- “Zero” Off-Mode Current
- Thermal Shutdown and Current Limit Protection

Applications

- Cellular Phones and Pagers
- Cellular Accessories
- Battery-Powered Equipment
- Laptop, Notebook, and Palmtop Computers
- Consumer/Personal Electronics

General Description

The MIC5252 is an efficient, precise CMOS voltage regulator optimized for ultra low-noise applications. It offers 1% initial accuracy, extremely low dropout voltage (135 mV at 150 mA) and low ground current (typically 90µA). The MIC5252 provides a very low-noise output, ideal for RF applications where a clean voltage source is required. The MIC5252 has a high PSRR even at low supply voltages, critical for battery operated electronics. A noise bypass pin is also available for further reduction of output noise.

Designed specifically for handheld and battery-powered devices, the MIC5252 provides a TTL logic-compatible enable pin. When disabled, power consumption drops nearly to zero.

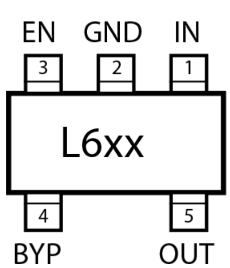
The MIC5252 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, which is critical in handheld wireless devices.

Key features include current limit, thermal shutdown, faster transient response, and an active clamp to speed up device turn-off. The MIC5252 is available in the 6-lead 2 mm × 2 mm VDFN package and the 5-Lead SOT-23 package in a wide range of output voltages.

Package Types

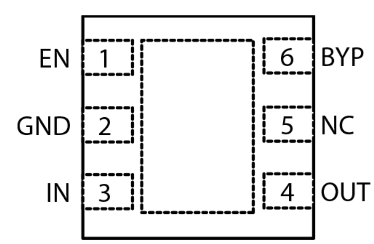
MIC5252-x.xYM5

5-Lead SOT-23
(Top View)

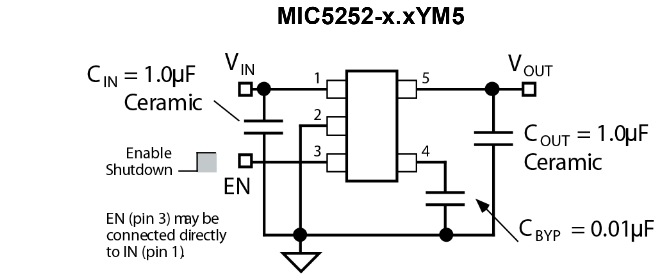


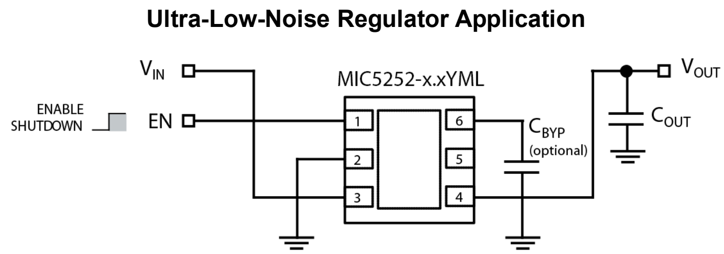
MIC5252-x.xYML

6-Lead VDFN
(Top View)

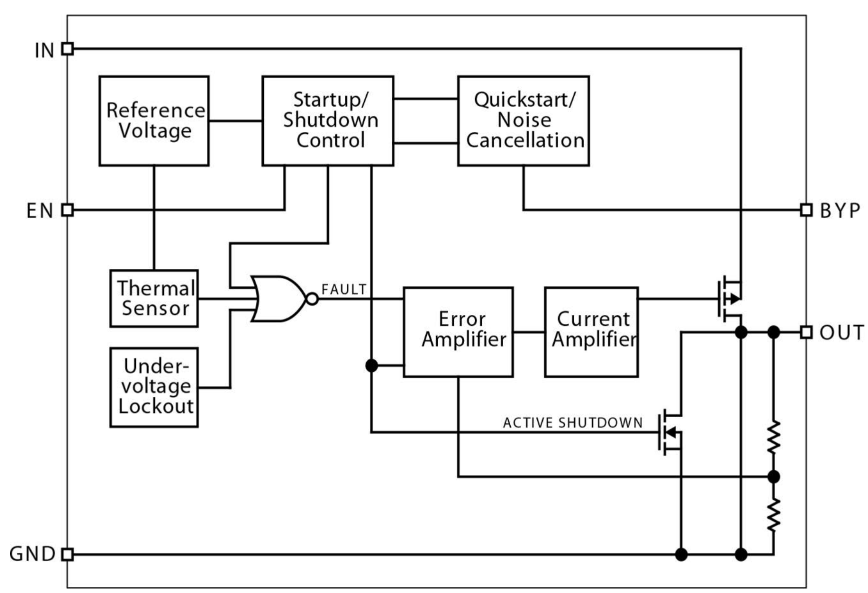


Typical Application Circuits





Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Input Voltage (V_{IN}) .... 0V to +7V
Enable Input Voltage (V_{EN}) .... 0V to +7V
Power Dissipation (P_D) .... Internally Limited (Note 1)
ESD Rating (Note 2) .... 2 kV

Operating Ratings ‡

Input Voltage (V_{IN}) .... +2.7V to +6V
Enable Input Voltage (V_{EN}) .... 0V to V_{IN}

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(MAX)} = (T_{J(MAX)} – T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The θ_{JA} of the MIC5252-x.xYM5 (all versions) is 235°C/W on a PC board. See **Section 4.7 "Thermal Considerations"** for further details.

2: Devices are ESD sensitive. Handling precautions recommended.

ELECTRICAL CHARACTERISTICS

$V_{IN} = V_{OUT}$ + 1V, $V_{EN} = V_{IN}$; I_{OUT} = 100 µA; T_J = 25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C; unless noted. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Accuracy	V_O	–1	—	1	%	I_{OUT} = 100 µA
		–3	—	**3**	%	
Line Regulation	ΔV_{LNR}	—	0.02	0.2	%	$V_{IN} = V_{OUT}$ + 1V to 6V
Load Regulation	ΔV_{LDR}	—	0.6	**1.5**	%	I_{OUT} = 0.1 mA to 150 mA (Note 2)
Dropout Voltage (Note 3)	$V_{IN} – V_{OUT}$	—	0.1	5	mV	I_{OUT} = 100 µA
		—	90	150	mV	I_{OUT} = 100 mA
		—	135	200	mV	I_{OUT} = 150 mA
		—	—	**250**	mV	I_{OUT} = 150 mA
Quiescent Current	I_Q	—	0.2	**1**	µA	V_{EN} ≤ 0.4V (shutdown)
Ground Pin Current (Note 4)	I_{GND}	—	90	**150**	µA	I_{OUT} = 0 mA
		—	117	**200**	µA	I_{OUT} = 150 mA
Ripple Rejection; I_{OUT} = 150 mA	PSRR	—	63	—	dB	f = 10 Hz, C_{OUT} = 1.0 µF, C_{BYP} = 0.01 µF
		—	48	—	dB	f = 10 Hz, $V_{IN} = V_{OUT}$ + 0.3V
		—	48	—	dB	f = 10 kHz, $V_{IN} = V_{OUT}$ + 0.3V
Current Limit	I_{LIM}	250	425	—	mA	V_{OUT} = 0V
Output Voltage Noise	e_n	—	30	—	$µV_{RMS}$	C_{OUT} = 1.0 µF, C_{BYP} = 0.01 µF, f = 10 Hz to 100 kHz

ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_{IN} = V_{OUT} + 1V$, $V_{EN} = V_{IN}$; $I_{OUT} = 100\ \mu A$; $T_J = 25°C$, **bold** values indicate $-40°C \le T_J \le +125°C$; unless noted. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Enable Input						
Enable Input Logic-Low Voltage	V_{IL}	—	—	**0.4**	V	V_{IN} = 2.7V to 5.5V, regulator shutdown
Enable Input Logic-High Voltage	V_{IH}	**1.6**	—	—	V	V_{IN} = 2.7V to 5.5V, regulator enabled
Enable Input Current	I_{EN}	—	0.01	**1**	µA	$V_{IL} \le 0.4V$, regulator shutdown
		—	0.01	**1**	µA	$V_{IH} \ge 1.6V$, regulator enabled
Shutdown Resistance Discharge	—	—	500	—	Ω	—
Thermal Protection						
Thermal Shutdown Temperature	—	—	150	—	°C	—
Thermal Shutdown Hysteresis	—	—	10	—	°C	—

Note 1: Specification for packaged product only.

2: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range from 0.1 mA to 150 mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

3: Dropout Voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value measured at 1V differential. For outputs below 2.7V, dropout voltage is the input-to-output voltage differential with the minimum input voltage 2.7V. Minimum input operating voltage is 2.7V.

4: Ground pin current is the regulator quiescent current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	°C	—
Maximum Junction Temperature	$T_{J(MAX)}$	–40	—	+125	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 5 seconds
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistance						
Thermal Resistance, SOT-23	θ_{JA}	—	235	—	°C/W	—
Thermal Resistance, 2x2 VDFN	θ_{JA}	—	90	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum rating. Sustained junction temperatures above that maximum can impact device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

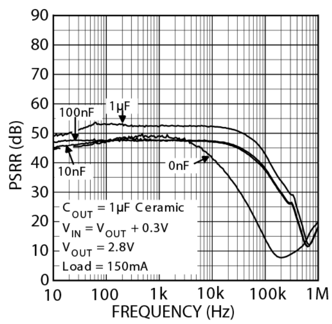


FIGURE 2-1: *PSRR with Bypass Variation (V_{IN} = V_{OUT} + 0.3V).*

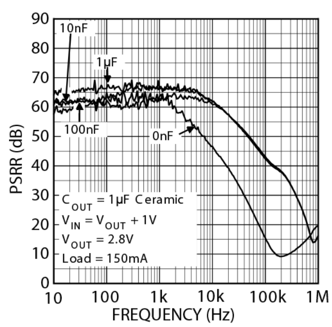


FIGURE 2-2: *PSRR with Bypass Cap Variation (V_{IN} = V_{OUT} + 1V).*

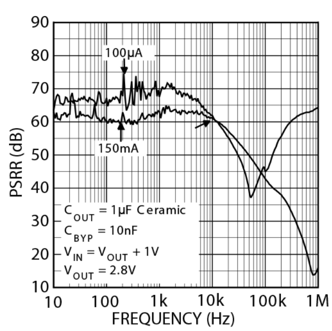


FIGURE 2-3: *PSRR with Load Variation.*

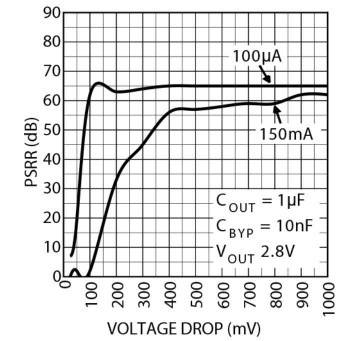


FIGURE 2-4: *PSRR at 100 Hz.*

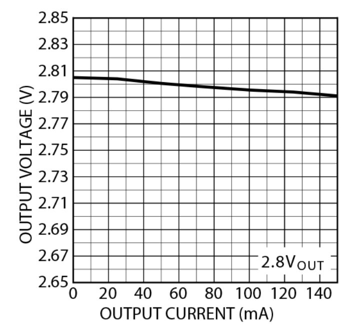


FIGURE 2-5: *Output Voltage vs. Load Current.*

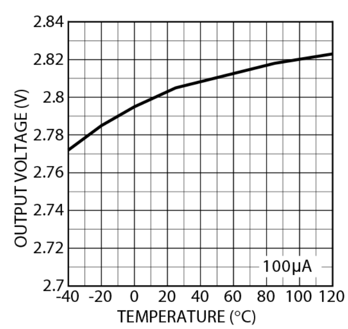


FIGURE 2-6: *Output Voltage vs. Temperature.*

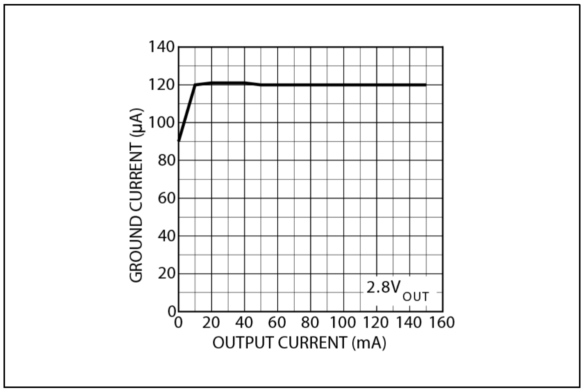


FIGURE 2-7: *Ground Current vs. Output Current.*

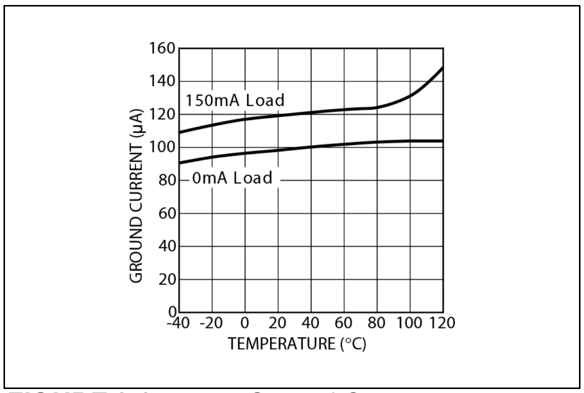


FIGURE 2-8: *Ground Current vs. Temperature.*

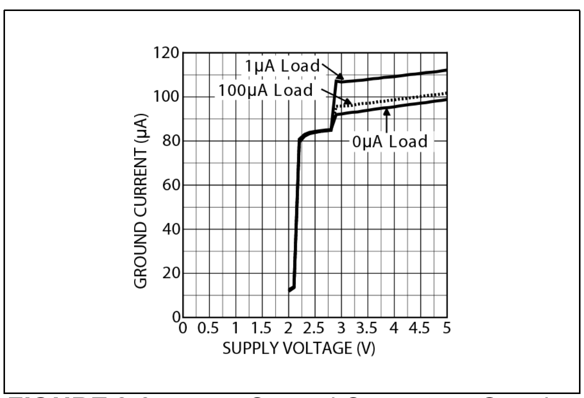


FIGURE 2-9: *Ground Current vs. Supply Voltage.*

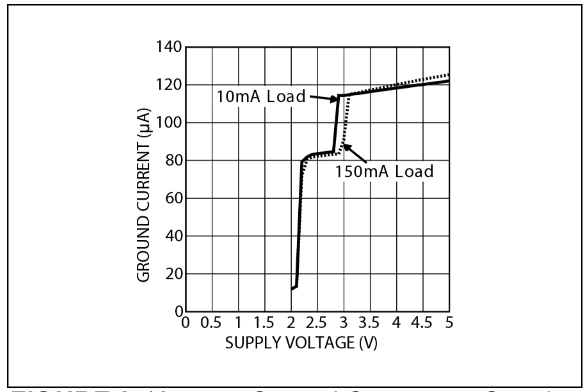


FIGURE 2-10: *Ground Current vs. Supply Voltage.*

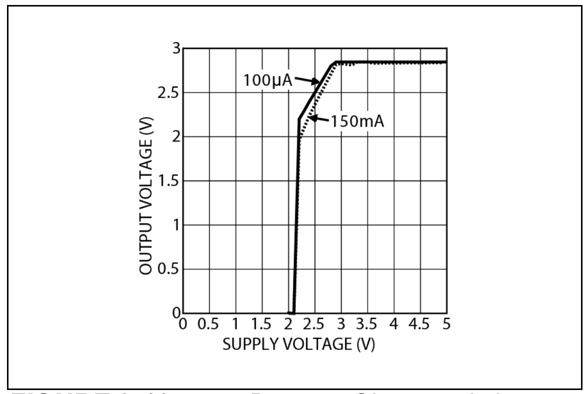


FIGURE 2-11: *Dropout Characteristics.*

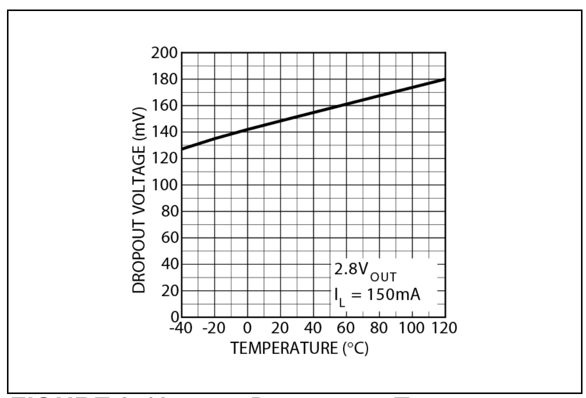


FIGURE 2-12: *Dropout vs. Temperature.*

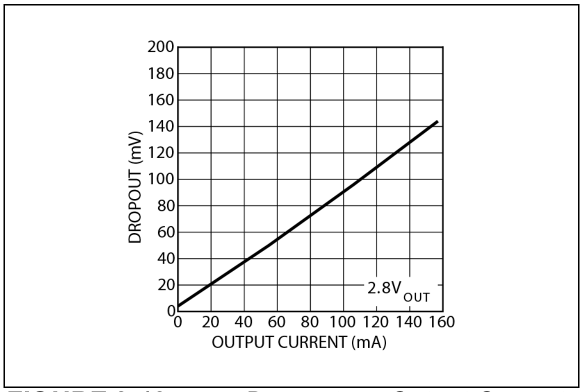


FIGURE 2-13: *Dropout vs. Output Current.*

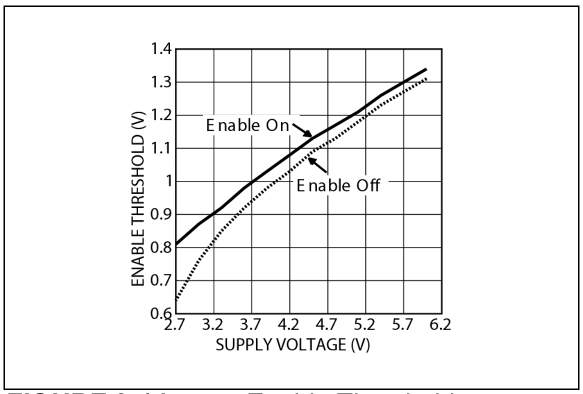


FIGURE 2-14: *Enable Threshold vs. Supply Voltage.*

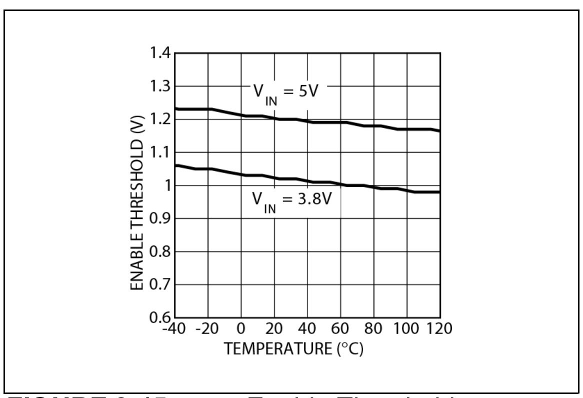


FIGURE 2-15: *Enable Threshold vs. Temperature.*

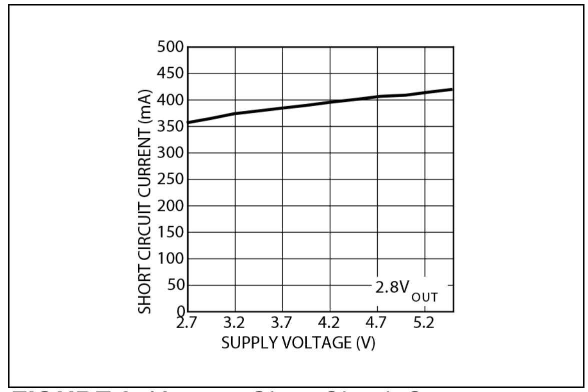


FIGURE 2-16: *Short Circuit Current vs. Input Supply Voltage.*

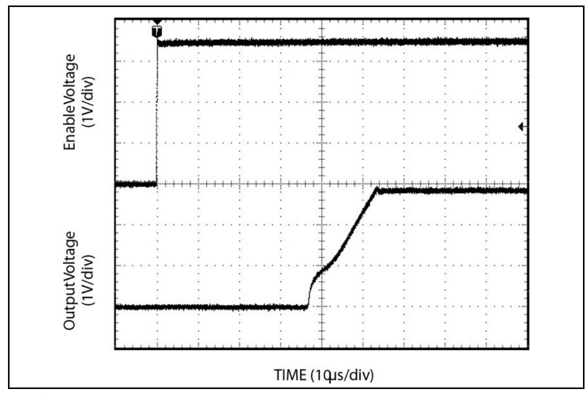


FIGURE 2-17: *Enable Pin Delay.*

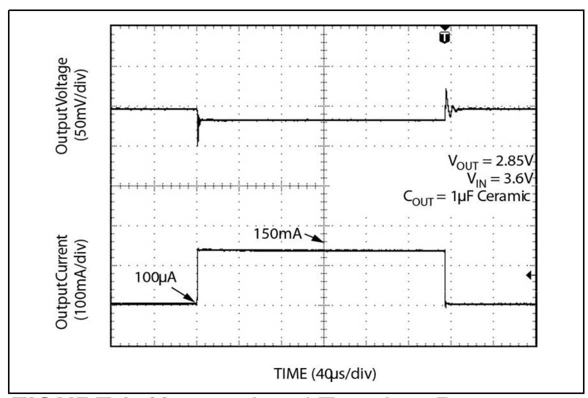


FIGURE 2-18: *Load Transient Response.*

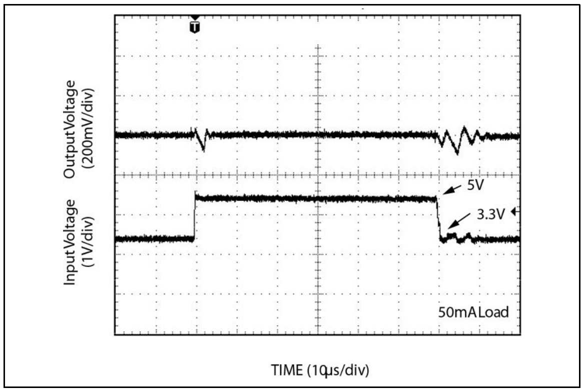


FIGURE 2-19: Line Transient Response.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

5-Lead SOT-23 Pin Number	6-Lead VDFN Pin Number	Pin Name	Description
1	3	IN	Supply Input.
2	2	GND	Ground.
3	1	EN	Enable/Shutdown (Input): CMOS compatible input. Logic high = enable; logic low = shutdown. Do not leave open.
4	6	BYP	Reference Bypass: Connect external 0.01 µF ≤ C_{BYP} ≤ 1.0 µF capacitor to GND to reduce output noise. May be left open.
5	4	OUT	Regulator Output.
—	5	NC	No Internal Connection.
—	EP	GND	Ground: Internally connected to the exposed pad. Connect externally to GND pin.

4.0 APPLICATION INFORMATION

4.1 Enable Shutdown

The MIC5252 comes with an active-high enable pin that allows the regulator to be disabled. Forcing the enable pin low disables the regulator and sends it into a "zero" off-mode-current state. In this state, current consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage. This part is CMOS and the enable pin cannot be left floating; a floating enable pin may cause an indeterminate state on the output.

4.2 Input Capacitor

The MIC5252 is a high performance, high bandwidth device. Therefore, it requires a well-bypassed input supply for optimal performance. A 1 µF capacitor is required from the input to ground to provide stability. Low-ESR ceramic capacitors provide optimal performance at a minimum of space. Additional high-frequency capacitors, such as small valued NPO dielectric type capacitors, help filter out high frequency noise and are good practice in any RF based circuit.

4.3 Output Capacitor

The MIC5252 requires an output capacitor for stability. The design requires 1 µF or greater on the output to maintain stability. The design is optimized for use with low-ESR ceramic chip capacitors. High ESR capacitors may cause high frequency oscillation. The maximum recommended ESR is 300 mΩ. The output capacitor can be increased, but performance has been optimized for a 1 µF ceramic output capacitor and does not improve significantly with larger capacitance.

X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60%, respectively, over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

4.4 Bypass Capacitor

A capacitor is required from the noise bypass pin to ground to reduce output voltage noise. The capacitor bypasses the internal reference. A 0.01 µF capacitor is recommended for applications that require low-noise outputs. The bypass capacitor can be increased, further reducing noise and improving PSRR. Turn-on time increases slightly with respect to bypass capacitance. A unique quick-start circuit allows the MIC5252 to drive a large capacitor on the bypass pin without significantly slowing turn-on time. Refer to the Typical Performance Curves section for performance with different bypass capacitors.

4.5 Active Shutdown

The MIC5252 also features an active shutdown clamp, which is an N-Channel MOSFET that turns on when the device is disabled. This allows the output capacitor and load to discharge, de-energizing the load.

4.6 No-Load Stability

The MIC5252 will remain stable and in regulation with no load unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications.

4.7 Thermal Considerations

The MIC5252 is designed to provide 150 mA of continuous current in a very small package. Maximum power dissipation can be calculated based on the output current and the voltage drop across the part. To determine the maximum power dissipation of the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

EQUATION 4-1:

$$P_{D(MAX)} = \left(\frac{T_{J(MAX)} - T_A}{\theta_{JA}}\right)$$

$T_{J(MAX)}$ is the maximum junction temperature of the die, 125°C, and T_A is the ambient operating temperature. θ_{JA} is layout-dependent; Table 4-1 shows examples of junction-to-ambient thermal resistance for the MIC5252.

TABLE 4-1: SOT-23-5 THERMAL RESISTANCE

Package	θ_{JA} Recommended Minimum Footprint	θ_{JA} 1" Square Copper Clad	θ_{JC}
SOT-23-5 (M5 or D5)	235°C/W	185°C/W	145°C/W

The actual power dissipation of the regulator circuit can be determined using the equation:

EQUATION 4-2:

$$P_D = [(V_{IN} - V_{OUT}) \times I_{OUT}] + V_{IN} I_{GND}$$

Substituting $P_{D(MAX)}$ for P_D and solving for the operating conditions that are critical to the application will give the maximum operating conditions for the regulator circuit. For example, when operating the MIC5252-2.8YM5 at 50°C with a minimum footprint layout, the maximum input voltage for a set output current can be determined as follows:

EQUATION 4-3:

$$P_{D(MAX)} = \left(\frac{125°C - 50°C}{235°C/W}\right)$$

Where:

$P_{D(MAX)}$ = 315 mW

The junction-to-ambient thermal resistance for the minimum footprint is 235°C/W, from Table 4-1. The maximum power dissipation must not be exceeded for proper operation. Using the output voltage of 2.8V and an output current of 150 mA, the maximum input voltage can be determined. Because this device is CMOS and the ground current is typically 100 µA over the load range, the power dissipation contributed by the ground current is <1% and can be ignored for this calculation.

EQUATION 4-4:

$$315mW = (V_{IN} - 2.8V) \times 150\ \text{mA}$$

$$315mW = V_{IN} \times 150\ \text{mA} - 420\ \text{mW}$$

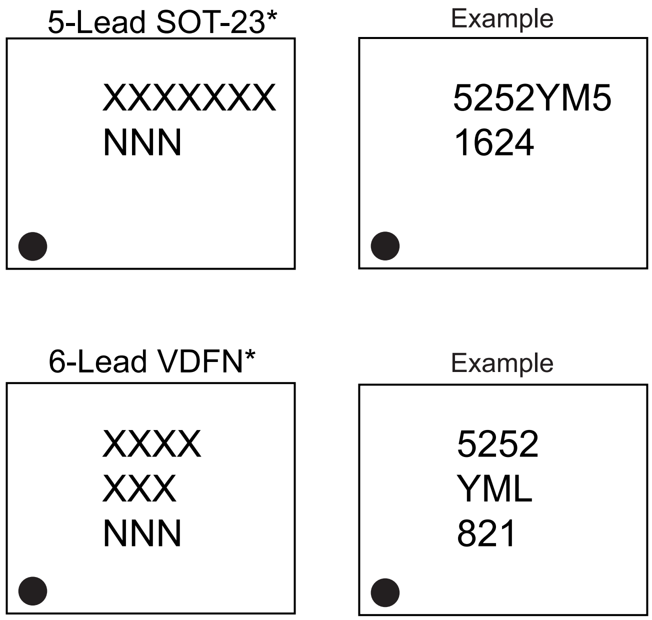
$$735\ \text{mW} = V_{IN} \times 150\ \text{mA}$$

$$V_{IN(MAX)} = 4.9V$$

Therefore, a 2.8V application at 150 mA of output current can accept a maximum input voltage of 4.9V in a SOT-23-5 package. For a full discussion of heat sinking and thermal effects on voltage regulators, refer to the “Regulator Thermals” section of Micrel’s Designing with Low-Dropout Voltage Regulators handbook.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

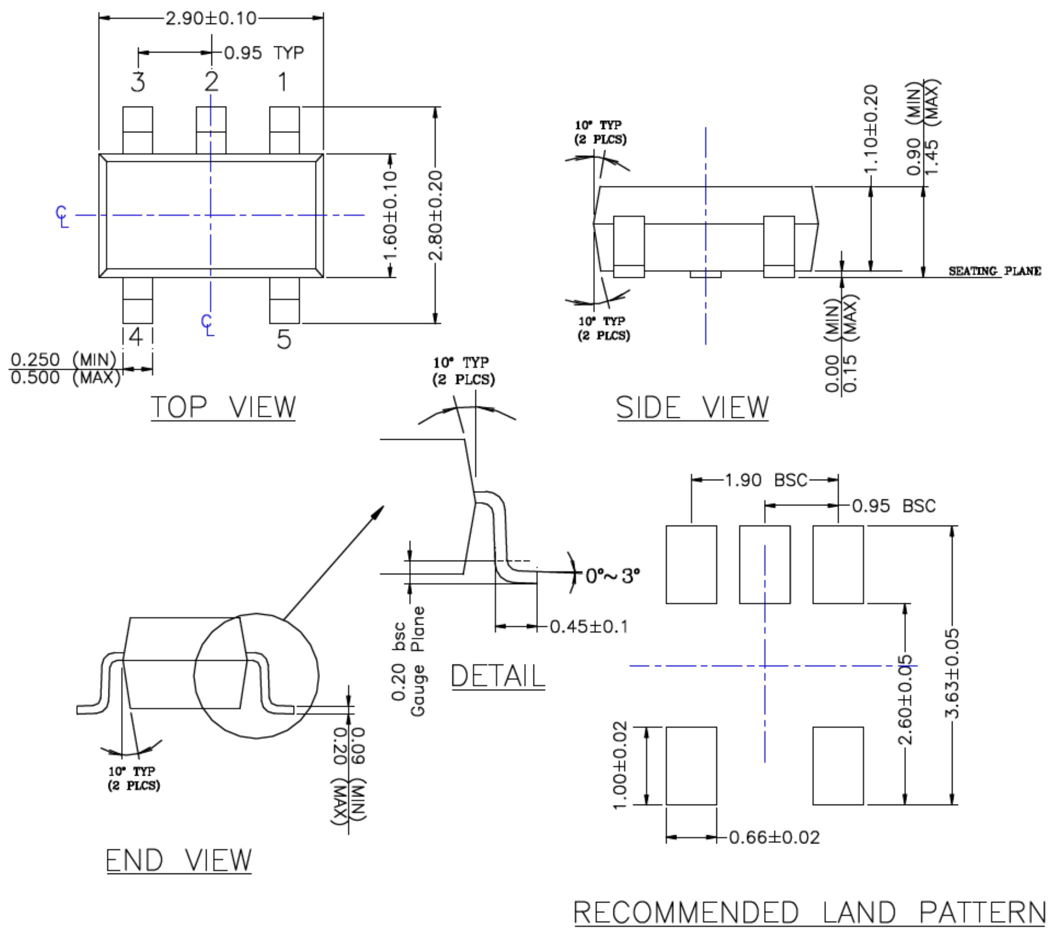
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

5-Lead SOT-23 Package Outline and Recommended Land Pattern

TITLE
5 LEAD SOT23 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOT23-5LD-PL-1	UNIT	MM



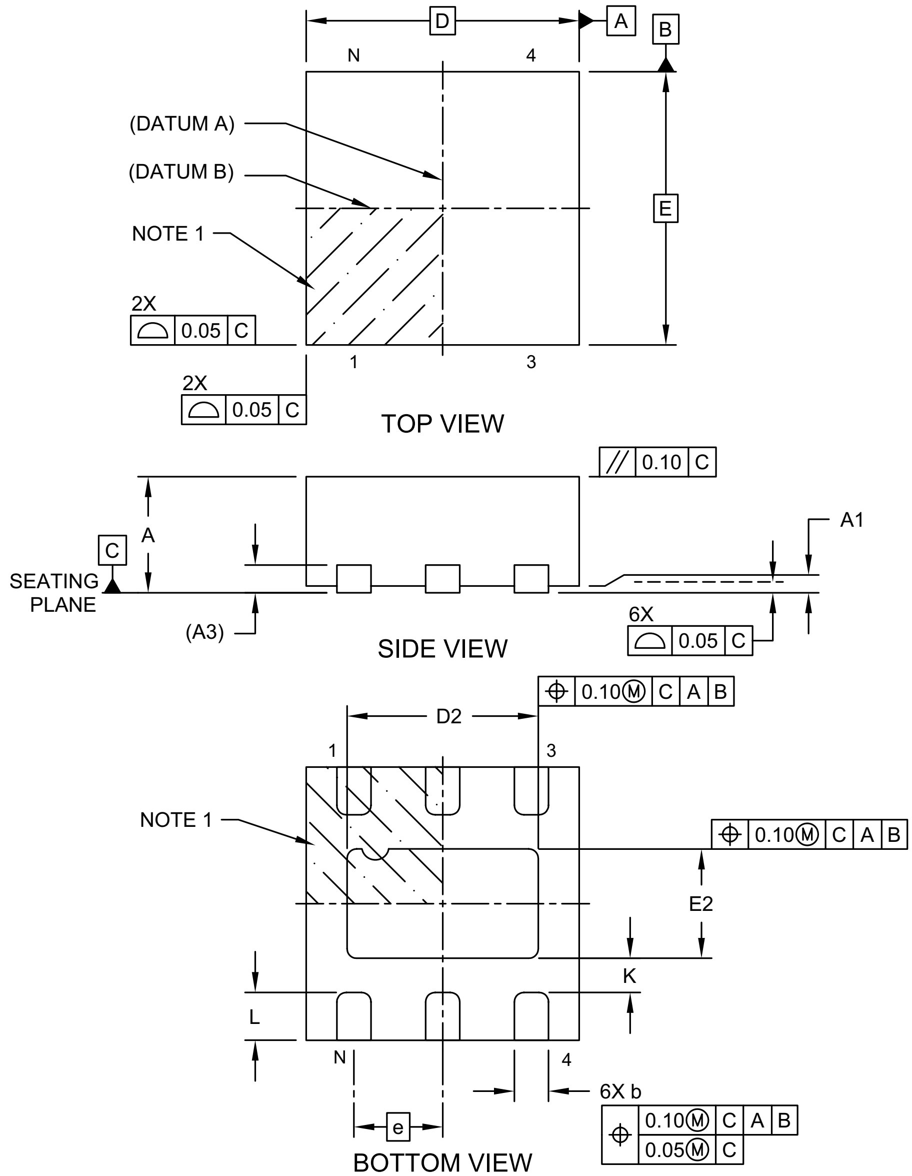
NOTE:
1. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & BURR.
2. PACKAGE OUTLINE INCLUSIVE OF SOLER PLATING.
3. DIMENSION AND TOLERANCE PER ANSI Y14.5M, 1982.
4. FOOT LENGTH MEASUREMENT BASED ON GAUGE PLANE METHOD.
5. DIE FACES UP FOR MOLD, AND FACES DOWN FOR TRIM/FORM.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

6-Lead 2mm × 2mm VDFN Package Outline and Recommended Land Pattern

6-Lead Very Thin Plastic Dual Flat, No Lead Package (JDA) - 2x2 mm Body [VDFN] Micrel Legacy Package

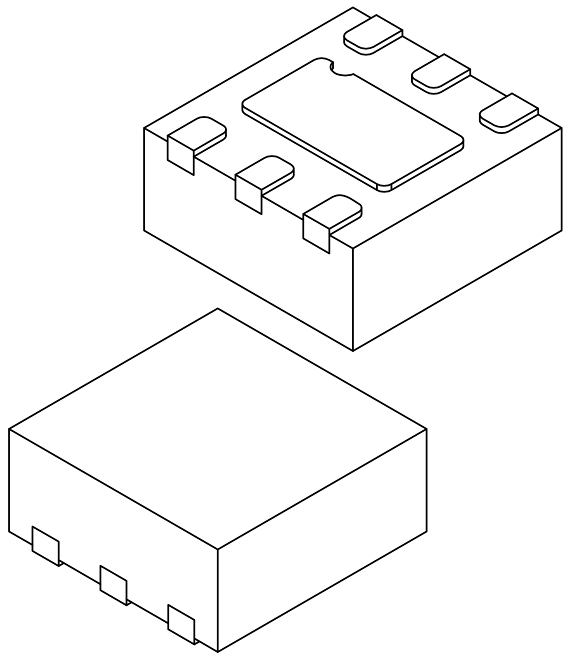
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1016A Sheet 1 of 2

6-Lead Very Thin Plastic Dual Flat, No Lead Package (JDA) - 2x2 mm Body [VDFN] Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.75	0.80	0.85
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

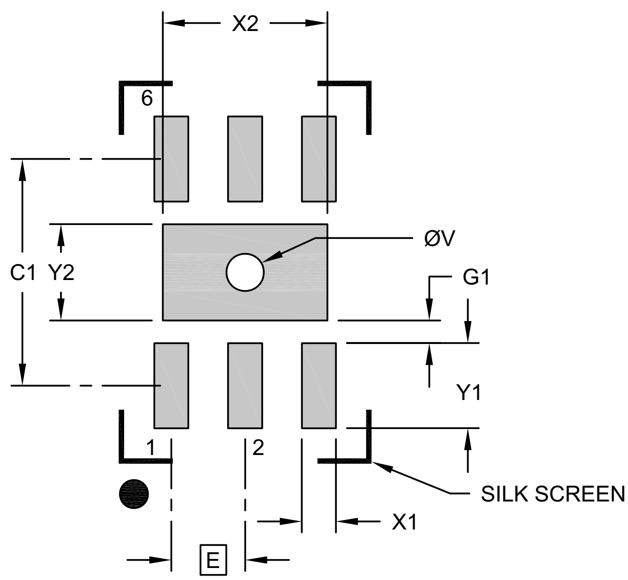
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1016A Sheet 2 of 2

6-Lead Very Thin Plastic Dual Flat, No Lead Package (JDA) - 2x2 mm Body [VDFN] Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			0.85
Optional Center Pad Length	Y2			1.45
Contact Pad Spacing	C1		2.00	
Contact Pad Width (X6)	X1			0.30
Contact Pad Length (X6)	Y1			0.75
Contact Pad to Center Pad (X6)	G1	0.20		
Thermal Via Diameter	V	0.27	0.30	0.33

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-21016A

APPENDIX A: REVISION HISTORY

Revision A (September 2021)

- Converted Micrel document MIC5252 to Microchip data sheet DS20006579A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	-X.XX	X	XX	-XX
Device	Output Voltage	Junction Temp. Range	Package	Media Type

Device:	MIC5252:	150 mA High PSRR, Low Noise µCap CMOS LDO
Output Voltage:	-1.5 = 1.5V -1.8 = 1.8V -2.5 = 2.5V -2.8 = 2.8V -2.85 = 2.85V -3.0 = 3.0V -4.75 = 4.75V	
Junction Temperature Range:	Y = –40°C to +125°C	
Package:	M5 = SOT-23-5 ML = 6-Lead 2x2 VDFN	
Media Type:	-TR = 5000/Reel	

Examples:

a) MIC5252-1.8YM5-TR: MIC5252, 1.8V Output Voltage, –40°C to +125°C Temp. Range, SOT-23-5, 5000/Reel

b) MIC5252-2.85YM5-TR: MIC5252, 2.85V Output Voltage, –40°C to +125°C Temp. Range, SOT-23-5, 5000/Reel

c) MIC5252-4.75YM5-TR: MIC5252, 4.75V Output Voltage, –40°C to +125°C Temp. Range, SOT-23-5, 5000/Reel

d) MIC5252-1.5YML-TR: MIC5252, 1.5V Output Voltage, –40°C to +125°C Temp. Range, 6-Lead 2x2 VDFN, 5000/Reel

e) MIC5252-3.0YML-TR: MIC5252, 3.0V Output Voltage, –40°C to +125°C Temp. Range, 6-Lead 2x2 VDFN, 5000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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