# UG0850 User Guide PolarFire FPGA Video Solution





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# Contents

Revision History         1           1.1         Revision 1.0         1
Overview
MIPI CSI-2
3.1         MIPI Packet Format         5           3.1.1         Short Packet         5           3.1.2         Long Packet         5
3.2 MIPI CSI-2 Based Solution
3.2.2       Implementing MIPI CSI-2 Receive Interface       6         3.2.3       Configuring the MIPI CSI-2 Receive Interface IP Cores       6
3.2.4       Implementing MIPI CSI-2 Transmit Interface         3.2.5       Configuring the MIPI CSI-2 Transmit Interface IP Cores
HDMI
SDI
5.1       XCVR Configuration for 3G-SDI Mode       16         5.2       XCVR Configuration For HD-SDI       16



# **Figures**

Figure 1	Imaging and Video Architecture	. 2
Figure 2	High-Speed Video Packet Structure	. 4
Figure 3	Low-Power Signal Processing	. 4
Figure 4	Short Packet Structure	. 5
Figure 5	Long Packet Structure	. 5
Figure 6	MIPI CSI-2 Receiver Interface	. 6
Figure 7	PF_IOD_GENERIC_RX in MIPI Mode	. 7
Figure 8	PF_IOD_GENERIC_RX Advanced Configuration	. 8
Figure 9	MIPI CSI-2 RxDecoder Configuration	
Figure 10	MIPI CSI-2 Transmitter Interface Use Case	. 9
Figure 11	MIPI CSI-2 Transmit Interface	10
Figure 12	PF_IOD_GENERIC_TX in MIPI Mode	11
Figure 13	PF_IOD_GENERIC_TX Advanced Configuration	12
Figure 14	MIPI CSI-2 Transmitter Configuration	12
Figure 15	HDMI Loopback Block Diagram	14
Figure 16	XCVR Configuration For 3G-SDI	16
Figure 17	XCVR Configuration For HD-SDI	17



# **Tables**

Table 1	SDI Configuration Register	. 15
Table 2	SDI Configuration Register Bit Field Description	. 15



# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

# 1.1 Revision 1.0

The first publication of this document.



# 2 Overview

Libero<sup>®</sup> SoC PolarFire Design Suite includes all the IP cores for building prototype solutions quickly. Thus, PolarFire FPGA-based video solutions save design time and cost without compromising performance.

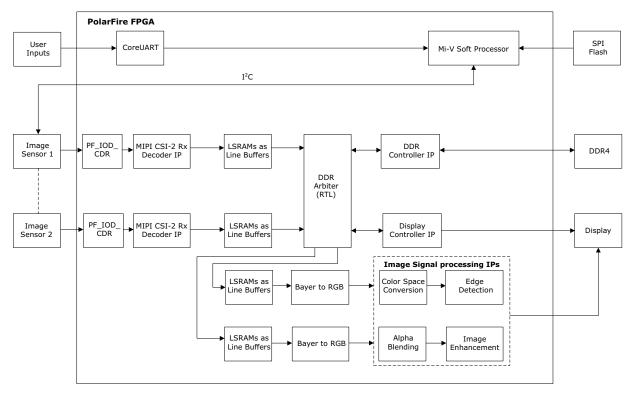
The prototype solutions can be validated on the PolarFire Video Kit, which features PolarFire MPF300T FPGA, SPI Flash, DDR4 memories, SDI, HDMI, and FTDI hardware. The on-board MIPI-CSI-2 interface can be used to connect to a dual camera daughter module. The on-board FMC connector can be used for connecting to daughter cards. For more information about the video kit, see *UG0856: PolarFire FPGA Video Kit User Guide*.

This document describes the following protocols for video solution:

- MIPI CSI-2, page 4
- HDMI, page 14
- SDI, page 15

The following figure shows the PolarFire video solution architecture.

Figure 1 • Imaging and Video Architecture



**Note:** In this solution, the camera data is received using the Microsemi's MIPI CSI-2 RX IP. The data is processed and transmitted to a display device using the HDMI interface. Alternately, Microsemi's SDI or HDMI RX and TX IPs can also be used to receive and transmit the data.



The following points summarize the video solution:

- The Mi-V soft processor is booted by a user application stored in SPI Flash. The user application
  initializes the camera sensors and processes the user requests from host PC via the UART
  interface.
- The PF\_IOD\_GENERIC\_RX block receives the high-speed MIPI CSI-2 serial data from the camera module. The IOD gear box component converts the serial data to parallel 8-bit format.
- The MIPI CSI2 RxDecoder PF IP decodes the MIPI byte packets and extracts the pixel data along with control signals.
- The raw pixel data is stored in LSRAMs as line buffers.
- The DDR Arbiter module writes these line buffers and stores video frames in DDR4.
- The DDR arbiter reads the line data and passes it to the other two LSRAMs from where the ISP modules like Bayer Conversion IP read and process the data.
- **Note:** Other signal processing requests like edge detection or alpha blending are also processed by the respective ISP module on demand. These requests come from host PC to Mi-V soft processor via the CoreUART block.
  - After processing, the ISP module passes the resultant data to the display device.



# 3 MIPI CSI-2

The MIPI CSI-2 (Camera Serial Interface) is the standard specification to transmit and receive the camera sensor raw pixel data in High speed serial format. The MIPI CSI-2 uses MIPI D-PHY as its PHY layer and sends data over it. MIPI DPHY supports 1 Lane to 4 Lanes. MIPI CSI-2 uses High- Speed (HS) and Low-Power (LP) modes, which are differentiated by the voltage levels as shown in Figure 3, page 4. In High-Speed mode Actual High Speed video packets are transferred. MIPI CSI-2 uses two kinds of High-Speed packets, Long packet and short packet. Long packets are used to transmit burst video data and short packets are used to send the control signals of the video (e.g frame start (FS), frame end (FE), Line Start and Line end). Figure 2, page 4 shows the different High speed packets and their occurrence.

### Figure 2 • High-Speed Video Packet Structure

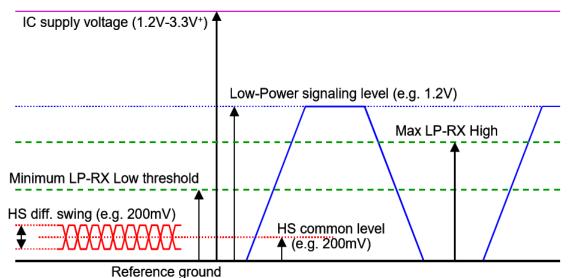


Note: The following points describe the terms used in Figure 2, page 4.

- FS: Frame Start Packet (short packet)
- Image: Pixel data of the image embedded in Long Packet
- FE: Frame End Packet (short Packet)

MIPI DPHY uses differential SLVS200 Signaling to transmit high-speed data and LVCMOS12 to transmit Low Power data. MIPI D-PHY switches between Differential High Speed mode and single ended Low Power mode on the fly on the same pair of I/Os. During Low Power mode it operates in very less speed so that it consumes low power.







# 3.1 MIPI Packet Format

This section introduces the MIPI packet formats.

## 3.1.1 Short Packet

The following figure shows the short packet structure.

### Figure 4 • Short Packet Structure

SoT or Sync Code (B8)	Data ID	Frame Number[7:0]	Frame Number[15:8]	ECC
--------------------------	---------	-------------------	--------------------	-----

## 3.1.2 Long Packet

The following figure shows the short packet structure.

### Figure 5 • Long Packet Structure

SoT B8	Data ID	Word Count[7:0]	Word Count[15:8]	ECC	Payload	CRC[7:0]	CRC[15:8]
--------	---------	--------------------	---------------------	-----	---------	----------	-----------

## 3.2 MIPI CSI-2 Based Solution

Implementation of MIPI CSI-2 based video solutions in FPGAs requires IP and design flows that reduce development time, and utilize minimal device resources to meet performance, power, and cost goals.

Microsemi offers MIPI CSI2 RxDecoder PF and MIPI CSI2 Transmitter PF IP cores, image signal processing (ISP) IP solutions, PF\_IOD\_GENERIC\_RX/TX hard IPs, high-speed transceiver hard IP, and other soft IP cores for the implementation of imaging and video solutions for PolarFire FPGAs. These IP cores are available in Libero<sup>®</sup> SoC PolarFire Design Suite for building prototype solutions quickly.

The following sections describe the building blocks of this solution and the implementation of receive and transmit interfaces.

## 3.2.1 Building Blocks of MIPI CSI-2 Video Solution

The following Microsemi IP cores form a complete MIPI CSI-2 video solution:

- Mi-V soft processor to configure the MIPI CSI-2 camera
- MIPI CSI-2 Rx and Tx IPs to decode and encode MIPI packets
- PF\_IOD\_GENERIC\_RX/TX to receive the high-speed serial MPI CSI-2 camera data
- · PLLs to generate fabric, receive and transmit clocks
- DDR Controller to store and retrieve the data
- Image Signal Processing Cores—Image Edge Detection, Bayer Conversion, and Image Enhancement IPs
- Transceiver blocks (Rx and Tx) to receive and send the data

For more information about the video solution, see

https://www.microsemi.com/product-directory/technology/3861-imaging#software-and-ip.



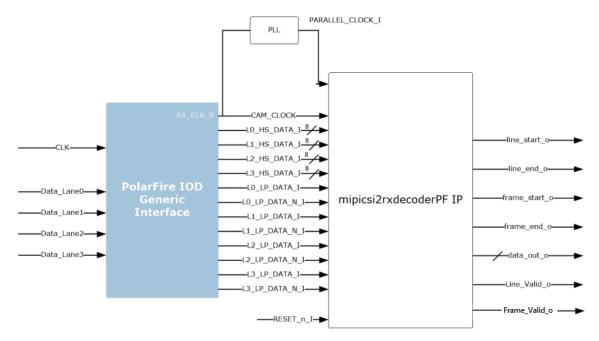
## 3.2.2 Implementing MIPI CSI-2 Receive Interface

As shown in Figure 1, page 2, the PF\_IOD\_GENERIC\_RX hard IP interfaces with the camera sensor module and passes the data to the MIPI CSI-2 Receiver Decoder IP. The PF\_IOD\_GENERIC\_RX and MIPI CSI2 RxDecoder PF IP form the receive path of the solution.

The PF\_IOD\_GENERIC\_RX is set to the MIPI mode to receive high-speed and low-power data. The high-speed MIPI CSI-2 serial data is passed through IOD gear box to convert the data into parallel 8-bit format. The MIPI CSI2 RxDecoder PF decodes the MIPI byte packets and extracts the pixel data along with the control signals.

The following figure shows the data and clock lines of the MIPI CSI-2 receiver interface solution.

Figure 6 • MIPI CSI-2 Receiver Interface



MIPI CSI2 RxDecoder PF IP decodes both high-speed short and long packets<sup>1</sup>. It supports RAW8, RAW10, and RAW12 data types for 1-Lane, 2-Lane, and 4-Lane interfaces.

## 3.2.3 Configuring the MIPI CSI-2 Receive Interface IP Cores

This section describes the configuration settings used for the PF\_IOD\_GENERIC\_RX and MIPI CSI2 RxDecoder PF IP cores in Libero.

The following figure shows the data rate, number of data I/Os, and other settings used for PF\_IOD\_GENERIC\_RX.

1.For more information about the packet format, see MIPI Packet Format, page 19.



## Figure 7 • PF\_IOD\_GENERIC\_RX in MIPI Mode

PolarFire IOD Generic Receive Interfaces Microsemi:SystemBuilder:PF_IOD_GENERIC_RX:1.1.109	
Configuration Advanced  PF_IOD_GENERIC DDR - aligned cloc DDR - centered cloc DDRX - aligned cloc DDRX - aligned cloc DDRX - fractional DDRX - fractional DDRX - dynamic c RX DDRX B G DIGRETIAL Clock input	Mbps Interface: RX_DDRX_B_G_C Max data rate: 740 Mbps Current data rate: 500 Mbps Maximum number of data I/O: one bank I/O Capture Clock: High Speed I/O clock (HS_IO_CLK) I/O clock speed: 250.00 MHz Fabric clock speed: 62.50 MHz
RX_DDRX_B_G     Differential data inputs       RX_DDRX_B_G     MIPI low power escape support       RX_DDRX_B_R     Fabric       Apply     New r       Fabric clock ratio     4	Timing: Q RX_CLK RXD XD0 XD1 XD2 XD3 XD2 XD3 XD2 XD3 XD2 XD3 XD
Data deserialization ratio     8       Fabric clock source     Fabric global clock       Enable BITSLIP port	* Waveform post bit-slip ** See user guide for actual latency between I/O and Fabric Receiver interface
	Image / Symbol /

The following points must be considered while configuring PF\_IOD\_GENERIC\_RX:

- Set the IOD data rate according to the per lane data rate of the MIPI camera. •
- Set the number of Data I/Os according to the number of lanes used by the MIPI camera. ٠
- Set the Clock to data relationship option to Centered because MIPI is a centered-aligned interface. •
- Enable the MIPI mode by selecting the MIPI Low power escape support check box. By enabling • the MIPI Mode all the Low Power Ports are added to IOD.
- Set the Fabric clock ratio to 4. ٠
- In the Advanced tab, set Received data organization to Received data independent per inputs • as shown in the following figure.





Configurator			— 🗆 X
PolarFire IOD G	eneric Receive Inte	erfaces	
Microsemi:SystemBuilder:PF_1	IOD_GENERIC_RX:1.1.109		
Q.	Configuration Advanced		configuration
■ PF_IOD_GENERIC_RX ▲	Fabric topology		Interface:
DDR - centered clock a	Fabric global clock from external	source	RX_DDRX_B_G_C Max data rate: 740
DDRX - centered clock DDRX - aligned clock a	Received data organization	Received data independent per inputs	Mbps Current data rate: 500
<ul> <li>DDRX - fractional align</li> <li>DDRX - dynamic data a</li> </ul>	RXD bus width	4	Mbps Maximum number of
-RX_DDRX_B_G_DYN	RXCTL bus width	1	data I/O: one bank
RX_DDRX_B_G_DYN RX_DDRX_B_G_DYN	Debug		I/O Capture Clock: High Speed I/O clock (HS_IO_CLK)
RX_DDRX_B_G_DYN	Expose dynamic delay control 🗌		I/O clock speed: 250.00 MHz
RX_DDRX_B_R_DYN			Fabric clock speed: 62.50 MHz
Apply New preset			Timing:
			(
			E RX_CLK_G **
	•		Image Symbol
Help -			OK Cancel
			Guilder

The MIPI CSI2 RxDecoder PF IP is configured as shown in the following figure.

#### Figure 9 • MIPI CSI-2 RxDecoder Configuration

Configurator

Configurator		-	$\Box$ $\times$
	RxDecoder PF e:mipicsi2rxdecoderPF:2.2.0	Config	gurator
Configuration			1
g_DATAWIDTH:	8		
g_LANE_WIDTH:	4 🗾 🕄		
g_NUM_OF_PIXELS:	1 •		
g_INPUT_DATA_INVERT:	0		
g_BUFF_DEPTH:	1920		
License:	C RTL C Obfuscated		
Help 🔻		ок	Cancel

The following points must be considered while configuring MIPI CSI2 RxDecoder PF:

- Set g\_DATAWIDTH to 8 for RAW8 data type. For RAW10/12 set g\_DATAWIDTH to 10/12. •
- Set g\_LANE\_WIDTH according to the number of lanes used by the MIPI camera. •
- Set g\_BUFF\_DEPTH according to the active horizontal resolution configured for the MIPI sensor.
- Set g\_NUM\_OF\_PIXELS according to the requirement. If this parameter is set to 1, only one pixel per clock is given as output. If this parameter is set to 4, four pixels per clock are given as output.



A PLL is required to generate the parallel clock (pixel clock). The RX\_CLK clock of PF\_IOD\_GENERIC\_RX serves as the input clock to the PLL. The PLL must be configured to produce the parallel clock based on the MIPI\_bit\_clk and the number of lanes used. The following equations are used to calculate the parallel clock:

CAM CLOCK I = (MIPI bit 
$$clk$$
)/4

EQ-1

PARALLEL CLOCK = (CAM CLOCK  $I \times Num$  of Lanes  $\times 8$ )/(g DATAWIDTH  $\times g$  NUM OF PIXELS)

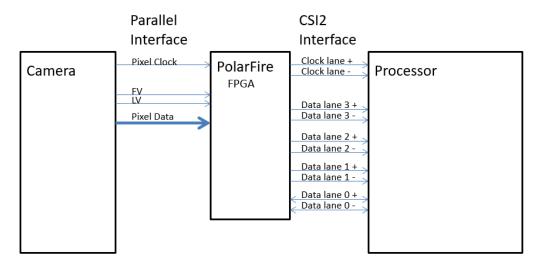
EQ-2

For more information about the MIPI CSI2 RxDecoder IP, see UG0806: MIPI CSI-2 Receiver User Guide for PolarFire.

## 3.2.4 Implementing MIPI CSI-2 Transmit Interface

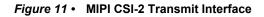
The MIPI CSI2 Transmitter PF IP converts the parallel video data into MIPI CSI-2 Byte packets. The typical system diagram for the MIPI CSI-2 transmitter interface is shown in the following diagram. The MIPI CSI2 Transmitter bridge is used to deliver data to a MIPI CSI-2 compatible receiver such as an ISP from standard Parallel video interface.

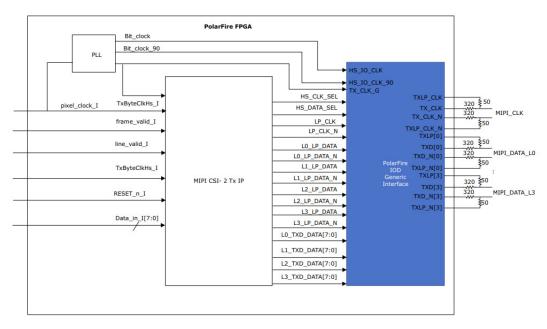
### Figure 10 • MIPI CSI-2 Transmitter Interface Use Case



The PF\_IOD\_GENERIC\_TX IP (with I/O gearing blocks) and the MIPI CSI2 Transmitter IP form the MIPI CSI-2 Transmitter interface in PolarFire devices, as shown in the following figure.







MIPI CSI2 Transmitter PF IP supports both high-speed short packets and long packets. It supports RAW8 and RAW10 data types for 1-Lane, 2-Lane, and 4-Lane interfaces.

An external resistor network shown in Figure 11, page 10 is required to accommodate the low-power and high-speed mode transitioning on the same signal pairs and also to bring down the voltage swing to 200 mV during high-speed clock and data transfers.

## 3.2.5 Configuring the MIPI CSI-2 Transmit Interface IP Cores

This section describes the configuration settings used for the PF\_IOD\_GENERIC\_TX and MIPI CSI2 Transmitter PF IP cores in Libero.

The following figure shows the data rate, number of data I/Os, and other settings used for PF\_IOD\_GENERIC\_TX.



### Figure 12 • PF\_IOD\_GENERIC\_TX in MIPI Mode

	r:PF_IOD_GENERIC_TX:1.1.106								
PF_IOD_GENERIC_T				Transmit int	erfac	e			
TX_DDR_G_A TX_DDR_G_C TX_DDRX_B_A_X2	Data rate Number of data I/Os	400	Mbps	Name	Ratio	Clock to data relationship	I/O clock source	Fabric clock	Max data rate
TX_DDRX_B_A_X3.5 TX_DDRX_B_A_X4	Clock to data relationship	Centered	•	TX_DDR_G_A	1	Aligned	Global	Global	500
TX_DDRX_B_A_X5 TX_DDRX_B_C_X2 TX_DDRX_B_C_X3.5	Use differential dock output Use differential data outputs	M		TX_DDR_G_C	1	Centered	Global High	Global	500 1000
TX_DDRX_B_C_X4 TX_DDRX_B_C_X5	Enable MIPI low power escape mode	V		TX_DDRX_B_A	2, 3.5, 4, 5	Aligned	Speed I/O Clock	Global	1600 1600 1600
Apply New prese	Ratio 4	<u> </u>		TX_DDRX_B_C	2, 3.5, 4, 5	Centered	High Speed I/O Clock	Global	1000 1600 1600 1600
	Data serialization ratio			TX_DDRX_B	2, 3.5, 4, 5	No forwarded clock	High Speed I/O Clock	Global	1000 1600 1600 1600

The following points must be considered while configuring PF\_IOD\_GENERIC\_TX:

- Set Data rate according to the required MIPI data rate per lane.
- Set Number of data I/Os according to the number of MIPI Lanes.
- Set Clock to data relationship to Centered because MIPI DPHY is a centered-aligned interface.
- Enable the MIPI low power escape mode check box.
- In the Advanced tab, set **Transmit data organization** to **Transmit data independent per outputs** as shown in the following figure.



### Figure 13 • PF\_IOD\_GENERIC\_TX Advanced Configuration

	PF_IOD_GENERIC_TX:1.1.106					
IOD_GENERIC_T		Transmit int	erface			
X_DDR_G_A X_DDR_G_C X_DDRX_B_A_X2 X_DDRX_B_A_X3.5	Transmit data organization         Transmit data independent per outputs           TXD bus width         4	Name	Ratio d	Clock to data relationship	I/O clock source	Fabric clock
X_DDRX_B_A_X3	TXCTL bus width	TX_DDR_G_A	1	Aligned	Global	Global
X_DDRX_B_A_X5 X_DDRX_B_C_X2	, Misc.	TX_DDR_G_C	1 0	Centered	Global	Global
X_DDRX_B_C_X3.5 X_DDRX_B_C_X4 X_DDRX_B_C_X5	Simulation mode Full	TX_DDRX_B_A	2, 3.5, 4 4, 5	Aligned	High Speed I/O Clock	Global
X_DDRX_B_X2		TX_DDRX_B_C	2, 3.5, 4, 5	Centered	High Speed I/O Clock	Global
		TX_DDRX_B	3.5, f	No forwarded clock	High Speed I/O Clock	Global

The MIPI CSI2 Transmitter PF IP is configured as shown in the following figure.

### Figure 14 • MIPI CSI-2 Transmitter Configuration

Configurator			_2	
MIPI CSI2 Tran		PF Confi	gura	tor
Configuration				
g_DATAWIDTH:	10	]		
g_LANE_WIDTH:	4	]		
g_HORIZANTAL_RESOLUTION:	1920	-		
g_TX_BYTE_FREQ:	50	-		
g_FREE_RUNNING_CLOCK:	1	]		
License:	⊂ RTL <sup>●</sup> Ob	fuscated		
Help 👻		O	ĸ	Cancel

The following points must be considered while configuring MIPI CSI2 Transmitter PF:

- Set g\_DATAWIDTH to 10 for RAW10 data type. For RAW8 set g\_DATAWIDTH to 8.
- Set g\_LANE\_WIDTH according to the number of lanes used by the MIPI camera.
- Set g\_HORIZONTAL\_RESOLUTION as the active resolution of the transmitted video.
- g\_TX\_BYTE\_FREQ is calculated using the following equation:

Pixel\_Clock\_I = TxByteClkHs\_I × Number of Lanes × 8 Bits per Pixel



Pixel\_clock\_i is the input clock with which incoming pixels are sampled. A PLL is used to generate the Byte clock (TxByteClkHs\_I) and bit clocks used by the MIPI DPHY block (PF\_IOD\_GENERIC\_TX). TxByteClkHs\_I must be configured such that the output MIPI CSI-2 packets sent on the interface are sampled. The following equations shows the relation between Pixel\_clock\_I and TxByteClkHs\_I depending on the number of lanes configured.

Pixel\_Clock\_I = TxByteClkHs\_I × Number of Lanes × 8 Bits per Pixel

EQ-3

### MIPI Bit Clock = $4 \times TxByteClkHs$ I

EQ-4

There are two MIPI bit clocks as per EQ-4, and these clocks are phase shifted by 90°. For more information about the MIPI CSI-2 Transmitter PF IP, see UG0826: MIPI CSI-2 Transmitter User Guide for PolarFire.



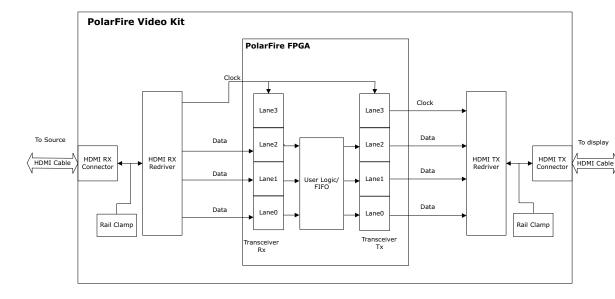
# 4 HDMI

HDMI and Display port solutions can be enabled on PolarFire devices using high speed transceivers. For more about configuring the high-speed transceivers, see *UG0677: PolarFire FPGA Transceiver User Guide*.

The TMDS signals in HDMI are DC coupled, with different differential impedances for sources and sinks. Devices such as PI3HDX1204E and PI3HDX1204B can be used for DC coupling and to ensure that impedances are at the right levels. Refer to the video board schematic for details link>.

For HDMI RX, the EDID ROM can be implemented as an I2C slave in the FPGA. Similarly, an I2C master implementation in the FPGA can be used to fetch details of a display connected to HDMI TX.

An example of how the transceiver can be configured for a HDMI 2.0 loopback is shown in the following block diagram. The transceiver should be configured in the PMA only mode.



### Figure 15 • HDMI Loopback Block Diagram



# 5 SDI

Microsemi's CoreSDIRX and CoreSDITX IP cores support SDI-based video solutions. CoreSDIRX and CoreSDITX IP cores support HD-SDI and 3G-SDI modes.

The SDI based video solution uses the PolarFire transceiver block, which converts the high-speed serial data into parallel data and passes this data to the FPGA fabric.

These two IP cores have a 32-bit CFG\_SDI register that must be configured for the required mode and color chroma sub-sampling.

This section tabulates the various segments of the CFG\_SDI register. For more information, see CoreSDIRX and CoreSDITX handbooks from Libero Catalog.

### Table 1 • SDI Configuration Register

Address	Register Name	Туре	Width	Reset Value	Description
0x00	CFG_SDI	R/W	32	0x0000082	SDI Configuration Register

Bit	Name	Туре	Reset Value	Description
31:25	Reserved	-	-	-
24	VALID	R/W	1	Valid bit. Active high. Indicates that the configuration data is valid.
23:10	Reserved	-	-	-
9:6	MODE	R/W	0010	Type of SDI Mode: 0010: HD-SDI 0101: 3G-SDI - Level A Other values are reserved.
5:3	Reserved	-	-	-
2:0	COLOR	R/W	010	Type of SDI Color. • 000: RGB (color coding), 4:4:4 (chroma sub- sampling) • 001: YCbCr (color coding), 4:4:4 (chroma sub- sampling) • 010: 001: YCbCr (color coding), 4:2:2 (chroma sub- sampling)
				Other values are reserved.

### Table 2 • SDI Configuration Register Bit Field Description



# 5.1 XCVR Configuration for 3G-SDI Mode

The following figure shows the transceiver data rate, PMA and PCS, and clock and resets settings for the 3G-SDI mode.

### Figure 16 • XCVR Configuration For 3G-SDI

Transceiver Interface		
Microsemi:SgCore:PF_XCVR:1.0.233		
PF_XCVR_default_configuration	🗉 General	
10GBASE-R SGMII	Number of lanes 1	Transceiver mode Duplex 💌
	PMA Settings	
	Transceiver data rate 2970 Mbps	
	TX clock division factor	CDR reference clock source Dedicated
	TX PLL base data rate 5940 Mbps	CDR lock mode Lock to data
	TX PLL bit clock frequency 2970 MHz	CDR reference clock frequency 148.50
	PCS Settings	
	PCS-Fabric interface width 40 💌 bits	FPGA interface frequency 74.25 MHz
	PMA Mode     Enable CDR Bit-slip port	
	C 8b10b Encoding/Decoding	
	C 64b6xb Gear Box © 64b66b	€ 64b67b
Apply New preset	Enable Disparity	Enable BER monitor state machine
The process	Enable Scrambler/Descrambler	Enable 32 bits data width
	C Soft PIPE Interface	
	Protocol PCIe Gen1 (2.5 Gbps)	
	Clocks and Resets	
	Interface Clocks	
	TX clock Regional 💌	RX clock Regional 💌
	Interface Resets PMA Reset TX and RX	PCS Reset RX Only
	Optional Ports	
	✓ Enable JA_CLK port	
	Enable TX_BYPASS_DATA port	Enable TX_ELEC_IDLE port
	Dynamic Reconfiguration	

# 5.2 XCVR Configuration For HD-SDI

Figure 17, page 17 shows the transceiver data rate, PMA and PCS, and clock and resets settings for the HD-SDI mode.

For more about configuring the high-speed transceivers, see UG0677: PolarFire FPGA Transceiver User Guide.



mi:SgCore:PF_XCVR:1.0.233	- 1	
-		
CVR_default_configuration ASE-R	General	
1	Number of lanes 1	Transceiver mode Duplex -
	PMA Settings	
	Transceiver data rate 1485 Mbps	
	TX clock division factor 4	CDR reference clock source Dedicated 💌
	TX PLL base data rate 5940 Mbps	CDR lock mode
	TX PLL bit clock frequency 2970 MHz	CDR reference clock frequency 148.50
	PCS Settings	
	PCS-Fabric interface width 40 v bits	FPGA interface frequency 37.125 MHz
	PMA Mode	
	Enable CDR Bit-slip port	
	8b10b Encoding/Decoding	
	C 64b6xb Gear Box	
	6 64b66b	C 646676
New preset	Enable Disparity	Enable BER monitor state machine
	Enable Scrambler/Descrambler	Enable 32 bits data width
	C Soft PIPE Interface	
	Protocol PCIe Gen1 (2.5 Gbps) 💌	
	Clocks and Resets	
	Interface Clocks	
	Use as PLL reference clock	
	TX clock Regional 💌	RX clock Regional 💌
	Interface Resets	
	PMA Reset TX and RX	PCS Reset RX Only
	Optional Ports	
	Enable JA_CLK port	
	Enable TX_BYPASS_DATA port	Enable TX_ELEC_IDLE port

Figure 17 • XCVR Configuration For HD-SDI

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