MRF24J40
Data Sheet

IEEE 802.15.4™ 2.4 GHz
RF Transceiver

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MRF24J40

IEEE 802.15.4™ 2.4 GHz RF Transceiver

Features:

- IEEE 802.15.4™ Standard Compliant RF Transceiver
- Supports ZigBee®, MiWi™, MiWi P2P and Proprietary Wireless Networking Protocols
- Simple, 4-Wire Serial Peripheral Interface (SPI)
- Integrated 20 MHz and 32.768 kHz Crystal Oscillator Circuitry
- Low-Current Consumption:
  - RX mode: 19 mA (typical)
  - TX mode: 23 mA (typical)
  - Sleep: 2 μA (typical)
- Small, 40-Pin Leadless QFN 6x6 mm^2 Package

RF/Analog Features:

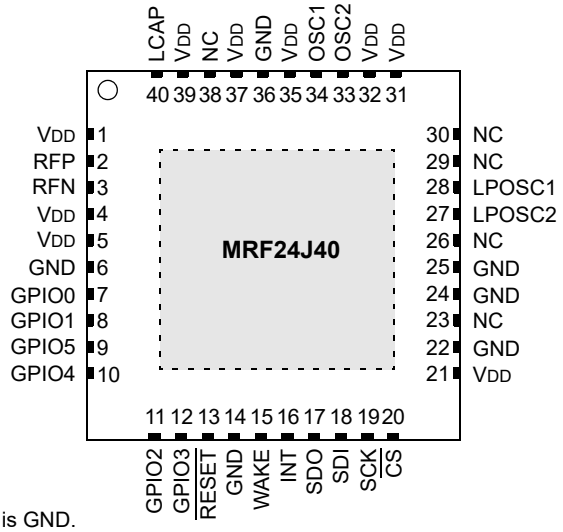
- ISM Band 2.405-2.48 GHz Operation
- Data Rate: 250 kbps (IEEE 802.15.4); 625 kbps (Turbo mode)
- -95 dBm Typical Sensitivity with +5 dBm Maximum Input Level
- +0 dBm Typical Output Power with 36 dB TX Power Control Range
- Differential RF Input/Output with Integrated TX/RX Switch
- Integrated Low Phase Noise VCO, Frequency Synthesizer and PLL Loop Filter
- Digital VCO and Filter Calibration
- Integrated RSSI ADC and I/Q DACs
- Integrated LDO
- High Receiver and RSSI Dynamic Range

MAC/Baseband Features:

- Hardware CSMA-CA Mechanism, Automatic Acknowledgement Response and FCS Check
- Independent Beacon, Transmit and GTS FIFO
- Supports all CCA modes and RSSI/ED
- Automatic Packet Retransmit Capability
- Hardware Security Engine (AES-128) with CTR, CCM and CBC-MAC modes
- Supports Encryption and Decryption for MAC Sublayer and Upper Layer

Pin Diagram:

40-Pin QFN



Note: Backside center pad is GND.

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1.0 OVERVIEW

The MRF24J40 is an IEEE 802.15.4™ Standard compliant 2.4 GHz RF transceiver. It integrates the PHY and MAC functionality in a single chip solution. Figure 1-1 shows a simplified block diagram of a MRF24J40 wireless node. The MRF24J40 creates a low-cost, low-power, low data rate (250 or 625 kbps) Wireless Personal Area Network (WPAN) device. The MRF24J40 interfaces to many popular Microchip PIC® microcontrollers via a 4-wire serial SPI interface, interrupt, wake and Reset pins.

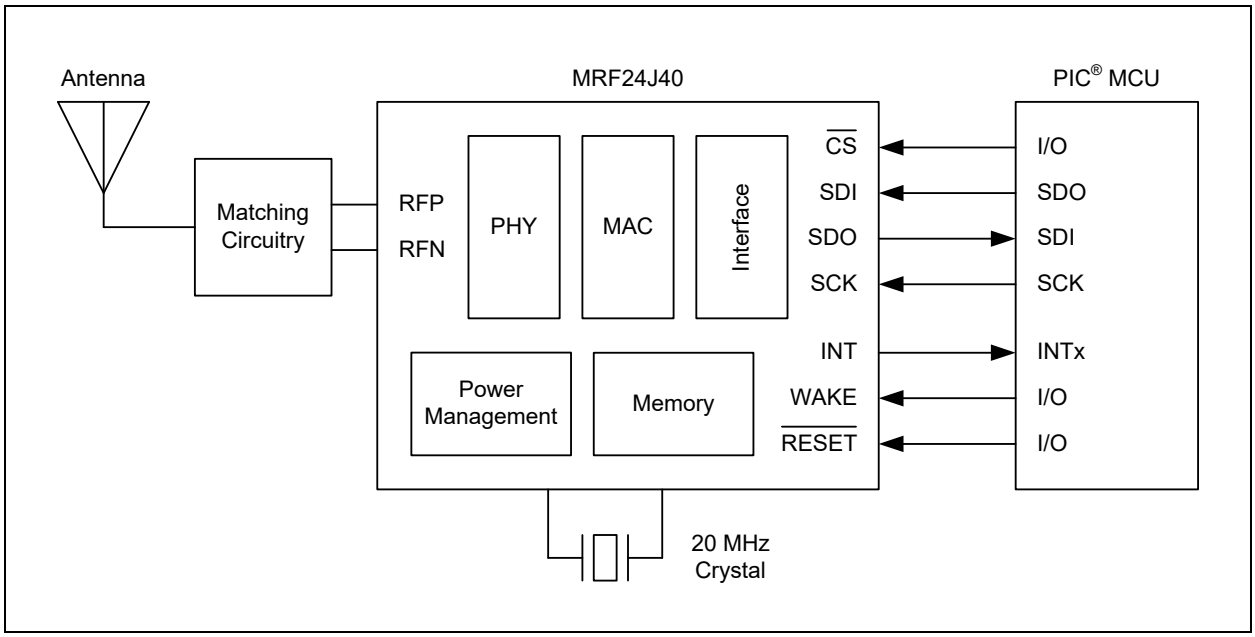
The MRF24J40 provides hardware support for:

- Energy Detection
- Carrier Sense
- Three CCA Modes
- CSMA-CA Algorithm
- Automatic Packet Retransmission
- Automatic Acknowledgment
- Independent Transmit, Beacon and GTS FIFO Buffers
- Security Engine supports Encryption and Decryption for MAC Sublayer and Upper Layer

These features reduce the processing load, allowing the use of low-cost 8-bit microcontrollers.

The MRF24J40 is compatible with Microchip's ZigBee®, MiWi™ and MiWi P2P software stacks. Each software stack is available as a free download, including source code, from the Microchip web site: http://www.microchip.com/wireless.

FIGURE 1-1: WIRELESS NODE BLOCK DIAGRAM

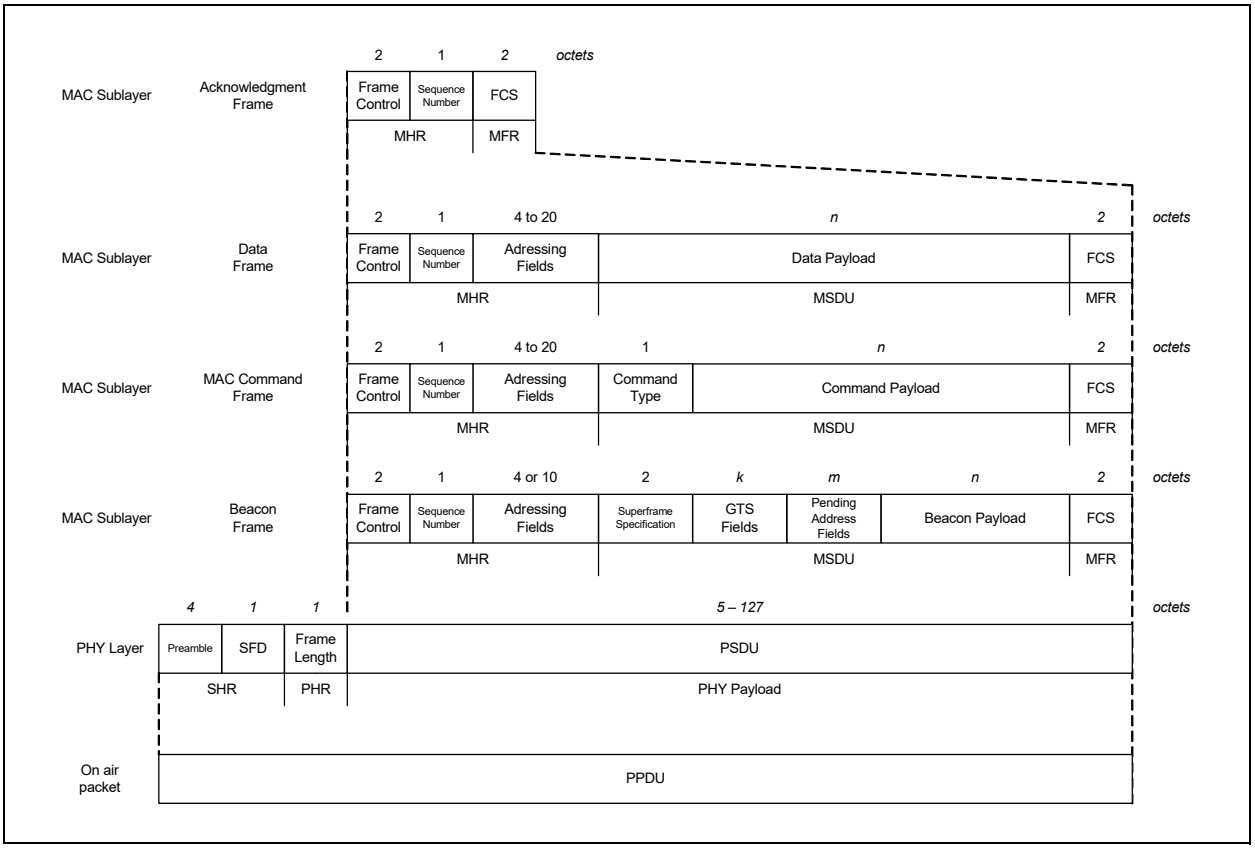


1.1 IEEE 802.15.4-2003 Standard

The MRF24J40 is compliant with the IEEE 802.15.4™-2003 Standard. The Standard specifies the physical (PHY) and Media Access Controller (MAC) functions that form the basis for a wireless network device. Figure 1-2 shows the structure of the PHY packet and MAC frame.

It is highly recommended that the design engineer be familiar with the IEEE 802.15.4-2003 Standard in order to best understand the configuration and operation of the MRF24J40. The Standard can be downloaded from the IEEE web site: http://www.ieee.org.

FIGURE 1-2: IEEE 802.15.4™ PHY PACKET AND MAC FRAME STRUCTURE



2.0 HARDWARE DESCRIPTION

2.1 2.1 Overview

The MRF24J40 is an IEEE 802.15.4 Standard compliant 2.4 GHz RF transceiver. It integrates the PHY and MAC functionality in a single chip solution. Figure 2-1 is a block diagram of the MRF24J40 circuitry.

A frequency synthesizer is clocked by an external 20 MHz crystal and generates a 2.4 GHz RF frequency.

The receiver is a low-IF architecture consisting of a Low Noise Amplifier (LNA), down conversion mixers, polyphase channel filters and baseband limiting amplifiers with a Receiver Signal Strength Indicator (RSSI).

The transmitter is a direct conversion architecture with a 0 dBm maximum output (typical) and 36 dB power control range.

An internal Transmit/Receive (TR) switch combines the transmitter and receiver circuits into differential RFP and RFN pins. These pins are connected to impedance matching circuitry (balun) and antenna. An external Power Amplifier (PA) and/or LNA can be controlled via the GPIO pins.

Six General Purpose Input/Output (GPIO) pins can be configured for control or monitoring purposes. They can also be configured to control external PA/LNA RF switches.

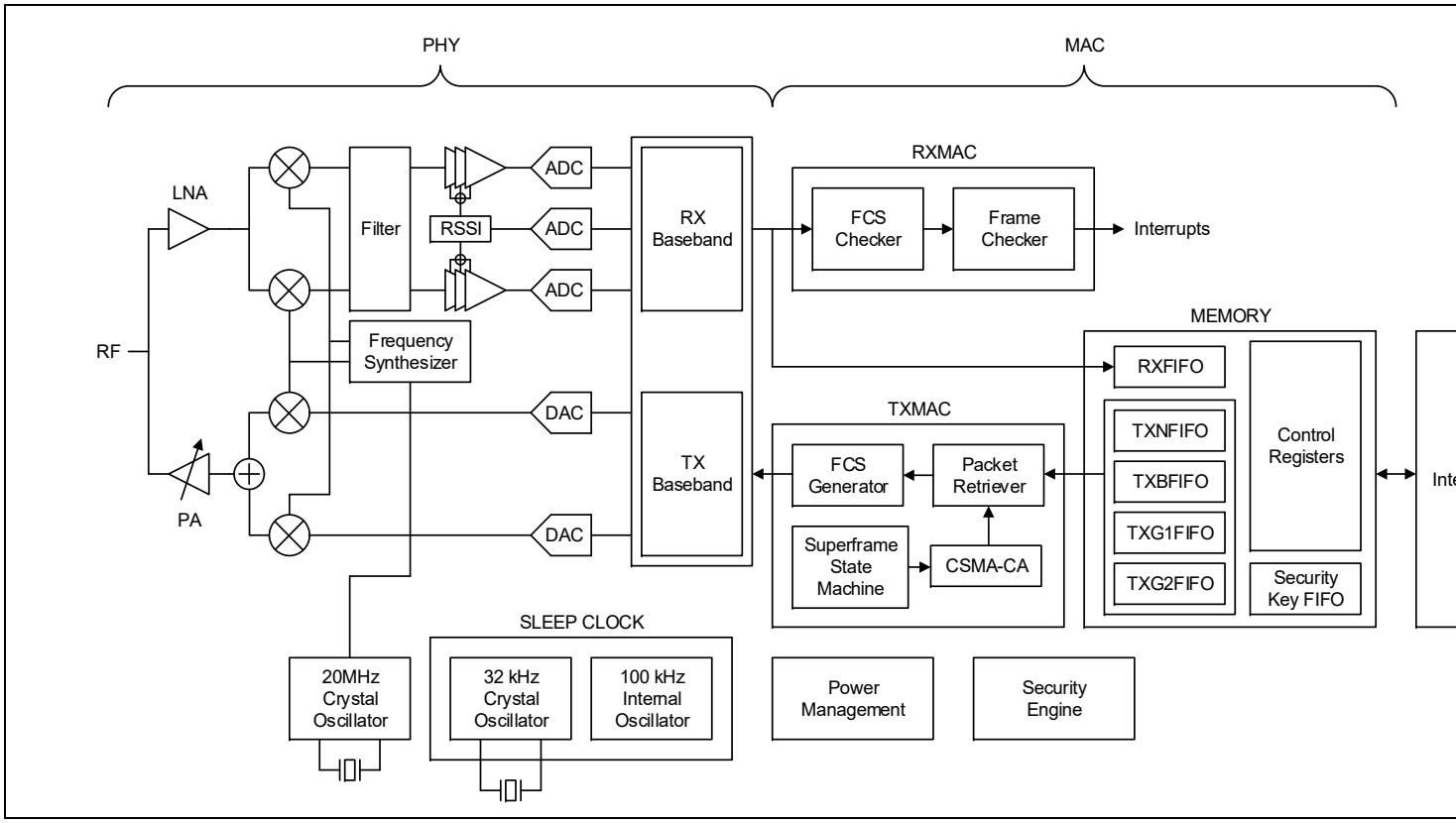
The power management circuitry consists of an integrated Low Dropout (LDO) voltage regulator. The MRF24J40 can be placed into a very low-current (2 μA typical) Sleep mode. An internal 100 kHz oscillator or 32 kHz external crystal oscillator can be used for Sleep mode timing.

The Media Access Controller (MAC) circuitry verifies reception and formats for transmission IEEE 802.15.4 Standard compliant packets. Data is buffered in Transmit and Receive FIFOs. Carrier Sense Multiple Access-Collision Avoidance (CSMA-CA), superframe constructor, receive frame filter and security engine functionality are implemented in hardware. The security engine provides hardware circuitry for AES-128 with CTR, CCM and CBC-MAC modes.

Control of the transceiver is via a 4-wire SPI, interrupt, wake and Reset pins.

2.2 Block Diagram

FIGURE 2-1: MRF24J40 ARCHITECTURE BLOCK DIAGRAM



2.3 Pin Descriptions

TABLE 2-1: MRF24J40 PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	VDD	Power	RF power supply. Bypass with a capacitor as close to the pin as possible.
2	RFP	AIO	Differential RF input/output (+).
3	RFN	AIO	Differential RF input/output (-).
4	VDD	Power	RF power supply. Bypass with a capacitor as close to the pin as possible.
5	VDD	Power	Guard ring power supply. Bypass with a capacitor as close to the pin as possible.
6	GND	Ground	Guard ring ground.
7	GPIO0	DIO	General purpose digital I/O, also used as external PA enable.
8	GPIO1	DIO	General purpose digital I/O, also used as external TX/RX switch control.
9	GPIO5	DIO	General purpose digital I/O.
10	GPIO4	DIO	General purpose digital I/O.
11	GPIO2	DIO	General purpose digital I/O, also used as external TX/RX switch control.
12	GPIO3	DIO	General purpose digital I/O.
13	$\overline{\text{RESET}}$	DI	Global hardware Reset pin active-low.
14	GND	Ground	Ground for digital circuit.
15	WAKE	DI	External wake-up trigger (must be enabled in software).
16	INT	DO	Interrupt pin to microcontroller.
17	SDO	DO	Serial interface data output from MRF24J40.
18	SDI	DI	Serial interface data input to MRF24J40.
19	SCK	DI	Serial interface clock.
20	$\overline{\text{CS}}$	DI	Serial interface enable.
21	VDD	Power	Digital circuit power supply. Bypass with a capacitor as close to the pin as possible.
22	GND	Ground	Ground for digital circuit.
23	NC	—	No Connection.
24	GND	Ground	Ground for digital circuit.
25	GND	Ground	Ground for digital circuit.
26	NC	—	No Connection. (Allow pin to float; do not connect signal.)
27	LPOSC2	AI	32 kHz crystal input.
28	LPOSC1	AI	32 kHz crystal input.
29	NC	—	No Connection. (Allow pin to float; do not connect signal.)
30	NC	—	No Connection. (Allow pin to float; do not connect signal.)
31	VDD	Power	Power supply for band gap reference circuit. Bypass with a capacitor as close to the pin as possible.
32	VDD	Power	Power supply for analog circuit. Bypass with a capacitor as close to the pin as possible.
33	OSC2	AI	20 MHz crystal input.
34	OSC1	AI	20 MHz crystal input.
35	VDD	Power	PLL power supply. Bypass with a capacitor as close to the pin as possible.
36	GND	Ground	Ground for PLL.
37	VDD	Power	Charge pump power supply. Bypass with a capacitor as close to the pin as possible.
38	NC	—	No Connection.
39	VDD	Power	VCO supply. Bypass with a capacitor as close to the pin as possible.
40	LCAP	—	PLL loop filter external capacitor. Connected to external 100 pF capacitor.

Legend: A = Analog, D = Digital, I = Input, O = Output

2.4 Power and Ground Pins

Recommended bypass capacitors are listed in Table 2-2. VDD pins 1 and 31 require two bypass capacitors to ensure sufficient bypass decoupling. Minimize trace length from the VDD pin to the bypass capacitors and make them as short as possible.

TABLE 2-2: RECOMMENDED BYPASS CAPACITOR VALUES

VDD Pin	Bypass Capacitor
1	47 pF and 0.01 μF
4	47 pF
5	0.1 μF
21	0.01 μF
31	47 pF and 0.01 μF
32	47 pF
35	47 pF
37	0.01 μF
39	1 μF

2.5 20 MHz Main Oscillator

The 20 MHz main oscillator provides the main frequency (MAINCLK) signal to internal RF, baseband and MAC circuitry. An external 20 MHz quartz crystal is connected to the OSC1 and OSC2 pins as shown in Figure 2-2. The crystal parameters are listed in Table 2-3.

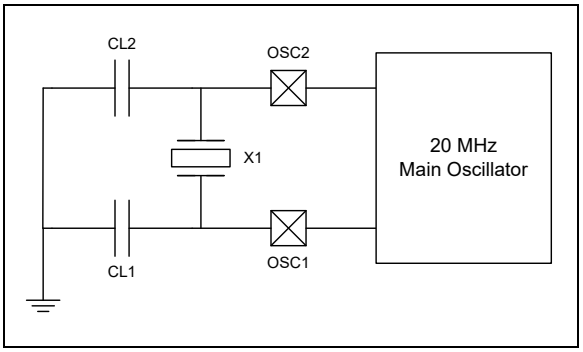
TABLE 2-3: 20 MHz CRYSTAL PARAMETERS(1)

Parameter	Value
Frequency	20 MHz
Frequency Tolerance at 25°C	±20 ppm(2)
Frequency Stability over Operating Temperature Range	±20 ppm(2)
Mode	Fundamental
Load Capacitance	10-15 pF
ESR	80Ω max.

Note 1: These values are for design guidance only.

2: IEEE 802.15.4™ Standard specifies transmitted center frequency tolerance shall be ±40 ppm maximum.

FIGURE 2-2: 20 MHz MAIN OSCILLATOR CRYSTAL CIRCUIT



2.6 Phase-Locked Loop

The Phase-Locked Loop (PLL) circuitry requires one external capacitor connected to pin 40 (LCAP). The recommended value is 100 pF. The PCB layout around the capacitor and pin 40 should be designed carefully such as to minimize interference to the PLL.

2.7 32 kHz External Crystal Oscillator

The 32 kHz external crystal oscillator provides one of two Sleep clock (SLPCLK) frequencies to Sleep mode counters. The Sleep mode counters time the Beacon Interval (BI) and inactive period for a beacon-enabled device and the Sleep interval for a nonbeacon-enabled device. Refer to **Section 3.15 "Sleep"** for more information.

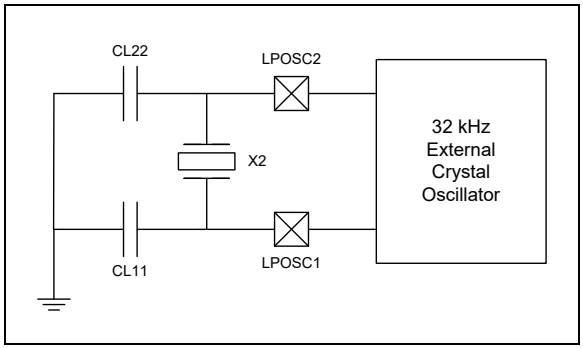
The SLPCLK frequency is selectable between the 32 kHz external crystal oscillator or 100 kHz internal oscillator. The 32 kHz external crystal oscillator provides better frequency accuracy and stability than the 100 kHz internal oscillator. An external 32 kHz tuning fork crystal is connected to the LPOSC1 and LPOSC2 pins, as shown in Figure 2-3. The crystal parameters are listed in Table 2-4.

TABLE 2-4: 32 kHz CRYSTAL PARAMETERS(1)

Parameter	Value
Frequency	32.768 kHz
Frequency Tolerance	±20 ppm
Load Capacitance	12.5 pF
ESR	70 kΩ max.

Note 1: These values are for design guidance only.

FIGURE 2-3: 32 kHz EXTERNAL OSCILLATOR CRYSTAL CIRCUIT



2.8 100 kHz Internal Oscillator

The 100 kHz internal oscillator requires no external components and provides one of two Sleep clock (SLPCLK) frequencies to Sleep mode counters. The Sleep mode counters time the Beacon Interval (BI) and inactive period for a beacon-enabled device and the Sleep interval for a nonbeacon-enabled device. Refer to **Section 3.15 "Sleep"** for more information.

The SLPCLK frequency is selectable between the 32 kHz external crystal oscillator or 100 kHz internal oscillator. The 32 kHz external crystal oscillator provides better frequency accuracy and stability than the 100 kHz internal oscillator. It is recommended that the 100 kHz internal oscillator be calibrated before use. The calibration procedure is given in **Section 3.15.1.2 "Sleep Clock Calibration"**.

2.9 Reset ($\overline{\text{RESET}}$) Pin

An external hardware Reset can be performed by asserting the $\overline{\text{RESET}}$ pin 13 low. The MRF24J40 will be released from Reset approximately 250 µs after the $\overline{\text{RESET}}$ pin is released. The $\overline{\text{RESET}}$ pin has an internal weak pull-up resistor.

2.10 Interrupt (INT) Pin

The Interrupt (INT) pin 16 provides an interrupt signal to the host microcontroller from the MRF24J40. The polarity is configured via the INTEDGE bit in the SLPCON0 (0x211[1]) register. Interrupts have to be enabled and unmasked before the INT pin is active. Refer to **Section 3.3 "Interrupts"** for a functional description of interrupts.

Note:	The INTEDGE polarity defaults to, 0 = Falling Edge. Ensure that the interrupt polarity matches the interrupt pin polarity on the host microcontroller.

Note:	The INT pin will remain high or low, depending on INTEDGE polarity setting, until INSTAT register is read.

2.11 Wake (WAKE) Pin

The Wake (WAKE) pin 15 provides an external wake-up signal to the MRF24J40 from the host microcontroller. It is used in conjunction with the Sleep modes of the MRF24J40. The WAKE pin is disabled by default. Refer to **Section 3.15.2 "Immediate Sleep and Wake-up Mode"** for a functional description of the Immediate Sleep and Wake-up modes.

2.12 General Purpose Input/Output (GPIO) Pins

Six GPIO pins can be configured individually for control or monitoring purposes. Input or output selection is configured by the TRISGPIO (0x34) register. GPIO data can be read/written to via the GPIO (0x33) register.

The GPIO pins have limited output drive capability. Table 2-5 lists the individual GPIO pin source current limits.

TABLE 2-5: GPIO SOURCE CURRENT LIMITS

Pin	Maximum Current Sourced
GPIO0	4 mA
GPIO1	1 mA
GPIO2	1 mA
GPIO3	1 mA
GPIO4	1 mA
GPIO5	1 mA

GPIO0, GPIO1 and GPIO2 can be configured to control external PA, LNA and RF switches by the internal RF state machine. This allows the external PA and LNA to be controlled by the MRF24J40 without any host microcontroller intervention. Refer to **Section 4.2 "External PA/LNA Control"** for control register configuration, timing diagrams and application information.

2.13 Serial Peripheral Interface (SPI) Port Pins

The MRF24J40 communicates with a host micro-controller via a 4-wire SPI port as a slave device. The MRF24J40 supports SPI (mode 0,0) which requires that SCK idles in a low state. The $\overline{CS}$ pin must be held low while communicating with the MRF24J40. Figure 2-4 shows timing for a write operation. Data is received by the MRF24J40 via the SDI pin and is clocked in on the rising edge of SCK. Figure 2-5 shows timing for a read operation. Data is sent by the MRF24J40 via the SDO pin and is clocked out on the falling edge of SCK.

Note: The $\overline{SDO}$ pin 17 defaults to a low state when $\overline{CS}$ is high (the MRF24J40 is not selected). If the MRF24J40 is to share a SPI bus, a tri-state buffer should be placed on the SDO signal to provide a high-impedance signal to the SPI bus. See **Section 4.4 "MRF24J40 Schematic and Bill of Materials"** for an example application circuit.

FIGURE 2-4: SPI PORT WRITE (INPUT) TIMING

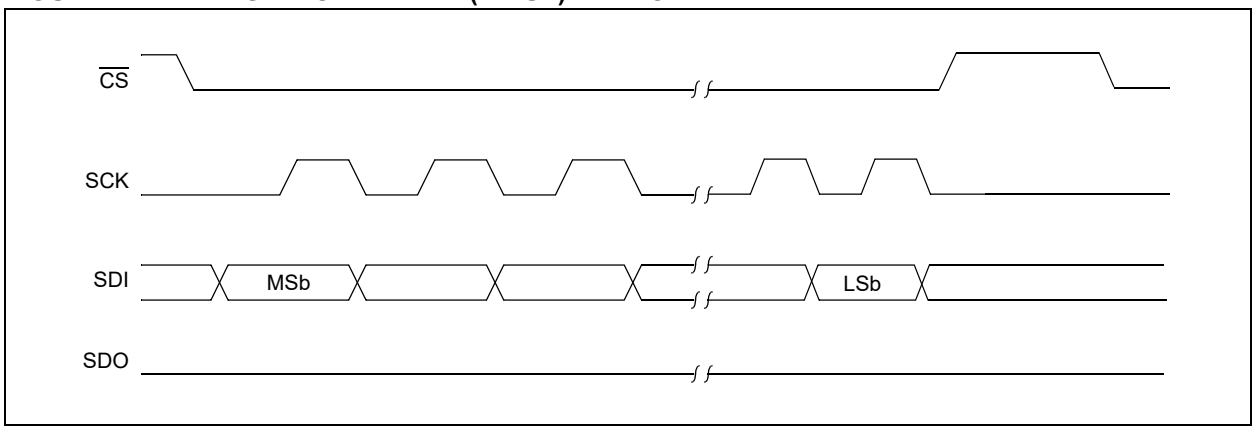
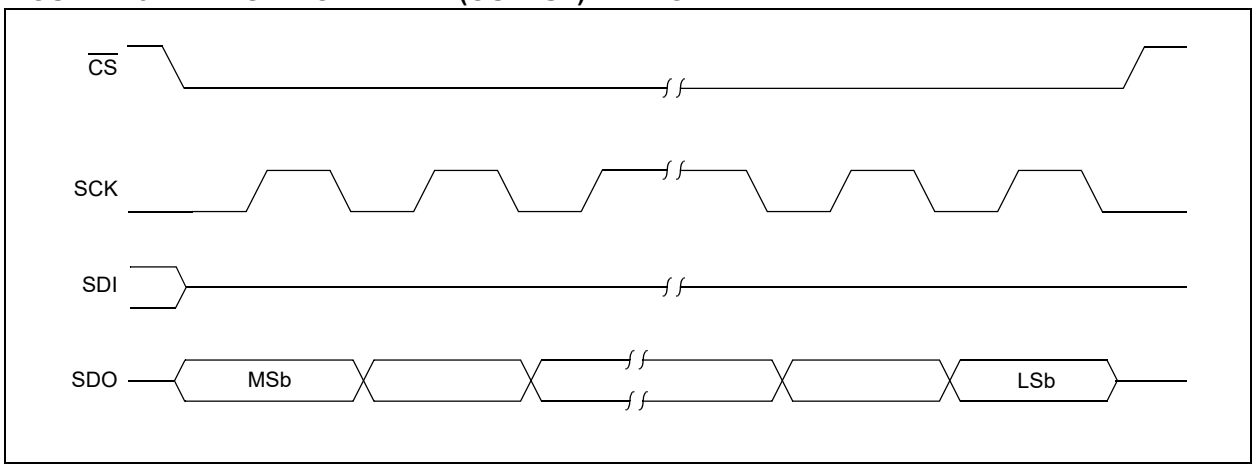


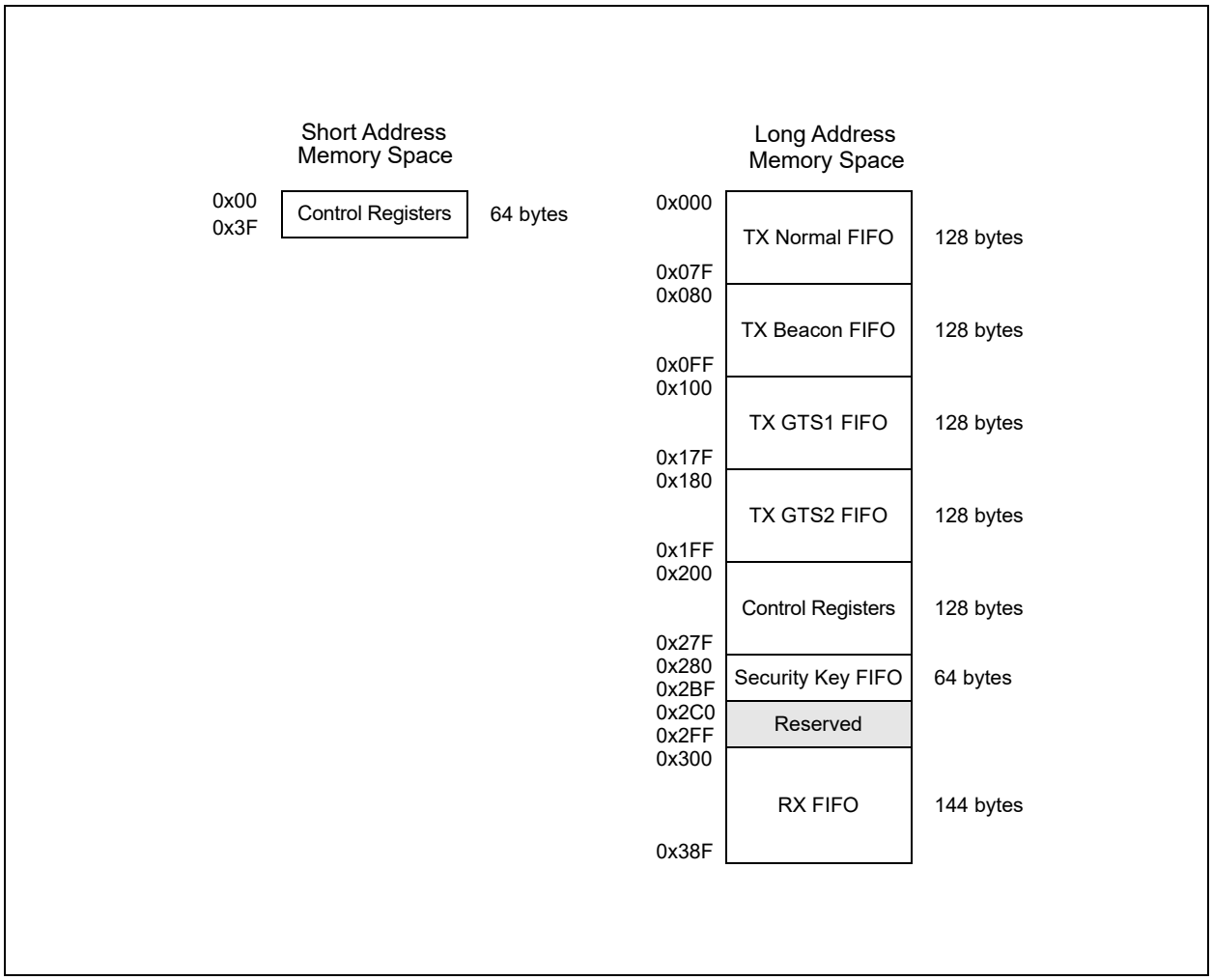
FIGURE 2-5: SPI PORT READ (OUTPUT) TIMING



2.14 Memory Organization

Memory in the MRF24J40 is implemented as static RAM and is accessible via the SPI port. Memory is functionally divided into control registers and data buffers (FIFOs), as shown in Figure 2-6. Control registers provide control, status and device addressing for MRF24J40 operations. FIFOs serve as temporary buffers for data transmission, reception and security keys. Memory is accessed via two addressing methods: Short and Long.

FIGURE 2-6: MEMORY MAP FOR MRF24J40



2.14.1 SHORT ADDRESS REGISTER INTERFACE

The short address memory space contains control registers with a 6-bit address range of 0x00 to 0x3F. Figure 2-7 shows a short address read and Figure 2-8 shows a short address write. The 8-bit SPI transfer begins with a '0' to indicate a short address transaction. It is followed by the 6-bit register address, Most Significant bit (MSb) first. The 8th bit indicates if it is a read ('0') or write ('1') transaction.

FIGURE 2-7: SHORT ADDRESS READ

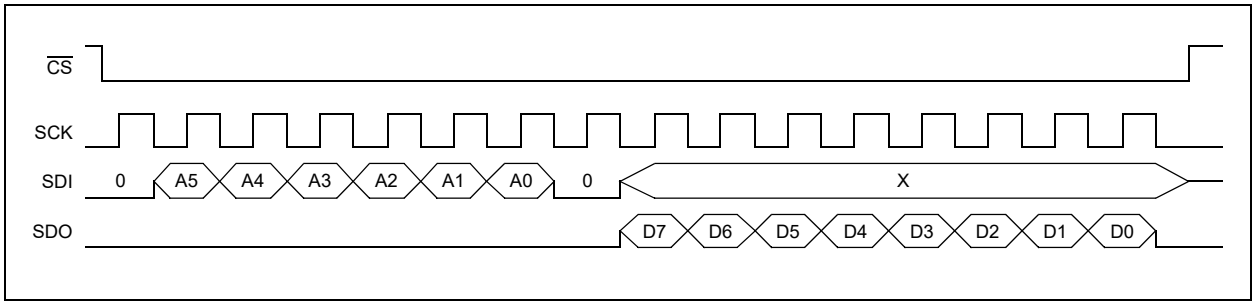
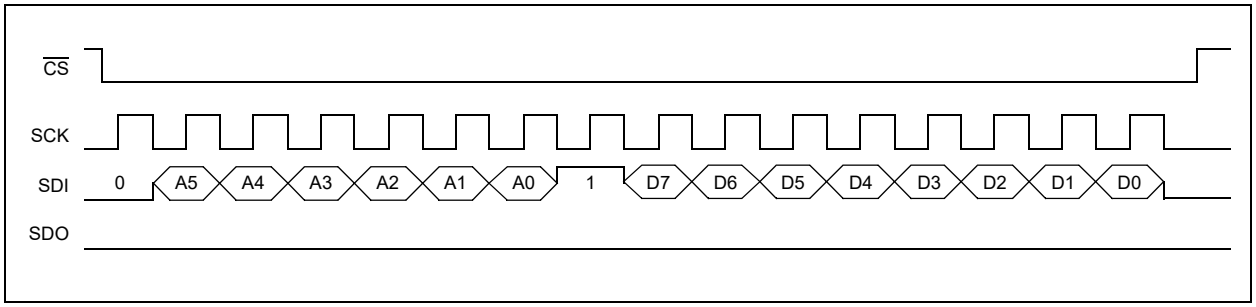


FIGURE 2-8: SHORT ADDRESS WRITE



2.14.2 LONG ADDRESS REGISTER INTERFACE

The long address memory space contains control registers and FIFOs with a 10-bit address range of 0x000 to 0x38F. Figure 2-9 shows a long address read and Figure 2-10 shows a long address write. The 12-bit SPI transfer begins with a '1' to indicate a long address transaction. It is followed by the 10-bit register address, Most Significant bit (MSb) first. The 12th bit indicates if it is a read ('0') or write ('1') transaction.

FIGURE 2-9: LONG ADDRESS READ

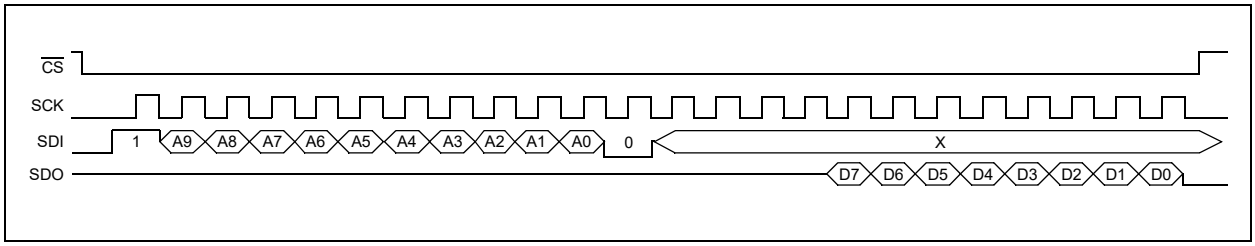
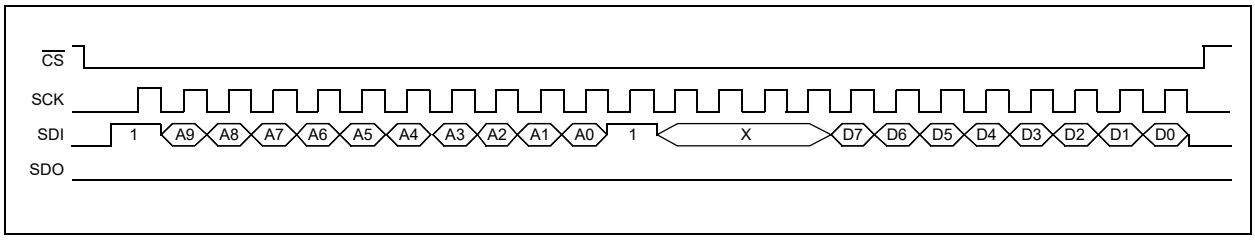


FIGURE 2-10: LONG ADDRESS WRITE



2.15 Control Register Description

Control registers provide control, status and device addressing for MRF24J40 operations. The following figures, tables and register definitions describe the control register operation.

2.15.1 CONTROL REGISTER MAP

FIGURE 2-11: SHORT ADDRESS CONTROL REGISTER MAP FOR MRF24J40

0x00	RXMCR	0x10	ORDER	0x20	ESLOTG67	0x30	RXSR
0x01	PANIDL	0x11	TXMCR	0x21	TXPEND	0x31	INTSTAT
0x02	PANIDH	0x12	ACKTMOUT	0x22	WAKECON	0x32	INTCON
0x03	SADRL	0x13	ESLOTG1	0x23	FRMOFFSET	0x33	GPIO
0x04	SADRH	0x14	SYMTICKL	0x24	TXSTAT	0x34	TRISGPIO
0x05	EADR0	0x15	SYMTICKH	0x25	TXBCON1	0x35	SLPACK
0x06	EADR1	0x16	PACON0	0x26	GATECLK	0x36	RFCTL
0x07	EADR2	0x17	PACON1	0x27	TXTIME	0x37	SECCR2
0x08	EADR3	0x18	PACON2	0x28	HSYMTMRL	0x38	BBREG0
0x09	EADR4	0x19	Reserved	0x29	HSYMTMRH	0x39	BBREG1
0x0A	EADR5	0x1A	TXBCON0	0x2A	SOFTRST	0x3A	BBREG2
0x0B	EADR6	0x1B	TXNCON	0x2B	Reserved	0x3B	BBREG3
0x0C	EADR7	0x1C	TXG1CON	0x2C	SECCON0	0x3C	BBREG4
0x0D	RXFLUSH	0x1D	TXG2CON	0x2D	SECCON1	0x3D	Reserved
0x0E	Reserved	0x1E	ESLOTG23	0x2E	TXSTBL	0x3E	BBREG6
0x0F	Reserved	0x1F	ESLOTG45	0x2F	Reserved	0x3F	CCAEDTH

FIGURE 2-12: LONG ADDRESS CONTROL REGISTER MAP FOR MRF24J40

0x200	RFCON0	0x210	RSSI	0x220	SLPCON1	ox230	ASSOEADR0	0x240	UPNONCE0
0x201	RFCON1	0x211	SLPCON0	0x221	Reserved	0x231	ASSOEADR1	0x241	UPNONCE1
0x202	RFCON2	0x212	Reserved	0x222	WAKETIMEL	0x232	ASSOEADR2	0x242	UPNONCE2
0x203	RFCON3	0x213	Reserved	0x223	WAKETIMEH	0x233	ASSOEADR3	0x243	UPNONCE3
0x204	Reserved	0x214	Reserved	0x224	REMCNTL	0x234	ASSOEADR4	0x244	UPNONCE4
0x205	RFCON5	0x215	Reserved	0x225	REMCNTH	0x235	ASSOEADR5	0x245	UPNONCE5
0x206	RFCON6	0x216	Reserved	0x226	MAINCNT0	0x236	ASSOEADR6	0x246	UPNONCE6
0x207	RFCON7	0x217	Reserved	0x227	MAINCNT1	0x237	ASSOEADR7	0x247	UPNONCE7
0x208	RFCON8	0x218	Reserved	0x228	MAINCNT2	0x238	ASSOSADR0	0x248	UPNONCE8
0x209	SLPCAL0	0x219	Reserved	0x229	MAINCNT3	0x239	ASSOSADR1	0x249	UPNONCE9
0x20A	SLPCAL1	0x21A	Reserved	0x22A	Reserved	0x23A	Reserved	0x24A	UPNONCE10
0x20B	SLPCAL2	0x21B	Reserved	0x22B	Reserved	0x23B	Reserved	0x24B	UPNONCE11
0x20C	Reserved	0x21C	Reserved	0x22C	Reserved	0x23C	Unimplemented	0x24C	UPNONCE12
0x20D	Reserved	0x21D	Reserved	0x22D	Reserved	0x23D	Unimplemented		
0x20E	Reserved	0x21E	Reserved	0x22E	Reserved	0x23E	Unimplemented		
0x20F	RFSTATE	0x21F	Reserved	0x22F	TESTMODE	0x23F	Unimplemented		

2.15.2 CONTROL REGISTER SUMMARY

TABLE 2-6: SHORT ADDRESS CONTROL REGISTER SUMMARY FOR MRF24J40

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on Page:
0x00	RXMCR	r	r	NOACKRSP	r	PANCOORD	COORD	ERRPKT	PROMI	0000 0000	22
0x01	PANIDL	PAN ID Low Byte (PANIDL[7:0])								0000 0000	23
0x02	PANIDH	PAN ID High Byte (PANIDH[15:8])								0000 0000	23
0x03	SADRL	Short Address Low Byte (SADRL[7:0])								0000 0000	24
0x04	SADRH	Short Address High Byte (SADRH[15:8])								0000 0000	24
0x05	EADR0	64-Bit Extended Address bits (EADR0[7:0])								0000 0000	25
0x06	EADR1	64-Bit Extended Address bits (EADR1[15:8])								0000 0000	25
0x07	EADR2	64-Bit Extended Address bits (EADR2[23:16])								0000 0000	25
0x08	EADR3	64-Bit Extended Address bits (EADR3[31:24])								0000 0000	26
0x09	EADR4	64-Bit Extended Address bits (EADR4[39:32])								0000 0000	26
0x0A	EADR5	64-Bit Extended Address bits (EADR5[47:40])								0000 0000	26
0x0B	EADR6	64-Bit Extended Address bits (EADR6[55:48])								0000 0000	27
0x0C	EADR7	64-Bit Extended Address bits (EADR7[63:56])								0000 0000	27
0x0D	RXFLUSH	r	WAKEPOL	WAKEPAD	r	CMDONLY	DATAONLY	BCNONLY	RXFLUSH	0000 0000	28
0x0E	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x0F	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x10	ORDER	BO3	BO2	BO1	BO0	SO3	SO2	SO1	SO0	1111 1111	29
0x11	TXMCR	NOCSMA	BATLIFEXT	SLOTTED	MACMINBE1	MACMINBE0	CSMABF2	CSMABF1	CSMABF0	0001 1100	30
0x12	ACKTMOUT	DRPACK	MAWD6	MAWD5	MAWD4	MAWD3	MAWD2	MAWD1	MAWD0	0011 1001	31
0x13	ESLOTG1	GTS1-3	GTS1-2	GTS1-1	GTS1-0	CAP3	CAP2	CAP1	CAP0	0000 0000	32
0x14	SYMTICKL	TICKP7	TICKP6	TICKP5	TICKP4	TICKP3	TICKP2	TICKP1	TICKP0	0100 0000	33
0x15	SYMTICKH	TXONT6	TXONT5	TXONT4	TXONT3	TXONT2	TXONT1	TXONT0	TICKP8	0101 0001	33
0x16	PACON0	PAONT7	PAONT6	PAONT5	PAONT4	PAONT3	PAONT2	PAONT1	PAONT0	0010 1001	34
0x17	PACON1	r	r	r	PAONTS3	PAONTS2	PAONTS1	PAONTS0	PAONT8	0000 0010	34
0x18	PACON2	FIFOEN	r	TXONTS3	TXONTS2	TXONTS1	TXONTS0	TXONT8	TXONT7	1000 1000	35
0x19	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x1A	TXBCON0	r	r	r	r	r	r	TXBSECEN	TXBTRIG	0000 0000	36
0x1B	TXNCON	r	r	r	FPSTAT	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG	0000 0000	37
0x1C	TXG1CON	TXG1RETRY1	TXG1RETRY0	TXG1SLOT2	TXG1SLOT1	TXG1SLOT0	TXG1ACKREQ	TXG1SECEN	TXG1TRIG	0000 0000	38
0x1D	TXG2CON	TXG2RETRY1	TXG2RETRY0	TXG2SLOT2	TXG2SLOT1	TXG2SLOT0	TXG2ACKREQ	TXG2SECEN	TXG2TRIG	0000 0000	38

Legend: r = reserved

TABLE 2-6: SHORT ADDRESS CONTROL REGISTER SUMMARY FOR MRF24J40 (CONTINUED)

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on Page:
0x1E	ESLOTG23	GTS3-3	GTS3-2	GTS3-1	GTS3-0	GTS2-3	GTS2-2	GTS2-1	GTS2-0	0000 0000	39
0x1F	ESLOTG45	GTS5-3	GTS5-2	GTS5-1	GTS5-0	GTS4-3	GTS4-2	GTS4-1	GTS4-0	0000 0000	39
0x20	ESLOTG67	r	r	r	r	GTS6-3	GTS6-2	GTS6-1	GTS6-0	0000 0000	39
0x21	TXPEND	MLIFS5	MLIFS4	MLIFS3	MLIFS2	MLIFS1	MLIFS0	GTSSWITCH	FPACK	1000 0100	40
0x22	WAKECON	IMMWAKE	REGWAKE	INTL	INTL	INTL	INTL	INTL	INTL	0000 0000	41
0x23	FRMOFFSET	OFFSET7	OFFSET6	OFFSET5	OFFSET4	OFFSET3	OFFSET2	OFFSET1	OFFSET0	0000 0000	42
0x24	TXSTAT	TXNRETRY1	TXNRETRY0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2STAT	TXG1STAT	TXNSTAT	0000 0000	43
0x25	TXBCON1	TXBMSK	$\overline{\text{WU}}$/BCN	RSSINUM1	RSSINUM0	r	r	r	r	0011 0000	44
0x26	GATECLK	r	r	r	r	GTSON	r	r	r	0000 0000	45
0x27	TXTIME	TURNTIME3	TURNTIME2	TURNTIME1	TURNTIME0	r	r	r	r	0100 1000	46
0x28	HSYMTMRL	HSYMTMR7	HSYMTMR6	HSYMTMR5	HSYMTMR4	HSYMTMR3	HSYMTMR2	HSYMTMR1	HSYMTMR0	0000 0000	47
0x29	HSYMTMRH	HSYMTMR15	HSYMTMR14	HSYMTMR13	HSYMTMR12	HSYMTMR11	HSYMTMR10	HSYMTMR09	HSYMTMR08	0000 0000	47
0x2A	SOFTRST	r	r	r	r	r	RSTPWR	RSTBB	RSTMAC	0000 0000	48
0x2B	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x2C	SECCON0	SECIGNORE	SECSTART	RXCIPHER2	RXCIPHER1	RXCIPHER0	TXNCIPHER2	TXNCIPHER1	TXNCIPHER0	0000 0000	49
0x2D	SECCON1	r	TXBCIPHER2	TXBCIPHER1	TXBCIPHER0	r	r	DISDEC	DISENC	0000 0000	50
0x2E	TXSTBL	RFSTBL3	RFSTBL2	RFSTBL1	RFSTBL0	MSIFS3	MSIFS2	MSIFS1	MSIFS0	0111 0101	51
0x2F	Reserved	r	r	r	r	r	r	r	r	0000 0000	—

Legend: r = reserved

TABLE 2-6: SHORT ADDRESS CONTROL REGISTER SUMMARY FOR MRF24J40 (CONTINUED)

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on Page:
0x30	RXSR	r	UPSECERR	BATIND	r	r	SECDECERR	r	r	0000 0000	52
0x31	INTSTAT	SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000	53
0x32	INTCON	SLPIE	WAKEIE	HSYMTMRIE	SECIE	RXIE	TXG2IE	TXG1IE	TXNIE	1111 1111	54
0x33	GPIO	r	r	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	0000 0000	55
0x34	TRISGPIO	r	r	TRISGP5	TRISGP4	TRISGP3	TRISGP2	TRISGP1	TRISGP0	0000 0000	55
0x35	SLPACK	SLPACK	WAKECNT6	WAKECNT5	WAKECNT4	WAKECNT3	WAKECNT2	WAKECNT1	WAKECNT0	0000 0000	56
0x36	RFCTL	r	r	r	WAKECNT8	WAKECNT7	RFRST	RFTXMODE	RFRXMODE	0000 0000	57
0x37	SECCR2	UPDEC	UPENC	TXG2CIPHER2	TXG2CIPHER1	TXG2CIPHER0	TXG1CIPHER2	TXG1CIPHER1	TXG1CIPHER0	0000 0000	58
0x38	BBREG0	r	r	r	r	r	r	r	TURBO	0000 0000	59
0x39	BBREG1	r	r	r	r	r	RXDECINV	r	r	0000 0000	59
0x3A	BBREG2	CCAMODE1	CCAMODE0	CCACSTH3	CCACSTH2	CCACSTH1	CCACSTH0	r	r	0100 1000	60
0x3B	BBREG3	PREVALIDTH3	PREVALIDTH2	PREVALIDTH1	PREVALIDTH0	PREDETTH2	PREDETTH1	PREDETTH0	r	1101 1000	60
0x3C	BBREG4	CSTH2	CSTH1	CSTH0	PRECNT2	PRECNT1	PRECNT0	r	r	1001 1100	61
0x3D	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x3E	BBREG6	RSSIMODE1	RSSIMODE2	r	r	r	r	r	RSSIRDY	0000 0001	61
0x3F	CCAEDTH	CCAEDTH7	CCAEDTH6	CCAEDTH5	CCAEDTH4	CCAEDTH3	CCAEDTH2	CCAEDTH1	CCAEDTH0	0000 0000	62

Legend: r = reserved

TABLE 2-7: LONG ADDRESS CONTROL REGISTER SUMMARY FOR MRF24J40

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on Page:
0x200	RFCON0	CHANNEL3	CHANNEL2	CHANNEL1	CHANNEL0	RFOPT3	RFOPT2	RFOPT1	RFOPT0	0000 0000	63
0x201	RFCON1	VCOOPT7	VCOOPT6	VCOOPT5	VCOOPT4	VCOOPT3	VCOOPT2	VCOOPT1	VCOOPT0	0000 0000	63
0x202	RFCON2	PLLEN	r	r	r	r	r	r	r	0000 0000	64
0x203	RFCON3	TXPWRL1	TXPWRL0	TXPWRS2	TXPWRS1	TXPWRS0	r	r	r	0000 0000	64
0x204	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x205	RFCON5	BATTH3	BATTH2	BATTH1	BATTH0	r	r	r	r	0000 0000	65
0x206	RFCON6	TXFIL	r	r	20MRECVR	BATEN	r	r	r	0000 0000	65
0x207	RFCON7	SLPCLKSEL1	SLPCLKSEL0	r	r	r	r	CLKOUTMODE1	CLKOUTMODE0	0000 0000	66
0x208	RFCON8	r	r	r	RFVCO	r	r	r	r	0000 0000	66
0x209	SLPCAL0	SLPCAL7	SLPCAL6	SLPCAL5	SLPCAL4	SLPCAL3	SLPCAL2	SLPCAL1	SLPCAL0	0000 0000	67
0x20A	SLPCAL1	SLPCAL15	SLPCAL14	SLPCAL13	SLPCAL12	SLPCAL11	SLPCAL10	SLPCAL9	SLPCAL8	0000 0000	67
0x20B	SLPCAL2	SLPCALRDY	r	r	SLPCALEN	SLPCAL19	SLPCAL18	SLPCAL17	SLPCAL16	0000 0000	68
0x20C	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x20D	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x20E	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x20F	RFSTATE	RFSTATE2	RFSTATE1	RFSTATE0	r	r	r	r	r	0000 0000	69
0x210	RSSI	RSSI7	RSSI6	RSSI5	RSSI4	RSSI3	RSSI2	RSSI1	RSSI0	0000 0000	69
0x211	SLPCON0	r	r	r	r	r	r	INTEDGE	$\overline{\text{SLPCLKEN}}$	0000 0000	70
0x212	Reserved	r	r	r	r	r	r	r	r	0000 0000	—

Legend: r = reserved

TABLE 2-7: LONG ADDRESS CONTROL REGISTER SUMMARY FOR MRF24J40 (CONTINUED)

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on Page:
0x213	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x214	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x215	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x216	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x217	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x218	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x219	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x21A	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x21B	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x21C	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x21D	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x21E	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x21F	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x220	SLPCON1	r	r	$\overline{\text{CLKOUTEN}}$	SLPCLKDIV4	SLPCLKDIV3	SLPCLKDIV2	SLPCLKDIV1	SLPCLKDIV0	0000 0000	70
0x221	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x222	WAKETIMEL	WAKETIME7	WAKETIME6	WAKETIME5	WAKETIME4	WAKETIME3	WAKETIME2	WAKETIME1	WAKETIME0	0000 1010	71
0x223	WAKETIMEH	r	r	r	r	r	WAKETIME10	WAKETIME9	WAKETIME8	0000 0000	71
0x224	REMCNTL	REMCNT7	REMCNT6	REMCNT5	REMCNT4	REMCNT3	REMCNT2	REMCNT1	REMCNT0	0000 0000	72
0x225	REMCNTH	REMCNT15	REMCNT14	REMCNT13	REMCNT12	REMCNT11	REMCNT10	REMCNT9	REMCNT8	0000 0000	72
0x226	MAINCNT0	MAINCNT7	MAINCNT6	MAINCNT5	MAINCNT4	MAINCNT3	MAINCNT2	MAINCNT1	MAINCNT0	0000 0000	73
0x227	MAINCNT1	MAINCNT15	MAINCNT14	MAINCNT13	MAINCNT12	MAINCNT11	MAINCNT10	MAINCNT9	MAINCNT8	0000 0000	73
0x228	MAINCNT2	MAINCNT23	MAINCNT22	MAINCNT21	MAINCNT20	MAINCNT19	MAINCNT18	MAINCNT17	MAINCNT16	0000 0000	74
0x229	MAINCNT3	STARTCNT	r	r	r	r	r	MAINCNT25	MAINCNT24	0000 0000	74
0x22A	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x22B	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x22C	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x22D	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x22E	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x22F	TESTMODE	r	r	r	RSSIWAIT1	RSSIWAIT0	TESTMODE2	TESTMODE1	TESTMODE0	0000 0000	75
0x230	ASSOEADR0	ASSOEADR0[7:0]								0000 0000	76
0x231	ASSOEADR1	ASSOEADR1[15:8]								0000 0000	76
0x232	ASSOEADR2	ASSOEADR2[23:16]								0000 0000	77
0x233	ASSOEADR3	ASSOEADR3[31:24]								0000 0000	77
0x234	ASSOEADR4	ASSOEADR4[39:32]								0000 0000	78
0x235	ASSOEADR5	ASSOEADR5[47:40]								0000 0000	78
0x236	ASSOEADR6	ASSOEADR6[55:48]								0000 0000	79
0x237	ASSOEADR7	ASSOEADR7[63:56]								0000 0000	79
0x238	ASSOSADR0	ASSOSADR0[7:0]								0000 0000	80
0x239	ASSOSADR1	ASSOSADR1[15:8]								0000 0000	80
0x23A	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x23B	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x23C	Unimple-mented	—	—	—	—	—	—	—	—	---- ----	—
0x23D	Unimple-mented	—	—	—	—	—	—	—	—	---- ----	—
0x23E	Unimple-mented	—	—	—	—	—	—	—	—	---- ----	—
0x23F	Unimple-mented	—	—	—	—	—	—	—	—	---- ----	—
0x240	UPNONCE0	UPNONCE[7:0]								0000 0000	81
0x241	UPNONCE1	UPNONCE[15:8]								0000 0000	81
0x242	UPNONCE2	UPNONCE[23:16]								0000 0000	82
0x243	UPNONCE3	UPNONCE[31:24]								0000 0000	82
0x244	UPNONCE4	UPNONCE[39:32]								0000 0000	83
0x245	UPNONCE5	UPNONCE[47:40]								0000 0000	83

Legend: r = reserved

TABLE 2-7: LONG ADDRESS CONTROL REGISTER SUMMARY FOR MRF24J40 (CONTINUED)

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on Page:
0x246	UPNONCE6	UPNONCE[55:48]								0000 0000	84
0x247	UPNONCE7	UPNONCE[63:56]								0000 0000	84
0x248	UPNONCE8	UPNONCE[71:64]								0000 0000	85
0x249	UPNONCE9	UPNONCE[79:72]								0000 0000	85
0x24A	UPNONCE10	UPNONCE[87:80]								0000 0000	86
0x24B	UPNONCE11	UPNONCE[95:88]								0000 0000	86
0x24C	UPNONCE12	UPNONCE[103:96]								0000 0000	87

Legend: r = reserved

2.15.3 SHORT ADDRESS CONTROL REGISTERS DETAIL

REGISTER 2-1: RXMCR: RECEIVE MAC CONTROL REGISTER (ADDRESS: 0x00)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	NOACKRSP	r	PANCOORD	COORD	ERRPKT	PROMI
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Reserved:** Maintain as '0'

bit 5 **NOACKRSP:** Automatic Acknowledgement Response bit
- 1 = Disables automatic Acknowledgement response
- 0 = Enables automatic Acknowledgement response. Acknowledgements are returned when they are requested (default).

bit 4 **Reserved:** Maintain as '0'

bit 3 **PANCOORD:** PAN Coordinator bit
- 1 = Set device as PAN coordinator
- 0 = Device is not set as PAN coordinator (default)

bit 2 **COORD:** Coordinator bit
- 1 = Set device as coordinator
- 0 = Device is not set as coordinator (default)

bit 1 **ERRPKT:** Packet Error Mode bit
- 1 = Accept all packets including those with CRC error
- 0 = Accept only packets with good CRC (default)

bit 0 **PROMI:** Promiscuous Mode bit
- 1 = Receive all packet types with good CRC
- 0 = Discard packet when there is a MAC address mismatch, illegal frame type, dPAN/sPAN or MAC short address mismatch (default)

REGISTER 2-2: PANIDL: PAN ID LOW BYTE REGISTER (ADDRESS: 0x01)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAN ID Low Byte (PANIDL[7:0])							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PANIDL[7:0]:** PAN ID Low Byte bits

REGISTER 2-3: PANIDH: PAN ID HIGH BYTE REGISTER (ADDRESS: 0x02)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAN ID High Byte (PANIDH[15:8])							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PANIDH[15:8]:** PAN ID High Byte bits

REGISTER 2-4: SADRL: SHORT ADDRESS LOW BYTE REGISTER (ADDRESS: 0x03)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Short Address Low Byte (SADRL[7:0])							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **SADRL[7:0]:** Short Address Low Byte bits

REGISTER 2-5: SADRH: SHORT ADDRESS HIGH BYTE REGISTER (ADDRESS: 0x04)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Short Address High Byte (SADRH[15:8])							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **SADRH[15:8]:** Short Address High Byte bits

REGISTER 2-6: EADR0: EXTENDED ADDRESS 0 REGISTER (ADDRESS: 0x05)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
64-Bit Extended Address bits (EADR[7:0])							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EADR[7:0]:** 64-Bit Extended Address bits

REGISTER 2-7: EADR1: EXTENDED ADDRESS 1 REGISTER (ADDRESS: 0x06)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
64-Bit Extended Address bits (EADR[15:8])							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EADR[15:8]:** 64-Bit Extended Address bits

REGISTER 2-8: EADR2: EXTENDED ADDRESS 2 REGISTER (ADDRESS: 0x07)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
64-Bit Extended Address bits (EADR[23:16])							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EADR[23:16]:** 64-Bit Extended Address bits

REGISTER 2-9: EADR3: EXTENDED ADDRESS 3 REGISTER (ADDRESS: 0x08)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
64-Bit Extended Address bits (EADR[31:24])							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EADR[31:24]:** 64-Bit Extended Address bits

REGISTER 2-10: EADR4: EXTENDED ADDRESS 4 REGISTER (ADDRESS: 0x09)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
64-Bit Extended Address bits (EADR[39:32])							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EADR[39:32]:** 64-Bit Extended Address bits

REGISTER 2-11: EADR5: EXTENDED ADDRESS 5 REGISTER (ADDRESS: 0x0A)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
64-Bit Extended Address bits (EADR[47:40])							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EADR[47:40]:** 64-Bit Extended Address bits

REGISTER 2-12: EADR6: EXTENDED ADDRESS 6 REGISTER (ADDRESS: 0x0B)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
64-Bit Extended Address bits (EADR[55:48])							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EADR[55:48]:** 64-Bit Extended Address bits

REGISTER 2-13: EADR7: EXTENDED ADDRESS 7 REGISTER (ADDRESS: 0x0C)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
64-Bit Extended Address bits (EADR[63:56])							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EADR[63:56]:** 64-Bit Extended Address bits

REGISTER 2-14: RXFLUSH: RECEIVE FIFO FLUSH REGISTER (ADDRESS: 0x0D)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	W-0
r	WAKEPOL	WAKEPAD	r	CMDONLY	DATAONLY	BCNONLY	RXFLUSH
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Reserved:** Maintain as '0'

bit 6 **WAKEPOL:** Wake Signal Polarity bit
- 1 = Wake signal polarity is active-high
- 0 = Wake signal polarity is active-low (default)

bit 5 **WAKEPAD:** Wake I/O Pin Enable bit
- 1 = Enable wake I/O pin
- 0 = Disable wake I/O pin (default)

bit 4 **Reserved:** Maintain as '0'

bit 3 **CMDONLY:** Command Frame Receive bit
- 1 = Only command frames are received, all other frames are filtered out
- 0 = All valid frames are received (default)

bit 2 **DATAONLY:** Data Frame Receive bit
- 1 = Only data frames are received, all other frames are filtered out
- 0 = All valid frames are received (default)

bit 1 **BCNONLY:** Beacon Frame Receive bit
- 1 = Only beacon frames are received, all other frames are filtered out
- 0 = All valid frames are received (default)

bit 0 **RXFLUSH:** Reset Receive FIFO Address Pointer bit
- 1 = Resets the RXFIFO Address Pointer to zero. RXFIFO data is not modified. Bit is automatically cleared to '0' by hardware.

REGISTER 2-15: ORDER: BEACON AND SUPERFRAME ORDER REGISTER (ADDRESS: 0x10)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
BO3(1)	BO2(1)	BO1(1)	BO0(1)	SO3(1)	SO2(1)	SO1(1)	SO0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **BO[3:0]:** Beacon Order bits (`macBeaconOrder`)(1)
Specifies how often the coordinator will transmit a beacon.(2)
`1111` = The coordinator will not transmit a beacon and the Superframe Order (SO) parameter value is ignored (default)
`1110` = 14
•
•
•
`0000` = 0

bit 3-0 **SO[3:0]:** Superframe Order bits (`macSuperframeOrder`)(1)
Specifies the length of the active portion of the superframe, including the beacon frame.(2)
`1111` = The superframe will not be active following the beacon (i.e., no active portion in the superframe (default))
`1110` = 14
•
•
•
`0000` = 0

Note 1: Refer to IEEE 802.15.4™-2003 Standard, Section 7.5.1.1 "Superframe Structure".
2: PANs that wish to use the superframe structure shall set `macBeaconOrder` to a value between 0 and 14 and `macSuperframeOrder` to a value between 0 and the value of `macBeaconOrder` (i.e., $0 \le SO \le BO \le 14$).

REGISTER 2-16: TXMCR: CSMA-CA MODE CONTROL REGISTER (ADDRESS: 0x11)

R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
NOCSMA	BATLIFEXT	SLOTTED	MACMINBE1	MACMINBE0	CSMABF2	CSMABF1	CSMABF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **NOCSMA:** No Carrier Sense Multiple Access (CSMA) Algorithm bits
1 = Disable CSMA-CA algorithm when transmitting in Unslotted mode with GTSSWITCH (TXPEND 0x21[1]) bit set
0 = Enable CSMA-CA algorithm when transmitting in Unslotted mode with GTSSWITCH (TXPEND 0x21[1]) bit set (default)

bit 6 **BATLIFEXT:** Battery Life Extension Mode bit (macBattLifeExt)
1 = Enable
0 = Disable (default)

bit 5 **SLOTTED:** Slotted CSMA-CA Mode bit
1 = Enable Slotted CSMA-CA mode
0 = Disable Slotted CSMA-CA mode (default)

bit 4-3 **MACMINBE[1:0]:** MAC Minimum Backoff Exponent bits (macMinBE)
The minimum value of the backoff exponent in the CSMA-CA algorithm. Note that if this value is set to '0', collision avoidance is disabled.(1)
Default: 0x3.

bit 2-0 **CSMABF[2:0]:** CSMA Backoff bits (macMaxCSMABackoff)
The maximum number of backoffs the CSMA-CA algorithm will attempt before declaring a channel access failure.(1)
111 = Undefined
110 = Undefined
101 = 5
100 = 4 (default)
011 = 3
010 = 2
001 = 1
000 = 0

Note 1: Refer to IEEE 802.15.4™-2003 Standard, Table 71 – MAC PIB attributes.

REGISTER 2-17: ACKTMOUT: MAC ACK TIME-OUT DURATION REGISTER (ADDRESS: 0x12)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1
DRPACK	MAWD6(1)	MAWD5(1)	MAWD4(1)	MAWD3(1)	MAWD2(1)	MAWD1(1)	MAWD0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **DRPACK:** Data Request Pending Acknowledgement bit(1)
Sets or clears the frame pending bit in the Acknowledgement frame for a received data request MAC command.
1 = Sets frame pending bit
0 = Clears frame pending bit

bit 6-0 **MAWD[6:0]:** macAckWaitDuration bits(2)
The maximum number of symbols to wait for an Acknowledgment frame to arrive following a transmitted data or MAC command frame. Units: Symbol period (16 μs). Default value: 0x39.

Note 1: Refer to IEEE 802.15.4™-2003 Standard, Section 5.4.2.2 "Data Transfer from a Coordinator" and Section 7.3 "MAC Command Frames".

2: Refer to IEEE 802.15.4™-2003 Standard, Table 71: MAC PIB Attributes.

REGISTER 2-18: ESLOTG1: GTS1 AND CAP END SLOT REGISTER (ADDRESS: 0x13)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GTS1-3	GTS1-2	GTS1-1	GTS1-0	CAP3	CAP2	CAP1	CAP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **GTS1-[3:0]:** End Slot of 1st GTS bits
1111 = 15
•
•
•
0000 = 0 (default)

bit 3-0 **CAP[3:0]:** Contention Access Period (CAP) End Slot bits
1111 = 15
•
•
•
0000 = 0 (default)

REGISTER 2-19: SYMTICKL: SYMBOL PERIOD TICK LOW BYTE REGISTER (ADDRESS: 0x14)

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TICKP7	TICKP6	TICKP5	TICKP4	TICKP3	TICKP2	TICKP1	TICKP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **TICKP[7:0]:** Symbol Period Tick bits

Number of ticks to define a symbol period. Tick period is based on the system clock frequency of 20 MHz. TICKP is a 9-bit value. The TICKP8 bit is located in SYMTICKH[0].
Units: tick (50 ns). Default value = 0x140 (320 * 50 ns = 16 μs).

REGISTER 2-20: SYMTICKH: SYMBOL PERIOD TICK HIGH BYTE REGISTER (ADDRESS: 0x15)

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
TXONT6(1)	TXONT5(1)	TXONT4(1)	TXONT3(1)	TXONT2(1)	TXONT1(1)	TXONT0(1)	TICKP8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 **TXONT[6:0]:** Transmitter Enable On Time Tick bits(1)

Transmitter on time before beginning of packet. TXONT is a 9-bit value. The TXONT[8:7] bits are located in PACON2[1:0]. Units: tick (50 ns). Default value = 0x028 (40 * 50 ns = 2 μs).

bit 0 **TICKP8:** Symbol Period Tick bit

Number of ticks to define a symbol period. Tick period is based on the system clock frequency of 20 MHz. TICKP is a 9-bit value. The TICKP[7:0] bits are located in SYMTICKL[7:0].
Units: tick (50 ns). Default value = 0x140 (320 * 50 ns = 16 μs).

Note 1: Refer to Figure 4-4 for timing diagram.

REGISTER 2-21: PACON0: POWER AMPLIFIER CONTROL 0 REGISTER (ADDRESS: 0x16)

R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1
PAONT7(1)	PAONT6(1)	PAONT5(1)	PAONT4(1)	PAONT3(1)	PAONT2(1)	PAONT1(1)	PAONT0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PAONT[7:0]:** Power Amplifier Enable On Time Tick bits(1)
Power amplifier on time before beginning of packet. PAONT is a 9-bit value. The PAONT8 bit is located in PACON1[0]. Units: tick (50 ns). Default value = 0x029 (41 * 50 ns = 2.05 μs).

Note 1: Refer to Figure 4-4 for timing diagram.

REGISTER 2-22: PACON1: POWER AMPLIFIER CONTROL 1 REGISTER (ADDRESS: 0x17)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
r	r	r	PAONTS3(1)	PAONTS2(1)	PAONTS1(1)	PAONTS0(1)	PAONT8(1)
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Reserved:** Maintain as '0'

bit 4-1 **PAONTS[3:0]:** Power Amplifier Enable On Time Symbol bits(1)
Power amplifier on time before beginning of packet. Units: symbol period (16 μs).
Minimum value: 0x1 (default) (1 * 16 μs = 16 μs).

bit 0 **PAONT8:** Power Amplifier Enable On Time Tick bit(1)
Power amplifier on time before beginning of packet. PAONT is a 9-bit value. The PAONT[7:0] bits are located in PACON0[7:0]. Units: tick (50 ns). Default value = 0x029 (41 * 50 ns = 2.05 μs).

Note 1: Refer to Figure 4-4 for timing diagram.

REGISTER 2-23: PACON2: POWER AMPLIFIER CONTROL 2 REGISTER (ADDRESS: 0x18)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
FIFOEN	r	TXONTS3(1)	TXONTS2(1)	TXONTS1(1)	TXONTS0(1)	TXONT8(1)	TXONT7(1)
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FIFOEN:** FIFO Enable bit
1 = Enabled (default). Always maintain this bit as a '1'.

bit 6 **Reserved:** Maintain as '0'

bit 5-2 **TXONTS[3:0]:** Transmitter Enable On Time Symbol bits(1)
Transmitter on time before beginning of packet. Units: symbol period (16 μs).
Minimum value: 0x1. Default value: 0x2 (2 * 16 μs = 32 μs). Recommended value: 0x6 (6 * 16 μs = 96 μs).

bit 1-0 **TXONT[8:7]:** Transmitter Enable On Time Tick bits(1)
Transmitter on time before beginning of packet. TXONT is a 9-bit value. TXONT[6:0] bits are located in SYMTICKH[7:1]. Units: tick (50 ns). Default value = 0x028 (40 * 50 ns = 2 μs).

Note 1: Refer to Figure 4-4 for timing diagram.

REGISTER 2-24: TXBCON0: TRANSMIT BEACON FIFO CONTROL 0 REGISTER (ADDRESS: 0x1A)

R-0	R-0	R-0	R-0	R-0	R-0	R/W-0	W-0
r	r	r	r	r	r	TXBSECEN	TXBTRIG
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Reserved:** Maintain as '0'

bit 1 **TXBSECEN:** TX Beacon FIFO Security Enabled bit
1 = Security enabled
0 = Security disabled (default)

bit 0 **TXBTRIG:** Transmit Frame in TX Beacon FIFO bit
1 = Transmit the frame in the TX Beacon FIFO; bit is automatically cleared by hardware

REGISTER 2-25: TXNCON: TRANSMIT NORMAL FIFO CONTROL REGISTER (ADDRESS: 0x1B)

R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	W-0
r	r	r	FPSTAT(1)	INDIRECT(4)	TXNACKREQ(2,4)	TXNSECEN(3,4)	TXNTRIG
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Reserved:** Maintain as '0'

bit 4 **FPSTAT:** Frame Pending Status bit(1)

Status of the frame pending bit in the received Acknowledgement frame.
1 = Sets frame pending bit
0 = Clears frame pending bit

bit 3 **INDIRECT:** Activate Indirect Transmission bit (coordinator only)(4)

1 = Indirect transmission enabled
0 = Indirect transmission disabled (default)

bit 2 **TXNACKREQ:** TX Normal FIFO Acknowledgement Request bit(2,4)

Transmit a frame with Acknowledgement frame expected. If Acknowledgement is not received, retransmit.
1 = Acknowledgement requested
0 = No Acknowledgement requested (default)

bit 1 **TXNSECEN:** TX Normal FIFO Security Enabled bit(3,4)

1 = Security enabled
0 = Security disabled (default)

bit 0 **TXNTRIG:** Transmit Frame in TX Normal FIFO bit

1 = Transmit the frame in the TX Normal FIFO; bit is automatically cleared by hardware

Note 1: Refer to IEEE 802.15.4™-2003 Standard, Section 7.2.1.1.3 "Frame Pending Subfield".
2: Refer to IEEE 802.15.4-2003 Standard, Section 7.2.1.1.4 "Acknowledgement Request Subfield".
3: Refer to IEEE 802.15.4-2003 Standard, Section 7.2.1.1.2 "Security Enabled Subfield".
4: Bit is cleared at the next triggering of TXN FIFO.

REGISTER 2-26: TXG1CON: GTS1 FIFO CONTROL REGISTER (ADDRESS: 0x1C)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	W-0
TXG1RETRY1	TXG1RETRY0	TXG1SLOT2	TXG1SLOT1	TXG1SLOT0	TXG1ACKREQ	TXG1SECEN	TXG1TRIG
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **TXG1RETRY[1:0]:** TX GTS1 FIFO Retry Times bits
Write: retry times of packet
Read: number of retry times of the successfully transmitted packet

bit 5-3 **TXG1SLOT[2:0]:** GTS Slot that TX GTS1 FIFO Occupies bits

bit 2 **TXG1ACKREQ:** TX GTS1 FIFO Acknowledgement Request bit
Transmit a frame with Acknowledgement frame expected. If Acknowledgement is not received, retransmit.
1 = Acknowledgement requested
0 = No Acknowledgement requested (default)

bit 1 **TXG1SECEN:** TX GTS1 FIFO Security Enabled bit
1 = Security enabled
0 = Security disabled (default)

bit 0 **TXG1TRIG:** Transmit Frame in TX GTS1 FIFO bit
1 = Transmit the frame in the TX GTS1 FIFO; bit is automatically cleared by hardware

REGISTER 2-27: TXG2CON: GTS2 FIFO CONTROL REGISTER (ADDRESS: 0x1D)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	W-0
TXG2RETRY1	TXG2RETRY0	TXG2SLOT2	TXG2SLOT1	TXG2SLOT0	TXG2ACKREQ	TXG2SECEN	TXG2TRIG
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **TXG2RETRY[1:0]:** TX GTS2 FIFO Retry Times bits
Write: retry times of packet
Read: number of retry times of the successfully transmitted packet

bit 5-3 **TXG2SLOT[2:0]:** GTS Slot that TX GTS2 FIFO Occupies bits

bit 2 **TXG2ACKREQ:** TX GTS2 FIFO Acknowledgement Request bit
Transmit a frame with Acknowledgement frame expected. If Acknowledgement is not received, retransmit.
1 = Acknowledgement requested
0 = No Acknowledgement requested (default)

bit 1 **TXG2SECEN:** TX GTS2 FIFO Security Enabled bit
1 = Security enabled
0 = Security disabled (default)

bit 0 **TXG2TRIG:** Transmit Frame in TX GTS2 FIFO bit
1 = Transmit the frame in the TX GTS2 FIFO; bit is automatically cleared by hardware

REGISTER 2-28: ESLOTG23: END SLOT OF GTS3 AND GTS2 REGISTER (ADDRESS: 0x1E)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GTS3-3	GTS3-2	GTS3-1	GTS3-0	GTS2-3	GTS2-2	GTS2-1	GTS2-0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **GTS3-[3:0]:** End Slot of 3rd GTS bits

bit 3-0 **GTS2-[3:0]:** End Slot of 2nd GTS bits

REGISTER 2-29: ESLOTG45: END SLOT OF GTS5 AND GTS4 REGISTER (ADDRESS: 0x1F)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GTS5-3	GTS5-2	GTS5-1	GTS5-0	GTS4-3	GTS4-2	GTS4-1	GTS4-0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **GTS5-[3:0]:** End Slot of 5th GTS bits

bit 3-0 **GTS4-[3:0]:** End Slot of 4th GTS bits

REGISTER 2-30: ESLOTG67: END SLOT OF GTS6 REGISTER (ADDRESS: 0x20)

R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	r	r	GTS6-3	GTS6-2	GTS6-1	GTS6-0
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Reserved:** Maintain as '0'

bit 3-0 **GTS6-[3:0]:** End Slot of 6th GTS bits
If 7th GTS exists, the end slot must be 15.

REGISTER 2-31: TXPEND: TX DATA PENDING REGISTER (ADDRESS: 0x21)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
MLIFS5	MLIFS4	MLIFS3	MLIFS2	MLIFS1	MLIFS0	GTSSWITCH	FPACK(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **MLIFS[5:0]:** Minimum Long Interframe Spacing bits
The minimum number of symbols forming a Long Interframe Spacing (LIFS) period. Refer to IEEE 802.15.4™-2003 Standard, Section 7.5.1.2 "IFS" and Table 70: MAC Sublayer Constants. MLIFS + RFSTBL = `aMinLIFSPeriod` = 40 symbols.
Units: symbol period (16 μs). Default value: 0x21. Recommended values: MLIFS = 0x1F and RFSTBL = 0x9.

bit 1 **GTSSWITCH:** Continue TX GTS FIFO Switch in CFP bit
`1` = GTS1 and GTS2 FIFO will toggle with each other during CFP
`0` = GTS1 and GTS2 FIFO will stop toggling with each other if the transmission fails (default)

bit 0 **FPACK:** Frame Pending bit in the Acknowledgement Frame bit(1)
Sets or clears the frame pending bit in the Acknowledgement frame.
`1` = Sets frame pending bit
`0` = Clears frame pending bit

Note 1: Refer to IEEE 802.15.4™-2003 Standard, Section 7.2.1.1.3 "Frame Pending Subfield" and Section 7.2.2.3.1 "Acknowledgement Frame MHR Fields".

REGISTER 2-32: WAKECON: WAKE CONTROL REGISTER (ADDRESS: 0x22)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IMMWAKE	REGWAKE	INTL	INTL	INTL	INTL	INTL	INTL
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IMMWAKE:** Immediate Wake-up Mode Enable bit
1 = Enable Immediate Wake-up mode
0 = Disable Immediate Wake-up mode (default)

bit 6 **REGWAKE:** Register Wake-up Signal bit
Host processor should set to '1', then clear to '0', to perform wake-up.

bit 5-0 **INTL[5:0]:** Interval to Start Beacon(1)
For Beacon-Enabled mode the timing interval between triggering slotted mode and the first time to transmit beacon.
Default Value: 0x00.

Note 1: Refer to Section 3.8.1.4 "Configuring Beacon-Enabled PAN Coordinator" for more information.

REGISTER 2-33: FRMOFFSET: SUPERFRAME COUNTER OFFSET TO ALIGN BEACON REGISTER (ADDRESS: 0x23)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OFFSET7(1)	OFFSET6(1)	OFFSET5(1)	OFFSET4(1)	OFFSET3(1)	OFFSET2(1)	OFFSET1(1)	OFFSET0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **OFFSET[7:0]:** Superframe Counter Offset for Align Air Slot Boundary bits(1)
For Beacon-Enabled mode device. Default value: 0x00. Recommended value: 0x15.

Note 1: Refer to **Section 3.8.1.6 "Configuring Beacon-Enabled Device"** for more information.

REGISTER 2-34: TXSTAT: TX MAC STATUS REGISTER (ADDRESS: 0x24)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TXNRETRY1	TXNRETRY0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2STAT	TXG1STAT	TXNSTAT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **TXNRETRY[1:0]:** TX Normal FIFO Retry Times bits
Number of retries of the most recent TX Normal FIFO transmission.

bit 5 **CCAFAIL:** Clear Channel Assessment (CCA) Status of Last Transmission bit
1 = Channel busy
0 = Channel Idle

bit 4 **TXG2FNT:** TX GTS2 FIFO Transmission failed due to not enough time before the end of GTS bit
1 = Failed
0 = Succeeded

bit 3 **TXG1FNT:** TX GTS1 FIFO Transmission failed due to not enough time before the end of GTS bit
1 = Failed
0 = Succeeded

bit 2 **TXG2STAT:** TX GTS2 FIFO Release Status bit
1 = Failed, retry count exceeded
0 = Succeeded

bit 1 **TXG1STAT:** TX GTS2 FIFO Release Status bit
1 = Failed, retry count exceeded
0 = Succeeded

bit 0 **TXNSTAT:** TX Normal FIFO Release Status bit
1 = Failed, retry count exceeded
0 = Succeeded

REGISTER 2-35: TXBCON1: TRANSMIT BEACON CONTROL 1 REGISTER (ADDRESS: 0x25)

R/W-0	R-0	R/W-1	R/W-1	R-0	R-0	R-0	R-0
TXBMSK	$\overline{WU}$/BCN	RSSINUM1	RSSINUM0	r	r	r	r
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TXBMSK:** TX Beacon FIFO Interrupt Mask bit
1 = TX Beacon FIFO interrupt is masked
0 = TX Beacon FIFO interrupt is not masked (default)

bit 6 **$\overline{WU}$/BCN:** $\overline{Wake\text{-}up}$/Beacon Interrupt Status bit
Indicates if the WAKEIF interrupt was due to beacon start or wake-up.
1 = Beacon start interrupt
0 = Wake-up interrupt

bit 5-4 **RSSINUM[1:0]:** RSSI Average Symbols bits
11 = 8 symbols (default)
10 = 4 symbols
01 = 2 symbols
00 = 1 symbol

bit 3-0 **Reserved:** Maintain as '0'

REGISTER 2-36: GATECLK: GATED CLOCK CONTROL REGISTER (ADDRESS: 0x26)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	r	r	GTSON	r	r	r
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Reserved:** Maintain as '0'

bit 3 **GTSON:** GTS FIFO Clock Enable bit
1 = Enabled
0 = Disabled (default)

bit 2-0 **Reserved:** Maintain as '0'

REGISTER 2-37: TXTIME: TX TURNAROUND TIME REGISTER (ADDRESS: 0x27)

R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
TURNTIME3	TURNTIME2	TURNTIME1	TURNTIME0	r	r	r	r
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **TURNTIME[3:0]:** Turnaround Time bits
Transmission to reception and reception to transmission turnaround time. Refer to IEEE 802.15.4™-2003 Standard, Table 18: PHY Constants and Section 7.5.6.4.2 "Acknowledgment".
TURNTIME + RFSTBL = `aTurnaroundTime` = 12 symbols.
Units: symbol period (16 μs). Default value: 0x4. Minimum value: 0x2.
Recommended values: TURNTIME = 0x3 and RFSTBL = 0x9.

bit 3-0 **Reserved:** Maintain as 0x8

REGISTER 2-38: HSYMTMRL: HALF SYMBOL TIMER LOW BYTE REGISTER (ADDRESS: 0x28)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HSYMTMR7	HSYMTMR6	HSYMTMR5	HSYMTMR4	HSYMTMR3	HSYMTMR2	HSYMTMR1	HSYMTMR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **HSYMTMR[7:0]:** Half Symbol Timer Low Byte bits
Units: 8 μs.

REGISTER 2-39: HSYMTMRH: HALF SYMBOL TIMER HIGH BYTE REGISTER (ADDRESS: 0x29)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HSYMTMR15	HSYMTMR14	HSYMTMR13	HSYMTMR12	HSYMTMR11	HSYMTMR10	HSYMTMR09	HSYMTMR08
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **HSYMTMR[15:8]:** Half Symbol Timer High Byte bits
Units: 8 μs.

REGISTER 2-40: SOFTRST: SOFTWARE RESET REGISTER (ADDRESS: 0x2A)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	W-0	W-0	W-0
r	r	r	r	r	RSTPWR	RSTBB	RSTMAC
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Reserved:** Maintain as '0'

bit 2 **RSTPWR:** Power Management Reset bit
1 = Reset power management circuitry (bit is automatically cleared to '0' by hardware)

bit 1 **RSTBB:** Baseband Reset bit
1 = Reset baseband circuitry (bit is automatically cleared to '0' by hardware)

bit 0 **RSTMAC:** MAC Reset bit
1 = Reset MAC circuitry (bit is automatically cleared to '0' by hardware)

REGISTER 2-41: SECCON0: SECURITY CONTROL 0 REGISTER (ADDRESS: 0x2C)

W-0	W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SECIGNORE	SECSTART	RXCIPHER2	RXCIPHER1	RXCIPHER0	TXNCIPHER2	TXNCIPHER1	TXNCIPHER0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SECIGNORE:** RX Security Decryption Ignore bit
1 = Ignore decryption process

bit 6 **SECSTART:** RX Security Decryption Start bit
1 = Start decryption process

bit 5-3 **RXCIPHER[2:0]:** RX FIFO Security Suite Select bits
111 = AES-CBC-MAC-32
110 = AES-CBC-MAC-64
101 = AES-CBC-MAC-128
100 = AES-CCM-32
011 = AES-CCM-64
010 = AES-CCM-128
001 = AES-CTR
000 = None (default)

bit 2-0 **TXNCIPHER[2:0]:** TX Normal FIFO Security Suite Select bits
111 = AES-CBC-MAC-32
110 = AES-CBC-MAC-64
101 = AES-CBC-MAC-128
100 = AES-CCM-32
011 = AES-CCM-64
010 = AES-CCM-128
001 = AES-CTR
000 = None (default)

REGISTER 2-42: SECCON1: SECURITY CONTROL 1 REGISTER (ADDRESS: 0x2D)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	TXBCIPHER2	TXBCIPHER1	TXBCIPHER0	r	r	DISDEC	DISENC
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Reserved:** Read as '0'

bit 6-4 **TXBCIPHER[2:0]:** TX Beacon FIFO Security Suite Select bits
111 = AES-CBC-MAC-32
110 = AES-CBC-MAC-64
101 = AES-CBC-MAC-128
100 = AES-CCM-32
011 = AES-CCM-64
010 = AES-CCM-128
001 = AES-CTR
000 = None (default)

bit 3-2 **Reserved:** Read as '0'

bit 1 **DISDEC:** Disable Decryption Function bit
1 = Will not generate a security interrupt if security enabled bit is set in the MAC header

bit 0 **DISENC:** Disable Encryption Function bit
1 = Will not encrypt packet if transmit security is enabled

REGISTER 2-43: TXSTBL: TX STABILIZATION REGISTER (ADDRESS: 0x2E)

R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1
RFSTBL3	RFSTBL2	RFSTBL1	RFSTBL0	MSIFS3	MSIFS2	MSIFS1	MSIFS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **RFSTBL[3:0]:** VCO Stabilization Period bits
Units: symbol period (16 μs). Default value: 0x7. Recommended value: 0x9.

bit 3-0 **MSIFS[3:0]:** Minimum Short Interframe Spacing bits
The minimum number of symbols forming a Short Interframe Spacing (SIFS) period. Refer to IEEE 802.15.4™-2003 Standard, Section 7.5.1.2 "IFS" and Table 70: MAC Sublayer Constants.
MSIFS + RFSTBL = `aMinSIFSPeriod` = 12 symbols.
Units: symbol period (16 μs). Default value: 0x5.

REGISTER 2-44: RXSR: RX MAC STATUS REGISTER (ADDRESS: 0x30)

R-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R/W-0
r	UPSECERR	BATIND(1)	r	r	SECDECERR	r	r
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Reserved:** Read as '0'

bit 6 **UPSECERR:** MIC Error in Upper Layer Security Mode bit
1 = MIC error occurred. Write '1' to clear
0 = MIC error did not occur

bit 5 **BATIND:** Battery Low-Voltage Indicator bit(1)
1 = Supply voltage is lower than battery low-voltage threshold
0 = Supply voltage is greater than battery low-voltage threshold

bit 4-3 **Reserved:** Maintain as '0'

bit 2 **SECDECERR:** Security Decryption Error
1 = Security decryption error occurred
0 = Security decryption error did not occur

bit 1-0 **Reserved:** Maintain as '0'

Note 1: Battery low-voltage threshold (BATTH) value set in the RFCON5 (0X205[7:4]) register and the Battery Monitor Enable (BATEN) bit located in the RFCON6 (0x206[3]) register.

REGISTER 2-45: INTSTAT: INTERRUPT STATUS REGISTER (ADDRESS: 0x31)

RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0
SLPIF(1)	WAKEIF(1)	HSYMTMRIF(1)	SECIF(1)	RXIF(1)	TXG2IF(1)	TXG1IF(1)	TXNIF(1)
bit 7							bit 0

Legend:	RC = Read to clear bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SLPIF:** Sleep Alert Interrupt bit(1)
1 = Sleep alert interrupt occurred
0 = No Sleep alert interrupt occurred

bit 6 **WAKEIF:** Wake-up Alert Interrupt bit(1)
1 = A wake-up alert interrupt occurred
0 = No wake-up alert interrupt occurred

bit 5 **HSYMTMRIF:** Half Symbol Timer Interrupt bit(1)
1 = A half symbol timer interrupt occurred
0 = No half symbol timer interrupt occurred

bit 4 **SECIF:** Security Key Request Interrupt bit(1)
1 = A security key request interrupt occurred
0 = No security key request interrupt occurred

bit 3 **RXIF:** RX FIFO Reception Interrupt bit(1)
1 = An RX FIFO reception interrupt occurred
0 = No RX FIFO reception interrupt occurred

bit 2 **TXG2IF:** TX GTS2 FIFO Transmission Interrupt bit(1)
1 = A TX GTS2 FIFO transmission interrupt occurred
0 = No TX GTS2 FIFO transmission interrupt occurred

bit 1 **TXG1IF:** TX GTS1 FIFO Transmission Interrupt bit(1)
1 = A TX GTS1 FIFO transmission interrupt occurred
0 = No TX GTS1 FIFO transmission interrupt occurred

bit 0 **TXNIF:** TX Normal FIFO Release Interrupt bit(1)
1 = A TX Normal FIFO transmission interrupt occurred
0 = No TX Normal FIFO transmission interrupt occurred

Note 1: Interrupt bits are cleared to '0' when the INTSTAT register is read.

REGISTER 2-46: INTCON: INTERRUPT CONTROL REGISTER (ADDRESS: 0x32)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
SLPIE	WAKEIE	HSYMTMRIE	SECIE	RXIE	TXG2IE	TXG1IE	TXNIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SLPIE:** Sleep Alert Interrupt Enable bit
1 = Disables the Sleep alert interrupt (default)
0 = Enables the Sleep alert interrupt

bit 6 **WAKEIE:** Wake-up Alert Interrupt Enable bit
1 = Disables the wake-up alert interrupt (default)
0 = Enables the wake-up alert interrupt

bit 5 **HSYMTMRIE:** Half Symbol Timer Interrupt Enable bit
1 = Disables the half symbol timer interrupt (default)
0 = Enables the half symbol timer interrupt

bit 4 **SECIE:** Security Key Request Interrupt Enable bit
1 = Disables the security key request interrupt (default)
0 = Enable security key request interrupt

bit 3 **RXIE:** RX FIFO Reception Interrupt Enable bit
1 = Disables the RX FIFO reception interrupt (default)
0 = Enables the RX FIFO reception interrupt

bit 2 **TXG2IE:** TX GTS2 FIFO Transmission Interrupt Enable bit
1 = Disables the TX GTS2 FIFO transmission interrupt (default)
0 = Enables the TX GTS2 FIFO transmission interrupt

bit 1 **TXG1IE:** TX GTS1 FIFO Transmission Interrupt Enable bit
1 = Disables the TX GTS1 FIFO transmission interrupt (default)
0 = Enables the TX GTS1 FIFO transmission interrupt

bit 0 **TXNIE:** TX Normal FIFO Transmission Interrupt Enable bit
1 = Disables the TX Normal FIFO transmission interrupt (default)
0 = Enables the TX Normal FIFO transmission interrupt

REGISTER 2-47: GPIO: GPIO PORT REGISTER (ADDRESS: 0x33)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Reserved:** Maintain as '0'

bit 5 **GPIO5:** General Purpose I/O GPIO5 bit

bit 4 **GPIO4:** General Purpose I/O GPIO4 bit

bit 3 **GPIO3:** General Purpose I/O GPIO3 bit

bit 2 **GPIO2:** General Purpose I/O GPIO2 bit

bit 1 **GPIO1:** General Purpose I/O GPIO1 bit

bit 0 **GPIO0:** General Purpose I/O GPIO0 bit

REGISTER 2-48: TRISGPIO: GPIO PIN DIRECTION REGISTER (ADDRESS: 0x34)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	TRISGP5	TRISGP4	TRISGP3	TRISGP2	TRISGP1	TRISGP0
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Reserved:** Maintain as '0'

bit 5 **TRISGP5:** General Purpose I/O GPIO5 Direction bit
1 = Output
0 = Input (default)

bit 4 **TRISGP4:** General Purpose I/O GPIO4 Direction bit
1 = Output
0 = Input (default)

bit 3 **TRISGP3:** General Purpose I/O GPIO3 Direction bit
1 = Output
0 = Input (default)

bit 2 **TRISGP2:** General Purpose I/O GPIO2 Direction bit
1 = Output
0 = Input (default)

bit 1 **TRISGP1:** General Purpose I/O GPIO1 Direction bit
1 = Output
0 = Input (default)

bit 0 **TRISGP0:** General Purpose I/O GPIO0 Direction bit
1 = Output
0 = Input (default)

REGISTER 2-49: SLPACK: SLEEP ACKNOWLEDGEMENT AND WAKE-UP COUNTER REGISTER (ADDRESS: 0x35)

W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SLPACK	WAKECNT6	WAKECNT5	WAKECNT4	WAKECNT3	WAKECNT2	WAKECNT1	WAKECNT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SLPACK:** Sleep Acknowledge bit

1 = Places the MRF24J40 to Sleep (automatically cleared to '0' by hardware)

bit 6-0 **WAKECNT[6:0]:** Wake Count bits

Main oscillator (20 MHz) start-up timer counter bits. WAKECNT is a 9-bit value. WAKECNT[8:7] bits are located in RFCTL[4:3]. Units: Sleep clock (SLPCLK) period.(1) Default value: 0x00. Recommended value: 0x05F.

Note 1: Sleep Clock (SLPCLK) period depends on the Sleep Clock Selection (SLPCLKSEL) RFCON7[7:6] and Sleep Clock Divisor (SLPCLKDIV) SLPCON1[4:0].

REGISTER 2-50: RFCTL: RF MODE CONTROL REGISTER (ADDRESS: 0x36)

W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	r	WAKECNT8	WAKECNT7	RFRST(2)	RFTXMODE	RFRXMODE
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Reserved:** Maintain as '0'

bit 4-3 **WAKECNT[8:7]:** Wake Count bits

Main oscillator (20 MHz) start-up timer counter bits. WAKECNT is a 9-bit value. WAKECNT[6:0] bits are located in SLPACK[6:0]. Units: Sleep clock (SLPCLK) period.(1) Default value: 0x00. Recommended value: 0x05F

bit 2 **RFRST:** RF State Machine Reset bit(2)

1 = Hold RF state machine in Reset
0 = Normal operation of RF state machine

bit 1 **RFTXMODE:** Forces RF Control State Machine to transmit State(3)

bit 0 **RFRXMODE:** Forces RF Control State Machine to receive State

Note 1: Sleep clock (SLPCLK) period depends on the Sleep clock selection (SLPCLKSEL) RFCON7[7:6] and Sleep clock divisor (SLPCLKDIV) SLPCON1[4:0].

2: Perform RF Reset by setting RFRST = 1 and then RFRST = 0. Delay at least 192 μs after performing to allow RF circuitry to calibrate.

3: Recommended sequence RFCTL = 0x06 (reset mode) then RFCTL = 0x02 (transmit mode).

REGISTER 2-51: SECCR2: SECURITY CONTROL 2 REGISTER (ADDRESS: 0x37)

W-0	W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPDEC	UPENC	TXG2CIPHER2	TXG2CIPHER1	TXG2CIPHER0	TXG1CIPHER2	TXG1CIPHER1	TXG1CIPHER0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **UPDEC:** Upper Layer Security Decryption Mode bit
1 = Perform upper layer decryption using TX Normal FIFO. Automatically cleared to '0' when finished.

bit 6 **UPENC:** Upper Layer Security Encryption Mode bit
1 = Perform upper layer encryption using TX Normal FIFO. Automatically cleared to '0' when finished.

bit 5-3 **TXG2CIPHER-[2:0]:** TX GTS2 FIFO Security Suite Select bits
111 = AES-CBC-MAC-32
110 = AES-CBC-MAC-64
101 = AES-CBC-MAC-128
100 = AES-CCM-32
011 = AES-CCM-64
010 = AES-CCM-128
001 = AES-CTR
000 = None (default)

bit 2-0 **TXG1CIPHER-[2:0]:** TX GTS1 FIFO Security Suite Select bits
111 = AES-CBC-MAC-32
110 = AES-CBC-MAC-64
101 = AES-CBC-MAC-128
100 = AES-CCM-32
011 = AES-CCM-64
010 = AES-CCM-128
001 = AES-CTR
000 = None (default)

REGISTER 2-52: BBREG0: BASEBAND 0 REGISTER (ADDRESS: 0x38)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	r	r	r	r	r	TURBO
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 **Reserved:** Maintain as '0'

bit 0 **TURBO:** Turbo Mode Enable bit
1 = Turbo mode (625 kbps)
0 = IEEE 802.15.4™ mode (250 kbps)

REGISTER 2-53: BBREG1: BASEBAND 1 REGISTER (ADDRESS: 0x39)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	r	r	r	RXDECINV	r	r
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Reserved:** Maintain as '0'

bit 2 **RXDECINV:** RX Decode Inversion bit
1 = RX decode symbol sign inverted
0 = RX decode symbol sign not inverted (default)

bit 1-0 **Reserved:** Maintain as '0'

REGISTER 2-54: BBREG2: BASEBAND 2 REGISTER (ADDRESS: 0x3A)

R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
CCAMODE1	CCAMODE0	CCACSTH3	CCACSTH2	CCATCSH1	CCACSTH0	r	r
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **CCAMODE[1:0]:** Clear Channel Assessment (CCA) Mode bits

11 = CCA Mode 3: Carrier sense with energy above threshold. CCA shall report a busy medium only upon the detection of a signal with the modulation and spreading characteristics of IEEE 802.15.4™ with energy above the Energy Detection (ED) threshold.

10 = CCA Mode 1: Energy above threshold. CCA shall report a busy medium upon detecting any energy above the Energy Detection (ED) threshold.

01 = CCA Mode 2: Carrier sense only. CCA shall report a busy medium only upon the detection of a signal with the modulation and spreading characteristics of IEEE 802.15.4. This signal may be above or below the Energy Detection (ED) threshold (default).

00 = Reserved

bit 5-2 **CCACSTH[3:0]:** Clear Channel Assessment (CCA) Carrier Sense (CS) Threshold bits

1111 =
1110 = Recommended value
1101 =
•
•
•
0010 = (default)
0001 =
0000 =

bit 1-0 **Reserved:** Maintain as '0'

REGISTER 2-55: BBREG3: BASEBAND 3 REGISTER (ADDRESS: 0x3B)

R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
PREVALIDTH3	PREVALIDTH2	PREVALIDTH1	PREVALIDTH0	PREDETTH2	PREDETTH1	PREDETTH0	r
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **PREVALIDTH[3:0]:** Preamble Search Energy Valid Threshold bits

1101 = IEEE 802.15.4™ (250 kbps) optimized value (default)
0011 = Turbo mode (625 kbps) optimized value

bit 3-1 **PREDETTH[2:0]:** Preamble Search Energy Detection Threshold bits
Default value: 0x4.

bit 0 **Reserved:** Maintain as '0'

REGISTER 2-56: BBREG4: BASEBAND 4 REGISTER (ADDRESS: 0x3C)

R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
CSTH2	CSTH1	CSTH0	PRECNT2	PRECNT1	PRECNT0	r	r
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **CSTH[2:0]:** Carrier Sense Threshold bits
100 = IEEE 802.15.4™ (250 kbps) optimized value (default)
010 = Turbo mode (625 kbps) optimized value

bit 4-2 **PRECNT[2:0]:** Preamble Counter Threshold bits
111 = Optimized value (default)

bit 1-0 **Reserved:** Maintain as '0'

REGISTER 2-57: BBREG6: BASEBAND 6 REGISTER (ADDRESS: 0x3E)

W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1
RSSIMODE1	RSSIMODE2	r	r	r	r	r	RSSIRDY
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **RSSIMODE1:** RSSI Mode 1 bit
1 = Initiate RSSI calculation (bit is automatically cleared to '0' by hardware)

bit 6 **RSSIMODE2:** RSSI Mode 2 bit
1 = Calculate RSSI for each received packet. The RSSI value is stored in RXFIFO
0 = RSSI calculation is not performed for each received packet (default)

bit 5-1 **Reserved:** Maintain as '0'

bit 0 **RSSIRDY:** RSSI Ready Signal for RSSIMODE1 bit
If RSSIMODE1 = 1, then
1 = RSSI calculation has finished and the RSSI value is ready
0 = RSSI calculation in progress

REGISTER 2-58: CCAEDTH: ENERGY DETECTION THRESHOLD FOR CCA REGISTER (ADDRESS: 0x3F)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCAEDTH7	CCAEDTH6	CCAEDTH5	CCAEDTH4	CCAEDTH3	CCAEDTH2	CCAEDTH1	CCAEDTH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **CCAEDTH[7:0]:** Clear Channel Assessment (CCA) Energy Detection (ED) Mode bits
If the in-band signal strength is greater than the threshold, the channel is busy. The 8-bit value can be mapped to a power level according to RSSI. Refer to **Section 3.6 "Received Signal Strength Indicator (RSSI)/Energy Detection (ED)"**.
Default value: 0x00. Recommended value: 0x60 (approximately -69 dBm).

2.15.4 LONG ADDRESS CONTROL REGISTERS DETAIL

REGISTER 2-59: RFCON0: RF CONTROL 0 REGISTER (ADDRESS: 0x200)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHANNEL3	CHANNEL2	CHANNEL1	CHANNEL0	RFOPT3	RFOPT2	RFOPT1	RFOPT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **CHANNEL[3:0]:** Channel Number bits
0000 = Channel 11 (2405 MHz) (default)
0001 = Channel 12 (2410 MHz)
0010 = Channel 13 (2415 MHz)
…
1111 = Channel 26 (2480 MHz)

bit 3-0 **RFOPT[3:0]:** RF Optimize Control bits
Default value: 0x0. Recommended value: 0x3.

REGISTER 2-60: RFCON1: RF CONTROL 1 REGISTER (ADDRESS: 0x201)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VCOOPT7	VCOOPT6	VCOOPT5	VCOOPT4	VCOOPT3	VCOOPT2	VCOOPT1	VCOOPT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **VCOOPT[7:0]:** VCO Optimize Control bits
Default value: 0x0. Recommended value: 0x2.

REGISTER 2-61: RFCON2: RF CONTROL 2 REGISTER (ADDRESS: 0x202)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLEN(1)	r	r	r	r	r	r	r
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **PLLEN:** PLL Enable bit(1)
1 = Enabled
0 = Disabled (default)

bit 6-0 **Reserved:** Maintain as '0'

Note 1: PLL must be enabled for RF reception or transmission.

REGISTER 2-62: RFCON3: RF CONTROL 3 REGISTER (ADDRESS: 0x203)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXPWRL1	TXPWRL0	TXPWRS2	TXPWRS1	TXPWRS0	r	r	r
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **TXPWRL[1:0]:** Large Scale Control for TX Power bits
11 = -30 dB
10 = -20 dB
01 = -10 dB
00 = 0 dB

bit 5-3 **TXPWRS[2:0]:** Small Scale Control for TX Power bits
111 = -6.3 dB
110 = -4.9 dB
101 = -3.7 dB
100 = -2.8 dB
011 = -1.9 dB
010 = -1.2 dB
001 = -0.5 dB
000 = 0 dB

bit 2-0 **Reserved:** Maintain as '0'

REGISTER 2-63: RFCON5: RF CONTROL 5 REGISTER (ADDRESS: 0x205)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BATTH3(1)	BATTH2(1)	BATTH1(1)	BATTH0(1)	r	r	r	r
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **BATTH[3:0]:** Battery Low-Voltage Threshold bits(1)
1110 = 3.5V
1101 = 3.3V
1100 = 3.2V
1011 = 3.1V
1010 = 2.8V
1001 = 2.7V
1000 = 2.6V
0111 = 2.5V
0110 = Undefined
...
0000 = Undefined

bit 3-0 **Reserved:** Maintain as '0'

Note 1: The Battery Low-Voltage Indicator (BATIND) bit is located in the RXSR (0x30[5]) register and the Battery Monitor Enable (BATEN) bit is located in the RFCON6 (0x206[3]) register.

REGISTER 2-64: RFCON6: RF CONTROL 6 REGISTER (ADDRESS: 0x206)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXFIL	r	r	20MRECVR	BATEN(1)	r	r	r
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TXFIL:** TX Filter Control bit
Default value: '0'. Recommended value: '1'.

bit 6-5 **Reserved:** Maintain as '0'

bit 4 **20MRECVR:** 20 MHz Clock Recovery Control bits
Recovery from Sleep control.
1 = Less than 1 ms (recommended)
0 = Less than 3 ms (default)

bit 3 **BATEN:** Battery Monitor Enable bit(1)
1 = Enabled
0 = Disabled (default)

Note 1: The Battery Low-Voltage Threshold (BATTH) bits are located in the RFCON5 (0x205[7:4]) register and the Battery Low-Voltage Indicator (BATIND) bit is located in the RXSR (0x30[5]) register.

REGISTER 2-64: RFCON6: RF CONTROL 6 REGISTER (ADDRESS: 0x206) (CONTINUED)

bit 2-0 **Reserved:** Maintain as '0'

Note 1: The Battery Low-Voltage Threshold (BATTH) bits are located in the RFCON5 (0x205[7:4]) register and the Battery Low-Voltage Indicator (BATIND) bit is located in the RXSR (0x30[5]) register.

REGISTER 2-65: RFCON7: RF CONTROL 7 REGISTER (ADDRESS: 0x207)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SLPCLKSEL1	SLPCLKSEL0	r	r	r	r	r	r
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SLPCLKSEL[1:0]:** Sleep Clock Selection bits
10 = 100 kHz internal oscillator
01 = 32 kHz external crystal oscillator

bit 5-0 **Reserved:** Maintain as '0'

REGISTER 2-66: RFCON8: RF CONTROL 8 REGISTER (ADDRESS: 0x208)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RFVCO	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Reserved:** Maintain as '0'

bit 4 **RFVCO:** VCO Control bit
Default value: '0'. Recommended value: '1'.

bit 3-0 **Reserved:** Maintain as '0'

REGISTER 2-67: SLPCAL0: SLEEP CALIBRATION 0 REGISTER (ADDRESS: 0x209)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
SLPCAL7	SLPCAL6	SLPCAL5	SLPCAL4	SLPCAL3	SLPCAL2	SLPCAL1	SLPCAL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **SLPCAL[7:0]:** Sleep Calibration Counter bits

20-bit counter to calibrate the Sleep Clock (SLPCLK) period. The counter contains the count of 16 SLPCLK periods. The SLPCLK period depends on the Sleep Clock Selection (SLPCLKSEL), RFCON7[7:6] and Sleep Clock Divisor (SLPCLKDIV) SLPCON1[4:0] bits. Units: tick (50 ns).

REGISTER 2-68: SLPCAL1: SLEEP CALIBRATION 1 REGISTER (ADDRESS: 0x20A)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
SLPCAL15	SLPCAL14	SLPCAL13	SLPCAL12	SLPCAL11	SLPCAL10	SLPCAL9	SLPCAL8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **SLPCAL[15:8]:** Sleep Calibration Counter bits

20-bit counter to calibrate the Sleep Clock (SLPCLK) period. The counter contains the count of 16 SLPCLK periods. The SLPCLK period depends on the Sleep Clock Selection (SLPCLKSEL), RFCON7[7:6] and Sleep Clock Divisor (SLPCLKDIV) SLPCON1[4:0] bits. Units: tick (50 ns).

REGISTER 2-69: SLPCAL2: SLEEP CALIBRATION 2 REGISTER (ADDRESS: 0x20B)

R-0	R/W-0	R/W-0	W-0	R-0	R-0	R-0	R-0
SLPCALRDY	r	r	SLPCALEN	SLPCAL19	SLPCAL18	SLPCAL17	SLPCAL16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SLPCALRDY:** Sleep Calibration Ready bit
1 = Sleep calibration count is complete

bit 6-5 **Reserved:** Maintain as '0'

bit 4 **SLPCALEN:** Sleep Calibration Enable bit
1 = Starts the Sleep calibration counter. Automatically cleared to '0' by hardware

bit 3-0 **SLPCAL[19:16]:** Sleep Calibration Counter bits
20-bit counter to calibrate the Sleep Clock (SLPCLK) period. The counter contains the count of 16 SLPCLK periods. The SLPCLK period depends on the Sleep Clock Selection (SLPCLKSEL), RFCON7[7:6] and Sleep Clock Divisor (SLPCLKDIV) SLPCON1[4:0] bits. Units: tick (50 ns).

REGISTER 2-70: RFSTATE: RF STATE REGISTER (ADDRESS: 0x20F)

R-0	R-0	R-0	U-0	U-0	U-0	U-0	U-0
RFSTATE2	RFSTATE1	RFSTATE0	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **RFSTATE[2:0]:** RF State Machine bits
111 = RTSEL2
110 = RTSEL1
101 = RX
100 = TX
011 = CALVCO
010 = SLEEP
001 = CALFIL
000 = RESET

bit 4-0 **Reserved:** Maintain as '0'

REGISTER 2-71: RSSI: AVERAGED RSSI VALUE REGISTER (ADDRESS: 0x210)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RSSI7(1)	RSSI6(1)	RSSI5(1)	RSSI4(1)	RSSI3(1)	RSSI2(1)	RSSI1(1)	RSSI0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **RSSI[7:0]:** Averaged RSSI Value bits(1)

Note 1: The number of RSSI samples averaged, set by RSSINUMx (0x25[5:4]) bits.

REGISTER 2-72: SLPCON0: SLEEP CLOCK CONTROL 0 REGISTER (ADDRESS: 0x211)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	r	r	r	r	INTEDGE(1)	$\overline{\text{SLPCLKEN}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Reserved:** Maintain as '0'

bit 1 **INTEDGE:** Interrupt Edge Polarity bit(1)
1 = Rising edge
0 = Falling edge (default)

bit 0 **$\overline{\text{SLPCLKEN}}$:** Sleep Clock Enable bit
1 = Disabled
0 = Enabled (default)

Note 1: Ensure that the interrupt polarity matches the interrupt pin polarity on the host microcontroller.

REGISTER 2-73: SLPCON1: SLEEP CLOCK CONTROL 1 REGISTER (ADDRESS: 0x220)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	$\overline{\text{CLKOUTEN}}$	SLPCLKDIV4	SLPCLKDIV3	SLPCLKDIV2	SLPCLKDIV1	SLPCLKDIV0
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Reserved:** Maintain as '0'

bit 5 **$\overline{\text{CLKOUTEN}}$:** CLKOUT Pin Enable bit
The CLKOUT pin 26 feature has been discontinued. It is recommended that it be disabled.
1 = Disable (recommended)
0 = Enable (default)

bit 4-0 **SLPCLKDIV[4:0]:** Sleep Clock Divisor bits
Sleep clock is divided by 2^n, where n = SLPCLKDIV.(1) Default value: 0x00.

Note 1: If the Sleep Clock Selection, SLPCLKSEL (0x207[7:6), is the internal oscillator (100 kHz), set SLPCLKDIV to a minimum value of 0x01.

REGISTER 2-74: WAKETIMEL: WAKE-UP TIME MATCH VALUE LOW REGISTER (ADDRESS: 0x222)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0
WAKETIME7(1)	WAKETIME6(1)	WAKETIME5(1)	WAKETIME4(1)	WAKETIME3(1)	WAKETIME2(1)	WAKETIME1(1)	WAKETIME0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **WAKETIME[7:0]:** Wake Time Match Value bits(1)
WAKETIME is an 11-bit value that is compared with the Main Counter (MAINCNT) to signal the time to enable (wake-up) the 20 MHz main oscillator when the MRF24J40 is using the Sleep mode timers. Default value: 0x00A. Minimum value: 0x001.

Note 1: Rule: WAKETIME > WAKECNT.

REGISTER 2-75: WAKETIMEH: WAKE-UP TIME MATCH VALUE HIGH REGISTER (ADDRESS: 0x223)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	r	r	r	WAKETIME10(1)	WAKETIME9(1)	WAKETIME8(1)
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Reserved:** Maintain as '0'

bit 2-0 **WAKETIME[10:8]:** Wake-up Time Counted by SLPCLK bits(1)
WAKETIME is an 11-bit value that is compared with the Main Counter (MAINCNT) to signal the time to enable (wake-up) the 20 MHz main oscillator when the MRF24J40 is using the Sleep mode timers. Default value: 0x00A. Minimum value: 0x001.

Note 1: Rule: WAKETIME > WAKECNT.

REGISTER 2-76: REMCNTL: REMAIN COUNTER LOW REGISTER (ADDRESS: 0x224)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
REMCNT7	REMCNT6	REMCNT5	REMCNT4	REMCNT3	REMCNT2	REMCNT1	REMCNT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **REMCNT[7:0]:** Remain Counter bits

Remain counter is a 16-bit counter. Together with the main counter times events: Beacon Interval (BI) and inactive period for beacon-enabled devices and Sleep interval for nonbeacon-enabled devices. Units: tick (50 ns).

REGISTER 2-77: REMCNTH: REMAIN COUNTER HIGH REGISTER (ADDRESS: 0x225)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
REMCNT15	REMCNT14	REMCNT13	REMCNT12	REMCNT11	REMCNT10	REMCNT9	REMCNT8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **REMCNT[15:8]:** Remain Counter bits

Remain counter is a 16-bit counter. Together with the main counter times events: Beacon Interval (BI) and inactive period for beacon-enabled devices and Sleep interval for nonbeacon-enabled devices. Units: tick (50 ns).

REGISTER 2-78: MAINCNT0: MAIN COUNTER 0 REGISTER (ADDRESS: 0x226)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MAINCNT7	MAINCNT6	MAINCNT5	MAINCNT4	MAINCNT3	MAINCNT2	MAINCNT1	MAINCNT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **MAINCNT[7:0]:** Main Counter bits

Main counter is a 26-bit counter. Together with the remain counter times events: Beacon Interval (BI) and inactive period for beacon-enabled devices and Sleep interval for nonbeacon-enabled devices. Units: SLPCLK.(1)

Note 1: Sleep Clock (SLPCLK) period depends on the Sleep Clock Selection (SLPCLKSEL) RFCON[7:6] and Sleep Clock Divisor (SLPCLKDIV) CLKCON[4:0] bits.

REGISTER 2-79: MAINCNT1: MAIN COUNTER 1 REGISTER (ADDRESS: 0x227)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MAINCNT15	MAINCNT14	MAINCNT13	MAINCNT12	MAINCNT11	MAINCNT10	MAINCNT9	MAINCNT8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **MAINCNT[15:8]:** Main Counter bits

Main counter is a 26-bit counter. Together with the remain counter times events: Beacon Interval (BI) and inactive period for beacon-enabled devices and Sleep interval for nonbeacon-enabled devices. Units: SLPCLK.(1)

Note 1: Sleep Clock (SLPCLK) period depends on the Sleep Clock Selection (SLPCLKSEL) RFCON[7:6] and Sleep Clock Divisor (SLPCLKDIV) CLKCON[4:0] bits.

REGISTER 2-80: MAINCNT2: MAIN COUNTER 2 REGISTER (ADDRESS: 0x228)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MAINCNT23	MAINCNT22	MAINCNT21	MAINCNT20	MAINCNT19	MAINCNT18	MAINCNT17	MAINCNT16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **MAINCNT[23:16]:** Main Counter bits

Main counter is a 26-bit counter. Together with the remain counter times events: Beacon Interval (BI) and inactive period for beacon-enabled devices and Sleep interval for nonbeacon-enabled devices. Units: SLPCLK.**(1)**

Note 1: Sleep Clock (SLPCLK) period depends on the Sleep Clock Selection (SLPCLKSEL) RFCON[7:6] and Sleep Clock Divisor (SLPCLKDIV) CLKCON[4:0] bits.

REGISTER 2-81: MAINCNT3: MAIN COUNTER 3 REGISTER (ADDRESS: 0x229)

W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STARTCNT	r	r	r	r	r	MAINCNT25	MAINCNT24
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **STARTCNT:** Start Sleep Mode Counters bits

1 = Trigger Sleep mode for Nonbeacon Enable mode (BO = 0xF and Slotted = 0). Bit automatically clears to '0'.

bit 6-2 **Reserved:** Maintain as '0'

bit 1-0 **MAINCNT[25:24]:** Main Counter bits

Main counter is a 26-bit counter. Together with the remain counter times events: Beacon Interval (BI) and inactive period for beacon-enabled devices and Sleep interval for nonbeacon-enabled devices. Units: SLPCLK.**(1)**

Note 1: Sleep Clock (SLPCLK) period depends on the Sleep Clock Selection (SLPCLKSEL) RFCON[7:6] and Sleep Clock Divisor (SLPCLKDIV) CLKCON[4:0] bits.

REGISTER 2-82: TESTMODE: TEST MODE REGISTER (ADDRESS: 0x22F)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
r	r	r	RSSIWAIT1	RSSIWAIT0	TESTMODE2	TESTMODE1	TESTMODE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Reserved:** Maintain as '0'

bit 4-3 **RSSIWAIT[1:0]:** RSSI State Machine Parameter bits
01 = Optimized value (default)

bit 2-0 **TESTMODE[2:0]:** Test Mode bits
111 = GPIO0, GPIO1 and GPIO2 are configured to control an external PA and/or LNA(1)
101 = Single Tone Test mode
000 = Normal operation (default)

Note 1: Refer to **Section 4.2 "External PA/LNA Control"** for more information.

REGISTER 2-83: ASSOEADR0: ASSOCIATED COORDINATOR EXTENDED ADDRESS 0 REGISTER (ADDRESS: 0x230)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASSOEADR7	ASSOEADR6	ASSOEADR5	ASSOEADR4	ASSOEADR3	ASSOEADR2	ASSOEADR1	ASSOEADR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ASSOEADR[7:0]:** 64-Bit Extended Address of Associated Coordinator bits

REGISTER 2-84: ASSOEADR1: ASSOCIATED COORDINATOR EXTENDED ADDRESS 1 REGISTER (ADDRESS: 0x231)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASSOEADR15	ASSOEADR14	ASSOEADR13	ASSOEADR12	ASSOEADR11	ASSOEADR10	ASSOEADR9	ASSOEADR8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ASSOEADR[15:8]:** 64-Bit Extended Address of Associated Coordinator bits

REGISTER 2-85: ASSOEADR2: ASSOCIATED COORDINATOR EXTENDED ADDRESS 2 REGISTER (ADDRESS: 0x232)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASSOEADR23	ASSOEADR22	ASSOEADR21	ASSOEADR20	ASSOEADR19	ASSOEADR18	ASSOEADR17	ASSOEADR16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ASSOEADR[23:16]:** 64-Bit Extended Address of Associated Coordinator bits

REGISTER 2-86: ASSOEADR3: ASSOCIATED COORDINATOR EXTENDED ADDRESS 3 REGISTER (ADDRESS: 0x233)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASSOEADR31	ASSOEADR30	ASSOEADR29	ASSOEADR28	ASSOEADR27	ASSOEADR26	ASSOEADR25	ASSOEADR24
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ASSOEADR[31:24]:** 64-Bit Extended Address of Associated Coordinator bits

REGISTER 2-87: ASSOEADR4: ASSOCIATED COORDINATOR EXTENDED ADDRESS 4 REGISTER (ADDRESS: 0x234)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASSOEADR39	ASSOEADR38	ASSOEADR37	ASSOEADR36	ASSOEADR35	ASSOEADR34	ASSOEADR33	ASSOEADR32
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ASSOEADR[39:32]:** 64-Bit Extended Address of Associated Coordinator bits

REGISTER 2-88: ASSOEADR5: ASSOCIATED COORDINATOR EXTENDED ADDRESS 5 REGISTER (ADDRESS: 0x235)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASSOEADR47	ASSOEADR46	ASSOEADR45	ASSOEADR44	ASSOEADR43	ASSOEADR42	ASSOEADR41	ASSOEADR40
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ASSOEADR[47:40]:** 64-Bit Extended Address of Associated Coordinator bits

REGISTER 2-89: ASSOEADR6: ASSOCIATED COORDINATOR EXTENDED ADDRESS 6 REGISTER (ADDRESS: 0x236)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASSOEADR55	ASSOEADR54	ASSOEADR53	ASSOEADR52	ASSOEADR51	ASSOEADR50	ASSOEADR49	ASSOEADR48
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ASSOEADR[55:48]:** 64-Bit Extended Address of Associated Coordinator bits

REGISTER 2-90: ASSOEADR7: ASSOCIATED COORDINATOR EXTENDED ADDRESS 7 REGISTER (ADDRESS: 0x237)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASSOEADR63	ASSOEADR62	ASSOEADR61	ASSOEADR60	ASSOEADR59	ASSOEADR58	ASSOEADR57	ASSOEADR56
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ASSOEADR[63:56]:** 64-Bit Extended Address of Associated Coordinator bits

REGISTER 2-91: ASSOSADR0: ASSOCIATED COORDINATOR SHORT ADDRESS 0 REGISTER (ADDRESS: 0x238)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASSOSADR7	ASSOSADR6	ASSOSADR5	ASSOSADR4	ASSOSADR3	ASSOSADR2	ASSOSADR1	ASSOSADR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ASSOSADR[7:0]:** 16-Bit Short Address of Associated Coordinator bits

REGISTER 2-92: ASSOSADR1: ASSOCIATED COORDINATOR SHORT ADDRESS 1 REGISTER (ADDRESS: 0x239)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASSOSADR15	ASSOSADR14	ASSOSADR13	ASSOSADR12	ASSOSADR11	ASSOSADR10	ASSOSADR9	ASSOSADR8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ASSOSADR[15:8]:** 16-Bit Short Address of Associated Coordinator bits

REGISTER 2-93: UPNONCE0: UPPER NONCE SECURITY 0 REGISTER (ADDRESS: 0x240)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE7	UPNONCE6	UPNONCE5	UPNONCE4	UPNONCE3	UPNONCE2	UPNONCE1	UPNONCE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[7:0]:** Upper Nonce bits
13-byte nonce value used in security.

REGISTER 2-94: UPNONCE1: UPPER NONCE SECURITY 1 REGISTER (ADDRESS: 0x241)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE15	UPNONCE14	UPNONCE13	UPNONCE12	UPNONCE11	UPNONCE10	UPNONCE9	UPNONCE8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[15:8]:** Upper Nonce bits
13-byte nonce value used in security.

REGISTER 2-95: UPNONCE2: UPPER NONCE SECURITY 2 REGISTER (ADDRESS: 0x242)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE23	UPNONCE22	UPNONCE21	UPNONCE20	UPNONCE19	UPNONCE18	UPNONCE17	UPNONCE16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[23:16]:** Upper Nonce bits
13-byte nonce value used in security.

REGISTER 2-96: UPNONCE3: UPPER NONCE SECURITY 3 REGISTER (ADDRESS: 0x243)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE31	UPNONCE30	UPNONCE29	UPNONCE28	UPNONCE27	UPNONCE26	UPNONCE25	UPNONCE24
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[31:24]:** Upper Nonce bits
13-byte nonce value used in security.

REGISTER 2-97: UPNONCE4: UPPER NONCE SECURITY 4 REGISTER (ADDRESS: 0x244)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE39	UPNONCE38	UPNONCE37	UPNONCE36	UPNONCE35	UPNONCE34	UPNONCE33	UPNONCE32
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[39:32]:** Upper Nonce bits
13-byte nonce value used in security.

REGISTER 2-98: UPNONCE5: UPPER NONCE SECURITY 5 REGISTER (ADDRESS: 0x245)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE47	UPNONCE46	UPNONCE45	UPNONCE44	UPNONCE43	UPNONCE42	UPNONCE41	UPNONCE40
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[47:40]:** Upper Nonce bits
13-byte nonce value used in security.

REGISTER 2-99: UPNONCE6: UPPER NONCE SECURITY 6 REGISTER (ADDRESS: 0x246)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE55	UPNONCE54	UPNONCE53	UPNONCE52	UPNONCE51	UPNONCE50	UPNONCE49	UPNONCE48
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[55:48]:** Upper Nonce bits
13-byte nonce value used in security.

REGISTER 2-100: UPNONCE7: UPPER NONCE SECURITY 7 REGISTER (ADDRESS: 0x247)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE63	UPNONCE62	UPNONCE61	UPNONCE60	UPNONCE59	UPNONCE58	UPNONCE57	UPNONCE56
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[63:56]:** Upper Nonce bits
13-byte nonce value used in security.

REGISTER 2-101: UPNONCE8: UPPER NONCE SECURITY 8 REGISTER (ADDRESS: 0x248)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE71	UPNONCE70	UPNONCE69	UPNONCE68	UPNONCE67	UPNONCE66	UPNONCE65	UPNONCE64
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[71:64]:** Upper Nonce bits
13-byte nonce value used in security.

REGISTER 2-102: UPNONCE9: UPPER NONCE SECURITY 9 REGISTER (ADDRESS: 0x249)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE79	UPNONCE78	UPNONCE77	UPNONCE76	UPNONCE75	UPNONCE74	UPNONCE73	UPNONCE72
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[79:72]:** Upper Nonce bits
13-byte nonce value used in security.

REGISTER 2-103: UPNONCE10: UPPER NONCE SECURITY 10 REGISTER (ADDRESS: 0x24A)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE87	UPNONCE86	UPNONCE85	UPNONCE84	UPNONCE83	UPNONCE82	UPNONCE81	UPNONCE80
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[87:80]:** Upper Nonce bits
13-byte nonce value used in security.

REGISTER 2-104: UPNONCE11: UPPER NONCE SECURITY 11 REGISTER (ADDRESS: 0x24B)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE95	UPNONCE94	UPNONCE93	UPNONCE92	UPNONCE91	UPNONCE90	UPNONCE89	UPNONCE88
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[95:88]:** Upper Nonce bits
13-byte nonce value used in security.

REGISTER 2-105: UPNONCE12: UPPER NONCE SECURITY 12 REGISTER (ADDRESS: 0x24C)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPNONCE103	UPNONCE102	UPNONCE101	UPNONCE100	UPNONCE99	UPNONCE98	UPNONCE97	UPNONCE96
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **UPNONCE[103:96]:** Upper Nonce bits
13-byte nonce value used in security.

NOTES:

3.0 FUNCTIONAL DESCRIPTION

3.1 Reset

The MRF24J40 has four Reset types:

- Power-on Reset – The MRF24J40 has built-in Power-on Reset circuitry that will automatically reset all control registers when power is applied. It is recommended to delay 2 ms after a Reset before accessing the MRF24J40 to allow the RF circuitry to start up and stabilize.
- $\overline{\text{RESET}}$ Pin – The MRF24J40 can be reset by the host microcontroller by asserting the $\overline{\text{RESET}}$ pin 13 low. All control registers will be reset. The MRF24J40 will be released from Reset approximately 250 μs after $\overline{\text{RESET}}$ is released. The $\overline{\text{RESET}}$ pin has an internal weak pull-up resistor. It is recommended to delay 2 ms after a Reset before accessing the MRF24J40 to allow the RF circuitry to start up and stabilize.
- Software Reset – A Software Reset can be performed by the host microcontroller. The power management circuitry is reset by setting the RSTPWR (0x2A[2]) bit to '1'. The control registers retain their values. The baseband circuitry is reset by setting the RSTBB (0x2A[1]) bit to '1'. The control registers retain their values. The MAC circuitry is reset by setting the RSTMAC (0x2A[0]) bit to '1'. All control registers will be reset. The Resets can be performed individually or together. The bit(s) will be automatically cleared to '0' by hardware. No delay is necessary after a Software Reset.
- RF State Machine Reset – Perform an RF State Machine Reset by setting to '1' the RFRST (RFCTL 0x36[2]) bit and then clearing to '0'. Delay at least 192 μs after performing to allow the RF circuitry to calibrate. The control registers retain their values.

Note: The RF state machine should be Reset after the frequency channel has been changed (RFCON0 0x200).

TABLE 3-1: REGISTERS ASSOCIATED WITH RESET

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2A	SOFTRST	r	r	r	r	r	RSTPWR	RSTBB	RSTMAC
0x36	RFCTL	r	r	r	WAKECNT8	WAKECNT7	RFRST	RFTXMODE	RFRXMODE

3.2 Initialization

Certain control register values must be initialized for basic operations. These values differ from the Power-on Reset values and provide improved operational parameters. These settings are normally made once after a Reset. After initialization, MRF24J40 features can be configured for the application. The steps for initialization are shown in Example 3-1.

EXAMPLE 3-1: INITIALIZING THE MRF24J40

Example steps to initialize the MRF24J40:

1. SOFTRST (0x2A) = 0x07 – Perform a software Reset. The bits will be automatically cleared to '0' by hardware.
2. PACON2 (0x18) = 0x98 – Initialize FIFOEN = 1 and TXONTS = 0x6.
3. TXSTBL (0x2E) = 0x95 – Initialize RFSTBL = 0x9.
4. RFCON0 (0x200) = 0x03 – Initialize RFOPT = 0x03.
5. RFCON1 (0x201) = 0x02 – Initialize VCOOPT = 0x02.
6. RFCON2 (0x202) = 0x80 – Enable PLL (PLLEN = 1).
7. RFCON6 (0x206) = 0x90 – Initialize TXFIL = 1 and 20MRECVR = 1.
8. RFCON7 (0x207) = 0x80 – Initialize SLPCLKSEL = 0x2 (100 kHz Internal oscillator).
9. RFCON8 (0x208) = 0x10 – Initialize RFVCO = 1.
10. SLPCON1 (0x220) = 0x21 – Initialize $\overline{\text{CLKOUTEN}}$ = 1 and SLPCLKDIV = 0x01.

Configuration for nonbeacon-enabled devices (see **Section 3.8 "Beacon-Enabled and Nonbeacon-Enabled Networks"**):

11. BBREG2 (0x3A) = 0x80 – Set CCA mode to ED.
12. CCAEDTH = 0x60 – Set CCA ED threshold.
13. BBREG6 (0x3E) = 0x40 – Set appended RSSI value to RXFIFO.
14. Enable interrupts – See **Section 3.3 "Interrupts"**.
15. Set channel – See **Section 3.4 "Channel Selection"**.

Note: Maintain 0x200[3:0] = 0x03

16. Set transmitter power - See "REGISTER 2-62: RF CONTROL 3 REGISTER (ADDRESS: 0x203)".
17. RFCTL (0x36) = 0x04 – Reset RF state machine.
18. RFCTL (0x36) = 0x00.
19. Delay at least 192 μs.

TABLE 3-2: REGISTERS ASSOCIATED WITH INITIALIZATION

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x18	PACON2	FIFOEN	r	TXONTS3	TXONTS2	TXONTS1	TXONTS0	TXONT8	TXONT7
0x2A	SOFTRST	r	r	r	r	r	RSTPWR	RSTBB	RSTMAC
0x2E	TXSTBL	RFSTBL3	RFSTBL2	RFSTBL1	RFSTBL0	MSIFS3	MSIFS2	MSIFS1	MSIFS0
0x201	RFCON1	VCOOPT7	VCOOPT6	VCOOPT5	VCOOPT4	VCOOPT3	VCOOPT2	VCOOPT1	VCOOPT0
0x202	RFCON2	PLLEN	r	r	r	r	r	r	r
0x206	RFCON6	TXFIL	r	r	20MRECVR	BATEN	r	r	r
0x207	RFCON7	SLPCLKSEL1	SLPSCKSEL0	r	r	r	r	r	r
0x208	RFCON8	r	r	r	RFVCO	r	r	r	r
0x220	SLPCON1	r	r	$\overline{\text{CLKOUTEN}}$	SLPCLKDIV4	SLPCLKDIV3	SLPCLKDIV2	SLPCLKDIV1	SLPCLKDIV0

3.3 Interrupts

The MRF24J40 has one interrupt (INT) pin 16 that signals one of eight interrupt events to the host microcontroller. The interrupt structure is shown in Figure 3-1. Interrupts are enabled via the INTCON (0x32) register. Interrupt flags are located in the INTSTAT (0x31) register. The INTSTAT register clears-to-zero upon read. Therefore, the host microcontroller should read and store the INTSTAT register and check the bits to determine which interrupt occurred. The INT pin will continue to signal an interrupt until the INTSTAT register is read. The edge polarity of the INT pin is configured via the INTEDGE bit in the SLPCON0 (0x211[1]) register.

Note 1: The INTEDGE polarity defaults to: 0 = Falling Edge. Ensure that the interrupt polarity matches the interrupt pin polarity of the host microcontroller.

2: The INT pin will remain high or low, depending on INTEDGE polarity setting, until INTSTAT register is read.

FIGURE 3-1: MRF24J40 INTERRUPT LOGIC

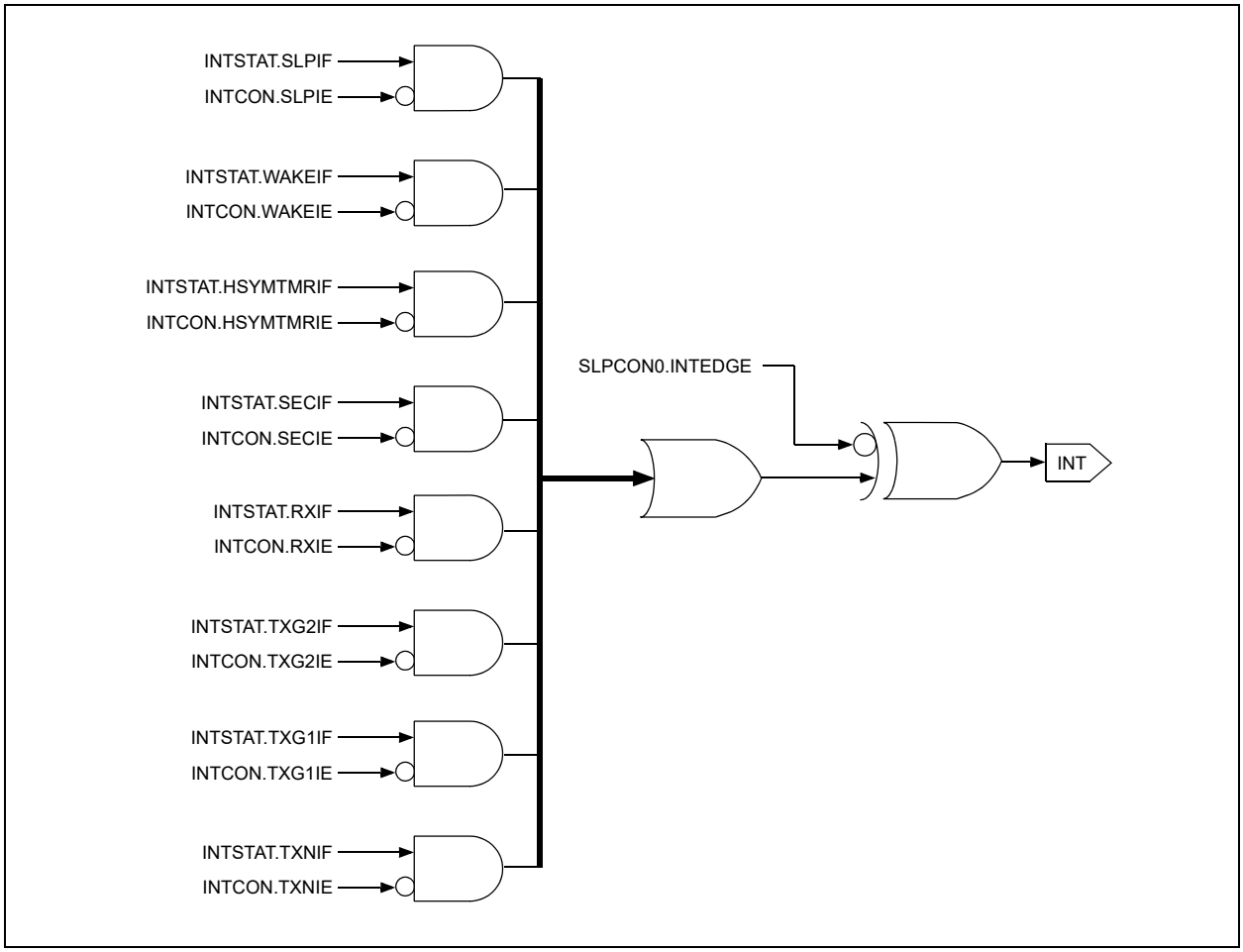


TABLE 3-3: REGISTERS ASSOCIATED WITH INTERRUPTS

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x31	INTSTAT	SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF
0x32	INTCON	SLPIE	WAKEIE	HSYMTMRIE	SECIE	RXIE	TXG2IE	TXG1IE	TXNIE
0x211	SLPCON0	r	r	r	r	r	r	INTEDGE	$\overline{\text{SLPCKEN}}$

3.4 Channel Selection

The MRF24J40 is capable of selecting one of sixteen channel frequencies in the 2.4 GHz band. The desired channel is selected by configuring the CHANNEL bits in the RFCON0 (0x200[7:4]) register. See Table 3-4 for the RFCON0 register setting for channel number and frequency.

Note:	Perform an RF State Machine Reset (see **Section 3.1 "Reset"**) after a channel frequency change. Then, delay at least 192 μs after the RF State Machine Reset, to allow the RF circuitry to calibrate.

TABLE 3-4: CHANNEL SELECTION RFCON0 (0x200) REGISTER SETTING

Channel Number	Frequency	Set Value
11	2.405 GHz	0x03
12	2.410 GHz	0x13
13	2.415 GHz	0x23
14	2.420 GHz	0x33
15	2.425 GHz	0x43
16	2.430 GHz	0x53
17	2.435 GHz	0x63
18	2.440 GHz	0x73
19	2.445 GHz	0x83
20	2.450 GHz	0x93
21	2.455 GHz	0xA3
22	2.460 GHz	0xB3
23	2.465 GHz	0xC3
24	2.470 GHz	0xD3
25	2.475 GHz	0xE3
26	2.480 GHz	0xF3

TABLE 3-5: REGISTERS ASSOCIATED WITH CHANNEL SELECTION

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x36	RFCTL	r	r	r	WAKECNT8	WAKECNT7	RFRST	RFTX-MODE	RFRX-MODE
0x200	RFCON0	CHANNEL3	CHANNEL2	CHANNEL1	CHANNEL0	RFOPT3	RFOPT2	RFOPT1	RFOPT0

3.5 Clear Channel Assessment (CCA)

The CCA signal is an indication to the MAC layer from the PHY layer as to whether the medium is busy or idle.

The MRF24J40 provides three methods of performing CCA. Refer to IEEE 802.15.4-2003 Standard, Section 6.7.9 “CCA”.

3.5.1 CCA MODE 1: ENERGY ABOVE THRESHOLD

CCA reports a busy medium upon detecting energy above the Energy Detection (ED) threshold.

1. Program CCAMODE 0x3A[7:6] to the value, ‘10’.
2. Program CCAEDTH 0x3F[7:0] with CCA ED threshold value (RSSI value).

   The 8-bit CCAEDTH threshold can be mapped to a power level according to RSSI. Refer to **Section 3.6 “Received Signal Strength Indicator (RSSI)/Energy Detection (ED)”**.

3.5.2 CCA MODE 2: CARRIER SENSE ONLY

CCA reports a busy medium only upon detection of a signal with the modulation and spreading characteristics of IEEE 802.15.4. This signal may or may not be above the ED threshold.

1. Program CCAMODE 0x3A[7:6] to the value, ‘01’.
2. Program CCACSTH 0x3A[5:2] with the CCA carrier sense threshold (units).

3.5.3 CCA MODE 3: CARRIER SENSE WITH ENERGY ABOVE THRESHOLD

CCA reports a busy medium only upon detection of a signal with modulation or spreading characteristics of IEEE 802.15.4 with energy above the ED threshold.

1. Program CCAMODE 0x3A[7:6] to the value, ‘11’.
2. Program CCACSTH 0x3A[5:2] with the CCA carrier sense threshold.
3. Program CCAEDTH 0x3F[7:0] with the CCA ED threshold (RSSI value).

   The 8-bit CCAEDTH threshold can be mapped to a power level according to RSSI. Refer to **Section 3.6 “Received Signal Strength Indicator (RSSI)/Energy Detection (ED)”**.

TABLE 3-6: REGISTERS ASSOCIATED WITH CCA

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3A	BBREG2	CCAMODE1	CCAMODE0	CCACSTH3	CCACSTH2	CCACSTH1	CCACSTH0	r	r
0x3F	CCAEDTH	CCAEDTH7	CCAEDTH6	CCAEDTH5	CCAEDTH4	CCAEDTH3	CCAEDTH2	CCAEDTH1	CCAEDTH0

3.6 Received Signal Strength Indicator (RSSI)/Energy Detection (ED)

RSSI/ED are an estimate of the received signal power within the bandwidth of an IEEE 802.15.4 channel. The RSSI value is an 8-bit value ranging from 0-255. The mapping between the RSSI values with the received power level is shown in Figure 3-3 and is shown in tabular form in Table 3-8. The number of symbols to average can be changed by programming the RSSINUM (TXBCON1 0x25[5:4]) bits.

The programmer can obtain the RSSI/ED value in one of two methods.

3.6.1 RSSI FIRMWARE REQUEST (RSSI MODE1)

In this mode, the host microcontroller sends a request to calculate RSSI, then waits until it is done and then reads the RSSI value. The steps are:

1. Set RSSIMODE1 0x3E[7] – Initiate RSSI calculation.
2. Wait until RSSIRDY 0x3E[0] is set to '1' – RSSI calculation is complete.
3. Read RSSI 0x210[7:0] – The RSSI register contains the averaged RSSI received power level for 8 symbol periods.

3.6.2 APPENDED RSSI TO THE RECEIVED PACKET (RSSI MODE 2)

The RSSI value is appended at the end of each successfully received packet.

To enable RSSI Mode 2, set RSSIMODE2 = 1 (0x3E[6]). The RSSI value will be appended to the RXFIFO as shown in Figure 3-2.

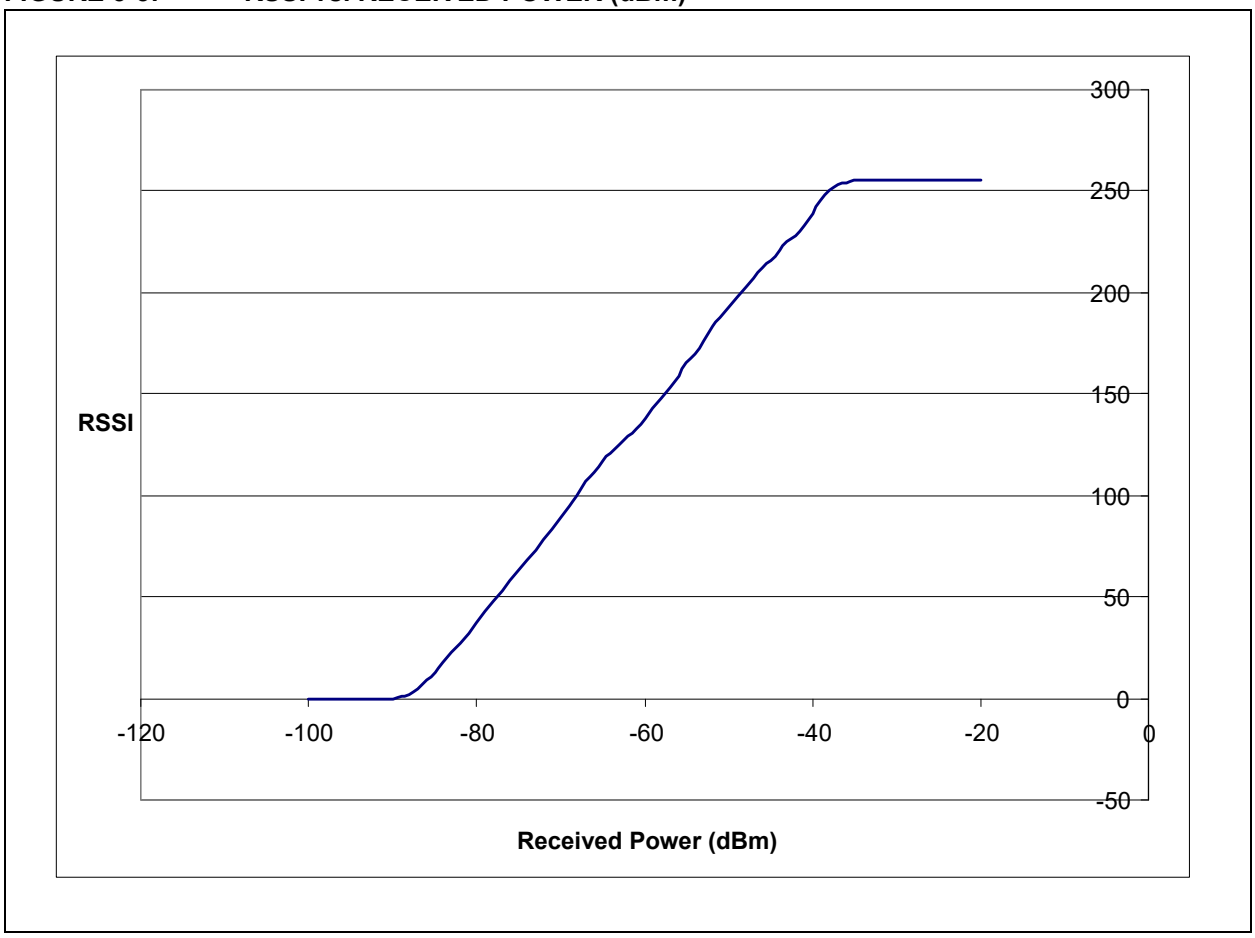
FIGURE 3-2: PACKET FORMAT IN RX FIFO

1 Octet	N Octets	M Octets	2 Octets	1 Octet	1 Octet
Frame Length	Header	Payload	FCS	LQI	RSSI

TABLE 3-7: REGISTERS ASSOCIATED WITH RSSI/ED

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x25	TXBCON1	TXBMSK	$\overline{WU}$/BCN	RSSINUM1	RSSINUM0	r	r	r	r
0x3E	BBREG6	RSSIMODE1	RSSIMODE2	r	r	r	r	r	RSSIRDY
0x210	RSSI	RSSI7	RSSI6	RSSI5	RSSI4	RSSI3	RSSI2	RSSI1	RSSI0

FIGURE 3-3: RSSI vs. RECEIVED POWER (dBm)



RSSI versus received power (dB) is shown in tabular form in Table 3-8.

TABLE 3-8: RSSI vs. RECEIVED POWER (dB)

Received Power (dBm)	RSSI Value (hex)	RSSI Value (dec)
-100	0x0	0
-99	0x0	0
-98	0x0	0
-97	0x0	0
-96	0x0	0
-95	0x0	0
-94	0x0	0
-93	0x0	0
-92	0x0	0
-91	0x0	0
-90	0x0	0
-89	0x1	1
-88	0x2	2
-87	0x5	5
-86	0x9	9
-85	0x0D	13
-84	0x12	18
-83	0x17	23
-82	0x1B	27
-81	0x20	32
-80	0x25	37
-79	0x2B	43
-78	0x30	48
-77	0x35	53
-76	0x3A	58
-75	0x3F	63
-74	0x44	68
-73	0x49	73
-72	0x4E	78
-71	0x53	83
-70	0x59	89
-69	0x5F	95
-68	0x64	100
-67	0x6B	107
-66	0x6F	111
-65	0x75	117
-64	0x79	121
-63	0x7D	125
-62	0x81	129
-61	0x85	133
-60	0x8A	138

TABLE 3-8: RSSI vs. RECEIVED POWER (dB) (CONTINUED)

Received Power (dBm)	RSSI Value (hex)	RSSI Value (dec)
-59	0x8F	143
-58	0x94	148
-57	0x99	153
-56	0x9F	159
-55	0xA5	165
-54	0xAA	170
-53	0xB0	176
-52	0xB7	183
-51	0xBC	188
-50	0xC1	193
-49	0xC6	198
-48	0xCB	203
-47	0xCF	207
-46	0xD4	212
-45	0xD8	216
-44	0xDD	221
-43	0xE1	225
-42	0xE4	228
-41	0xE9	233
-40	0xEF	239
-39	0xF5	245
-38	0xFA	250
-37	0xFD	253
-36	0xFE	254
-35	0xFF	255
-34	0xFF	255
-33	0xFF	255
-32	0xFF	255
-31	0xFF	255
-30	0xFF	255
-29	0xFF	255
-28	0xFF	255
-27	0xFF	255
-26	0xFF	255
-25	0xFF	255
-24	0xFF	255
-23	0xFF	255
-22	0xFF	255
-21	0xFF	255
-20	0xFF	255

3.7 Link Quality Indication (LQI)

Link Quality Indication (LQI) is a characterization of strength or quality of a received packet. Several metrics, for example, RSSI, Signal to Noise Ratio (SNR), RSSI combined with SNR, etc., can be used for measuring link quality. Using RSSI or SNR alone may not be the best way to estimate the quality of a link. The received RSSI value will be a very high value if a packet is received with greater signal strength or even if an interferer is present in the channel. Hence, for better approximation of link quality, the MRF24J40 reports the correlation degree between spreading sequences and the incoming chips during the reception of a packet. This correlation value must be directly mapped to a range of 0-255 (256 values) using software, where an LQI value of 0 indicates that the quality of the link is very low, and an LQI value of 255 indicates the quality of the link is very high. The correlation degree between spreading sequences and incoming chips is computed over a period of 3 symbol periods during the reception of the preamble of a packet.

EQUATION 3-1: LQI

LQI (0-255) = (CORR - a).b

where,

- CORR = LQI reported along with each packet in the RX FIFO, as shown in Figure 3-2.
- a = 50
- b = 4
  - Values of ‘a’ and ‘b’ are found empirically based on Packet Error Rate (PER) measurements as a function of the correlation value.

3.8 Beacon-Enabled and Nonbeacon-Enabled Networks

The IEEE 802.15.4 Standard defines two modes of operation:

- Beacon-enabled network
- Nonbeacon-enabled network

3.8.1 BEACON-ENABLED NETWORK

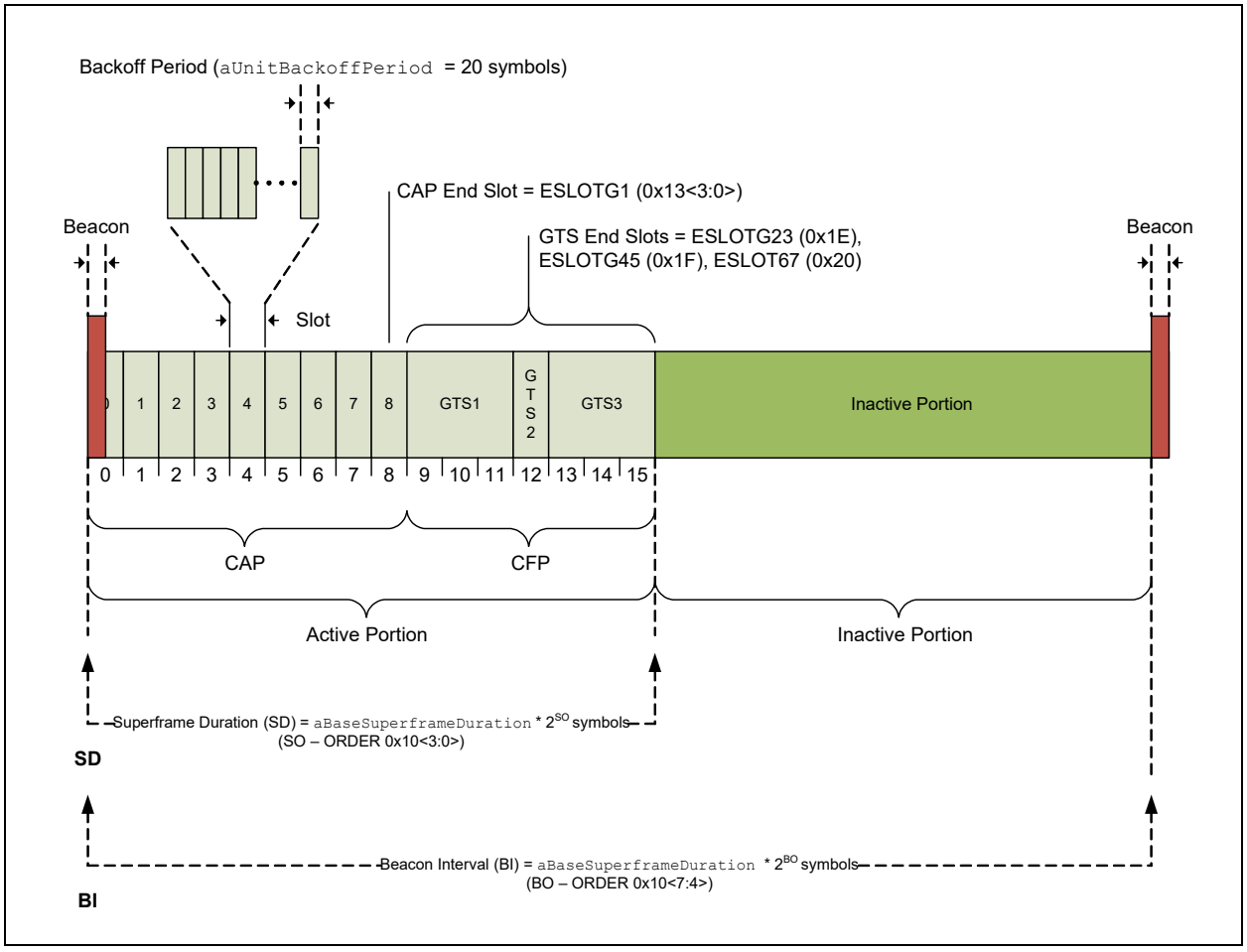
In a beacon-enabled network, beacons will be transmitted periodically by the PAN coordinator. These beacons are mainly used to provide synchronization services between all the devices in the PAN and also to support other extended features, like Guaranteed Time Slots (GTS), a Quality of Service (QoS) mechanism for the IEEE 802.15.4 Standard. The PAN coordinator defines the structure of the superframe using beacons.

3.8.1.1 Superframe Structure

The superframe structure is shown in Figure 3-4. A superframe is bounded by the transmission of a beacon frame and can have an active and inactive portion. The coordinator will interact with its PAN only during the active portion of the superframe, and during the inactive portion of the superframe, the coordinator can go to a low-power mode. The active portion of the superframe is divided into 16 equally spaced slots and is composed of three parts: a beacon, a Contention Access Period (CAP) and an optional Contention Free Period (CFP). The structure of the superframe depends on the values of Beacon Order (BO) and Superframe Order (SO). The CFP, if present, follows immediately after the CAP and extends to the end of active portion of the superframe. Any allocated GTSs shall be located in the CFP of the active portion of the superframe.

All the frames transmitted in the CAP, except Acknowledgement frames and data frames that immediately follow the data request command, must use slotted CSMA-CA. Refer to **Section 3.9 "Carrier Sense Multiple Access-Collision Avoidance (CSMA-CA) Algorithm"** for more information.

FIGURE 3-4: SUPERFRAME STRUCTURE



3.8.1.2 BO and SO

Values of Beacon Order (BO) and Superframe Order (SO) determine the Beacon Interval (BI) and Superframe Duration (SD).

Beacon Interval (BI) in terms of BO can be expressed as:

$$BI = aBaseSuperframeduration * 2^{BO}$$

Similarly, Superframe Duration (SD) in terms of SO can be expressed as:

$$SD = aBaseSuperframeduration * 2^{SO}$$

where `aBaseSuperframeduration` = 960 symbols.

BO and SO can be configured by programming the BO (0x10[7:4]) bits and SO (0x10[3:0]) bits in the ORDER register. For beacon-enabled networks, the values of BO and SO should be in the range, $0 \leq SO \leq BO \leq 14$. If the values of BO and SO are equal, then the superframe does not have any inactive portion. A Beacon Interval can be as short as 15 ms or a long as 251 seconds based on the values of BO and SO.

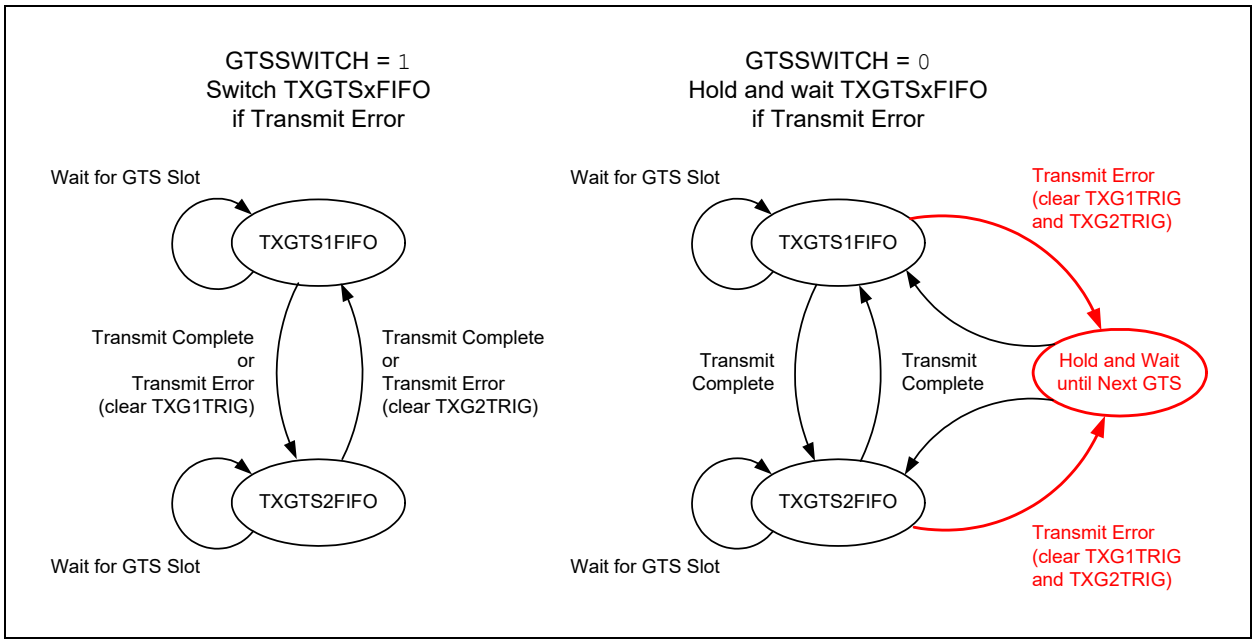
3.8.1.3 GTS

If a device wants to transmit or receive during CFP, it sends out a “GTS request” in the CAP to the PAN coordinator. The PAN coordinator broadcasts the address of the device number for that device in the beacon frame if resources are available.

To support GTS operation, MRF24J40 uses TXGTS1FIFO and TXGTS2FIFO. The TXGTS1FIFO and TXGTS2FIFO are ping-pong FIFOs and can be assigned to different GTS slots or to the same slots. If both are assigned to the same slot, they take turns for transmission within that slot. TXGTS1FIFO and TXGTS2FIFO can be triggered ahead of their slot time, but transmission from the FIFO will take place exactly at the assigned slot time.

Refer to **Section 3.12 “Transmission”** for information on how to transmit a data frame using the TXGTSxFIFOs.

FIGURE 3-5: GTSFIFO STATE DIAGRAM



3.8.1.4 Configuring Beacon-Enabled PAN Coordinator

The following steps configure the MRF24J40 as a coordinator in a beacon-enabled network:

1. Set the PANCOORD (RXMCR 0x00[3]) bit = 1 to configure as PAN coordinator.
2. Set the SLOTTED (TXMCR 0x11[5]) bit = 1 to use Slotted CSMA-CA mode.
3. Load the beacon frame into the TXBFIFO (0x080-0x0FF).
4. Set the TXBMSK (TXBCON1 0x25[7]) bit = 1 to mask the beacon interrupt mask.
5. Set INTL (WAKECON 0x22[5:0]) value to 0x03.
6. Program the CAP end slot (ESLOTG1 0x13[3:0]) value. If the coordinator supports Guaranteed Time Slot operation, refer to **Section 3.8.1.5 "Configuring Beacon-Enabled GTS Settings for PAN Coordinator"** below.
7. Calibrate the Sleep Clock (SLPCLK) frequency. Refer to **Section 3.15.1.2 "Sleep Clock Calibration"**.
8. Set WAKECNT (SLPACK 0x35[6:0]) value = 0x5F to set the main oscillator (20 MHz) start-up timer value.
9. Program the Beacon Interval into the Main Counter, MAINCNT (0x229[1:0], 0x228, 0x227, 0x226), and Remain Counter, REMCNT (0x225, 0x224), according to BO and SO values. Refer to **Section 3.15.1.3 "Sleep Mode Counters"**.
10. Configure the BO (ORDER 0x10[7:4]) and SO (ORDER 0x10[3:0]) values. After configuring BO and SO, the beacon frame will be sent immediately.

3.8.1.5 Configuring Beacon-Enabled GTS Settings for PAN Coordinator

The following steps configure the MRF24J40 as a coordinator in a beacon-enabled network with Guaranteed Time Slots:

1. Set the GTSON (GATECLK 0x26 [3]) bit = 1 to enable the GTS FIFO clock.
2. Based on the number of GTSs that are active for the current superframe, program the end slot value of each GTS into the ESLOT registers as shown in Table 3-9.

TABLE 3-9: PROGRAMMING END SLOT VALUES

GTS Number	Register
CAP	ESLOTG1 0x13[3:0]
GTS1	ESLOTG1 0x13[7:4]
GTS2	ESLOTG23 0x1E[3:0]
GTS3	ESLOTG23 0x1E[7:4]
GTS4	ESLOTG45 0x1F[3:0]
GTS5	ESLOTG45 0x1F[7:4]
GTS6	ESLOTG67 0x20[3:0]
GTS7	If 7th GTS exists, the end slot must be 15

3. Set the GTSSWITCH (TXPEND 0x21[1]) bit = 1 so that if a TXGTS1FIFO or TXGTS2FIFO transmission error occurs, it will switch to another TXGTSxFIFO.

3.8.1.6 Configuring Beacon-Enabled Device

The following steps configure the MRF24J40 as a device in a beacon-enabled network:

1. Set the SLOTTED (TXMCR 0x11[5]) bit = 1 to use Slotted CSMA-CA mode.
2. Set the OFFSET (FRMOFFSET 0x23[7:0]) value = 0x15 for optimum timing alignment.
3. Calibrate the Sleep Clock (SLPCLK) frequency. Refer to **Section 3.15.1.2 "Sleep Clock Calibration"**.
4. Program the associated coordinator's 64-bit extended address to the ASSOEADR registers (0x230-0x237).
5. Program the associated coordinator's 16-bit short address to the ASSOSADR registers (0x238-0x239).

Note:	The device will align its beacon frame with the associated coordinator's beacon frame only when the source address matches the ASSOEADR or ASSOSADR value.

6. Parse the received associated coordinator's beacon frame and extract the values of BO and SO. Calculate the inactive period and program the Main Counter, MAINCNT (0x229[1:0], 0x228, 0x227, 0x226), and Remain Counter, REMCNT (0x225, 0x224), according to the BO and SO values. Refer to **Section 3.15.1.3 "Sleep Mode Counters"**.
7. Program the CAP end slot (ESLOTG1 0x13[3:0]) value.

3.8.1.7 Configuring Beacon-Enabled GTS Settings for Device

The following steps configure the MRF24J40 as a device in a beacon-enabled network with Guaranteed Time Slots:

1. Set the GTSON (GATECLK 0x26[3]) bit = 1 to enable the GTS FIFO clock.
2. Parse the received beacon frame and obtain the GTS allocation information. Program the end slot value of the CAP and each GTS into the ESLOT registers, as shown in Table 3-9.
3. Set the GTSSWITCH (TXPEND 0x21[1]) bit = 1 so that if a TXGTS1FIFO or TXGTS2FIFO transmission error occurs, it will switch to another TXGTSxFIFO.

3.8.2 NONBEACON-ENABLED NETWORK

A nonbeacon-enabled network does not transmit a beacon unless it receives a beacon request, and hence, does not have any superframe structure. A nonbeacon-enabled network uses unslotted CSMA-CA to access the medium. The unslotted CSMA-CA is explained in **Section 3.9 "Carrier Sense Multiple Access-Collision Avoidance (CSMA-CA) Algorithm"**. For nonbeacon-enabled networks, both BO and SO are set to 15. Guaranteed Time Slots (GTS) are not supported, and generally, devices require less computing power as there are no strict timing requirements that need to be met.

3.8.2.1 Configuring Nonbeacon-Enabled PAN Coordinator

The following steps configure the MRF24J40 as a coordinator in a nonbeacon-enabled network:

1. Set the PANCOORD (RXMCR 0x00[3]) bit = 1 to configure as the PAN coordinator.
2. Clear the SLOTTED (TXMCR 0x11[5]) bit = 0 to configure Unslotted CSMA-CA mode.
3. Configure BO (ORDER 0x10[7:4]) value = 0xF.
4. Configure SO (ORDER 0x10[3:0]) value = 0xF.

3.8.2.2 Configuring Nonbeacon-Enabled Device

The following steps configure the MRF24J40 as a device in a nonbeacon-enabled network:

1. Clear the PANCOORD (RXMCR 0x00[3]) bit = 0 to configure as device.
2. Clear the SLOTTED (TXMCR 0x11[5]) bit = 0 to use Unslotted CSMA-CA mode.

TABLE 3-10: REGISTERS ASSOCIATED WITH SETTING UP BEACON-ENABLED AND NONBEACON-ENABLED NETWORKS

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	RXMCR	r	r	NOACKRSP	r	PANCOORD	COORD	ERRPKT	PROMI
0x10	ORDER	BO3	BO2	BO1	BO0	SO3	SO2	SO1	SO0
0x11	TXMCR	NOCSMA	BATLIFEXT	SLOTTED	MACMINBE1	MACMINB0	CSMABF2	CSMABF1	CSMABF0
0x13	ESLOTG1	GTS1-3	GTS1-2	GTS1-1	GTS1-0	CAP3	CAP2	CAP1	CAP0
0x1E	ESLOTG23	GTS3-3	GTS3-2	GTS3-1	GTS3-0	GTS2-3	GTS2-2	GTS2-1	GTS2-0
0x1F	ESLOTG45	GTS5-3	GTS5-2	GTS5-1	GTS5-0	GTS4-3	GTS4-2	GTS4-1	GTS4-0
0x20	ESLOTG67	r	r	r	r	GTS6-3	GTS6-2	GTS6-1	GTS6-0
0x21	TXPEND	MLIFS5	MLIFS4	MLIFS3	MLIFS2	MLIFS1	MLIFS0	GTSSWITCH	FPACK
0x22	WAKECON	IMMWAKE	REGWAKE	INTL	INTL	INTL	INTL	INTL	INTL
0x23	FRMOFFSET	OFFSET7	OFFSET6	OFFSET5	OFFSET4	OFFSET3	OFFSET2	OFFSET1	OFFSET0
0x25	TXBCON1	TXBMSK	$\overline{\text{WU}}$/BCN	RSSINUM1	RSSINUM0	r	r	r	r
0x26	GATECLK	r	r	r	r	GTSON	r	r	r
0x35	SLPACK	SLPACK	WAKECNT6	WAKECNT5	WAKECNT4	WAKECNT3	WAKECNT2	WAKECNT1	WAKECNT0
0x224	REMCNTL	REMCNT7	REMCNT6	REMCNT5	REMCNT4	REMCNT3	REMCNT2	REMCNT1	REMCNT0
0x225	REMCNTH	REMCNT15	REMCNT14	REMCNT13	REMCNT12	REMCNT11	REMCNT10	REMCNT9	REMCNT8
0x226	MAINCNT0	MAINCNT7	MAINCNT6	MAINCNT5	MAINCNT4	MAINCNT3	MAINCNT2	MAINCNT1	MAINCNT0
0x227	MAINCNT1	MAINCNT15	MAINCNT14	MAINCNT13	MAINCNT12	MAINCNT11	MAINCNT10	MAINCNT9	MAINCNT8
0x228	MAINCNT2	MAINCNT23	MAINCNT22	MAINCNT21	MAINCNT20	MAINCNT19	MAINCNT18	MAINCNT17	MAINCNT16
0x229	MAINCNT3	STARTCNT	r	r	r	r	r	MAINCNT25	MAINCNT24
0x230	ASSOEADR0	ASSOEADR7	ASSOEADR6	ASSOEADR5	ASSOEADR4	ASSOEADR3	ASSOEADR2	ASSOEADR1	ASSOEADR0
0x231	ASSOEADR1	ASSOEADR15	ASSOEADR14	ASSOEADR13	ASSOEADR12	ASSOEADR11	ASSOEADR10	ASSOEADR9	ASSOEADR8
0x232	ASSOEADR2	ASSOEADR23	ASSOEADR22	ASSOEADR21	ASSOEADR20	ASSOEADR19	ASSOEADR18	ASSOEADR17	ASSOEADR16
0x233	ASSOEADR3	ASSOEADR31	ASSOEADR30	ASSOEADR29	ASSOEADR28	ASSOEADR27	ASSOEADR26	ASSOEADR25	ASSOEADR24
0x234	ASSOEADR4	ASSOEADR39	ASSOEADR38	ASSOEADR37	ASSOEADR36	ASSOEADR35	ASSOEADR34	ASSOEADR33	ASSOEADR32
0x235	ASSOEADR5	ASSOEADR47	ASSOEADR46	ASSOEADR45	ASSOEADR44	ASSOEADR43	ASSOEADR42	ASSOEADR41	ASSOEADR40
0x236	ASSOEADR6	ASSOEADR55	ASSOEADR54	ASSOEADR53	ASSOEADR52	ASSOEADR51	ASSOEADR50	ASSOEADR49	ASSOEADR48
0x237	ASSOEADR7	ASSOEADR63	ASSOEADR62	ASSOEADR61	ASSOEADR60	ASSOEADR59	ASSOEADR58	ASSOEADR57	ASSOEADR56
0x238	ASSOSADR0	ASSOSADR7	ASSOSADR6	ASSOSADR5	ASSOSADR4	ASSOSADR3	ASSOSADR2	ASSOSADR1	ASSOSADR0
0x239	ASSOSADR1	ASSOSADR15	ASSOSADR14	ASSOSADR13	ASSOSADR12	ASSOSADR11	ASSOSADR10	ASSOSADR9	ASSOSADR8

3.9 Carrier Sense Multiple Access-Collision Avoidance (CSMA-CA) Algorithm

MRF24J40 supports both unslotted and slotted CSMA-CA mechanisms, as defined in the IEEE 802.15.4 Standard. In both modes, the CSMA-CA algorithm is implemented using units of time called backoff periods. In slotted CSMA-CA, the back-off period boundaries of every device on the PAN shall be aligned with the superframe slot boundaries of the PAN coordinator. In unslotted CSMA-CA, the backoff periods of one device are not related in time to the backoff periods of any other device in the PAN. Refer to IEEE 802.15.4-2003, Section 7.5.1.3 "The CSMA-CA Algorithm" for more information. This section covers the two modes and their settings.

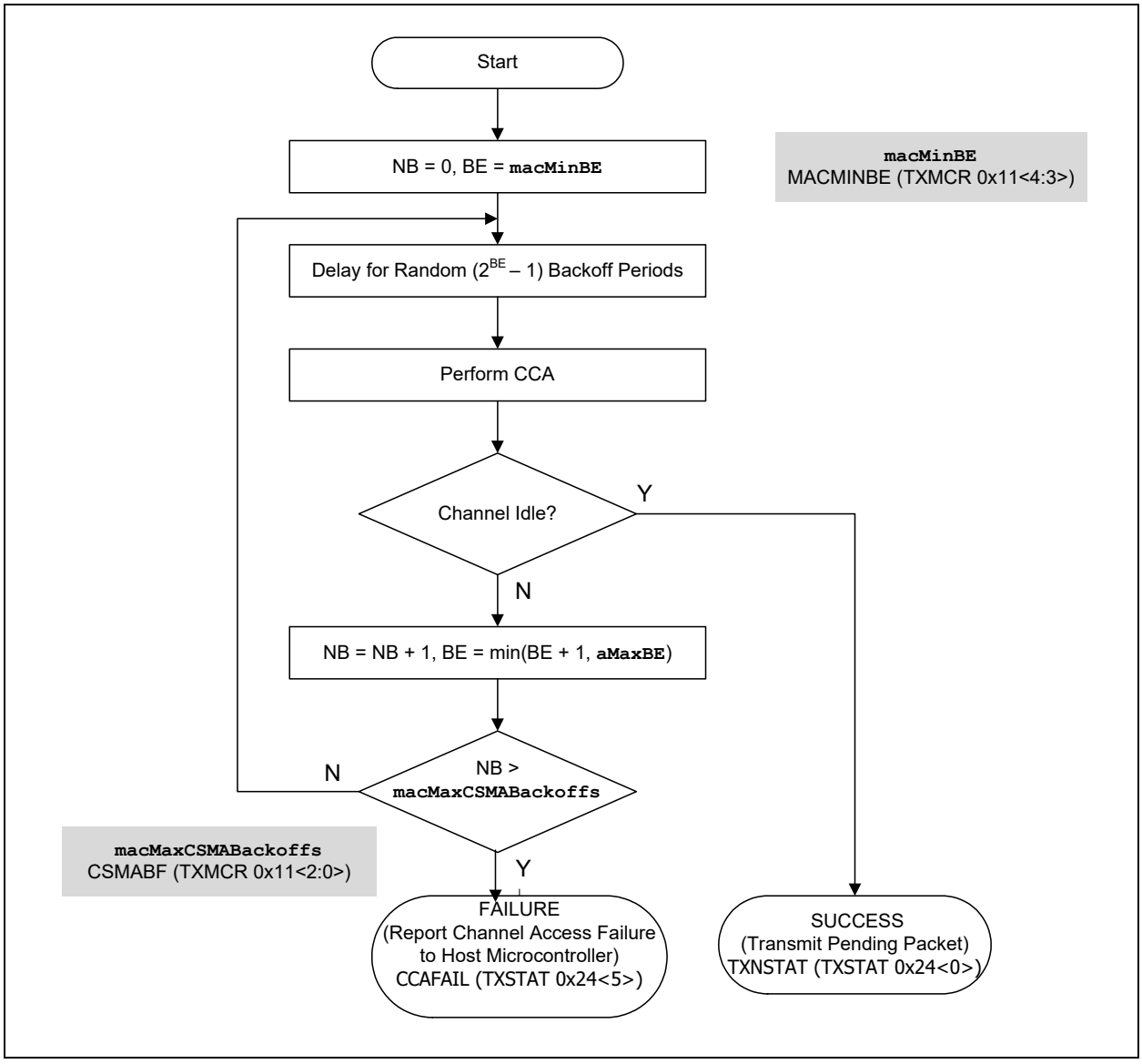
Note:	Acknowledgment and beacon frames are sent without using a CSMA-CA mechanism.

3.9.1 UNSLOTTED CSMA-CA MODE

Figure 3-6 shows the unslotted CSMA-CA algorithm. This mode is used in a nonbeacon-enabled network where the backoff periods of one device are not related in time to the backoff periods of any other device in the network. Refer to IEEE 802.15.4-2003, Section 7.5.1.3 "The CSMA-CA Algorithm" for more information.

Configuring the MRF24J40 for nonbeacon-enabled network operation is covered in **Section 3.8.2 "Nonbeacon-Enabled Network"**.

FIGURE 3-6: UNSLOTTED CSMA-CA ALGORITHM



To configure the MRF24J40 for Unslotted CSMA-CA mode, clear SLOTTED (TXMCR 0x11[5]) bit = 0.

The macMinBE and macMaxCSMABackoff values in the MRF24J40 are set to the IEEE 802.15.4 Standard defaults. To program their values:

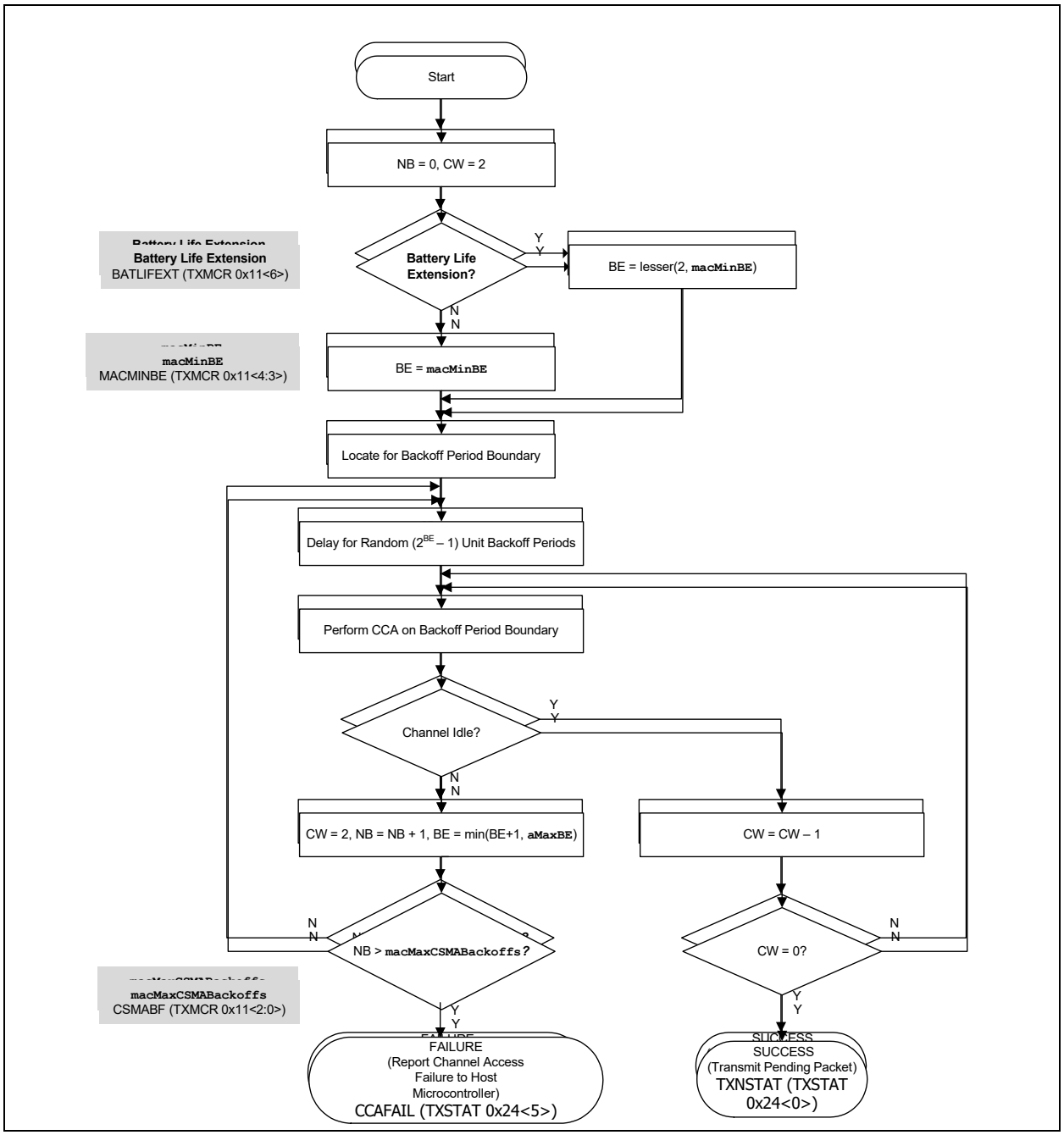
- macMinBE – Program MACMINBE (TXMCR 0x11[4:3]) bits to a value between 0 and 3 (the IEEE 802.15.4 Standard default is 3).
- macMaxCSMABackoff – Program CSMABF (TXMCR 0x11[2:0]) bits to a value between 0 and 5 (the IEEE 802.15.4 Standard default is 4).

3.9.2 SLOTTED CSMA-CA MODE

Figure 3-7 shows the slotted CSMA-CA algorithm. This mode is used on a beacon-enabled network where the backoff period boundaries of every device on the network shall be aligned with the superframe slot boundaries of the PAN coordinator. Refer to IEEE 802.15.4-2003, Section 7.5.1.3 "The CSMA-CA Algorithm" for more information.

Configuring the MRF24J40 for beacon-enabled network operation is covered in **Section 3.8.1 "Beacon-Enabled Network"**.

FIGURE 3-7: SLOTTED CSMA-CA ALGORITHM



To configure the MRF24J40 for Slotted CSMA-CA mode, set SLOTTED (TXMCR 0x11[5]) bit = 1.

To program the battery life extension bit in the Slotted CSMA-CA mode, set BATLIFEXT (TXMCR 0x11[6]) bit = 1.

The macMinBE and macMaxCSMABackoff values are set to the IEEE 802.15.4 Standard defaults. To change their values:

- macMinBE – Program MACMINBE (TXMCR 0x11[4:3]) bits to a value between 0 and 3 (the default is 3).
- macMaxCSMABackoff – Program CSMABF (TXMCR 0x11[2:0]) bits to a value between 0 and 5 (the default is 4).

TABLE 3-11: REGISTERS ASSOCIATED WITH CSMA-CA

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x11	TXMCR	NOCSMA	BATLIFEXT	SLOTTED	MACMINBE1	MACMINB0	CSMABF2	CSMABF1	CSMABF0

3.10 Interframe Spacing (IFS)

Interframe Spacing (IFS) allows the MAC sublayer time to process data received by the PHY. The length of the IFS period depends on the size of the frame that is to be transmitted. Frames up to aMaxSIFSFrameSize (18 octets) in length shall be followed by a SIFS period of at least aMinSIFSPeriod (12) symbols. Frames with lengths greater than aMaxSIFSFrameSize shall be followed by a LIFS period of at least aMinLIFSPeriod (40) symbols. If the transmission requires an Acknowledgment, the IFS shall follow the Acknowledgment frame. Figure 3-8 shows the relationship between frames and IFS periods. Refer to IEEE 802.15.4-2003, Section 7.5.1.2 “IFS” for more information.

The IEEE 802.15.4 Specification defines aMinSIFSPeriod as a constant value of 12 symbol periods. The aMinSIFSPeriod can be programmed by the MSIFS (TXSTBL 0x2E[3:0]) and RFSTBL (TXSTBL 0x2E[7:4]) bits, where aMinSIFSPeriod = MSIFS + RFSTBL.

The IEEE 802.15.4 Specification defines aMinLIFSPeriod as a constant value of 40 symbol periods. The aMinLIFSPeriod can be programmed by the MLIFS (TXPEND 0x21[7:2]) and RFSTBL (TXSTBL 0x2E[7:4]) bits, where aMinLIFSPeriod = MLFS + RFSTBL.

The IEEE 802.15.4 Specification defines aTurnaroundTime as a constant value of 12 symbol periods. The aTurnaroundTime can be programmed by the TURNTIME (TXTIME 0x27[7:4]) and RFSTBL (TXSTBL 0x2E[7:4]) bits, where aTurnaroundTime = TURNTIME + RFSTBL.

FIGURE 3-8: INTERFRAME SPACING (IFS)

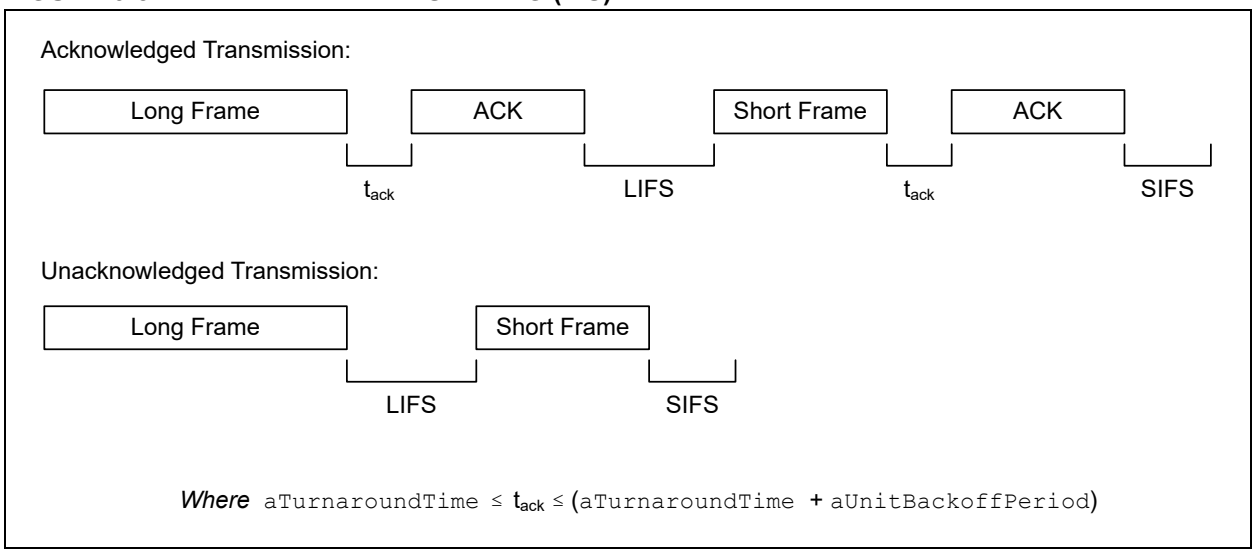


TABLE 3-12: REGISTERS ASSOCIATED WITH INTERFRAME SPACING

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x21	TXPEND	MLIFS5	MLIFS4	MLIFS3	MLIFS2	MLIFS1	MLIFS0	GTSSWITCH	FPACK
0x27	TXTIME	TURNTIME3	TURNTIME2	TURNTIME1	TURNTIME0	r	r	r	r
0x2E	TXSTBL	RFSTBL3	RFSTBL2	RFSTBL1	RFSTBL0	MSIFS3	MSIFS2	MSIFS1	MSIFS0

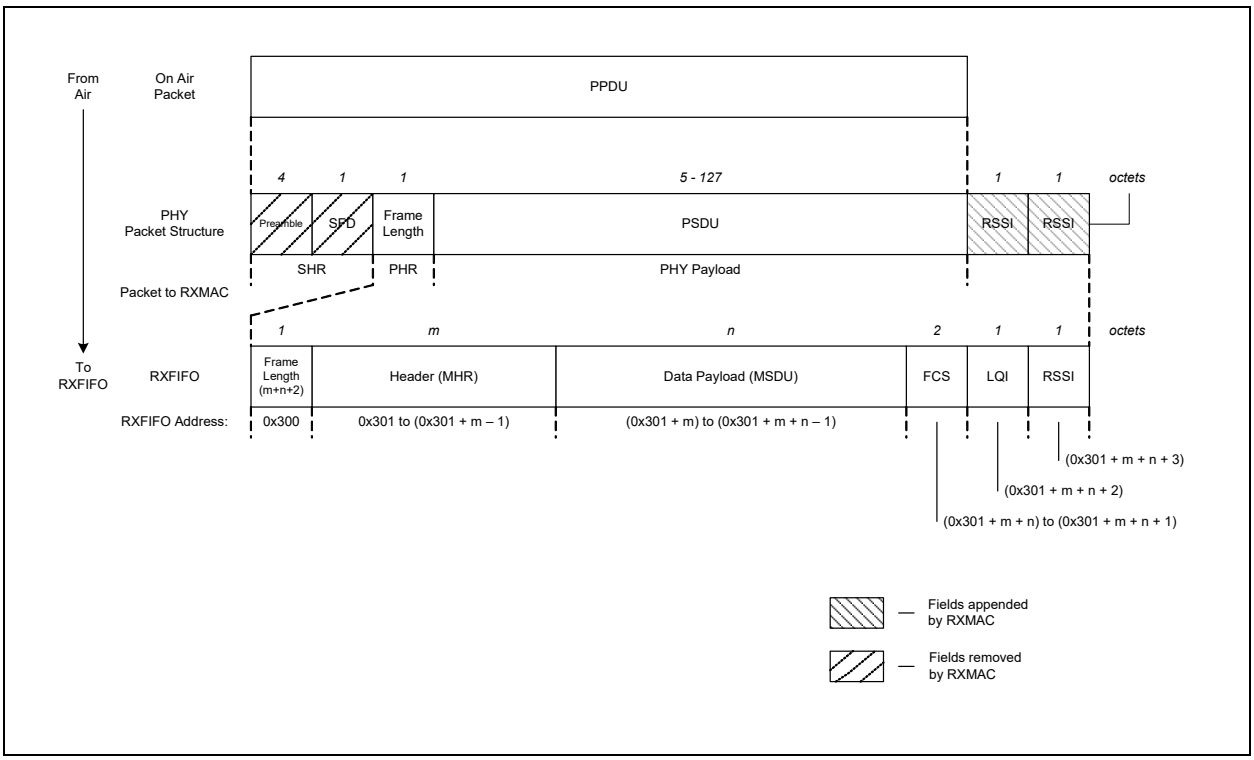
3.11 Reception

An IEEE 802.15.4 compliant packet is prefixed with a Synchronization Header (SHR) containing the preamble sequence and Start-of-Frame Delimiter (SFD) fields. The preamble sequence enables the receiver to achieve symbol synchronization.

The MRF24J40 monitors incoming signals and looks for the preamble of IEEE 802.15.4 packets. When a valid synchronization is obtained, the entire packet is demodulated and the CRC is calculated and checked. The packet is accepted or rejected depending on the reception mode and frame filter, and placed in the RXFIFO buffer. When the packet is placed in the RXFIFO, a Receive Interrupt (RXIF 0x31[3]) is issued. The RXFIFO address mapping is shown in Figure 3-9.

The following sections detail the reception operation of the MRF24J40.

FIGURE 3-9: PACKET RECEPTION



3.11.1 RECEPTION MODES

The MRF24J40 can be configured for one of three different Reception modes as shown in Table 3-13. An explanation of each of the modes follows.

TABLE 3-13: RECEPTION MODES

Receive Mode	RXMCR (0x00[1:0])
Normal	00 (default)
Error	10
Promiscuous	01

3.11.1.1 Normal Mode

Normal mode accepts only packets with a good CRC and satisfies the requirements of the IEEE 802.15.4 Specification, Section 7.5.6.2 “Reception and Rejection”:

1. The frame type subfield of the frame control field shall not contain an illegal frame type.
2. If the frame type indicates that the frame is a beacon frame, the source PAN identifier shall match macPANId unless macPANID is equal to 0xFFFF, in which case, the beacon frame will be accepted regardless of the source PAN identifier.
3. If a destination PAN identifier is included in the frame, it shall match macPANId or shall be the broadcast PAN identifier (0xFFFF).
4. If a short destination address is included in the frame, it shall match either macShortAddress or the broadcast address (0xFFFF). Otherwise, if an extended destination address is included in the frame, it shall match aExtendedAddress.
5. If only source addressing fields are included in a data or MAC command frame, the frame shall be accepted only if the device is a PAN coordinator and the source PAN identifier matches macPANId.

3.11.1.2 Error Mode

Error mode accepts packets with good or bad CRC.

3.11.1.3 Promiscuous Mode

Promiscuous mode accepts all packets with a good CRC.

3.11.2 FRAME FORMAT FILTER

Once the packet has been accepted, depending on the Reception mode above, the frame format is filtered according to Table 3-14. Command, data or beacon only frames can be filtered and placed in the RXFIFO buffer. All frames (default) can be selected placing all frame formats (command, data and beacon) in the RXFIFO.

TABLE 3-14: FRAME FORMAT FILTER

Filter Mode	RXFLUSH (0x0D[3:1])
All Frames	000 (default)
Command Only	100
Data Only	010
Beacon Only	001

3.11.3 ACKNOWLEDGMENT REQUEST

If the received packet has the Acknowledgment request bit set to ‘1’ (bit 5 of the Frame Control Field – refer to IEEE 802.15.4 Standard, Section 7.2.1.1 “Frame Control Field”), the TXMAC circuitry will send an Acknowledgment packet automatically. This feature minimizes the processing duties of the host microcontroller and keeps the Acknowledgment timing within the IEEE 802.15.4 Specification.

The sequence number field of the Acknowledgment frame will contain the value of the sequence number of the received frame for which the Acknowledgment is to be sent.

Refer to **Section 3.13 “Acknowledgement”** for more information.

3.11.4 RECEIVE INTERRUPT

Once the packet is accepted, depending on the Reception mode (Normal, Error or Promiscuous) and frame format (all, command, data or beacon), it is placed in the RXFIFO buffer and a Receive Interrupt (RXIF 0x31[3]) is issued.

Note:	The INTSTAT (0x31) register clears-to-zero upon read. Therefore, the host microcontroller should read and store the INTSTAT register and check the bits to determine which interrupt occurred. Refer to **Section 3.3 “Interrupts”** for more information.

Data is placed into the RXFIFO buffer as shown in Figure 3-9. The host processor reads the RXFIFO via the SPI port by reading addresses, 0x300-0x38F. Address, 0x300, contains the received packet frame length which includes the header length, data payload length, plus 2 for the FCS bytes. An LQI and RSSI value comes after the FCS. Refer to **Section 3.6 “Received Signal Strength Indicator (RSSI)/Energy Detection (ED)”** and **Section 3.7 “Link Quality Indication (LQI)”** for more information.

The RXFIFO is a 128-byte dual port buffer. The RXMAC circuitry places the packet into the RXFIFO sequentially, byte by byte, using an internal pointer. The internal pointer is reset one of three ways:

1. When the host microcontroller reads the first byte of the packet.
2. Manually by setting the RXFLUSH (0x0D[0]) bit. The bit is automatically cleared to '0' by hardware.
3. Software Reset (see **Section 3.1 "Reset"** for more information).

The RXFIFO can only hold one packet at a time. It is highly recommended that the host microcontroller read the entire RXFIFO without interruption so that received packets are not missed.

Note:	When the first byte of the RXFIFO is read, the MRF24J40 is ready to receive the next packet. To avoid receiving a packet while the RXFIFO is being read, set the Receive Decode Inversion (RXDECINV) bit (0x39[2]) to '1' to disable the MRF24J40 from receiving a packet off the air. Once the data is read from the RXFIFO, the RXDECINV should be cleared to '0' to enable packet reception.

Example 3-2 shows example steps to read the RXFIFO.

EXAMPLE 3-2: STEPS TO READ RXFIFO

Example steps to read the RXFIFO:

1. Receive RXIF interrupt.
2. Disable host microcontroller interrupts.
3. Set RXDECINV = 1; disable receiving packets off air.
4. Read address, 0x300; get RXFIFO frame length value.
5. Read RXFIFO addresses, 0x301 through (0x300 + Frame Length + 2); read packet data plus LQI and RSSI.
6. Clear RXDECINV = 0; enable receiving packets.
7. Enable host microcontroller interrupts.

3.11.5 SECURITY

If the received packet has the security enabled bit set to '1' (bit 3 of the frame control field; refer to IEEE 802.15.4 Standard, Section 7.2.1.1 "Frame Control Field") a Security Interrupt (SECIF 0x31[4]) is issued. The host microcontroller can then decide to decrypt or ignore the packet. See **Section 3.17 "Security"** for more information.

TABLE 3-15: REGISTERS ASSOCIATED WITH RECEPTION

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	RXMCR	r	r	NOACKRSP	r	PANCOORD	COORD	ERRPKT	PROMI
0x0D	RXFLUSH	r	WAKEPOL	WAKEPAD	r	CMDONLY	DATAONLY	BCNONLY	RXFLUSH
0x2A	SOFTRST	r	r	r	r	r	RSTPWR	RSTBB	RSTMAC
0x31	INSTAT	SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF
0x32	INTCON	SLPIE	WAKEIE	HSYMTMRIE	SECIE	RXIE	TXG2IE	TXG1IE	TXNIE
0x39	BBREG1	r	r	r	r	r	RXDECINV	r	r

3.12 Transmission

IEEE 802.15.4 Standard defines four frame types: Acknowledgment, Data, Beacon and MAC Command frame. The transmission of the Acknowledgment frame is handled automatically in hardware by the MRF24J40 and is covered in **Section 3.13 "Acknowledgement"**. Hardware management of the transmission of data, beacon and MAC command frames are handled in four transmit (TX) FIFOs.

Each TX FIFO has a specific purpose depending on if the MRF24J40 is configured for Beacon or Non-beacon-Enabled mode. Configuring the MRF24J40 for beacon-enabled network operation is covered in **Section 3.8.1 "Beacon-Enabled Network"**. Configuring the MRF24J40 for nonbeacon-enabled network operation is covered in **Section 3.8.2 "Nonbeacon-Enabled Network"**.

The four TX FIFOs are:

TX Normal FIFO – Used for the transmission of data and MAC command frames during the Contention Access Phase (CAP) of the superframe if the device is operating in Beacon-Enabled mode and for all transmissions when the device is operating in Nonbeacon-Enabled mode.

TX Beacon FIFO – Used for the transmission of the beacon frames.

TX GTS1 FIFO and TX GTS2 FIFO – Used for the transmission of data during the Contention Free Period (CFP) of the superframe if the device is operating in Beacon-Enabled mode. Refer to **Section 3.8.1 "Beacon-Enabled Network"** for more information about guaranteed time slots in Beacon-Enabled mode.

Figure 3-10 summarizes the memory map for each of the TX FIFOs. Each TX FIFO occupies 128 bytes of memory and can hold one frame at a time.

Figure 3-11 shows the flow of data from the TX FIFO to on air packet and summarizes the data, beacon and MAC command frames.

FIGURE 3-10: MEMORY MAP OF TX FIFOS

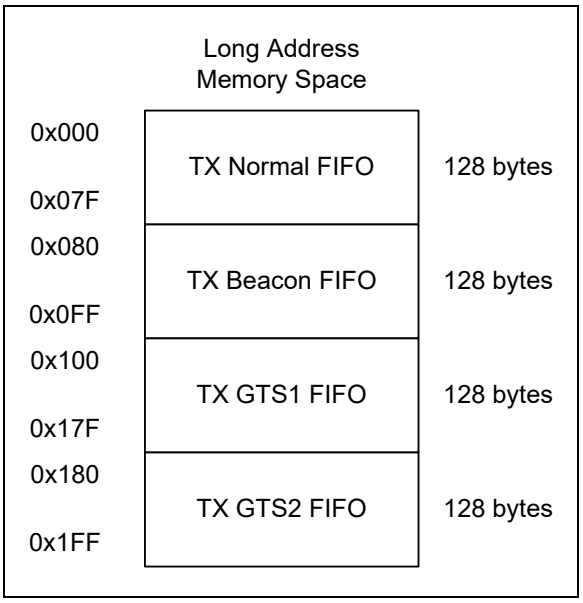
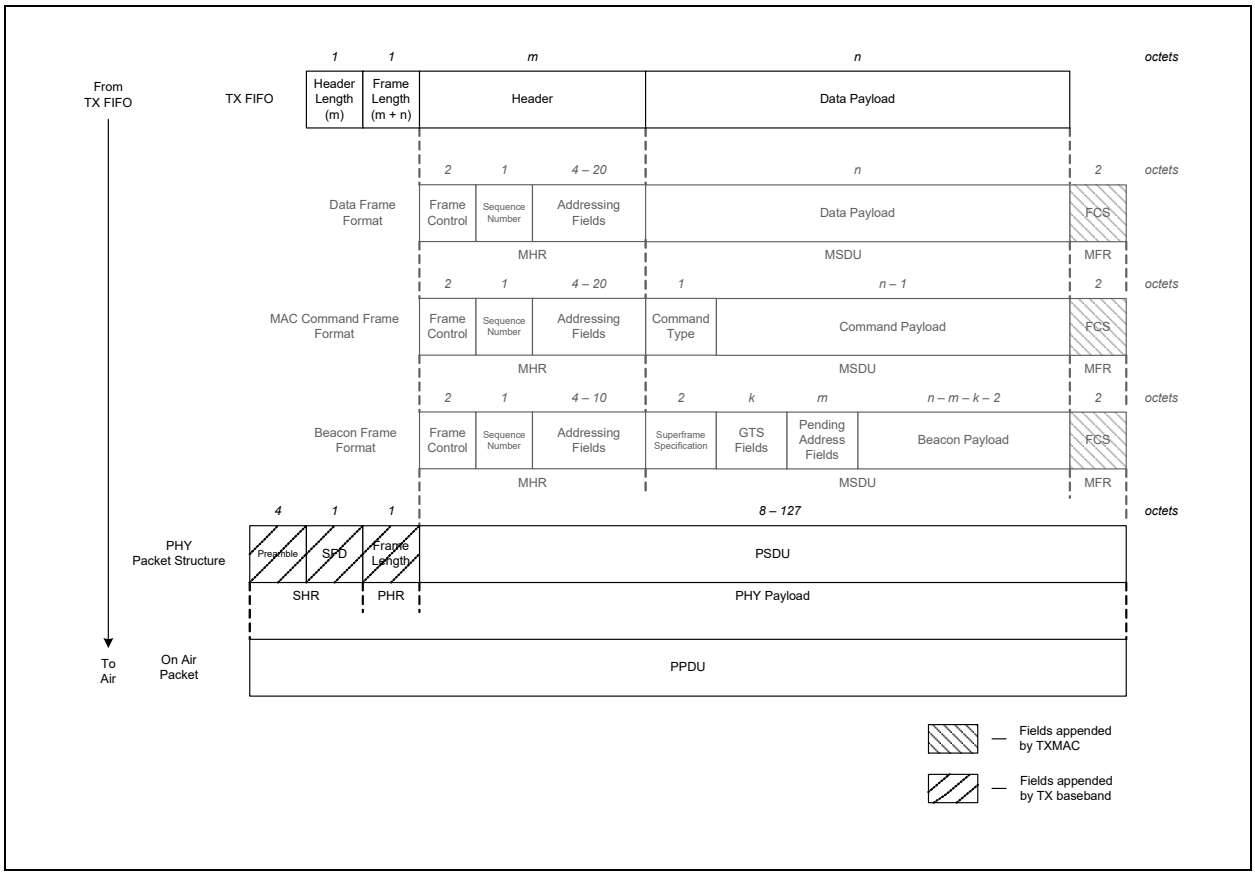


FIGURE 3-11: PACKET TRANSMISSION



3.12.1 TX FIFOs FRAME STRUCTURE

The TX FIFOs are divided into four fields:

Header length – Used primarily in Security mode and contains the length, in octets (bytes), of the MAC Header (MHR). In Unsecure mode, this field is ignored.

Note:	The header length field as implemented in the MRF24J40 is 5-bits long. Therefore, the header length maximum value is 31 octets (bytes).

Frame length – Contains the length, in octets (bytes), of the MAC Header (MHR) and data payload.

Header – Contains the MAC Header (MHR).

Payload – Contains the data payload.

When the individual TX FIFO is triggered, the MRF24J40 will handle transmitting the packet using the CSMA-CA algorithm, Acknowledgment of the packet (optional), retransmit if Acknowledgment not received within required time period and interframe spacing. The MRF24J40 will add the Synchronization Header (SHR), PHY Header (PHR) and Frame Check Sequence (FCS) automatically. If a packet is to be transmitted using in-line security, the Message Integrity Code (MIC) will be appended in the data payload by the MRF24J40. Refer to **Section 3.17 "Security"** for more information about transmitting and receiving data in Security mode. In Beacon-Enabled mode, the MRF24J40 will handle superframe timing, transmission of the beacon and data packets during CAP and CFP.

3.12.2 TX NORMAL FIFO

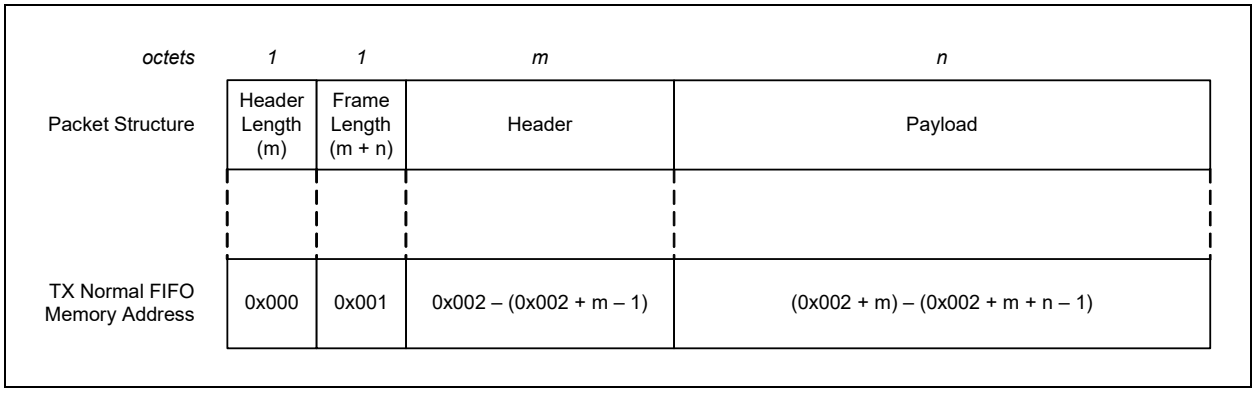
In Beacon-Enabled mode, the TX Normal FIFO is used for the transmission of data and MAC command frames during the Contention Access Phase (CAP) of the superframe.

In Nonbeacon-Enabled mode, the TX Normal FIFO is used for all transmissions.

To transmit a packet in the TX Normal FIFO, perform the following steps:

1. The host processor loads the TX Normal FIFO with IEEE 802.15.4 compliant data or MAC command frame using the format shown in Figure 3-12.

FIGURE 3-12: TX NORMAL FIFO FORMAT



2. If the packet requires an Acknowledgment, the Acknowledgment request bit in the frame control field should be set to '1' in the MAC Header (MHR) when the host microcontroller loads the TX Normal FIFO, and set the TXNACKREQ (TXNCON 0x1B[2]) bit = 1. Refer to **Section 3.13 "Acknowledgement"** for more information about Acknowledgment configuration.
3. If the frame is to be encrypted, the security enabled bit in the frame control field should be set to '1' in the MAC Header (MHR) when the host microcontroller loads the TX Normal FIFO, and set the TXNSECEN (TXNCON 0x1B[1]) bit = 1. Refer to **Section 3.17 "Security"** for more information about Security modes.
4. Transmit the packet by setting the TXNTRIG (TXNCON 0x1B[0]) bit = 1. The bit will be automatically cleared by hardware.
5. A TXNIF (INTSTAT 0x31[0]) interrupt will be issued. The TXNSTAT (TXSTAT 0x24[0]) bit indicates the status of the transmission:

   TXNSTAT = 0: Transmission was successful

   TXNSTAT = 1: Transmission failed, retry count exceeded

   The number of retries of the most recent transmission is contained in the TXNRETRY (TXSTAT 0x24[7:6]) bits. The CCAFAIL (TXSTAT 0x24[5]) bit = 1 indicates if the failed transmission was due to the channel busy (CSMA-CA timed out).

3.12.3 TX BEACON FIFO

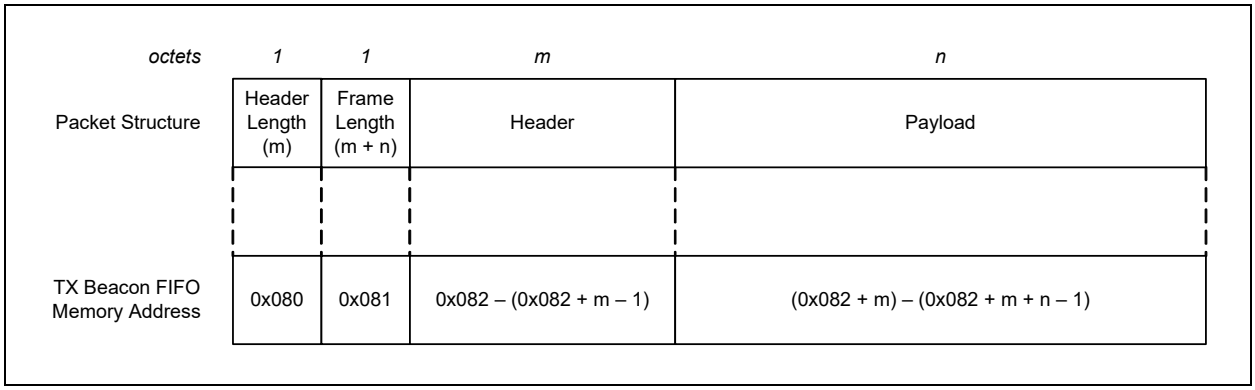
In Beacon-Enabled mode, the TX Beacon FIFO is used for the transmission of beacon frames during the beacon slot of the superframe.

In Nonbeacon-Enabled mode, the TX Beacon FIFO is used for the transmission of a beacon frame at the time it is triggered (transmitted).

To transmit a packet in the TX Beacon FIFO, perform the following steps:

1. The host processor loads the TX Beacon FIFO with an IEEE 802.15.4 compliant beacon frame using the format shown in Figure 3-13.

FIGURE 3-13: TX BEACON FIFO FORMAT



2. If the beacon frame is to be encrypted, the security enabled bit in the frame control field should be set to '1' in the MAC Header (MHR) when the host microcontroller loads the TX Beacon FIFO, and set the TXBSECEN (TXBCON 0x1A[1]) bit = 1. Refer to **Section 3.17 "Security"** for more information about Security modes.
3. Transmit the packet by setting the TXBTRIG (TXBCON 0x1A[0]) bit = 1. The bit will be automatically cleared by hardware. If the MRF24J40 is configured for Beacon-Enabled mode, the beacon frame will be transmitted at the beacon slot time at the beginning of the superframe. In Nonbeacon-Enabled mode, the beacon frame is transmitted at the time of triggering.

3.12.4 TX GTSx FIFO

In Beacon-Enabled mode, the TX GTSx FIFOs are used for the transmission of data or MAC command frames during the CFP of the superframe. Refer to **Section 3.8.1 "Beacon-Enabled Network"** for more information about guaranteed time slots in Beacon-Enabled mode.

To transmit a packet in the TX GTSx FIFO, perform the following steps:

1. The host processor loads the respective TX GTSx FIFO with an IEEE 802.15.4 compliant data or MAC command frame using the format shown in Figure 3-14.

FIGURE 3-14: TX GTS1 AND GTS2 FIFOS FORMAT

octets	*1*	*1*	*m*	*n*
Packet Structure	Header Length (m)	Frame Length (m + n)	Header	Payload
TX GTS1 FIFO Memory Address	0x100	0x101	0x102 – (0x102 + m – 1)	(0x102 + m) – (0x102 + m + n – 1)
TX GTS2 FIFO Memory Address	0x180	0x181	0x182 – (0x182 + m – 1)	(0x182 + m) – (0x182 + m + n – 1)

2. If the packet requires an Acknowledgment, the Acknowledgment request bit in the frame control field should be set to '1' in the MAC Header (MHR) when the host microcontroller loads the respective TX GTSx FIFO, and set the TXG1ACKREQ (TXG1CON 0x1C[2]) or TXG2ACKREQ (TXG2CON 0x1D[2]) bit = 1. Refer to **Section 3.13 "Acknowledgement"** for more information about Acknowledgment configuration.
3. Program the number of retry times for the respective TX GTSx FIFO in the TXG1RETRY (TXG1CON 0x1C[7:6]) or TXG2RETRY (TXG2CON 0x1D[7:6]) bits.
4. If the frame is to be encrypted, the security enabled bit in the frame control field should be set to '1' in the MAC Header (MHR) when the host microcontroller loads the TX GTSx FIFO, and set the TXG1SECEN (TXG1CON 0x1C[1]) or TXG2SECEN (TXG2CON 0x1D[1]) bit = 1. Refer to **Section 3.17 "Security"** for more information about Security modes.
5. Program the slot number for the respective TX GTSx FIFO in the TXG1SLOT (TXG1CON 0x1C[5:3] or TXG2SLOT (TXG2CON 0x1D[5:3]) bits.
6. Transmit the packet in the respective TX GTSx FIFO by setting the TXG1TRIG (TXG1CON 0x1C[0]) or TXG2TRIG (TXG2CON 0x1D[0]) bit = 1. The bit will be automatically cleared by hardware. The packet will be transmitted at the corresponding slot time of the superframe.
7. A TXG1IF (INTSTAT 0x31[1]) or TXG2IF (INTSTAT 0x31[2]) interrupt will be issued. The TXG1STAT (TXSTAT 0x24[1]) or TXG2STAT (TXSTAT 0x24[2]) bit indicates the status of the transmission:

   TXGxSTAT = 0: Transmission was successful

   TXGxSTAT = 1: Transmission failed, retry count exceeded

   The number of retries of the most recent transmission is contained in the TXG1RETRY (TXG1CON 0x1C[7:6]) or TXG2RETRY (TXG2CON 0x1D[7:6]) bits. The CCAFAIL (TXSTAT 0x24[5]) bit = 1 indicates if the failed transmission was due to the channel busy (CSMA-CA timed out). The TXG1FNT (TXSTAT 0x24[3]) or TXG2FNT (TXSTAT 0x24[4]) bit = 1 indicates if the TX GTSx FIFO transmission failed due to not enough time to transmit in the guaranteed time slot.

TABLE 3-16: REGISTERS ASSOCIATED WITH TRANSMISSION

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1A	TXBCON0	r	r	r	r	r	r	TXBSECEN	TXBTRIG
0x1B	TXNCON	r	r	r	FPSTAT	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG
0x1C	TXG1CON	TXG1RETRY1	TXG1RETRY0	TXG1SLOT2	TXG1SLOT1	TXG1SLOT0	TXG1ACKREQ	TXG1SECEN	TXG1TRIG
0x1D	TXG2CON	TXG2RETRY1	TXG2RETRY0	TXG2SLOT2	TXG2SLOT1	TXG2SLOT0	TXG2ACKREQ	TXG2SECEN	TXG2TRIG
0x24	TXSTAT	TXNRETRY1	TXNRETRY0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2STAT	TXG1STAT	TXNSTAT
0x31	INTSTAT	SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF
0x32	INTCON	SLPIE	WAKEIE	HSYMTMRIE	SECIE	RXIE	TXG2IE	TXG1IE	TXNIE

3.13 Acknowledgement

An Acknowledgment frame is used for confirming successful frame reception. The successful reception of a data or MAC command frame can be optionally confirmed with an Acknowledgment frame. If the originator does not receive an Acknowledgment after, at most macAckWaitDuration (54) symbols, it assumes that the transmission was unsuccessful and retries the frame transmission. The turnaround time from the reception of the packet to the transmission of the Acknowledgment shall be less than aTurnaroundTime (12) symbols. Acknowledgment frames are sent without using a CSMA-CA mechanism. Refer to IEEE 802.15.4-2003 Standard, Section 7.5.6.4 "Use of Acknowledgments" for more information.

The MRF24J40 provides hardware support for:

- Acknowledgment Request – Originator
- Acknowledgment Request – Recipient
- Reception of Acknowledgment with Frame Pending bit
- Transmission of Acknowledgment with Frame Pending bit

These features are explained below.

3.13.1 ACKNOWLEDGMENT REQUEST – ORIGINATOR

A data or MAC command frame, transmitted by an originator with the Acknowledgment request subfield in its frame control field set to '1', shall be Acknowledged by the recipient. The originator shall wait for at most macAckWaitDuration (54) symbols for the corresponding Acknowledgment frame to be received. If an Acknowledgment is received, the transmission is successful. If an Acknowledgment is not received, the originator shall conclude that the transmission failed. If the transmission was direct, the originator shall retransmit the data or MAC command frame and wait. If an Acknowledgment is not received after aMaxFrameRetries (3) transmissions, the originator shall assume the transmission has failed and notify the upper layers of the failure.

The MRF24J40 features hardware retransmit. It will automatically retransmit the packet if an Acknowledgment has not been received. The Acknowledgment request bit in the frame control field should be programmed into the transmit FIFO of interest and the applicable xACKREQ bit should be set:

- TXNACKREQ (TXNCON 0x1B[2]) – When the TX Normal FIFO transmits a frame, an Acknowledgment frame is expected. If an Acknowledgment is not received, retransmit.
- TXG1ACKREQ (TXG1CON 0x1C[2]) – When the TX GTS1 FIFO transmits a frame, an Acknowledgment frame is expected. If an Acknowledgment is not received, retransmit.
- TXG2ACKREQ (TXG2CON 0x1D[2]) – When the TX GTS2 FIFO transmits a frame, an Acknowledgment frame is expected. If an Acknowledgment is not received, retransmit.

When the frame is transmitted, the MRF24J40 will expect an Acknowledgment frame within macAckWaitDuration. If an Acknowledgment is not received, it will retransmit aMaxFrameRetries.

The macAckWaitDuration value can be programmed by the MAWD (ACKTMOUT 0x12[6:0]) bits.

The aMaxFrameRetries value is a constant and not configurable. The number of retry times of the most recent TXNFIFO transmission can be read in the TXNRETRY (TXSTAT 0x24[7:6]) bits. The number of retry times for the TX GTS1 FIFO and TX GTS2 FIFO can be programmed or read in the TXG1RETRY (TXG1CON 0x1C[7:6]) and TXG2RETRY (TXG2CON 0x1D[7:6]) bits.

3.13.2 ACKNOWLEDGMENT REQUEST – RECIPIENT

The MRF24J40 features hardware automatic Acknowledgment. It will automatically Acknowledge a frame if the received frame has the Acknowledgment request subfield in the frame control field set to '1'. This will maintain the RX-TX timing requirements of the IEEE 802.15.4 Specification.

Automatic Acknowledgment is enabled by clearing the NOACKRSP (RXMCR 0x00[5]) bit = 0. To disable automatic Acknowledgment, set the NOACKRSP (RXMCR 0x00[5]) bit = 1.

The transmission of an Acknowledgment frame in a nonbeacon-enabled network, or in the CFP, shall commence aTurnaroundTime (12) symbols after the reception of the data or MAC command frame. The transmission of an Acknowledgment frame in the CAP shall commence at a backoff slot boundary. In this case, the transmission of an Acknowledgment frame shall commence between aTurnaroundTime and (aTurnaroundTime + aUnitBackoffPeriod) symbols after the reception of the data or MAC command frame.

The IEEE 802.15.4 Specification defines aTurnaroundTime as a constant value of 12 symbol periods. The aTurnaroundTime can be programmed by the TURNTIME (TXTIME 0x27[7:4]) and RFSTBL (TXSTBL 0x2E[7:4]) bits where aTurnaroundTime = TURNTIME + RFSTBL.

3.13.3 RECEPTION OF ACKNOWLEDGMENT WITH FRAME PENDING BIT

The status of the frame pending bit in the frame control field of the received Acknowledgment frame is reflected in the FPSTAT (TXNCON 0x1B[4]) bit.

3.13.4 TRANSMISSION OF ACKNOWLEDGMENT WITH FRAME PENDING BIT

The frame pending bit in the frame control field of an Acknowledgment frame indicates that a device has additional data to send to the recipient following the current transfer. Refer to IEEE 802.15.4-2003 Standard, Section 7.2.1.1.3 "Frame Pending Subfield".

Acknowledgment of a data request MAC command – In response to a data request MAC command, if the MRF24J40 has additional (pending) data, it can set the frame pending bit of the Acknowledgment frame by setting DRPACK (ACKTMOUT 0x12[7]) = 1. This will only set the frame pending bit for an Acknowledgment of a data request MAC command.

TABLE 3-17: REGISTERS ASSOCIATED WITH ACKNOWLEDGEMENT

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	RXMCR	r	r	NOACKRSP	r	PANCOORD	COORD	ERRPKT	PROMI
0x12	ACKTMOUT	DRPACK	MAWD6	MAWD5	MAWD4	MAWD3	MAWD2	MAWD1	MAWD0
0x1B	TXNCON	r	r	r	FPSTAT	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG
0x1C	TXG1CON	TXG1RETRY1	TXG1RETRY0	TXG1SLOT2	TXG1SLOT1	TXG1SLOT0	TXG1ACKREQ	TXG1SECEN	TXG1TRIG
0x1D	TXG2CON	TXG2RETRY1	TXG2RETRY0	TXG2SLOT2	TXG2SLOT1	TXG2SLOT0	TXG2ACKREQ	TXG2SECEN	TXG2TRIG
0x21	TXPEND	MLIFS5	MLIFS4	MLIFS3	MLIFS2	MLIFS1	MLIFS0	GTSSWITCH	FPACK
0x24	TXSTAT	TXNRETRY1	TXNRETRY0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2STAT	TXG1STAT	TXNSTAT
0x27	TXTIME	TURNTIME3	TURNTIME2	TURNTIME1	TURNTIME0	r	r	r	r
0x2E	TXSTBL	RFSTBL3	RFSTBL2	RFSTBL1	RFSTBL0	MSIFS3	MSIFS2	MSIFS1	MSIFS0

3.14 Battery Monitor

The MRF24J40 provides a battery monitor feature to monitor the system supplied voltage. A threshold voltage level (BATTH) can be set and the system supplied voltage can be monitored by the Battery Low Indicator (BATIND) to determine if the voltage is above or below the threshold. The following steps set the threshold and enable battery monitoring:

1. Set the battery monitor threshold (BATTH) voltage in the RFCON5 (0x205[7:4]) register.
2. Enable battery monitoring by setting BATEN = 1 in the RFCON6 (0x206[3]) register.
3. Periodically, monitor the Battery Low Indicator (BATIND) bit in the RXSR (0x30[5]) register to determine if the system supply voltage is above or below the battery monitor threshold (BATTH).

TABLE 3-18: REGISTERS ASSOCIATED WITH POWER MANAGEMENT

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x30	RXSR	r	UPSECERR	BATIND	r	r	SECDECERR	r	r
0x205	RFCON5	BATTH3	BATTH2	BATTH1	BATTH0	r	r	r	r
0x206	RFCON6	TXFIL	r	r	20MRECVR	BATEN	r	r	r

3.15 Sleep

The MRF24J40 can be placed into a low-current Sleep mode. During Sleep, the 20 MHz main oscillator is turned off, disabling the RF, baseband and MAC circuitry. Data is retained in the control and FIFO registers and the MRF24J40 is accessible via the SPI port. There are two Sleep modes:

- Timed Sleep Mode
- Immediate Sleep and Wake Mode

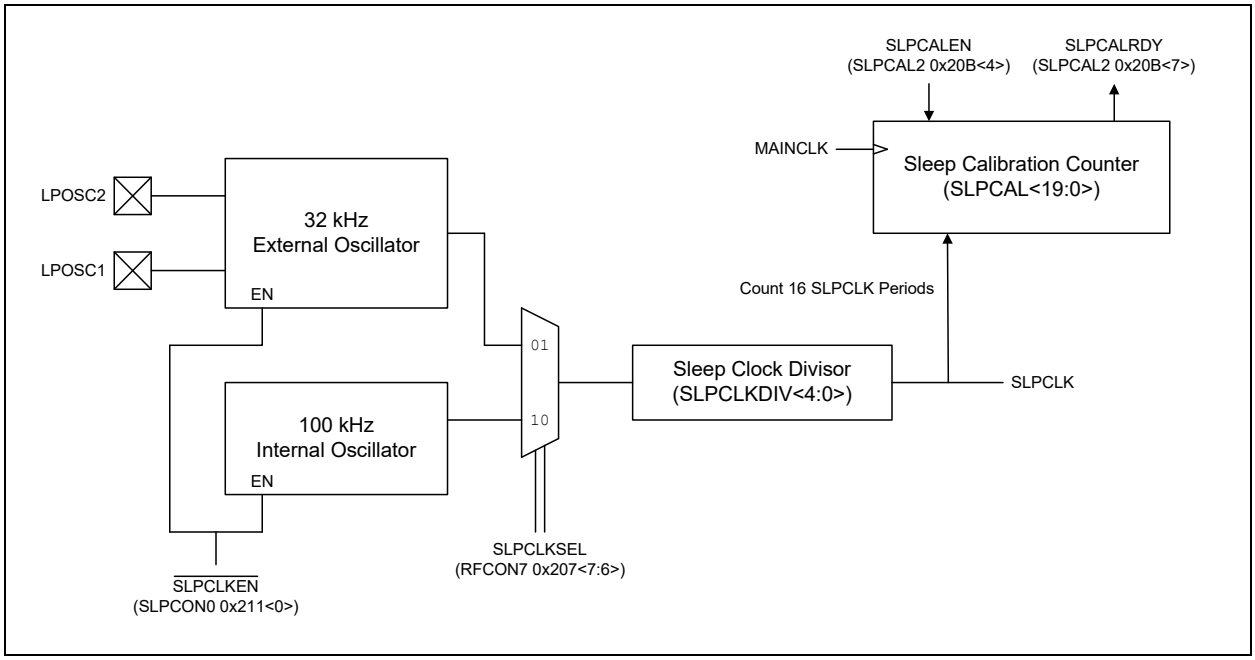
3.15.1 TIMED SLEEP MODE

The Timed Sleep Mode uses several counters to time events for the Sleep and wake-up of the MRF24J40. The following sections cover Sleep clock generation, calibration and counters.

3.15.1.1 Sleep Clock Generation

Figure 3-15 shows the Sleep clock generation circuitry. The Sleep Clock (SLPCLK) frequency is selectable between a 100 kHz internal oscillator or a 32 kHz external crystal oscillator. The Sleep Clock Enable (SLPCLKEN) bit in the SLPCON0 (0x211[0]) register can enable (SLPCLKEN = 0; default setting) or disable (SLPCLKEN = 1) the Sleep clock oscillators. The SLPCLK frequency can be further divided by the Sleep Clock Divisor (SLPCLKDIV) 0x220[4:0] bits. The SLPCLK frequency can be calibrated; the procedure is listed in **Section 3.15.1.2 "Sleep Clock Calibration"** below.

FIGURE 3-15: SLEEP CLOCK GENERATION



The 100 kHz internal oscillator requires no external components. However, it is not as accurate or stable as the 32 kHz external crystal oscillator. It is recommended that it be calibrated before use. See **Section 3.15.1.2 "Sleep Clock Calibration"** below for the Sleep clock calibration procedure.

To select the 100 kHz internal oscillator as the source of SLPCLK, set the SLPCLKSEL bits (RFCON7 0x207[7:6] to '10')

The 32 kHz external crystal oscillator provides better frequency accuracy and stability than the 100 kHz internal oscillator. The 32 kHz external crystal oscillator external circuitry is explained in detail in **Section 2.7 "32 kHz External Crystal Oscillator"**.

To select the 32 kHz external crystal oscillator as the source of SLPCLK, set the SLPCLKSEL bits (RFCON7 0x207[7:6]) to '01'.

3.15.1.2 Sleep Clock Calibration

The SLPCLK frequency is calibrated by a 20-bit SLPCAL register clocked by the 20 MHz main oscillator (50 ns period). Sixteen samples of the SLPCLK are counted and stored in the SLPCAL register. To perform SLPCLK calibration:

1. Select the source of SLPCLK.
2. Begin calibration by setting the SLPCALEN bit (SLPCAL2 0x20B[4]) to '1'. Sixteen samples of the SLPCLK are counted and stored in the SLPCAL register.
3. Calibration is complete when the SLPCALRDY bit (SLPCAL2 0x20B[7]) is set to '1'.

The 20-bit SLPCAL value is contained in registers, SLPCAL2, SLPCAL1 and SLPCAL0 (0x20B[3:0], 0x20A and 0x209). The Sleep clock period is calculated as shown in Equation 3-2.

EQUATION 3-2:

$$P_{SLPCAL} = SLPCAL * 50\ ns/16$$

The SLPCLK frequency can be slowed by setting the Sleep Clock Division (SLPCLKDIV) bits (SLPCON1 0x220[4:0]).

3.15.1.3 Sleep Mode Counters

Figure 3-16 shows the Sleep mode counters. A summary of the counters are:

Main Counter (0x229[1:0], 0x228, 0x227, 0x226) – A 26-bit counter clocked by SLPCLK. Together with the Remain Counter times events as listed in Table 3-19.

Remain Counter (0x225, 0x224) – A 16-bit counter clocked by MAINCLK. Together with the Main Counter times events as listed in Table 3-19.

Wake Time (0x223[2:0], 0x222) – An 11-bit value that is compared with the main counter value to signal the time to enable (wake-up) the 20 MHz main oscillator. Table 3-20 gives the recommended values for WAKETIME depending on the SLPCLK frequency.

Wake Count (0x36[4:3], 0x35[6:0]) – A 9-bit counter clocked by SLPCLK. During the time the wake counter is counting, the 20 MHz main oscillator is starting up, stabilizing and disabled to the RF, baseband and MAC circuitry. The recommended wake count period is 2 ms to allow the 20 MHz main oscillator to stabilize. Table 3-20 gives the recommended values for WAKECNT depending on the SLPCLK frequency.

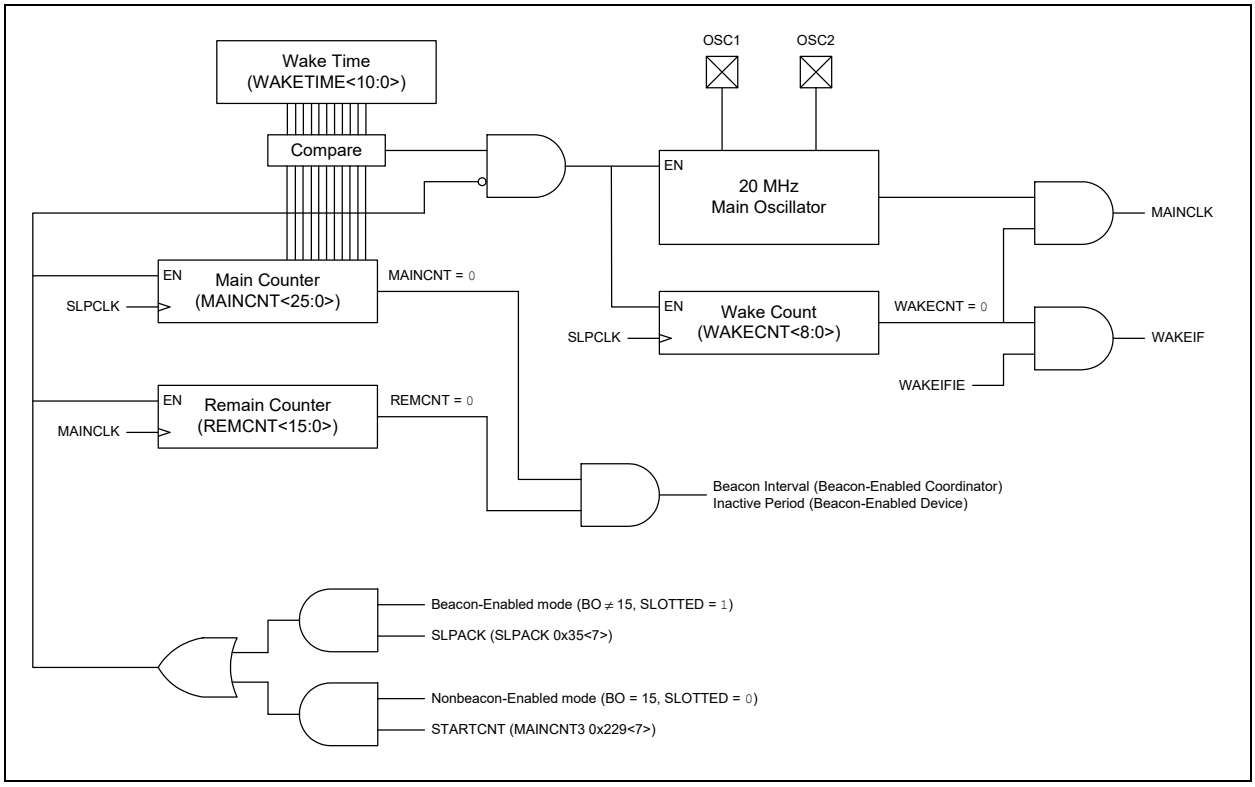
TABLE 3-19: MAIN AND REMAIN COUNTER TIMED EVENTS

Mode	Timed Event
Beacon-Enabled Coordinator	Beacon Interval (BI)
Beacon-Enabled Device	Inactive Period
Nonbeacon-Enabled Coordinator or Device	Sleep Interval

TABLE 3-20: WAKE TIME AND WAKE COUNT RECOMMENDED VALUES

SLPCLK Source	SLPCLKDIV	WAKETIME (2.1 ms)	WAKECNT (2 ms)
100 kHz	0x01	0x0D2	0x0C8
32 kHz	0x00	0x045	0x042

FIGURE 3-16: SLEEP MODE COUNTERS



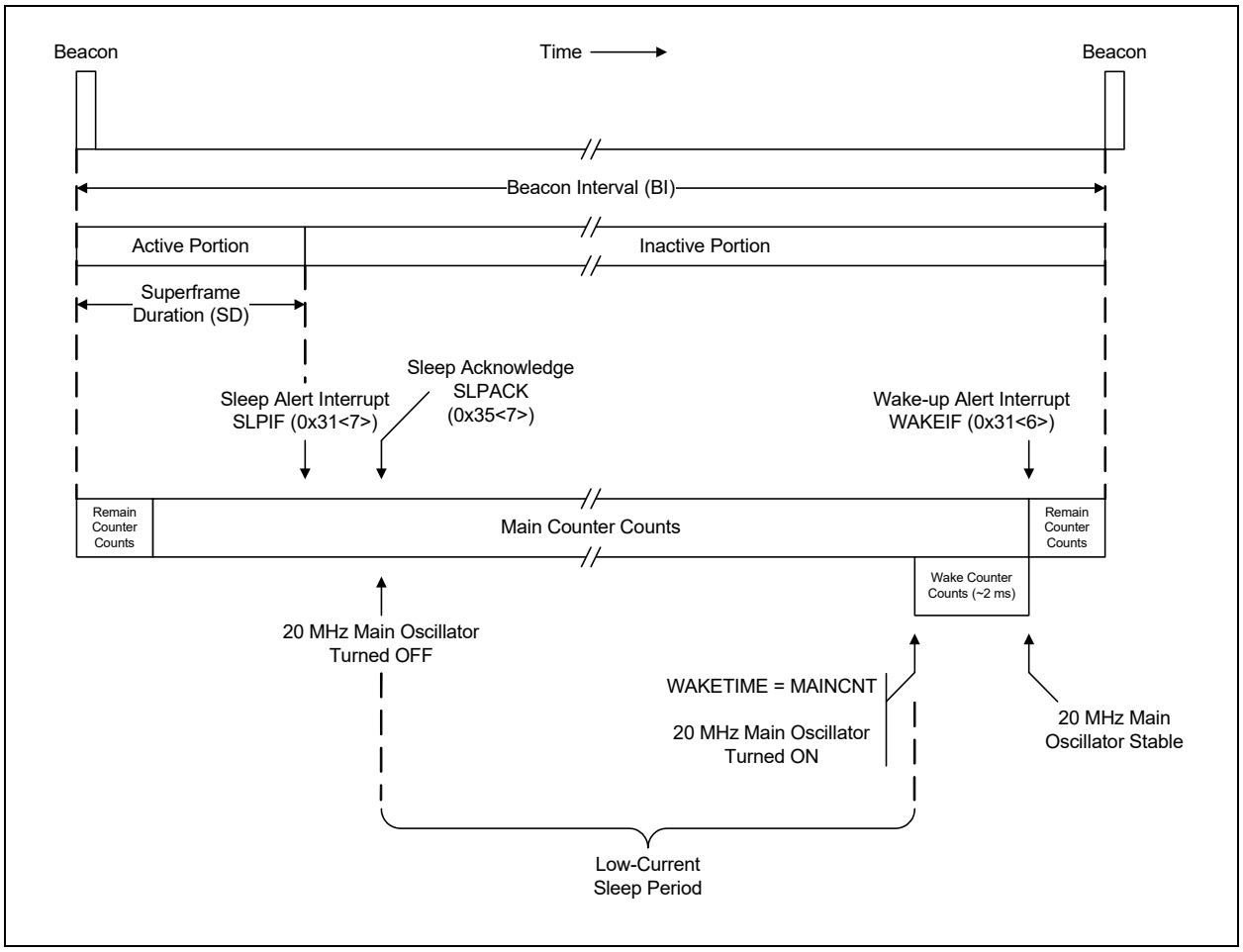
Beacon-Enabled Coordinator mode – Figure 3-17 shows the Sleep time line for Beacon-Enabled Coordinator mode. In this mode, the sum of the main and remain counters is the Beacon Interval (BI) of the superframe. The MRF24J40 will transmit a beacon packet as per Beacon Interval shown in Equation 3-3.

EQUATION 3-3:

Beacon Interval = (MAINCNT * SLPCLK Period) + (REMCNT * 50 ns)

The MRF24J40 alerts the host processor on the boundary of the active and inactive portion via a Sleep Alert Interrupt (SLPIF 0x31[7]). The host microcontroller Acknowledges the interrupt (SLPACK 0x35[7]), at which time, the MRF24J40 turns off the 20 MHz main oscillator. As the main counter counts, when WAKETIME = MAINCNT, the 20 MHz main oscillator is turned on. The wake counter counts as the 20 MHz main oscillator stabilizes and MAINCLK is disabled. The MRF24J40 alerts the host processor with a wake-up alert interrupt (0x31[6]).

FIGURE 3-17: BEACON-ENABLED COORDINATOR SLEEP TIME LINE



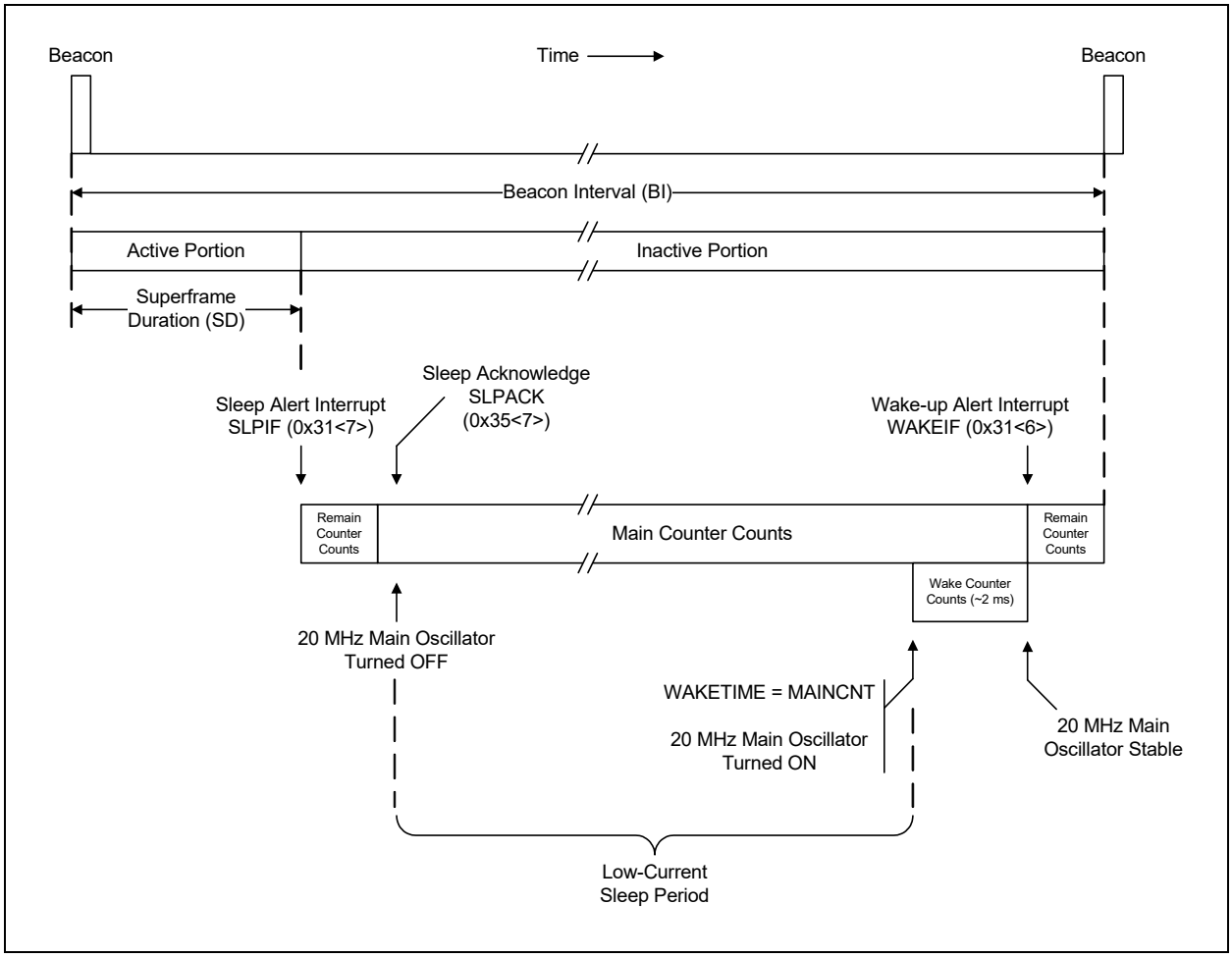
Beacon-Enabled Device mode – Figure 3-18 shows the Sleep time line for Beacon-Enabled Device mode. In this mode, the sum of the main and remain counters is the inactive period of the superframe. The MRF24J40 will time the inactive period as shown in Equation 3-4.

EQUATION 3-4:

Inactive Period = (MAINCNT * SLPCLK Period) + (REMCNT * 50 ns)

The MRF24J40 alerts the host processor on the boundary of the active and inactive portion via a Sleep Alert Interrupt (SLPIF 0x31[7]). The host microcontroller Acknowledges the interrupt (SLPACK 0x35[7]), at which time, the MRF24J40 turns off the 20 MHz main oscillator. As the main counter counts, when WAKETIME = MAINCNT, the 20 MHz main oscillator is turned on. The wake counter counts as the 20 MHz main oscillator stabilizes. The MRF24J40 alerts the host processor with a wake-up alert interrupt (0x31[6]).

FIGURE 3-18: BEACON-ENABLED DEVICE SLEEP TIME LINE

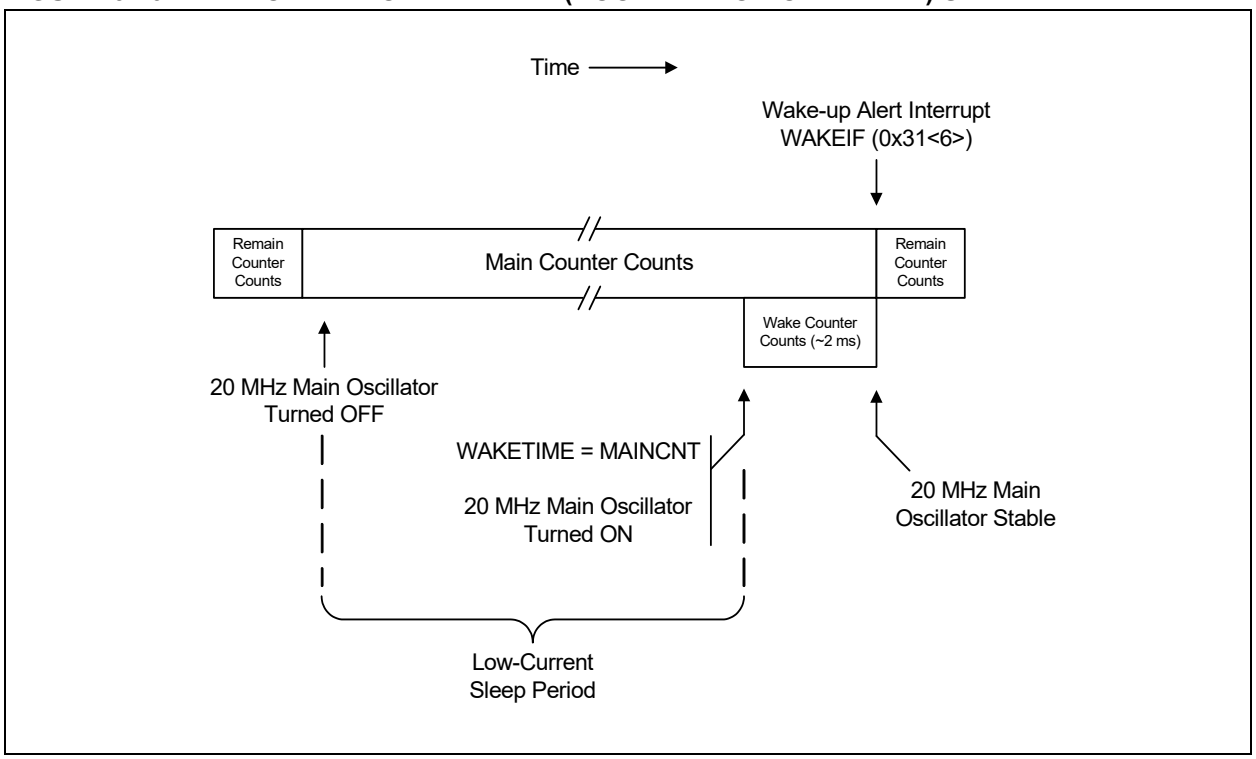


Nonbeacon-Enabled (Coordinator or Device) mode – Figure 3-19 shows the Sleep time line for Non-beacon-Enabled (Coordinator or Device) mode. In this mode, the host processor puts the MRF24J40 to Sleep by setting the STARTCNT (0x229[7]) bit. At the end of the Sleep interval, the MRF24J40 alerts the host processor with a wake-up alert interrupt (0x31[6]).

EQUATION 3-5:

Sleep Interval = (MAINCNT * SLPCLK Period) – WAKETIME + [(REMCNT * 50 ns)/2]

FIGURE 3-19: NONBEACON-ENABLED (COORDINATOR OR DEVICE) SLEEP TIME LINE



3.15.2 IMMEDIATE SLEEP AND WAKE-UP MODE

In the Immediate Sleep and Wake-up mode, the host microcontroller places the MRF24J40 to Sleep and wakes it up.

To enable the Immediate Wake-up mode, set the IMMWAKE (0x22[7]) bit to '1'.

To place the MRF24J40 to Sleep immediately, perform the following two steps:

1. Perform a Power Management Reset by setting the RSTPWR (0x2A[2]) bit to '1'. The bit will be automatically cleared to '0' by hardware.
2. Put the MRF24J40 to Sleep immediately by setting the SLPACK (0x35[7]) bit to '1'. The bit will be automatically cleared to '0' by hardware.

Wake-up can be performed in one of two methods:

1. Wake-up on WAKE pin 15. To enable the WAKE pin, set the WAKEPAD (0x0D[5]) bit to '1' and set the WAKE pin polarity. Set the WAKEPOL (0x0D[7]) bit to '1' for active-high signal, or clear to '0' for active-low signal.

or

2. Wake-up on register. To wake up the MRF24J40 from Sleep via the SPI port, set the REGWAKE (0x22[6]) bit to '1' and then clear to '0'.

After wake-up, delay at least 2 ms to allow 20 MHz main oscillator time to stabilize before transmitting or receiving.

Example 3-3 summarizes the steps to prepare the MRF24J40 for wake-up on WAKE pin and placing to Sleep.

EXAMPLE 3-3: IMMEDIATE SLEEP AND WAKE

The steps to prepare the MRF24J40 for immediate sleep and wake up on WAKE pin

Prepare WAKE pin:

1. WAKE pin = low
2. RXFLUSH (0x0D) = 0x60 – Enable WAKE pin and set polarity to active-high
3. WAKECON (0x22) = 0x80 – Enable Immediate Wake-up mode

Put to Sleep:

4. SOFTRST (0x2A) = 0x04 – Perform a Power Management Reset
5. SLPACK (0x35) = 0x80 – Put MRF24J40 to Sleep immediately

To Wake:

6. WAKE pin = high – Wake-up
7. RFCTL (0x36) = 0x04 - RF State Machine reset
8. RFCTL (0x36) = 0x00
9. Delay 2 ms to allow 20 MHz main oscillator time to stabilize before transmitting or receiving.

TABLE 3-21: REGISTERS ASSOCIATED WITH SLEEP

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0D	RXFLUSH	r	WAKEPLOL	WAKEPAD	r	CMDONLY	DATAONLY	BCNONLY	RXFLUSH
0x22	WAKECON	IMMWAKE	REGWAKE	INTL	INTL	INTL	INTL	INTL	INTL
0x2A	SOFTRST	r	r	r	r	r	RSTPWR	RSTBB	RSTMAC
0x31	INSTAT	SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF
0x32	INTCON	SLPIE	WAKEIE	HSYMTMRIE	SECIE	RXIE	TXG2IE	TXG1IE	TXNIE
0x35	SLPACK	SLPACK	WAKECNT6	WAKECNT5	WAKECNT4	WAKECNT3	WAKECNT2	WAKECNT1	WAKECNT0
0x36	RFCTL	r	r	r	WAKECNT8	WAKECNT7	RFRST	RFTXMODE	RFRXMODE
0x207	RFCON7	SLPCLKSEL1	SLPCLKSEL0	r	r	r	r	r	r
0x20B	SLPCAL2	SLPCALRDY	r	r	SLPCALEN	SLPCAL19	SLPCAL18	SLPCAL17	SLPCAL16
0x211	SLPCON0	r	r	r	r	r	r	INTEDGE	SLPCLKEN
0x220	SLPCON1	r	r	CLKOUTEN	SLPCLKDIV4	SLPCLKDIV3	SLPCLKDIV2	SLPCLKDIV1	SLPCLKDIV0
0x223	WAKETIMEH	r	r	r	r	r	WAKETIME10	WAKETIME9	WAKETIME8
0x224	REMCNTL	REMCNT7	REMCNT6	REMCNT5	REMCNT4	REMCNT3	REMCNT2	REMCNT1	REMCNT0
0x225	REMCNTH	REMCNT15	REMCNT14	REMCNT13	REMCNT12	REMCNT11	REMCNT10	REMCNT9	REMCNT8
0x226	MAINCNT0	MAINCNT7	MAINCNT6	MAINCNT5	MAINCNT4	MAINCNT3	MAINCNT2	MAINCNT1	MAINCNT0
0x227	MAINCNT1	MAINCNT15	MAINCNT14	MAINCNT13	MAINCNT12	MAINCNT11	MAINCNT10	MAINCNT9	MAINCNT8
0x228	MAINCNT2	MAINCNT23	MAINCNT22	MAINCNT21	MAINCNT20	MAINCNT19	MAINCNT18	MAINCNT17	MAINCNT16
0x229	MAINCNT3	STARTCNT	r	r	r	r	r	MAINCNT25	MAINCNT24

3.16 MAC Timer

Many features of the IEEE 802.15.4-2003 Standard are based on a symbol period of 16 μs. A 16-bit MAC timer is provided to generate interrupts configurable in multiples of 8 μs. The MAC timer begins counting down when a value is written to the HSYMTMRH (0x29) register. A HSYMTMRIF (0x31[5]) interrupt is generated when the count reaches zero.

TABLE 3-22: REGISTERS ASSOCIATED WITH THE MAC TIMER

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x28	HSYMTMRL	HSYMTMR7	HSYMTMR6	HSYMTMR5	HSYMTMR4	HSYMTMR3	HSYMTMR2	HSYMTMR1	HSYMTMR0
0x29	HSYMTMRH	HSYMTMR15	HSYMTMR14	HSYMTMR13	HSYMTMR12	HSYMTMR11	HSYMTMR10	HSYMTMR9	HSYMTMR8
0x31	INSTAT	SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF
0x32	INTCON	SLPIE	WAKEIE	HSYMTMRIE	SECIE	RXIE	TXG2IE	TXG1IE	TXNIE

3.17 Security

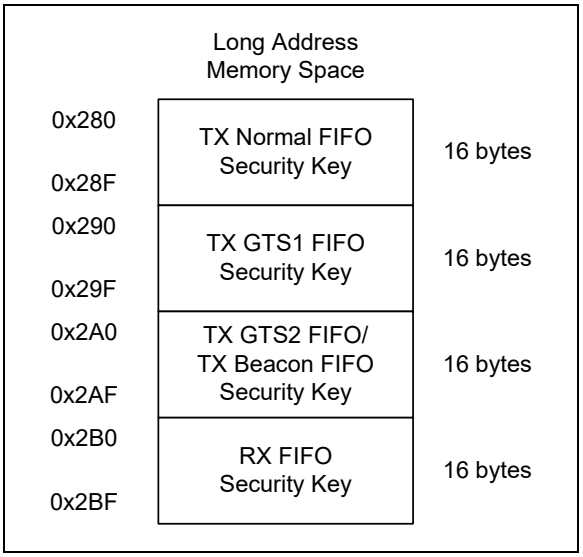
The MRF24J40 provides a hardware security engine that implements the Advanced Encryption Standard, 128-bit (AES-128) according to the IEEE 802.15.4-2003 Standard. The MRF24J40 supports seven security suites which provide a group of security operations designed to provide security services on MAC and upper layer frames.

- AES-CTR
- AES-CCM-128
- AES-CCM-64
- AES-CCM-32
- AES-CRC-MAC-128
- AES-CRC-MAC-64
- AES-CRC-MAC-32

Security keys are stored in the Security Key FIFO. Four security keys, three for encryption and one for decryption, are stored in the memory locations shown in Figure 3-20.

The security engine can be used for the encryption and decryption of MAC sublayer frames for transmission and reception of secured frames and provide security encryption and decryption services to the upper layers. These functions are described in the following subsections.

FIGURE 3-20: MEMORY MAP OF SECURITY KEY FIFO



Note: The TX GTS2 FIFO and TX Beacon FIFO share the same security key memory location.

3.17.1 MAC SUBLAYER TRANSMIT ENCRYPTION

A frame can be encrypted and transmitted from each of the TX FIFOs. Table 3-23 lists the TX FIFO and associated security key memory address and control register bits.

TABLE 3-23: ENCRYPTION SECURITY KEY AND CONTROL REGISTER BITS

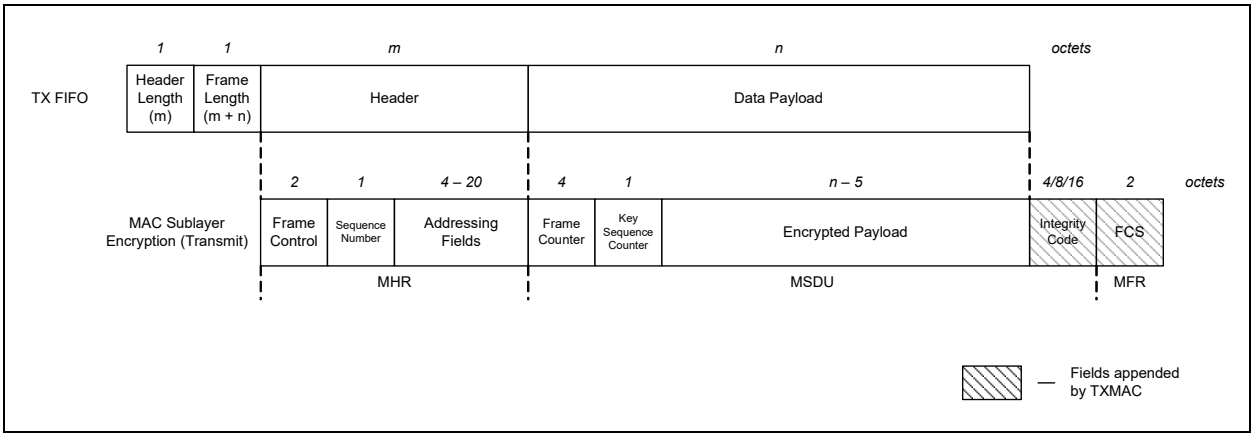
TX FIFO	Security Key Memory Address	Security Suite Select Bits	Security Enable Bits	Trigger Bit
TX Normal FIFO	0x280-0x28F	TXNCIPHER (SECCON0 0x2C[2:0])	TXNSECEN (TXNCON 0x1B[1])	TXNTRIG (TXNCON 0x1B[0])
TX GTS1 FIFO	0x290-0x29F	TXG1CIPHER (SECCR2 0x37[2:0])	TXG1SECEN (TXG1CON 0x1C[1])	TXG1TRIG (TXG1CON 0x1C[0])
TX GTS2 FIFO	0x2A0-0x2AF	TXG2CIPHER (SECCR2 0x37[5:3])	TXG2SECEN (TXG2CON 0x1D[1])	TXG2TRIG (TXG2CON 0x1D[0])
TX Beacon FIFO	0x2A0-0x2AF	TXBCIPHER (SECCON1 0x2D[6:4])	TXBCNSECEN (TXBCON 0x1A[1])	TXBCNTRIG (TXBCON 0x1A[0])

Note: The TX GTS2 FIFO and TX Beacon FIFO share the same security key memory location.

To transmit a secured frame, perform the following steps:

1. The host processor loads one of the four TX FIFOs with an IEEE 802.15.4 compliant frame to be encrypted using the format shown in Figure 3-21.

FIGURE 3-21: SECURITY TX FIFO FORMAT



2. Program the corresponding TX FIFO 128-bit security key into the Security Key FIFO memory address, as shown in Table 3-23.
3. Select the security suite for the corresponding TX FIFO and program the security select bits as shown in Table 3-23. The security suite selection values are shown in Table 3-24.

TABLE 3-24: SECURITY SUITE SELECTION VALUE

Mode	Security Suite Select Bits (see Table 3-23)
None	000
AES-CTR	001
AES-CCM-128	010
AES-CCM-64	011
AES-CCM-32	100
AES-CBC-MAC-128	101
AES-CBC-MAC-64	110
AES-CBC-MAC-32	111

4. Encrypt and transmit the packet by setting the Security Enable (TXxSECEN) = 1 and Trigger (TXxTRIG) bits = 1 for the respective TX FIFO, as shown in Table 3-23.
5. Depending on which TX FIFO the secure packet was transmit from, the status of the transmission is read as,

TX Normal FIFO – A TXNIF (INTSTAT 0x31[0]) interrupt will be issued. The TXNSTAT (TXSTAT 0x24[0]) bit indicates the status of the transmission:

TXNSTAT = 0: Transmission was successful

TXNSTAT = 1: Transmission failed, retry count exceeded

The number of retries of the most recent transmission is contained in the TXNRETRY (TXSTAT 0x24[7:6]) bits. The CCAFAIL (TXSTAT 0x24[5]) bit = 1 indicates if the failed transmission was due to the channel busy (CSMA-CA timed out).

TX GTSx FIFO – A TXG1IF (INTSTAT 0x31[1]) or TXG2IF (INTSTAT 0x31[2]) interrupt will be issued. The TXG1STAT (TXSTAT 0x24[1]) or TXG2STAT (TXSTAT 0x24[2]) bit indicates the status of the transmission:

TXGxSTAT = 1: Transmission was successful

TXGxSTAT = 0: Transmission failed, retry count exceeded

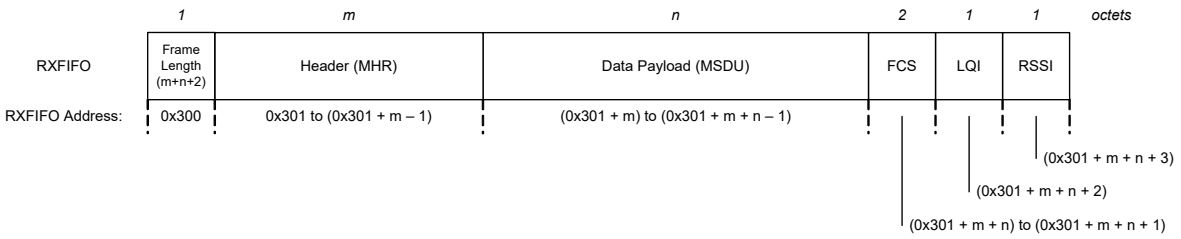
The number of retries of the most recent transmission is contained in the TXG1RETRY (TXG1CON 0x1C[7:6]) or TXG2RETRY (TXG2CON 0x1D[7:6]) bits. The CCAFAIL (TXSTAT 0x24[5]) bit = 1 indicates if the failed transmission was due to the channel busy (CSMA-CA timed out). The TXG1FNT (TXSTAT 0x24[3]) or TXG2FNT (TXSTAT 0x24[4]) bit = 1 indicates if TX GTSx FIFO transmission failed due to not enough time to transmit in the guaranteed time slot.

3.17.2 MAC SUBLAYER RECEIVE DECRYPTION

To receive and decrypt a secured frame from the RXFIFO, perform the following steps:

1. When a packet is received and the security enable bit = 1 in the frame control field, the MRF24J40 issues a Security Interrupt, SECIF (INTSTAT 0x31[4]). The Security Interrupt indicates to the host microcontroller that the received frame was secured. The host microcontroller can choose to decrypt or ignore the frame. The format of the received frame is shown in Example 3-22.

FIGURE 3-22: SECURITY RX FIFO FORMAT



2. If the decryption should be ignored, set the SECIGNORE (SECCON0 0x2C[7]) bit = 1. The encrypted packet can be discarded or read from the RXFIFO and processed in the upper layers.
3. The host microcontroller loads the security key into the RX FIFO Security Key memory location as shown in Table 3-25.

TABLE 3-25: DECRYPTION SECURITY KEY AND CONTROL REGISTER BITS

FIFO	Security Key Memory Address
RX FIFO	0x2B0-0x2BF

4. Select the security suite and program the RXCIPHER (SECCON0 0x2C[5:3]) bits. The security suite selection values are shown in Table 3-24.
5. Start the decryption by setting the SECSTART (SECCON0 0x2C[6]) bit = 1.
6. When the decryption process is complete, a Receive Interrupt (RXIF 0x31[3]) is issued.
7. Check the decryption status by reading SECDECERR (RXSR 0x30[2])
   SECDECERR = 0: No Decryption Error
   SECDECERR = 1: Decryption Error

Note: If decryption error has occurred and the packet in the FIFO needs to be discarded, then set RXFLUSH (RXFLUSH 0x0D[0]) bit = 1.

3.17.3 UPPER LAYER ENCRYPTION

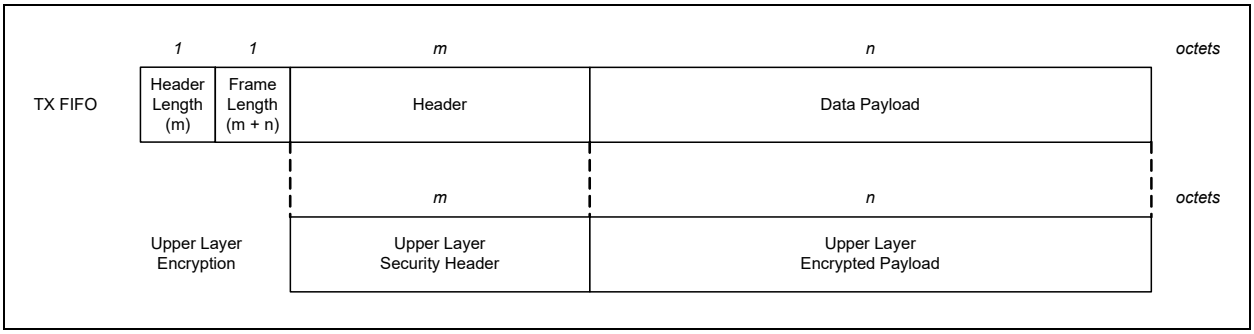
To encrypt an upper layer frame, perform the following steps:

1. The host microcontroller loads the TXNFIFO with the upper layer frame for encryption into the TXNFIFO using the format shown in Figure 3-23. The header length field indicates the number of octets (bytes) that is not encrypted.

Note: The header length field, as implemented in the MRF24J40, is 5 bits long. Therefore, the header length maximum value is 31 octets (bytes). This conforms to the IEEE 802.15.4-2003 Specification. However, it does not conform to the IEEE 802.15.4-2006 Standard. The work around is to:

- Use a header length no longer than 31 octets (bytes)
- Implement a security algorithm in the upper layers

FIGURE 3-23: UPPER LAYER ENCRYPTION AND DECRYPTION FORMAT



2. The host microcontroller loads the 13-byte NONCE value into the UPNONCE12 through UPNONCE0 (0x240 through 0x24C) registers.
3. Program the 128-bit security key into the TX Normal FIFO Security Key FIFO memory address, 0x280 through 0x28F.
4. Select the security suite and program the TXNCIPHER (SECCON0 0x2C[2:0]) bits. The security suite selection values are shown in Table 3-24.
5. Enable Upper Layer Security Encryption mode by setting the UPENC (SECCR2 0x37[6]) bit = 1.
6. Encrypt the frame by setting the TXNTRIG (TXNCON 0x1B[0]) bit and TXNSECEN (TXNCON 0x1B[1]) to 1.
7. A TXNIF (INTSTAT 0x31[0]) interrupt will be issued. The TXNSTAT (TXSTAT 0x24[0]) bit = 0 indicates the encryption has completed.
8. The encrypted frame is available in the TXNFIFO and can be read by the host microcontroller.

   Application Hint: The encryption can be checked by decrypting the frame data (refer **Section 3.17.4 "Upper Layer Decryption"**) and comparing it to the original frame data.

3.17.4 UPPER LAYER DECRYPTION

To decrypt an upper layer frame, perform the following steps:

1. The host microcontroller loads the TXNFIFO with the upper layer frame for decryption into the TXNFIFO using the format shown in Figure 3-23. The header length field indicates the number of octets (bytes) that are not encrypted.
2. The host microcontroller loads the 13-byte NONCE value into the UPNONCE12 through UPNONCE0 (0x240 through 0x24C) registers.

Note: The header length field, as implemented in the MRF24J40, is 5-bits long. Therefore, the header length maximum value is 31 octets (bytes). This conforms to the IEEE 802.15.4-2003 Specification. However, it does not conform to the IEEE 802.15.4-2006 Standard. The work around is to:

- Use a header length no longer than 31 octets (bytes)
- Implement a security algorithm in the upper layers

3. Program the 128-bit security key into the TX Normal FIFO Security Key FIFO memory address, 0x280 through 0x28F.
4. Select the security suite and program the TXNCIPHER (SECCON0 0x2C[2:0]) bits. The security suite selection values are shown in Table 3-24.
5. Enable Upper Layer Security Decryption mode by setting the UPDEC (SECCR2 0x37[7]) bit = 1.
6. Start Decrypting the frame by setting the TXNTRIG (TXNCON 0x1B[0]) bit to 1.
7. A TXNIF (INTSTAT 0x31[0]) interrupt will be issued. The TXNSTAT (TXSTAT 0x24[0]) bit = 0 indicates that the decryption process has completed.
8. Check if a MIC error occurred by reading the UPSECERR (0x30[6]) bit:

   UPSECERR = 0: No MIC error

   UPSECERR = 1: MIC error occurred; write '1' to clear error
9. The decrypted frame is available in the TXNFIFO and can be read by the host microcontroller.

TABLE 3-26: REGISTERS ASSOCIATED WITH SECURITY

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1A	TXBCON0	r	r	r	r	r	r	TXBSECEN	TXBTRIG
0x1B	TXNCON	r	r	r	FPSTAT	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG
0x1C	TXG1CON	TXG1RETRY1	TXG1RETRY0	TXG1SLOT2	TXG1SLOT1	TXG1SLOT0	TXG1ACKREQ	TXG1SECEN	TXG1TRIG
0x1D	TXG2CON	TXG2RETRY1	TXG2RETRY0	TXG2SLOT2	TXG2SLOT1	TXG2SLOT0	TXG2ACKREQ	TXG2SECEN	TXG2TRIG
0x24	TXSTAT	TXNRETRY1	TXNRETRY0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2STAT	TXG1STAT	TXNSTAT
0x2C	SECCON0	SECIGNORE	SECSTART	RXCIPHER2	RXCIPHER1	RXCIPHER0	TXNCIPHER2	TXNCIPHER1	TXNCIPHER0
0x2D	SECCON1	r	TXBCIPHER2	TXBCIPHER1	TXBCIPHER0	r	r	DISDEC	DISENC
0x30	RXSR	r	UPSECERR	BATIND	r	r	SECDECERR	r	r
0x31	INTSTAT	SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF
0x32	INTCON	SLPIE	WAKEIE	HSYMTMRIE	SECIE	RXIE	TXG2IE	TXG1IE	TXNIE
0x37	SECCR2	UPDEC	UPENC	TXG2CIPHER2	TXG2CIPHER1	TXG2CIPHER0	TXG1CIPHER2	TXG1CIPHER1	TXG1CIPHER0
0x240	UPNONCE0	UPNONCE[7:0]							
0x241	UPNONCE1	UPNONCE[15:8]							
0x242	UPNONCE2	UPNONCE[23:16]							
0x243	UPNONCE3	UPNONCE[31:24]							
0x244	UPNONCE4	UPNONCE[39:32]							
0x245	UPNONCE5	UPNONCE[47:40]							
0x246	UPNONCE6	UPNONCE[55:48]							
0x247	UPNONCE7	UPNONCE[63:56]							
0x248	UPNONCE8	UPNONCE[71:64]							
0x249	UPNONCE9	UPNONCE[79:72]							
0x24A	UPNONCE10	UPNONCE[87:80]							
0x24B	UPNONCE11	UPNONCE[95:88]							
0x24C	UPNONCE12	UPNONCE[103:96]							

3.18 Turbo Mode

The MRF24J40 provides a Turbo mode to transmit and receive at 625 kbps (2.5 times 250 kbps). This mode enables higher data rates for proprietary protocols.

To configure the MRF24J40 for Turbo mode, perform the following steps:

1. Enable Turbo mode by setting the TURBO (BBREG0 0x38[0]) bit = 1.
2. Set the baseband parameter, PREVALIDTH (BBREG3 0x3B[7:4]) bits = 0011.
3. Set baseband parameter, CSTH (BBREG4 0x3C[7:5]) bits = 010.
4. Perform a baseband circuitry Reset, RSTBB (SOFTRST 0x2A[1]) = 1.

TABLE 3-27: REGISTERS ASSOCIATED WITH TURBO MODE

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2A	SOFTRST	r	r	r	r	r	RSTPWR	RSTBB	RSTMAC
0x38	BBREG0	r	r	r	r	r	r	r	TURBO
0x3B	BBREG3	PREVALIDTH3	PREVALIDTH2	PREVALIDTH1	PREVALIDTH0	PREDETTH2	PREDETTH1	PREDETTH0	r
0x3C	BBREG4	CSTH2	CSTH1	CSTH0	PRECNT2	PRECNT1	PRECNT0	r	r

NOTES:

4.0 APPLICATIONS

4.1 Antenna/Balun

Figure 4-1 is an example of the circuit diagram of a balun to match to a 50Ω antenna. A balun is the impedance transformer from unbalanced input of the PCB antenna and the balanced input of the RF transceiver (pins RFP and RFN).

Figure 4-2 shows the measured impedance of the balun where the center of the band is very close to 50Ω. When using low tolerance components (i.e., ±5%) along with an appropriate ground, the impedance will remain close to the 50Ω measurement.

FIGURE 4-1: EXAMPLE BALUN CIRCUIT DIAGRAM

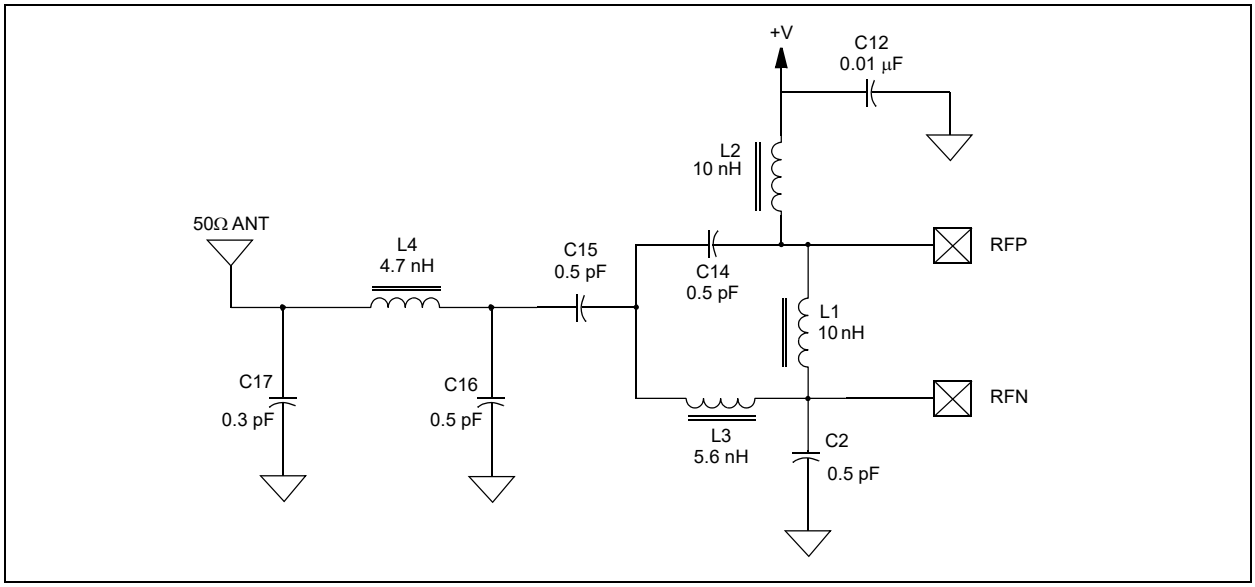
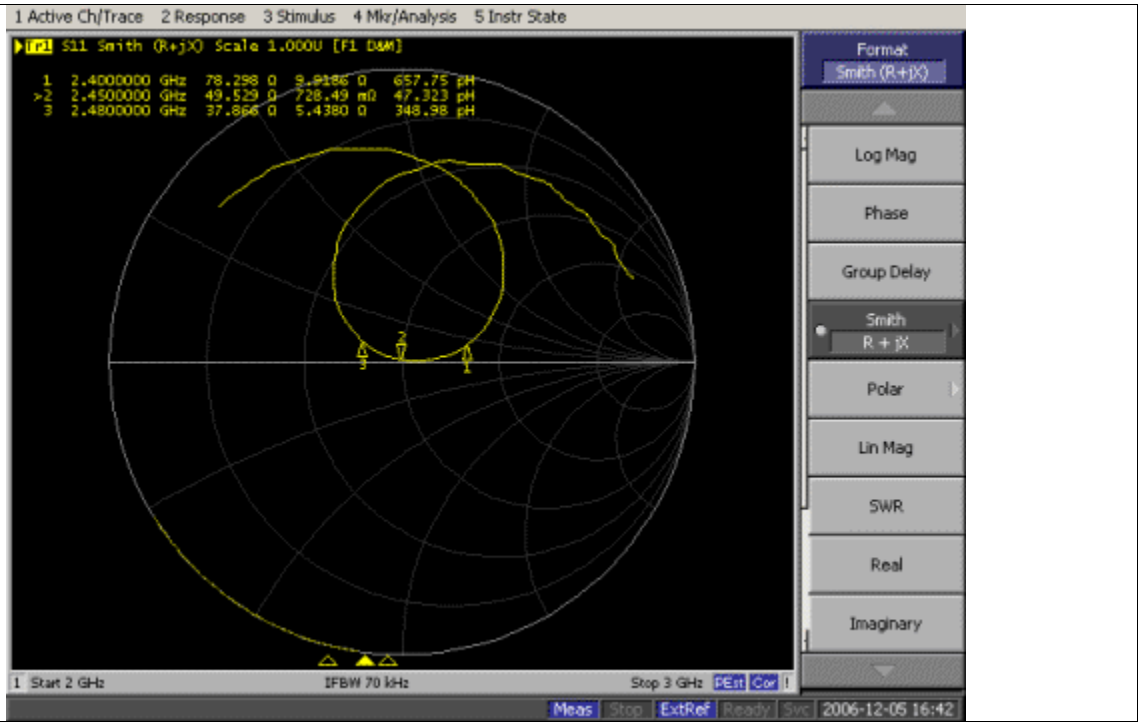


FIGURE 4-2: BALUN CIRCUIT MEASURED IMPEDANCE



4.2 External PA/LNA Control

External PA, LNA and RF switches can be controlled by the MRF24J40 internal RF state machine. Figure 4-3 shows a typical application circuit with external PA, LNA and RF switches. Setting TESTMODE (0x22F[2:0]) bits to '111' will configure pins, GPIO0, GPIO1 and GPIO2, to operate according to Table 4-1. The external PA/LNA timing diagram is shown in Figure 4-4.

TABLE 4-1: GPIO EXTERNAL PA/LNA SIGNALING

GPIO	Receive	Transmit	Maximum Current Source
GPIO0	Low	High	4 ma
GPIO1	Low	High	1 ma
GPIO2	High	Low	1 ma

FIGURE 4-3: EXTERNAL PA/LNA BLOCK DIAGRAM

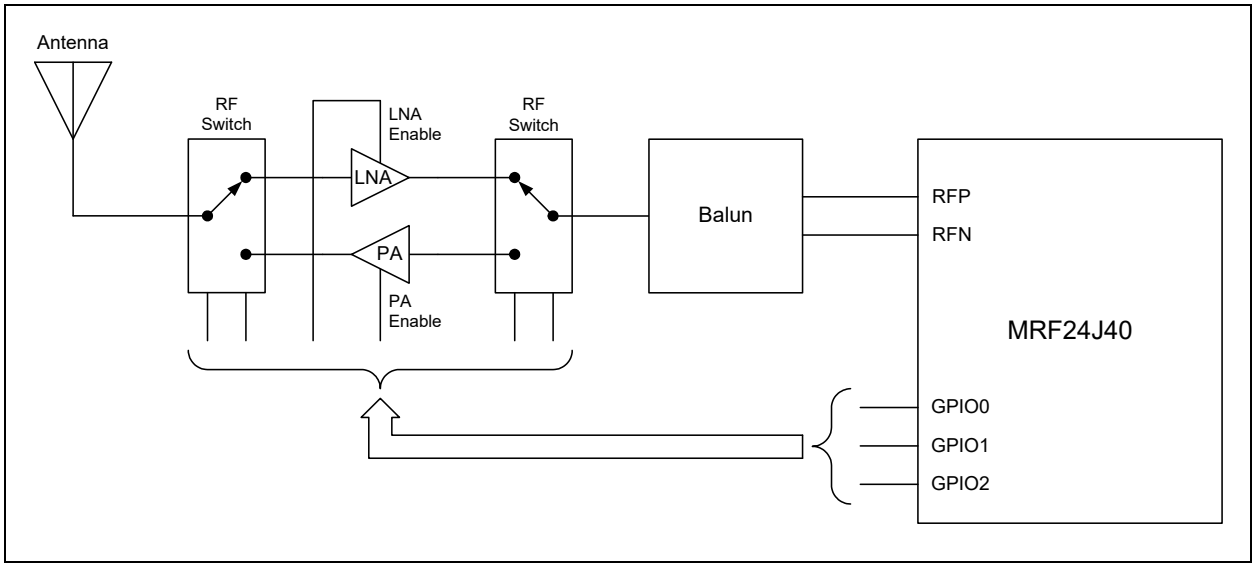
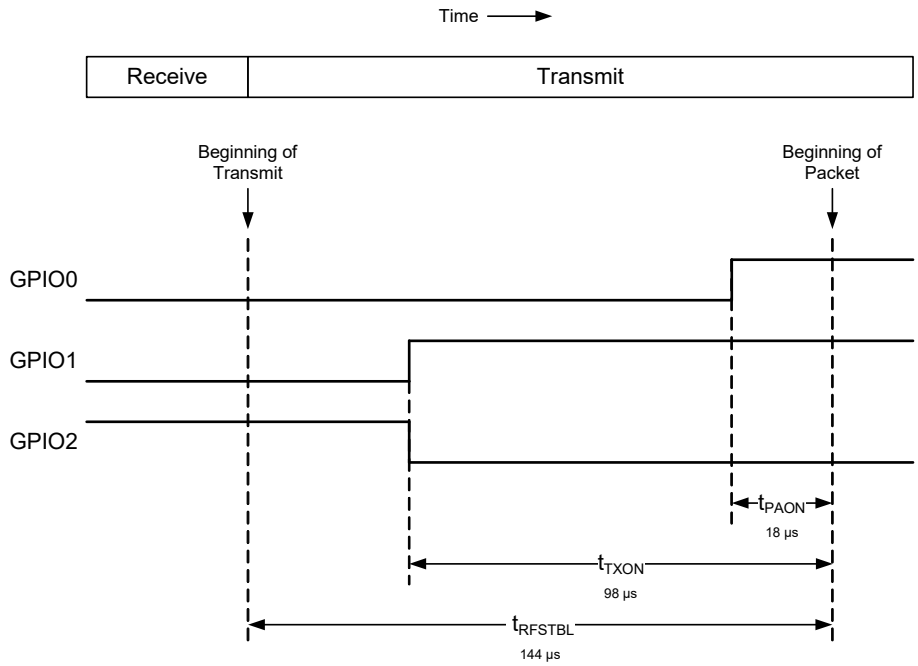


FIGURE 4-4: EXTERNAL PA/LNA TIMING DIAGRAM



RF Stabilization Time (t_{RFSTBL}) = RFSTBL * 16 µs

144 µs = 9 * 16 µs

Transmit On Time (t_{TXON}) = TXONTS * 16 µs + TXONT * 50 ns

98 µs = 6 * 16 µs + 40 * 50 ns

PA On Time (t_{PAON}) = PAONTS * 16 µs + PAONT + 50 ns

18.05 µs = 1 * 16 µs + 41 * 50 ns

Rule: $t_{rfstbl} > t_{txon} > t_{paon}$

TABLE 4-2: REGISTERS ASSOCIATED WITH EXTERNAL PA/LNA

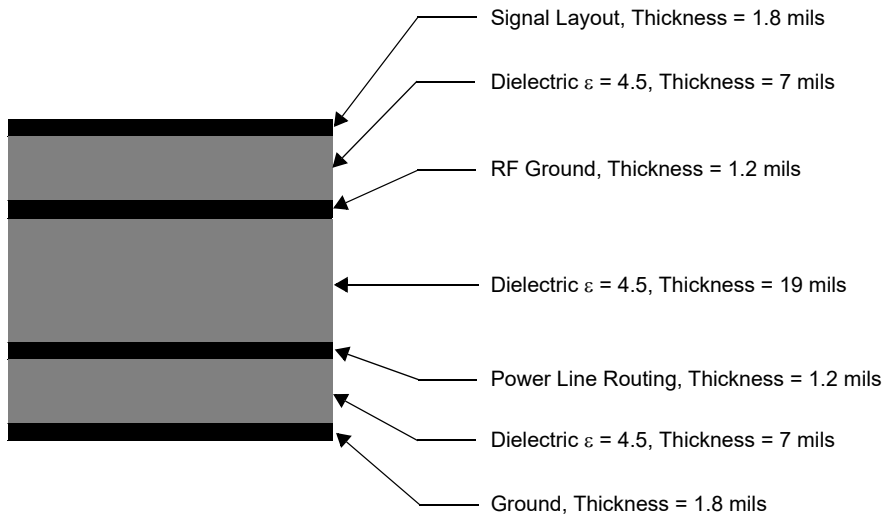
Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x15	SYMTICKH	TXONT6	TXONT5	TXONT4	TXONT3	TXONT2	TXONT1	TXONT0	TICKP8
0x16	PACON0	PAONT7	PAONT6	PAONT5	PAONT4	PAONT3	PAONT2	PAONT1	PAONT0
0x17	PACON1	r	r	r	PAONTS3	PAONTS2	PAONTS1	PAONTS0	PAONT8
0x18	PACON2	FIFOEN	r	TXONTS3	TXONTS2	TXONTS1	TXONTS0	TXONT8	TXONT7
0x2E	TXSTBL	RFSTBL3	RFSTBL2	RFSTBL1	RFSTBL0	MSIFS3	MSIFS2	MSIFS1	MSIFS0
0x22F	TESTMODE	r	r	r	RSSIWAIT1	RSSIWAIT0	TESTMODE2	TESTMODE1	TESTMODE0

4.3 PCB Layout Design

The following guidelines are intended to aid users in high-frequency PCB layout design.

The printed circuit board is comprised of four basic FR4 layers: signal layout, RF ground, power line routing and ground (see Figure 4-5). The guidelines will explain the requirements of these layers.

FIGURE 4-5: FOUR BASIC COPPER FR4 LAYERS



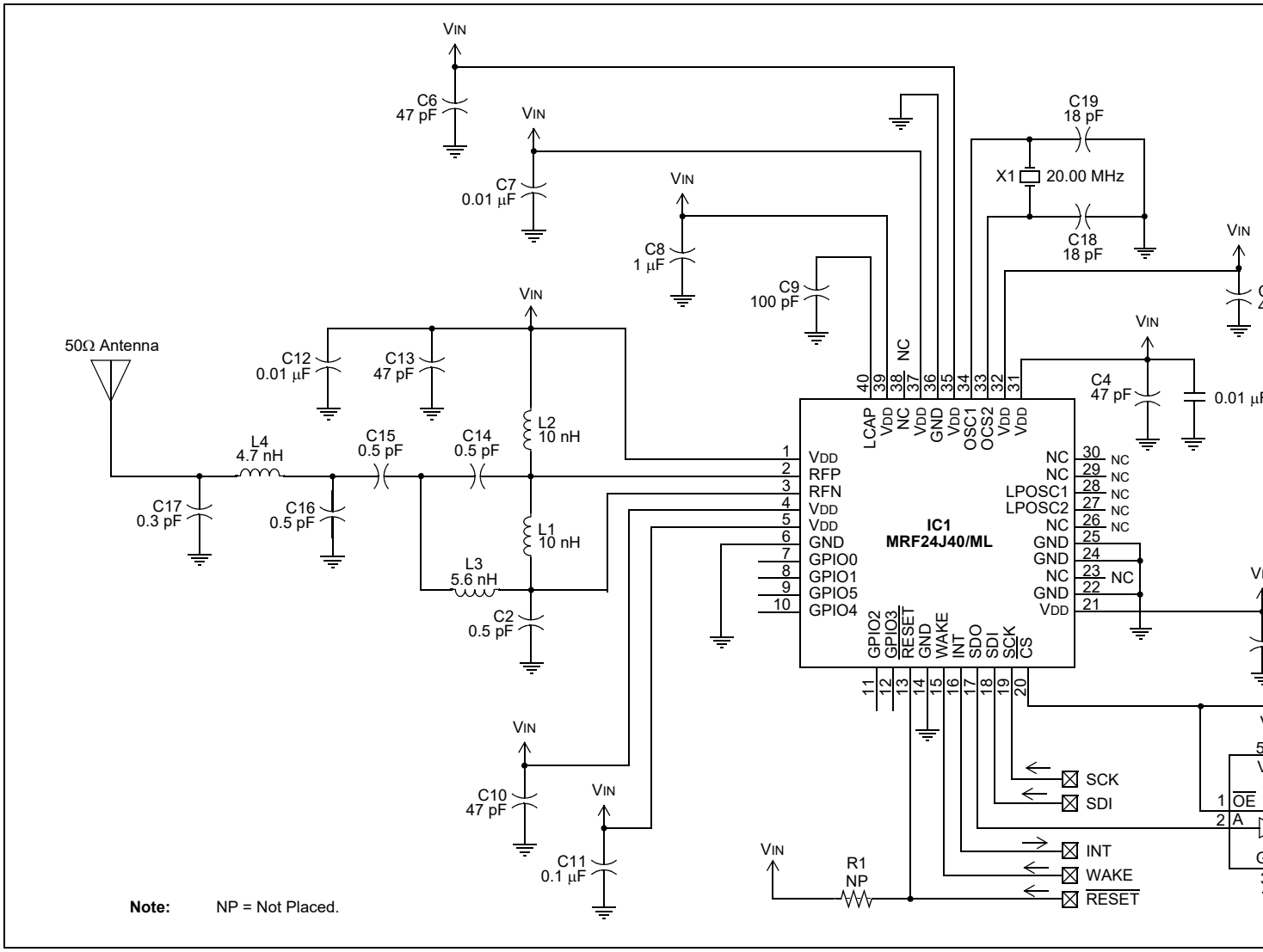
Note: Care should be taken with all ground lines to prevent breakage.

- It is important to keep the original PCB thickness since any change will affect antenna performance (see total thickness of dielectric) or microstrip lines characteristic impedance.
- The first layer width of a 50Ω characteristic impedance microstrip line is 12 mils.
- Avoid having microstrip lines longer than 2.5 cm, since that line might get very close to a quarter wave length of the working frequency of the board which is 3.0 cm, and start behaving as an antenna.
- Except for the antenna layout, avoid sharp corners since they can act as an antenna. Round corners will eliminate possible future EMI problems.
- Digital lines by definition are prone to be very noisy when handling periodic waveforms and fast clock/switching rates. Avoid laying out a RF signal close to any digital lines.
- A via filled ground patch underneath the IC transceiver is mandatory.
- A power supply must be distributed to each pin in a star topology and low-ESR capacitors must be placed at each pin for proper decoupling noise.
- Thorough decoupling on each power pin is beneficial for reducing in-band transceiver noise, particularly when this noise degrades performance. Usually, low value caps (27-47 pF) combined with large value caps (100 nF) will cover a large spectrum of frequency.
- Passive components (inductors) must be in the high-frequency category and the SRF (Self-Resonant Frequency) should be at least two times higher than the operating frequency.

4.4 MRF24J40 Schematic and Bill of Materials

4.4.1 SCHEMATIC

FIGURE 4-6: MRF24J40 SCHEMATIC



Note: NP = Not Placed.

4.4.2 BILL OF MATERIALS

TABLE 4-3: MRF24J40 BILL OF MATERIALS

Designator	Description
C2	Chip Capacitor 0402 COG 0.5P
C3	Chip Capacitor 0402 X7R 10N
C4	Chip Capacitor 0402 COG 47P
C5	Chip Capacitor 0402 COG 47P
C6	Chip Capacitor 0402 COG 47P
C7	Chip Capacitor 0402 X7R 10N
C8	Chip Capacitor 0402 X5R 1U
C9	Chip Capacitor 0402 COG 100P
C10	Chip Capacitor 0402 COG 47P
C11	Chip Capacitor 0402 X5R 100N
C12	Chip Capacitor 0402 X5R 100N
C13	Chip Capacitor 0402 COG 47P
C14	Chip Capacitor 0402 COG 0.5P
C15	Chip Capacitor 0402 COG 0.5P
C16	Chip Capacitor 0402 COG 0.5P
C17	Chip Capacitor 0402 COG 0.3P
C18	Chip Capacitor 0402 COG 18P
C19	Chip Capacitor 0402 COG 18P
IC1	MRF24J40-I/ML
IC2	Buffer, SC70 Package, NC7SZ125P5X
L1	Chip Inductor 0402 10N
L2	Chip Inductor 0402 10N
L3	Chip Inductor 0402 5.6N
L4	Chip Inductor 0402 4.7N
R1	Not Placed
X1	20 MHz Crystal, Abracon P/N ABM8 - 156 - 20.000MHz - T

5.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +85°C
Storage temperature ..... -65°C to +150°C
Voltage on any combined digital and analog pin with respect to VSS (except VDD) ..... -0.5V to (VDD + 0.5V)
Voltage on VDD with respect to VSS ..... -0.3V to 3.6V
Maximum output current sunk by GPIO1-GPIO5 pins ..... 1 mA
Maximum output current sourced by GPIO1-GPIO5 pins ..... 1 mA
Maximum output current sunk by GPIO0 pin ..... 4 mA
Maximum output current sourced by GPIO0 pin ..... 4 mA

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 5-1: RECOMMENDED OPERATING CONDITIONS

Parameters	Min	Typ	Max	Units
Ambient Operating Temperature	-40	—	+85	°C
Supply Voltage for RF, Analog and Digital Circuits	3.0	—	3.6	V
Supply Voltage for Digital I/O	3.0	3.3	3.6	V
Input High Voltage (V_{IH})	0.5 x V_{DD}	—	V_{DD} + 0.3	V
Input Low Voltage (V_{IL})	-0.3	—	0.2 x V_{DD}	V

TABLE 5-2: CURRENT CONSUMPTION

Typical Values: T_A = 25°C, V_{DD} = 3.3V

Chip Mode	Condition	Min	Typ	Max	Units
Sleep	Sleep Clock Disabled	—	2	—	μA
TX	At maximum output power	—	23	—	mA
RX	—	—	19	—	mA

TABLE 5-3: RECEIVER AC CHARACTERISTICS

Typical Values: T_A = 25°C, V_{DD} = 3.3V, LO Frequency = 2.445 GHz

Parameters	Condition	Min	Typ	Max	Units
RF Input Frequency	—	2.405	—	2.480	GHz
RF Sensitivity	At antenna input with O-QPSK signal and 3.5 dB front end loss is assumed	—	-95	—	dBm
Maximum RF Input	LNA at high gain	+5	—	—	dBm
LO Leakage	Measured at balun matching network input at frequency 2.405-2.48 GHz	—	-60	—	dBm
Noise Figure (including matching)		—	8	—	dB
Adjacent Channel Rejection	@ +/- 5 MHz	30	—	—	dB
Alternate Channel Rejection	@ +/- 10 MHz	40	—	—	dB
RSSI Range	—	—	50	—	dB
RSSI Error	—	-5	—	5	dB

TABLE 5-4: TRANSMITTER AC CHARACTERISTICS

Typical Values: T_A = 25°C, V_{DD} = 3.3V, LO Frequency = 2.445 GHz

Parameters	Condition	Min	Typ	Max	Units
RF Carrier Frequency	—	2.405	—	2.480	GHz
Maximum RF Output Power	—	—	0	—	dBm
RF Output Power Control Range	—	—	36	—	dB
TX Gain Control Resolution	Programmed by register	—	1.25	—	dB
Carrier Suppression	—	—	-30	—	dBc
TX Spectrum Mask for O-QPSK Signal	Offset frequency > 3.5 MHz, at 0 dBm output power	-33	—	—	dBm
TX EVM	—	—	13	—	%

FIGURE 5-1: EXAMPLE SPI SLAVE MODE TIMING

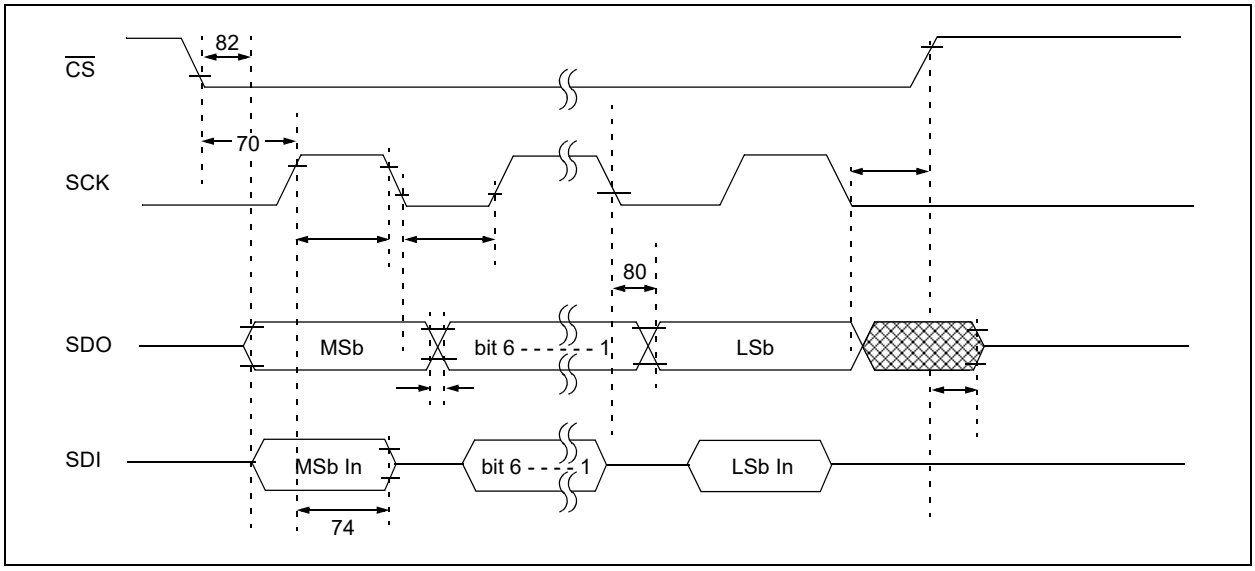


TABLE 5-5: EXAMPLE SPI SLAVE MODE REQUIREMENTS

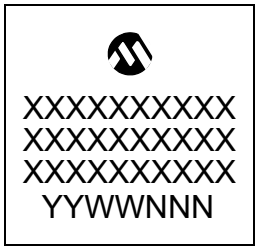
Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH	$\overline{CS}$ ↓ to SCK ↑ Input		50	—	ns	—
71	TscH	SCK Input High Time	Single Byte	50	—	ns	—
72	TscL	SCK Input Low Time	Single Byte	50	—	ns	—
74	TscH2diL	Hold Time of SDI Data Input to SCK Edge		25	—	ns	—
75	TdoR	SDO Data Output Rise Time		—	25	ns	—
76	TdoF	SDO Data Output Fall Time		—	25	ns	—
78	TscR	SCK Output Rise Time (Master mode)		—	25	ns	—
80	TscH2doV, TscL2doV	SDO Data Output Valid after SCK Edge		50	—	ns	—
82	TssL2doV	SDO Data Output Valid after $\overline{CS}$ ↓ Edge		50	—	ns	—
83	TscL2ssH	$\overline{CS}$ ↑ after SCK Edge		50	—	ns	—

NOTES:

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

40-Lead QFN



Example

Legend:	XX...X	Product-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

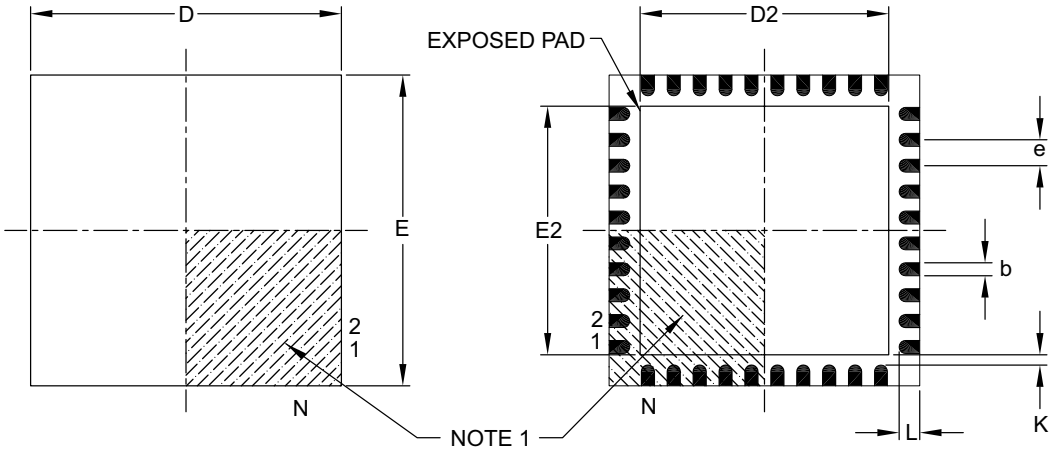
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

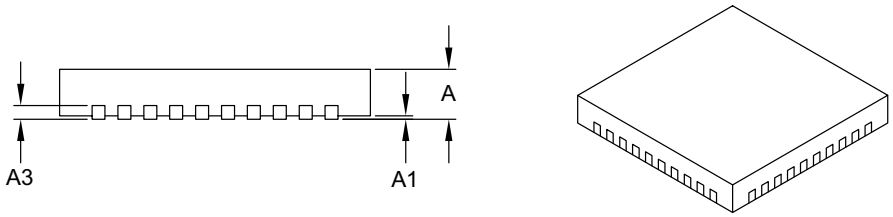
6.2 Package Details

The following sections give the technical details of the packages.

40-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6x0.9 mm Body [QFN] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.50	4.65	4.80
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.50	4.65	4.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-118C

APPENDIX A: REVISION HISTORY

Revision B (October 2008)

Entire data sheet re-written.

Revision C (August 2010)

This document includes the updated technical information.

Revision D (August 2019)

- Minimum operating voltage of the device is revised to 3.0V.
- Updated with new Microchip template, trademarks and document number DS30009776.

Revision E (March 2021)

- Updated correlation value and added equation 3-1 in **Section 3.7 “Link Quality Indication (LQI)”**.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	MRF24J40: IEEE 802.15.4™ 2.4 GHz RF Transceiver
Temperature Range	I = -40°C to +85°C (Industrial)
Package	ML = QFN (Plastic Quad Flat, No Lead) T = Tape and Reel

Example:

a) MRF24J40-I/ML: Industrial temperature, QFN package.

b) MRF24J40T-I/ML: Industrial temperature, QFN package, tape and reel.

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