MTCH650/2

Programmable Voltage Boost with Built-in Level Shifters and Serial Interface with Output Enable

MTCH652 Features:

- 19 High Voltage I/O Lines
- Built-in Boost
- Internal Switch
- 1.8V to 5.5V Input Operating Range
- Low Quiescent Current: <200 µA
- Low Shutdown Current: 1.5 µA, typical
- Up to 50 mA Output Current, at V_{IN} = 3.6V and V_{OUT} = 12V
- The Boost is Driven by an External PWM Allowing for Greater Boost Flexibility
- Selectable Output Voltage Range: 6V, 8V, 10V, 12V, 14V, 16V and 18V
- Selectable Current Limiting
- Selectable Soft Start
- High-Speed SPI Interface:
  - 1 MHz max.
- Output Enable (OE) Independent of SPI Interface
- Built-in Discharge Circuit

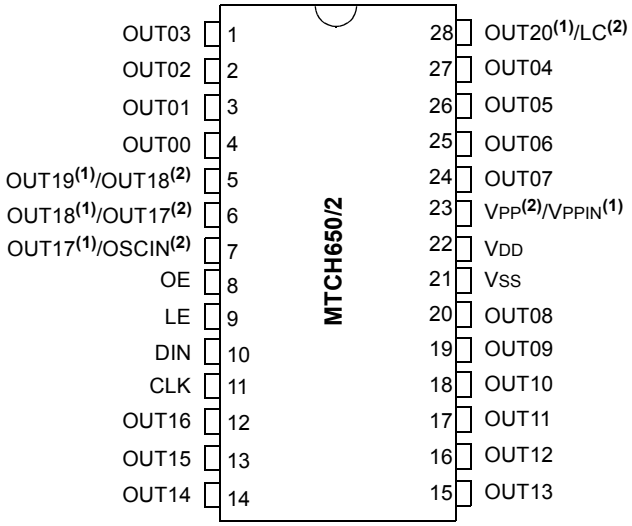
MTCH650 Features:

- 21 High Voltage I/O lines
- 1.8V to 5.5V Input Operating Range
- Low Quiescent Current: <200 µA
- Low Shutdown Current: 1.5 µA typical
- Up to 100 mA Output Current with 5 mA per OUTxx Channel
- Output Enable (OE) Independent of SPI Interface
- 3.6 to 18V External V_{PPIN} Range

Package Type:

- 28-pin SOIC, SSOP
- 28-pin UQFN (4x4)

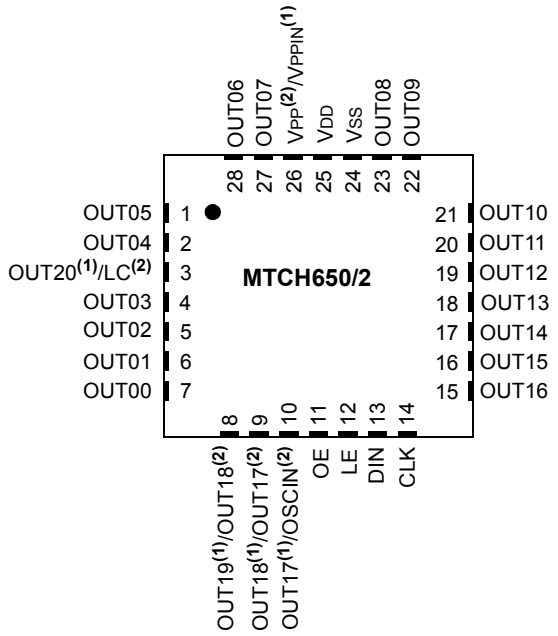
FIGURE 1: 28-PIN SOIC, SSOP DIAGRAM



Note 1: MTCH650

2: MTCH652

FIGURE 2: 28-PIN UQFN DIAGRAM



Note 1: MTCH650

2: MTCH652

TABLE 1: PIN FUNCTION TABLE FOR MTCH650

I/O	28-Pin SOIC/SSOP	28-Pin UQFN	Description
Vss	21	24	Electrical ground or GND
VDD	22	25	Input Voltage Pin
VPP	—	—	Boost Voltage Output
VPPIN	23	26	Boost Voltage Input
LC	—	—	Inductor Boost Connection
OE	8	11	Digital Input (ST)
LE	9	12	Digital Input (ST)
DIN	10	13	Digital Input (ST)
CLK	11	14	Digital Input (TTL)
OSCIN	—	—	Digital Input (TTL)
OUT00	4	7	HV Analog Output
OUT01	3	6	HV Analog Output
OUT02	2	5	HV Analog Output
OUT03	1	4	HV Analog Output
OUT04	27	2	HV Analog Output
OUT05	26	1	HV Analog Output
OUT06	25	28	HV Analog Output
OUT07	24	27	HV Analog Output
OUT08	20	23	HV Analog Output
OUT09	19	22	HV Analog Output
OUT10	18	21	HV Analog Output
OUT11	17	20	HV Analog Output
OUT12	16	19	HV Analog Output
OUT13	15	18	HV Analog Output
OUT14	14	17	HV Analog Output
OUT15	13	16	HV Analog Output
OUT16	12	15	HV Analog Output
OUT17	7	10	HV Analog Output
OUT18	6	9	HV Analog Output
OUT19	5	8	HV Analog Output
OUT20	28	3	HV Analog Output

INPUT VOLTAGE (VDD)

Connect the input voltage to VDD. This pin must be decoupled to GND with a recommended 1 µf minimum capacitor.

BOOST VOLTAGE INPUT (VPPIN)

Boost input voltage must be decoupled to GND with recommended 1 µf minimum capacitor.

OUTPUT ENABLE INPUT (OE)

When OE is set to logic '0', all output latches (OUTxx) are GND. When OE is set to logic '1', all output latches that are set to drive '1' will output the boost voltage level. The OE state is ignored and all OUTxx are high-impedance (High Z) during shutdown or soft-start transient.

LATCH ENABLE INPUT (LE)

Latch Enable Input (LE) is the active-low latch input used for latching-in serial data. Serial data is ignored unless LE is logic '0'. After clocking serial data, the data is internally latched when LE changes from logic '0' to logic '1'.

SERIAL DATA INPUT (DIN)

Serial data input.

SERIAL DATA CLOCK INPUT (CLK)

Serial data clock input.

HV OUTPUT (OUTXX)

High-voltage output pins.

TABLE 2: PIN FUNCTION TABLE FOR MTCH652

I/O	28-Pin SOIC/SSOP	28-Pin UQFN	Description
Vss	21	24	Electrical ground or GND
VDD	22	25	Input Voltage Pin
VPP	23	26	Boost Voltage Output
VPPIN	—	—	Boost Voltage Input
LC	28	3	Inductor Boost Connection
OE	8	11	Digital Input (ST)
LE	9	12	Digital Input (ST)
DIN	10	13	Digital Input (ST)
CLK	11	14	Digital Input (TTL)
OSCIN	7	10	Digital Input (TTL)
OUT00	4	7	HV Analog Output
OUT01	3	6	HV Analog Output
OUT02	2	5	HV Analog Output
OUT03	1	4	HV Analog Output
OUT04	27	2	HV Analog Output
OUT05	26	1	HV Analog Output
OUT06	25	28	HV Analog Output
OUT07	24	27	HV Analog Output
OUT08	20	23	HV Analog Output
OUT09	19	22	HV Analog Output
OUT10	18	21	HV Analog Output
OUT11	17	20	HV Analog Output
OUT12	16	19	HV Analog Output
OUT13	15	18	HV Analog Output
OUT14	14	17	HV Analog Output
OUT15	13	16	HV Analog Output
OUT16	12	15	HV Analog Output
OUT17	6	9	HV Analog Output
OUT18	5	8	HV Analog Output
OUT19	—	—	HV Analog Output
OUT20	—	—	HV Analog Output

INPUT VOLTAGE (VDD)

Connect the input voltage to VDD. This pin must be decoupled to GND with a recommended 1 µf minimum capacitor.

BOOST VOLTAGE OUTPUT (VPP)

Boost output voltage must be decoupled to GND with a recommended 1 µf minimum capacitor.

BOOST INDUCTOR INPUT (LC)

The Boost Inductor Input must be decoupled to GND on the VDD side with a recommended 1 µf minimum capacitor.

OUTPUT ENABLE INPUT (OE)

When OE is set to logic '0', all output latches (OUTxx) are GND. When OE is set to logic '1', all output latches that are set to drive '1' will output the boost voltage level. The OE state is ignored and all OUTxx are high-impedance (High Z) during shutdown or soft-start transient.

LATCH ENABLE INPUT (LE)

Latch Enable Input (LE) is the active-low latch input used for latching-in serial data. Serial data is ignored unless LE is logic '0'. After clocking serial data, the data is internally latched when LE changes from logic '0' to logic '1'.

SERIAL DATA INPUT (DIN)

Serial data input.

SERIAL DATA CLOCK INPUT (CLK)

Serial data clock input.

PWM INPUT (OSCIN)

PWM input signal for boost.

HV OUTPUT (OUTXX)

High-voltage output pins.

Table of Contents

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1.0 DEVICE OVERVIEW

MTCH652 is a compact boost converter, with up to 19 level shifters, which provides an easy-to-use solution for driving High Voltage (HV) outputs. MTCH650 is a line driver device, with 21 level shifters available.

The devices contain a Configuration register (CONFIG) and a data (DATA) register. The CONFIG register can be adjusted using the SPI interface, allowing for voltage changes during application time. The CONFIG register sets the output voltage, the current limit and the Soft Start settings. The DATA register configures the 19/21 bit output mask for the HV output latches. The Output Enable (OE) allows for efficient cycling of the boost voltage on the HV output latches without the delay of setting HV output latches via the serial interface. The HV output latches are set to '0' when Output Enable (OE) is '0'. The HV output latches are set to the output mask when OE is '1'.

MTCH650/2 require only a 3-wire serial interface, latch enable (LE) and two capacitors. MTCH652 requires an additional PWM and a small inductor. The PWM is used to drive the boost and allows flexibility in duty cycle and frequency. The selectable internal Soft Start limits initial in-rush currents, preventing system brown-outs.

Note:	While MTCH650 and MTCH652 are very similar, MTCH650 does not include a built-in boost circuit. MTCH650 will require an external boost voltage device, such as MCP16301 or the output of the MTCH652.

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM FOR MTCH650

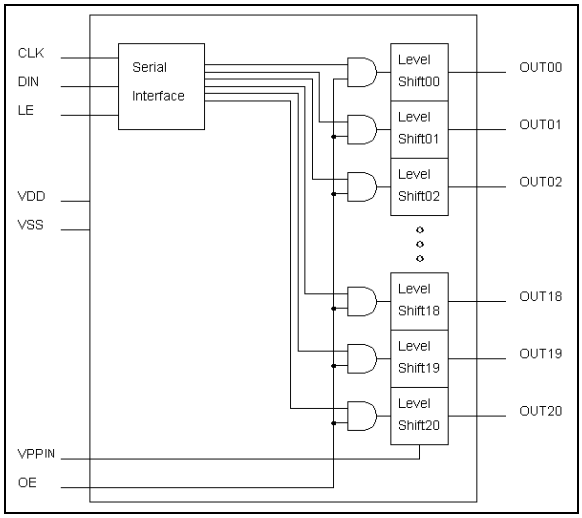
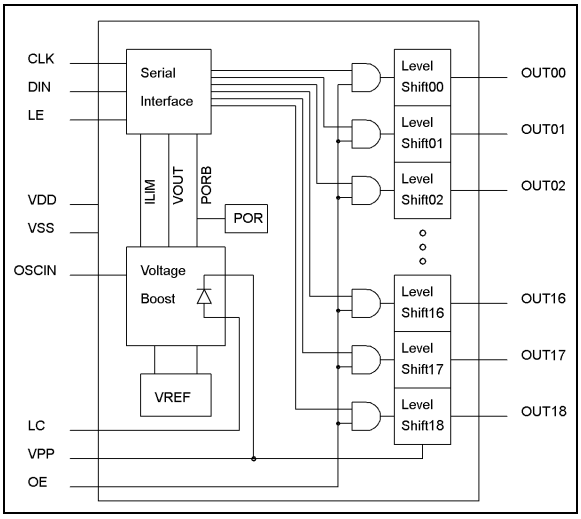


FIGURE 1-2: FUNCTIONAL BLOCK DIAGRAM FOR MTCH652



2.0 POWER-ON RESET (POR)

The on-chip POR circuit holds the device in a Reset state until V_{DD} has reached V_{POR}. The POR is not configurable.

All latches are cleared when POR is active. When V_{DD} is below V_{POR}, the internal shift register will reset to all '0's.

3.0 SERIAL INTERFACE

The serial interface allows configuration of MTCH650/2 during operation. The clock and serial data stream are used to configure a 3-byte wide shift register prior to latching the desired data using Latch Enable (LE) input.

3.1 Loading Data

The shift register is three bytes wide and shifts data from right to left. Therefore, data must be entered in *MSB first to LSB last* sequence, starting with the leading dummy bits set to zero if necessary.

The Data Word selects which HV outputs (OUTxx) are to be cycled with Output Enable (OE).

The Configuration Word sets the shutdown state, boost voltage, current limit and other miscellaneous options.

In addition, Latch Enable (LE) can serve as a chip-select. A high state on LE disables the input shift registers, allowing for sharing of the SPI bus.

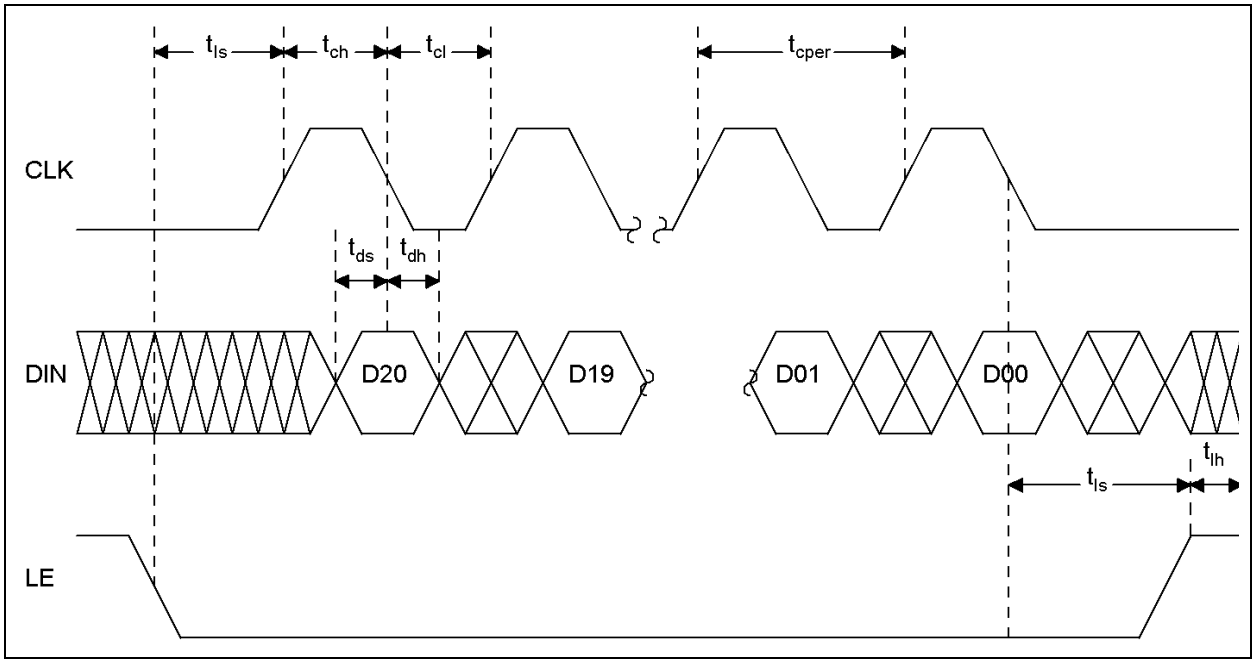
The shift register is written using a clock input, CLK, and a data input, DIN. Data is read on the falling CLK edge. The master loads DIN when CLK is high. The MTCH650 will latch DIN data value on the CLK falling edge.

The contents of the shift register are then loaded into the latches using the latch enable input, LE. The LE signal is asynchronous to the clock. Data is latched on the rising edge of LE. The LE is also a chip-select. If LE is held high, then the device will not accept new serial data. The falling edge of LE re-enables data input and resets the shift register, allowing new data to be clocked-in.

In User mode, latched values are held until overwritten by new data or a POR event occurs.

See Figure 3-1 for details.

FIGURE 3-1: SERIAL TIMING INTERFACE



3.2 Configuration Word

The Configuration Word is selected by setting the LSB of the data stream to '0'. In User mode, using the MTCH652, the output voltage and current limit of the boost circuit can be selected.

Complete Configuration Word documentation can be found in Register 3-1.

3.3 Data Word

The Data Word consists of three bytes of data which set the 21 output pins of the MTCH650, or 19 output pins of the MTCH652, low or high. The Data Word is selected by setting the LSB of the data stream to '1'.

Complete Data Word documentation can be found in Register 3-2.

REGISTER 3-1: CONFIGURATION WORD REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	ILIMDIS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VCMPSEN	SSDIS	ILIM1	ILIM0	VOUT2	VOUT1	VOUT0	SELECT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-9 **Unimplemented:** Read as '0'

bit 8 **ILIMDIS:** Disable Current Limit bit(1)
- 0 = Current limiting enabled (normal operation)
- 1 = Current limiting disabled

bit 7 **VCMPSEN:** Synchronize Boost Regulator Release to OSCIN bit(1)
- 0 = Synchronization disabled (normal operation). When target VPP is achieved, boost regulator switches off asynchronously to OSCIN
- 1 = Synchronization enabled. When target VPP is achieved, boost regulator switches off on rising edge of OSCIN.

bit 6 **SSDIS:** Disable Soft Start bit(1)
- 0 = Soft Start enabled (normal operation)
- 1 = Soft Start disabled, part will start using the current limit set by ILIM<1:0>

bit 5-4 **ILIM<1:0>:** Current Limit Select bit(1)
- 00 = 200 mA
- 01 = 600 mA
- 10 = 1A
- 11 = Over 1.5A

bit 3-1 **VOUT<2:0>:** Boost Voltage Select bits

MTCH652:
- 000 = Shutdown state, Outputs (OUTxx) High-Impedance
- 001 = 6V
- 010 = 8V
- 011 = 10V
- 100 = 12V
- 101 = 14V
- 110 = 16V
- 111 = 18V

MTCH650:
- 000 = Shutdown state, Outputs (OUTxx) High-Impedance
- 001 to 111 = Normal mode

Note 1: OUT19 and OUT20 only implement on MTCH650.

REGISTER 3-1: CONFIGURATION WORD REGISTER

bit 0 **SELECT:** Select Configuration Word or Data Word bit
0 = Configuration Word selected
1 = Data Word selected

Note 1: OUT19 and OUT20 only implement on MTCH650.

REGISTER 3-2: DATA WORD REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	OUTSEL20	OUTSEL19	OUTSEL18	OUTSEL17	OUTSEL16	OUTSEL15
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OUTSEL14	OUTSEL13	OUTSEL12	OUTSEL11	OUTSEL10	OUTSEL9	OUTSEL8	OUTSEL7
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OUTSEL6	OUTSEL5	OUTSEL4	OUTSEL3	OUTSEL2	OUTSEL1	OUTSEL0	SELECT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-22 **Unimplemented:** Read as '0'

bit 21-1 **OUTSEL<20:0>:** Set Output Latches High or Low bits **(1)**
1 = OUT_nn set high
0 = OUT_nn set low

bit 0 **SELECT:** Select Configuration Word or Data Word bit
0 = Configuration Word selected
1 = Data Word selected

Note 1: OUT19 and OUT20 are implemented only on MTCH650.

4.0 VOLTAGE BOOST INTERFACE

MTCH652 includes a voltage boost circuit which generates selectable High Voltage (HV) from V_{DD} using modulated input signal in combination with external inductance and capacitance. The switch and diode are built into the device.

4.1 Boost Connections

4.1.1 INPUTS

OSCIN – a modulated input signal typically derived from a PWM. The duty cycle range is typically from 60 to 90%.

VOUT<2:0> – 3-bit output voltage-select settings. Refer to Register 3-1 for configuration details.

ILIM<1:0> – 2-bit current-limit setting used to limit the maximum current the boost can draw to prevent brown-out of current-limited power supplies. Refer to Register 3-1 for configuration details.

V_{PPIN} – HV input on MTCH650.

4.1.2 OUTPUTS

V_{PP} – HV output of the boost circuit on MTCH652.

LC – Connection for both external inductor and external capacitor for the boost circuit on MTCH652.

4.2 Boost Operation

Under normal operation, OSCIN modulates the gate of the internal switching transistor to build up energy in the LC and raise V_{PP}. The internal circuitry regulates the boost voltage based on the configuration for VOUT<2:0> and ILIM<1:0>. VOUT and ILIM can be changed by the user via the serial interface.

4.3 Soft Start

The boost circuit is equipped with an automatic soft-start feature. This soft-start feature prevents a high initial in-rush current from pulling down the power supply, which will result in a brown-out condition. The current is limited to approximately 200 mA during the initial 16384 OSCIN cycles or about 16 ms with 1 MHz OSCIN frequency after enabling the boost circuit.

After the soft start has timed-out, the current limit reverts to the value selected by the ILIM<1:0> setting.

Disable soft start by setting SSDIS = 1.

4.4 V_{PP} Discharge

When the value of VOUT<2:0> is changed to a lower voltage and the circuit is active, the V_{PP} discharge transistor is enabled until the lower new VOUT is reached. This quickly reduces V_{PP} to the new value. If VOUT<2:0> is changed from a lower to higher voltage, V_{PP} discharge has no effect.

5.0 APPLICATION INFORMATION

5.1 Input Capacitor Selection

Using an input bypass capacitor reduces peak current transients drawn from the input supply and also reduces switching noise generated by the boost. Typically, a ceramic low ESR X5R or X7R capacitor between 1 µF to 10 µF is acceptable.

In applications that are extremely sensitive to high frequency noise, smaller caps with higher operational bandwidth may be placed in parallel with standard recommended values. In applications using much lower than an 1 MHz switching frequency, or in cases with >1A peak inductor currents, larger cap sizes may also be placed in parallel with the standard values.

5.2 Output Capacitor Selection

The output capacitor helps to provide a stable output voltage during sudden load transients and reduces output voltage ripple. As with the input capacitor, X5R and X7R ceramic capacitors are well suited for this application. Typical values are 1 µF to 10 µF.

Note:	Increasing the capacitance value will increase the rise and fall times when switching between boost voltages.

5.3 Inductor Selection

MTCH652 can be used with small surface mount inductors. Typical inductance values are 1 µH to 10 µH.

Note:	An inductance value of 2.2 µH is recommended for initial evaluation.

Several parameters are used to select the correct inductor, maximum rated current, saturation current and copper resistance (ESR). The input current can be much higher than the output current using a boost converter device. A lower ESR value will yield a higher efficiency rate for the converter, which is a common trade-off in component size versus efficiency.

The saturation current specifies a point at which the inductance has rolled off a percentage of the rated value. This can range from 20% to 40% reduction in inductance. As the inductance rolls off, the inductor current increases, as does the peak switch current. It is important to keep the inductance from rolling off too much, causing the switch current to reach the peak limit.

Basic inductor selection is based on a DCR < 0.25 Ω and I_{SAT} > 1.5 x I_{LIM} or 1.5 x I_{PK} (L) (whichever is greater), where I_{LIM} = selected current limit value and I_{PK} (L) = Peak inductor current. Examples of recommended inductors are shown in Table 5-1.

TABLE 5-1: EXAMPLES OF RECOMMENDED INDUCTORS

Part Number	Value (µH)	DCR Ω (typ.)	I_{SAT} (A)	Size WxLxH (mm)
(TDK) MLP2012S2R2M	2.2	0.23	0.8	1.25x2.0x1.0
(Taijo Yuden) CKP2012N2R2M-T	2.2	0.2	0.8	1.25x2.0x1.0
(Samsung) CIG21C2R2MNE	2.2	0.25	0.8	1.25x2.0x1.0
(Taiyo Yuden) BRC2012T1R0M	1	0.06	1.5	1.25x2.0x1.4
(Taiyo Yuden) BRC2012T1R5MD	1.5	0.09	1.2	1.25x2.0x1.4
(Taiyo Yuden) BRC2012T2R2MD	2.2	0.11	1.1	1.25x2.0x1.4
(TDK Corporation) MLP2012S1R0MT0S1	1	0.16	1	1.25x2.0x1
(TDK Corporation) MLP2012S2R2MT0S1	2.2	0.23	0.8	1.25x2.0x1

5.4 PCB Layout Information

Mindful layout techniques are important to any switching circuitry. When wiring high-current paths, short and wide traces should be used. It is important that the input and output capacitors be placed as close as possible to MTCH652 to minimize loop area.

The HV outputs should be routed away from the switching node and switching current loop. When possible, ground planes and traces should be used to help shield the feedback signal and also minimize noise and magnetic interference. In many cases, MTCH650/2 are used in conjunction with sensitive sensing lines. The HV outputs from the MTCH650/2 should be shielded or routed away from these sense lines to reduce noise (see Figure 5-1 and Figure 5-2).

FIGURE 5-1: MTCH652 SOIC AND SSOP RECOMMENDED LAYOUT

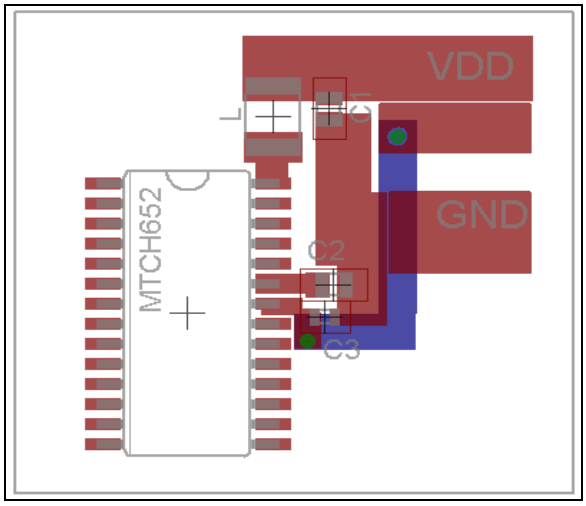
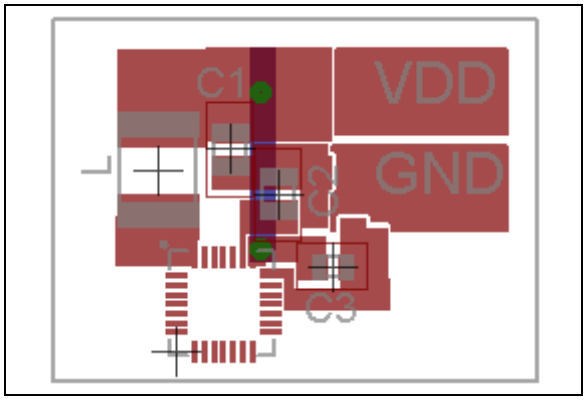


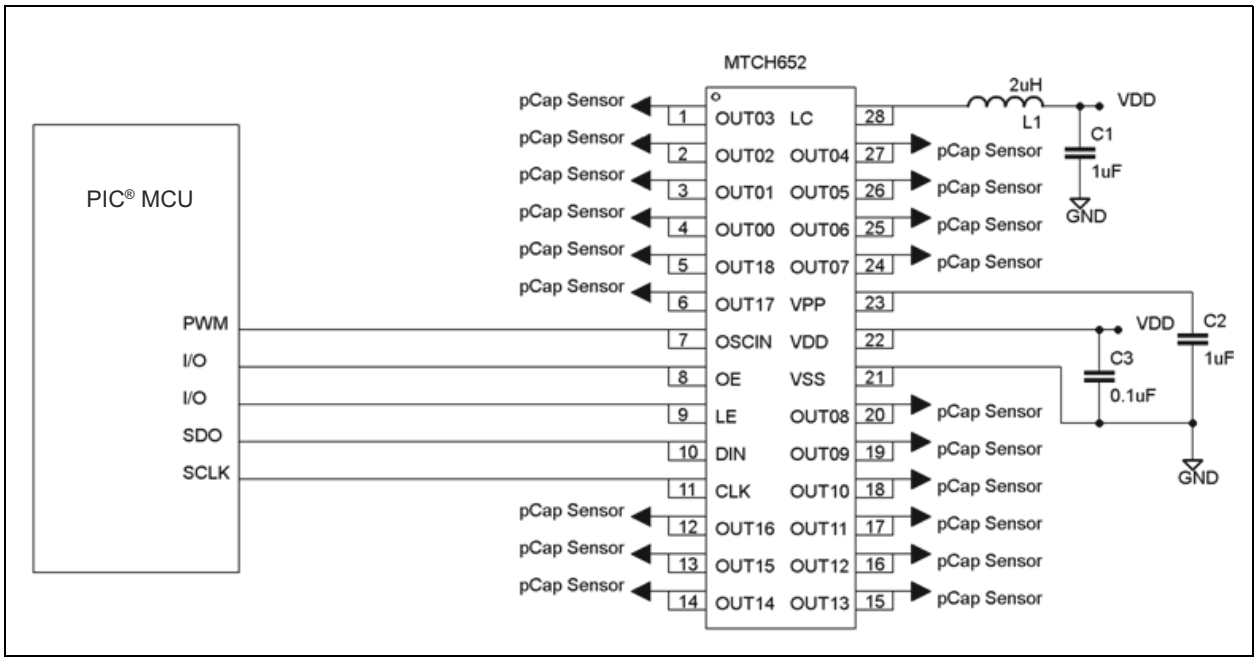
FIGURE 5-2: MTCH652 UQFN RECOMMENDED LAYOUT



6.0 APPLICATION EXAMPLE

MTCH650/2 are very simple to set up and use, only requiring configuration of a Configuration Word and a Data Word. The difference between MTCH650 and MTCH652 is the addition of the PWM input and the selectable options for VOUT and ILIM. Figure 6-1 shows a typical application using a PIC® microcontroller and MTCH652.

FIGURE 6-1: TYPICAL APPLICATION



6.1 MTCH650/2 Connections

The following pins are required to drive MTCH650/2 from the host side:

- PWM – Output (MTCH652 only)
- OE – Output
- LE – Output
- SDO(1) – serial data output
- SCLK(1) – serial data clock output

Note 1: These pins can be from a standard MSSP module or bit-banged.

6.2 MTCH650/2 Initialization

The following shows the basic operations for initialization addressed in additional individual notes within this section:

1. On the host, I/O ports to be used for OE and LE functionality should be configured as outputs. Set OE low and set LE high.
2. Configure the host SPI port for 1 MHz or equivalent bit-bang function. It is recommended that a function that takes the bit mask and sends it to MTCH650/2 be created. Example 6-1 shows such an example.
3. Host sends command to configure the MTCH650/2 CONFIG Word to default settings:
   - ILIMDIS = 0 – ILO Enabled
   - VCMPSEN = 0 – Synchronization Disabled
   - SSDID = 0 – Soft Start Enabled
   - ILIM = 00 – ILIM = 200 mA
   - VOUT = 000 – Boost Disabled

4. (MTCH652 only) Configure the host PWM to output on the correct I/O pin. It is recommended that PWM starts at a frequency of 500 kHz with a 70% duty cycle. It may be necessary to later adjust the parameters to optimize the efficiency and ripple.

EXAMPLE 6-1: BIT-BANG CODE

```
void send MTCH65x (unsigned long data)
{
        unsigned int x;

        MTCH65x_LE_LAT_CLR;
        // clear LE to start
        for (x=0; x<24; x++)
        {
               if (data&0x800000)
               {
                      MTCH65x_DIN_LAT_SET;
                      // bit is a 1
               }
               else
               {
                      MTCH65x_DIN_LAT_CLR;
                      // bit is a 0
               }
               MTCH65x_CLK_LAT_SET;
               MTCH65x_CLK_LAT_CLR;
               data <<= 1;
               // rotate in next bit
        }
        MTCH65x_LE_LAT_SET;
        //set LE latch in the data
}
```

6.3 SPI Specifics

MTCH650/2 serial interface uses the PIC MCU MSSP SPI defaults. The specifics are:

- De-assert LE
- The host changes the state of DIN when CLK is low, data is latched on a low-to-high transition of CLK on the MTCH650/2
- After clocking-in all serial data assert LE, this will latch the new data into the MTCH650/2 internal registers.

6.4 Setting the Boost Voltage

The boost voltage is set with VOUT<2:0> in the Configuration Word. The rise and fall times for boost voltage changes are dependent on ILIM, the capacitor and on V_{PP}. The user must ensure that, when changing boost voltages, the new V_{PP} voltage has settled to the correct value.

6.5 Low Power

For Low-Power or Shutdown modes, set VOUT<2:0> = 000. Turn off the PWM for the absolute minimum operating power mode.

6.6 HV Level Shifters, DATA Latches and OE

Control of the HV level shifters is accessed through the bits OUTSEL<20:0> in the Data Word. Only bits that are set in OUTSEL will have the boost voltage set on the HV level shifters when OE is asserted. All others will remain in a de-asserted state at V_{SS}. When OE is de-asserted, all HV level shifters will be held at V_{SS}.

The user must be aware that MTCH652 has limited current drive. Driving all HV level shifters at the same time may cause an unintended drop in boost. Alternatives for higher drive are to lower the boost voltage or use MTCH650 with an external high-voltage supply.

7.0 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +85°C
Storage temperature ..... -65°C to +150°C
Voltage on pins with respect to V_{SS}
- on LC, V_{PP}, OUTxx ..... -0.3V to 24V
- on V_{DD} pin ..... -0.3V to +6.0V
- on all other pins ..... -0.3V to (V_{DD} + 0.3V)

Total power dissipation(1)
- UQFN ..... 2W at ambient T_A = 25°C (-20 mW/C for T_A > 25°C)
- SOIC ..... 1.4W at T_A = 25°C (-14 mW/C for T_A > 25°C)

Maximum current out of V_{SS} pin 1.5A
Maximum current into LC pin 1.5A
Maximum current in/out of V_{PP}/V_{PPIN} pin 1.5A
Maximum current into V_{DD} pin ..... 250 mA
Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}) ..... ±20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sourced by analog outputs, -40°C < T_A < +85°C for industrial ..... 25 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

7.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \le V_{DD} \le V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \le T_A \le T_{A\_MAX}$

V_{DD} — Operating Supply Voltage

MTCH650/2

- V_{DDMIN} ..... +1.8V
- V_{DDMAX} ..... +5.5V

T_A — Operating Ambient Temperature Range

Industrial Temperature

- T_{A_MIN} ..... -40°C
- T_{A_MAX} ..... +85°C

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table 7-6: “Thermal Characteristics” to calculate device specifications.

7.3 DC Characteristics

TABLE 7-1: BASIC OPERATING CHARACTERISTICS

DC Characteristics		Standard Operating Conditions (unless otherwise stated)				
Sym.	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
VDD	**Supply Voltage**	1.8	—	5.5	V	
IPD	**Standby Current**	—	2	TBD	µA	VDD = 3.6V
IDD	**Supply Current(1)**	—	1.4	TBD	mA	ILIM = 00, VDD = 3.6, Boost to 18V, unloaded
IDD	**Supply Current(1)**	—	0.85	TBD	mA	ILIM = 01, VDD = 3.6, Boost to 18V, unloaded
IDD	**Supply Current(1)**	—	0.8	TBD	mA	ILIM = 10, VDD = 3.6, Boost to 18V, unloaded
VPOR	**Power-on Reset Release Voltage**	0.7	1.1	1.75	V	

Note 1: ILIM = 11, current strongly dependent on OSCIN frequency and duty cycle.

TABLE 7-2: I/O CHARACTERISTICS

DC Characteristics		Standard Operating Conditions (unless otherwise stated)				
Sym.	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
VIL	**Digital Input Low Voltage**	VSS	—	0.2 VDD	V	
VIH	**Digital Input High Voltage**	0.8 VDD	—	VDD	V	
IIL	**Digital Input Leakage Current**	—	±5	±125	nA	85°C; VSS ≤ VPIN ≤ VDD
VOL	**Output Low Voltage**	—	—	0.6	V	IOL = 5 mA
VOH	**Output High Voltage**	VPP – 0.7	—	—	V	IOH = 5 mA

7.4 Analog and AC Characteristics

TABLE 7-3: SERIAL INTERFACE TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)						
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
SI1	t_{ch}	**External CLK High Time**	0.5	∞	µs	
SI2	t_{cl}	**External CLK Low Time**	0.5	∞	µs	
SI3	t_{cper}	**External CLK Period**	1	∞	µs	
SI4	f_c	**External CLK Frequency**	DC	1	MHz	
SI5	t_{ds}	**DIN Setup Time**	10	∞	ns	
SI6	t_{dh}	**DIN Hold Time**	10	∞	ns	
SI7	t_{ls}	**LE Setup Time**	10	∞	ns	
SI8	t_{lh}	**LE High Time**	10	∞	ns	

Note 1: See Figure 3-1 for the corresponding timing diagram.

TABLE 7-4: MTCH652 VOLTAGE BOOST AND TIMING AND ANALOG CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
VB1	FOSC	**External OSCIN Frequency**	—	—	2	MHz	
—	—	**Duty Cycle**	—	—	90%	—	
VB2	VPP	**High Voltage Output**	VDD – 0.8	VDD – 0.3	VDD	V	VOUT = 000 (boost disabled)
			5.4	6	6.6	V	VOUT = 001
			7.2	8	8.8	V	VOUT = 010
			9.0	10	11.0	V	VOUT = 011
			10.8	12	13.2	V	VOUT = 100
			12.6	14	15.4	V	VOUT = 101
			14.4	16	17.6	V	VOUT = 110
			16.2	18	19.8	V	VOUT = 111
VB3	VRIPP	**Ripple Voltage**	—	40	—	mVPP	VDD = 3.6V, Boost to VPP = 18V, 1 µH inductor, 150 pF load, 1 µF VPP capacitor, ILIM = 00
			—	75	—	mVPP	VDD = 3.6V, Boost to VPP = 18V, 1 µH inductor, 150 pF load, 1 µF VPP capacitor, ILIM = 01
			—	85	—	mVPP	VDD = 3.6V, Boost to VPP = 18V, 1 µH inductor, 150 pF load, 1 µF VPP capacitor, ILIM = 10
VB4	ILIMIT	**Switch Current Limit(1)**	—	0.15	0.3	A	ILIM = 00
			—	0.6	1	A	ILIM = 01
			—	1	1.5	A	ILIM = 10
			—	—	1.6	A	ILIM = 11, OSCIN/duty cycle Limited
VB5	IAVG	**Average Output Current**	—	0.5	—	mA	

TABLE 7-4: MTCH652 VOLTAGE BOOST AND TIMING AND ANALOG CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
VB9	t_{resp}	**Response Time**	—	2.3	—	ms	Total for all channels; VPP = 18V, Cload = 15pF per channel, OE frequency = 1 MHZ, ILIM = 00, VDD = 3.6V Boost with 1 µH inductor to VPP = 18V, CVPP = 1uF, unloaded, FOSC = 1 MHz, (**Note 2**)
			—	400	—	µs	Total for all channels; VPP = 18V, Cload = 15pF per channel, OE frequency = 1 MHZ, ILIM = 01, VDD = 3.6V Boost with 1 µH inductor to VPP = 18V, CVPP = 1uF, unloaded, FOSC = 1 MHz, (**Note 2**)
			—	175	—	µs	Total for all channels; VPP = 18V, Cload = 15pF per channel, OE frequency = 1 MHZ, ILIM = 10, VDD = 3.6V Boost with 1 µH inductor to VPP = 18V, CVPP = 1uF, unloaded, FOSC = 1 MHz, (**Note 2**)
		Fall Time	—	—	100	µs	All ILIM, VDD = 3.6V, program fall from VPP = 18V to VPP = 6V Boost with 1 µH inductor, unloaded, CVPP = 1uF, FOSC = 1 MHz

Note 1: These specs are tested at DC. Actual thresholds under dynamic operation may be higher.

2: CVPP = Capacitance between VPP and VSS = C2 in application diagram.

TABLE 7-5: MTCH650 VPP ANALOG CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)						
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
VP1	VPP	**High Voltage Input**	3.6	18	V	VDD < 3.6V
			VDD	18	V	VDD ≥ 3.6V

TABLE 7-6: THERMAL CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)					
Param. No.	**Sym.**	**Characteristic**	**Typ.**	**Units**	**Conditions**
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	69.7	°C/W	28-pin SOIC package
			48	°C/W	28-pin UQFN package
TH02	θ_{JC}	Thermal Resistance Junction to Case	18.9	°C/W	28-pin SOIC package
			12	°C/W	28-pin UQFN package
TH03	T_{JMAX}	Maximum Junction Temperature	150	°C	

NOTES:

8.0 TYPICAL PERFORMANCE CURVES

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "MAXIMUM", "Max.", "MINIMUM" or "Min." represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

FIGURE 8-1: TYPICAL PWM; f_{PWM} = 500 kHz, 70% DUTY CYCLE, V_{DD} = 3.3V

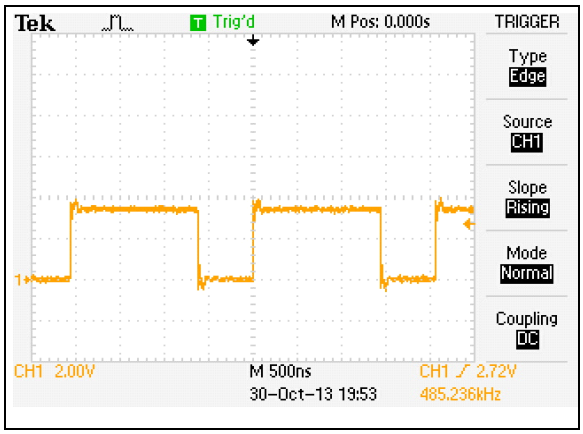


FIGURE 8-2: OE vs. OUT00; V_{DD} = 3.3V, V_{PP} = 18V, $CV_{PP}(C2)$ = 10 µF

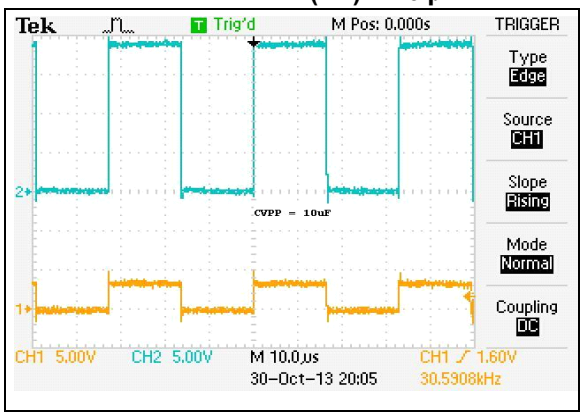


FIGURE 8-3: OE vs. OUT00; V_{DD} = 3.3V, V_{PP} = 18V, $CV_{PP}(C2)$ = 1 µF

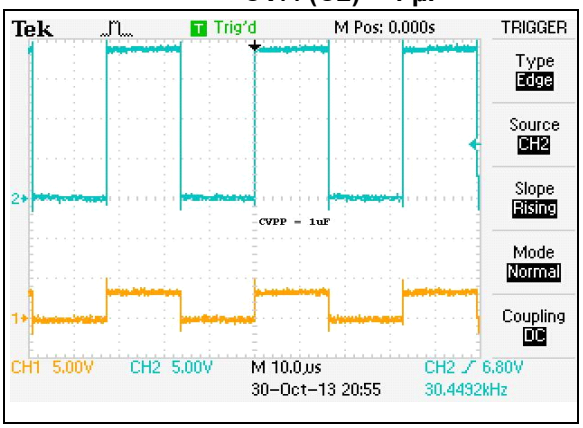


FIGURE 8-4: BOOST V_{PP} 6V TO 18V AND DISCHARGE 18V TO 6V; DISCHARGE ON, V_{DD} = 3.3V, CV_{PP} (C2) = 10 µF

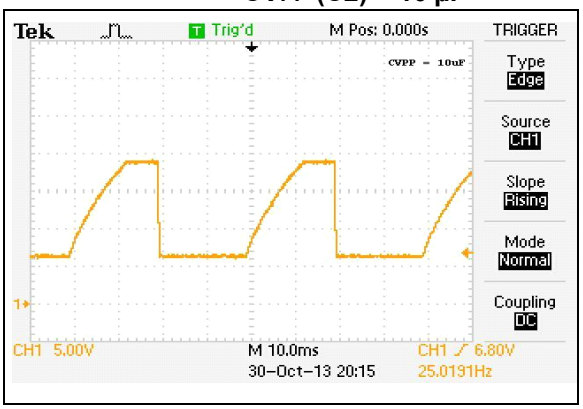


FIGURE 8-5: BOOST VPP 6V TO 18V AND DISCHARGE 18V TO 6V; DISCHARGE ON, VDD = 3.3V, CVPP (C2) = 1 µF

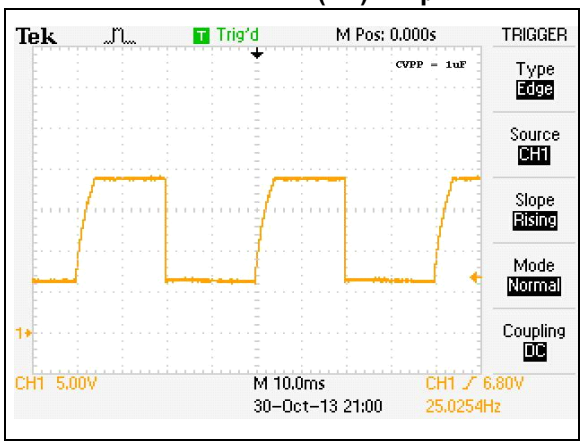


FIGURE 8-6: RIPPLE ON VPP AND OUT00; VDD = 3.3V, VPP = 18V, CVPP (C2) = 10 µF

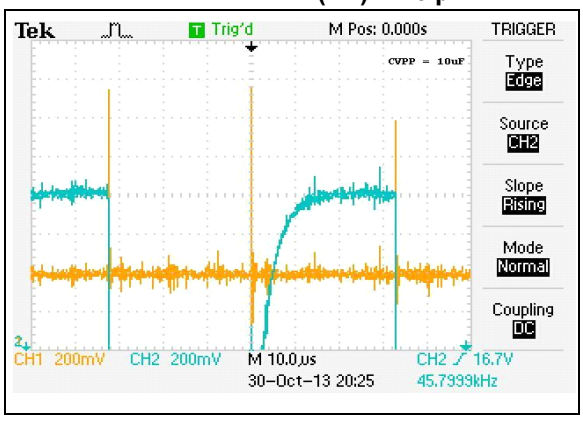
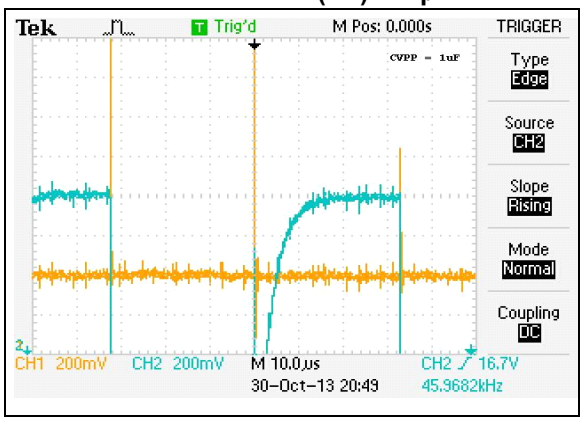


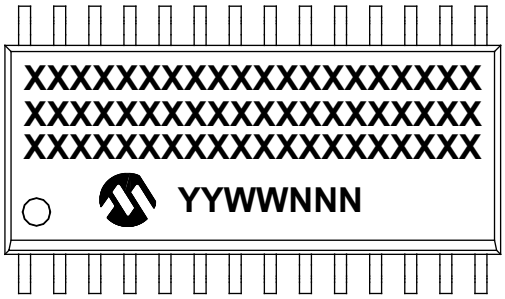
FIGURE 8-7: RIPPLE ON VPP AND OUT00; VDD = 3.3V, VPP = 18V, CVPP (C2) = 1 µF



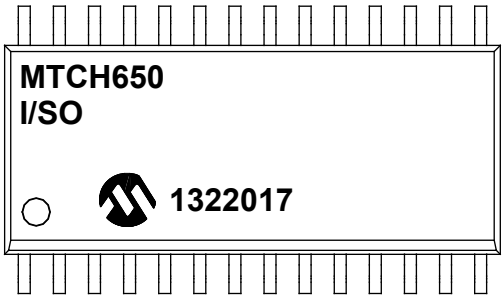
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

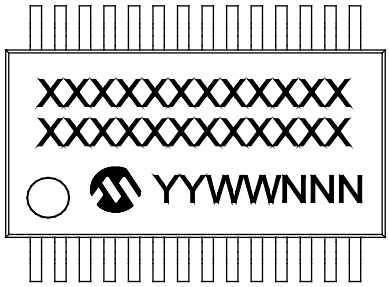
28-Lead SOIC (7.50 mm)



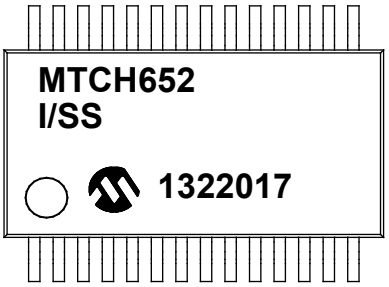
Example



28-Lead SSOP (5.30 mm)



Example



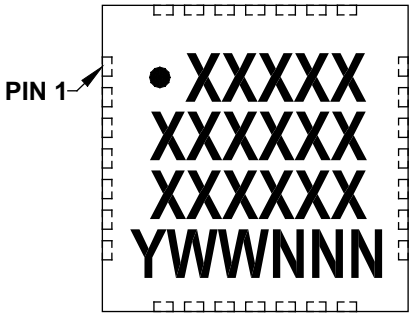
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

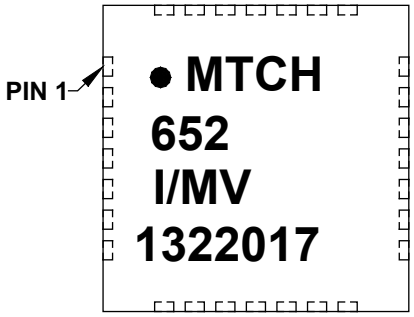
***** Standard PIC® device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

9.1 Package Marking Information (Continued)

28-Lead UQFN (4x4x0.5 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

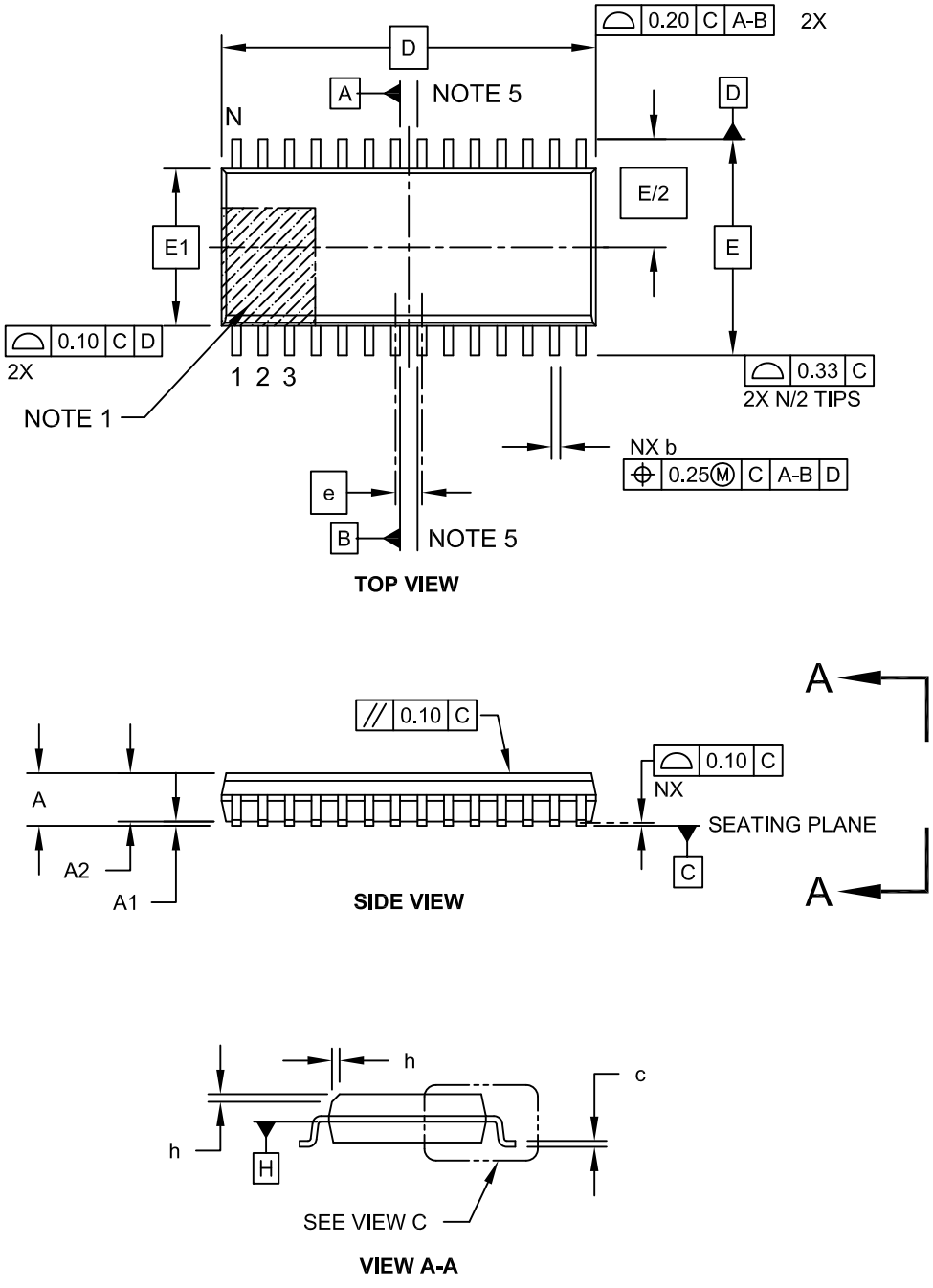
***** Standard PIC® device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

9.2 Package Details

The following sections give the technical details of the packages.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

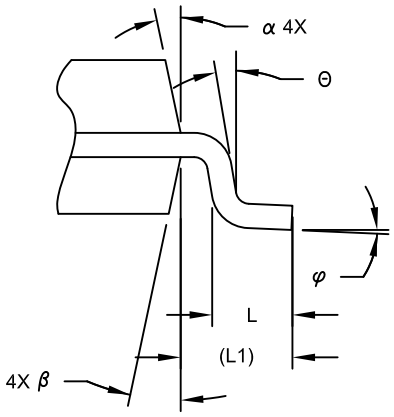
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



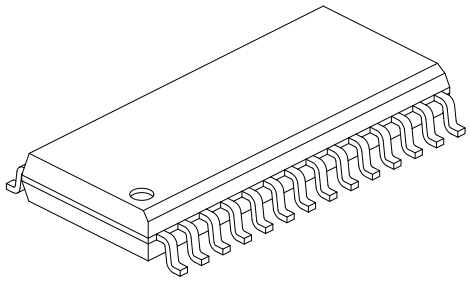
Microchip Technology Drawing C04-052C Sheet 1 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

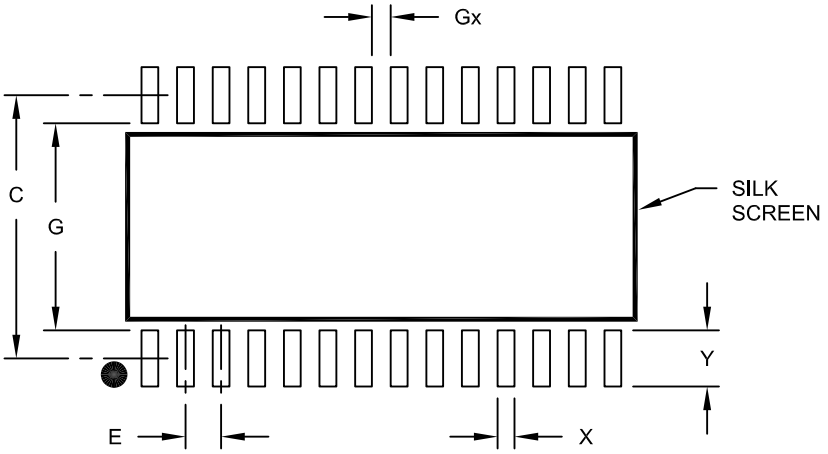
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

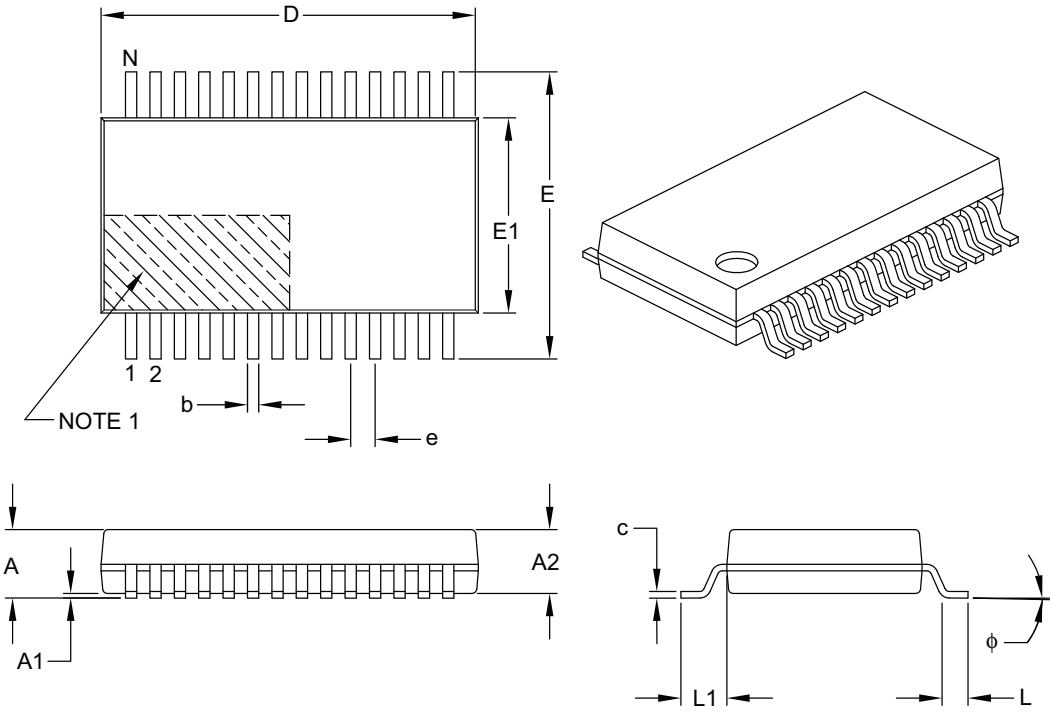
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

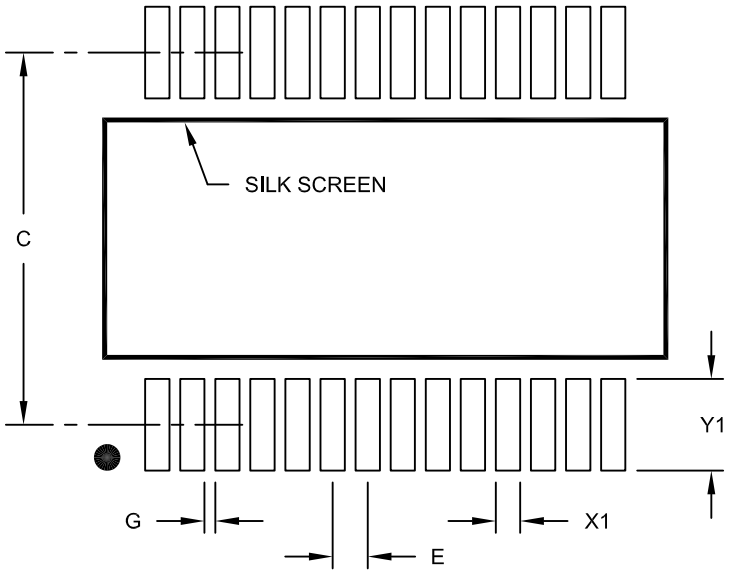
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

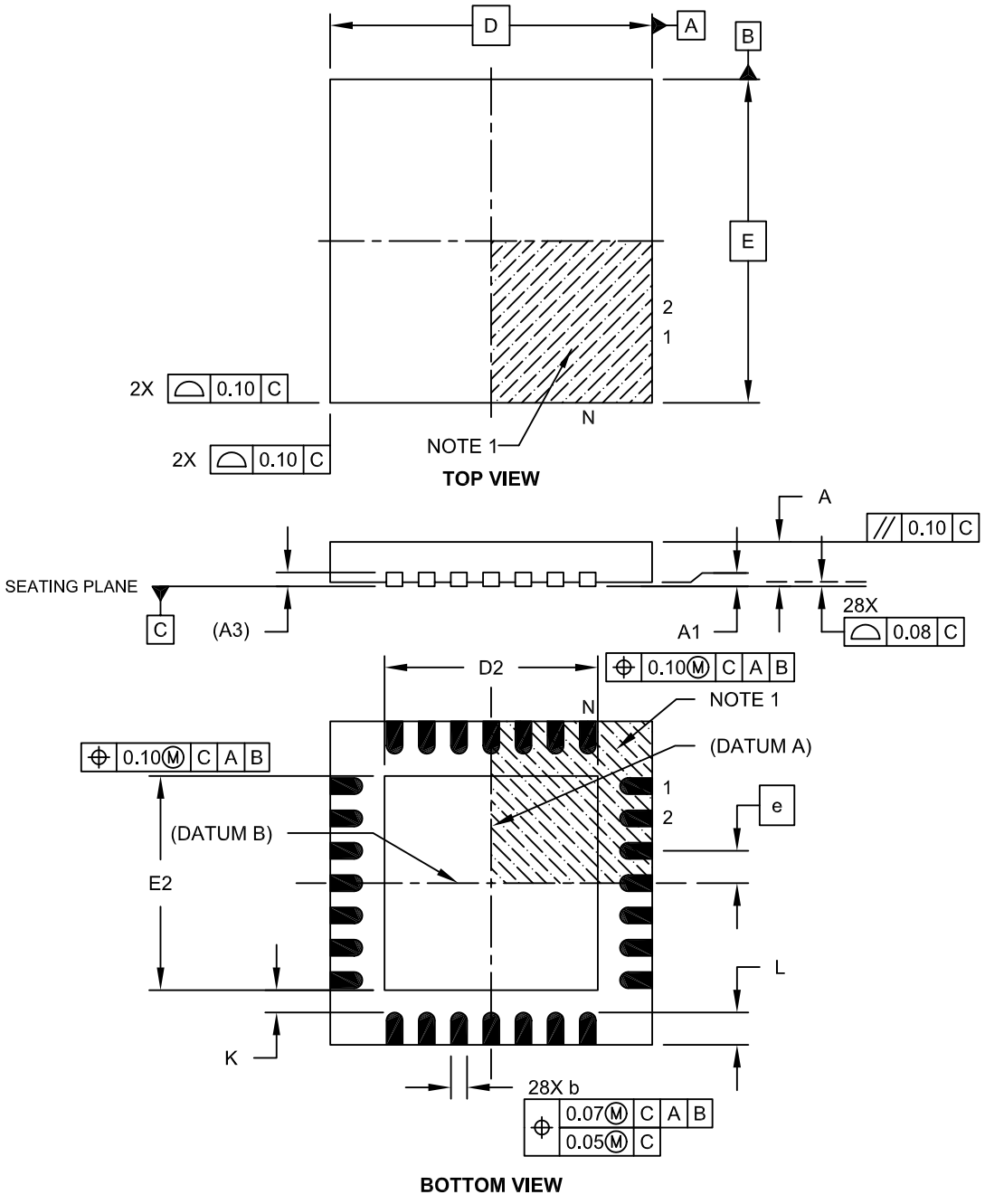
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

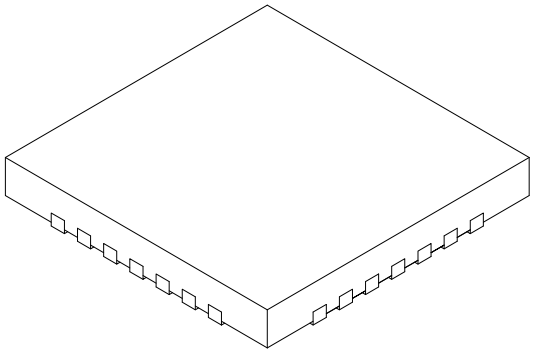
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-152A Sheet 1 of 2

28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.55	2.65	2.75
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.55	2.65	2.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

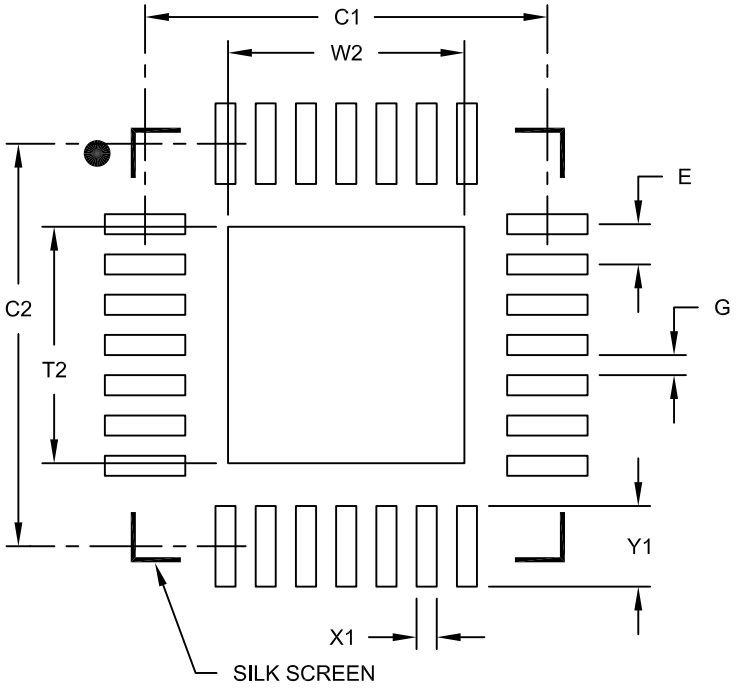
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-152A Sheet 2 of 2

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 4x4 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			2.35
Optional Center Pad Length	T2			2.35
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2152A

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (04/2014)

Initial release of this data sheet.

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PART NO.	[X](1)	-	X	/XX	XXX
Device	Tape and Reel Option		Temperature Range	Package	Pattern

Device:	MTCH650; MTCH652
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel(1)
Temperature Range:	I = -40°C to +85°C (Industrial)
Package:(2)	SO = 28-pin SOIC SS = 28-pin SSOP MV = 28-pin UQFN (4x4x0.5)
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) MTCH652 - I/SO
Industrial temperature
SOIC package.

b) MTCH650 - I/SS
Industrial temperature
SSOP package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.

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