PL133-97

Low-Power DC to 150MHz 1:9 Fanout Buffer IC

FEATURES

- 1:9 LVCMOS output fanout buffer for DC to 150MHz
- 8mA Output Drive Strength
- Low power consumption for portable applications
- Low input-output delay
- Output-Output skew less than 250ps
- Low Additive Phase Jitter of 60fs RMS
- 2.5V to 3.3V, ±10% operation
- 1.8V ± 10% operation up to 67MHz
- Operating temperature range from -40°C to 85°C
- Available in 16-Pin QFN GREEN/RoHS package

DESCRIPTION

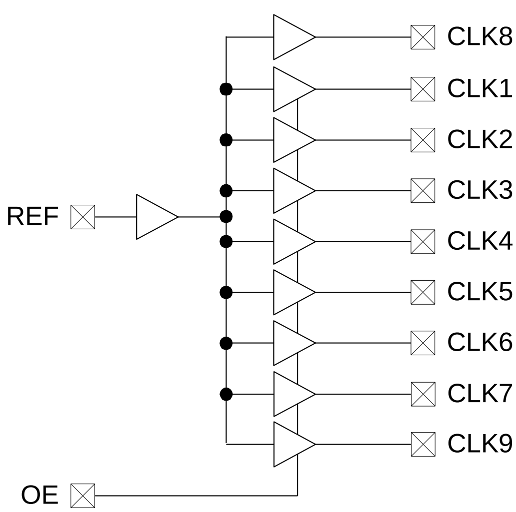
The PL133-97 is an advanced fanout buffer design for high performance, low-power, small form factor applications. The PL133-97 accepts a reference clock input from DC to 150MHz and provides 6 outputs of the same frequency.

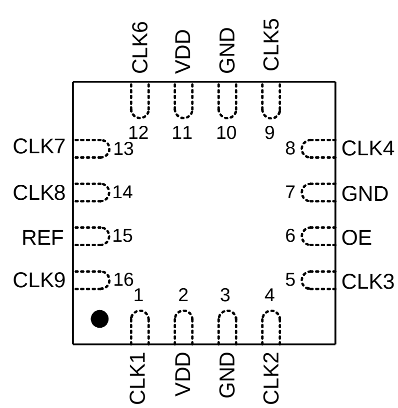
The PL133-97 is offered in a QFN-16L 3x3mm package and it offers the best phase noise, additive jitter performance, and lowest power consumption of any comparable IC.

The PL133-97 outputs can be disabled to a high impedance (tri-state) by pulling low the OE pin. When the OE pin is high, the outputs are enabled and follow the REF input signal. When the OE pin is left open, a pull-up resistor on the chip will default the OE pin to logic 1 so the outputs are enabled.

CLK8 is a free running output that remains enabled when the OE pin is pulled low.

BLOCK DIAGRAM AND PACKAGE PINOUT





QFN-16L

PIN DESCRIPTIONS

Name	QFN-16L	Type	Description
REF	15	I	Input reference frequency.
CLK1	1	O	Buffered clock output
CLK2	4	O	Buffered clock output
CLK3	5	O	Buffered clock output
CLK4	8	O	Buffered clock output
CLK5	9	O	Buffered clock output
CLK6	12	O	Buffered clock output
CLK7	13	O	Buffered clock output
CLK8	14	O	Buffered clock output, free running, does not disable with OE.
CLK9	16	O	Buffered clock output
VDD	2, 11	P	VDD connection
GND	3, 7, 10	P	GND connection
OE	6	I	Output Enable Control Input with 130KΩ Pull-Up
ePad	-	-	Center Pad for Thermal Relief. Connect to GND.

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

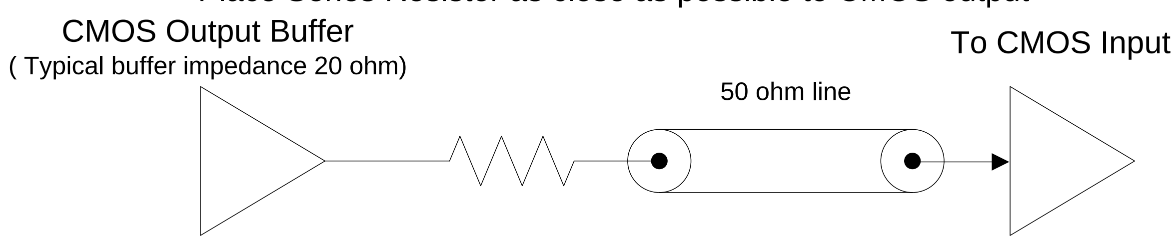
- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces (> 1 inch) as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs using frequencies < 50MHz and 0.01μF for designs using frequencies > 50MHz.

Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



Connect a 33 ohm series resistor at each of the output clocks to enhance the stability of the output signal

ABSOLUTE MAXIMUM CONDITIONS

Supply Voltage to Ground Potential ......–0.5V to 4.6V
DC Input Voltage ....V_{SS} – 0.5V to 4.6V
Storage Temperature .... –65°C to 150°C
Junction Temperature................................ 150°C
Static Discharge Voltage (per MIL-STD-883, Method 3015).............> 2000V

OPERATING CONDITIONS

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	1.62	3.63	V
T_A	Commercial Operating Temperature (ambient temperature)	0	70	°C
	Industrial Operating Temperature (ambient temperature)	-40	85	°C
C_L	Load Capacitance, below 100 MHz, V_{DD} > 2.25V	–	30	pF
	Load Capacitance between 100 MHz and 134 MHz, V_{DD} > 2.25V	–	10	pF
	Load Capacitance, above 134 MHz, V_{DD} > 2.25V	–	5	pF
	Load Capacitance, below 67MHz, 1.62V < V_{DD} < 2.25V	–	15	pF
C_{IN}	Input Capacitance	–	7	pF
REF, CLK[1:9]	Operating Frequency, Input=Output	DC	150	MHz
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

ELECTRICAL CHARACTERISTICS (Commercial and Industrial Temperature Devices)

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage [1]	V_{DD} > 2.25V	–	0.8	V
V_{IH}	Input HIGH Voltage [1]	V_{DD} > 2.25V	2.0	–	V
I_{IL}	Input LOW Current	V_{IN} = 0V	–	50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–	100	µA
V_{OL}	Output LOW Voltage [2]	I_{OL} = 8 mA	–	0.4	V
V_{OH}	Output HIGH Voltage [2]	I_{OH} = –8 mA	2.4	–	V
I_{DD}	Supply Current	66.67MHz with unloaded outputs	–	32	mA
R_{PU}	OE Pin Pull-Up Resistance		100	–	KΩ

SWITCHING CHARACTERISTICS (Commercial and Industrial Temperature Devices) [3]

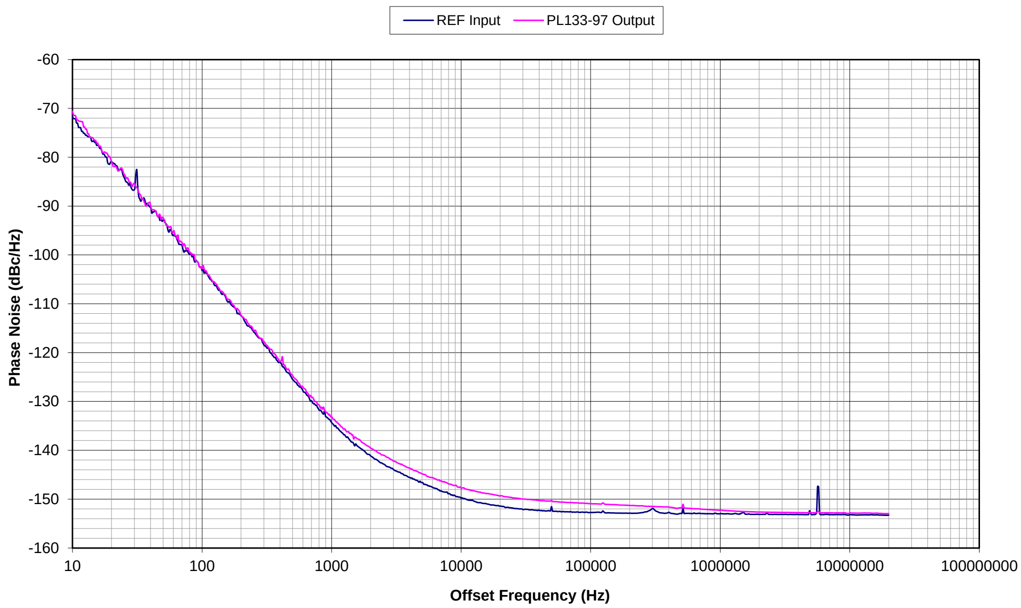
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
	Duty Cycle [2] = t2 ÷ t1	Measured at 1.4V, V_{DD}=3.3V, Input=50%	40	50	60	%
		Measured at V_{DD}/2 , Input = 50%	40	50	60	%
t_3	Rise Time [2]	0.8V → 2.0V , V_{DD}=3.3V , 30pF Load	–	–	1.5	ns
		10% → 90% , V_{DD}=2.5V , 15pF Load	–	–	2.5	ns
		10% → 90% , V_{DD}=1.8V , 15pF Load	–	–	4.5	ns
t_4	Fall Time [2]	2.0V → 0.8V , V_{DD}=3.3V , 30pF Load	–	–	1.5	ns
		90% → 10% , V_{DD}=2.5V , 15pF Load	–	–	2.5	ns
		90% → 10% , V_{DD}=1.8V , 15pF Load	–	–	4.5	ns
t_5	Output to Output Skew [2]	All outputs equally loaded	–	–	250	ps
t_6	Propagation Delay, REF Rising Edge to CLKX Rising Edge [2]	Measured at V_{DD}/2	1	5	9.2	ns

Notes:
1. REF input has a threshold voltage of V_{DD}/2
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.
3. All parameters are specified with loaded outputs.

NOISE CHARACTERISTICS (Commercial and Industrial Temperature Devices)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
	Additive Phase Jitter	V_{DD}=3.3V, Frequency=100MHz Offset=12KHz ~ 20MHz		60		fs

PL133-97 Additive Phase Jitter:
VDD=3.3V, CLK=100MHz, Integration Range 12KHz to 20MHz: 0.059ps typical.

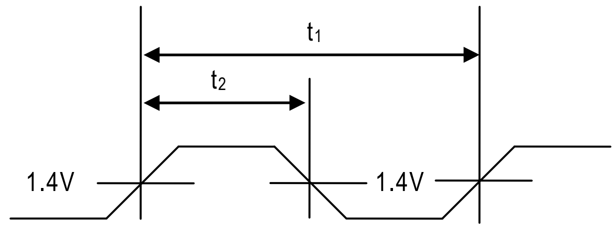


When a buffer is used to pass a signal then the buffer will add a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. To quantify the noise addition in the buffer we compare the Phase Jitter numbers from the input and the output. The difference is called "Additive Phase Jitter". The formula for the Additive Phase Jitter is as follows:

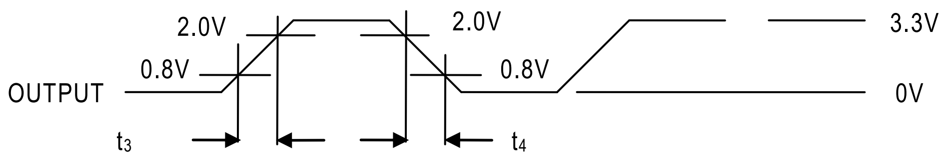
$$\text{Additive Phase Jitter} = \sqrt{(\text{Output Phase Jitter})^2 - (\text{Input Phase Jitter})^2}$$

SWITCHING WAVEFORMS

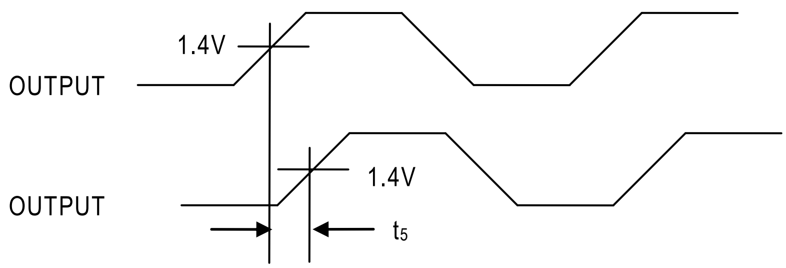
Duty Cycle Timing



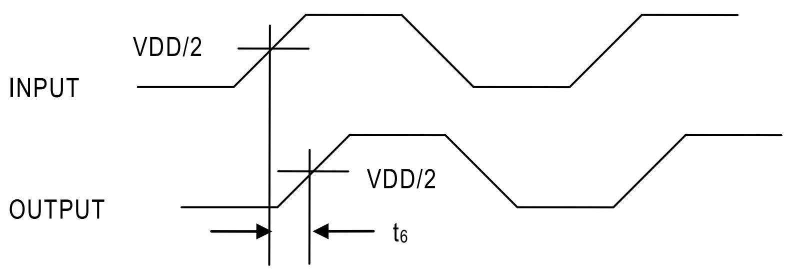
All Outputs Rise/Fall Time



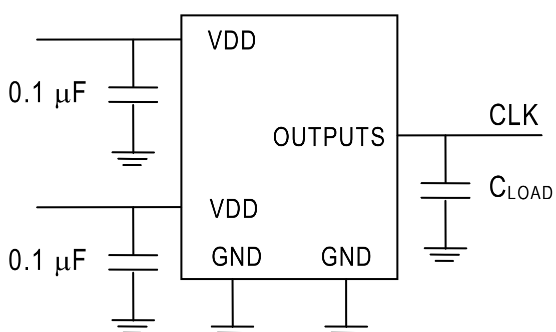
Output-Output Skew



Input-Output Propagation Delay



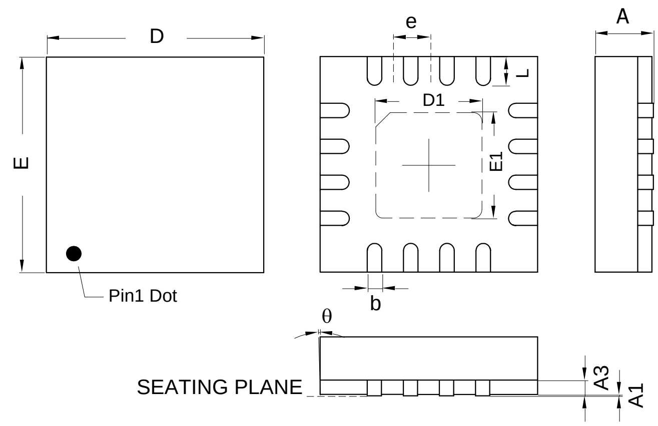
TEST CIRCUIT



PACKAGE DRAWING

QFN-16L

Symbol	Dimension in MM	
	Min.	Max.
A	0.7	0.8
A1	0.05	0.05
A3	0.20	
b	0.18	0.30
D	3.00 BSC	
E	3.00 BSC	
D1	--	1.70
E1	--	1.70
L	0.30	0.50
e	0.50 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL133-97 X X - X

Part Number — PL133-97

R=Tape & Reel

Package Type
Q=QFN

Temperature Range
C=Commercial (0°C to 70°C)
I=Industrial (-40°C to 85°C)

Part/Order Number	Marking	Package Option
Green (Lead-Free) Package		
PL133-97QC-R	P133 97 LLL	16-Pin QFN (Tape and Reel)
PL133-97QI-R	P133 97I LLL	16-Pin QFN (Tape and Reel)

***Note: LLL designates lot number**

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