

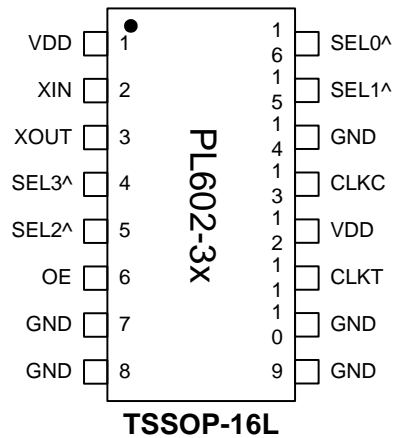
750kHz – 800MHz Low Phase Noise Multiplier XO

Universal Low Phase Noise IC's

FEATURES

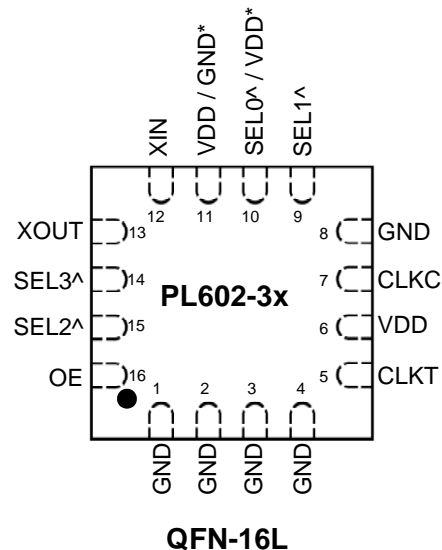
- Selectable 750kHz to 800MHz range.
- Low phase noise output
 - -127dBc/Hz for 155.52MHz @ 10kHz offset
 - -115dBc/Hz for 622.08MHz @ 10kHz offset
- LVCMOS (PL602-37), LVPECL (PL602-35 and PL602-38) or LVDS (PL602-39) output.
- 12MHz to 25MHz crystal input.
- No external crystal load capacitors required.
- Output Enable selector.
- Selectable /16 to x32 frequency divider/multiplier.
- 3.3V operation.
- Available in 16-Pin TSSOP or 16-pin 3x3mm QFN GREEN/RoHS compliant packages.

PIN CONFIGURATION (Top View)

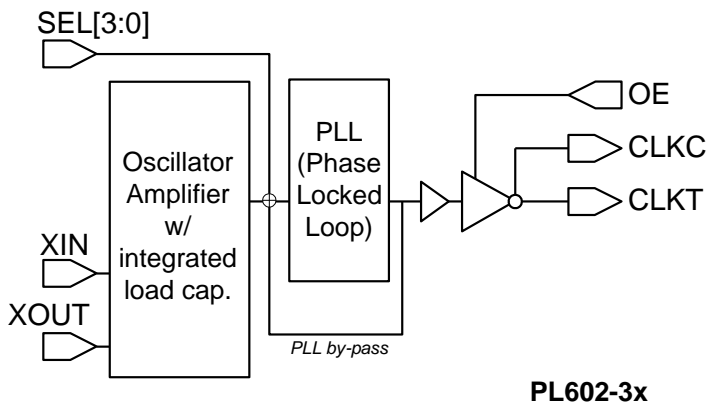


DESCRIPTION

The PL602-35 (LVPECL with inverted OE), PL602-37 (LVCMOS), PL602-38 (LVPECL), and PL602-39 (LVDS) are high performance and low phase noise XO IC chips. They provide phase noise performance as low as -127dBc at 10kHz offset (at 155MHz), by multiplying the input crystal frequency up to 32x. The very low jitter makes them ideal for a wide range of applications, including SONET/SDH and FEC. They accept fundamental parallel resonant mode crystals from 12MHz to 25MHz.



BLOCK DIAGRAM



- ^: Internal pull-up
 - *: On QFN package, PL602-35/-38 do not have SEL0 available: Pin 10 is VDD, pin 11 is GND. However, PL602-37/-39 have SEL0 (pin 10), and pin11 is VDD. See pin assignment table for details.
- Note: On QFN package there is a large center pad for thermal relief. This pad needs to be connected to GND.

OUTPUT ENABLE LOGICAL LEVELS

Part #	OE	State
PL602-38	0 (Default)	Output enabled
	1	Tri-state
PL602-35 PL602-37 PL602-39	0	Tri-state
	1 (Default)	Output enabled

OE input: Logical states defined by LVPECL levels for PL602-38
Logical states defined by LVCMOS levels for PL602-37/-39



PL602-35/-37/-38/-39

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FREQUENCY SELECTION TABLE

SEL3	SEL2	SEL1	SEL0	Selected Multiplier
0	0	1	1	Fin x 32
0	1	1	0	Fin / 8
0	1	1	1	Fin x 2
1	0	0	1	Fin / 2
1	0	1	0	Fin / 16
1	0	1	1	Fin x 4
1	1	0	0	Fin / 4
1	1	0	1	Fin x 8
1	1	1	0	Fin x 16
1	1	1	1	No multiplication

Note: SEL0 is not available (always "1") for PL602-35 and PL602-38 in 3x3mm package

PIN DESCRIPTIONS PL602-35 and PL602-38 (see next page for PL602-37/-39)

Name	TSSOP Pin number	3x3mm QFN Pin number	Type	Description
XIN	2	12	I	Crystal input (See Crystal Specification on page 4)
XOUT	3	13	I	Crystal output (See Crystal Specification on page 4)
OE	6	16	I	Output enable pin (See OE logic state table on page 1)
GND	7,8,9,10,14	1,2,3,4,8,11	P	Ground connection
CLKT	11	5	O	LVPECL True output
CLKC	13	7	O	LVPECL Complementary output
SEL0	16	Not available	I	Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND.
SEL1	15	9	I	
SEL2	5	15	I	
SEL3	4	14	I	
VDD	1, 12	6,10	P	+3.3V power supply.

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PIN DESCRIPTIONS PL602-37/-39 (see previous page for PL602-35/-38)

Name	TSSOP Pin number	3x3mm QFN Pin number	Type	Description
XIN	2	12	I	Crystal input. See Crystal Specification on page 4.
XOUT	3	13	I	Crystal output. See Crystal Specification on page 4.
OE	6	16	I	Output enable pin (see OE logic state table on page 1).
GND	7,8,9,10,14	1,2,3,4,8	P	Ground.
CLKT	11	5	O	LVDS True output for PL602-39. No Connect for PL602-37
CLKC	13	7	O	LVDS Complementary output for PL602-39 LVCMOS out for PL602-37
SEL0	16	10	I	Multiplier selector pins. These pins have an internal pull-up that will default SELx to '1' when not connected to GND.
SEL1	15	9	I	
SEL2	5	15	I	
SEL3	4	14	I	
VDD	1, 12	6,11	P	+3.3V power supply.

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ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	-0.5	$V_{DD}+0.5$	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model		2.5		kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. * **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode	12		25	MHz
Crystal Loading Rating	C_L (xtal)			20		pF
Recommended ESR	R_E	AT cut			30	Ω

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Supply Current, Dynamic (with Loaded Outputs)	I_{DD}	LVPECL/LVDS/ LVCMOS	$F_{OUT} < 24\text{MHz}$			60/28/15	mA
			$24\text{MHz} < F_{OUT} < 96\text{MHz}$			65/45/30	
			$96\text{MHz} < F_{OUT} < 800\text{MHz}$			100/80/40	
Operating Voltage	V_{DD}		2.97		3.63	V	
Output Clock Duty Cycle		@ 50% V_{DD} (LVCMOS)	45	50	55	%	
		@ 1.25V (LVDS)	45	50	55		
		@ $V_{DD} - 1.3\text{V}$ (LVPECL)	45	50	55		
Short Circuit Current				± 50		mA	

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4. Jitter Specifications

PARAMETERS	CONDITIONS	FREQUENCY	MIN.	TYP.	MAX.	UNITS
Period Jitter, RMS	With capacitive decoupling between V_{DD} and GND. Over 10,000 cycles.	155.52MHz		4.3		ps
		622.08MHz		5.0		
Period Jitter, Peak-to-Peak	With capacitive decoupling between V_{DD} and GND. Over 10,000 cycles.	155.52MHz		35		ps
		622.08MHz		45		
Integrated Jitter, RMS	Integrated 12 kHz to 20 MHz	155.52MHz		2.4		ps
		622.08MHz		2.5		

5. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise, relative to carrier (typical)	155.52MHz	-63	-93	-117	-126	-123	dBc/Hz
	622.08MHz	-52	-83	-105	-113	-110	

6. LVCMOS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output drive current	I_{OH}	$V_{OH} = V_{DD} - 0.4V$, $V_{DD} = 3.3V$	10			mA
	I_{OL}	$V_{OL} = 0.4V$, $V_{DD} = 3.3V$	10			mA
Output Clock Rise/Fall Time		0.3V ~ 3.0V with 15 pF load		2.4		ns

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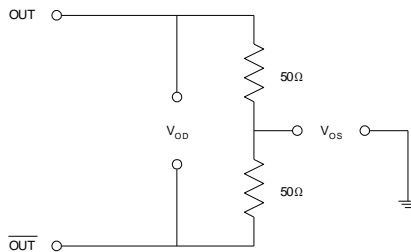
7. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	$R_L = 100\Omega$ (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		± 1	± 10	μA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

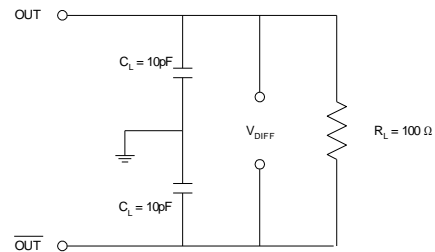
8. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	$R_L = 100\Omega$ $C_L = 10\text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

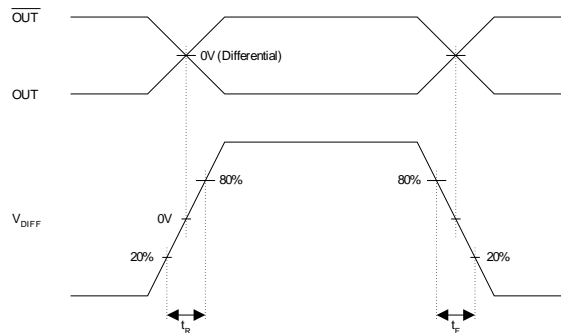
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



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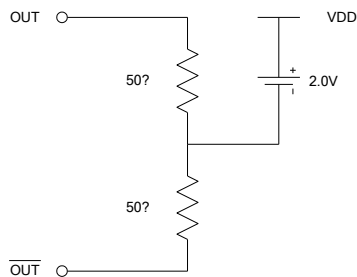
9. LVPECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	$R_L = 50\Omega$ to ($V_{DD} - 2V$) (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	V_{OL}			$V_{DD} - 1.620$	V

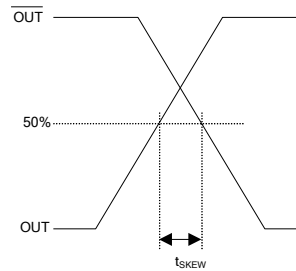
10. LVPECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	20%~80% of Waveform		0.6	1.5	ns
Clock Fall Time	t_f			0.6	1.5	ns

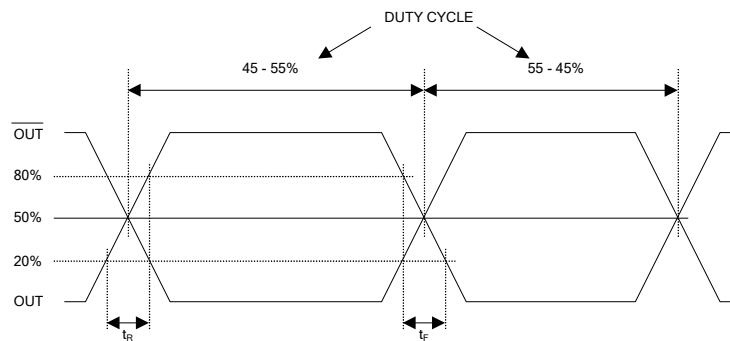
LVPECL Levels Test Circuit



LVPECL Output Skew



LVPECL Transition Time Waveform



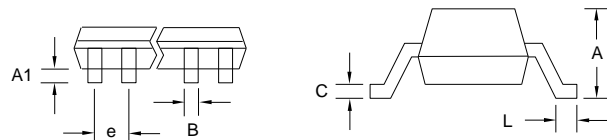
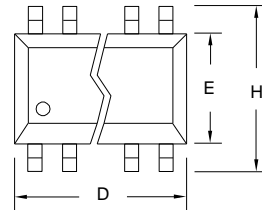
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PACKAGE INFORMATION (GREEN PACKAGE COMPLIANT)

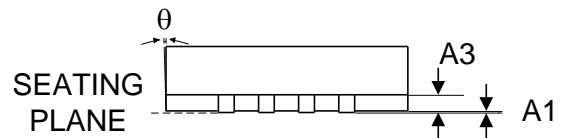
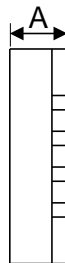
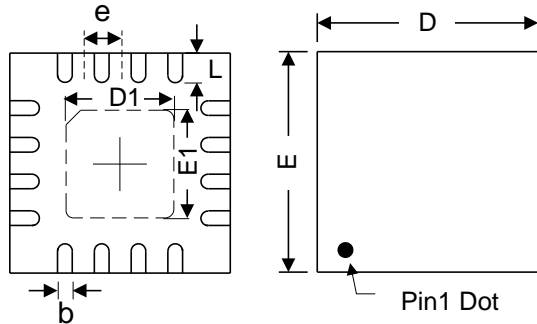
TSSOP-16L

Symbol	Dimension in MM	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
b	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.20	6.60
L	0.45	0.75
e	0.65 BSC	



QFN-16L

Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20		
b	0.20	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
L	0.250	0.300	0.350
e	0.50BSC		



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ORDERING INFORMATION

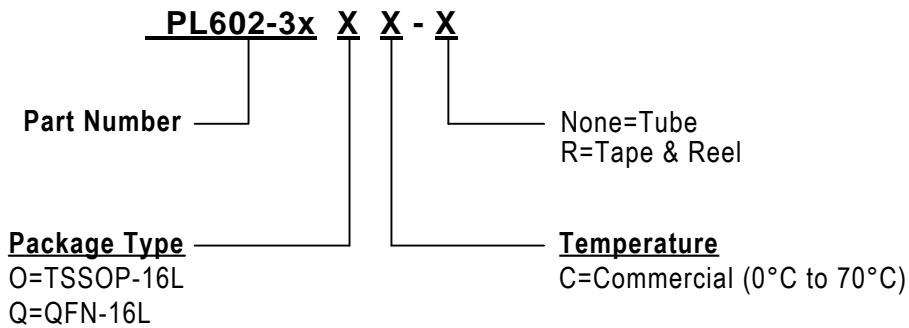
For part ordering, please contact our Sales Department:

2180 Fortune Drive, San Jose, CA 95131, USA

Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type, Operating temperature range, shipping method



Part/Order Number	Marking	Package Option
PL602-35OC	P602-35 OC	16-Pin TSSOP Tube
PL602-35OC-R	LLLLL	16-Pin TSSOP (Tape and Reel)
PL602-35QC-R	P602 35 LLL	16-Pin 3×3 QFN (Tape and Reel)
PL602-37OC	P602-37 OC	16-Pin TSSOP Tube
PL602-37OC-R	LLLLL	16-Pin TSSOP (Tape and Reel)
PL602-37QC-R	P602 37 LLL	16-Pin 3×3 QFN (Tape and Reel)
PL602-38OC	P602-38 OC	16-Pin TSSOP Tube
PL602-38OC-R	LLLLL	16-Pin TSSOP (Tape and Reel)
PL602-38QC-R	P602 38 LLL	16-Pin 3×3 QFN (Tape and Reel)
PL602-39OC	P602-39 OC	16-Pin TSSOP Tube
PL602-39OC-R	LLLLL	16-Pin TSSOP (Tape and Reel)
PL602-39QC-R	P602 39 LLL	16-Pin 3×3 QFN (Tape and Reel)

*Note: "LLL" and "LLLLL" designates lot number



PL602-35/-37/-38/-39

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