PL607041

ClockWorks® PCIe Quad Outputs Ultra-Low Jitter, HCSL Frequency Synthesizer

General Description

The PL607041 is a member of the ClockWorks® family of devices from Micrel and provides an extremely low-noise Spread-Spectrum clock for PCI Express requirements.

The device operates from a 3.3V or 2.5V power supply and synthesizes four HCSL output clocks at 25MHz, 100MHz, 125MHz, and 200MHz. The PL607041 accepts a 25MHz crystal.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

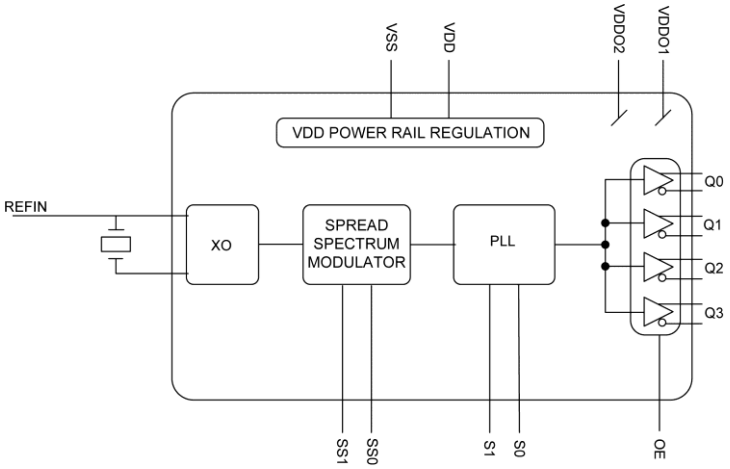
Features

- 25MHz fundamental crystal or reference input
- Generates four HCSL clock outputs at 25MHz, 100MHz, 125MHz, and 200MHz
- Spread spectrum for EMI reduction
- 2.5V or 3.3V operating range
- Typical phase jitter @ 100MHz (1.5MHz to 10MHz): 320fs
- Compliant with PCI Express Gen1, Gen2, and Gen3
- Industrial temperature range (–40°C to +85°C)
- RoHS and PFOS compliant
- Available in 24-pin 4mm × 4mm QFN package

Applications

- Servers
- Storage systems
- Switches and routers
- Gigabit Ethernet
- Set-top boxes/DVRs

Block Diagram



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Ripple Blocker is a trademark of Micrel, Inc.

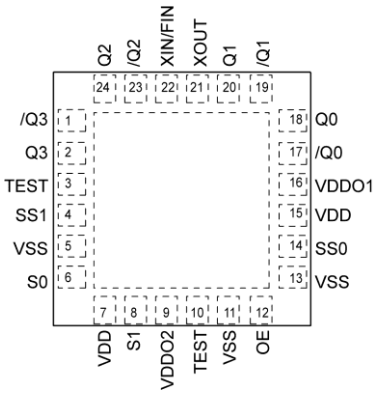
Ordering Information[1]

Part Number	Marking	Shipping	Junction Temperature Range	Package
PL607041UMG	PL607 041	Tube	–40° to +85°C	24-Pin QFN
PL607041UMG TR	PL607 041	Tape and Reel	–40° to +85°C	24-Pin QFN

Note:

1. Devices are RoHS and PFOS compliant.

Pin Configuration



24-Pin QFN
(Top View)

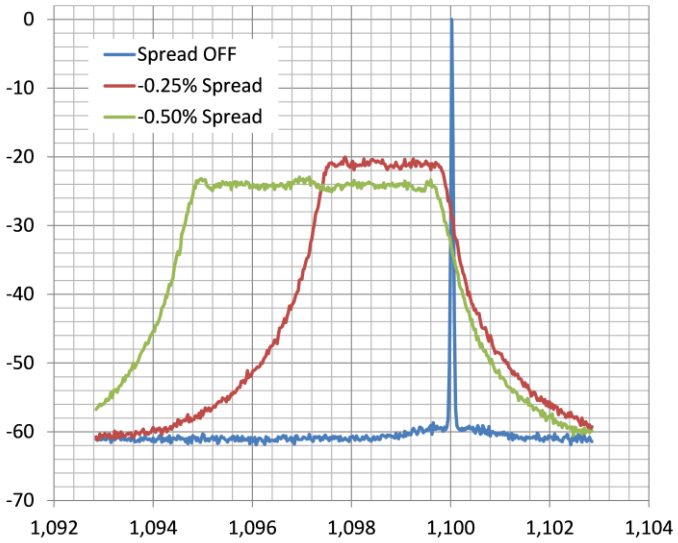
Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
17, 18 19, 20	/Q0, Q0 /Q1, Q1	O, (DIF)	HCSL	Differential Clock Outputs pins.
23, 24 1, 2	/Q2, Q2 /Q3, Q3	O, (DIF)	HCSL	Differential Clock Outputs pins.
9	VDDO2	PWR		Power Supply.
16	VDDO1	PWR		Power Supply.
7, 15	VDD	PWR		Core Power Supply.
5, 11, 13	VSS	PWR		Power Supply Ground.
6, 8	S0, S1	I	LVCMOS	Frequency Select for 25MHz, 100MHz, 125MHz, and 200MHz. Each pin has a 45kΩ pull-up.
14, 4	SS0, SS1	I	LVCMOS	Spread Spectrum Select pins. Each pin has a 60kΩ pull-up.
22	XIN/FIN	I, (SE)	Crystal	Crystal or Reference Input, no load caps needed (see Figure 5).
21	XOUT	O, (SE)	Crystal	Crystal Output, no load caps needed (see Figure 5).
12	OE	I, (SE)	LVCMOS	Output Enable/Disable.
3, 10	TEST	I		Factory test pins. Keep these pins floating.

EMI Reduction

The Spread Spectrum modulation causes the emission of spectral components in the clock signal to be reduced. The spectrum plot on the right shows measurement results with the two spread settings versus no spread. This plot is looking at the 11th harmonic in a 100MHz clock, at 1.1GHz. The scale is normalized to the strength of this spur without spread. The plot shows about 21dB reduction for -0.25% spread magnitude and 24dB for -0.50% spread magnitude.

The plot also shows how the frequency spreading is happening downwards.



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Absolute Maximum Ratings[2]

Supply Voltage ($V_{DD,}$ $V_{DDO1/2}$).....+4.6V
Input Voltage (V_{IN}).....–0.50V to V_{DD} + 0.5V
Lead Temperature (soldering, 20s).....260°C
Case Temperature .....115°C
Storage Temperature (Ts).....–65°C to +150°C

Operating Ratings[3]

Supply Voltage (V_{IN})..... +2.375V to +3.465V
Ambient Temperature (T_A) .....–40°C to +85°C
Junction Thermal Resistance[4]
QFN (θ_{JA}) .....50°C/W
QFN (ψ_{JB}).....30°C/W

Electrical Characteristics[5]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}, $V_{DDO1/2}$	2.5V operating voltage		2.375	2.5	2.625	V
V_{DD}, $V_{DDO1/2}$	3.3V operating voltage		3.135	3.3	3.465	V
I_{DD}	Supply current V_{DD} + V_{DDO}	Outputs 50Ω to V_{SS}		150	185	mA

HCSL DC Electrical Characteristics[5]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C. RL = 50Ω to V_{SS}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage		660	700	850	mV
V_{OL}	Output Low Voltage		–150	0	27	mV
V_{CROSS}	Crossing Point Voltage		250	350	550	mV

LVCMOS (S0, S1) Electrical Characteristics[5]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		2.0		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	–150			µA

Notes:

2. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. The device is not guaranteed to function outside its operating ratings.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
5. The circuit is designed to meet the AC and DC specifications shown in the above table(s) after thermal equilibrium has been established.

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	15pF load capacitance		Fundamental, Parallel Resonant		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitor, C0			1	7	pF
Correlation Drive Level			10	100	µW

AC Electrical Characteristics[6, 7]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C. RL = 50Ω to V_{SS}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency			25 100 125 200		MHz
F_{REF}	Crystal Input Frequency			25		MHz
FIN	Reference Input Frequency			25		MHz
FIN	FIN Signal Amplitude	Internally AC-coupled	0.9		V_{DD}	V_{PP}
T_R/T_F	HCSL Output Rise/Fall Time	20% - 80%	150	300	450	ps
ODC	Output Duty Cycle		48	50	52	%
T_{SKEW}	Output-to-Output Skew	Note 7			45	ps
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(Ø)$	RMS Phase Jitter[8]	100MHz Integration Range (1.5MHz – 10MHz)		320		fs
	Cycle-to-Cycle Jitter				30	ps, peak

Notes:

6. All phase noise measurements were taken with an Agilent 5052B phase noise system.
7. Defined as skew between outputs at the same supply voltage and with equal load conditions; measured at the output differential crossing points.
8. Measured using 25MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz.

Spread Spectrum Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Modulation Rate[9]			31.6		kHz
Modulation Magnitude[10]	Setting is -0.25%	-0.073 to -0.265	0 to -0.250	+0.031 to -0.375	%
	Setting is -0.50%	-0.136 to -0.383	0 to -0.500	+0.078 to -0.589	%

Notes:

9. The modulation rate is created from the crystal frequency, divided by 792.
10. The typical modulation makes the output frequency sweep between the target frequency (0%) and the down-spread value (-0.25% or -0.5%). There is process variation on the modulation magnitude and the smallest and largest possible modulation magnitude sweep ranges are listed in the table.

Truth Tables

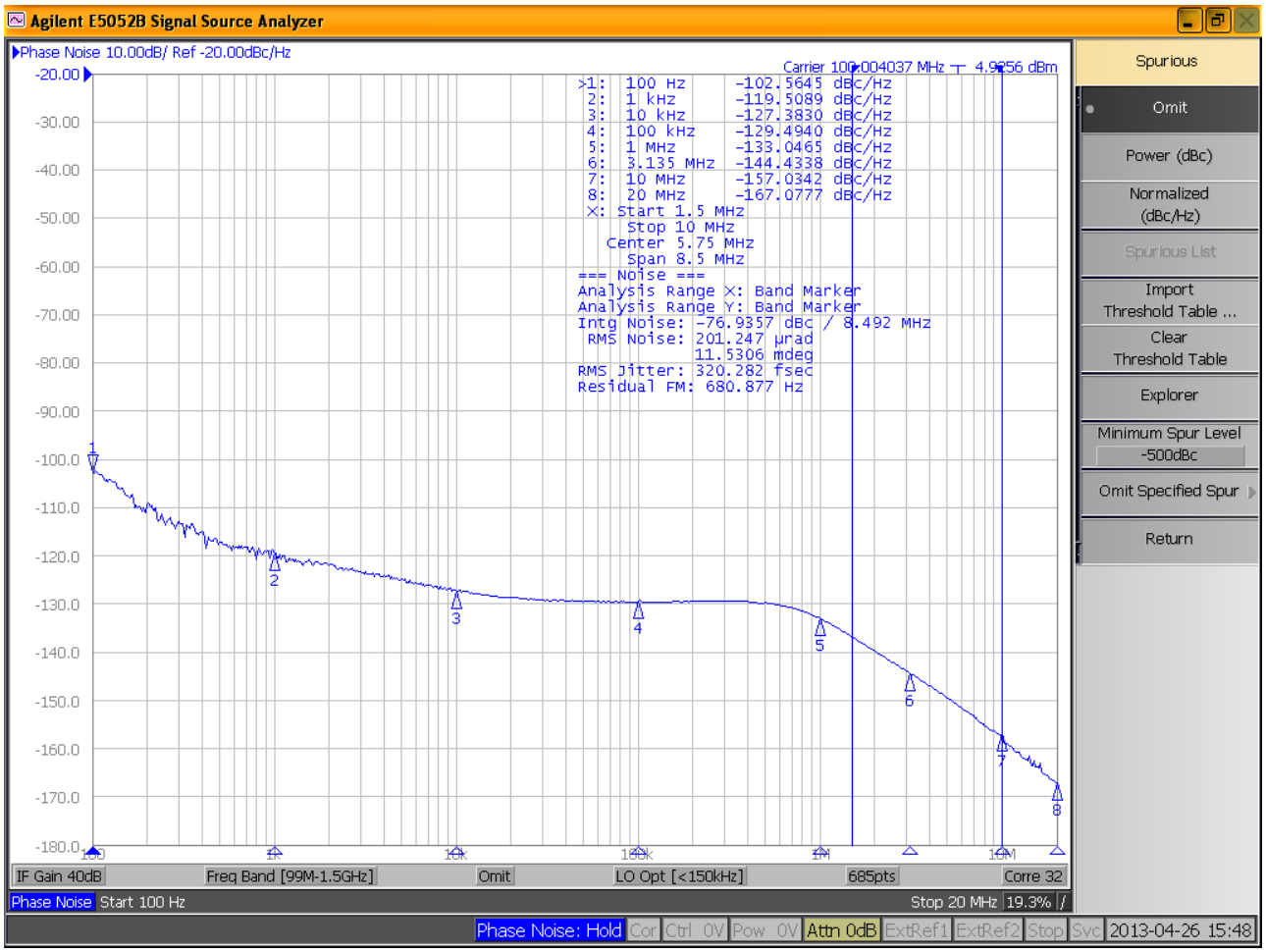
S1	S0	OUTPUT
0	0	25MHz
0	1	100MHz
1	0	125MHz
1	1	200MHz

SS1[11]	SS0[11]	Spread Type	Spread
0	0	Spread is OFF	No Spread
0	1	Down Spread	-0.25%
1	0	Spread is OFF	No Spread
1	1	Down Spread	-0.50%

Note:

11. SS0 is turning ON/OFF the spread spectrum modulation and SS1 is selecting the spread magnitude.

Phase Noise Plot



Phase Noise Plot: 100MHz, 1.5MHz – 10MHz 320fs

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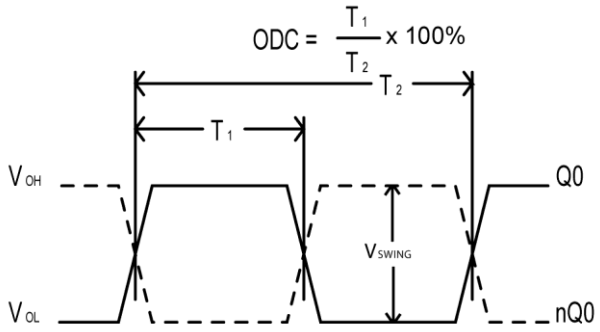


Figure 1. Duty Cycle Timing

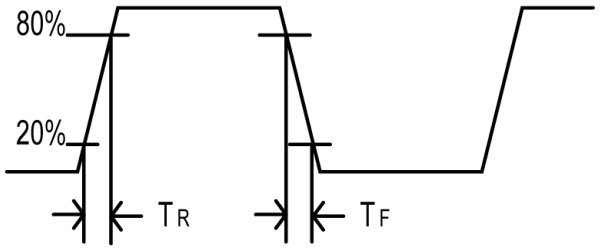


Figure 2. All Outputs Rise/Fall Times

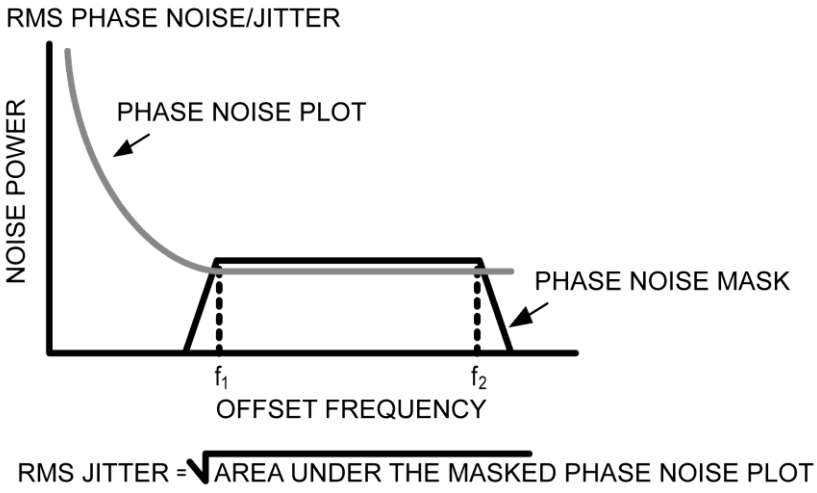


Figure 3. RMS Phase/Noise Jitter

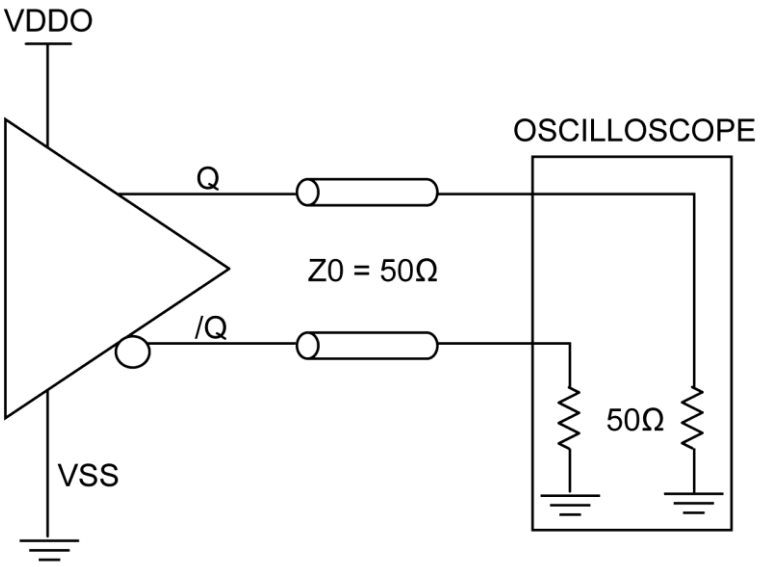


Figure 4. HCSL Output Load and Test Circuit

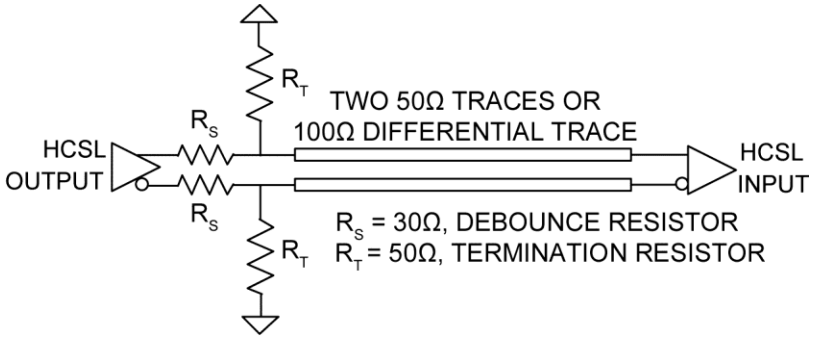


Figure 5. HCSL Recommended Application Termination (Source Terminated)

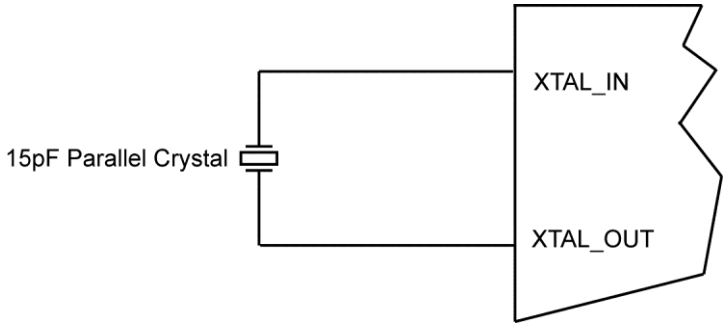


Figure 6. Crystal Input Interface

Application Information

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die so no external capacitance is needed. See the *Selecting a Quartz Crystal for the Clockworks Flex / Family of Precision Synthesizers* application note for more details.

Contact Micrel's TCG applications group at: tcghelp@micrel.com if you need help selecting a suitable crystal for your application.

Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7nF above) between the VDD and VSS pins, as close as possible to those pins and at the same side of the PCB as the IC. The shorter the physical path from VDD to capacitor and back from capacitor to VSS, the more effective the decoupling. Use one 4.7nF capacitor for each VDD pin on the PL607041.

The impedance value of the Ferrite Bead (FB) needs to be between 240Ω and 600Ω with a saturation current ≥150mA.

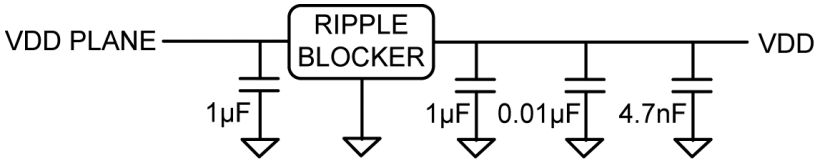
VDDO1 and VDDO2 pins connect directly to the VDD Plane. All VDD pins on the PL607041 connect to VDD after the power supply filter.

HCSL Outputs

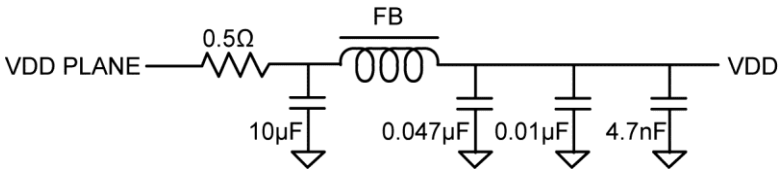
HCSL outputs are to be terminated with 50Ω to V_{SS}. For best performance load all outputs. If you want to AC-couple or change the termination, contact Micrel's application group: tcghelp@micrel.com (see Figure 5).

Power Supply Filtering Recommendations

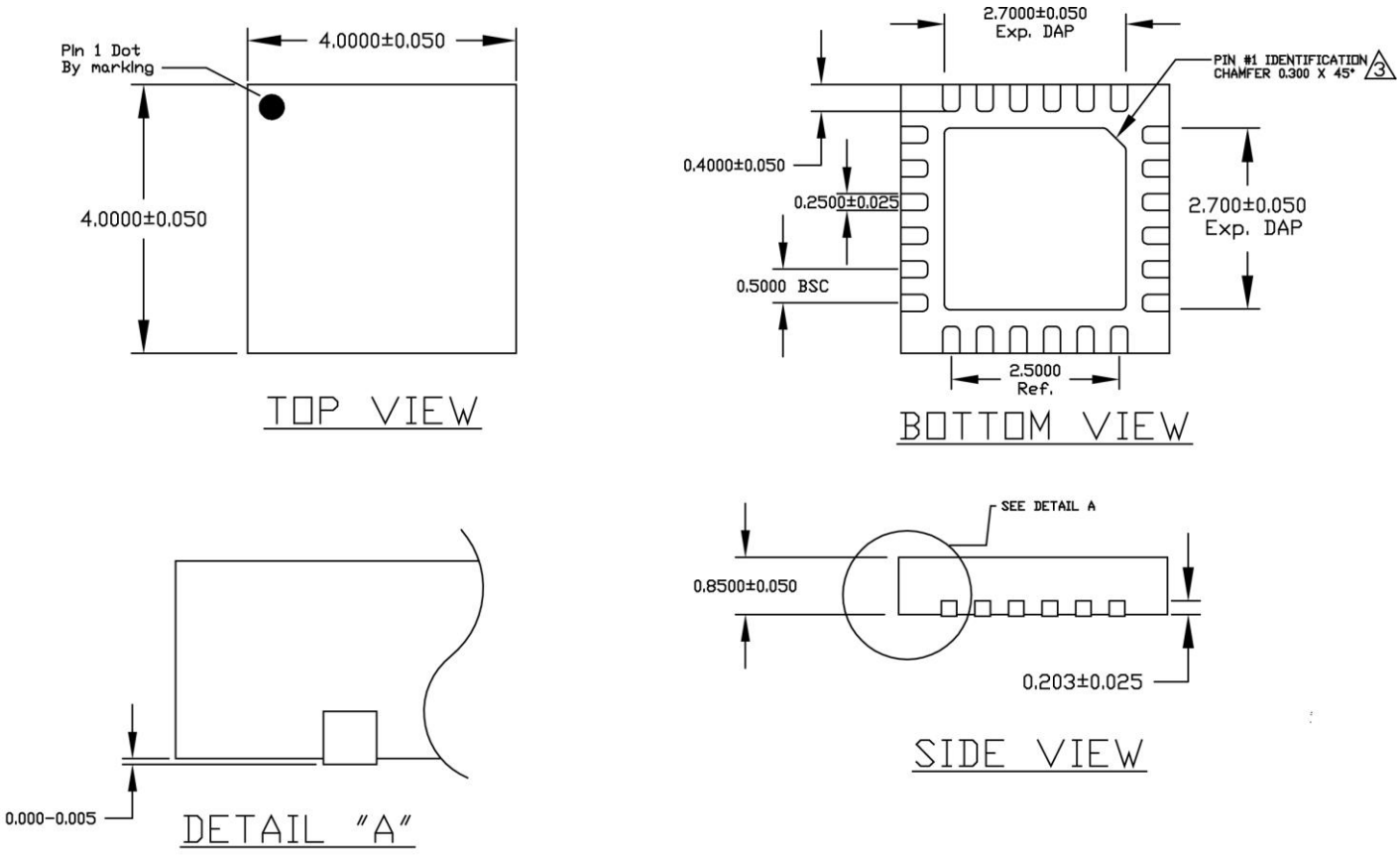
Preferred filter, using Micrel's MIC94300 or MIC94310 Ripple Blocker™:



Alternative, traditional filter, using a ferrite bead:



Package Information[12]



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS (mm).
2. THE PIN#1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
3. CHAMFER STYLE PIN 1 IDENTIFIER ON BOTTOM SIDE

24-Pin QFN

Note:

12. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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