PM4329

HDLIU 32

32 Channel High Density E1/T1/J1 Line Interface Unit

Product Overview

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Issue No. 6: November, 2005

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Copyright

PMC-2030541, Issue 6

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U.S. Patent No. US5973977 and US6774693. Canadian Patent No. CA2242152. Other relevant patent grants may also exist.

Revision History

Issue No.	Issue Date	Details of Change
6	November 2005	Updated ordering information including ROHS compliant device.
5	November 2004	Production released version. Updated receiver sensitivity with characterized values. Added Integrated Add/Drop Multiplexer for 155Mbps & 622Mbps application.
4	May 2004	Preliminary version for FCA.
3	October 2003	Advance issue. Added ALOS detection calibration description.
2	June 2003	Advance issue.
1	April 2003	Initial Creation

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Preface

In order to understand the information in this document, the reader should have a strong working understanding of both T1 and E1 standards.

Related Documents

For a current and complete list of the documentation available for this device, visit the web site at http://www.pmc-sierra.com

Document	Description
Product Overview (PMC-2030541)	The Product Overview describes the high level features of the device and is intended for the system designer. The Product Overview is essential reading for system architects who are evaluating the device and for designers who will use the device.
Hardware Specification (PMC- 2031990)	The Hardware Specification describes the device in sufficient detail so that a hardware designer can design a board or system utilizing this device. The intended audience of the Hardware Specification is hardware designers who are using the device in their designs.
Hardware Design Guide (PMC- 2031949)	The Hardware Design Guide provides additional board level design information. The Hardware Design Guide is written for hardware designers who are using the device in their designs. Note that there may also be other guides that assist with programming of the device.
Register Descriptions (PMC- 2040080)	The Register Descriptions describes all of the registers used in the device. This document is provided for designers who are building software interfaces.

1 Introduction

This Product Overview describes the features and applications of the PMC-Sierra HDLIU 32.

In order to understand the information in this document, the reader should have a strong working understanding of T1 and E1.

1.1 Standards References

Remember that PMC-Sierra products are only one part of your unique system. Ensure that all aspects of your system support standards compliance.

1. ANSI – T1.102-1993 – American National Standard for Telecommunications – Digital Hierarchy – Electrical Interfaces.

2. ANSI – T1.107-1995 – American National Standard for Telecommunications – Digital Hierarchy – Formats Specification.

3. ANSI – T1.403-1999 – American National Standard for Telecommunications – Carrier to Customer Installation – DS-1 Metallic Interface Specification.

4. ANSI – T1.408-1990 – American National Standard for Telecommunications – Integrated Services Digital Network (ISDN) Primary Rate – Customer Installation Metallic Interfaces Layer 1 Specification.

5. AT&T – TR 62411 – Accunet T1.5 – Service Description and Interface Specification, December 1990.

6. AT&T – TR 62411 – Accunet T1.5 – Service Description and Interface Specification, Addendum 1, March 1991.

7. AT&T – TR 62411 – Accunet T1.5 – Service Description and Interface Specification, Addendum 2, October 1992.

8. TR-TSY-000170 – Bellcore – Digital Cross-Connect System Requirements and Objectives, Issue 1, November 1985.

9. TR-N1WT-000233 – Bell Communications Research – Wideband and Broadband Digital Cross-Connect Systems Generic Criteria, Issue 3, November 1993.

10. TR-NWT-000303 – Bell Communications Research – Integrated Digital Loop Carrier Generic Requirements, Objectives, and Interface, Issue 2, December, 1992.

11. TR-TSY-000499 – Bell Communications Research – Transport Systems Generic Requirements (TSGR): Common Requirement, Issue 5, December, 1993.

12. ETSI – ETS 300 011 – ISDN Primary Rate User-Network Interface Specification and Test Principles, 1992.

13. ETSI – ETS 300 233 – Access Digital Section for ISDN Primary Rates.

14. ETSI – CTR 4 – Integrated Services Digital Network (ISDN); Attachment requirements for terminal equipment to connect to an ISDN using ISDN primary rate access, November 1995.

15. ETSI – CTR 12 – Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2 048 kbit/s digital unstructured leased lines (D2048U) Attachment requirements for terminal equipment interface, December 1993.

16. ETSI – CTR 13 – Business Telecommunications (BTC); 2 048 kbit/s digital structured leased lines (D2048S); Attachment requirements for terminal equipment interface, January 1996.

17. FCC Rules – Part 68.308 – Signal Power Limitations.

18. ITU-T – Recommendation G.703 – Physical/Electrical Characteristics of Hierarchical Digital Interface, Geneva, 1998.

19. ITU-T – Recommendation G.704 – Synchronous Frame Structures Used at Primary Hierarchical Levels, July 1998.

20. ITU-T Recommendation G.772 – Protected Monitoring Points Provided on Digital Transmission Systems, 1992.

21. ITU-T – Recommendation G.775 – Loss of Signal (LOS), November 1998.

22. ITU-T Recommendation G.823, - The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy, 1993.

23. ITU-T – Recommendation I.431 – Primary Rate User-Network Interface – Layer 1 Specification, 1993.

24. ITU-T Recommendation O.151, - Error Performance Measuring Equipment For Digital Systems at the Primary Bit Rate and Above, 1992.

25. TTC Standard JT-G703 – Physical/Electrical Characteristics of Hierarchical Digital Interfaces, 1995.

26. TTC Standard JT-G704 – Frame Structures on Primary and Secondary Hierarchical Digital Interfaces, 1995.

27. TTC Standard JT-I431 – ISDN Primary Rate User-Network Interface Layer 1 – Specification, 1995.

28. Nippon Telegraph and Telephone Corporation – Technical Reference for High-Speed Digital Leased Circuit Services, Third Edition, 1990.

29. ITU-T Recommendation G.824, The Control of Jitter and Wander within Digital Networks which are based on the 1544 kbit/s Hierarchy (March 1993).

30. PMC-Sierra, Inc. *Saturn Compatible Scaleable Bandwidth Interface (SBI) Specification*. PMC-1980577. Issue 3, 1998

31. Electronic Industries Association. Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device): EIA/JESD51. December 1995.

32. Electronic Industries Alliance 1999. Integrated Circuit Thermal Test Method Environmental Conditions -Junction-to-Board: JESD51-8. October 1999.

33. Telcordia Technologies. Network Equipment-Building System (NEBS) Requirements: Physical Protection: Telcordia Technologies Generic Requirements GR-63-CORE. Issue 1. October 1995.

34. SEMI (Semiconductor Equipment and Materials International). SEMI G30-88 Test Method for Junction-to-Case Thermal Resistance Measurements of Ceramic Packages. 1988.

35. IEEE. 1149.1b-1994 IEEE Standard Test Access Port and Boundary-Scan Architecture. Sept 22, 1994

2 Product Applications

2.1 T1/E1 Tributary Line Application

Figure 1 and Figure 2 shows how the HDLIU 32 can be used together with the TEMAP 84 (PM5366) or TEMAP 28 (PM5341) in T1 and E1 tributary card application, respectively.

Figure 1 T1 Tributary Card Application

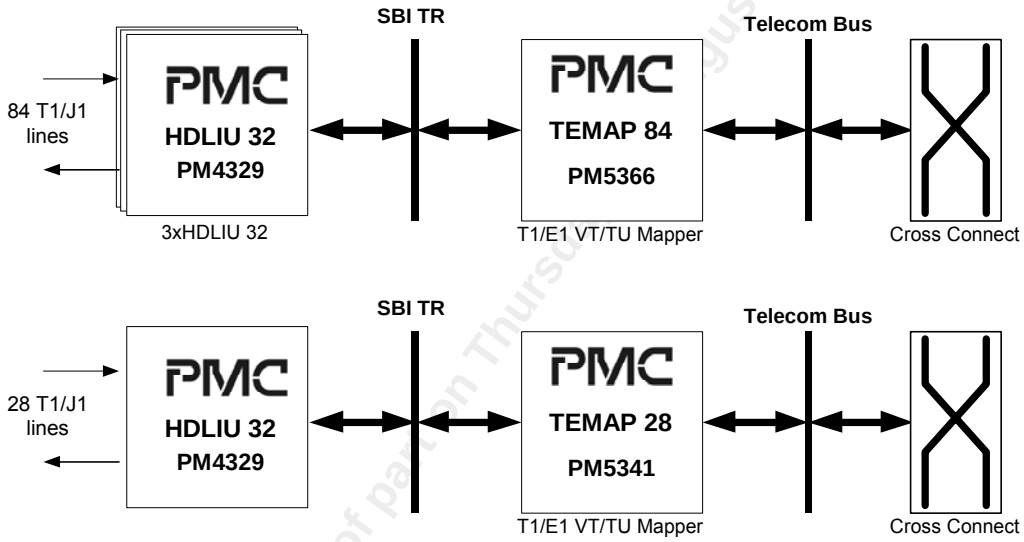
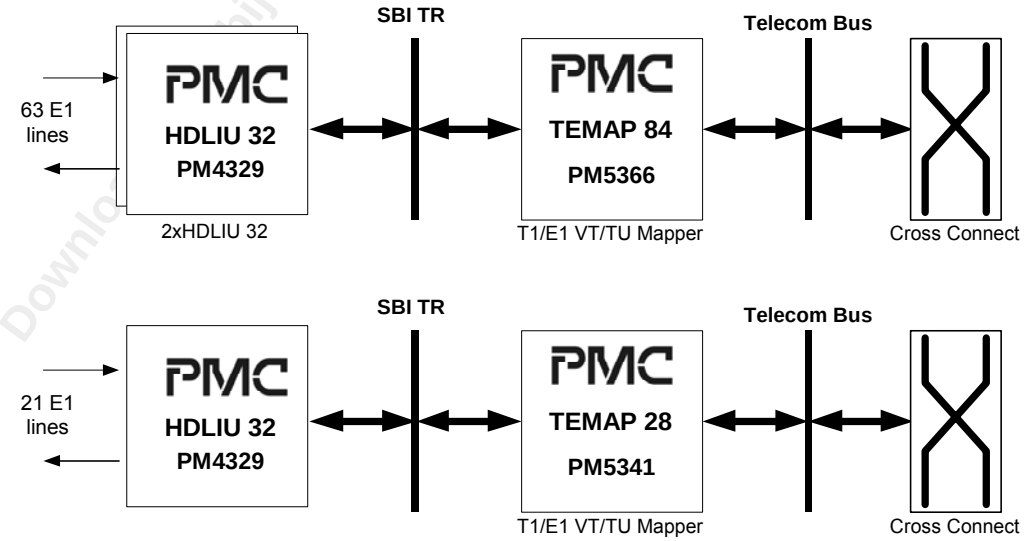
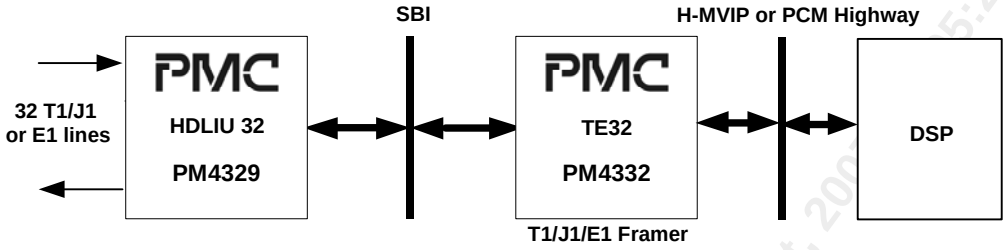


Figure 2 E1 Tributary Card Application



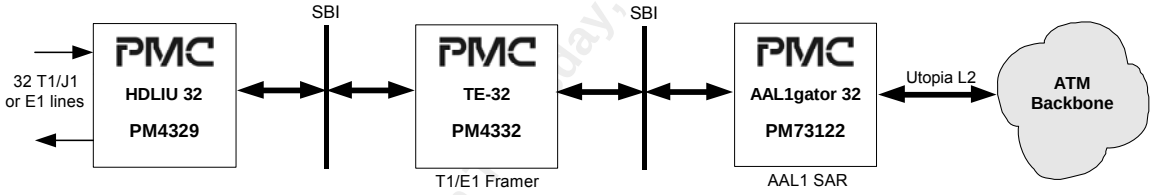
2.2 Voice Gateway

Figure 3 Voice Gateway



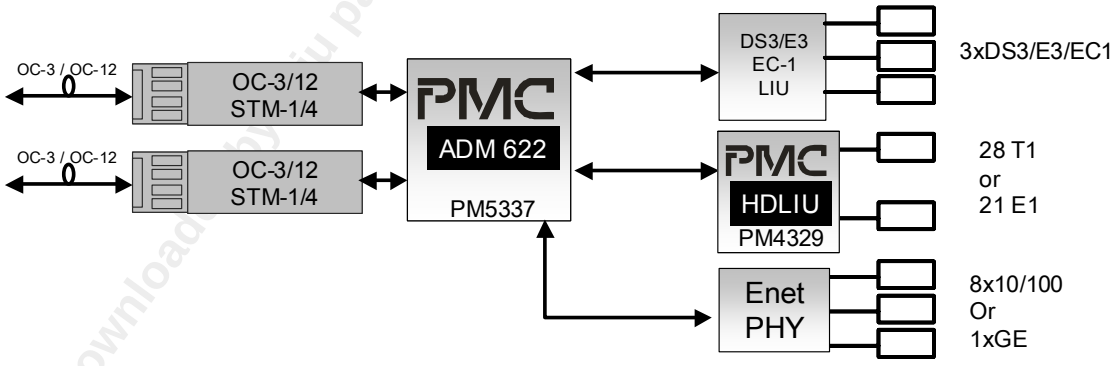
2.3 High Density Leased Line Circuit Emulation Application

Figure 4 High Density Leased Line Circuit Emulation

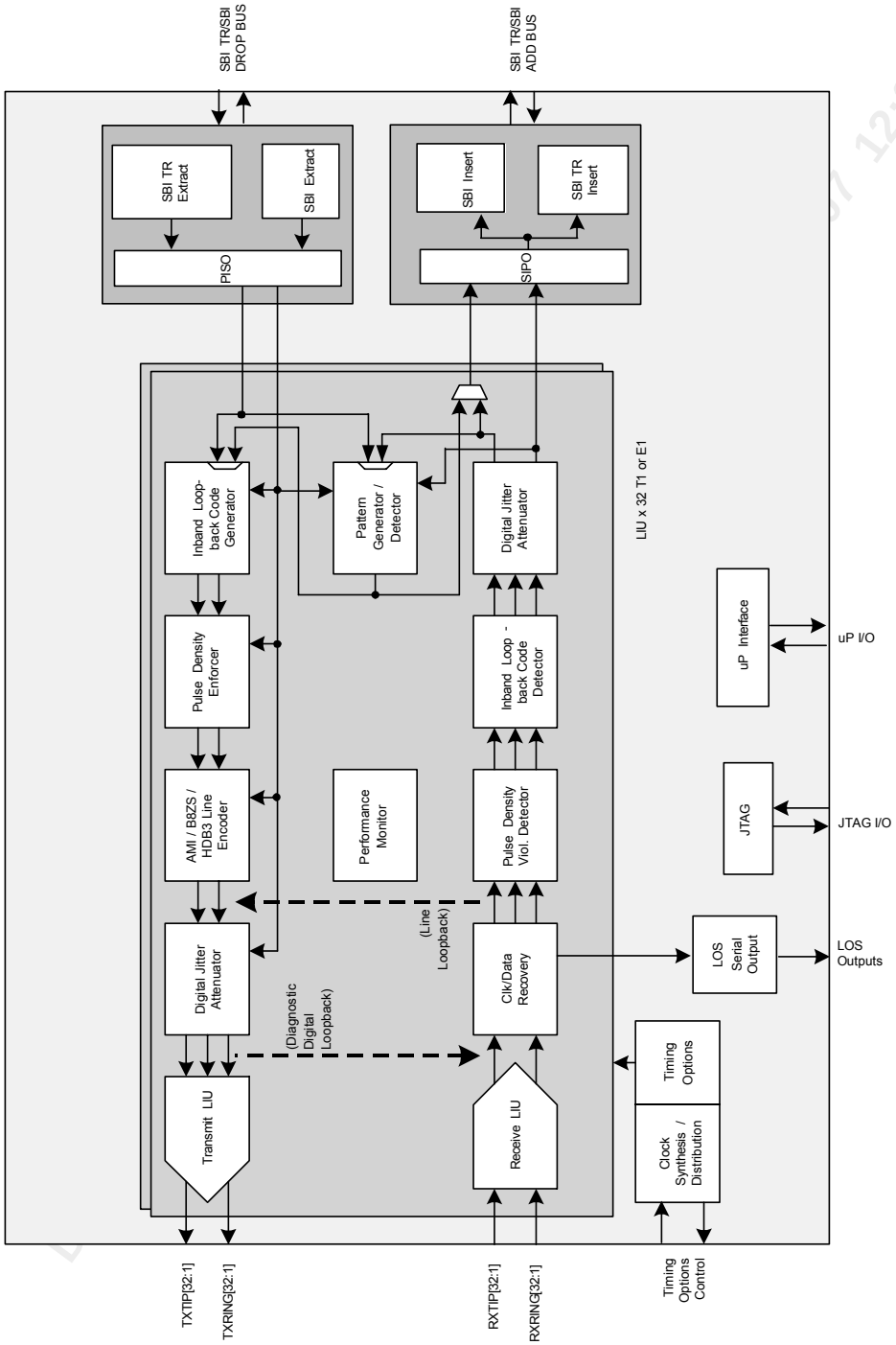


2.4 Integrated Add/Drop Multiplexer for 155Mbps & 622Mbps

Figure 5 Integrated Add/Drop Multiplexer for 155Mbps & 622Mbps



3 Block Diagram



4 Product Features

The following table shows a feature comparison of the PM4329 HDLIU 32 and the existing PM4323 OCTLIU LT and PM4235 OCTLIU ST.

Table 1 LIU Feature Comparison

Category	Feature	PM4323 OCTLIU LT	PM4235 OCTLIU ST	PM4329 HDLIU 32
General Features				
	Number of T1/J1/E1line interface units.	8	8	32
	Optional encoding/decoding of B8ZS, HDB3 and AMI line codes per E1/T1 link.	Yes	Yes	Yes
	Provides receive equalization, clock recovery and line performance monitoring.	Yes	Yes	Yes
	Provides receive and transmit clock jitter attenuation.	Yes	Yes	Yes
	Provides a selectable, de-jittered T1 or E1 recovered output clock for system timing and redundancy.	Yes	Yes	Yes
	Provides per link PRBS generator and detector for error testing at DS1 and E1 rates as recommended in ITU-T 0.151.	Yes	Yes	Yes
	Register configurable support for 19.44MHz SBI bus. Converts serial unchannelized T1/E1 links into 19.44MHz SBI bus format (with mapping). Converts to links from 19.44MHz SBI bus into serial link (with mapping).	Yes	Yes	Yes
	Register configurable support for 19.44MHz SBI TR bus. Converts serial unchannelized T1/E1 links into 19.44MHz SBI TR bus format (with mapping). Converts to links from 19.44MHz SBI TR bus into serial link (with mapping).	Yes	Yes	Yes
	Serial Clock and Data I/O	Yes	Yes	No
	Provides an IEEE 1149.1 JTAG compliant Test Access Port and controller for boundary scan test of the digital I/O.	Yes	Yes	Yes

Category	Feature	PM4323 OCTLIU LT	PM4235 OCTLIU ST	PM4329 HDLIU 32
	Able to use the same board components for T1 100Ω and E1 120Ω mode.	Yes	Yes	Yes
	Mixed E1 and T1 links	No, all 8 links must be either T1 or E1.	No, all 8 links must be either T1 or E1.	Partially. All 16 links in each half (1-16 or 17-32) must be either T1 or E1. Each half is independent of each other. Requires external termination.
	8-bit microprocessor interface for configuration, control and status monitoring.	Multiplexed or non multiplexed address/data bus	Multiplexed or non multiplexed address/data bus	Multiplexed address/data bus
	Provides a hardware only (no microprocessor) mode in which configuration data is read from an SPI-compatible serial PROM.	Yes	Yes	No
RX Feature				
	Programmable internal termination for Rx.	No, requires external termination	No, requires external termination	Yes, for T1 100Ω and E1 120Ω, external termination required for E1 75Ω
	Typical T1/E1 signal recovery using PIC 22 gauge cable emulation	43dB for T1 39dB for E1	12dB	24dB for T1 22dB for E1
	Guaranteed minimum T1/E1 signal recovery using PIC 22 gauge cable emulation	36dB	12dB	17dB for T1 16dB for E1
	Requires RX RAM tables	Yes	Yes	No
	Supports G.772 compliant non-intrusive protected monitoring points	Yes	Yes	Yes, requires specific external board components.
	Recovers clocks and data using a digital phase locked loop for high jitter performance.	Yes	Yes	Yes
	Tolerates more than 0.4 UI peak-to-peak; high frequency jitter as required by AT&T TR 62411 and Bellcore TR-TSY-000170.	Yes	Yes	Yes
	Performs B8ZS or AMI decoding when processing a bipolar DS-1 signal and HDB3 or AMI decoding when processing a bipolar E1 signal.	Yes	Yes	Yes

Category	Feature	PM4323 OCTLIU LT	PM4235 OCTLIU ST	PM4329 HDLIU 32
	Detects line code violations (LCVs), B8ZS/HDB3 line code signatures, and 4 (e1), 8 (T1+B8ZS) or 16(T1 AMI) successive zeros.	Yes	Yes	Yes
	Accumulates up to 8191 line code violations over an interval defined by the period between software write accesses to the LCV register for performance monitoring.	Yes	Yes	Yes
	Detects loss of signal (LOS), which is defined as 10, 15, 31, 63, or 175 successive zeros.	Yes	Yes	Yes
	Detects programmable inband loopback activate and deactivate code sequences received in the DS-1 data stream when they are present for 5.1 seconds. Optionally, enters loopback mode automatically on detection of an inband loopback code.	Yes	Yes	Yes
	Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window.	Yes	Yes	Yes
	The receiver inputs and transmitter outputs are tri-stated when the low voltage power supply (1.8V) is not connected. The AVD 3.3V supply must still be connected.	Yes	Yes	Yes
	TLIU Monitoring. Ability to monitor the TXTIP/TXRING pins, on each port, to check for activity, using the RLIU (on the redundant device via the TLIU TXTIP/TXRING pins).	No	No	Yes
	Requires external FETs to control impedance switching for work and protect redundancy applications	Yes, FET are required to switch the redundant Rx termination	Yes, FET are required to switch the redundant Rx termination	No, termination switched internally, except in E1 75Ω (which requires external termination/ impedance matching).
TX Feature				
	Current or Voltage mode	Current	Current	Voltage
	Internal termination for TLIU	No, requires external termination	No, requires external termination	Yes, provided for E1 120Ω. No termination required for T1 as per short haul T1 spec.
	Supports single rail PCM and signaling data from 1.544 Mbits/s and 2.048	Yes	Yes	Yes

Category	Feature	PM4323 OCTLIU LT	PM4235 OCTLIU ST	PM4329 HDLIU 32
	Mbits/s backplane buses.			
	Generates DSX-1 short haul pulses with programmable pulse shape compatible with AT&T, ANSI and ITU requirements.	Yes	Yes	Yes
	Generates DSX-1 long haul pulses with programmable pulse shape compatible with AT&T, ANSI and ITU requirements.	Yes	No	No
	Number of pulse template waveforms that can be stored on chip in internal memory per LIU.	12	12	1
	Internal pulse template memory is initialized to predefined templates.	Yes (12) T1.102 (LBO 0dB) T1.102 (LBO 7.5dB) T1.102 (LBO 15dB) T1.102 (LBO 22.5dB) T1.102 (0-110 ft) T1.102 (110-220 ft) T1.102 (220-330 ft) T1.102 (330-440 ft) T1.102 (440-550 ft) T1.102 (550-660 ft) E1 120 Ω E1 75 Ω	Yes (8), T1.102 (0-110 ft) T1.102 (110-220 ft) T1.102 (220-330 ft) T1.102 (330-440 ft) T1.102 (440-550 ft) T1.102 (550-660 ft) E1 120 Ω E1 75 Ω	No
	Generates E1 pulses compliant to G.703 recommendations.	Yes	Yes	Yes
	Provides a digitally programmable pulse shape extending up to 5 transmitted bit periods for custom long haul pulse shaping applications.	Yes	No, only 2 UI is required for short haul	No, only 2 UI is required for short haul
	Provides line outputs that are voltage limited and may be tristated for protection or in redundant applications	No, outputs are current limited (not voltage limited) but they can still be tri-stated (but require external FETs to tri-state the termination if transformer is on line card).	No, outputs are current limited (not voltage limited) but they can still be tri-stated (but require external FETs to tri-state the termination if transformer is on line card).	Yes
	Provides a digital phase locked loop for generation of a low jitter transmit clock complying with all jitter attenuation, jitter transfer and residual jitter specifications of AT&T TR62411 and ETSI TBR 12 and TBR 13.	Yes	Yes	Yes
	Allows bipolar violation transparent operation for error restoring regenerator applications	Yes	Yes	Yes

Category	Feature	PM4323 OCTLIU LT	PM4235 OCTLIU ST	PM4329 HDLIU 32
	Allows bipolar violation insertion for diagnostic testing purposes.	Yes	Yes	Yes
	Supports all ones transmission for alarm indication signal generation.	Yes	Yes	Yes
	Performs B8ZS or AMI decoding when processing a DS-1 signal and HDB3 or AMI decoding when processing an E1 signal.	Yes	Yes	Yes
	Detects violations of the ANSI T1.403 12.5% pulse density rule over a, moving 192-bit window and optionally stuffs ones to maintain minimum ones density.	Yes	Yes	Yes
	Supports transmission of a programmable unframed inband loopback code sequence.	Yes	Yes	Yes
	Able to drive arbitrary lengths of unterminated cable/twisted pair without undue thermal stress. (i.e. 140' of cable)	No	No	Yes
Standards				
	MeetsT1/J1 and E1 network access specifications including:	Long Haul : ANSI T1.102 ANSI T1.403 ANSI T1.408 AT&T TR62411 ITU-T G.703 ITU-T G.704 ETSI 300-011 TBR 4 TBR 12 TBR 13	Short Haul : ANSI T1.102 AT&T TR62411 ITU-T G.703 ITU-T G.704 ETSI 300-011 TBR 4 TBR 12 TBR 13	Short Haul : ANSI T1.102 AT&T TR62411 ITU-T G.703 ITU-T G.704 ETSI 300-011 TBR 4 TBR 12 TBR 13
System Features				
	When used in conjunction with TEMAP 84 and TEMAP 28, the system must meet: GR253 GR496 G.783	Yes	Yes	Yes
Package		Available in a high density 288 pin Tape-SBGA (23mm x 23mm)	Available in a high density 288 pin Tape-SBGA (23mm x 23mm)	Available in a high density 276-pin L2BGA (27mm x 27mm)

Category	Feature	PM4323 OCTLIU LT	PM4235 OCTLIU ST	PM4329 HDLIU 32
Power		Implemented in a low power 3.3V	Implemented in a low power 3.3V	Implemented in a low power 3.3V

5 Datapath

5.1 Line Interface Unit

The HDLIU 32 has two independent Clock Synthesis Units which each clock 16 LIUs; LIUs #1 to #16 use CSU#1; LIUs #17 to #32 use CSU#2. The 16x LIU groups (1-16 and 17-32) can be configured to operate in either E1 or T1 mode.

5.2 Receive Interface

The analog receive interface is configurable to operate in both E1 and T1 short-haul applications. Analog circuitry is provided to allow direct reception of short haul E1 and T1 compatible signals with typically up to 22dB cable loss (at 1.024 MHz) in E1 mode or typically up to 24dB cable loss (at 772 kHz) in T1 mode using a minimum of external components. External termination resistors are not required for both E1 120Ω mode and T1 mode.

5.3 Clock and Data Recovery (CDRC)

The Clock and Data Recovery function is provided by the Clock and Data Recovery (CDRC) block. The CDRC provides clock and PCM data recovery, B8ZS and HDB3 decoding, line code violation detection, and loss of signal detection. It recovers the clock from the incoming RZ data pulses using a digital phase-locked-loop and reconstructs the NRZ data. Loss of signal is indicated after a programmable threshold of consecutive bit periods of the absence of pulses on both the positive and negative line pulse inputs and is cleared after the occurrence of a single line pulse. An alternate loss of signal indication is provided which is cleared upon meeting a 1-in-8 pulse density criteria for T1 and a 1-in-4 pulse density criteria for E1. If enabled, a microprocessor interrupt is generated when a loss of signal is detected and when the signal returns. A line code violation is defined as a bipolar violation (BPV) for AMI-coded signals, is defined as a BPV that is not part of a zero substitution code for B8ZS-coded signals, and is defined as a bipolar violation of the same polarity as the last bipolar violation for HDB3-coded signals.

In T1 mode, the input jitter tolerance of the HDLIU 32 complies with the Bellcore Document TA-TSY-000170 and with the AT&T specification TR62411. The tolerance is measured with a QRSS sequence (2^{20}-1 with 14 zero restriction).

For E1 applications, the input jitter tolerance complies with the ITU-T Recommendation G.823 “The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy.”

5.4 Receive Jitter Attenuator (RJAT)

The Receive Jitter Attenuator (RJAT) digital PLL attenuates the jitter present on the RXTIP/RXRING inputs.

The jitter characteristics of the Receive Jitter Attenuator (RJAT) are the same as the Transmit Jitter Attenuator (TJAT).

5.5 T1 Inband Loopback Code Detector (IBCD)

The T1 Inband Loopback Code Detection function is provided by the IBCD block. This block detects the presence of either of two programmable INBAND LOOPBACK ACTIVATE and DEACTIVATE code sequences in the receive data stream. Each INBAND LOOPBACK code sequence is defined as the repetition of the programmed code in the PCM stream for at least 5.1 seconds. The detection algorithm tolerates more than the minimum number of discrepancy bits in order to detect framed PCM data in the presence of a 10^{-2} bit error rate. The code sequence detection and timing is compatible with the specifications defined in T1.403-1993, TA-TSY-000312, and TR-TSY-000303. LOOPBACK ACTIVATE and DEACTIVATE code indication is provided through internal register bits. An interrupt is generated to indicate when either code status has changed.

5.6 T1 Pulse Density Violation Detector (PDVD)

The Pulse Density Violation Detection function is provided by the PDVD block. The block detects pulse density violations of the requirement that there be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23). The PDVD also detects periods of 16 consecutive zeros in the incoming data. Pulse density violation detection is provided through an internal register bit. An interrupt is generated to signal a 16 consecutive zero event, and/or a change of state on the pulse density violation indication.

5.7 Performance Monitor Counters (PMON)

The Performance Monitor block accumulates line code violation events with a saturating counter over consecutive intervals as defined by the period between writes to trigger registers (typically 1 second). When the trigger is applied, the PMON transfers the counter value into holding registers and resets the counter to begin accumulating events for the interval. The counter is reset in such a manner that error events occurring during the reset are not missed.

5.8 Pseudo Random Binary Sequence Generation and Detection (PRBS)

The Pseudo Random Binary Sequence Generator/Detector (PRBS) block is a software selectable PRBS generator and checker for 2^{11}-1, 2^{15}-1 or 2^{20}-1 PRBS polynomials for use in the T1 and E1 links. PRBS patterns may be generated and detected in either the transmit or receive directions.

5.9 T1 Inband Loopback Code Generator (XIBC)

The T1 Inband Loopback Code Generator (XIBC) block generates a stream of inband loopback codes (IBC) to be inserted into a T1 data stream. The IBC stream consists of continuous repetitions of a specific code. The contents of the code and its length are programmable from 3 to 8 bits.

5.10 Pulse Density Enforcer (XPDE)

The Pulse Density Enforcer function is provided by the XPDE block. This block monitors the digital output of the transmitter and detects when the stream is about to violate the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window. If a density violation is detected, the block can be enabled to insert a logic 1 into the digital stream to ensure the resultant output no longer violates the pulse density requirement. When the XPDE is disabled from inserting logic 1s, the digital stream from the transmitter is passed through unaltered.

5.11 Transmit Jitter Attenuator (TJAT)

The Transmit Jitter Attenuation function is provided by a digital phase lock loop and 80-bit deep FIFO. The depth of the 80-bit FIFO is fully programmable; to allow the depth to be optimized for low latency applications.

The jitter attenuator generates the jitter-free 1.544 MHz or 2.048 MHz Transmit clock output by adjusting the Transmit clock's phase in 1/96 UI increments to minimize the phase difference between the generated Transmit clock and input data clock to TJAT. Jitter fluctuations in the phase of the input data clock are attenuated by the phase-locked loop within TJAT so that the frequency of Transmit clock is equal to the average frequency of the input data clock. For T1 applications, to best fit the jitter attenuation transfer function recommended by TR 62411, phase fluctuations with a jitter frequency above 5.7 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 5.7 Hz are tracked by the generated Transmit clock. In E1 applications, the corner frequency is 7.6 Hz. To provide a smooth flow of data out of TJAT, the Transmit clock is used to read data out of the FIFO.

5.12 Line Transmitter

The line transmitter generates Alternate Mark Inversion (AMI) transmit pulses suitable for use in the DSX-1 (short haul T1) and short haul E1 environments.

The output pulse shape is synthesized digitally with digital-to-analog (DAC) converters. The DAC's produce differential bipolar outputs that directly drive the TXTIP[32:1] and TXRING[32:1] pins. The output is applied to a line-coupling transformer in a differential manner, which when viewed from the line side of the transformer produce the output pulses at the required levels and ensures a small positive to negative pulse imbalance.

The pulse shape is user programmable. For T1 short haul, the cable length between the HDLIU 32 and the cross-connect (where the pulse template specifications are given) greatly affects the resulting pulse shapes. Hence, the data applied to the converter must account for different cable lengths. For CEPT E1 applications the pulse template is specified at the transmitter, thus only one setting is required.

5.13 Timing Options (TOPS)

The Timing Options block provides a means of selecting the source of the internal input clock to the TJAT block, and the reference clock for the TJAT digital PLL.

5.14 Scaleable Bandwidth Interconnect Transport (SBI TR) Interface

The Scaleable Bandwidth Interconnect Transport (SBI TR) Bus is a synchronous, time-division multiplexed bus designed to transfer, in a pin-efficient manner, data belonging to a number of independently timed links of varying bandwidth. The bus is timed to a reference 19.44MHz clock, a 2 kHz (or fraction thereof) frame pulse and synchronization pulse. All sources and sinks of data on the bus are timed to the reference clock, frame pulse and synchronization pulse.

The SBI TR Bus is a parallel bus that can be used as alternative to SBI in applications where latency is of concern. The SBI TR is used to transfer link information consisting of data, alarm and link rate information with minimum latency.

The multiplexed links are separated into three groups. Each group may be configured independently to carry up to 28 T1/J1s or 21 E1s. The HDLIU 32 may be configured to use any 32 T1/J1 or E1 tributaries from any of the three groups.

5.15 Scaleable Bandwidth Interconnect (SBI) Interface

The Scaleable Bandwidth Interconnect is a synchronous, time-division multiplexed bus designed to transfer, in a pin-efficient manner, data belonging to a number of independently timed links of varying bandwidth. The bus is timed to a reference 19.44MHz clock and a 2 kHz (or fraction thereof) frame pulse. All sources and sinks of data on the bus are timed to the reference clock and frame pulse.

The SBI multiplexing structure is modeled on the SONET/SDH standards. The SONET/SDH virtual tributary structure is used to carry T1/J1 and E1 links.

The multiplexed links are separated into three Synchronous Payload Envelopes (SPE). Each envelope may be configured independently to carry up to 28 T1/J1s or 21 E1s. The HDLIU 32 may be configured to use any 32 T1/J1 or E1 tributaries from any of the three SPE's.

5.16 SBI Extractor and PISO

The SBI Extract block receives data from the either the SBI or the SBI TR DROP bus and converts it to serial bit streams for transmission. The SBI Extract block may be configured to enable or disable extraction of individual tributaries within the SBI/SBI TR DROP bus. It may also be configured to generate an all-1s output to the transmit LIU when an alarm indication is signaled for a particular tributary via the SBI bus.

5.17 SBI Inserter and SIPO

The SBI Insert block receives serial data from the LIUs and inserts it on the either the SBI or SBI TR ADD bus. The SBI Insert block may be configured to enable or disable transmission of individual tributaries on to the SBI/SBI TR ADD bus.

5.18 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported.

5.19 Microprocessor Interface

The Microprocessor Interface Block provides normal and test mode registers, the interrupt logic, and the logic required to connect to the Serial Processor Interface. The Microprocessor Interface uses a multiplexed address/data bus. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the HDLIU 32.

6 Ordering Information

Part Number	Product Name	Description
PM4329-BI	HDLIU 32	276-Pin L2BGA package
PM4329-BGI	HDLIU 32	276-Pin L2BGA, 27 x 27 x 1.55 mm, 1.00 mm BP (ROHS-Compliant)

Call your PMC-Sierra sales representative for the fully qualified part number.

Glossary

Term	Definition
CDRC	Clock and Data Recovery Unit
CSU	Clock Synthesis Unit
LIU	Line Interface Unit
HDLIU	High Density Line Interface Unit
OCTLIU	Octal Line Interface Unit
IBCD	Inband Code Detector
JAT	Jitter Attenuator
PDVD	Pulse Density Violator Detector
PISO	Parallel In Serial Out
PMON	Performance Monitor
PRBS	Pseudo Random Generator
SBI	Scaleable Bandwidth Interconnect
SBI TR	Scaleable Bandwidth Interconnect Transport
SIPO	Serial In Parallel Out
XIBC	Inband Code Transmitter
XPDE	Pulse Density Enforcer
UIpp	Unit Intervals peak to peak
PRBS	Pseudo Random Binary Sequence

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